INTEGRATED CIRCUITS

DATA SHEET

TDA1517ATW
8 W BTL or 2 × 4 W SE power amplifier

Product specification
Supersedes data of 2001 Feb 14
File under Integrated Circuits, IC01

2001 Apr 17

Philips
Semiconductors

FEATURES

- Requires very few external components
- Flexibility in use: mono Bridge-Tied Load (BTL) and stereo Single-Ended (SE); it should be noted that in stereo applications the outputs of both amplifiers are in opposite phase
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- AC and DC short-circuit safe to ground and V_P
- Electrostatic discharge protection
- Thermal protection
- Reverse polarity safe
- Capable of handling high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA1517ATW is an integrated class-AB output amplifier contained in a plastic heatsink thin shrink small outline package (HTSSOP20). The device is primarily developed for multimedia applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		6	12	18	V
I_{ORM}	repetitive peak output current		–	–	2.5	A
$I_{q(tot)}$	total quiescent current		–	40	80	mA
I_{stb}	standby current		–	0.1	100	μA
SE application						
P_o	output power	THD = 10%; R_L = 4 Ω	–	4	–	W
SVRR	supply voltage ripple rejection	R_S = 0 Ω	46	–	–	dB
α_{cs}	channel separation	R_S = 10 kΩ	40	55	–	dB
$V_{n(o)}$	noise output voltage	R_S = 0 Ω	–	50	–	μV
$\lvert Z_i \rvert$	input impedance		50	–	–	kΩ
BTL application						
P_o	output power	THD = 10%; R_L = 8 Ω	–	8	–	W
SVRR	supply voltage ripple rejection	R_S = 0 Ω	50	–	–	dB
$\lvert \Delta V_{OO} \rvert$	output offset voltage		–	–	150	mV
$V_{n(o)(offset)}$	noise output offset voltage	R_S = 0 Ω	–	70	–	μV
$\lvert Z_i \rvert$	input impedance		25	–	–	kΩ

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1517ATW	HTSSOP20	plastic, heatsink thin shrink small outline package; 20 leads; body width 4.4 mm	SOT527-1

BLOCK DIAGRAM

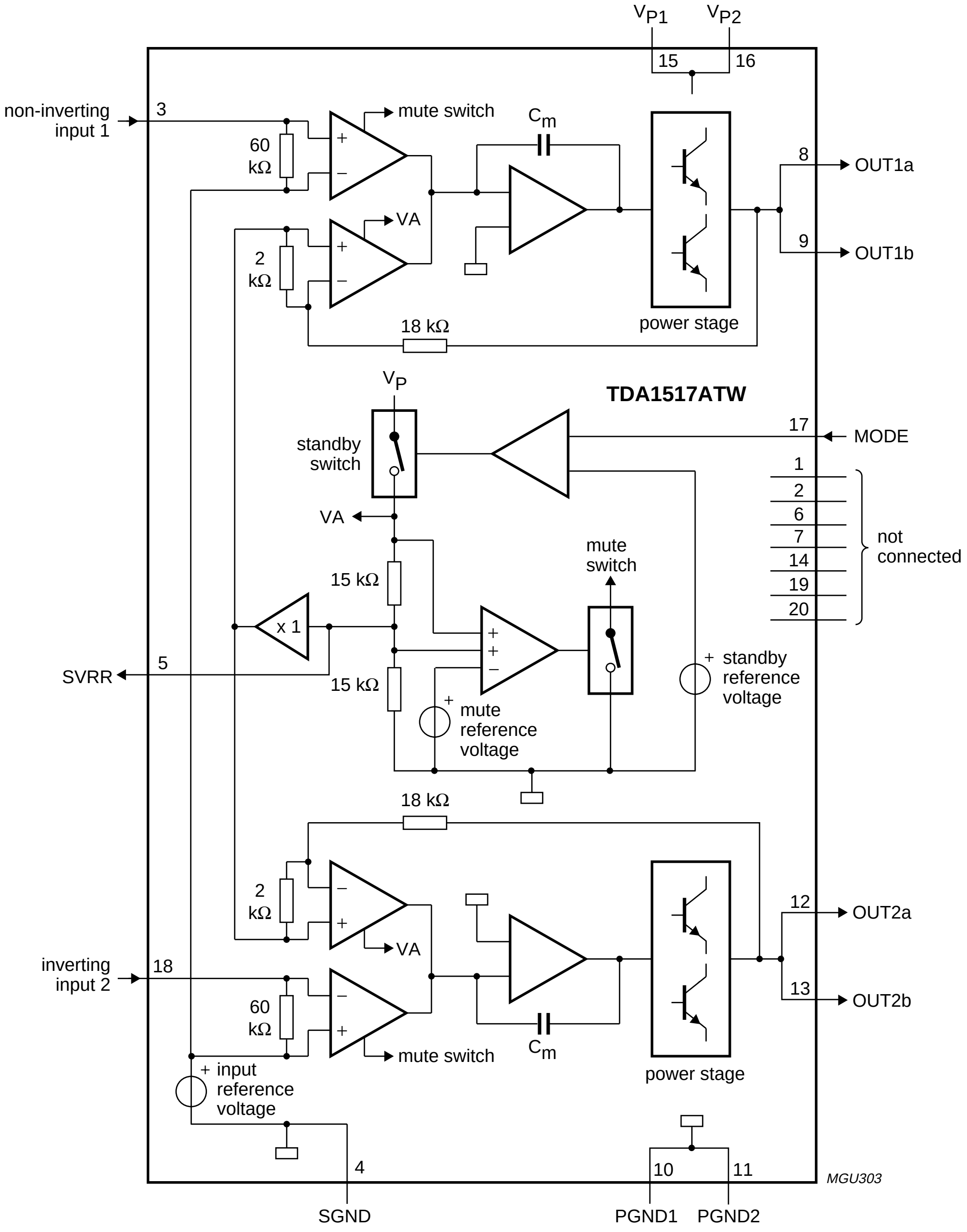


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
IN1+	3	non-inverting input 1
SGND	4	signal ground
SVRR	5	supply voltage ripple rejection
n.c.	6	not connected
n.c.	7	not connected
OUT1a	8	output 1a
OUT1b	9	output 1b
PGND1	10	power ground 1
PGND2	11	power ground 2
OUT2a	12	output 2a
OUT2b	13	output 2b
n.c.	14	not connected
V_{P1}	15	supply voltage 1
V_{P2}	16	supply voltage 2
MODE	17	mode select switch
IN2–	18	inverting input 2
n.c.	19	not connected
n.c.	20	not connected

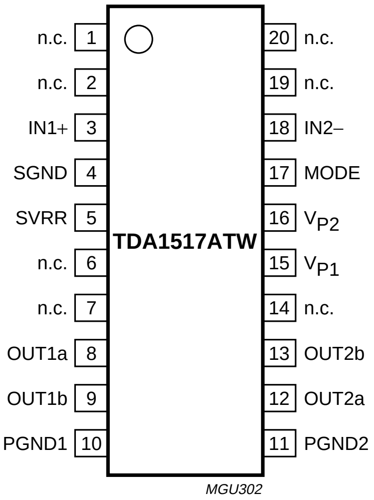


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1517ATW contains two identical amplifiers with differential input stages. This device can be used for Bridge-Tied Load (BTL) or Single-Ended (SE) applications. The gain of each amplifier is fixed at 20 dB. A special feature of this device is the mode select switch. Since this pin has a very low input current (<40 µA), a low cost supply switch can be used. With this switch the TDA1517ATW can be switched into three modes:

- Standby: low supply current
- Mute: input signal suppressed
- Operating: normal on condition.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT.
V_P	supply voltage		–	18	V
V_{PSC}	AC and DC short-circuit-safe voltage		–	18	V
V_{rp}	reverse polarity voltage		–	6	V
ERG_o	energy handling capability at outputs	$V_P = 0$ V	–	200	mJ
I_{OSM}	non-repetitive peak output current		–	4	A
I_{ORM}	repetitive peak output current		–	2.5	A
P_{tot}	total power dissipation		–	5	W
T_{vj}	virtual junction temperature		–	150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
tbf			–	–

DC CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C; measured in Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6.0	12	18	V
I_q	quiescent current	$R_L = \infty$	–	40	80	mA
Operating condition						
$V_{MODE(oper)}$	mode switch voltage level		8.5	–	V_P	V
$I_{MODE(oper)}$	mode switch current	$V_{MODE} = 12$ V	–	15	40	μA
V_O	DC output voltage		–	5.7	–	V
$\lvert\Delta V_{OO}\rvert$	DC output offset voltage		–	–	150	mV
Mute condition						
$V_{MODE(mute)}$	mode switch voltage level		3.3	–	6.4	V
V_O	DC output voltage		–	5.7	–	V
$\lvert\Delta V_{OO}\rvert$	DC output offset voltage		–	–	150	mV
Standby condition						
$V_{MODE(stb)}$	mode switch voltage level		0	–	2	V
I_{stb}	standby current		–	0.1	100	μA

Note

1. The circuit is DC adjusted at $V_P = 6$ to 18 V and AC operating at $V_P = 8.5$ to 18 V.

AC CHARACTERISTICS

V_P = 12 V; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SE application; note 1						
P_o	output power	note 2				
		THD = 1%	2.5	3.3	–	W
		THD = 10%	3	4	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
$f_{ro(L)}$	low frequency roll-off	–1 dB; note 3	–	25	–	Hz
$f_{ro(H)}$	high frequency roll off	–1 dB	20	–	–	kHz
G_V	voltage gain		19	20	21	dB
$\lvert \Delta G_V \rvert$	channel balance		–	–	1	dB
SVRR	supply voltage ripple rejection	note 4				
		on	46	–	–	dB
		mute	46	–	–	dB
		standby	80	–	–	dB
$\lvert Z_i \rvert$	input impedance		50	60	75	kΩ
$V_{n(o)(rms)}$	noise output voltage (RMS value)	note 5				
		on; R_S = 0 Ω	–	50	–	μV
		on; R_S = 10 kΩ	–	70	100	μV
		mute; note 6	–	50	–	μV
α_{cs}	channel separation	R_S = 10 kΩ	40	55	–	dB
$V_{o(mote)}$	output voltage in mute	note 7	–	–	2	mV
BTL application; note 8						
P_O	output power	note 2				
		THD = 1%	5	6.6	–	W
		THD = 10%	6.5	8.0	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.03	–	%
$f_{ro(L)}$	low frequency roll-off	–1 dB; note 3	–	25	–	Hz
$f_{ro(H)}$	high frequency roll off	–1 dB	20	–	–	kHz
G_V	voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection	note 4				
		on	50	–	–	dB
		mute	50	–	–	dB
		standby	80	–	–	dB
$\lvert Z_i \rvert$	input impedance		25	30	38	kΩ
$V_{n(o)(rms)}$	noise output voltage (RMS value)	note 5				
		on; R_S = 0 Ω	–	70	–	μV
		on; R_S = 10 kΩ	–	100	200	μV
		mute; note 6	–	60	–	μV
$V_{o(mute)}$	output voltage in mute	note 7	–	–	2	mV

Notes to the characteristics

1. R_L = 4 Ω, measured in Fig.4.
2. Output power is measured directly at the output pins of the IC.
3. Frequency response externally fixed.
4. $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); R_S = 0 Ω.
5. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of R_S.
7. $V_i = V_{i(max)}$ = 1 V (RMS).
8. R_L = 8 Ω, measured in Fig.3.

APPLICATION INFORMATION

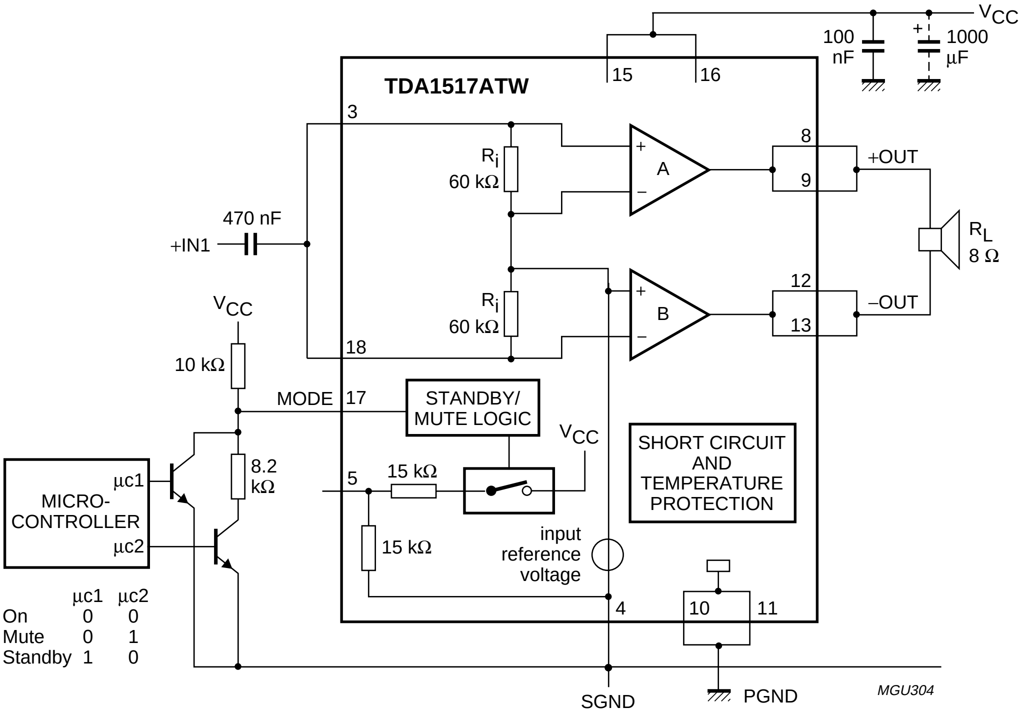


Fig.3 BTL application block diagram.

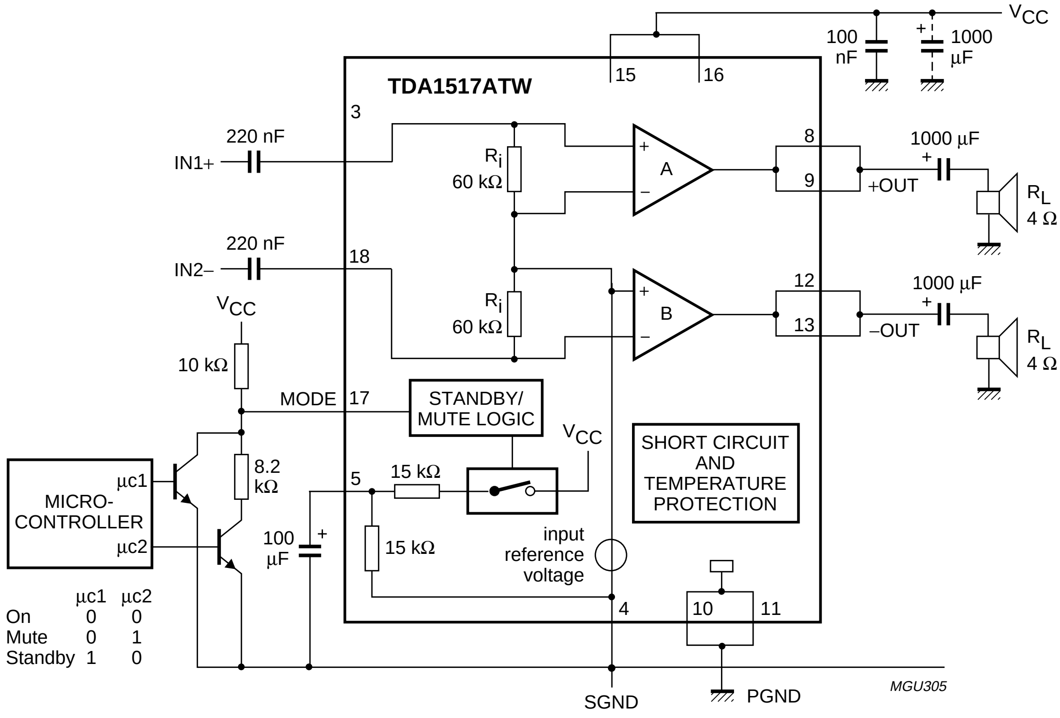


Fig.4 SE application block diagram.

Test conditions

T_{amb} = 25 °C; unless otherwise specified: V_P = 12 V, BTL application, f = 1 kHz, R_L = 8 Ω, fixed gain = 26 dB, audio band-pass: 22 Hz to 22 kHz. In the figures as a function of frequency a band-pass of 10 Hz to 80 kHz was applied.

The BTL application block diagram is shown in Fig.3. The PCB layout [which accommodates both the mono (BTL) and stereo (single-ended) application] is shown in Fig.6.

Printed-Circuit Board (PCB) layout and grounding

For high system performance levels certain grounding techniques are imperative. The input reference grounds have to be tied to their respective source grounds and must have separate traces from the power ground traces; this will separate the large (output) signal currents from interfering with the small AC input signals. The small signal ground traces should be located physically as far as possible from the power ground traces. Supply and output traces should be as wide as possible for delivering maximum output power.

Proper supply bypassing is critical for low noise performance and high power supply rejection. The respective capacitor locations should be as close as possible to the device and grounded to the power ground. Decoupling the power supply also prevents unwanted oscillations. For suppressing higher frequency transients (spikes) on the supply line a capacitor with low ESR (typical 0.1 µF) has to be placed as close as possible to the device. For suppressing lower frequency noise and ripple signals, a large electrolytic capacitor (e.g. 1000 µF or greater) must be placed close to the IC.

In single-ended (stereo) application a bypass capacitor connected to pin SVR reduces the noise and ripple on the midrail voltage. For good THD and noise performance a low ESR capacitor is recommended.

Input configuration

It should be noted that the DC level of the input pins is approximately 2.1 V; a coupling capacitor is therefore necessary.

The formula for the cut-off frequency at the input is as follows: $f_{IC} = \frac{1}{2 \times \pi \times R_i C_i}$

thus $f_{IC} = \frac{1}{2 \times \pi \times 30 \times 10^{-3} \times 470 \times 10^{-9}} = 11\ \text{Hz}$

As can be seen it is not necessary to use high capacitor values for the input; so the delay during switch-on, which is necessary for charging the input capacitors, can be minimized. This results in a good low frequency response and good switch-on behaviour.

In stereo applications (single-ended) coupling capacitors on both input and output are necessary. It should be noted that the outputs of both amplifiers are in opposite phase.

Built-in protection circuits

The IC contains two types of protection circuits:

- Short-circuits the outputs to ground, the supply to ground and across the load: short-circuit is detected and controlled by a SOAR protection circuit
- Thermal shut-down protection: the junction temperature is measured by a temperature sensor. Thermal foldback is activated at a junction temperature of >150 °C.

Output power

The output power as a function of supply voltage has been measured on the output pins and at THD = 10%. The maximum output power is limited by the maximum allowable power dissipation and the maximum available output current, 2.5 A repetitive peak current.

Supply voltage ripple rejection

The SVRR has been measured without an electrolytic capacitor on pin 5 and at a bandwidth of 10 Hz to 80 kHz. The curves for operating and mute condition (respectively) were measured with $R_{source} = 0\ \Omega$. Only in single-ended applications is an electrolytic capacitor (e.g. 100 µF) on pin 5 necessary to improve the SVRR behaviour.

Headroom

A typical music CD requires at least 12 dB (is factor 15.85) dynamic headroom (compared with the average power output) for passing the loudest portions without distortion. The following calculation can be made for this application at $V_P = 12$ V and $R_L = 8\ \Omega$: P_o at THD = 0.1% is approximately 5 W (see Fig.7).

Average listening level without any distortion yields:

$$P_{ALL} = \frac{P_{tot}}{factor} = \frac{5}{15.85} = 315\ \text{mW}$$

The power dissipation can be derived from Fig.11 for 0 dB and 12 dB headroom.

Table 1 Power rating

RATING	HEADROOM	POWER DISSIPATION
$P_o = 5$ W (THD = 0.1%)	0 dB	3.5 W
	12 dB	2.0 W

Thus for the average listening level (music power) a power dissipation of 2.0 W can be used for the thermal PCB calculation; see Section “Thermal behaviour (PCB design considerations)”.

Mode pin

For the 3 functional modes: standby, mute and operate, the MODE pin can be driven by a 3-state logic output stage, e.g. a microcontroller with some extra components for DC-level shifting; see Fig.10 for the respective DC levels.

- Standby mode is activated by a low DC level between 0 and 2 V. The power consumption of the IC will be reduced to <0.12 mW.
- Mute mode is activated by a DC level between 3.3 and 6.4 V. The outputs of the amplifier will be muted (no audio output); however the amplifier is DC biased and the DC level of the output pins stays at half the supply voltage. The input coupling capacitors are charged when in mute mode to avoid pop-noise.
- The IC will be in the operating condition when the voltage at pin MODE is between 8.5 V and V_{CC}.

Switch-on/switch-off

To avoid audible plops during switch-on and switch-off of the supply voltage, the MODE pin has to be set in standby condition (V_{CC} level) before the voltage is applied (switch-on) or removed (switch-off). The input and SVRR capacitors are smoothly charged during mute mode.

The turn-on and turn-off time can be influenced by an RC-circuit connected to the MODE pin. Switching the device or the MODE pin rapidly on and off may cause ‘click and pop’ noise. This can be prevented by proper timing on the MODE pin. Further improvement in the BTL application can be obtained by connecting an electrolytic capacitor (e.g. 100 µF) between the SVRR pin and signal ground.

Thermal behaviour (PCB design considerations)

The typical thermal resistance [$R_{th(j-a)}$] of the IC in the HTSSOP20 package is 37 K/W if the IC is soldered on a printed-circuit board with double sided 35 µm copper with a minimum area of approximately 30 cm^2. The actual usable thermal resistance depends strongly on the mounting method of the device on the printed-circuit board, the soldering method and the area and thickness of the copper on the printed-circuit board.

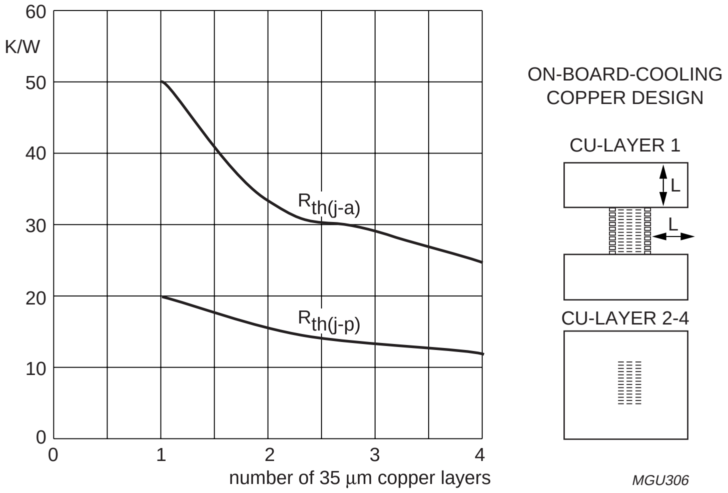
The bottom ‘heat-spreader’ of the IC has to be soldered efficiently on the ‘thermal land’ of the copper area of the printed-circuit board using the re-flow solder technique.

A number of thermal vias in the ‘thermal land’ provide a thermal path to the opposite copper site of the printed-circuit board. The size of the surface layers should be as large as needed to dissipate the heat.

The thermal vias (0.3 mm ∅) in the ‘thermal land’ should not use web construction techniques, because those will have high thermal resistance; continuous connection completely around the via-hole is recommended.

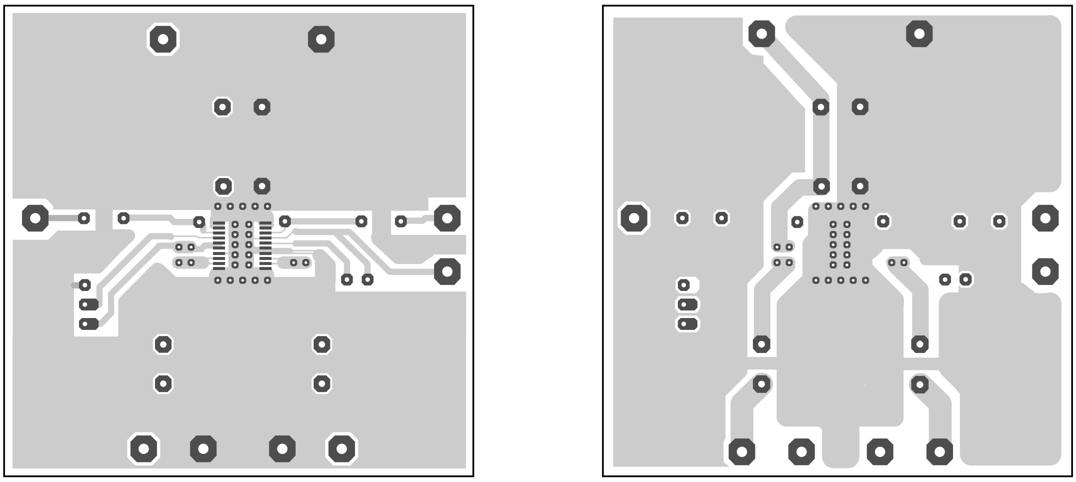
For a maximum ambient temperature of 60 °C the following calculation can be made: for the application at V_P = 12 V and R_L = 8 Ω the (ALL-) music power dissipation approximately 2.0 W;
$T_{j(max)} = T_{amb} + P \times R_{th(j-a)} = 60\ °C + 2.0 \times 37 = 134\ °C$.

Note: the above calculation holds for application at ‘average listening level’ music output signals. Applying (or testing) with sine wave signals will produce approximately twice the music power dissipation; at worst case condition this can activate the maximum temperature protection.



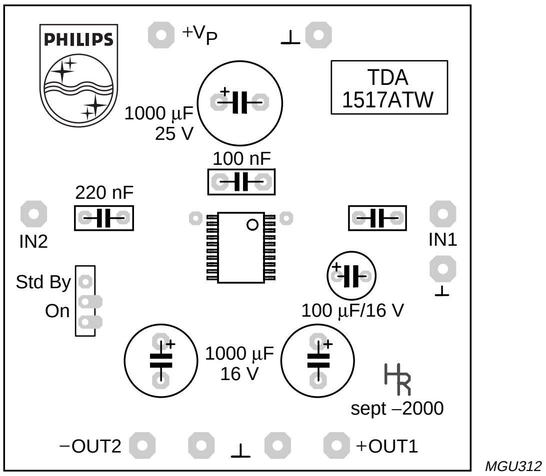
$R_{th(j-p)}$ curve is given for practical calculation purpose.
L = 30 mm plus vias

Fig.5 Thermal resistance of the HTSSOP20 mounted on printed-circuit board.



top view
bottom copper layout

top view
top copper layout



top view
component layout

For BTL applications the two 1000 µF/16 V capacitors must be replaced by 0 Ω jumpers.

Fig.6 Printed-circuit board layout for BTL and SE application.

Typical performance characteristics for BTL application at V_P = 12 V and R_L = 8 Ω

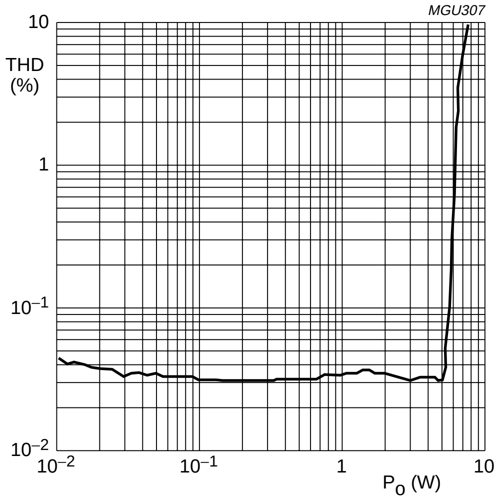


Fig.7 THD as a function of P_o.

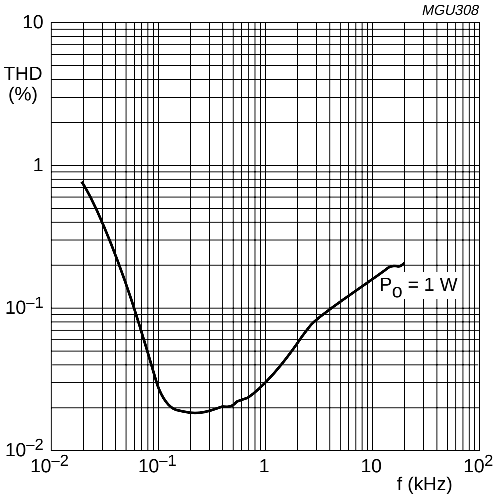


Fig.8 THD as a function of frequency.

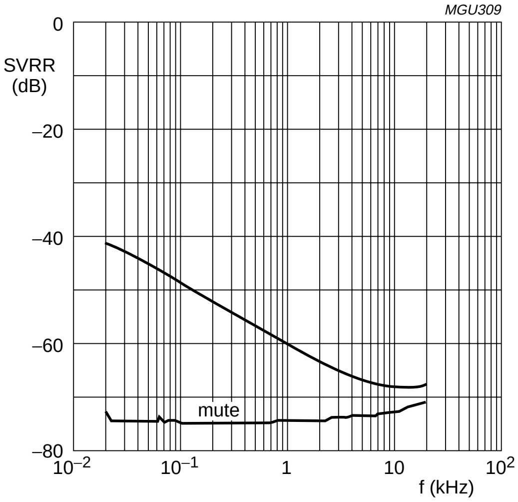


Fig.9 SVRR as a function of frequency.

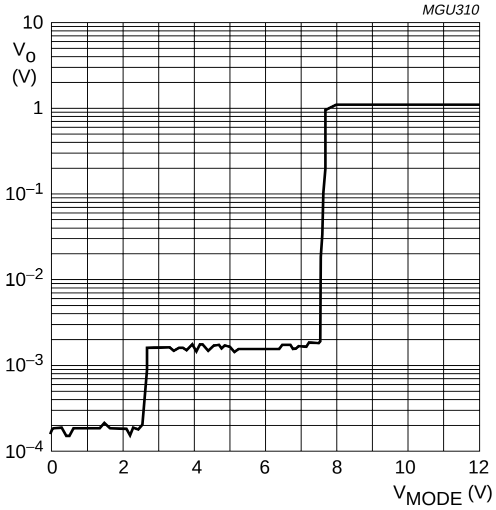


Fig.10 V_o as a function of V_{MODE}.

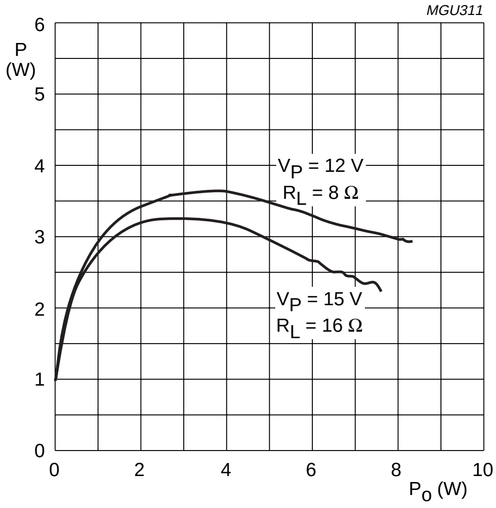


Fig.11 Power dissipation as a function of P_o.

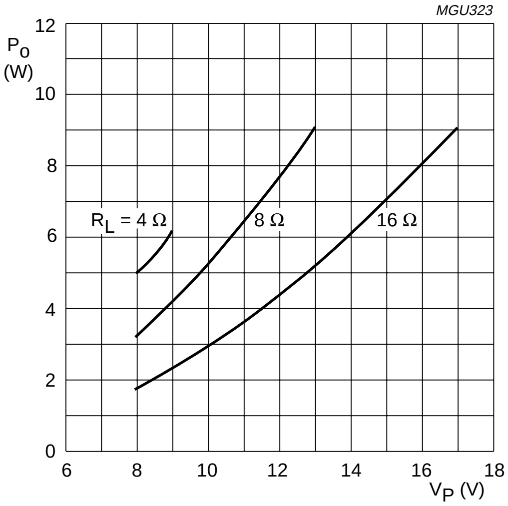
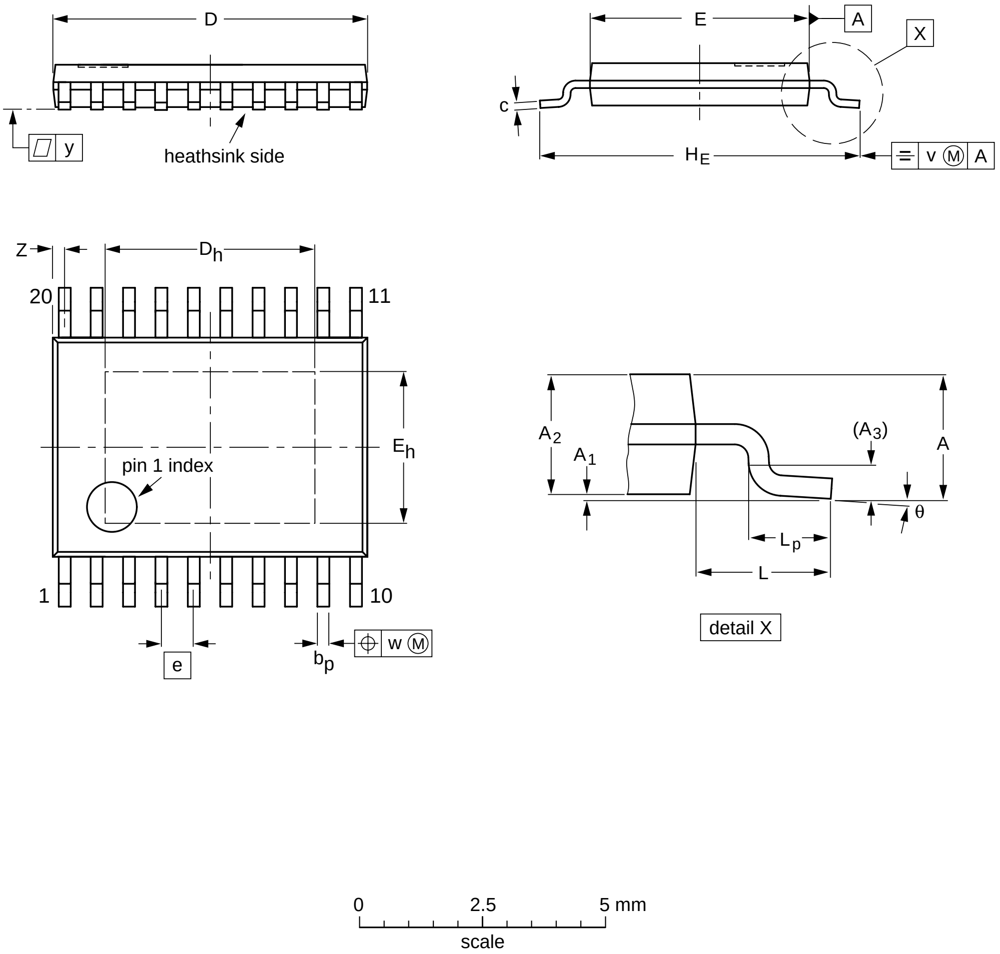


Fig.12 P_o as a function of V_P.

PACKAGE OUTLINE

HTSSOP20: plastic, heatsink thin shrink small outline package; 20 leads; body width 4.4 mm **SOT527-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	D_h	E(2)	E_h	e	H_E	L	L_p	v	w	y	Z(1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.20 0.09	6.6 6.4	4.3 4.1	4.5 4.3	3.1 2.9	0.65	6.6 6.2	1.0	0.75 0.50	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT527-1						~~99-11-12~~ 00-07-12

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[(1)]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS(1)	PRODUCT STATUS(2)	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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