LPC4350/30/20/10

32-bit ARM Cortex-M4/M0 MCU; up to 264 kB SRAM; Ethernet; two High-speed USBs; advanced configurable peripherals

Rev. 1 — 29 October 2010 Objective data sheet

1. General description

The LPC4350/30/20/10 are ARM Cortex-M4 based microcontrollers for embedded applications. The ARM Cortex-M4 is a next generation core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration.

The LPC4350/30/20/10 operate at CPU frequencies of up to 150 MHz. The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point processor is integrated in the core.

The LPC4350/30/20/10 include an ARM Cortex-M0 coprocessor, up to 264 kB of data memory, advanced configurable peripherals such as the State Configurable Timer (SCT) and the Serial General Purpose I/O (SGPIO) interface, two High-speed USB controllers, Ethernet, LCD, an external memory controller, and multiple digital and analog peripherals.

2. Features and benefits

- Cortex-M4 Processor core
  - ARM Cortex-M4 processor, running at frequencies of up to 150 MHz.
  - ARM Cortex-M4 built-in Memory Protection Unit (MPU) supporting eight regions.
  - ARM Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC).
  - Hardware floating-point unit.
  - Non-maskable Interrupt (NMI) input.
  - JTAG and Serial Wire Debug (SWD), serial trace, eight breakpoints, and four watch points.
  - System tick timer.
- Cortex-M0 Processor core
  - ARM Cortex-M0 co-processor capable of off-loading the main ARM Cortex-M4 application processor.
  - Running at frequencies of up to 150 MHz.
  - JTAG, Serial Wire Debug, and built-in NVIC.
- On-chip memory
  - 200 kB SRAM for code and data use.
  - Two 32 kB SRAM blocks with separate bus access. Both SRAM blocks can be powered down individually.
  - 32 kB ROM containing boot code and on-chip software drivers.

- 32 bit One-Time Programmable (OTP) memory for customer use.
- Configurable digital peripherals
  - Serial GPIO (SGPIO) interface.
  - State Configurable Timer (SCT) subsystem on AHB.
- Serial interfaces
  - Quad SPI Flash Interface (SPIFI) with four lanes and up to 40 MB per second.
  - 10/100T Ethernet MAC with RMII and MII interfaces and DMA support for high throughput at low CPU load.
  - One High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip high-speed PHY.
  - One High-speed USB 2.0 Host/Device interface with DMA support, on-chip full-speed PHY and ULPI interface to external high-speed PHY.
  - One 550 UART with DMA support and full modem interface.
  - Three 550 USARTs with DMA and synchronous mode support and a smart card interface conforming to ISO7816 specification. One USART with IrDA interface.
  - One C_CAN 2.0B controller with one channel.
  - Two SSP controllers with FIFO and multi-protocol support. Both SSPs with DMA support.
  - One SPI controller.
  - One Fast-mode Plus I^2C-bus interface with monitor mode and with open-drain I/O pins conforming to the full I^2C-bus specification. Supports data rates of up to 1 Mbit/s.
  - One Fast-mode I^2C-bus interface with monitor mode and with standard I/O pins.
  - Two I^2S interfaces, each with DMA support and with one input and one output.
- Digital peripherals
  - External Memory Controller (EMC) supporting external SRAM, ROM, flash, and SDRAM devices.
  - LCD controller with dedicated DMA controller and a selectable display resolution of up to 1024 $\times$ 768 pixels. Supports monochrome, Super-Twisted Nematic (STN), and Thin-Film Transistor (TFT) panels; supports up to 24-bit true-color mode.
  - Secure Digital Input Output (SDIO) card interface.
  - Eight-channel General-Purpose DMA (GPDMA) controller can access all memories on the AHB and all DMA-capable AHB slaves.
  - Up to 146 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors and open-drain modes.
  - GPIO registers are located on the AHB for fast access. GPIO ports have DMA support.
  - Four general-purpose timer/counters with capture and match capabilities.
  - One motor control Pulse Width Modulator (PWM) for three-phase motor control.
  - One Quadrature Encoder Interface (QEI).
  - Repetitive Interrupt timer (RI timer).
  - Windowed watchdog timer (WWDT).
  - Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
  - Alarm timer; can be battery powered.

- Analog peripherals
  - One 10-bit DAC with DMA support and a data conversion rate of 400 kSamples/s.
  - Two 10-bit ADCs with DMA support and a data conversion rate of 400 kSamples/s. ADC inputs are shared between the two ADCs.
- Security
  - AES decryption engine programmable through an on-chip API.
  - Two 128-bit secure OTP memories for AES key storage and customer use.
  - Unique ID for each device.
- Clock generation unit
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz Internal RC (IRC) oscillator trimmed to 1 % accuracy.
  - Ultra-low power Real-Time Clock (RTC) crystal oscillator.
  - Three PLLs allow CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. The second PLL is dedicated to the High-speed USB, the third PLL can be used as audio PLL.
  - Clock output.
- Power
  - Single 3.3 V (2.2 V to 3.6 V) power supply with on-chip DC-to-DC converter for the core supply and the RTC power domain.
  - RTC power domain can be powered separately by a 3 V battery supply.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Sleep mode via wake-up interrupts from various peripherals.
  - Wake-up from Deep-sleep, Power-down, and Deep power-down modes via external interrupts and interrupts generated by battery powered blocks in the RTC power domain.
  - Brownout detect with four separate thresholds for interrupt and forced reset.
  - Power-On Reset (POR).
  - Available as 256 LBGA package, as 208-pin and 144-pin LQFP packages, and as 180-pin and 100-pin LBGA packages.

3. Applications

- Industrial
- Consumer
- White goods
- RFID readers
- e-Metering

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC4350	LBGA256	plastic low profile ball grid array package; 256 balls; body 17 x 17 x 1 mm	sot740-2
LPC4350	BGA180	<tbd>	<tbd>
LPC4330	LBGA256	plastic low profile ball grid array package; 256 balls; body 17 x 17 x 1 mm	sot740-2
LPC4330	LQFP208	<tbd>	<tbd>
LPC4330	BGA180	<tbd>	<tbd>
LPC4320	LQFP144	<tbd>	<tbd>
LPC4320	BGA100	<tbd>	<tbd>
LPC4310	LQFP144	<tbd>	<tbd>
LPC4310	BGA100	<tbd>	<tbd>

4.1 Ordering options

Table 2. Ordering options

Type number	SRAM	LCD	Ethernet	USB0 (Host/ Device/OTG)	USB1 (Host/ Device)	Package
LPC4350	264 kB	yes	yes	yes	yes	LBGA256
LPC4350	<tbd>	yes	yes	yes	yes	BGA180
LPC4330	<tbd>	no	yes	yes	yes	LBGA256
LPC4330	<tbd>	no	yes	yes	yes	LQFP208
LPC4330	<tbd>	no	yes	yes	yes	BGA180
LPC4320	<tbd>	no	no	yes	no	LQFP144
LPC4320	<tbd>	no	no	yes	no	BGA100
LPC4310	<tbd>	no	no	no	no	LQFP144
LPC4310	<tbd>	no	no	no	no	BGA100

5. Block diagram

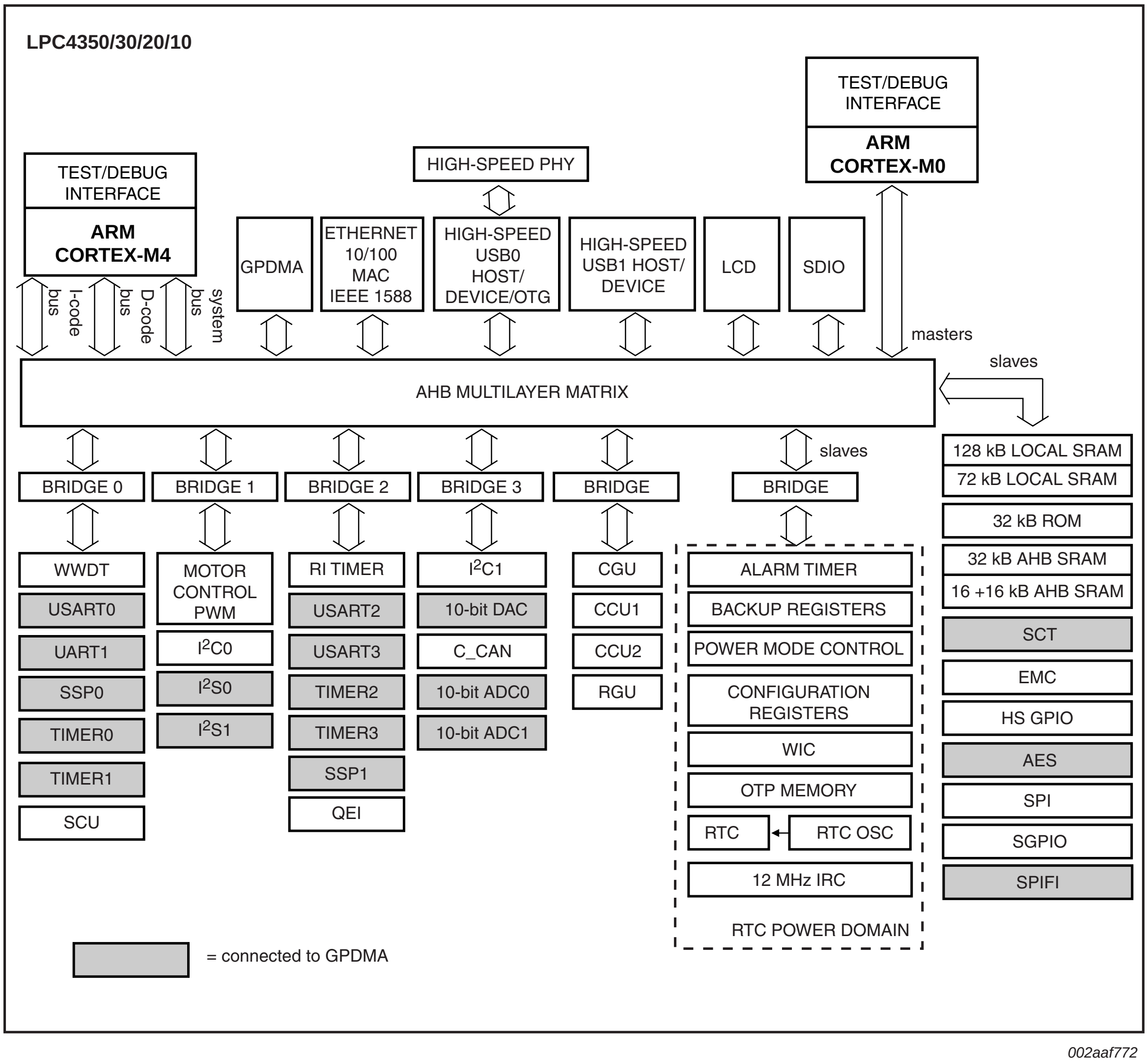


Fig 1. LPC4350/30/20/10 Block diagram

6. Pinning information

6.1 Pinning

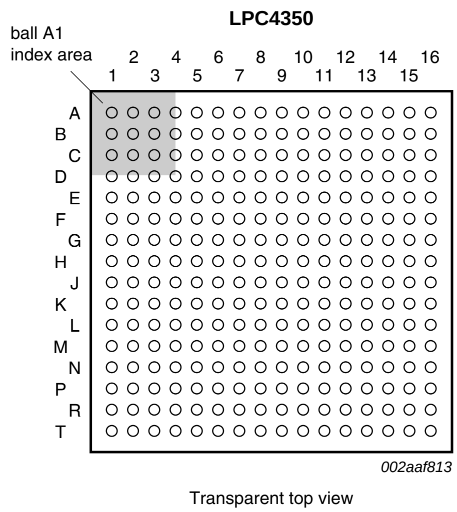


Fig 2. Pin configuration BGA256 package

6.2 Pin description

On the LPC4350/30/20/10, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin may support up to four different digital functions, including General Purpose I/O (GPIO), selectable through the SYSCON registers. Note that the pin name is not indicative of the GPIO port assigned to it.

Analog functions and power pins are pinned out separately and do not share pins with digital functions.

Not all functions listed in Table 3 are available on all packages. See Table 2 for availability of USB0, USB1, Ethernet, and LCD functions.

Table 3. Pin description

Symbol	LBGA256 pin	Reset state	Type	Description
Multiplexed digital pins				
P0_0[2]	L3	I; PU	I/O	**GPIO0[0]** — General purpose digital input/output pin.
			I/O	**SSP1_MISO** — Master In Slave Out for SSP1.
			I	**ENET_RXD1** — Ethernet receive data 1 (RMII/MII interface).
			I/O	**SGPIO0** — General purpose digital input/output pin.
P0_1[2]	M2	I; PU	I/O	**GPIO0[1]** — General purpose digital input/output pin.
			I/O	**SSP1_MOSI** — Master Out Slave in for SSP1.
			O	**ENET_TXD1** — Ethernet transmit data 1 (RMII/MII interface).
			I/O	**SGPIO1** — General purpose digital input/output pin.

Table 3. Pin description *...continued*

Symbol	LBGA256 pin	Reset state	Type	Description
P1_0[2]	P2	I; PU	I/O	**GPIO0[4] —** General purpose digital input/output pin.
			I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
			I/O	**EXTBUS_A5 —** External memory address line 5.
			-	n.c.
P1_1[2]	R2	I; PU	I/O	**GPIO0[8] —** General purpose digital input/output pin.
			O	**CTOUT_7 —** SCT output 7. Match output 3 of timer 1.
			I/O	**EXTBUS_A6 —** External memory address line 6. Boot control pin 0.
			I/O	**SGPIO8 —** General purpose digital input/output pin.
P1_2[2]	R3	I; PU	I/O	**GPIO0[9] —** General purpose digital input/output pin.
			O	**CTOUT_6 —** SCT output 6. Match output 2 of timer 1.
			I/O	**EXTBUS_A7 —** External memory address line 7. Boot control pin 1.
			I/O	**SGPIO9 —** General purpose digital input/output pin.
P1_3[2]	P5	I; PU	I/O	**GPIO0[10] —** General purpose digital input/output pin.
			O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
			I/O	**SGPIO10 —** General purpose digital input/output pin.
			O	**EXTBUS_OE —** LOW active Output Enable signal.
P1_4[2]	T3	I; PU	I/O	**GPIO0[11] —** General purpose digital input/output pin.
			O	**CTOUT_9 —** SCT output 9. Match output 1 of timer 2.
			I/O	**SGPIO11 —** General purpose digital input/output pin.
			O	**EXTBUS_BLS0 —** LOW active Byte Lane select signal 0.
P1_5[2]	R5	I; PU	I/O	**GPIO1[8] —** General purpose digital input/output pin.
			O	**CTOUT_10 —** SCT output 10. Match output 2 of timer 2.
			-	n.c.
			O	**EXTBUS_CS0 —** LOW active Chip Select 0 signal.
P1_6[2]	T4	I; PU	I/O	**GPIO1[9] —** General purpose digital input/output pin.
			I	**CTIN_5 —** SCT input 5. Capture input 2 of timer 2.
			-	n.c.
			O	**EXTBUS_WE —** LOW active Write Enable signal.
P1_7[2]	T5	I; PU	I/O	**GPIO1[0] —** General purpose digital input/output pin.
			I	**U1_DSR —** Data Set Ready input for UART1.
			O	**CTOUT_13 —** SCT output 13. Match output 1 of timer 3.
			I/O	**EXTBUS_D0 —** External memory data line 0.
P1_8[2]	R7	I; PU	I/O	**GPIO1[1] —** General purpose digital input/output pin.
			O	**U1_DTR —** Data Terminal Ready output for UART1.
			O	**CTOUT_12 —** SCT output 12. Match output 0 of timer 3.
			I/O	**EXTBUS_D1 —** External memory data line 1.
P1_9[2]	T7	I; PU	I/O	**GPIO1[2] —** General purpose digital input/output pin.
			O	**U1_RTS —** Request to Send output for UART1.
			O	**CTOUT_11 —** SCT output 11. Match output 3 of timer 2.
			I/O	**EXTBUS_D2 —** External memory data line 2.

Table 3. Pin description *…continued*

Symbol	LBGA256 pin	Reset state	Type	Description
P1_10[2]	R8	I; PU	I/O	**GPIO1[3] —** General purpose digital input/output pin.
			I	**U1_RI —** Ring Indicator input for UART1.
			O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
			I/O	**EXTBUS_D3 —** External memory data line 3.
P1_11[2]	T9	I; PU	I/O	**GPIO1[4] —** General purpose digital input/output pin.
			I	**U1_CTS —** Clear to Send input for UART1.
			O	**CTOUT_15 —** SCT output 15. Match output 3 of timer 3.
			I/O	**EXTBUS_D4 —** External memory data line 4.
P1_12[2]	R9	I; PU	I/O	**GPIO1[5] —** General purpose digital input/output pin.
			I	**U1_DCD —** Data Carrier Detect input for UART1.
			-	n.c.
			I/O	**EXTBUS_D5 —** External memory data line 5.
P1_13[2]	R10	I; PU	I/O	**GPIO1[6] —** General purpose digital input/output pin.
			O	**U1_TXD —** Transmitter output for UART1.
			-	n.c.
			I/O	**EXTBUS_D6 —** External memory data line 6.
P1_14[2]	R11	I; PU	I/O	**GPIO1[7] —** General purpose digital input/output pin.
			I	**U1_RXD —** Receiver input for UART1.
			-	n.c.
			I/O	**EXTBUS_D7 —** External memory data line 7.
P1_15[2]	T12	I; PU	I/O	**GPIO0[2] —** General purpose digital input/output pin.
			O	**U2_TXD —** Transmitter output for USART2.
			I/O	**SGPIO2 —** General purpose digital input/output pin.
			I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
P1_16[2]	M7	I; PU	I/O	**GPIO0[3] —** General purpose digital input/output pin.
			I	**U2_RXD —** Receiver input for USART2.
			I/O	**SGPIO3 —** General purpose digital input/output pin.
			I	**ENET_RX_DV —** Ethernet Receive Data Valid (MII interface).
P1_17[2]	M8	I; PU	I/O	**GPIO0[12] —** General purpose digital input/output pin.
			I/O	**U2_UCLK —** Serial clock input/output for USART2 in synchronous mode.
			-	n.c.
			I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
P1_18[2]	N12	I; PU	I/O	**GPIO0[13] —** General purpose digital input/output pin.
			I/O	**U2_DIR —** RS-485/EIA-485 output enable/direction control for USART2.
			-	n.c.
			O	**ENET_TXD0 —** Ethernet transmit data 0 (RMII/MII interface).

Table 3. Pin description *...continued*

Symbol	LBGA256 pin	Reset state	Type	Description
P1_19[2]	M11	<tbd>	I	**ENET_TX_CLK (ENET_REF_CLK) —** Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
			I/O	**SSP1_SCK —** Serial clock for SSP1.
			O	**CLKOUT —** Clock output pin.
			I/O	**I2S1_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
P1_20[2]	M10	I; PU	I/O	**GPIO0[15] —** General purpose digital input/output pin.
			I/O	**SSP1_SSEL —** Slave Select for SSP1.
			-	n.c.
			O	**ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface).
P2_0[2]	T16	<tbd>	I/O	**SGPIO4 —** General purpose digital input/output pin.
			O	**U0_TXD —** Transmitter output for USART0.
			I/O	**EXTBUS_A13 —** External memory address line 13.
			O	**USB0_PWR_EN —** VBUS drive signal (towards external charge pump or power management unit); indicates that Vbus must be driven (active high).
P2_1[2]	N15	<tbd>	I/O	**SGPIO5 —** General purpose digital input/output pin.
			I	**U0_RXD —** Receiver input for USART0.
			I/O	**EXTBUS_A12 —** External memory address line 12.
			O	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
P2_2[2]	M15	<tbd>	I/O	**SGPIO6 —** General purpose digital input/output pin.
			I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
			I/O	**EXTBUS_A11 —** External memory address line 11.
			O	**USB0_IND1 —** <tbd>.
P2_3[2]	J12	<tbd>	I/O	**SGPIO12 —** General purpose digital input/output pin.
			I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I^2C pad).
			O	**U3_TXD —** Transmitter output for USART3.
			I	**CTIN_1 —** SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
P2_4[2]	K11	<tbd>	I/O	**SGPIO13 —** General purpose digital input/output pin.
			I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I^2C pad).
			I	**U3_RXD —** Receiver input for USART3.
			I	**CTIN_0 —** SCT input 0. Capture input 0 of timer 0, 1, 2, 3.
P2_5[3]	K14	<tbd>	I/O	**SGPIO14 —** General purpose digital input/output pin.
			I	**CTIN_2 —** SCT input 2. Capture input 2 of timer 0.
			I	**USB1_VBUS —** Monitors the presence of USB1 bus power. **Note:** This signal must be HIGH for USB reset to occur.
			I	**ADCTRIG1 —** ADC trigger input 1.

Table 3. Pin description *…continued*

Symbol	LBGA256 pin	Reset state	Type	Description
P2_6[2]	K16	<tbd>	I/O	**SGPIO7 —** General purpose digital input/output pin.
			I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
			I/O	**EXTBUS_A10 —** External memory address line 10.
			O	**USB0_IND0 —** <tbd>.
P2_7[2]	H14	I; PU	I/O	**GPIO0[7] —** General purpose digital input/output pin. This pin is sampled at RESET for ISP entry.
			O	**CTOUT_1 —** SCT output 1. Match output 1 of timer 0.
			I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
			I/O	**EXTBUS_A9 —** External memory address line 9.
P2_8[2]	J16	<tbd>	I/O	**SGPIO15 —** General purpose digital input/output pin.
			O	**CTOUT_0 —** SCT output 0. Match output 0 of timer 0.
			I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
			I/O	**EXTBUS_A8 —** External memory address line 8. Boot control pin 2.
P2_9[2]	H16	I; PU	I/O	**GPIO1[10] —** General purpose digital input/output pin.
			O	**CTOUT_3 —** SCT output 3. Match output 3 of timer 0.
			I/O	**U3_BAUD —** <tbd> for USART3.
			I/O	**EXTBUS_A0 —** External memory address line 0.
P2_10[2]	G16	I; PU	I/O	**GPIO0[14] —** General purpose digital input/output pin.
			O	**CTOUT_2 —** SCT output 2. Match output 2 of timer 0.
			O	**U2_TXD —** Transmitter output for USART2.
			I/O	**EXTBUS_A1 —** External memory address line 1.
P2_11[2]	F16	I; PU	I/O	**GPIO1[11] —** General purpose digital input/output pin.
			O	**CTOUT_5 —** SCT output 5. Match output 1 of timer 1.
			I	**U2_RXD —** Receiver input for USART2.
			I/O	**EXTBUS_A2 —** External memory address line 2.
P2_12[2]	E15	I; PU	I/O	**GPIO1[12] —** General purpose digital input/output pin.
			O	**CTOUT_4 —** SCT output 4. Match output 0 of timer 1.
			-	n.c.
			I/O	**EXTBUS_A3 —** External memory address line 3.
P2_13[2]	C16	I; PU	I/O	**GPIO1[13] —** General purpose digital input/output pin.
			I	**CTIN_4 —** SCT input 4. Capture input 2 of timer 1.
			-	n.c.
			I/O	**EXTBUS_A4 —** External memory address line 4.
P3_0[2]	F13	<tbd>	I/O	**I2S0_TX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
			O	**I2S0_RX_MCLK —** I2S0 receive master clock.
			I/O	**I2S0_RX_SCK —** I2S0 transmit clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
			O	**I2S0_TX_MCLK —** I2S0 transmit master clock.

Table 3. Pin description *…continued*

Symbol	LBGA256 pin	Reset state	Type	Description
P3_1[2]	G11	<tbd>	I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
			I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
			I	**CAN1_RD —** CAN1 receiver input.
			O	**USB1_IND1 —** USB1 Port indicator LED control output 1.
P3_2[2]	F11	<tbd>	I/O	**I2S0_TX_SDA —** I2S0 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
			I/O	**I2S0_RX_SDA —** I2S0 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
			O	**CAN1_TD —** CAN1 transmitter output.
			O	**USB1_IND0 —** USB1 Port indicator LED control output 0.
P3_3[4]	B14	<tbd>	I/O	**SPI_SCK —** Serial clock for SPI.
			-	n.c.
			I/O	**SSP0_SCK —** Serial clock for SSP0.
			O	**SPIFI_SCK —** Serial clock for SPIFI.
P3_4[2]	A15	I; PU	I/O	**GPIO1[14] —** General purpose digital input/output pin.
			I/O	**I2S0_RX_SDA —** I2S0 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
			I/O	**I2S1_TX_SDA —** I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
			I/O	**SPIFI_SIO3 —** I/O lane 3 for SPIFI.
P3_5[2]	C12	I; PU	I/O	**GPIO1[15] —** General purpose digital input/output pin.
			I/O	**I2S1_RX_SDA —** I2S1 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
			I/O	**I2S1_TX_SDA —** I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
			I/O	**SPIFI_SIO2 —** I/O lane 2 for SPIFI.
P3_6[2]	B13	I; PU	I/O	**GPIO0[6] —** General purpose digital input/output pin.
			I/O	**SPI_MISO —** Master In Slave Out for SPI.
			I/O	**SSP0_SSEL —** Slave Select for SSP0.
			I/O	**SPIFI_MISO —** Input I1 in SPIFI quad mode; SPIFI output IO1.
P3_7[2]	C11	I; PU	I/O	**GPIO5[1] —** General purpose digital input/output pin.
			I/O	**SPI_MOSI —** Master Out Slave In for SPI.
			I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
			I/O	**SPIFI_MOSI —** Input I0 in SPIFI quad mode; SPIFI output IO0.

Table 3. Pin description *...continued*

Symbol	LBGA256 pin	Reset state	Type	Description
P3_8[2]	C10	I; PU	I/O	**GPIO5[2] —** General purpose digital input/output pin.
			I	**SPI_SSEL —** Slave Select for SPI. Note that this pin in an input pin only. The SPI in master mode cannot drive the CS input on the slave. Any GPIO pin can be used for SPI chip select in master mode.
			I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
			I/O	**SPIFI_CS —** SPIFI serial flash chip select.
P4_0[2]	D5	I; PU	I/O	**GPIO2[0] —** General purpose digital input/output pin.
			O	**MCOA0 —** Motor control PWM channel 0, output A.
			I	**NMI —** External interrupt input to NMI.
			O	**ENET_MDC —** Ethernet MIIM clock.
P4_1[2]	A1	I; PU	I/O	**GPIO2[1] —** General purpose digital input/output pin.
			O	**CTOUT_1 —** SCT output 1. Match output 1 of timer 0.
			O	**LCDVD0 —** LCD data.
			I	**ENET_COL —** Ethernet Collision detect (MII interface).
P4_2[2]	D3	I; PU	I/O	**GPIO2[2] —** General purpose digital input/output pin.
			O	**CTOUT_0 —** SCT output 0. Match output 0 of timer 0.
			O	**LCDVD3 —** LCD data.
			I/O	**SGPIO8 —** General purpose digital input/output pin.
P4_3[2]	C2	I; PU	I/O	**GPIO2[3] —** General purpose digital input/output pin.
			O	**CTOUT_3 —** SCT output 0. Match output 3 of timer 0.
			O	**LCDVD2 —** LCD data.
			I/O	**SGPIO9 —** General purpose digital input/output pin.
P4_4[2]	B1	I; PU	I/O	**GPIO2[4] —** General purpose digital input/output pin.
			O	**CTOUT_2 —** SCT output 2. Match output 2 of timer 0.
			O	**LCDVD1 —** LCD data.
			I/O	**SGPIO10 —** General purpose digital input/output pin.
P4_5[2]	D2	I; PU	I/O	**GPIO2[5] —** General purpose digital input/output pin.
			O	**CTOUT_5 —** SCT output 5. Match output 1 of timer 1.
			O	**LCDFP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
			I/O	**SGPIO11 —** General purpose digital input/output pin.
P4_6[2]	C1	I; PU	I/O	**GPIO2[6] —** General purpose digital input/output pin.
			O	**CTOUT_4 —** SCT output 4. Match output 0 of timer 1.
			O	**LCDENAB/LCDM —** STN AC bias drive or TFT data enable input.
			I/O	**SGPIO12 —** General purpose digital input/output pin.
P4_7[2]	H4	<tbd>	O	**I2S0_TX_MCLK —** I2S0 transmit master clock.
			O	**LCDDCLK —** LCD panel clock.
			I	**GP_CLKIN —** General purpose clock input to the CGU.
			O	**I2S0_RX_MCLK —** I2S0 receive master clock.

Table 3. Pin description *…continued*

Symbol	LBGA256 pin	Reset state	Type	Description
P4_8[2]	E2	I; PU	I/O	**GPIO5[3] —** General purpose digital input/output pin.
			I	**CTIN_5 —** SCT input 5. Capture input 2 of timer 2.
			O	**LCDVD9 —** LCD data.
			I/O	**SGPIO13 —** General purpose digital input/output pin.
P4_9[2]	L2	I; PU	I/O	**GPIO5[4] —** General purpose digital input/output pin.
			I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
			O	**LCDVD11 —** LCD data.
			I/O	**SGPIO14 —** General purpose digital input/output pin.
P4_10[2]	M3	I; PU	I/O	**GPIO5[5] —** General purpose digital input/output pin.
			I	**CTIN_2 —** SCT input 2. Capture input 2 of timer 0.
			O	**LCDVD10 —** LCD data.
			I/O	**SGPIO15 —** General purpose digital input/output pin.
P5_0[2]	N3	I; PU	I/O	**GPIO2[9] —** General purpose digital input/output pin.
			O	**MCOB2 —** Motor control PWM channel 2, output B.
			I/O	**EXTBUS_D12 —** External memory data line 12.
			-	n.c.
P5_1[2]	P3	I; PU	I/O	**GPIO2[10] —** General purpose digital input/output pin.
			I	**MCI2 —** Motor control PWM channel 2, input.
			I/O	**EXTBUS_D13 —** External memory data line 13.
			-	n.c.
P5_2[2]	R4	I; PU	I/O	**GPIO2[11] —** General purpose digital input/output pin.
			I	**MCI1 —** Motor control PWM channel 1, input.
			I/O	**EXTBUS_D14 —** External memory data line 14.
			-	n.c.
P5_3[2]	T8	I; PU	I/O	**GPIO2[12] —** General purpose digital input/output pin.
			I	**MCI0 —** Motor control PWM channel 0, input.
			I/O	**EXTBUS_D15 —** External memory data line 15.
			-	n.c.
P5_4[2]	P9	I; PU	I/O	**GPIO2[13] —** General purpose digital input/output pin.
			O	**MCOB0 —** Motor control PWM channel 0, output B.
			I/O	**EXTBUS_D8 —** External memory data line 8.
			-	n.c.
P5_5[2]	P10	I; PU	I/O	**GPIO2[14] —** General purpose digital input/output pin.
			O	**MCOA1 —** Motor control PWM channel 1, output A.
			I/O	**EXTBUS_D9 —** External memory data line 9.
			-	n.c.
P5_6[2]	T13	I; PU	I/O	**GPIO2[15] —** General purpose digital input/output pin.
			O	**MCOB1 —** Motor control PWM channel 1, output B.
			I/O	**EXTBUS_D10 —** External memory data line 10.
			-	n.c.

Table 3. Pin description *…continued*

Symbol	LBGA256 pin	Reset state	Type	Description
P5_7[2]	R12	I; PU	I/O	**GPIO2[7] —** General purpose digital input/output pin.
			O	**MCOA2 —** Motor control PWM channel 2, output A.
			I/O	**EXTBUS_D11 —** External memory data line 11.
			-	n.c.
P6_0[2]	M12	<tbd>	I/O	**I2S0_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2*S-bus specification*.
			O	**I2S0_RX_MCLK —** I2S0 receive master clock.
			-	n.c.
			-	n.c.
P6_1[2]	R15	I; PU	I/O	**GPIO3[0] —** General purpose digital input/output pin.
			O	**EXTBUS_DYCS1 —** SDRAM chip select 1.
			I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
			I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the I^2*S-bus specification*.
P6_2[2]	L13	I; PU	I/O	**GPIO3[1] —** General purpose digital input/output pin.
			O	**EXTBUS_CKEOUT1 —** SDRAM clock enable 1.
			I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
			I/O	**I2S0_RX_SDA —** I2S0 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the I^2*S-bus specification*.
P6_3[2]	P15	I; PU	I/O	**GPIO3[2] —** General purpose digital input/output pin.
			O	**USB0_PWR_EN —** VBUS drive signal (towards external charge pump or power management unit); indicates that the VBUS signal must be driven (active HIGH).
			I/O	**SGPIO4 —** General purpose digital input/output pin.
			O	**EXTBUS_CS1 —** LOW active Chip Select 1 signal.
P6_4[2]	R16	I; PU	I/O	**GPIO3[3] —** General purpose digital input/output pin.
			I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
			O	**U0_TXD —** Transmitter output for USART0.
			O	**EXTBUS_CAS —** LOW active SDRAM Column Address Strobe.
P6_5[2]	P16	I; PU	I/O	**GPIO3[4] —** General purpose digital input/output pin.
			O	**CTOUT_6 —** SCT output 6. Match output 2 of timer 1.
			I	**U0_RXD —** Receiver input for USART0.
			O	**EXTBUS_RAS —** LOW active SDRAM Row Address Strobe.
P6_6[2]	L14	I; PU	I/O	**GPIO0[5] —** General purpose digital input/output pin.
			O	**EXTBUS_BLS1 —** LOW active Byte Lane select signal 1.
			I/O	**SGPIO5 —** General purpose digital input/output pin.
			O	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).

Table 3. Pin description *...continued*

Symbol	LBGA256 pin	Reset state	Type	Description
P6_7[2]	J13	I; PU	I/O	**GPIO5[6] —** General purpose digital input/output pin.
			I/O	**EXTBUS_A15 —** External memory address line 15.
			I/O	**SGPIO6 —** General purpose digital input/output pin.
			O	**USB0_IND1 —** USB1 port indicator LED control output 1.
P6_8[2]	H13	I; PU	I/O	**GPIO5[7] —** General purpose digital input/output pin.
			I/O	**EXTBUS_A14 —** External memory address line 14.
			I/O	**SGPIO7 —** General purpose digital input/output pin.
			O	**USB0_IND0 —** USB1 port indicator LED control output 0.
P6_9[2]	J15	I; PU	I/O	**GPIO3[5] —** General purpose digital input/output pin.
			-	n.c.
			-	n.c.
			O	**EXTBUS_DYCS0 —** SDRAM chip select 0.
P6_10[2]	H15	I; PU	I/O	**GPIO3[6] —** General purpose digital input/output pin.
			O	**MCABORT —** Motor control PWM, LOW-active fast abort.
			-	n.c.
			O	**EXTBUS_DQMOUT1 —** Data mask 1 used with SDRAM and static devices.
P6_11[2]	H12	I; PU	I/O	**GPIO3[7] —** General purpose digital input/output pin.
			-	n.c.
			-	n.c.
			O	**EXTBUS_CKEOUT0 —** SDRAM clock enable 0.
P6_12[2]	G15	I; PU	I/O	**GPIO2[8] —** General purpose digital input/output pin.
			O	**CTOUT_7 —** SCT output 7. Match output 3 of timer 1.
			-	n.c.
			O	**EXTBUS_DQMOUT0 —** Data mask 0 used with SDRAM and static devices.
P7_0[2]	B16	I; PU	I/O	**GPIO3[8] —** General purpose digital input/output pin.
			O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
			-	n.c.
			O	**LCDLE —** Line end signal.
P7_1[2]	C14	I; PU	I/O	**GPIO3[9] —** General purpose digital input/output pin.
			O	**CTOUT_15 —** SCT output 15. Match output 3 of timer 3.
			I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
			O	**LCDVD19 —** LCD data.
P7_2[2]	A16	I; PU	I/O	**GPIO3[10] —** General purpose digital input/output pin.
			I	**CTIN_4 —** SCT input 4. Capture input 2 of timer 1.
			I/O	**I2S0_TX_SDA —** I2S0 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
			O	**LCDVD18 —** LCD data.

Table 3. Pin description *…continued*

Symbol	LBGA256 pin	Reset state	Type	Description
P7_3[2]	C13	I; PU	I/O	**GPIO3[11] —** General purpose digital input/output pin.
			I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
			I/O	**I2S1_TX_SDA —** I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
			O	**LCDVD17 —** LCD data.
P7_4[2]	C8	I; PU	I/O	**GPIO3[12] —** General purpose digital input/output pin.
			O	**CTOUT_13 —** SCT output 13. Match output 1 of timer 3.
			I/O	**I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
			O	**LCDVD16 —** LCD data.
P7_5[2]	A7	I; PU	I/O	**GPIO3[13] —** General purpose digital input/output pin.
			O	**CTOUT_12 —** SCT output 12. Match output 0 of timer 3.
			I/O	**I2S1_RX_SDA —** I2S1 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
			O	**LCDVD8 —** LCD data.
P7_6[2]	C7	I; PU	I/O	**GPIO3[14] —** General purpose digital input/output pin.
			O	**CTOUT_11 —** SCT output 1. Match output 3 of timer 2.
			I/O	**I2S1_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
			O	**LCDLP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
P7_7[2]	B6	I; PU	I/O	**GPIO3[15] —** General purpose digital input/output pin.
			O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
			O	**ENET_MDC —** Ethernet MIIM clock.
			O	**LCDPWR —** LCD panel power enable.
P8_0[2]	E5	I; PU	I/O	**GPIO4[0] —** General purpose digital input/output pin.
			O	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
			-	n.c.
			I	**MCI2 —** Motor control PWM channel 2, input.
P8_1[2]	H5	I; PU	I/O	**GPIO4[1] —** General purpose digital input/output pin.
			O	**USB0_IND1 —** USB0 port indicator LED control output 1.
			-	n.c.
			I	**MCI1 —** Motor control PWM channel 1, input.
P8_2[2]	K4	I; PU	I/O	**GPIO4[2] —** General purpose digital input/output pin.
			O	**USB0_IND0 —** USB0 port indicator LED control output 0.
			-	n.c.
			I	**MCI0 —** Motor control PWM channel 0, input.

Table 3. Pin description *…continued*

Symbol	LBGA256 pin	Reset state	Type	Description
P8_3[2]	J3	I; PU	I/O	**GPIO4[3] —** General purpose digital input/output pin.
			I/O	**USB1_ULPI_D2 —** ULPI link bidirectional data line 2.
			-	n.c.
			O	**LCDVD12 —** LCD data.
P8_4[2]	J2	I; PU	I/O	**GPIO4[4] —** General purpose digital input/output pin.
			I/O	**USB1_ULPI_D1 —** ULPI link bidirectional data line 1.
			-	n.c.
			O	**LCDVD7 —** LCD data.
P8_5[2]	J1	I; PU	I/O	**GPIO4[5] —** General purpose digital input/output pin.
			I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
			-	n.c.
			O	**LCDVD6 —** LCD data.
P8_6[2]	K3	I; PU	I/O	**GPIO4[6] —** General purpose digital input/output pin.
			I	**USB1_ULPI_NXT —** ULPI link NXT signal. Data flow control signal from the PHY.
			-	n.c.
			O	**LCDVD5 —** LCD data.
P8_7[2]	K1	I; PU	I/O	**GPIO4[7] —** General purpose digital input/output pin.
			O	**USB1_ULPI_STP —** ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
			-	n.c.
			O	**LCDVD4 —** LCD data.
P8_8[2]	L1	<tbd>	-	n.c.
			I	**USB1_ULPI_CLK —** ULPI link CLK signal. 60 MHz clock generated by the PHY.
			-	n.c.
			I/O	**I2S1_TX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
P9_0[2]	T1	I; PU	I/O	**GPIO4[12] —** General purpose digital input/output pin.
			O	**$\overline{\text{MCABORT}}$ —** Motor control PWM, LOW-active fast abort.
			-	n.c.
			-	n.c.
P9_1[2]	N6	I; PU	I/O	**GPIO4[13] —** General purpose digital input/output pin.
			O	**MCOA2 —** Motor control PWM channel 2, output A.
			-	n.c.
			-	n.c.
P9_2[2]	N8	I; PU	I/O	**GPIO4[14] —** General purpose digital input/output pin.
			O	**MCOB2 —** Motor control PWM channel 2, output B.
			-	n.c.
			-	n.c.

Table 3. Pin description *...continued*

Symbol	LBGA256 pin	Reset state	Type	Description
P9_3[2]	M6	I; PU	I/O	**GPIO4[15] —** General purpose digital input/output pin.
			O	**MCOA0 —** Motor control PWM channel 0, output A.
			O	**USB1_IND1 —** USB1 Port indicator LED control output 1.
			-	n.c.
P9_4[2]	N10	I; PU	I/O	**GPIO5[8] —** General purpose digital input/output pin.
			O	**MCOB0 —** Motor control PWM channel 0, output B.
			O	**USB1_IND0 —** USB1 Port indicator LED control output 0.
			-	n.c.
P9_5[2]	M9	I; PU	I/O	**GPIO5[9] —** General purpose digital input/output pin.
			O	**MCOA1 —** Motor control PWM channel 1, output A.
			O	**USB1_VBUS_EN —** USB1 VBUS power enable.
			I/O	**I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
P9_6[2]	L11	I; PU	I/O	**GPIO4[11] —** General purpose digital input/output pin.
			O	**MCOB1 —** Motor control PWM channel 1, output B.
			O	**USB1_PWR_FAULT —** USB1 Port power fault signal indicating over-current condition; this signal monitors over-current on the USB1 bus (external circuitry required to detect over-current condition).
			I/O	**I2S1_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
PA_0[4]	L12	<tbd>	-	n.c.
			O	**SPIFI_SCK —** Serial clock for SPIFI.
			-	n.c.
			O	**I2S1_TX_MCLK —** I2S1 transmit master clock.
PA_1[2]	J14	I; PU	I/O	**GPIO4[8] —** General purpose digital input/output pin.
			I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
			-	n.c.
			-	n.c.
PA_2[2]	K15	I; PU	I/O	**GPIO4[9] —** General purpose digital input/output pin.
			I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
			-	n.c.
			-	n.c.
PA_3[2]	H11	I; PU	I/O	**GPIO4[10] —** General purpose digital input/output pin.
			I	**QEI_PHA —** Quadrature Encoder Interface PHA input.
			-	n.c.
			I/O	**SPIFI_SIO3 —** I/O lane 3 for SPIFI.
PA_4[2]	G13	I; PU	I/O	**GPIO0[16] —** General purpose digital input/output pin.
			O	**CTOUT_9 —** SCT output 9. Match output 1 of timer 2.
			-	n.c.
			I/O	**EXTBUS_A23 —** External memory address line 23.

Table 3. Pin description *…continued*

Symbol	LBGA256 pin	Reset state	Type	Description
PB_0[2]	B15	I; PU	I/O	**GPIO5[10] —** General purpose digital input/output pin.
			O	**CTOUT_10 —** SCT output 10. Match output 2 of timer 2.
			O	**LCDVD23 —** LCD data.
			-	n.c.
PB_1[2]	A14	I; PU	I/O	**GPIO5[11] —** General purpose digital input/output pin.
			I	**USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULP data line direction.
			O	**LCDVD22 —** LCD data.
			-	n.c.
PB_2[2]	B12	I; PU	I/O	**GPIO5[12] —** General purpose digital input/output pin.
			I/O	**USB1_ULPI_D7 —** ULPI link bidirectional data line 7.
			O	**LCDVD21 —** LCD data.
			-	n.c.
PB_3[2]	A13	I; PU	I/O	**GPIO5[13] —** General purpose digital input/output pin.
			I/O	**USB1_ULPI_D6 —** ULPI link bidirectional data line 6.
			O	**LCDVD20 —** LCD data.
			-	n.c.
PB_4[2]	B11	I; PU	I/O	**GPIO5[14] —** General purpose digital input/output pin.
			I/O	**USB1_ULPI_D5 —** ULPI link bidirectional data line 5.
			O	**LCDVD15 —** LCD data.
			-	n.c.
PB_5[2]	A12	I; PU	I/O	**GPIO5[15] —** General purpose digital input/output pin.
			I/O	**USB1_ULPI_D4 —** ULPI link bidirectional data line 4.
			O	**LCDVD14 —** LCD data.
			-	n.c.
PB_6[2]	A6	I; PU	I/O	**GPIO5[0] —** General purpose digital input/output pin.
			I/O	**USB1_ULPI_D3 —** ULPI link bidirectional data line 3.
			O	**LCDVD13 —** LCD data.
			-	n.c.
PC_0[2]	D4	<tbd>	I/O	**ENET_RX_CLK (ENET_REF_CLK) —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
			I	**USB1_ULPI_CLK —** ULPI link CLK signal. 60 MHz clock generated by the PHY.
			-	n.c.
			I/O	**SDIO_CLK —** SDIO card clock.
PC_1[2]	E4	<tbd>	I/O	**USB1_ULPI_D7 —** ULPI link bidirectional data line 7.
			O	**SDIO_VOLT0 —** SDIO bus voltage select output 0.
			I	**U1_RI —** Ring Indicator input for UART 1.
			O	**ENET_MDC —** Ethernet MIIM clock.

Table 3. Pin description *...continued*

Symbol	LBGA256 pin	Reset state	Type	Description
PC_2[2]	F6	<tbd>	I/O	**USB1_ULPI_D6 —** ULPI link bidirectional data line 6.
			O	**SDIO_RST —** SDIO reset signal for MMC4.4 card.
			I	**U1_CTS —** Clear to Send input for UART 1.
			O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
PC_3[2]	F5	<tbd>	I/O	**USB1_ULPI_D5 —** ULPI link bidirectional data line 5.
			O	**SDIO_VOLT1 —** SDIO bus voltage select output 1.
			O	**U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
			O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
PC_4[2]	F4	<tbd>	I/O	**SDIO_D0 —** SDIO data bus line 0.
			I/O	**USB1_ULPI_D4 —** ULPI link bidirectional data line 4.
			I/O	**SPIFI_CS —** SPIFI serial flash chip select.
			I	**ENET_COL —** Ethernet Collision detect (MII interface).
PC_5[2]	G4	<tbd>	I/O	**SDIO_D1 —** SDIO data bus line 1.
			I/O	**USB1_ULPI_D3 —** ULPI link bidirectional data line 3.
			I/O	**SPIFI_MISO —** Input I1 in SPIFI quad mode; SPIFI output IO1.
			O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
PC_6[2]	H6	I; PU	I/O	**GPIO6[0] —** General purpose digital input/output pin.
			I/O	**USB1_ULPI_D2 —** ULPI link bidirectional data line 2.
			I/O	**SDIO_D2 —** SDIO data bus line 2.
			I	**ENET_RXD2 —** Ethernet receive data 2 (RMII/MII interface).
PC_7[2]	G5	I; PU	I/O	**GPIO6[1] —** General purpose digital input/output pin.
			I/O	**USB1_ULPI_D1 —** ULPI link bidirectional data line 1.
			I/O	**SDIO_D3 —** SDIO data bus line 3.
			I	**ENET_RXD3 —** Ethernet receive data 3 (RMII/MII interface).
PC_8[2]	N4	<tbd>	I	**SDIO_CD —** SDIO card detect input.
			I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
			I/O	**SPIFI_SIO2 —** I/O lane 2 for SPIFI.
			I	**ENET_CRS (ENET_CRS_DV) —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
PC_9[2]	K2	I; PU	I/O	**GPIO6[2] —** General purpose digital input/output pin.
			I	**USB1_ULPI_NXT —** ULPI link NXT signal. Data flow control signal from the PHY.
			O	**SDIO_POW —** <tbd>.
			I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
PC_10[2]	M5	I; PU	I/O	**GPIO6[3] —** General purpose digital input/output pin.
			O	**USB1_ULPI_STP —** ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
			I	**U1_DSR —** Data Set Ready input for UART 1.
			I/O	**SDIO_CMD —** SDIO command signal.

Table 3. Pin description *...continued*

Symbol	LBGA256 pin	Reset state	Type	Description
PC_11[2]	L5	I; PU	I/O	**GPIO6[4] —** General purpose digital input/output pin.
			I	**USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULP data line direction.
			I	**U1_DCD —** Data Carrier Detect input for UART 1.
			I/O	**SDIO_D4 —** SDIO data bus line 4.
PC_12[2]	L6	I; PU	I/O	**GPIO6[5] —** General purpose digital input/output pin.
			-	n.c.
			O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
			I/O	**SDIO_D5 —** SDIO data bus line 5.
PC_13[2]	M1	I; PU	I/O	**GPIO6[6] —** General purpose digital input/output pin.
			-	n.c.
			O	**U1_TXD —** Transmitter output for UART 1.
			I/O	**SDIO_D6 —** SDIO data bus line 6.
PC_14[2]	N1	I; PU	I/O	**GPIO6[7] —** General purpose digital input/output pin.
			-	n.c.
			I	**U1_RXD —** Receiver input for UART 1.
			I/O	**SDIO_D7 —** SDIO data bus line 7.
PD_0[2]	N2	I; PU	I/O	**GPIO7[0] —** General purpose digital input/output pin.
			O	**CTOUT_15 —** SCT output 15. Match output 3 of timer 3.
			O	**EXTBUS_DQMOUT2 —** Data mask 2 used with SDRAM and static devices.
			I/O	**SGPIO4 —** General purpose digital input/output pin.
PD_1[2]	P1	I; PU	I/O	**GPIO7[1] —** General purpose digital input/output pin.
			-	n.c.
			O	**EXTBUS_CKEOUT2 —** SDRAM clock enable 2.
			I/O	**SGPIO5 —** General purpose digital input/output pin.
PD_2[2]	R1	I; PU	I/O	**GPIO7[2] —** General purpose digital input/output pin.
			O	**CTOUT_7 —** SCT output 7. Match output 3 of timer 1.
			I/O	**EXTBUS_D16 —** External memory data line 16.
			I/O	**SGPIO6 —** General purpose digital input/output pin.
PD_3[2]	P4	I; PU	I/O	**GPIO7[3] —** General purpose digital input/output pin.
			O	**CTOUT_6 —** SCT output 7. Match output 2 of timer 1.
			I/O	**EXTBUS_D17 —** External memory data line 17.
			I/O	**SGPIO7 —** General purpose digital input/output pin.
PD_4[2]	T2	I; PU	I/O	**GPIO7[4] —** General purpose digital input/output pin.
			O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
			I/O	**EXTBUS_D18 —** External memory data line 18.
			I/O	**SGPIO8 —** General purpose digital input/output pin.

Table 3. Pin description *...continued*

Symbol	LBGA256 pin	Reset state	Type	Description
PD_5[2]	P6	I; PU	I/O	**GPIO7[5] —** General purpose digital input/output pin.
			O	**CTOUT_9 —** SCT output 9. Match output 1 of timer 2.
			I/O	**EXTBUS_D19 —** External memory data line 19.
			I/O	**SGPIO9 —** General purpose digital input/output pin.
PD_6[2]	R6	I; PU	I/O	**GPIO7[6] —** General purpose digital input/output pin.
			O	**CTOUT_10 —** SCT output 10. Match output 2 of timer 2.
			I/O	**EXTBUS_D20 —** External memory data line 20.
			I/O	**SGPIO10 —** General purpose digital input/output pin.
PD_7[2]	T6	I; PU	I/O	**GPIO7[7] —** General purpose digital input/output pin.
			I	**CTIN_5 —** SCT input 5. Capture input 2 of timer 2.
			I/O	**EXTBUS_D21 —** External memory data line 21.
			I/O	**SGPIO11 —** General purpose digital input/output pin.
PD_8[2]	P8	I; PU	I/O	**GPIO7[8] —** General purpose digital input/output pin.
			I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
			I/O	**EXTBUS_D22 —** External memory data line 22.
			I/O	**SGPIO12 —** General purpose digital input/output pin.
PD_9[2]	T11	I; PU	I/O	**GPIO7[9] —** General purpose digital input/output pin.
			O	**CTOUT_13 —** SCT output 13. Match output 1 of timer 3.
			I/O	**EXTBUS_D23 —** External memory data line 23.
			I/O	**SGPIO13 —** General purpose digital input/output pin.
PD_10[2]	P11	I; PU	I/O	**GPIO7[10] —** General purpose digital input/output pin.
			I	**CTIN_1 —** SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
			O	**$\overline{\text{EXTBUS\_BLS3}}$ —** LOW active Byte Lane select signal 3.
			-	n.c.
PD_11[2]	N9	I; PU	I/O	**GPIO7[11] —** General purpose digital input/output pin.
			-	n.c.
			O	**$\overline{\text{EXTBUS\_CS3}}$ —** LOW active Chip Select 3 signal.
			-	n.c.
PD_12[2]	N11	I; PU	I/O	**GPIO7[12] —** General purpose digital input/output pin.
			-	n.c.
			O	**$\overline{\text{EXTBUS\_CS2}}$ —** LOW active Chip Select 2 signal.
			-	n.c.
PD_13[2]	T14	I; PU	I/O	**GPIO7[13] —** General purpose digital input/output pin.
			I	**CTIN_0 —** SCT input 0. Capture input 0 of timer 0, 1, 2, 3.
			O	**$\overline{\text{EXTBUS\_BLS2}}$ —** LOW active Byte Lane select signal 2.
			-	n.c.

Table 3. Pin description *…continued*

Symbol	LBGA256 pin	Reset state	Type	Description
PD_14[2]	R13	I; PU	I/O	**GPIO7[14]** — General purpose digital input/output pin.
			-	n.c.
			O	**EXTBUS_DYCS2** — SDRAM chip select 2.
			-	n.c.
PD_15[2]	T15	I; PU	I/O	**GPIO7[15]** — General purpose digital input/output pin.
			-	n.c.
			I/O	**EXTBUS_A17** — External memory address line 17.
			-	n.c.
PD_16[2]	R14	I; PU	I/O	**GPIO7[16]** — General purpose digital input/output pin.
			-	n.c.
			I/O	**EXTBUS_A16** — External memory address line 16.
			-	n.c.
PE_0[2]	P14	I; PU	I/O	**GPIO7[17]** — General purpose digital input/output pin.
			-	n.c.
			-	n.c.
			I/O	**EXTBUS_A18** — External memory address line 18.
PE_1[2]	N14	I; PU	I/O	**GPIO7[18]** — General purpose digital input/output pin.
			-	n.c.
			-	n.c.
			I/O	**EXTBUS_A19** — External memory address line 19.
PE_2[2]	M14	<tbd>	I	**ADCTRIG0** — ADC trigger input 0.
			I	**CAN1_RD** — CAN1 receiver input.
			I/O	**SPIFI_MOSI** — Input I0 in SPIFI quad mode; SPIFI output IO0.
			I/O	**EXTBUS_A20** — External memory address line 20.
PE_3[2]	K12	I; PU	I/O	**GPIO7[19]** — General purpose digital input/output pin.
			O	**CAN1_TD** — CAN1 transmitter output.
			I	**ADCTRIG1** — ADC trigger input 1.
			I/O	**EXTBUS_A21** — External memory address line 21.
PE_4[2]	K13	I; PU	I/O	**GPIO7[20]** — General purpose digital input/output pin.
			I	**NMI** — External interrupt input to NMI.
			-	n.c.
			I/O	**EXTBUS_A22** — External memory address line 22.
PE_5[2]	N16	I; PU	I/O	**GPIO7[21]** — General purpose digital input/output pin.
			O	**CTOUT_3** — SCT output 3. Match output 3 of timer 0.
			O	**U1_RTS** — Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
			I/O	**EXTBUS_D24** — External memory data line 24.

Table 3. Pin description *…continued*

Symbol	LBGA256 pin	Reset state	Type	Description
PE_6[2]	M16	I; PU	I/O	**GPIO7[22] —** General purpose digital input/output pin.
			O	**CTOUT_2 —** SCT output 2. Match output 2 of timer 0.
			I	**U1_RI —** Ring Indicator input for UART 1.
			I/O	**EXTBUS_D25 —** External memory data line 25.
PE_7[2]	F15	I; PU	I/O	**GPIO7[23] —** General purpose digital input/output pin.
			O	**CTOUT_5 —** SCT output 5. Match output 1 of timer 1.
			I	**U1_CTS —** Clear to Send input for UART1.
			I/O	**EXTBUS_D26 —** External memory data line 26.
PE_8[2]	F14	I; PU	I/O	**GPIO7[24] —** General purpose digital input/output pin.
			O	**CTOUT_4 —** SCT output 4. Match output 0 of timer 0.
			I	**U1_DSR —** Data Set Ready input for UART 1.
			I/O	**EXTBUS_D27 —** External memory data line 27.
PE_9[2]	E16	I; PU	I/O	**GPIO7[25] —** General purpose digital input/output pin.
			I	**CTIN_4 —** SCT input 4. Capture input 2 of timer 1.
			I	**U1_DCD —** Data Carrier Detect input for UART 1.
			I/O	**EXTBUS_D28 —** External memory data line 28.
PE_10[2]	E14	I; PU	I/O	**GPIO7[26] —** General purpose digital input/output pin.
			I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
			O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
			I/O	**EXTBUS_D29 —** External memory data line 29.
PE_11[2]	D16	I; PU	I/O	**GPIO7[27] —** General purpose digital input/output pin.
			O	**CTOUT_12 —** SCT output 12. Match output 0 of timer 3.
			O	**U1_TXD —** Transmitter output for UART 1.
			I/O	**EXTBUS_D30 —** External memory data line 30.
PE_12[2]	D15	I; PU	I/O	**GPIO7[28] —** General purpose digital input/output pin.
			O	**CTOUT_11 —** SCT output 11. Match output 3 of timer 2.
			I	**U1_RXD —** Receiver input for UART 1.
			I/O	**EXTBUS_D31 —** External memory data line 31.
PE_13[2]	G14	I; PU	I/O	**GPIO7[29] —** General purpose digital input/output pin.
			O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
			I/O	**I2C1_SDA —** I^{2}C1 data input/output (this pin does not use a specialized I^{2}C pad).
			O	**EXTBUS_DQMOUT3 —** Data mask 3 used with SDRAM and static devices.
PE_14[2]	C15	I; PU	I/O	**GPIO7[30] —** General purpose digital input/output pin.
			-	n.c.
			-	n.c.
			O	**EXTBUS_DYCS3 —** SDRAM chip select 3.

Table 3. Pin description *...continued*

Symbol	LBGA256 pin	Reset state	Type	Description
PE_15[2]	E13	I; PU	I/O	**GPIO7[31] —** General purpose digital input/output pin.
			O	**CTOUT_0 —** SCT output 0. Match output 0 of timer 0.
			I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I^2C pad).
			O	**EXTBUS_CKEOUT3 —** SDRAM clock enable 3.
PF_0[2]	D12	<tbd>	I/O	**SSP0_SCK —** Serial clock for SSP0.
			-	n.c.
			-	n.c.
			-	n.c.
PF_1[2]	E11	I; PU	I/O	**GPIO0[17] —** General purpose digital input/output pin.
			-	n.c.
			I/O	**SSP0_SSEL —** Slave Select for SSP0.
			I/O	**SGPIO0 —** General purpose digital input/output pin.
PF_2[2]	D11	I; PU	I/O	**GPIO0[18] —** General purpose digital input/output pin.
			O	**U3_TXD —** Transmitter output for USART3.
			I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
			I/O	**SGPIO1 —** General purpose digital input/output pin.
PF_3[2]	E10	I; PU	I/O	**GPIO0[19] —** General purpose digital input/output pin.
			I	**U3_RXD —** Receiver input for USART3.
			I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
			-	n.c.
PF_4[2]	D10	<tbd>	I/O	**SSP1_SCK —** Serial clock for SSP1.
			I	**GP_CLKIN —** General purpose clock input to the CGU.
			O	**TRACECLK —** Trace clock.
			-	n.c.
PF_5[2]	E9	I; PU	I/O	**GPIO0[20] —** General purpose digital input/output pin.
			I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
			I/O	**SSP1_SSEL —** Slave Select for SSP1.
			O	**TRACEDATA[0] —** Trace data, bit 0.
PF_6[2]	E7	I; PU	I/O	**GPIO0[21] —** General purpose digital input/output pin.
			I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
			I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
			O	**TRACEDATA[1] —** Trace data, bit 1.
PF_7[2]	B7	I; PU	I/O	**GPIO0[22] —** General purpose digital input/output pin.
			I/O	**U3_BAUD —** <tbd> for USART3.
			I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
			O	**TRACEDATA[2] —** Trace data, bit 2.

Table 3. Pin description *...continued*

Symbol	LBGA256 pin	Reset state	Type	Description
PF_8[2]	E6	I; PU	I/O	**GPIO0[23]** — General purpose digital input/output pin.
			I/O	**U0_UCLK** — Serial clock input/output for USART0 in synchronous mode.
			I	**CTIN_2** — SCT input 2. Capture input 2 of timer 0.
			O	**TRACEDATA[3]** — Trace data, bit 3.
PF_9[2]	D6	I; PU	I/O	**GPIO0[24]** — General purpose digital input/output pin.
			I/O	**U0_DIR** — RS-485/EIA-485 output enable/direction control for USART0.
			O	**CTOUT_1** — SCT output 1. Match output 1 of timer 0.
			-	n.c.
PF_10[2]	A3	I; PU	I/O	**GPIO0[25]** — General purpose digital input/output pin.
			O	**U0_TXD** — Transmitter output for USART0.
			I	**SDIO_WP** — SDIO card write protect input.
			-	n.c.
PF_11[2]	A2	I; PU	I/O	**GPIO0[26]** — General purpose digital input/output pin.
			I	**U0_RXD** — Receiver input for USART0.
			O	**SDIO_VOLT2** — SDIO bus voltage select output 2.
			-	n.c.
Clock pins				
CLK0[4]	N5	<tbd>	O	**EXTBUS_CLK0** — SDRAM clock 0.
			O	**CLKOUT** — Clock output pin.
			-	n.c.
			-	n.c.
CLK1[4]	T10	<tbd>	-	n.c.
			O	**I2S1_RX_MCLK** — I2S1 receive master clock.
			-	n.c.
			-	n.c.
CLK2[4]	D14	<tbd>	O	**EXTBUS_CLK2** — SDRAM clock 2.
			O	**CLKOUT** — Clock output pin.
			-	n.c.
			-	n.c.
CLK3[4]	P12	<tbd>	-	n.c.
			-	n.c.
			-	n.c.
			-	n.c.
Debug pins				
DBGEN[2]	L4	<tbd>	I	JTAG interface control signal. Also used for boundary scan.
TCK[2]	J5	<tbd>	I	Test Clock for JTAG interface.
$\overline{\text{TRST}}$[2]	M4	<tbd>	I	Test Reset for JTAG interface.
TMS[2]	K6	<tbd>	I	Test Mode Select for JTAG interface.
TDO[2]	K5	<tbd>	O	Test Data Out for JTAG interface.
TDI[2]	J4	<tbd>	I	Test Data In for JTAG interface.

Table 3. Pin description *...continued*

Symbol	LBGA256 pin	Reset state	Type	Description
USB0 pins				
USB0_DP[5]	F2	<tbd>	I/O	USB0 bidirectional D+ line.
USB0_DM[5]	G2	<tbd>	I/O	USB0 bidirectional D– line.
USB0_VBUS[5]	F1	<tbd>	I/O	VBUS pin (power on USB cable).
USB0_ID[6]	H2	<tbd>	I	Indicates to the transceiver whether connected to an A-device (LOW) or a B-device (HIGH).
USB0_RREF[6]	H1	<tbd>		12.0 kΩ (accuracy 1%) on-board resistor to ground for current reference.
USB1 pins				
USB1_DP[7]	F12	<tbd>	I/O	USB1 bidirectional D+ line.
USB1_DM[7]	G12	<tbd>	I/O	USB1 bidirectional D– line.
I^{2}C-bus pins				
I2C0_SCL[8]	L15	<tbd>	I/O	I^{2}C clock input/output. Open-drain output (for I^{2}C-bus compliance).
I2C0_SDA[8]	L16	<tbd>	I/O	I^{2}C data input/output. Open-drain output (for I^{2}C-bus compliance).
Reset and wake-up pins				
$\overline{\text{RESET}}$[9]	D9	<tbd>	I	External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
WAKEUP0[9]	A9	<tbd>	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.
WAKEUP1[9]	A10	<tbd>	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.
WAKEUP2[9]	C9	<tbd>	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.
WAKEUP3[9]	D8	<tbd>	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes.
ADC pins				
ADC0[6]	E3	<tbd>	I	ADC0/1 input channel 0. Shared between ADC0, ADC1, and DAC.
ADC1[6]	C3	<tbd>	I	ADC0/1 input channel 1.
ADC2[6]	A4	<tbd>	I	ADC0/1 input channel 2.
ADC3[6]	B5	<tbd>	I	ADC0/1 input channel 3.
ADC4[6]	C6	<tbd>	I	ADC0/1 input channel 4.
ADC5[6]	B3	<tbd>	I	ADC0/1 input channel 5.
ADC6[6]	A5	<tbd>	I	ADC0/1 input channel 6.
ADC7[6]	C5	<tbd>	I	ADC0/1 input channel 7.
RTC				
RTC_ALARM	A11	-	O	RTC controlled output.
RTC_SAMPLE	B9	-	O	Sampling strobe output.
RTCX1	A8	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	B8	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
Crystal oscillator pins				
XTAL1[6]	D1	-	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2[6]	E1	-	O	Output from the oscillator amplifier.

Table 3. Pin description *…continued*

Symbol	LBGA256 pin	Reset state	Type	Description
Power and ground pins				
USB0_VDDA 3V3_DRIVER	F3	-	-	Separate analog 3.3 V power supply for driver.
USB0 _VDDA3V3	G3	-	-	USB 3.3 V separate power supply voltage.
USB0_VSSA _TERM	H3	-	-	Dedicated analog ground for clean reference for termination resistors.
USB0_VSSA _REF	G1	-	-	Dedicated clean analog ground for generation of reference currents and voltages.
VDDA	B4	-	-	Analog power supply.
VBAT	B10	-	-	RTC power supply: 3.3 V on this pin supplies power to the RTC.
VDDREG	F10; F9; L8; L7		-	Main regulator power supply.
VPP	E8	-	-	OTP programming voltage.
VDDIO	F7; J7; N7; L10; E12; N13; L9; H10; G10; D7; J6; F8; K7	-	-	I/O power supply.
VSS	H7; K8; G9; J11; J10	-	-	Ground.
VSSIO	G6; J8; J9; K9; K10; P7; M13; P13; D13; G8; H8; G7; C4; H9	-	-	Ground.
VSSA	B2	-	-	Analog ground.

[1] I = input, O = output, IA = inactive; PU = pull-up enabled; F = floating

[2] Digital I/O pin. Not 5 V tolerant.

[3] Digital I/O pin. 5 V tolerant.

[4] Digital high-speed I/O pin.

[5] 5 V tolerant analog I/O pin.

[6] 3.3 V tolerant analog I/O pin.

[7] 5 V tolerant USB I/O pin.

[8] I^2C-bus 5 V tolerant open-drain pin.

[9] RESET input pin.

[10] ALARM output pin.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC4350/30/20/10 use a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slaves ports of the matrix to be accessed simultaneously by different bus masters.

An ARM Cortex-M0 co-processor is included in the LPC4350/30/20/10, capable of off-loading the main ARM Cortex-M4 application processor. Most peripheral interrupts are connected to both processors. The processors communicate with each other via an interprocessor communication protocol.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point processor is integrated in the core. The processor includes a NVIC with up to 53 interrupts.

7.3 ARM Cortex-M0 co-processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M0 co-processor uses a 3-stage pipeline von Neumann architecture and a small but powerful instruction set providing high-end processing hardware. The co-processor incorporates a NVIC with 32 interrupts.

7.4 Interprocessor communication

The ARM Cortex-M4 and ARM Cortex-M0 interprocessor communication is based on using shared SRAM as mailbox and one processor raising an interrupt on the other processor's NVIC, for example after it has delivered a new message in the mailbox. The receiving processor can reply by raising an interrupt on the sending processor's NVIC to acknowledge the message.

7.5 AHB multilayer matrix

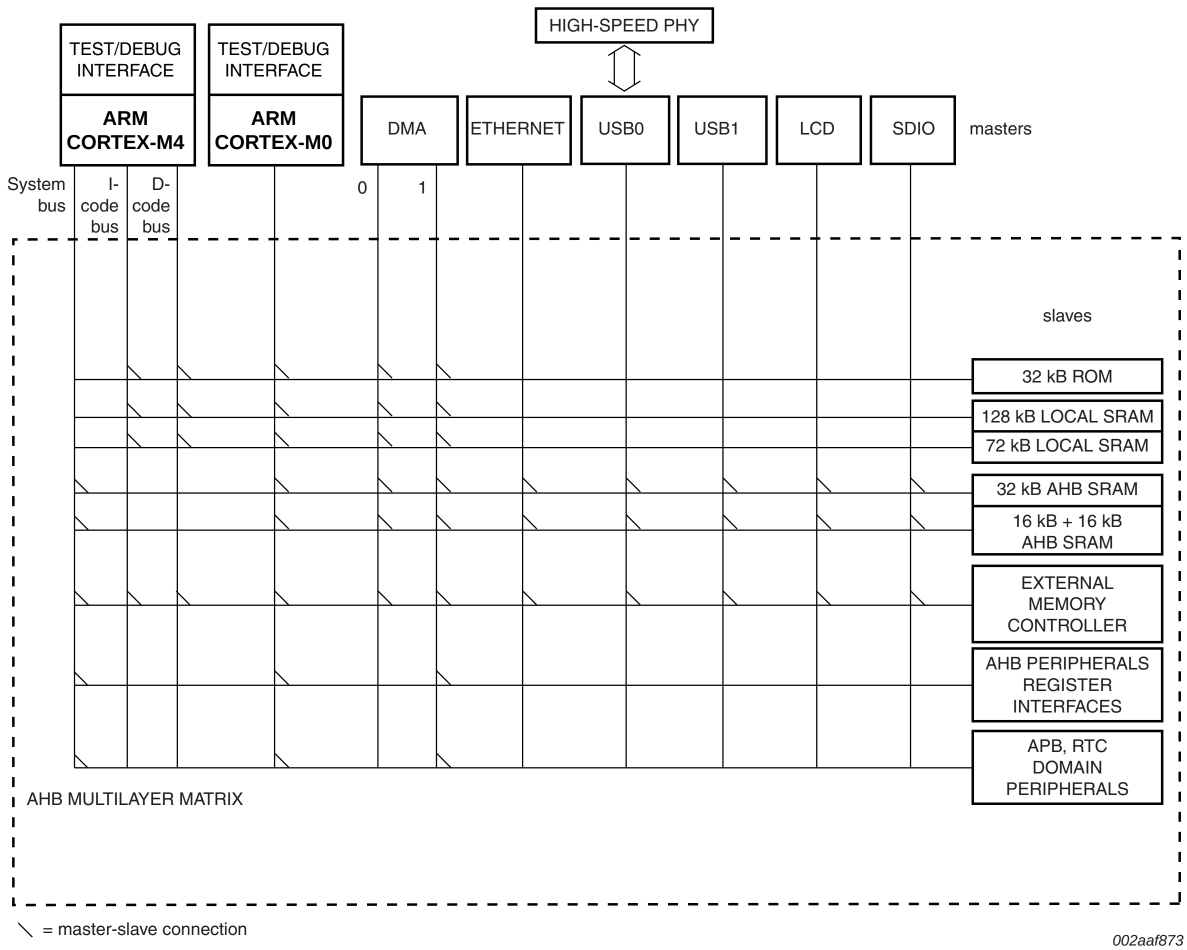


Fig 3. AHB multilayer matrix master and slave connections

7.6 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

The ARM Cortex-M0 co-processor has its own NVIC with 32 vectored interrupts. Most peripheral interrupts are shared between the Cortex-M0 and Cortex-M4 NVICs.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC4350/30/20/10, the Cortex-M4 NVIC supports up to 53 vectored interrupts.
- 32 programmable interrupt priority levels with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).

- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

7.7 On-chip static RAM

The LPC4350/30/20/10 support up to 200 kB local SRAM and an additional 64 kB AHB SRAM with separate bus master access for higher throughput and individual power control for low power operation.

7.8 Memory mapping

The memory map shown in Figure 4 and Figure 5 is global to both the Cortex-M4 and the Cortex-M0 processors and all SRAM is shared between both processors. Each processor uses its own ARM private bus memory map for the NVIC and other system functions.

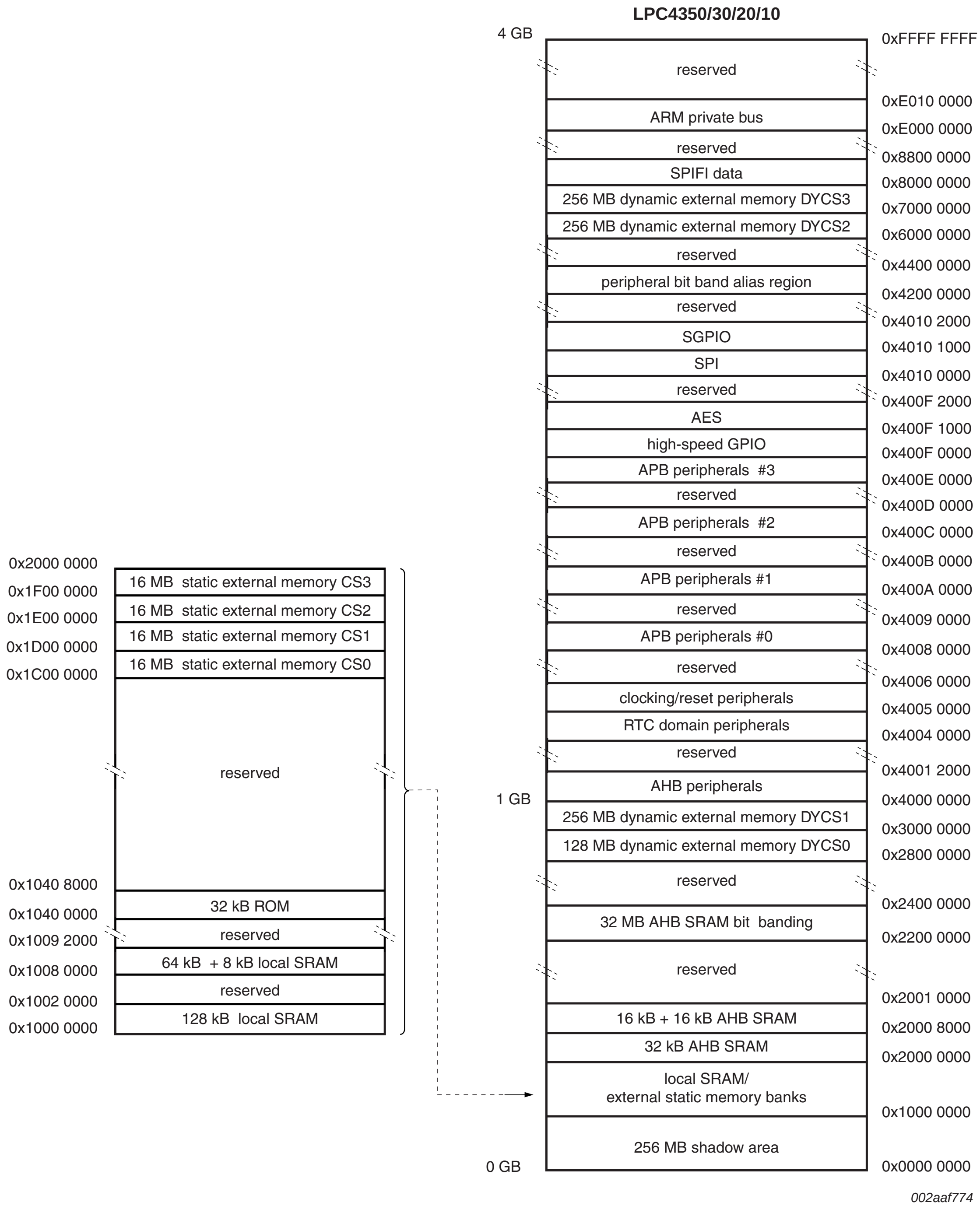


Fig 4. LPC4350/30/20/10 Memory mapping (overview)

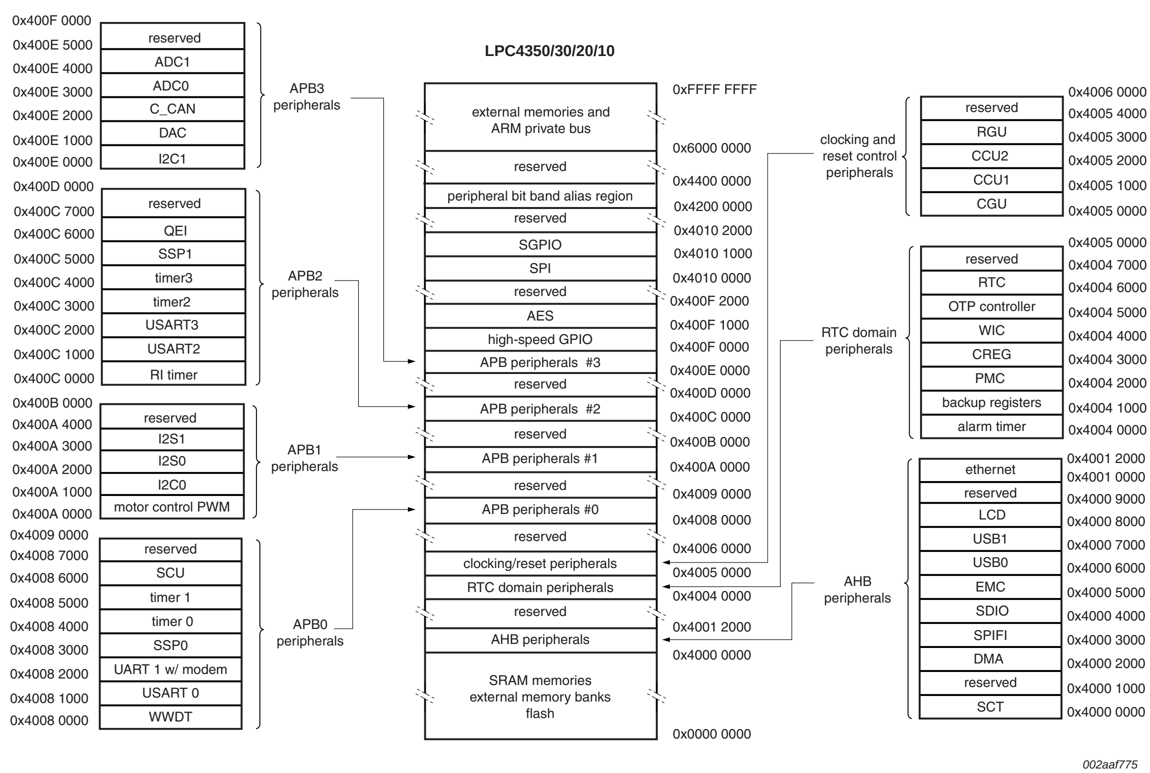


Fig 5. LPC4350/30/20/10 Memory mapping (peripherals)

7.9 Security features

7.9.1 AES decryption engine

The hardware AES engine can decrypt data using the AES algorithm.

7.9.1.1 Features

- Decryption of external flash data connected to the quad SPI Flash Interface (SPIFI) and other external boot sources.
- Secure storage of decryption keys.
- Support for CMAC hash calculation to authenticate encrypted data.
- Data is processed in little endian mode. This means that the first byte read from flash is integrated into the AES codeword as least significant byte. The 16th byte read from flash is the most significant byte of the first AES codeword.
- AES engine performance of 1 byte/clock cycle.
- Programmable through an on-chip API.
- DMA transfers supported through the GPDMA.

7.9.2 One-Time Programmable (OTP) memory

The OTP provides two 128-bit non-volatile memories to store AES decryption keys or other custom data.

7.10 General Purpose I/O (GPIO)

The LPC4350/30/20/10 provide 8 GPIO ports with up to 32 GPIO pins each.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

All GPIO pins default to inputs with pull-up resistors enabled on reset.

7.10.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- GPIO ports can create an interrupt.

7.11 Configurable digital peripherals

7.11.1 State Configurable Timer (SCT) subsystem

The SCT allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCT are shared with the capture and match inputs/outputs of the 32-bit general purpose counter/timers.

The SCT can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable
- Limit, halt, stop, and start conditions
- Values of Match/Capture registers, plus reload or capture control values

In the two-counter case, the following operational elements are global to the SCT, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.11.1.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counter(s) clocked by bus clock or selected input.
- Up counter(s) or up-down counter(s).
- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs and interrupts.
- Selected event(s) can limit, halt, start, or stop a counter.
- Supports:
  - 8 inputs (one input connected internally)
  - 16 outputs
  - 16 match/capture registers
  - 16 events
  - 32 states

7.11.2 Serial GPIO (SGPIO)

The Serial GPIOs offer standard GPIO functionality enhanced with features to accelerate serial stream processing.

7.11.2.1 Features

- Each SGPIO input/output slice can be used to perform a serial to parallel or parallel to serial data conversion.
- 16 SGPIO input/output slices each with a 32-bit FIFO that can shift the input value from a pin or an output value to a pin with every cycle of a shift clock.
- Each slice is double-buffered.
- Interrupt is generated on a full FIFO, shift clock, or pattern match.
- Slices can be concatenated to increase buffer size.
- Each slice has a 32-bit pattern match filter.

7.12 AHB peripherals

7.12.1 General Purpose DMA (GPDMA)

The DMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receives. The source and destination areas can each be either a memory region or a peripheral for master 1, but only memory for master 0.

7.12.1.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- Two AHB bus masters for transferring data. These interfaces transfer data when a DMA request goes active. Master 1 can access memories and peripherals, master 0 can access memories only.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.

- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.12.2 SPI Flash Interface (SPIFI)

The SPI Flash Interface (allows low-cost serial flash memories to be connected to the ARM Cortex-M3 processor with little performance penalty compared to parallel flash devices with higher pin count.

After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Erasure and programming are handled by simple sequences of commands.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization and then move to a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.12.2.1 Features

- Interfaces to serial flash memory in the main memory map.
- Supports classic and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Data rates of up to 40 MB per second.
- Supports DMA access.

7.12.3 SDIO card interface

The SDIO card interface supports the following modes to control:

- Secure Digital memory (SD version 3.0)
- Secure Digital I/O (SDIO version 2.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.1)
- MultiMedia Cards (MMC version 4.4)

7.12.4 External Memory Controller (EMC)

The LPC4350/30/20/10 EMC is a Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals.

7.12.4.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- Low transaction latency.

- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 24 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read
  - Programmable Wait States
  - Bus turnaround delay
  - Output enable and write enable delays
  - Extended wait
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EXTBUS_CKEOUT and EXTBUS_CLK signals to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.12.5 High-speed USB Host/Device/OTG interface (USB0)

Remark: Not available on all parts and packages. See Table 2.

The USB OTG module allows the LPC4350/30/20/10 to connect directly to a USB Host such as a PC (in device mode) or to a USB Device in host mode.

7.12.5.1 Features

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Contains UTMI+ compliant transceiver (PHY).
- Supports interrupts.
- This module has its own, integrated DMA engine.

7.12.6 High-speed USB Host/Device interface with ULPI (USB1)

Remark: Not available on all parts and packages. See Table 2.

The USB1 interface can operate as a full-speed USB Host/Device interface or can connect to an external ULPI PHY for High-speed operation.

7.12.6.1 Features

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals if connected to external ULPI PHY.
- Supports all full-speed USB-compliant peripherals.
- Supports interrupts.
- This module has its own, integrated DMA engine.

7.12.7 LCD controller

Remark: Not available on all parts and packages. See Table 2.

The LCD controller provides all of the necessary control signals to interface directly to a variety of color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512-byte color palette allows reducing bus utilization (i.e. memory size of the displayed data) while still supporting a large number of colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time needed to operate the display.

7.12.7.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized for color STN and TFT.
- 24 bpp true-color non-palettized for color TFT.
- Programmable timing for different display panels.

- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

7.12.8 Ethernet

Remark: Not available on all parts and packages. See Table 2.

7.12.8.1 Features

- 10/100 Mbit/s
- TCP/IP hardware checksum
- IP checksum
- DMA support
- Power management remote wake-up frame and magic packet detection
- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Supports IEEE1588 timestamping.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.

7.13 Digital serial peripherals

7.13.1 UART1

The LPC4350/30/20/10 contain one UART with standard transmit and receive data lines, UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

UART1 includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.13.1.1 Features

- Maximum UART data bit rate of <tbd> MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.

- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Equipped with standard modem interface signals. This module also provides full support for hardware flow control.
- Support for RS-485/9-bit/EIA-485 mode (UART1).
- DMA support.

7.13.2 USART0/2/3

The LPC4350/30/20/10 contain three USARTs. In addition to standard transmit and receive data lines, the USARTs support a synchronous mode.

The USARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.13.2.1 Features

- Maximum UART data bit rate of <tbd> MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit/EIA-485 mode.
- USART3 includes an IrDA mode to support infrared communication.
- All USARTs have DMA support.
- Support for synchronous mode.
- Smart card mode conforming to ISO7816 specification

7.13.3 SPI serial I/O controller

The LPC4350/30/20/10 contain one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

7.13.3.1 Features

- Maximum SPI data bit rate <tbd>
- Compliant with SPI specification
- Synchronous, serial, full duplex communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

7.13.4 SSP0/1 serial I/O controllers

The LPC4350/30/20/10 contain two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.13.4.1 Features

- Maximum SSP speed of <tbd> Mbit/s (master) or <tbd> Mbit/s (slave)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- DMA transfers supported by GPDMA

7.13.5 I^{2}C0/1-bus interfaces

The LPC4350/30/20/10 each contain two I^{2}C-bus controllers.

The I^{2}C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^{2}C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.13.5.1 Features

- I^{2}C0 is a standard I^{2}C compliant bus interface with open-drain pins. I^{2}C0 also supports Fast mode plus with bit rates up to 1 Mbit/s.
- I^{2}C1 uses standard I/O pins with bit rates of up to 400 kbit/s (Fast I^{2}C-bus).
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^{2}C-bus can be used for test and diagnostic purposes.
- All I^{2}C-bus controllers support multiple address recognition and a bus monitor mode.

7.13.6 I2S0/1 interfaces

The I2S-bus provides a standard communication interface for digital audio applications.

The *I2S-bus specification* defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I2S-bus connection has one master, which is always the master, and one slave. The I2S-bus interface provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

7.13.6.1 Features

- Both I2S interfaces have separate input/output channels, each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 96 kHz (16, 22.05, 32, 44.1, 48, 96) kHz.
- Support for an audio master clock.
- Configurable word select period in master mode (separately for I2S-bus input and output).
- Two 8-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests for each I2S interface, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I2S-bus input and I2S-bus output.

7.13.7 C_CAN

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller allows to build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a very high level of security.

7.13.7.1 Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.

7.14 Counter/timers and motor control

7.14.1 General purpose 32-bit timers/external event counters

The LPC4350/30/20/10 include four 32-bit timer/counters. The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.14.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

7.14.2 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input is also provided that causes the PWM to immediately release all motor drive outputs. At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

7.14.3 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

7.14.3.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with "less than" interrupt.
- Uses 32-bit registers for position and velocity.
- Three position compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).

7.14.4 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 32-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.14.4.1 Features

- 32-bit counter. Counter can be free-running or be reset by a generated interrupt.
- 32-bit compare value.
- 32-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.

7.14.5 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.14.5.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.

- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.

7.15 Analog peripherals

7.15.1 Analog-to-Digital Converter (ADC0/1)

7.15.1.1 Features

- 10-bit successive approximation analog to digital converter.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 to 3 V.
- Sampling frequency up to 400 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal <tbd>.
- Individual result registers for each A/D channel to reduce interrupt overhead.
- DMA support.

7.15.2 Digital-to-Analog Converter (DAC)

7.15.2.1 Features

- 10-bit resolution
- Integral Non-Linearity (INL) <tbd>
- Differential Non-Linearity (DNL) <tbd>
- Monotonic by design (resistor string architecture)
- Controllable conversion speed
- Low power consumption

7.16 Peripherals in the RTC power domain

7.16.1 RTC

The Real Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses very little power when its registers are not being accessed by the CPU, especially reduced power modes. On the LPC4350/30/20/10, the RTC is clocked by a separate 32 kHz oscillator that produces a 1 Hz internal time reference. The RTC is powered by its own power supply pin, VBAT.

7.16.1.1 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.
- Ultra-low power design to support battery powered systems. Less than 1 μA required for battery operation. Uses power from the CPU power supply when it is present.

- Dedicated battery power supply pin.
- RTC power supply is isolated from the rest of the chip.
- Calibration counter allows adjustment to better than ±1 sec/day with 1 sec resolution.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Alarm interrupt can be generated for a specific date/time.

7.16.2 Alarm timer

The alarm timer is a 16-bit timer and counts down at 1 kHz from a preset value generating alarms in intervals of up to 1 min. The counter triggers a status bit when it reaches 0x00 and asserts an interrupt if enabled.

The alarm timer is part of the RTC power domain and can be battery powered.

7.17 System control

7.17.1 Configuration registers (CREG)

The following settings are controlled in the configuration register block:

- BOD trip settings
- Oscillator output
- DMA-to-peripheral muxing
- Ethernet mode
- Memory mapping
- Timer/USART inputs
- Enabling the USB controllers

In addition, the CREG block contains the part identification and part configuration information.

7.17.2 System Control Unit (SCU)

The system control unit determines the function and electrical mode of the digital pins. By default function 0 is selected for all pins with pull-up enabled.

Analog I/Os for the ADCs and the DAC as well as most USB functions reside on separate pins and are not controlled through the SCU.

7.17.3 Clock Generation Unit (CGU)

The Clock Generator Unit (CGU) generates 21 outputs called base clocks. The CGU outputs are unrelated in frequency and phase and can have different clock sources within the CGU. One CGU output is routed to the CLKOUT pins.

Within each clock area there may be multiple branch clocks, which offers very flexible control for power-management purposes. All branch clocks are outputs of one of two Clock Control Units (CCUs) and can be controlled independently. Branch clocks derived from the same base clock are synchronous in frequency and phase.

7.17.4 Internal RC oscillator (IRC)

The IRC is used as the clock source for the WWDT and/or as the clock that drives the PLLs and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC4350/30/20/10 use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.17.5 PLL0 and PLL2

PLL0 is a dedicated PLL for the USB0 High-speed controller, and PLL2 can be used as an audio PLL.

PLL0 and PLL2 are identical PLL blocks. In addition, PLL2 has a fractional rate divider to control the output frequency with a very fine granularity.

PLL0 and PLL2 accept an input clock frequency from an external oscillator in the range of 14 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The CCO operates in the range of 4.3 MHz to 550 MHz.

7.17.6 System PLL1

The PLL1 accepts an input clock frequency from an external oscillator in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.17.7 Reset Generation Unit (RGU)

The RGU allows generation of independent reset signals for individual blocks and peripherals on the LPC4350/30/20/10.

7.17.8 Power control

The LPC4350/30/20/10 support four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.

The LPC4350/30/20/10 can wake up from Deep-sleep, Power-down, and Deep power-down modes via the WAKEUP[3:0] pins and interrupts generated by battery powered blocks in the RTC power domain.

7.18 Serial Wire Debug/JTAG

<tbd>

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)	on pin VDD_REG	2.2[2]	3.6	V
$V_{DD(IO)}$	I/O supply voltage	on pin VDDIO	2.2	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA	2.0	3.6	V
V_{BAT}	battery supply voltage	for the RTC	2.2	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP	2.7	3.6	V
V_{IA}	analog input voltage	on ADC	0	$V_{DDA(3V3)}$	V
V_I	input voltage	only valid when the $V_{DD(IO)}$ supply voltage is present [3]	2.0	3.6	V
I_{DD}	supply current	per supply pin [4]	-	<tbd>	mA
I_{SS}	ground current	per ground pin [4]	-	<tbd>	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$; $T_j < 125$ °C	-	<tbd>	mA
T_{stg}	storage temperature	[5]	<tbd>	<tbd>	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	<tbd>	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins [6]	<tbd>	<tbd>	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] 2.0 V if VBAT ≥ 2.2 V.

[3] Including voltage on outputs in 3-state mode; at 2.0 V the speed will be reduced.

[4] The peak current is limited to 25 times the corresponding maximum current.

[5] Dependent on package type.

[6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \qquad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 5. Thermal characteristics

V_{DD} = 2.2 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature		-	-	<tbd>	°C

10. Static characteristics

Table 6. Static characteristics
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(IO)}$	I/O supply voltage		[2]	2.2	-	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)			2.2	-	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			2.0	-	3.6	V
V_{BAT}	battery supply voltage		[3]	2.2	-	3.6	V
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	active mode; code `while(1){}` executed from <tbd>; all peripherals disabled					
		CCLK = 12 MHz; PLL disabled	[4]	-	<tbd>	-	mA
		CCLK = 100 MHz; PLL enabled	[4]	-	<tbd>	-	mA
		CCLK = 150 MHz; PLL enabled	[4]	-	<tbd>	-	mA
		sleep mode	[4]	-	<tbd>	-	mA
		deep sleep mode	[4][6]	-	<tbd>	-	μA
		power-down mode	[4][6]	-	<tbd>	-	μA
		deep power-down mode; RTC not running	[4]	-	<tbd>	-	nA
I_{BAT}	battery supply current	deep power-down mode; RTC running			<tbd>		
		$V_{DD(REG)(3V3)}$ present	[7]	-	<tbd>	-	nA
		$V_{DD(REG)(3V3)}$ not present	[8]	-	<tbd>	-	nA
$I_{DD(IO)}$	I/O supply current	deep sleep mode	[9]	-	<tbd>	-	nA
		power-down mode	[9]	-	<tbd>	-	nA
		deep power-down mode	[9]	-	<tbd>	-	nA
$I_{DD(ADC)}$	ADC supply current	deep sleep mode	[10]	-	<tbd>	-	nA
		power-down mode	[10]	-	<tbd>	-	nA
		deep power-down mode	[10]	-	<tbd>	-	nA

Table 6. Static characteristics *…continued*

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Digital pins						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	-	<tbd>	μA
I_{IH}	HIGH-level input current	V_I = $V_{DD(IO)}$; on-chip pull-down resistor disabled	-	-	<tbd>	μA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = $V_{DD(IO)}$; on-chip pull-up/down resistors disabled	-	-	<tbd>	μA
V_I	input voltage	pin configured to provide a digital function [11][12][13]	<tbd>	-	<tbd>	V
V_O	output voltage	output active	<tbd>	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage		<tbd>	-	-	V
V_{IL}	LOW-level input voltage		-	-	<tbd>	V
V_{hys}	hysteresis voltage		<tbd>	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	$V_{DD(IO)}$ – 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	<tbd>	V
I_{OH}	HIGH-level output current	V_{OH} = $V_{DD(IO)}$ – 0.4 V	<tbd>	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	<tbd>	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V [14]	-	-	<tbd>	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = $V_{DD(IO)}$ [14]	-	-	<tbd>	mA
I_{pd}	pull-down current	V_I = 3.6 V	<tbd>	<tbd>	<tbd>	μA
I_{pu}	pull-up current	V_I = 0 V	<tbd>	<tbd>	<tbd>	μA
		$V_{DD(IO)} < V_I < 3.6$ V	<tbd>	<tbd>	<tbd>	μA
Open-drain I²C0-bus pins						
V_{IH}	HIGH-level input voltage		<tbd>	-	-	V
V_{IL}	LOW-level input voltage		-	-	<tbd>	V
V_{hys}	hysteresis voltage		-	<tbd>	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = <tbd> mA	-	-	<tbd>	V
I_{LI}	input leakage current	V_I = $V_{DD(IO)}$ [15]	-	<tbd>	<tbd>	μA
		V_I = 5 V	-	<tbd>	<tbd>	μA

Table 6. Static characteristics *…continued*

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Oscillator pins						
$V_{i(XTAL1)}$	input voltage on pin XTAL1		–0.5	-	1.2	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2		–0.5	-	1.2	V
USB pins						
V_{IC}	common-mode input voltage	high-speed mode	<tbd>	<tbd>	<tbd>	mV
		full-speed/low-speed mode	<tbd>	-	<tbd>	mV
		chirp mode	<tbd>	-	<tbd>	mV
$V_{i(dif)}$	differential input voltage		<tbd>	<tbd>	<tbd>	mV

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Minimum value is 2.0 V if $V_{BAT} \geq 2.2$ V.

[3] The RTC typically fails when V_{BAT} drops below <tbd>.

[4] $V_{DD(REG)(3V3)}$ = 3.3 V; T_{amb} = 25 °C for all power consumption measurements.

[5] IRC running at 12 MHz; <tbd>.

[6] BOD disabled.

[7] On pin VBAT; $I_{DD(REG)(3V3)}$ = <tbd> nA; $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{BAT} < V_{DD(REG)(3V3)}$; T_{amb} = 25 °C.

[8] On pin VBAT; V_{BAT} = 3.3 V; T_{amb} = 25 °C.

[9] All internal pull-ups disabled. All pins configured as output and driven LOW. $V_{DD(REG)(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[10] $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[11] Including voltage on outputs in 3-state mode.

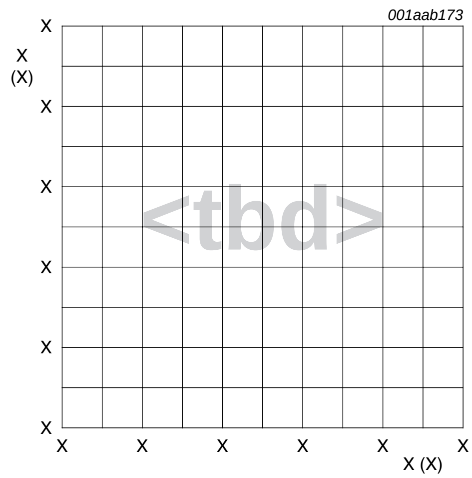
[12] $V_{DD(REG)(3V3)}$ supply voltages must be present.

[13] 3-state outputs go into 3-state mode in Deep power-down mode.

[14] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

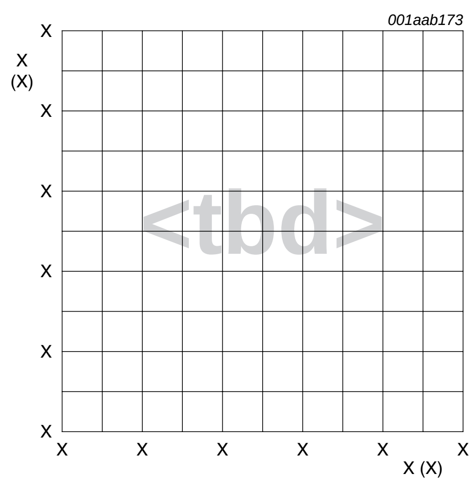
[15] To V_{SS}.

10.1 Electrical pin characteristics



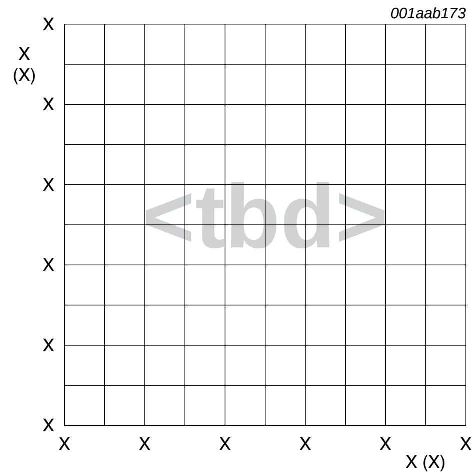
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; standard port pins.

Fig 6. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



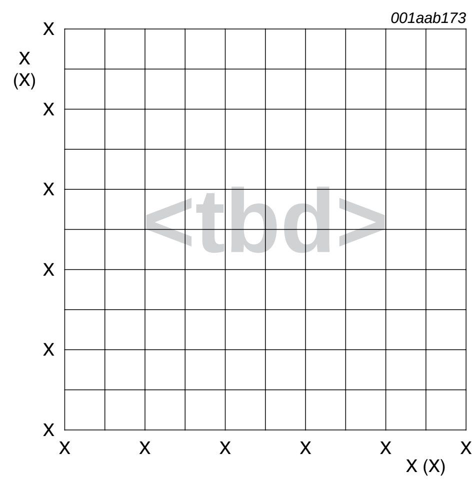
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; standard port pins.

Fig 7. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; standard port pins.

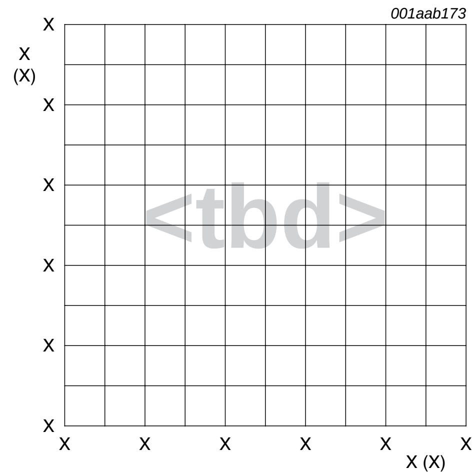
Fig 8. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; standard port pins.

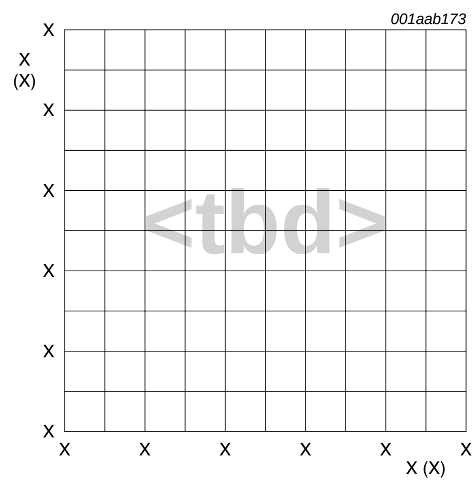
Fig 9. Typical pull-down current I_{pd} versus input voltage V_I

10.2 Power consumption



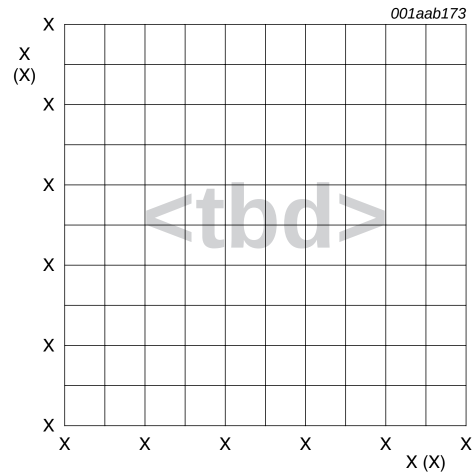
Conditions: <tbd>.

Fig 10. Typical supply current versus regulator supply voltage $V_{DD(REEG)(3V3)}$ in active mode



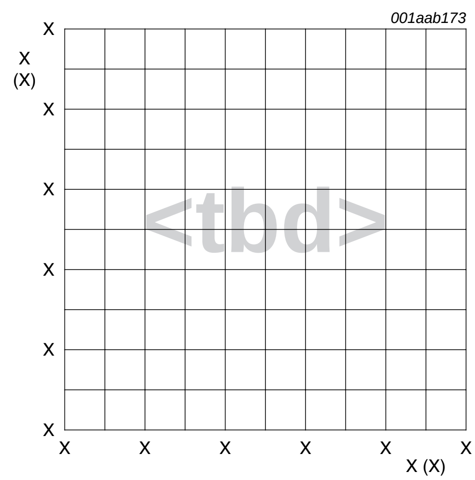
Conditions: <tbd>.

Fig 11. Typical supply current versus temperature in active mode



Conditions: <tbd>

Fig 12. Typical supply current versus temperature in Sleep mode



Conditions: <tbd>

Fig 13. Typical supply current versus temperature in Deep-sleep mode

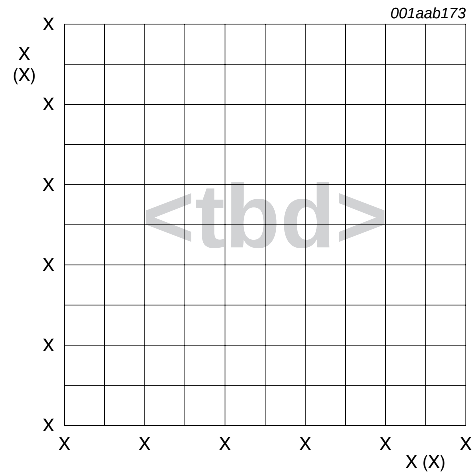


Fig 14. Typical supply current versus temperature in Power-down mode

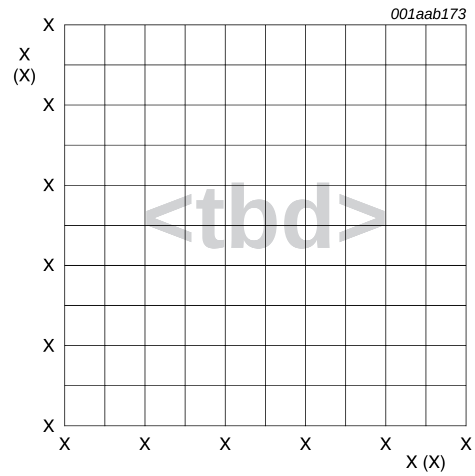


Fig 15. Typical supply current versus temperature in Deep power-down mode

Table 7. Power consumption for individual peripherals

T_{amb} = 25 °C; $V_{DD(REEG)(3V3)}$ = 3.3 V.

Peripheral	Conditions	Typical I_{DD}[1]
<tbd>	<tbd>	

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11. Dynamic characteristics

11.1 Digital I/O and CLKOUT pins, oscillator, PLL, and C_CAN

Table 8. Dynamic characteristics: Digital I/O and CLKOUT pins, oscillator, PLL, and C_CAN

$V_{DD(IO)}$, $V_{DD(REG)(3V3)}$ over specified ranges; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Digital I/O pins							
t_{THL}	HIGH to LOW transition time	C_L = 30 pF		<tbd>	-	<tbd>	ns
t_{TLH}	LOW to HIGH transition time	C_L = 30 pF		<tbd>	-	<tbd>	ns
CLKOUT pin							
f_{clk}	clock frequency	on pin CLKOUT		-	-	<tbd>	MHz
Oscillator							
$t_{startup}$	start-up time	at maximum frequency	[1]	-	<tbd>	-	µs
PLL0							
$f_{i(PLL)}$	PLL input frequency			0.014	-	25	MHz
$f_{o(PLL)}$	PLL output frequency			4.3	-	550	MHz
		CCO; direct mode		275	-	550	MHz
PLL1							
$f_{i(PLL)}$	PLL input frequency			10	-	25	MHz
$f_{o(PLL)}$	PLL output frequency			10	-	160	MHz
		CCO; direct mode		156	-	320	MHz
Jitter specification for C_CAN							
$t_{jit(cc)(p-p)}$	cycle to cycle jitter (peak-to-peak value)	on CAN TD1 pin		-	<tbd>	<tbd>	ns

[1] Oscillator start-up time depends on the quality of the crystal. For most crystals it takes about 1000 clock pulses until the clock is fully stable.

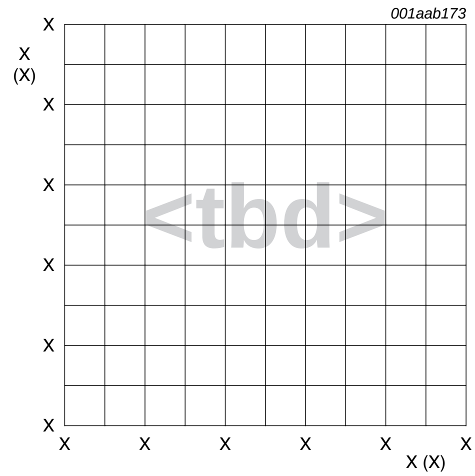


Fig 16. I/O delay versus $V_{DD(IO)}$ for digital I/O pins

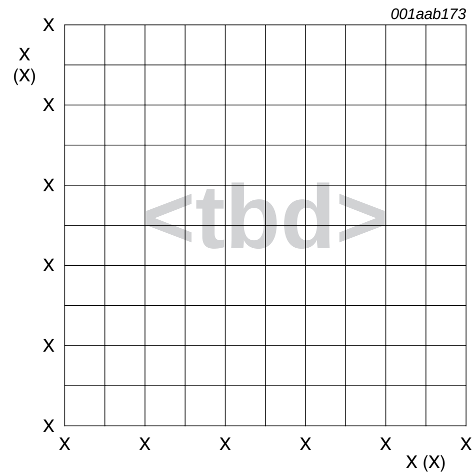


Fig 17. I/O delay versus $V_{DD(IO)}$ for CLKOUT pin

11.2 External clock

Table 9. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; $V_{DD(IO)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

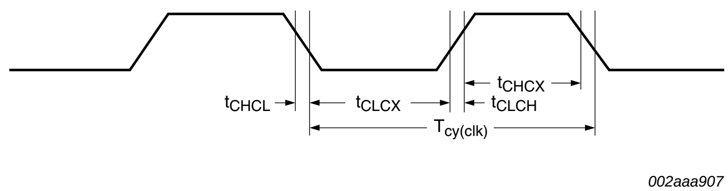


Fig 18. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.3 IRC and RTC oscillators

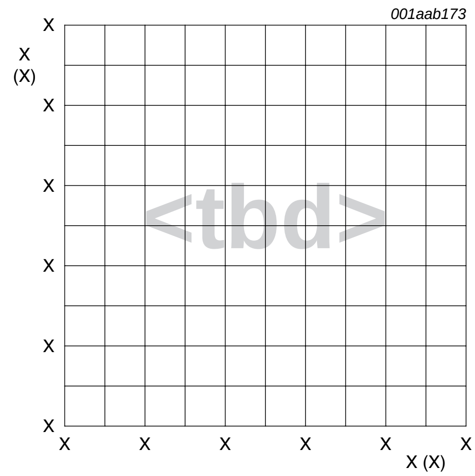
Table 10. Dynamic characteristic: IRC and RTC oscillators

T_{amb} = –40 °C to +85 °C; <tbd> ≤ $V_{DD(IO)}$ ≤ <tbd>.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	<tbd>	12.00	<tbd>	MHz
$f_{i(RTC)}$	RTC input frequency	-	-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1% accuracy is guaranteed for 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V and T_{amb} = –40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz 1 % accuracy specification for voltages below 2.7 V.

Fig 19. Internal RC oscillator frequency versus temperature

11.4 I²C-bus

Table 11. Dynamic characteristic: I²C-bus pins

T_{amb} = –40 °C to +85 °C.[1]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz
t_f	fall time [3][4][5][6]	of both SDA and SCL signals Standard-mode	-	300	ns
		Fast-mode	20 + 0.1 × C_b	300	ns
		Fast-mode Plus	-	120	ns

Table 11. Dynamic characteristic: I²C-bus pins

T_{amb} = –40 °C to +85 °C.[1]

Symbol	Parameter		Conditions	Min	Max	Unit
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	μs
			Fast-mode	1.3	-	μs
			Fast-mode Plus	0.5	-	μs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	μs
			Fast-mode	0.6	-	μs
			Fast-mode Plus	0.26	-	μs
$t_{HD;DAT}$	data hold time	[2][3][7]	Standard-mode	0	-	μs
			Fast-mode	0	-	μs
			Fast-mode Plus	0	-	μs
$t_{SU;DAT}$	data set-up time	[8][9]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[6] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[7] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[8] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[9] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

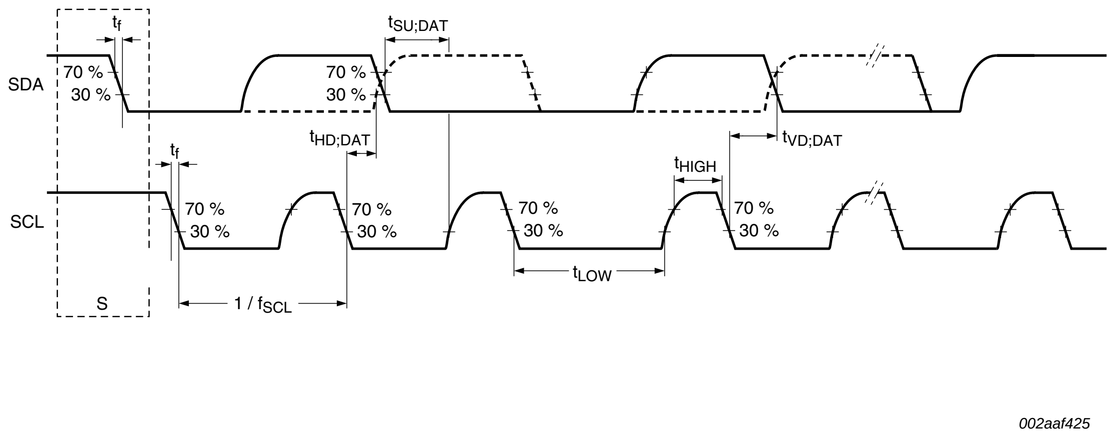


Fig 20. I²C-bus pins clock timing

11.5 SSP interface

Table 12. Dynamic characteristics: SSP pins in SPI mode

Symbol	Parameter	Conditions		Min	Max	Unit
$T_{cy(PCLK)}$	PCLK cycle time			<tbd>	-	ns
$T_{cy(clk)}$	clock cycle time		[1]	<tbd>	-	ns
SSP master						
t_{DS}	data set-up time	in SPI mode	[2]	<tbd>	$T_{cy(clk)}$	ns
t_{DH}	data hold time	in SPI mode	[2]	-	<tbd>	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	<tbd>	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	-	<tbd>	ns
SSP slave						
t_{DS}	data set-up time	in SPI mode	[3][4]	<tbd>	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	<tbd> × $T_{cy(PCLK)}$ + <tbd>	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	<tbd> × $T_{cy(PCLK)}$ + <tbd>	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	<tbd> × $T_{cy(PCLK)}$ + <tbd>	ns

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] T_{amb} = −40 °C to 85 °C; $V_{DD(REG)(3V3)}$ = 2.0 V to 3.6 V; $V_{DD(IO)}$ = 2.0 V to 3.6 V.

[3] $T_{cy(clk)}$ = 12 × $T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{DD(IO)}$ = 3.3 V.

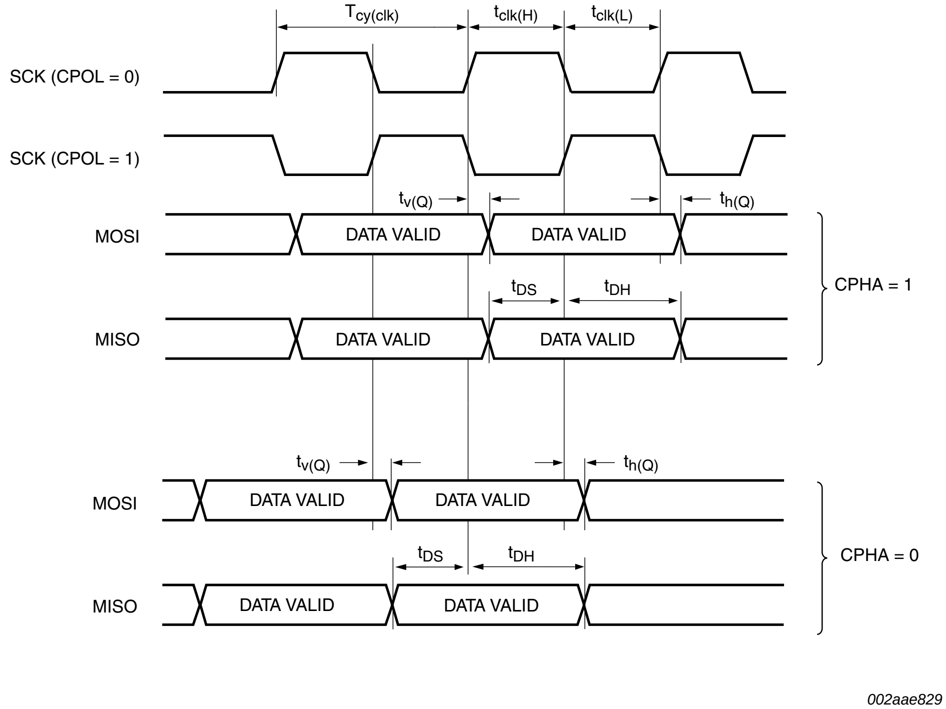


Fig 21. SSP master timing in SPI mode

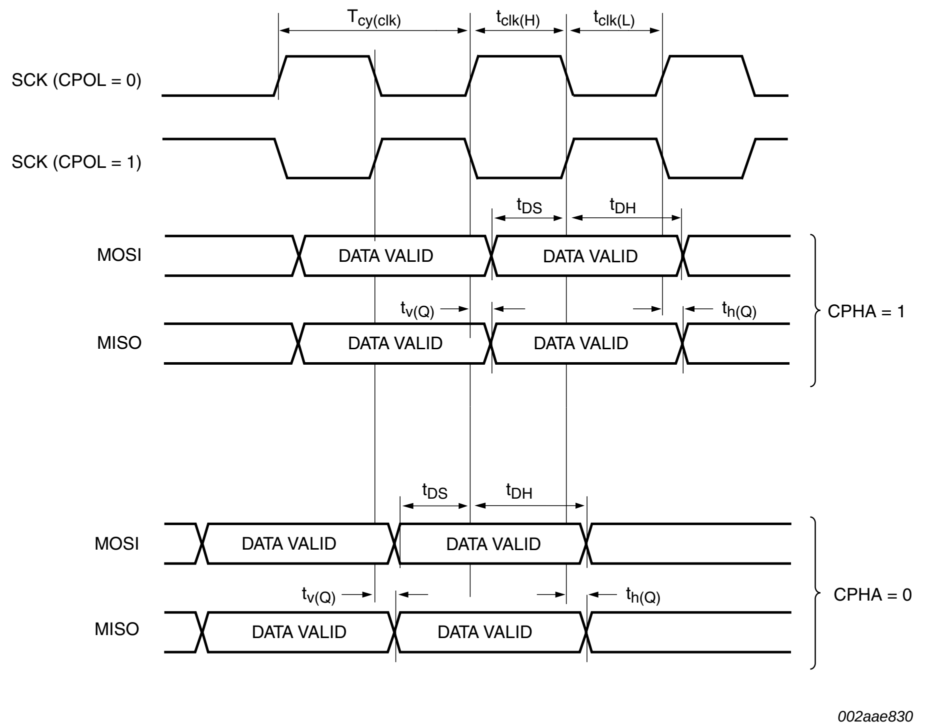


Fig 22. SSP slave timing in SPI mode

11.6 USART3 IrDA

Table 13. Dynamic characteristics: USART3 IrDA

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{r(tx)}$	transmit rise time		<tbd>	<tbd>	ns
$t_{f(tx)}$	transmit fall time		-	<tbd>	ns

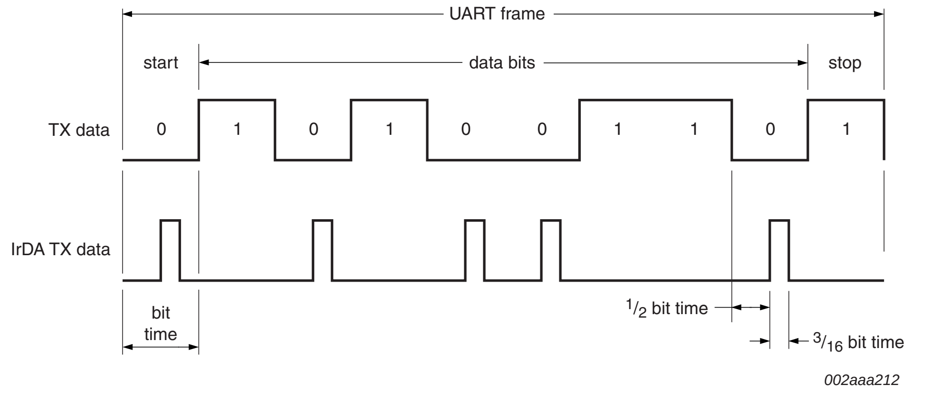


Fig 23. USART3 IrDA transmit timing

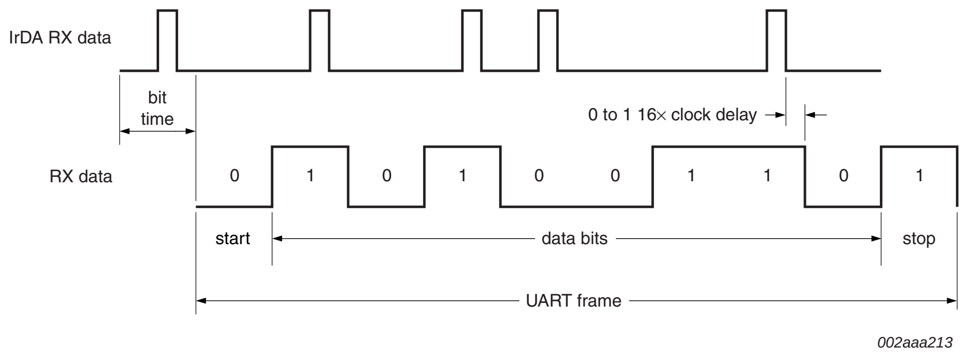


Fig 24. USART3 IrDA receive timing

11.7 Dynamic external memory interface

Table 14. Dynamic characteristics: Dynamic external memory interface

C_L = 30 pF; T_{amb} = −40 °C to 85 °C; $V_{DD(REG)(3V3)}$ and $V_{DD(IO)}$ over specified ranges <tbd>; AHB clock = <tbd> MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common						
$t_{d(SV)}$	chip select valid delay time		-	<tbd>	<tbd>	ns
$t_{h(S)}$	chip select hold time		<tbd>	<tbd>	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		-	<tbd>	<tbd>	ns
$t_{h(RAS)}$	row address strobe hold time		<tbd>	<tbd>	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		-	<tbd>	<tbd>	ns
$t_{h(CAS)}$	column address strobe hold time		<tbd>	<tbd>	-	ns
$t_{d(WV)}$	write valid delay time		-	<tbd>	<tbd>	ns
$t_{h(W)}$	write hold time		<tbd>	<tbd>	-	ns
$t_{d(GV)}$	output enable valid delay time		-	<tbd>	<tbd>	ns
$t_{h(G)}$	output enable hold time		<tbd>	<tbd>	-	ns
$t_{d(AV)}$	address valid delay time		-	<tbd>	<tbd>	ns
$t_{h(A)}$	address hold time		<tbd>	<tbd>	-	ns
Read cycle parameters						
$t_{su(D)}$	data input set-up time		<tbd>	<tbd>	-	ns
$t_{h(D)}$	data input hold time		<tbd>	<tbd>	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time		-	<tbd>	<tbd>	ns
$t_{h(Q)}$	data output hold time		<tbd>	<tbd>	-	ns

11.8 Static external memory interface

Table 15. Dynamic characteristics: Static external memory interface

C_L = 30 pF; T_{amb} = −40 °C to 85 °C; $V_{DD(REG)(3V3)}$ and $V_{DD(IO)}$ over specified ranges <tbd>; AHB clock = 1 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common to read and write cycles[1]						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time		<tbd>	<tbd>	<tbd>	ns
Read cycle parameters[1][2]						
t_{OELAV}	$\overline{OE}$ LOW to address valid time		<tbd>	<tbd>	<tbd>	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		<tbd> + $T_{cy(CCLK)}$ × WAITOEN	0 + $T_{cy(CCLK)}$ × WAITOEN	<tbd> + $T_{cy(CCLK)}$ × WAITOEN	ns
t_{am}	memory access time	[3][4]	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − <tbd>	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − <tbd>	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − <tbd>	ns
$t_{h(D)}$	data input hold time	[5]	<tbd>	<tbd>	<tbd>	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		<tbd>	<tbd>	<tbd>	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		<tbd>	<tbd>	<tbd>	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time		<tbd> + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	0 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	<tbd> + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	
t_{BLSLAV}	$\overline{BLS}$ LOW to address valid time		<tbd>	<tbd>	<tbd>	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time		<tbd>	<tbd>	<tbd>	ns
Write cycle parameters[1][6]						
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time		<tbd> + $T_{cy(CCLK)}$ × (1 + WAITWEN)	<tbd> + $T_{cy(CCLK)}$ × (1 + WAITWEN)	<tbd> + $T_{cy(CCLK)}$ × (1 + WAITWEN)	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time		<tbd>	<tbd>	<tbd>	ns
t_{WELDV}	$\overline{WE}$ LOW to data valid time		<tbd>	<tbd>	<tbd>	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		<tbd>	<tbd>	<tbd>	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[3]	<tbd> + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	0 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	<tbd> + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[3]	<tbd> + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 3)	0 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 3)	<tbd> + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 3)	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	[3]	<tbd> + $T_{cy(CCLK)}$	<tbd> + $T_{cy(CCLK)}$	<tbd> + $T_{cy(CCLK)}$	ns

Table 15. Dynamic characteristics: Static external memory interface *…continued*
C_L = 30 pF; T_{amb} = −40 °C to 85 °C; $V_{DD(REG)(3V3)}$ and $V_{DD(IO)}$ over specified ranges <tbd>; AHB clock = 1 MHz

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time		[3]	<tbd>	<tbd>	<tbd>	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time		[3]	<tbd>	<tbd>	<tbd>	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time		[3]	<tbd>	<tbd>	<tbd>	ns

[1] V_{OH} = 2.5 V, V_{OL} = 0.2 V.

[2] V_{IH} = 2.5 V, V_{IL} = 0.5 V.

[3] $T_{cy(CCLK)}$ = 1/CCLK.

[4] Latest of address valid, $\overline{CS}$ LOW, $\overline{OE}$ LOW to data valid.

[5] Earliest of $\overline{CS}$ HIGH, $\overline{OE}$ HIGH, address change to data invalid.

[6] Byte lane state bit (PB) = 1.

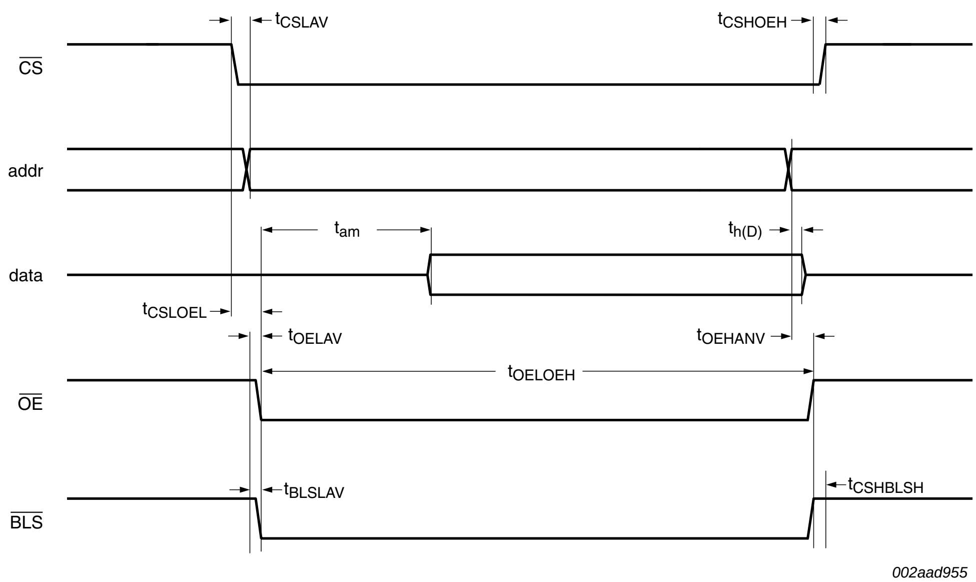


Fig 25. Static external memory controller read access

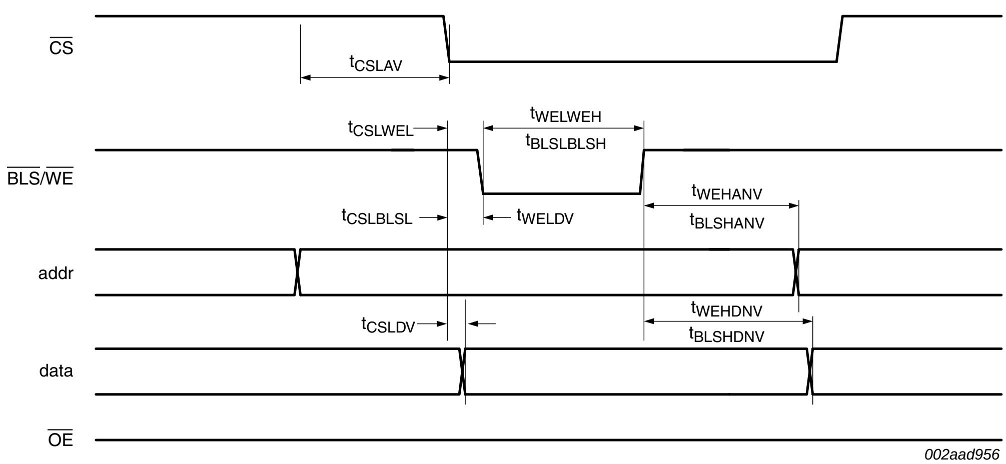


Fig 26. Static external memory controller write access

12. ADC/DAC electrical characteristics

Table 16. ADC characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = –40 °C to +85 °C; ADC frequency 4.5 MHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	$V_{DDA(3V3)}$	V
C_{ia}	analog input capacitance		-	-	<tbd>	pF
E_D	differential linearity error	[1][2][3]	-	-	<tbd>	LSB
$E_{L(adj)}$	integral non-linearity	[1][4]	-	-	<tbd>	LSB
E_O	offset error	[1][5]	-	–	<tbd>	LSB
E_G	gain error	[1][6]	-	-	<tbd>	%
E_T	absolute error	[1][7]	-	-	<tbd>	LSB
R_{vsi}	voltage source interface resistance	[8]	-	-	<tbd>	kΩ
R_i	input resistance	[9][10]	-	-	<tbd>	MΩ
$f_{clk(ADC)}$	ADC clock frequency		-	-	<tbd>	MHz
$f_{c(ADC)}$	ADC conversion frequency		-	-	<tbd>	kSamples/s

[1] Conditions: V_{SSA} = 0 V, $V_{DDA(3V3)}$ = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 27.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 27.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 27.

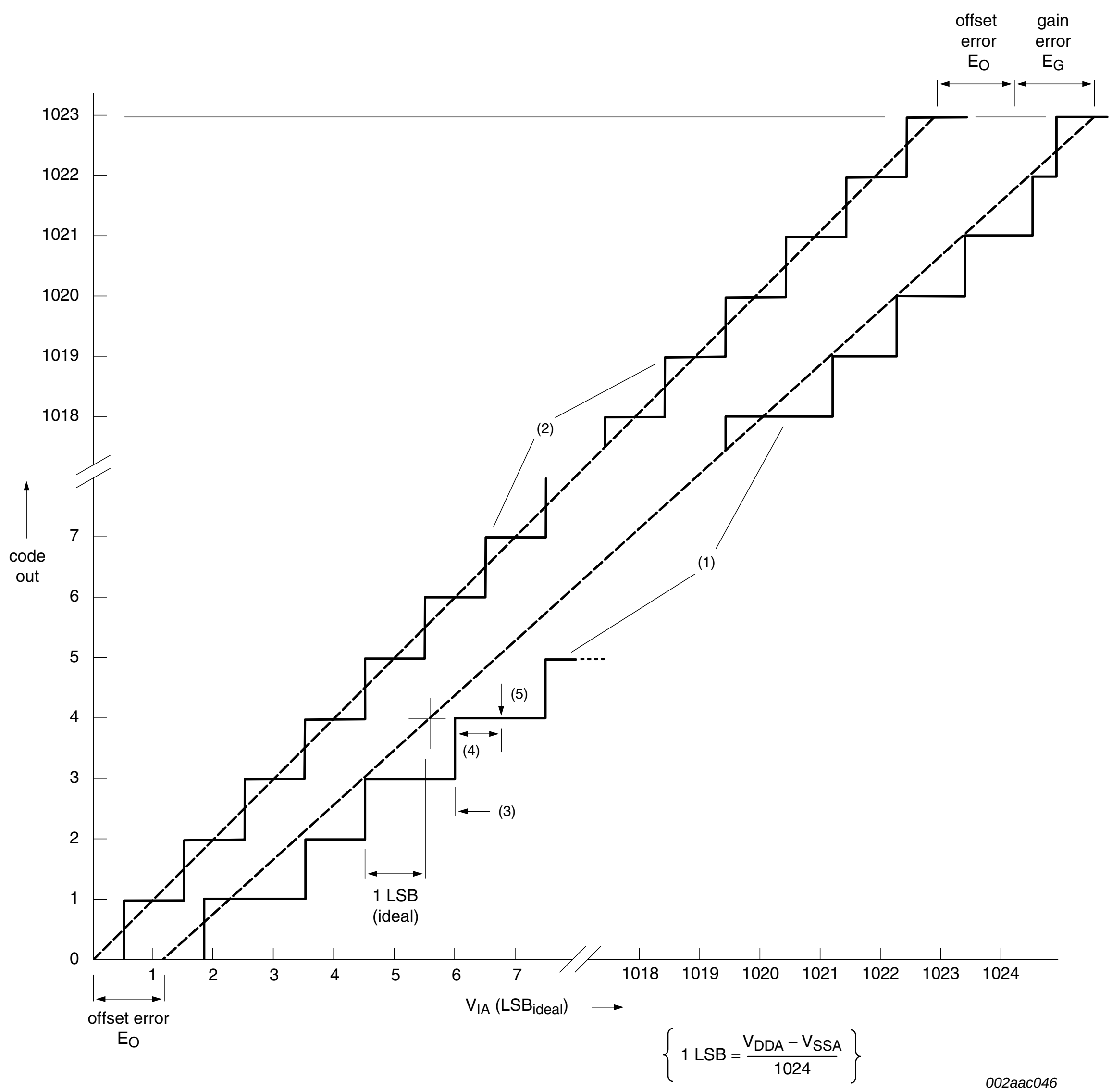
[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 27.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 27.

[8] See <tbd>.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 4.5 MHz and analog input capacitance C_{ia} = 1pF.

[10] Input resistance R_i depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

(6) V_{DDA} refers to $V_{DDA(3V3)}$ on pin VDDA and V_{SSA} to analog ground on pin VSSA.

Fig 27. 10-bit ADC characteristics

Table 17. DAC electrical characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = –40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
E_D	differential linearity error		-	<tbd>	-	LSB
$E_{L(adj)}$	integral non-linearity		-	<tbd>	-	LSB
E_O	offset error		-	<tbd>	-	%
E_G	gain error		-	<tbd>	-	%
C_L	load capacitance		-	<tbd>	-	pF
R_L	load resistance		<tbd>	-	-	kΩ

13. Application information

13.1 XTAL1 input

The input voltage to the on-chip oscillators is limited to 1.2 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed.

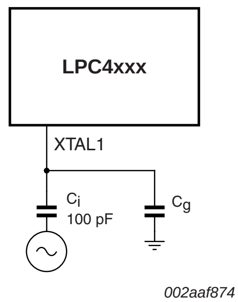


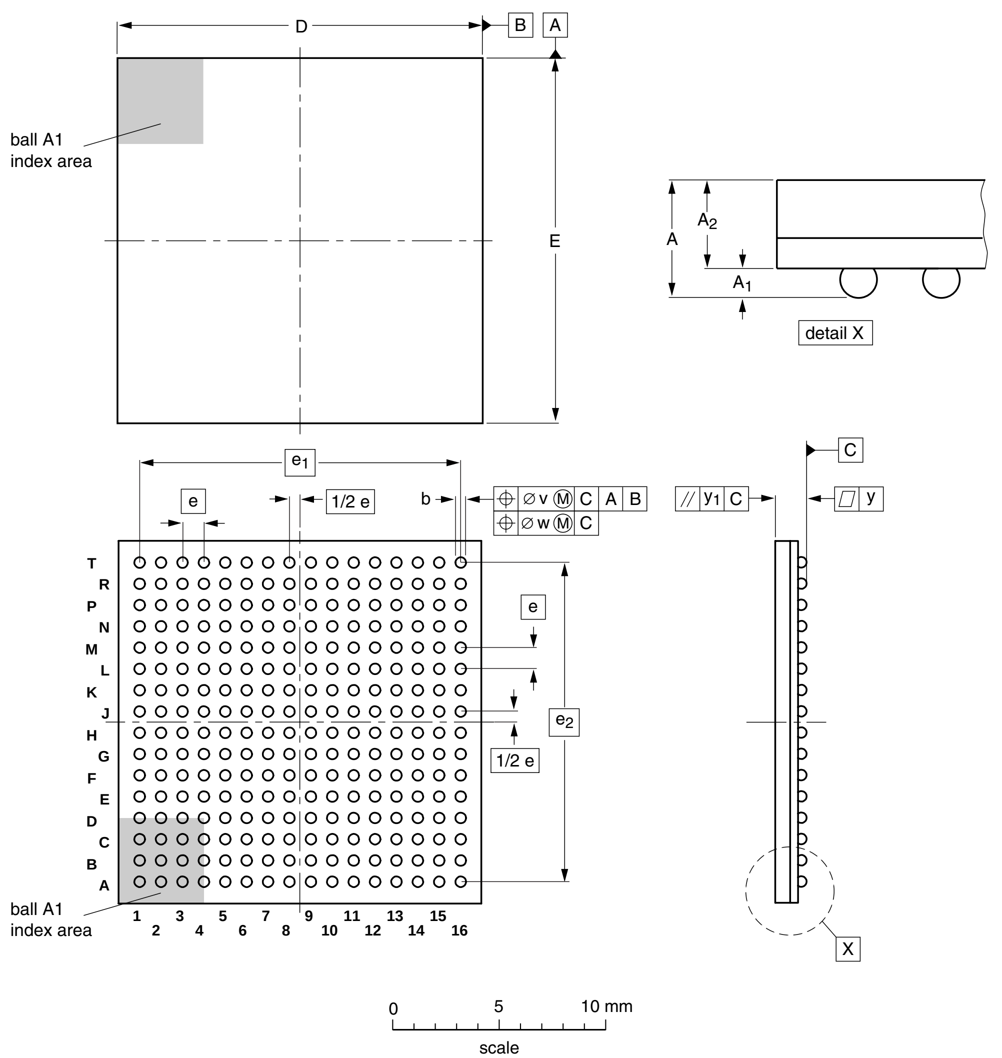
Fig 28. Slave mode operation of the on-chip oscillator

13.2 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

14. Package outline

LBGA256: plastic low profile ball grid array package; 256 balls; body 17 x 17 x 1 mm **SOT740-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.55	0.45 0.35	1.1 0.9	0.55 0.45	17.2 16.8	17.2 16.8	1	15	15	0.25	0.1	0.12	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT740-2	- - -	MO-192	- - -			~~05-06-16~~ 05-08-04

Fig 29. Package outline LBGA256 package sot740_2

15. Abbreviations

Table 18. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
BOD	BrownOut Detection
CAN	Controller Area Network
CMAC	Cipher-based Message Authentication Code
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DAC	Digital-to-Analog Converter
DC-DC	Direct Current-to-Direct Current
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MAC	Media Access Control
MCU	MicroController Unit
MIIM	Media Independent Interface Management
n.c.	not connected
OHCI	Open Host Controller Interface
OTG	On-The-Go
PHY	Physical Layer
PLL	Phase-Locked Loop
PMC	Power Mode Control
PWM	Pulse Width Modulator
RIT	Repetitive Interrupt Timer
RMII	Reduced Media Independent Interface
SDRAM	Synchronous Dynamic Random Access Memory
SIMD	Single Instruction Multiple Data
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TCP/IP	Transmission Control Protocol/Internet Protocol
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface

Table 18. Abbreviations *…continued*

Acronym	Description
USART	Universal Synchronous Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
UTMI	USB2.0 Transceiver Macrocell Interface

16. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC4350_30_20_10 v.1	20101029	Objective data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contents

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Date of release: 29 October 2010

Document identifier: LPC4350_30_20_10