DATA SHEET

PCF8832
STN RGB - 384 output column driver

Preliminary specification

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Philips
Semiconductors

PHILIPS

CONTENTS

STN RGB - 384 output column driver PCF8832

1 FEATURES

- LCD controller or column driver
- 384 column outputs (128 × RGB)
- Display data RAM 168 × 128 (RGB)
- 256 colours (RGB = 332)
- Blue intermediate grey scales are alterable with a command
- Interface compatibilities:
  - I^2C-bus
  - 8-bit parallel interface (8080 Intel CPU or 6800 Motorola CPU)
  - 3-line or 4-line Serial Peripheral Interface (SPI)
  - 3-line serial interface
- Display features:
  - Area scrolling
  - Partial display mode with MUX rate 1 : 8 to 1 : 160
  - Landscape or portrait mode
  - Software-programmable grey scale method
  - N-line inversion
- On-chip:
  - Oscillator for display system requires no external components (external clock is also possible)
  - Generation of V_{COL} and V_M
  - Switching regulator controller for generation of row voltages (V_H and V_L)
  - Row-driver control and configuration logic
- Logic supply voltage range from 1.5 to 3.3 V
- Analog supply voltage range from 2.4 to 3.5 V for V_{COL} generation
- Analog supply voltage range for V_H and V_L generation: 2.4 to 3.5 V
- Display supply voltage range from 2.5 to 4.0 V
- Low power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Manufactured in silicon gate CMOS process
- Optimizes layout for COF, COG and TCP assembly.

2 APPLICATIONS

- Mobile phones
- Personal Digital Assistant (PDA)
- Automotive information systems
- Point-of-sale terminals
- Instrumentation.

3 GENERAL DESCRIPTION

The PCF8832 column driver is a low power CMOS LCD controller, column driver and power supply controller that drives colour STN displays together with a suitable row driver. The column driver offers four microcontroller interfaces (8080-type system, 6800-type system, SPI and I^2C-bus).

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8832U	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

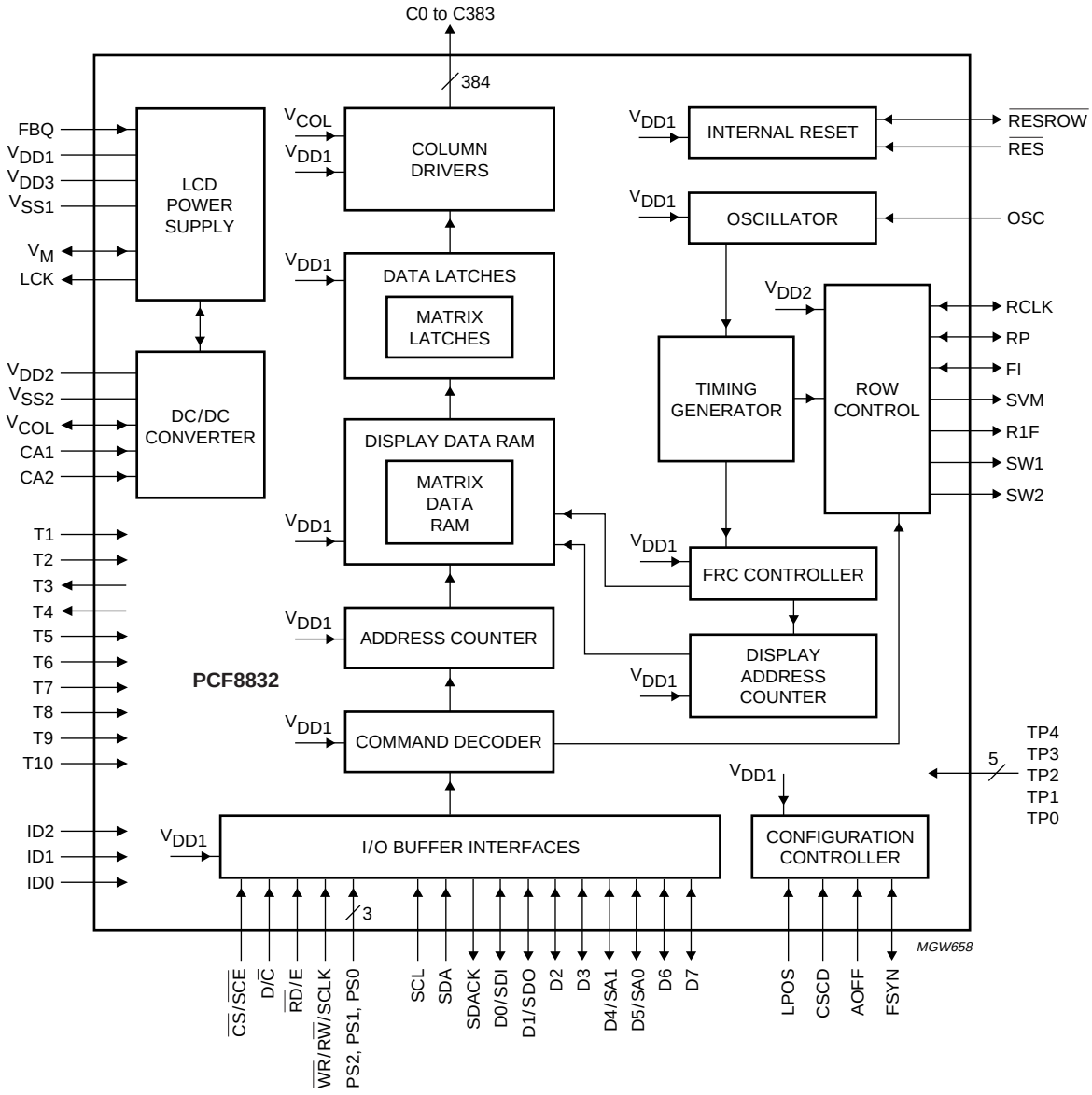


Fig.1 Block diagram.

6 PINNING

SYMBOL	PAD[1]	TYPE	DESCRIPTION
C0 to C47 C48 to C71 C72 to C311 C312 to C335 C336 to C383	184 to 231 235 to 258 261 to 122 2 to 25 29 to 76	O	LCD column outputs
FSYN	77	I/O	test input/output
RCLK	78	I/O	row driver clock input/output
RP	79	I/O	start frame scan input/output
FI	80	I/O	inversion signal input/output
SVM	81	O	select row-off level output
$\overline{\text{RESROW}}$	82	I/O	row driver reset input/output
R1F	83	O	output to select shift register order
SW1	84	O	output to swap/no swap register 1
SW2	85	O	output to swap/no swap register 2
V_M	86 to 91	I/O PS	MID-level column driving voltage (level between V_{COL} and V_{SS})
LCK	92	O	output clock for the switching regulator
T8 T7 T6	93 94 95	I	test inputs; note 2
FBQ	96	I	feedback input from inductive DC-to-DC convertor
T4	97	O	test output; note 3
V_{COL}	98 to 103	I/O PS	HIGH-level column driving voltage
CA1 CA2	104 to 109 110 to 115	I	capacitor connections for DC-to-DC convertor
V_{SS2}	116 to 121	PS	system ground
V_{SS1}	122 to 127	PS	system ground
TP0 TP1 TP2 TP3 TP4	128 129 130 131 132	I	trimming inputs for $v_{H(reg)}$
T1	133	I	test input; note 4
OSC	134	I	external clock input or external resistor connection; note 5
T5 T2	135 136	I	test inputs; note 4
ID0 ID1 ID2	137 138 139	I	manufacturer code input; note 6
LPOS	140	I	input indicating a left-sided chip
CSCD	141	I	configuration setting

SYMBOL	PAD(1)	TYPE	DESCRIPTION
AOFF	142	I	analog circuits on/off switching input
PS0 PS1 PS2	143 144 145	I	serial or parallel interface mode setting inputs
V_{DD1}	146 to 151	PS	logic power supply voltage
V_{DD2}	152 to 157	PS	capacitive booster supply voltage
V_{DD3}	158 to 160	PS	analog power supply voltage
T9	161, 162	I	test input; note 7
T10	163, 164	I	test input; note 7
D0/SDI	165	I/O	parallel or serial data input/output
D1/SDO	166	I/O	parallel or serial data input/output
D2	167	I/O	parallel data input/output
D3	168	I/O	parallel data input/output
D4/SA1	169	I/O	parallel data or I^2C-bus slave address input/output
D5/SA0	170	I/O	parallel data or I^2C-bus slave address input/output
D6	171	I/O	parallel data input/output
D7	172	I/O	parallel data input/output
$\overline{RES}$	173	I	external reset input, active LOW
$\overline{CS}/\overline{SCE}$	174	I	chip select parallel interface or serial chip enable input
$\overline{RD}$/E	175	I	read clock (8080) or clock (6800) input
$\overline{WR}/R\overline{W}$/SCLK	176	I	write clock (8080) or read write selector (6800) or serial clock input
D/$\overline{C}$	177	I	data or command indicator input
T3	178	O	test output; note 3
SDA	179, 180	I	I^2C-bus data input
SDACK	181	O	I^2C-bus acknowledge output
SCL	182, 183	I	I^2C-bus clock input

Notes

1. Dummy pads are located at positions 1, 26, 27, 28, 232, 233, 234, 259 and 260.
2. Must be connected to V_M in the application.
3. Must be left open-circuit in the application.
4. Must be connected to V_{SS1} in the application.
5. If an external clock is applied, the internal oscillator must be switched off with a software command.
6. Pads ID2, ID1 and ID0 must be connected; manufacturer code recommended for Philips ID2 = ID1 = ID0 = 0.
7. Must be connected to V_{DD1} in the application.

7 FUNCTIONAL DESCRIPTION

7.1 I/O buffer and interface

The interface is the connection between the outside world and PCF8832. One of five industrial standard interfaces can be selected using the interface configuration inputs PS2, PS1 and PS0.

7.2 Configuration control

It is possible to configure the PCF8832s to use external voltages, see Table 2.

Table 1 Default configuration settings

INPUT	DEFAULT VALUE
CSCD	0
FSYN	0
LPOS	1

Table 2 Analog circuit configuration

ANALOG SWITCHING0	EFFECT
AOFF = 0	analog part active
AOFF = 1	analog part switched off, analog voltages are input through V_{COL}, V_M

7.3 Oscillator

The on-chip oscillator provides the clock signal for the display system. An external clock signal, if used, is connected to the OSC input. In this case the internal oscillator must be switched off by a software command. To improve the timing accuracy there is an external resistor option. If this option is used, the external resistor must be connected between OSC and V_{DD1} and the appropriate register must be set. If the internal resistor is selected, the OSC input must be left open-circuit.

7.4 Display data RAM

The Display Data RAM (DDRAM) is a $128 \times 9 \times 168$-bit static RAM for display data storage. During RAM access, data is transferred to the DDRAM via the interface.

7.5 Address counter

The address counter sets the addresses of the display data RAM for writing operations.

7.6 Display address counter

The display is generated by continuously reading-out rows of RAM data to the dot matrix LCD via the column outputs. The display status (all dots on/off and normal/inverse video) is set via the interface.

7.7 Command decoder

The command decoder identifies command words arriving at the interface and routes the following data bytes to their destination.

7.8 DC-to-DC converter

The voltage multiplier generates the required column voltage V_{COL}. Pins CA1 and CA2 must be connected to an external capacitor. If the capacitive DC-to-DC converter is switched off by AOFF = 1, then V_{COL} must be supplied externally.

7.9 LCD power supply

The LCD power supply block generates the row voltage level V_M (equivalent to $\frac{V_{COL}}{2}$). If the LCD power supply is switched off by AOFF = 1, then V_M must be supplied from an external source.

7.10 Internal reset

The internal reset circuit handles hardware and software resets, provides the reset signal required internally and controls the reset signal for the row driver IC.

7.11 Timing generator

The timing generator produces the various signals required to coordinate the column driver with the row driver.

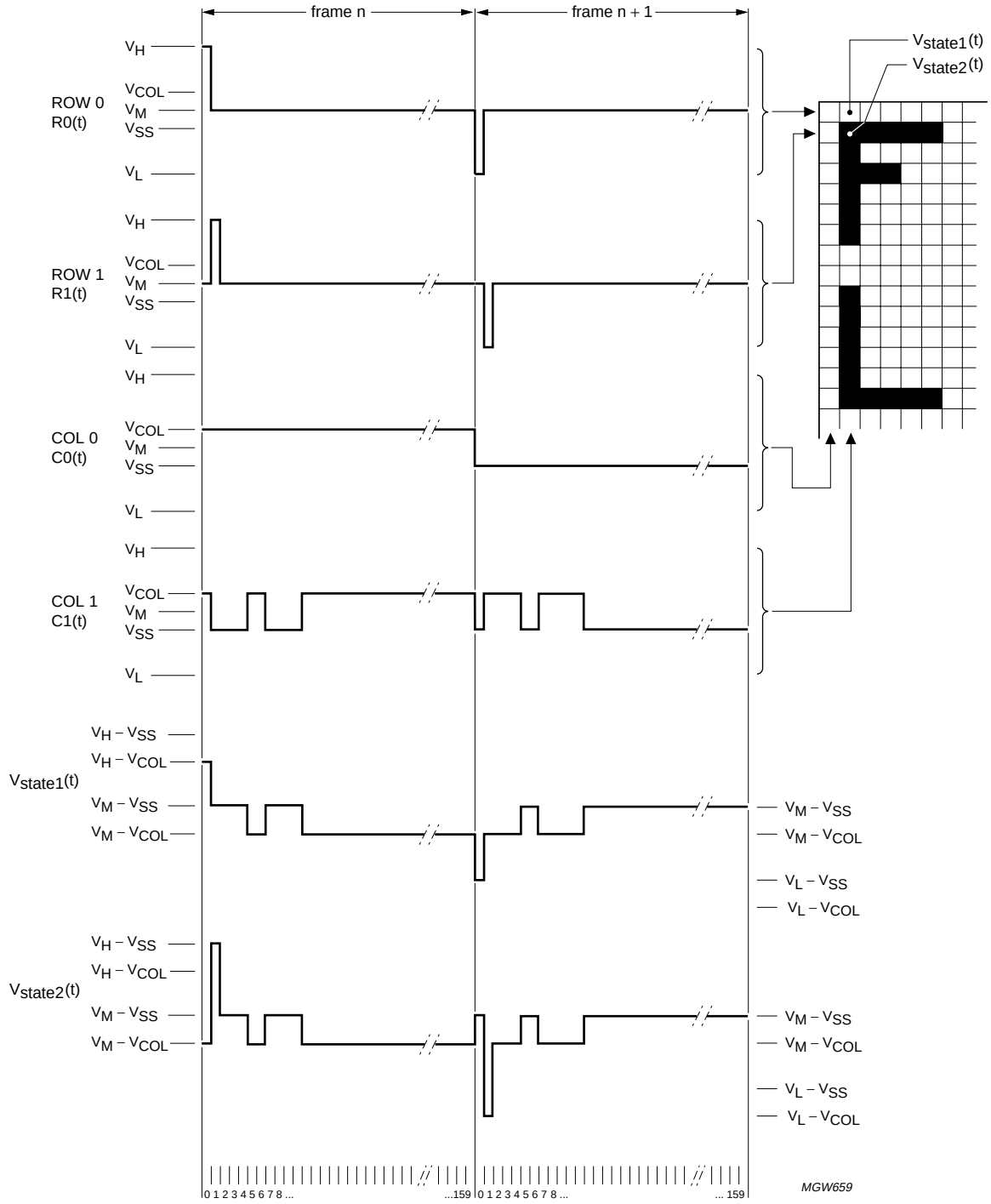
7.12 Row driver control

The row driver IC is controlled completely by commands from the column driver.

7.13 Column drivers and data latches

The LCD drive section includes 128×3 column outputs (C0 to C383) which should be connected directly to the LCD. The column output signals are generated in accordance with the data in the display latches. The data are loaded from the display RAM when the corresponding row signal is active. Unused column outputs should be left open-circuit when less than 384 columns are required.

7.14 LCD waveforms and DDRAM to data mapping



(1) $V_{state1}(t) = R0(t) - C1(t)$.
(2) $V_{state2}(t) = R1(t) - C1(t)$.

Fig.2 Typical LCD driver waveforms.

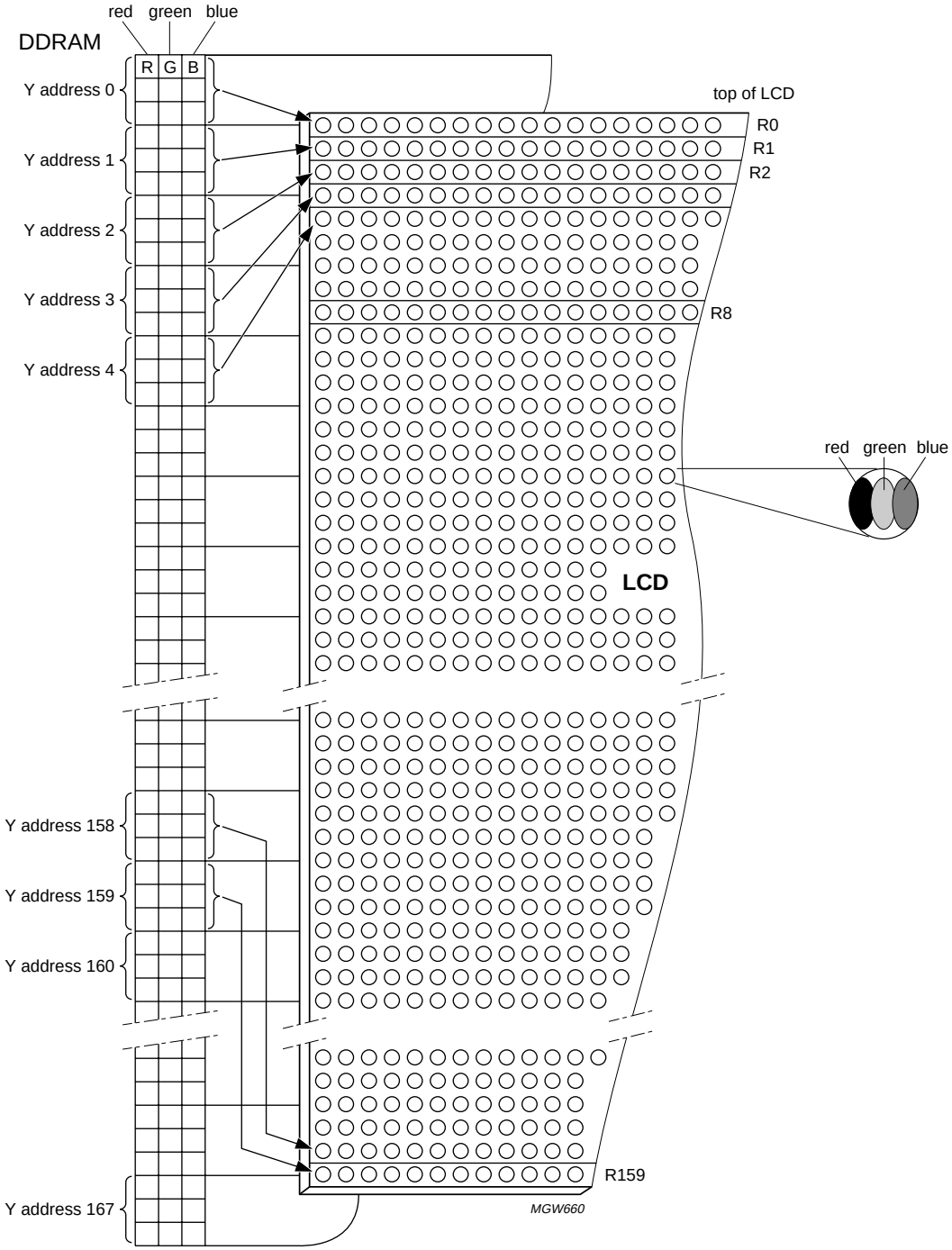


Fig.3 DDRAM-to-display mapping.

7.15 Frame rate control

The FRC controller generates the RGB grey scales by means of frame rate control. There are two FRC options, selectable via software commands, to give 9-frame or 7-frame working. For every pixel, eight shades of grey are created over the number of frames of the selected option.

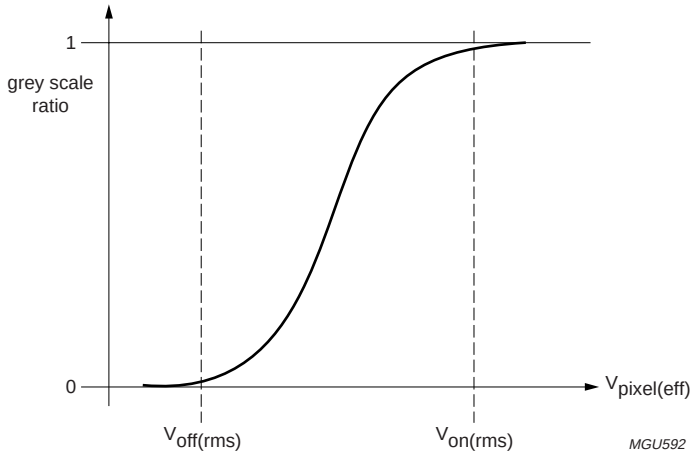


Fig.4 Grey scale ratio as a function of effective pixel voltage.

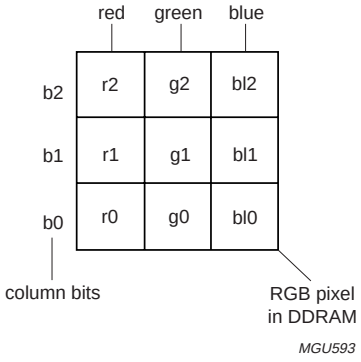


Fig.5 Pixel bit definition.

7.15.1 Frame rate control with 9 frames

Table 3 Grey scale encoding; 9 frames

b2	b1	b0	EFFECTIVE PIXEL VOLTAGE
0	0	0	$^0/_9$ $V_{off(rms)}$
0	0	1	$^2/_9$
0	1	0	$^3/_9$
0	1	1	$^4/_9$
1	0	0	$^5/_9$
1	0	1	$^6/_9$
1	1	0	$^7/_9$
1	1	1	$^9/_9$ $V_{on(rms)}$

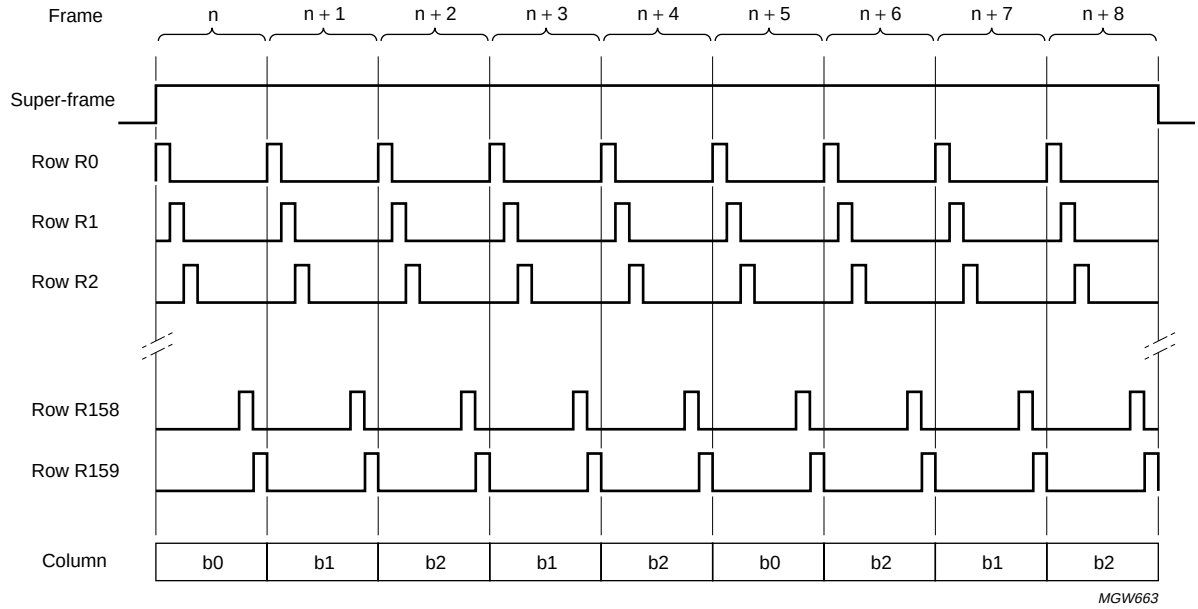


Fig.6 FRC driving scheme with 9 frames.

7.15.2 Frame rate control with 7 frames

Table 4 Grey scale encoding; 7 frames

b2	b1	b0	EFFECTIVE PIXEL VOLTAGE
0	0	0	$^0/_7$ $V_{off(rms)}$
0	0	1	$^1/_7$
0	1	0	$^2/_7$
0	1	1	$^3/_7$
1	0	0	$^4/_7$
1	0	1	$^5/_7$
1	1	0	$^6/_7$
1	1	1	$^7/_7$ $V_{on(rms)}$

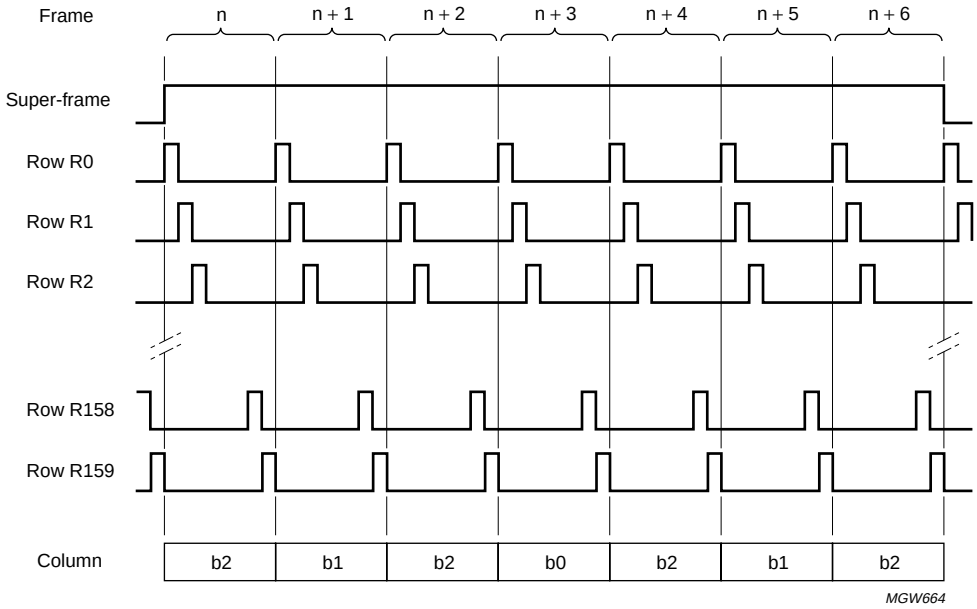


Fig.7 FRC driving scheme with 7 frames.

7.16 Waveforms with frame inversion or n-line inversion

The PCF8832 offers the possibility of using different waveforms. Figure 8 shows the standard Alt and Pleshko (APT) frame inversion waveforms. N-line inversion, synchronized and asynchronous to the frame, are shown in Figs 9 and 10. Selection of one of these options is made via software command.

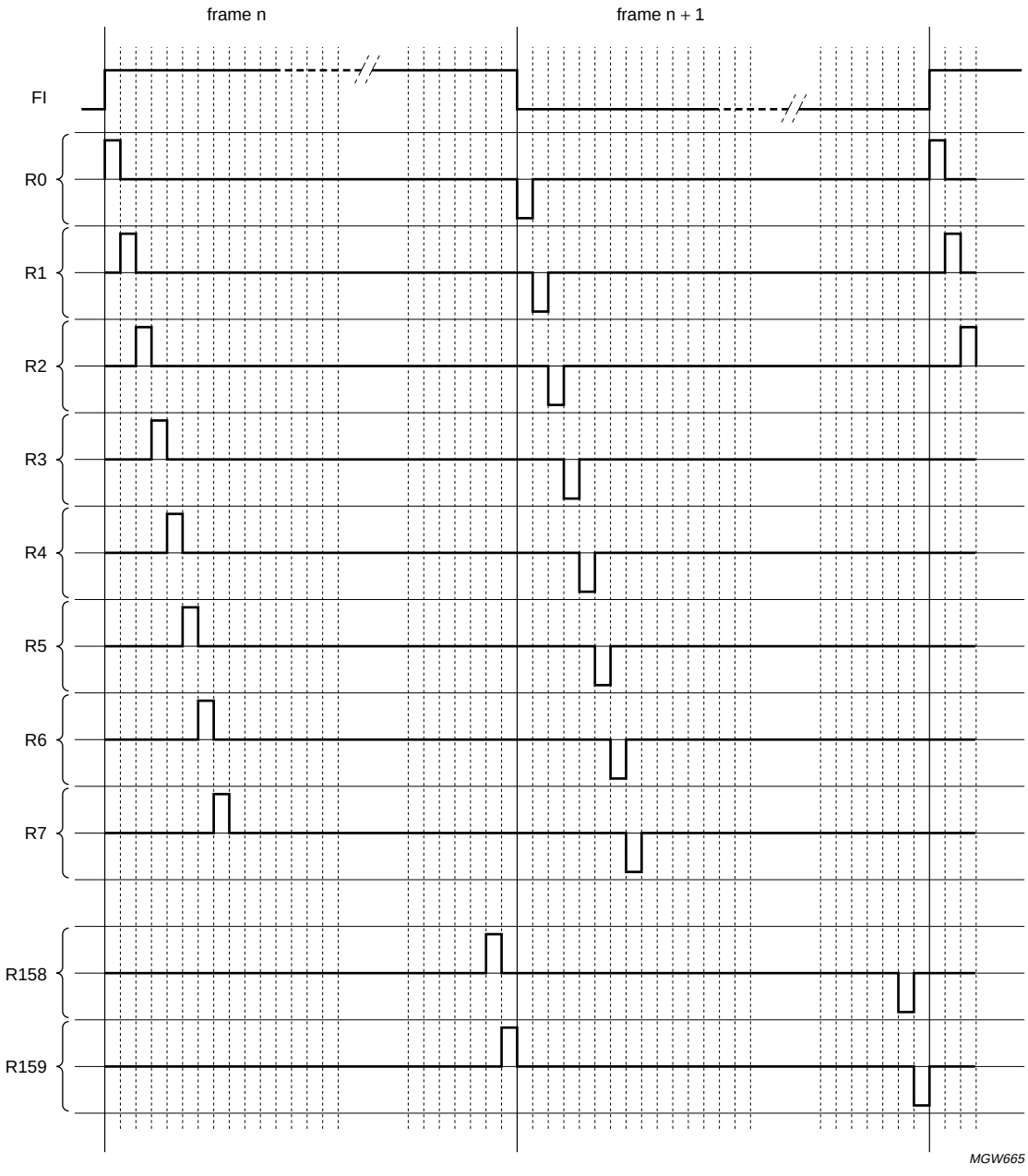


Fig.8 Frame inversion.

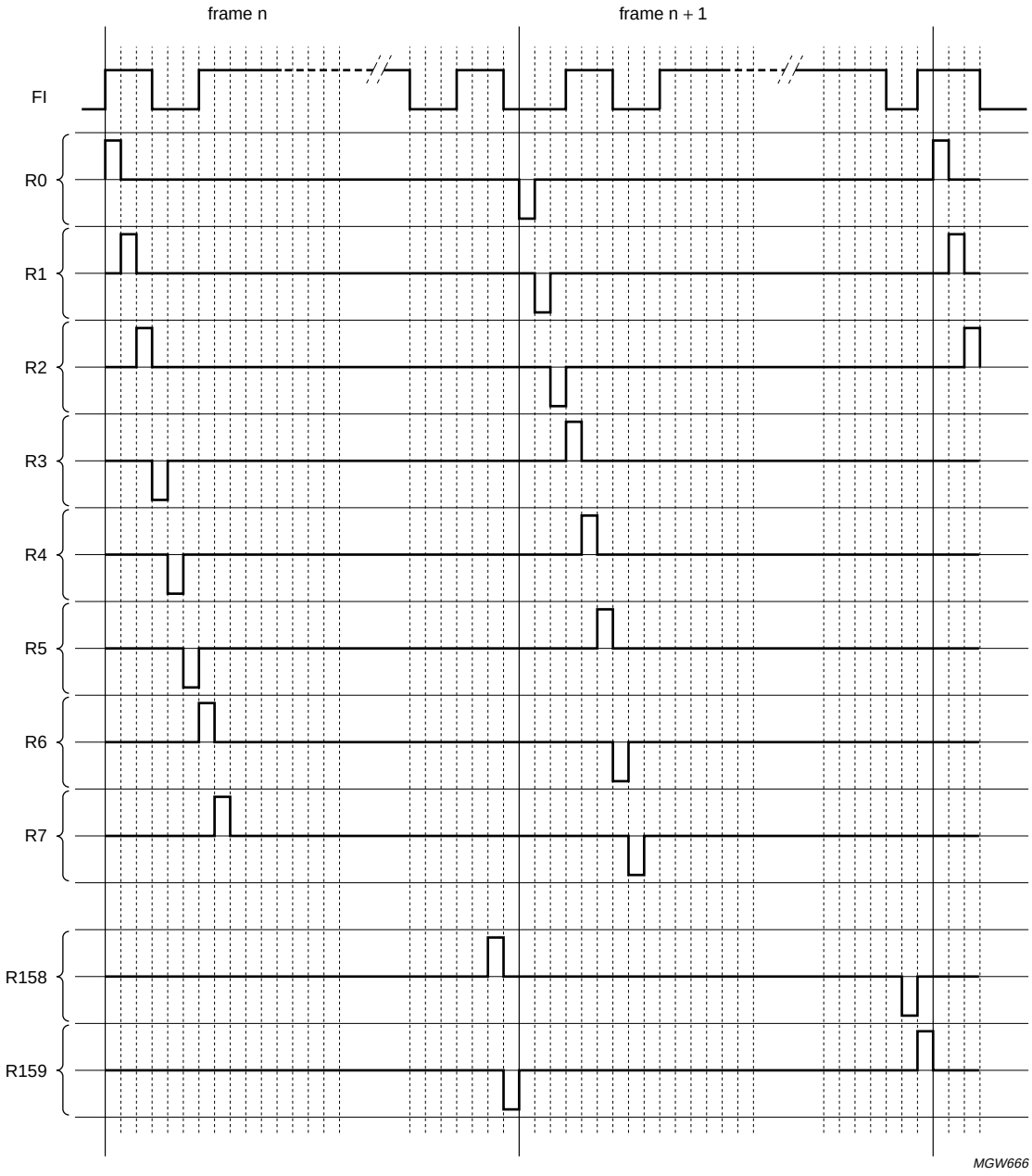


Fig.9 N-line inversion, synchronized with frame.

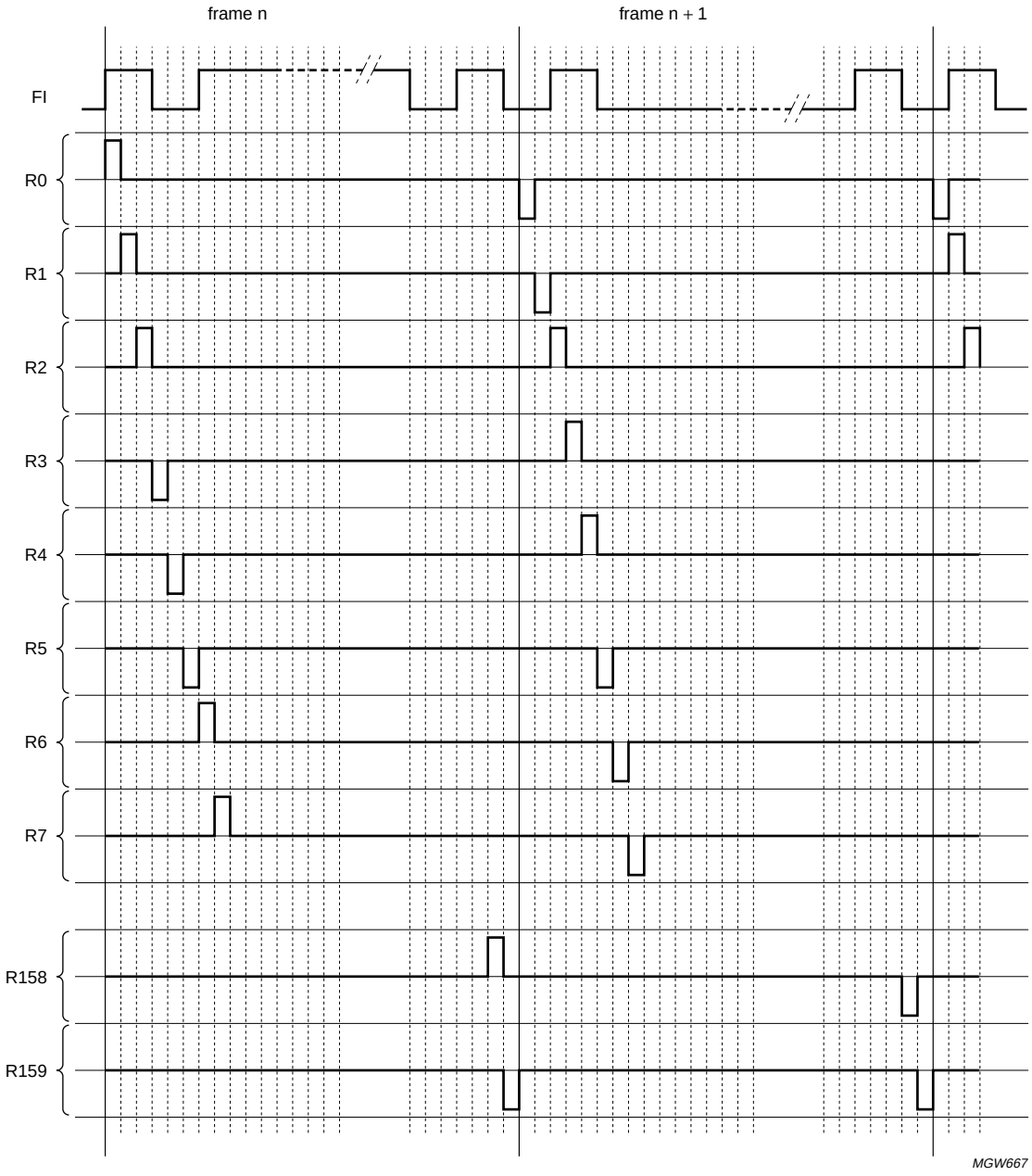


Fig.10 N-line inversion, not synchronized with frame.

7.17 DDRAM addressing

Data is written byte-wise into the RAM matrix of the PCF8832 as illustrated in Fig.11. The display RAM has a matrix of 168 × 128 × 9 bits. RAM locations are addressed by the address pointers. The address ranges are X = 0 to X = 127 (7F) and Y = 0 to Y = 167 (A7H). Addresses outside of these ranges are not allowed.

Before writing to the RAM, a window must be defined into which it can be written. The window is programmable via the command registers with xs and ys designating the start address, and xe and ye designating the end address. If, for example, the whole display content is to be written, the window is defined by the following values: xs = 0 (0H), ys = 0 (0H), xe = 127 (7FH) and ys = 159 (9FH).

In vertical addressing mode (V = 1), the Y-address increments after each byte. After the last Y-address (Y = ye), Y wraps around to ys and X increments to address the next column. In horizontal addressing mode (V = 0), the X-address increments after each byte. After the last X-address (X = xe), X wraps around to xs and Y increments to address the next row. After the very last address (X = xe and Y = ye) the address pointers wrap around to address (X = xs and Y = ys). For flexibility in handling a wide variety of display architectures, the commands ‘RAM data addressing’ and ‘data control’ define flags MX, MY and L, which allows mirroring of the X and Y-addresses and selection of landscape or portrait mode. All combinations of flags are allowed. The available combinations of writing to the display RAM are shown in Figs 12 to 17. When MX, MY, V or L are changed, the data must be rewritten to the display RAM.

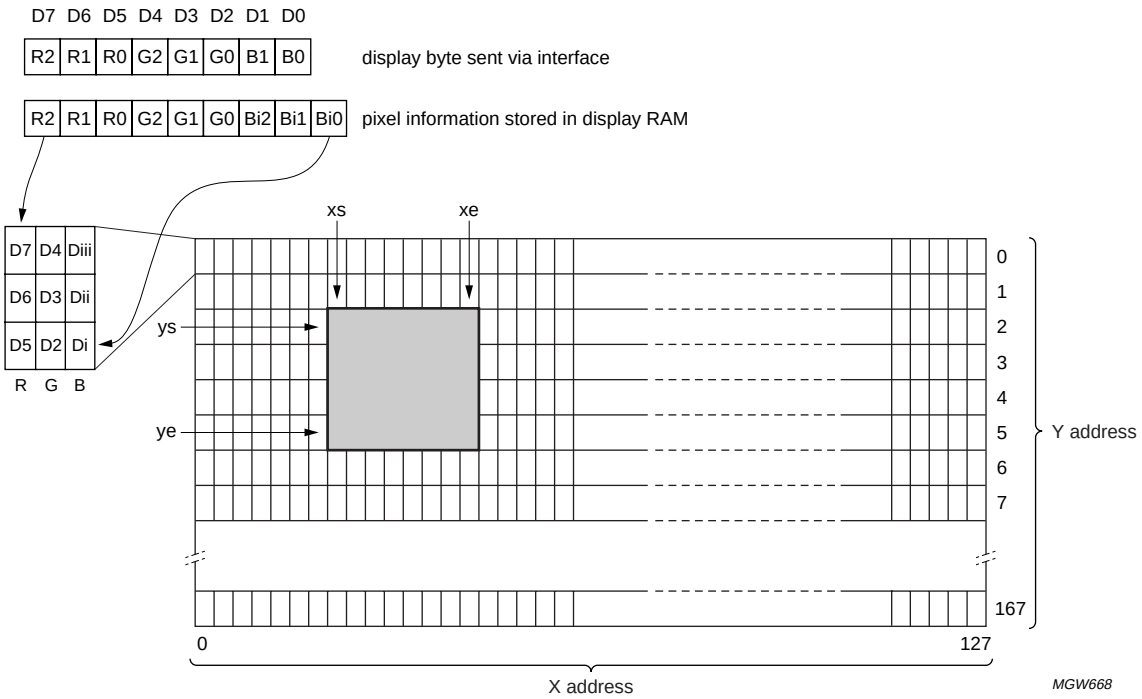
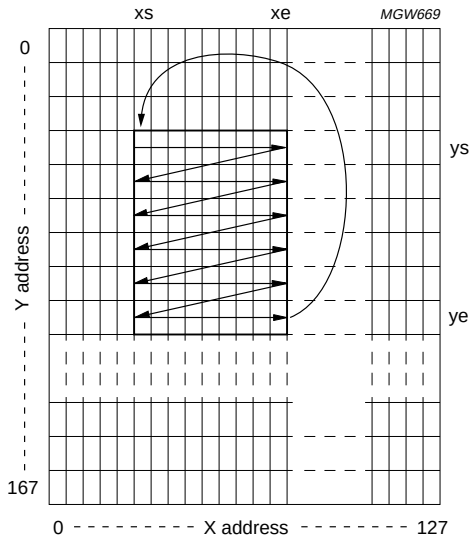
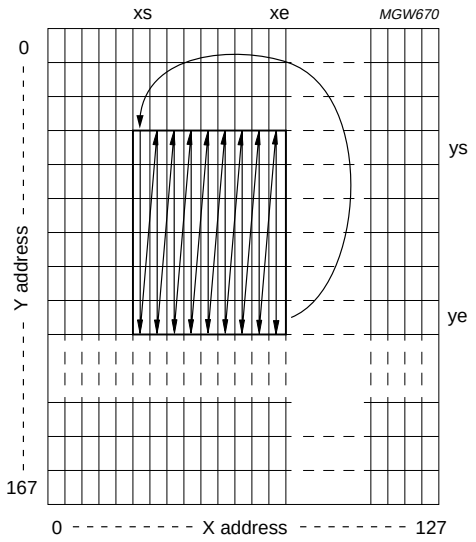


Fig.11 RAM format and addressing.

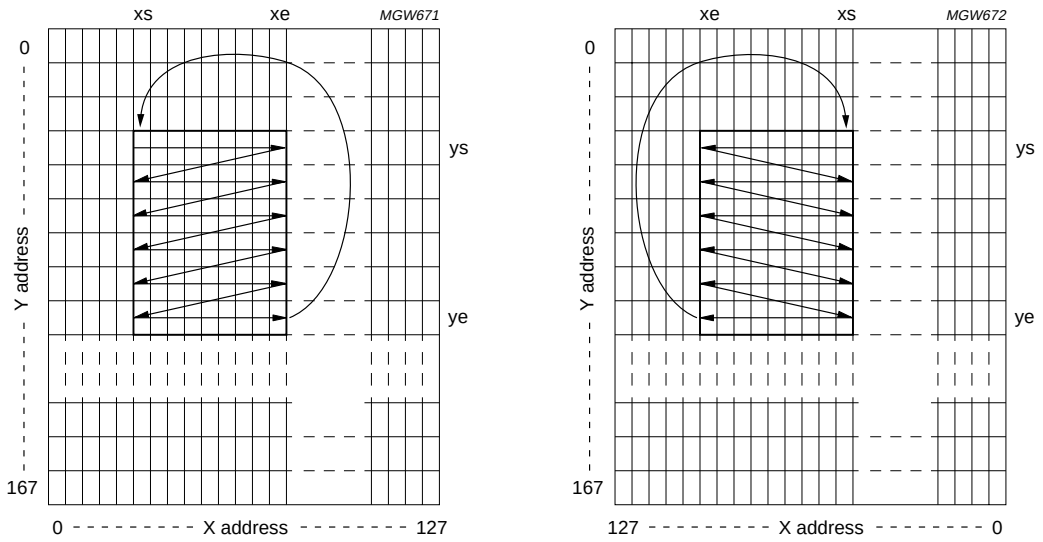


a. V = 0, MX = 0, MY = 0 and L = 0.



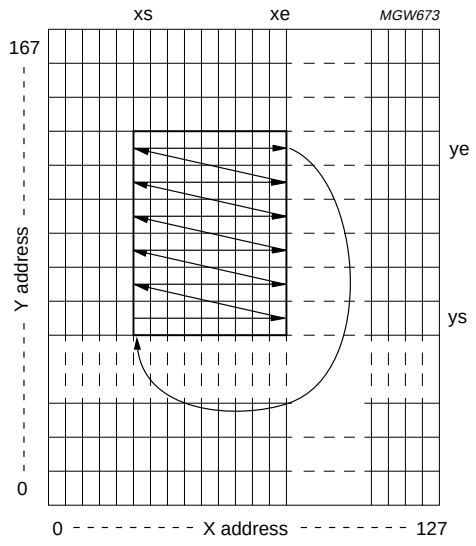
b. V = 1, MX = 0, MY = 0 and L = 0.

Fig.12 Sequence of writing data bytes into RAM as a function of vertical control bit V.

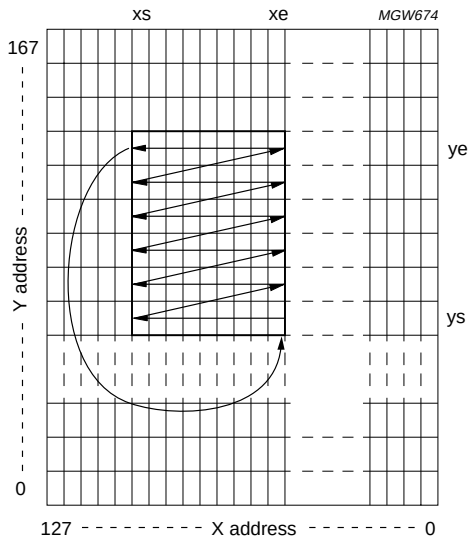


a. V = 0, MX = 0, MY = 0 and L = 0.

b. V = 0, MX = 1, MY = 0 and L = 0.

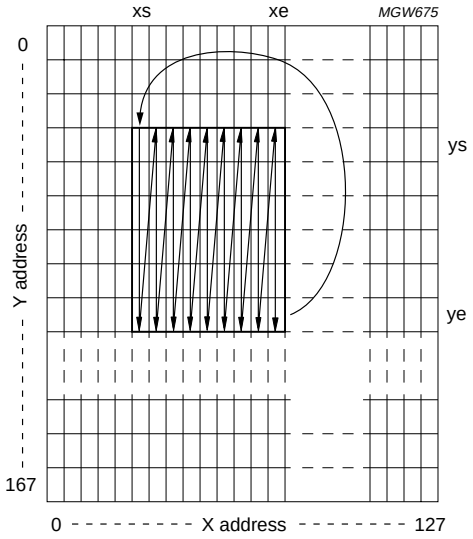


c. V = 0, MX = 0, MY = 1 and L = 0.

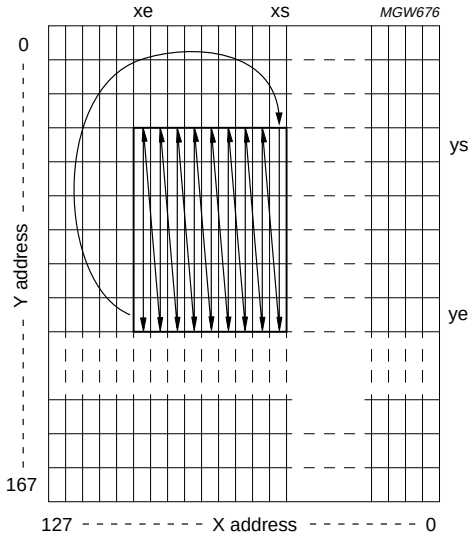


d. V = 0, MX = 1, MY = 1 and L = 0.

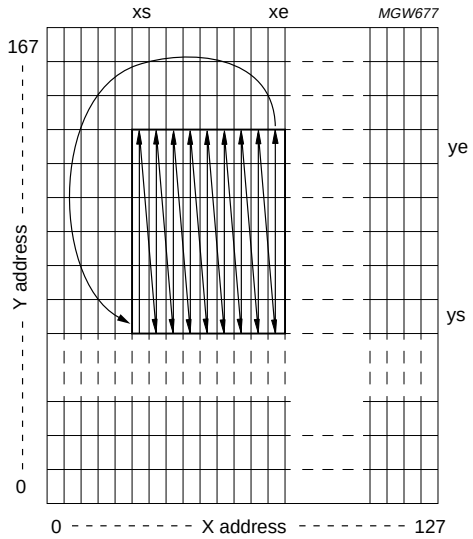
Fig.13 Sequence of writing data bytes into RAM with horizontal addressing (V = 0) as a function of mirror control bits MX and MY.



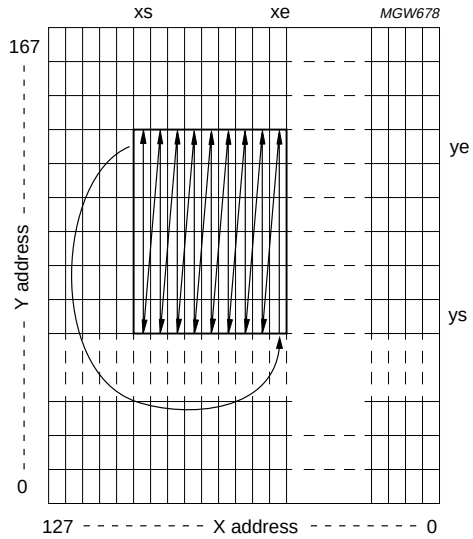
a. V = 1, MX = 0, MY = 0 and L = 0.



b. V = 1, MX = 1, MY = 0 and L = 0.

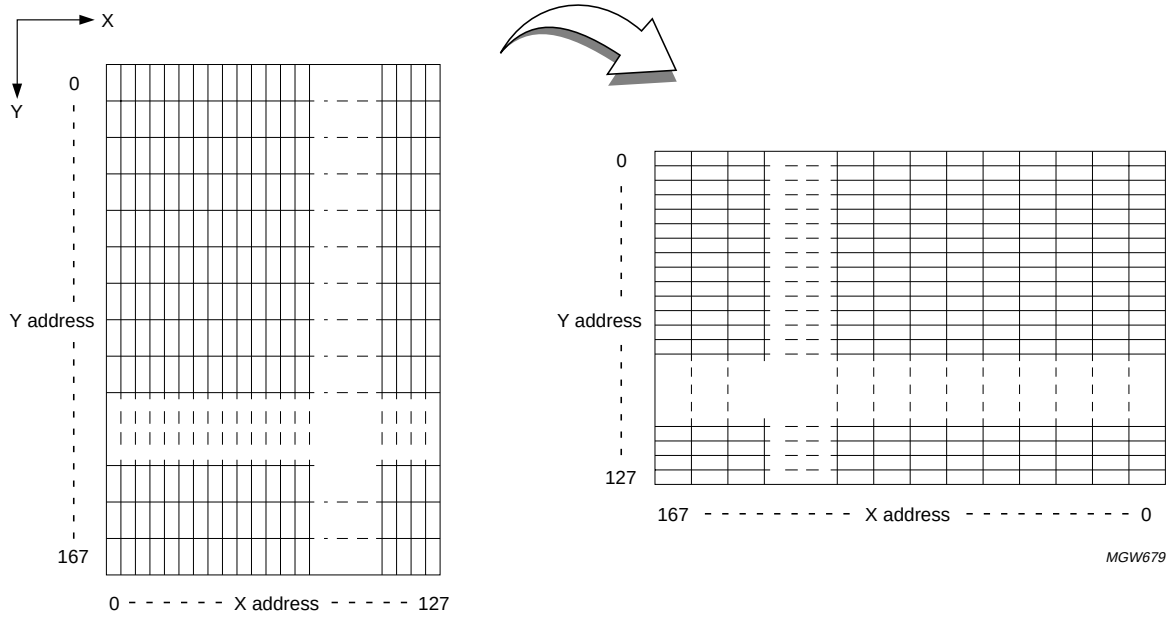


c. V = 1, MX = 0, MY = 1 and L = 0.



d. V = 1, MX = 1, MY = 1 and L = 0.

Fig.14 Sequence of writing data bytes into RAM with vertical addressing (V = 1) as a function of mirror control bits MX and MY.



a. Portrait (L = 0). b. Landscape (L = 1).

Fig.15 Principle of landscape/portrait switching using landscape control bit L.

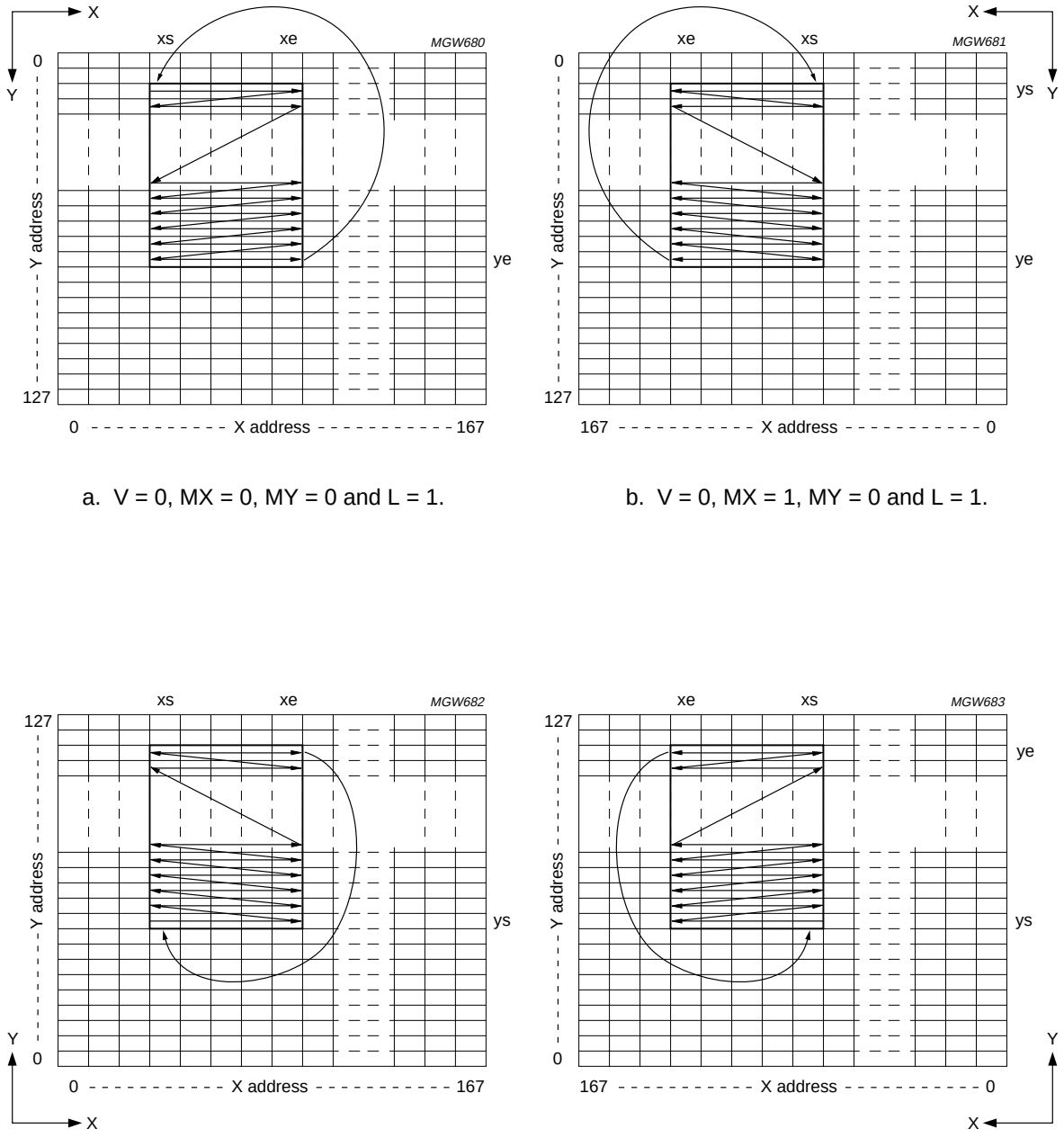


Fig.16 Sequence of writing data bytes into RAM with horizontal addressing and in landscape mode as a function of mirror control bits MX and MY.

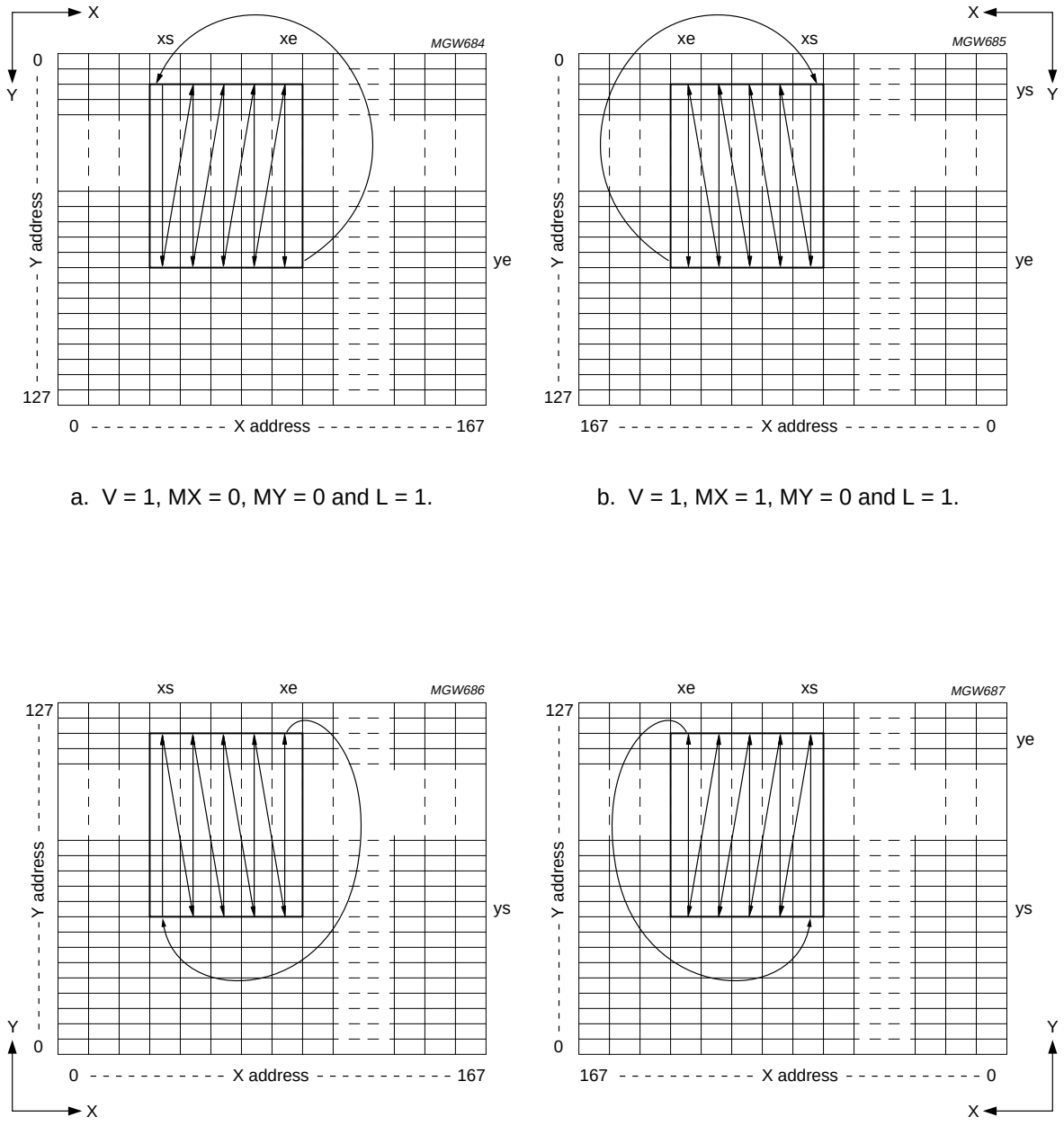


Fig.17 Sequence of writing data bytes into RAM with vertical addressing and in landscape mode as a function of mirror control bits MX and MY.

8 INSTRUCTIONS

The PCF8832 communicates with the host via two 8-bit parallel interfaces, a 3-line or a 4-line serial peripheral interface or an I^2C-bus interface. Processing of the instructions does not require the display clock.

The PCF8832 has two access types, those defining the operating mode of the device (instructions) and those filling the display RAM. The latter are the most frequently used. Efficient data transfer is achieved by auto-incrementing RAM address pointers.

There are three types of instructions:

- Defining display configuration
- Miscellaneous instructions
- Setting X and Y-addresses.

The initial sequence to be sent to the IC is given in Table 5.

Table 5 Initial instruction sequence

CONTROL BYTE (HEX)	REGISTER VALUE (HEX)
85	06
A2	00

Table 6 Command register

Only command register addresses shown are allowed; after reset the registers go to their default value; δ is equivalent to don't care; see Table 7 for explanation of control bits used

ADR (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT (HEX)	DESCRIPTION
00	0	0	0	0	0	0	0	0	00	NOP (no operation)
01	0	0	0	0	0	δ	RSTA	PD	01	Power-down
02	0	0	0	0		MY	MX	0	00	RAM data addressing
03	0	0	0	0	0	δ	L	V	00	data control
04	0	δ	δ	0	SPS	PM	DIM	DON	00	display settings
05	0	0	0	0	0	0	ER	EC	02	oscillator-related bits
06	xs[7]	xs[6]	xs[5]	xs[4]	xs[3]	xs[2]	xs[1]	xs[0]	00	X-ADR start; 0 ≤ xs ≤ FF
07	xe[7]	xe[6]	xe[5]	xe[4]	xe[3]	xe[2]	xe[1]	xe[0]	7F	X-ADR end; xs ≤ xe ≤ FF
08	ys[7]	ys[6]	ys[5]	ys[4]	ys[3]	ys[2]	ys[1]	ys[0]	00	Y-ADR start; 0 ≤ ys ≤ A8
09	ye[7]	ye[6]	ye[5]	ye[4]	ye[3]	ye[2]	ye[1]	ye[0]	A7	Y-ADR end; ys ≤ ye ≤ A8
0A	δ	δ	δ	δ	δ	VMOE	VCOE	OFQ	07	IO configuration; oscillator frequency
0B	NLI7	NLI6	NLI5	NLI4	NLI3	NLI2	NLI1	NLI0	00	n-line inversion
0C	0	0	b002	b001	b000	b012	b011	b010	01	mapping blue scale b00; b01
0D	0	0	b102	b101	b100	b112	b111	b110	27	mapping blue scale b10; b11
0E	0	0	0	0	δ	0	0	CF0	00	colour filter (RGB array)
0F	AA1S7	AA1S6	AA1S5	AA1S4	AA1S3	AA1S2	AA1S1	AA1S0	00	active area 1 start ADR
10	AA1E7	AA1E6	AA1E5	AA1E4	AA1E3	AA1E2	AA1E1	AA1E0	4F	active area 1 end ADR
11	AA2S7	AA2S6	AA2S5	AA2S4	AA2S3	AA2S2	AA2S1	AA2S0	50	active area 2 start ADR
12	AA2E7	AA2E6	AA2E5	AA2E4	AA2E3	AA2E2	AA2E1	AA2E0	9F	active area 2 end ADR
13	DSA17	DSA16	DSA15	DSA14	DSA13	DSA12	DSA11	DSA10	00	scroll area start ADR; DSA1 ≤ DSA2
14	DSA27	DSA26	DSA25	DSA24	DSA23	DSA22	DSA21	DSA20	00	scroll area end ADR
15	SEP7	SEP6	SEP5	SEP4	SEP3	SEP2	SEP1	SEP0	00	scroll entry point
16	0	0	δ	FFQ4	FFQ3	FFQ2	FFQ1	FFQ0	05	set frame frequency

ADR (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT (HEX)	DESCRIPTION
17	0	0	0	0	FI	IR	0	FRCM	0D	frame inversion; FRC
18	VPR7	VPR6	VPR5	VPR4	VPR3	VPR2	VPR1	VPR0	A2	program V_{HREG}
19	0	0	0	0	VPC3	VPC2	VPC1	VPC0	05	program V_{COL}
1A	0	0	SLB2	SLB1	SLB0	SLA2	SLA1	SLA0	07	temperature compensation slopes
1B	0	0	SLD2	SLD1	SLD0	SLC2	SLC1	SLC0	10	temperature compensation slopes
1C	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	D1	VOP_{VH} limit value
1D	0	0	0	DBL	SEC	R1F	SW2	SW1	04	row driver control
1E	0	0	0	0	0	ID2	ID1	ID0	00	chip identity
1F	0	TD6	TD5	TD4	TD3	TD2	TD1	TD0	20	temperature read data
3F	0	0	1	1	1	1	1	1	–	software reset

Table 7 Explanation of control bits used in Table 6

BIT	0	1
PD	active mode	Power-down mode
RSTA	no register read	read value from select address
MX	no mirror X	mirror X
MY	no mirror Y	mirror Y
L	portrait mode	landscape mode
V	RAM write in X direction	vertical RAM write, in Y direction
DON	display off	display on
DIM	normal display	display inverse video mode
PM	no partial display mode	partial display mode active
SPS	scroll inactive	start programmed scroll active
EC	internal oscillator	external clock applied
ER	external resistor used	internal resistor used
OFQ	f_{LCK} = 300 kHz	oscillator frequency at LCK output f_{LCK} = 600 kHz
VMOE	V_M is input	V_M is enabled as output
VCOE	V_{COL} is input	V_{COL} is enabled as output
IR	asynchronous n-line inversion	n-line inversion related to frame
FI	no frame inversion	frame inversion active
FRCM	frame rate control, 7-frame method	frame rate control, 9-frame method
Row driver control		
DBL	single line mode	double line mode
SEC	first half of RAM is displayed (DBL = 1)	second half of RAM is displayed (DBL = 1)
R1F	shift register 2 first in chain	shift register 1 first in chain
SW1	normal row shift direction REG1[0 to 79]	swapped shift direction REG1[79 to 0]
SW2	normal row shift direction REG2[80 to 159]	swapped shift direction REG2[159 to 80]

Table 8 N-line inversion (NLI[7:0] < 160)

NLI[7:0]	DESCRIPTION
00000000	no n-line inversion (frame inversion)
00000001	inversion after each row
00000010	inversion after 2 rows
to	to
01100100	inversion after 100 rows
to	to
10011111	inversion after 159 rows

Decoding of the blue bits is shown in Table 9. The data byte for one pixel contains 8 bits (RRRGGGBB). The red and green bits will be written directly to the RAM. For the blue bits, the data to be written for B[1:0] values are defined in the command register (address 0CH and 0DH). The procedure for writing the blue bits is:

1. Program the blue scale register (ADR: 0CH and 0DH) e.g. set register 0CH to 01H.
2. Send pixel information via interface; the pixel value via interface is ADH, (RRR = 101), (GGG = 011) and (B[1:0] = 01).
3. Write procedure of pixel information to display RAM:
   a) RRR and GGG is written directly to the RAM
   b) The two blue bits decide which register bits are to be used, in this example b012, b011 and b010 will be written as blue pixel information to the display RAM.

Table 9 Translation of blue bits

b[1:0]	REGISTER BITS 0CH and 0DH
00	b002 b001 b000
01	b012 b011 b010
10	b102 b101 b100
11	b112 b111 b110

Table 10 Column output voltage (ΔV_{COL} = 100 mV)

VPC[3:0]	V_{COL} (V)
0000	2.5
to	to
1111	4.0

Table 11 Set frame frequency

FFQ[4:0]	FRAME FREQUENCY (Hz)
00000	20
00001	40
00010	60
00011	80
00100	100
00101	120
00110	140
00111	160
01000	180
01001	200
01010	220
01011	240
01100	260
01101	280
01110	300
01111	320
10000	340
10001	360
10010	380
10011	400
10100	–
10101	–
10110	–
10111	–
11000	–
11001	–
11010	–
11011	–
11100	–
11101	–
11110	–
11111	–

Table 12 Colour filter

CF0	C0	C1	C2	C3	C4	C5	C6	C7	to	C383
0	R	G	B	R	G	B	R	G		B
1	B	G	R	B	G	R	B	G		R

8.1 Function sets

8.1.1 NOP

The 'no operation' functionality is provided by the NOP register. According to the interface protocol, first the address 00H and then the register value 00H must be sent.

8.1.2 RESET

The chip has a hardware and a software reset. After power-up, a hardware reset input ($\overline{RES}$) must be applied. The hardware and software resets give the same results. After a reset the chip has the following state:

- All column outputs set to V_{SS} (display off)
- RAM data undefined
- Power-down mode
- Command register set to default states (see Table 6).

8.1.3 SOFTWARE RESET

The software reset is applied following interface protocol:

1. Send a control byte with the software register address (3FH).
2. Send the register value (3FH).

8.1.4 POWER-DOWN

During Power-down (PD), all static currents are switched off (no internal oscillator, no timing and no LCD segment drive system) and all LCD column outputs are connected internally to V_{SS}. The I/O buffer and interface remain operational.

When PD = 1, the PCF8832 is in the Power-down mode:

- All column outputs are set to V_{SS} (display off)
- Interface is operational; commands can be executed
- RAM contents are not cleared; RAM data can be written
- Register settings remain unchanged.

8.1.5 VERTICAL OR HORIZONTAL ADDRESSING

When V = 0, horizontal addressing is selected and the data is written into the DDRAM as shown in Fig.13. When V = 1, vertical addressing is selected and the data is written into the DDRAM as shown in Fig.14.

8.1.6 DISPLAY ON/OFF

Table 13 Display mode bits DIM and DON

DIM	DON	MODE	V_{pixel}
0	0	all pixels off	$V_{off(rms)}$
0	1	normal mode	pixel value: (000) = $V_{off(rms)}$; (111) = $V_{on(rms)}$
1	0	all pixels on	$V_{on(rms)}$
1	1	inverse video mode	pixel value: (111) = $V_{off(rms)}$; (000) = $V_{on(rms)}$

8.1.7 PARTIAL MODE

The following steps must be performed to enter partial mode (PM), refer to Fig.18:

1. Set start address of active area 1 AA1S[7:0].
2. Set end address of active area 1 AA1E[7:0].
3. Set start address of active area 2 AA2S[7:0].
4. Set end address of active area 2 AA2E[7:0].
5. Enter partial mode PM = 1.

When setting the addresses the following condition must be ensured:

$0 \leq AA1S < AA1E < AA2S < AA2E \leq 9FH$

In partial mode, the MUX rate of the driver is set automatically to the minimum required thus reducing power consumption. The appropriate operating voltages V_H and V_{COL} must be programmed. Scroll mode cannot be used in partial mode.

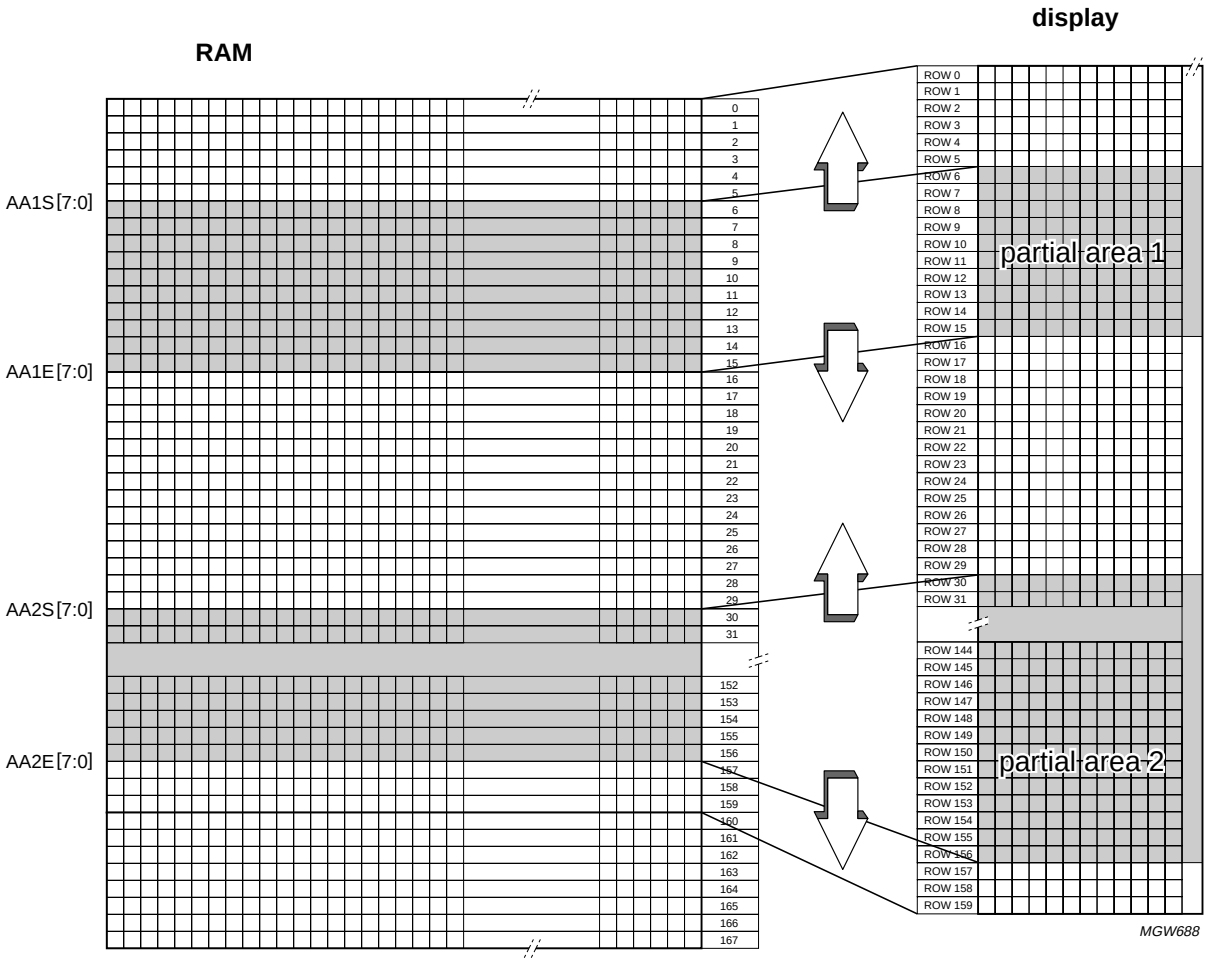


Fig.18 Partial mode.

8.1.8 SCROLL MODE

The following steps must be performed to enter scroll mode, refer to Fig.19:

1. Define the scroll area:
   a) Set start address DSA1[7:0]
   b) Set end address DSA2[7:0].
2. Set Scroll Entry Point SEP[7:0].
3. Enter scroll mode by setting Start Programmed Scroll SPS = 1.
4. After the desired time interval, increment the scroll address to SEP + n for an n-line step.
5. Keep incrementing the scroll address at regular intervals.
6. Stop scroll mode SPS = 0.

If DSA1 = n with 0 < n < 159 and DSA2 = 159, then only one fixed area at the top of the display is used. In this configuration the hidden part of the RAM Y-addresses 160 to 167 can be used in scroll mode.

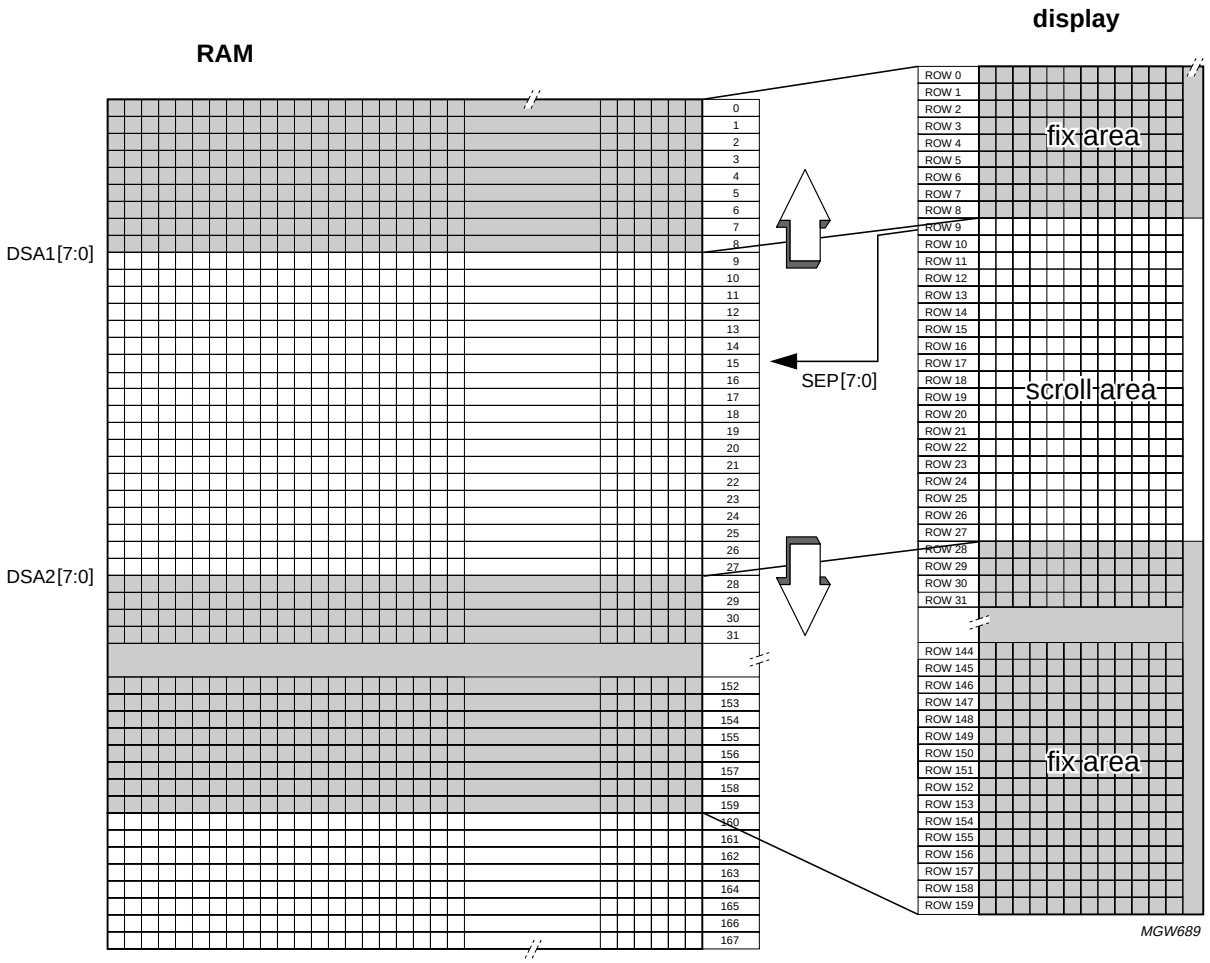


Fig.19 Scroll mode.

8.1.9 DOUBLE LINE MODE

If DBL = 1, then two rows will be selected at the same time. In this case, only the half of the RAM content can be displayed. The SEC bit selects the part of the RAM to be displayed (see Fig.20).

Double line mode can be used in combination with the scroll mode. If SEC = 0, the first part of the RAM Y-address 0 to 79 will appear on the display in double line mode. During scroll mode, the hidden part of the RAM Y-address 80 to 167 can be scrolled-up. If SEC = 1, the second part of the RAM will be displayed.

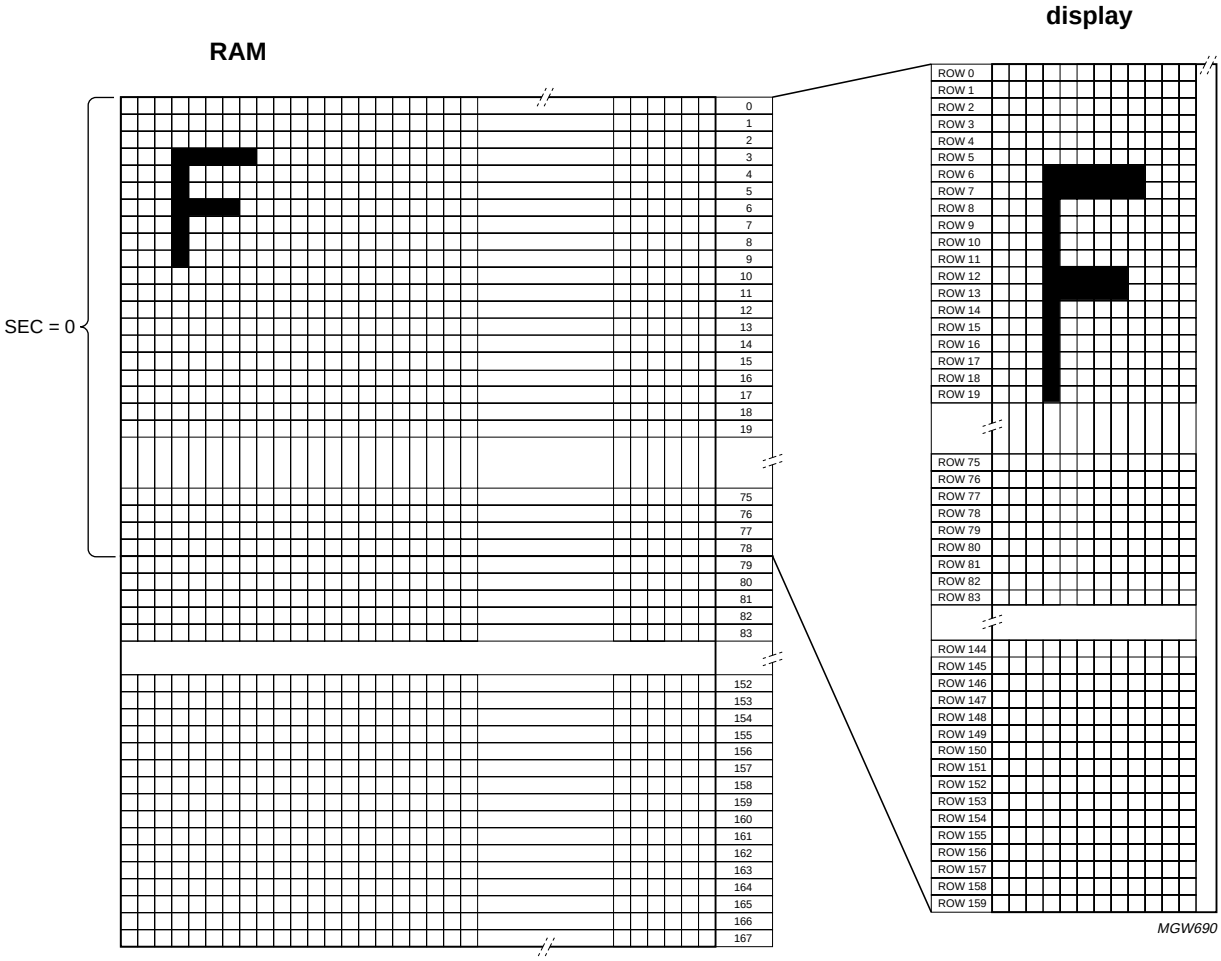


Fig.20 Double line mode.

8.2 Set Y-address

Bits ys[7:0] and ye[7:0] define the Y-address range of the display RAM for writing data. Values of ys and ye are between 0 and 167 (A7H); ys must be smaller then ye.

Table 14 Y-address range

y7	y6	y5	y_4	y3	y2	y1	y0	BANK
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
to								
1	0	1	0	0	1	1	0	166
1	0	1	0	0	1	1	1	167

8.3 Set X-address

Bits xs and xe define the X-address range of the display RAM for writing data. Values of xs, xe are between 0 and 127 (7FH); xs must be smaller then xe.

8.4 Programming V_{COL}

V_{COL} can be programmed in the range $V_{COL(min)}$ = 2.5 V to $V_{COL(max)}$ = 4.0 V. The following equation shows the calculation of V_{COL}

$$V_{COL} = V_{COL(min)} + VPC \times \Delta V_{COL}$$

Where

VPC is a 4-bit value that can be set via the command register (see Table 10)

ΔV_{COL} = 100 mV.

Regardless of the equation, the value of V_{COL} is limited to the range 2.5 to 4.0 V.

8.5 Calculation of V_H

The following equation shows how to calculate V_H. R1 and R2 are external resistors (see Fig.62).

$$V_H = V_{H(reg)} \times K_{RES} \text{ where } K_{RES} = \frac{R1 + R2}{R2}$$

8.6 Programming of $V_{H(reg)}$

The voltage $V_{H(reg)}$ regulates the external row voltage level V_H with the control of the external inductive DC-to-DC converter. If the external voltage $V_{FBQ} < V_{H(reg)}$, the switching clock LCK will start to boost the row voltage level. If $V_{FBQ} \geq V_{H(reg)}$, the clock LCK stops to maintain the row voltage level. The following equation shows the calculation of $V_{H(reg)}$

$$V_{H(reg)} = V_{H(reg)(min)} + \Delta V_{H(reg)} \times f_{min}(VPR + TP) \times VL$$

Where

V_T is the signed value dependent on temperature sensor output and programmed slope

VPR is an 8-bit value, set via the command register

$\Delta V_{H(reg)}$ = 7 mV (step size of $V_{H(reg)}$)

$V_{H(reg)(min)}$ = 200 mV

VL is an 8-bit value, set via the command register

TP is a 5-bit signed value provided via the $V_{H(reg)}$ trimming inputs TP4, TP3, TP2, TP1 and TP0

f_{min} is a minimum function, with VL it is possible to limit the generated voltage (the low voltage limit is zero).

If VL < (VPR + TP), $V_{H(reg)}$ will be limited to the following level

$$V_{H(reg)} = V_{H(reg)(min)} + \Delta V_{H(reg)} \times VL$$

Table 15 $V_{H(reg)}$ trimming

$V_{H(reg)}$ TRIMMING INPUTS					VALUE
TP4	TP3	TP2	TP1	TP0	
1	0	0	0	0	–16
1	0	0	0	1	–15
to					
1	1	1	1	1	–1
0	0	0	0	0	0
0	0	0	0	1	+1
to					
0	1	1	1	0	+14
0	1	1	1	1	+15

9 INTERFACES

9.1 Interface definitions

Table 16 Selection of interface type

PS2	PS1	PS0	INTERFACE	READ-BACK SELECT	REMARKS
0	0	0	3-line SPI	via command bit RSTAT	
0	0	1	4-line SPI	via command bit RSTAT	
0	1	0	I^2C-bus	via R/$\overline{W}$ in slave address	
0	1	1	serial (3-line)	via command bit RSTAT	
1	0	0	8080 MPU basic	$\overline{WR}$ write strobe	basic protocol only
1	1	0	8080 MPU	$\overline{WR}$ write strobe	
1	0	1	6800 MPU basic	R/$\overline{W}$ = 1	CS used as clock; basic protocol only
1	1	1	6800 MPU	R/$\overline{W}$ = 1	

Table 17 Control byte definition

INTERFACE	D7	D6	D5	D4	D3	D2	D1	D0	COMMENT
I^2C-bus	CO	D/$\overline{C}$	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	
Parallel (8080)	CO	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	external signal A0 used
Parallel (6800)	CO	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	external signal A0 used
SPI (3-line)	CO	D/$\overline{C}$	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	
SPI (4-line)	CO	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	external signal A0 used
Serial (3-line)	CO	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	first bit for DC

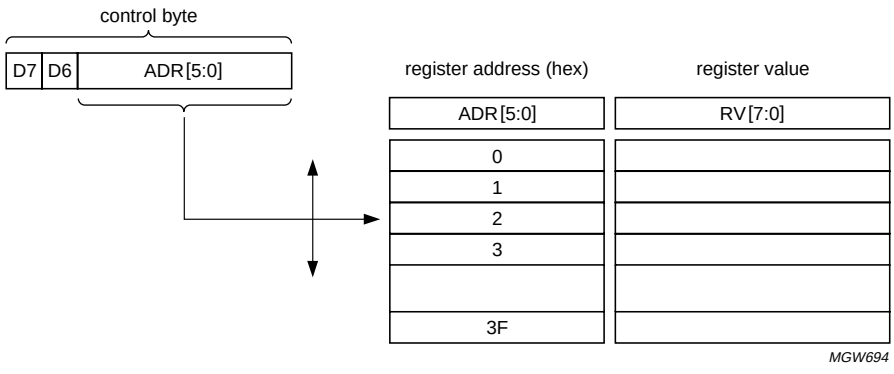


Fig.21 Command register addressing.

Table 18 Bits CO and D/$\overline{C}$

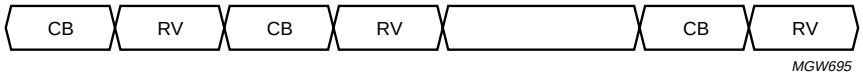
RSTA(1)	CO	D/$\overline{C}$	DESCRIPTION
0	0	0	write stream of commands, starting at register ADR[5:0]
	0	1	write stream of data to RAM, ADR[5:0] don't care
	1	0	write single command to register ADR[5:0]
	1	1	write single RAM data, ADR[5:0] don't care
1(2)	0	0	read all registers, starting at register ADR[5:0]
	0	1	not used
	1	0	read single register at ADR[5:0]
	1	1	not used

Notes

1. RSTA specifies the read or write mode of register RSTA: 0 = write mode; 1 = read mode. RSTA is used only with the serial and I^2C-bus interfaces.
2. Read mode protocol for serial interfaces.

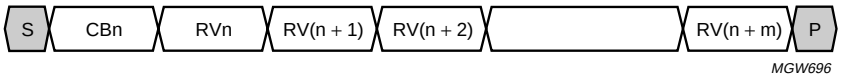
9.2 General protocol

The generally-supported protocols for programming the LCD driver are shown in Figs 22 and 23.



CB = control byte.
RV = register value.

Fig.22 Basic protocol (D/$\overline{C}$ = 0).



S = start data transmission.
CBn = control byte that points to address n.
RVn = register value for register of address n.
RV(n + 1) = register value for register of address n + 1.
P = stop data transmission.

Fig.23 Advanced protocol (D/$\overline{C}$ = 0).

10 PARALLEL INTERFACES

The parallel interfaces that can be selected are the 6800-type and 8080-type 8-bit bidirectional interface for communication between the microcontroller and the LCD driver chip. The selection of an interface is done with inputs PS2, PS1 and PS0, see Table 16.

10.1 6800-type parallel interface

The interface functions of the 6800-type parallel interface are shown in Table 19. Figures 24 to 29 show the data transfer in different modes. The transmission byte (TB) shown in these figures is a register value or a control byte, depending on the mode and protocol used.

Table 19 6800-type parallel interface function

D/$\overline{C}$	R/$\overline{WR}$	OPERATION
0	0	command data write
0	1	read status register
1	0	display data write
1	1	none

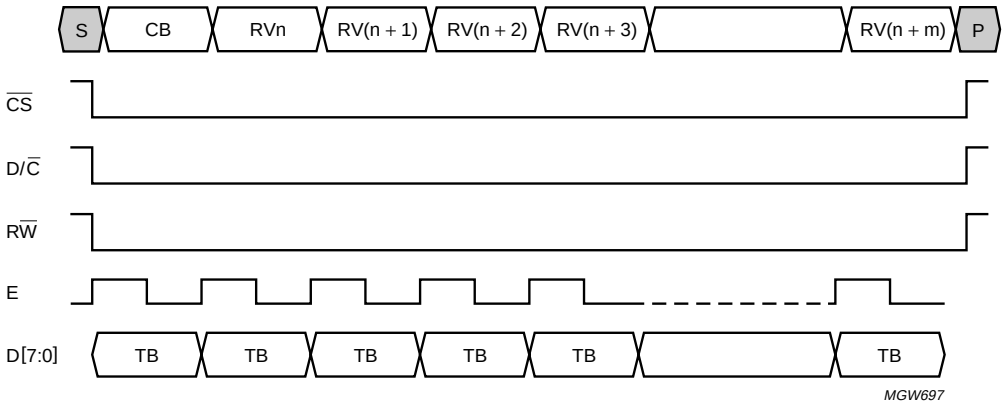


Fig.24 Parallel bus protocol, advanced write to register (PS[2:0] = 111).

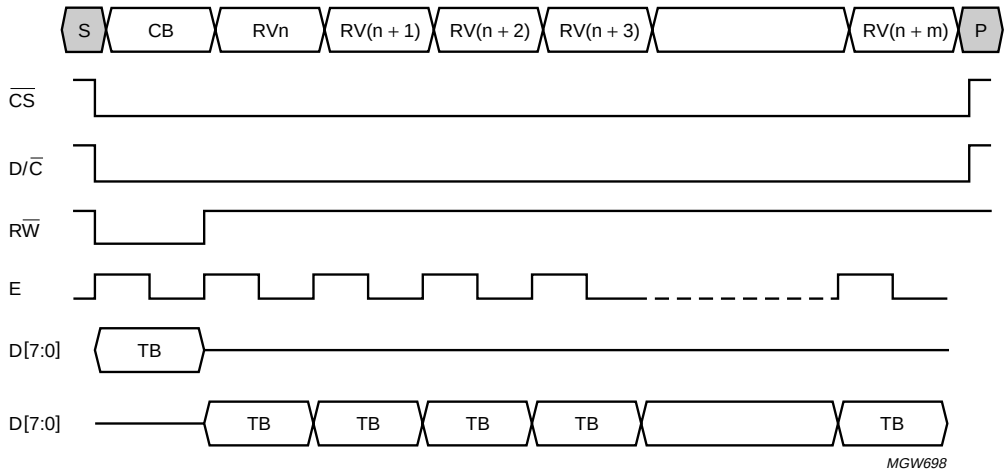


Fig.25 Parallel bus protocol, advanced read from register (PS[2:0] = 111).

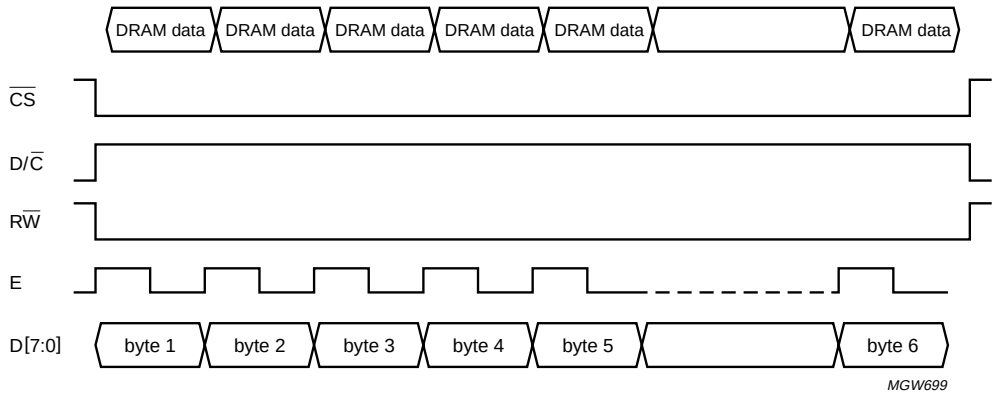


Fig.26 Parallel bus protocol, write to RAM.

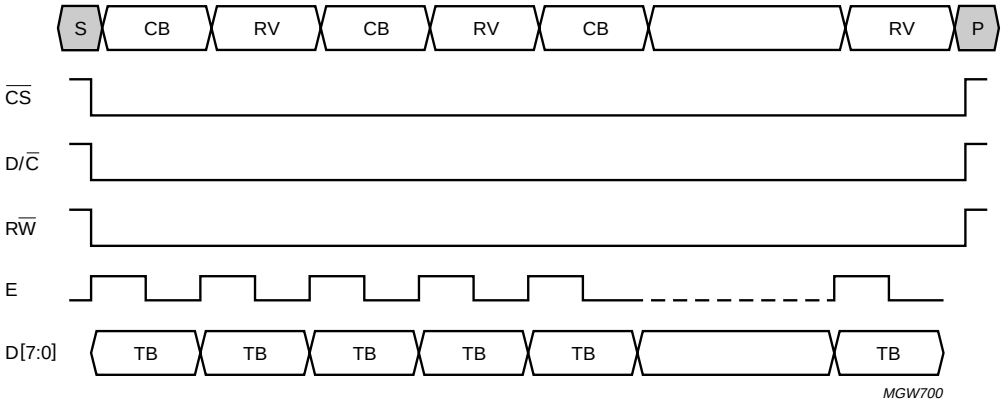


Fig.27 Parallel bus protocol, basic write to register (PS[2:0] = 111).

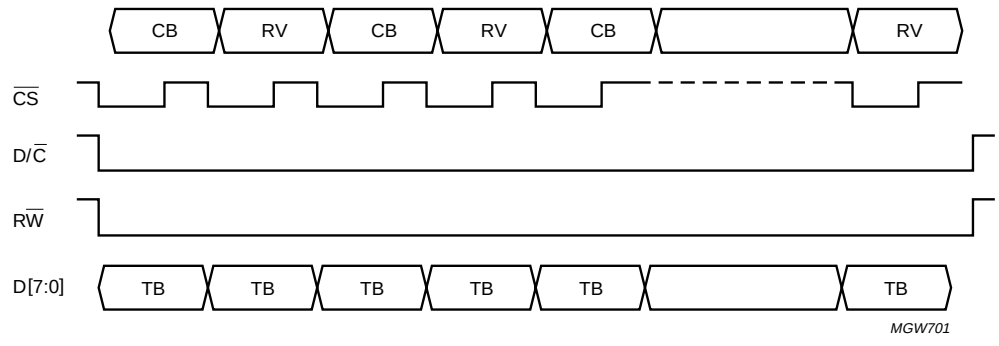


Fig.28 Parallel bus protocol, basic write to register (PS[2:0] = 101).

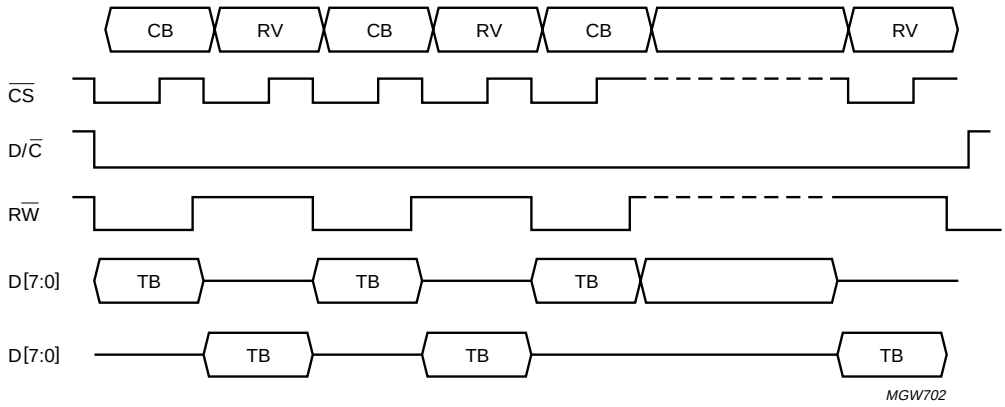


Fig.29 Parallel bus protocol, basic read from register (PS[2:0] = 101).

10.2 8080-type parallel interface

The interface functions of the 8080-type parallel interface are given in Table 20. Figures 30 to 34 show the data transfer in different modes. The transmission byte (TB) shown in these figures is a register value or a control byte, depending on mode and protocol used.

Table 20 8080-type parallel interface function

A0 (D/$\overline{C}$)	$\overline{RD}$(1)	$\overline{WR}$(1)	OPERATION
0	1	↑	command data write
1	1	↑	display data write
0	↑	1	read status register
1	↑	1	none
1	↑	↑	not allowed

Note

1. ↑ indicates a rising edge.

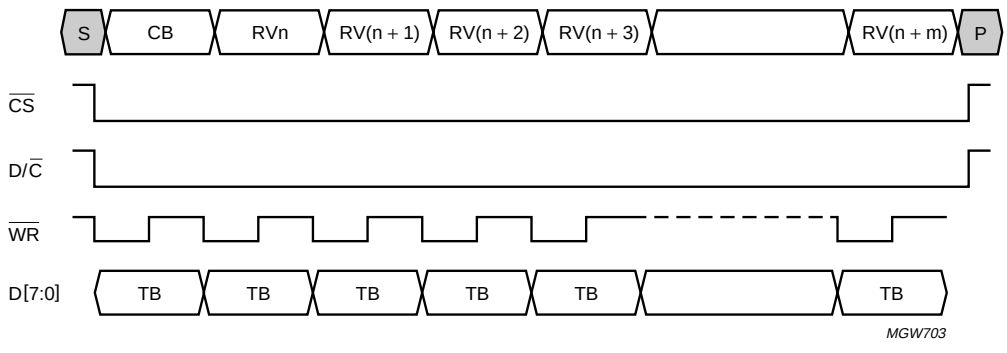


Fig.30 Parallel bus protocol, advanced write to register (PS[2:0] = 110).

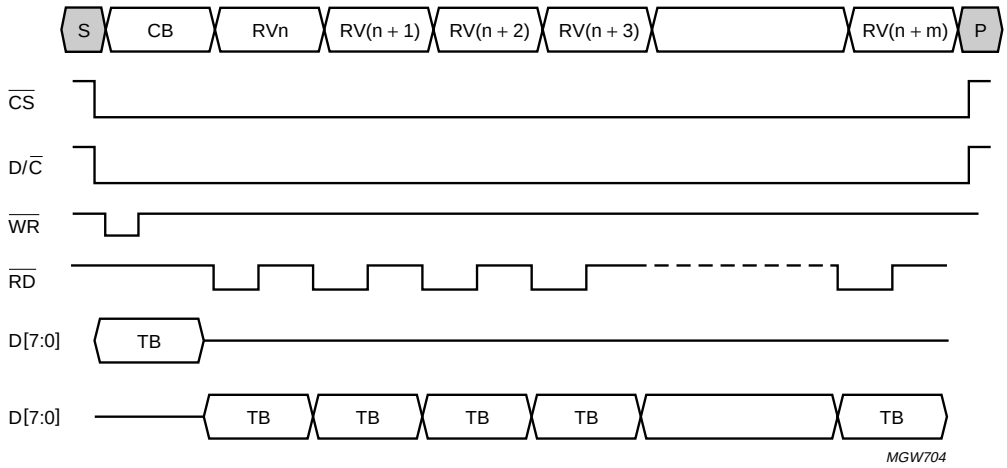


Fig.31 Parallel bus protocol, advanced read from register (PS[2:0] = 110).

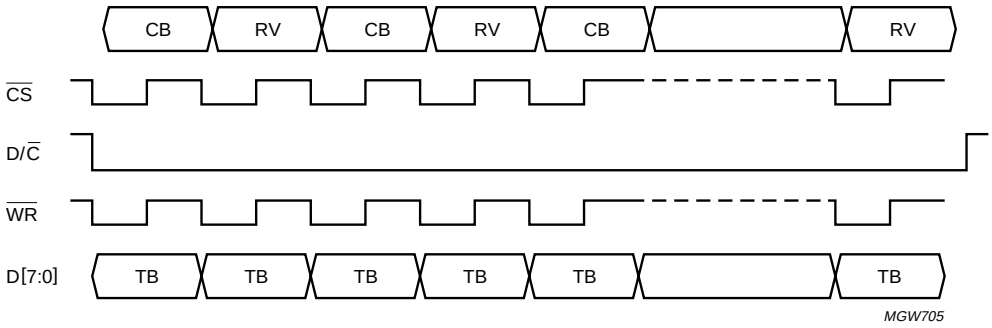


Fig.32 Parallel bus protocol, basic write to register (PS[2:0] = 100).

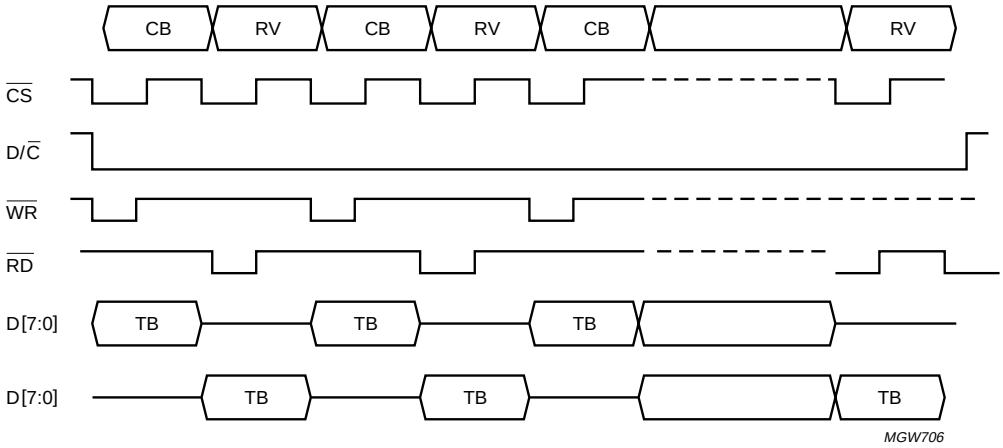


Fig.33 Parallel bus protocol, basic read from register (PS[2:0] = 100).

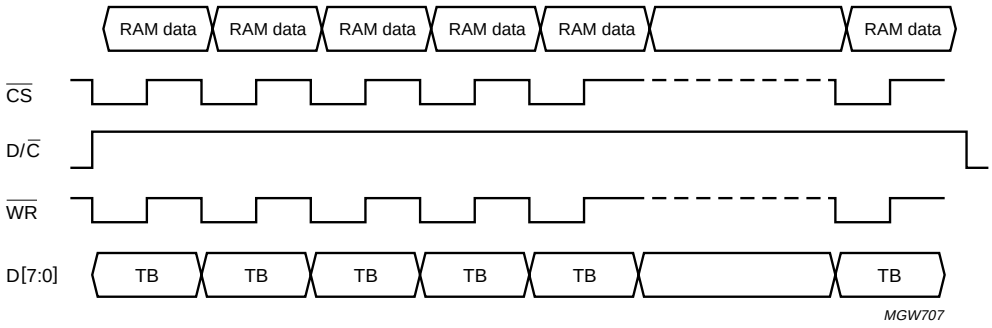


Fig.34 Parallel bus protocol, write to display RAM (PS[2:0] = 100).

11 SERIAL INTERFACES

Communication with the microcontroller can also occur via a clock-synchronized serial peripheral interface. It is possible to select two different 3-line interfaces (SPI **and** serial interface) or a 4-line SPI.

11.1 Serial peripheral interface

The SPI is a 3-line or 4-line interface for communication between the microcontroller and the LCD driver chip. The three lines are: $\overline{SCE}$ (chip enable), SCLK (serial clock) and SDI (serial data). For the 4-line serial interface a separate D/$\overline{C}$ line is included.

The PCF8832 is connected to the serial data I/O of the microcontroller by two pins: SDI (data input) and SDO (data output) which must be connected together.

11.1.1 WRITE MODE

The display data/command indication may be controlled either via software (3-line SPI) or the D/$\overline{C}$ select pin (4-line SPI). When the D/$\overline{C}$ pin is used, display data is transmitted when D/$\overline{C}$ is HIGH and command data is transmitted when D/$\overline{C}$ is LOW (see Figs 35 and 36). When D/$\overline{C}$ is not used, then the D/$\overline{C}$ is set via the control byte.

When the 3-line SPI interface is used, the display data/command is controlled by software (see Figs 37 and 38).

If $\overline{SCE}$ is pulled HIGH during a serial display data stream, the interrupted byte is invalid data but all previously transmitted data are valid.

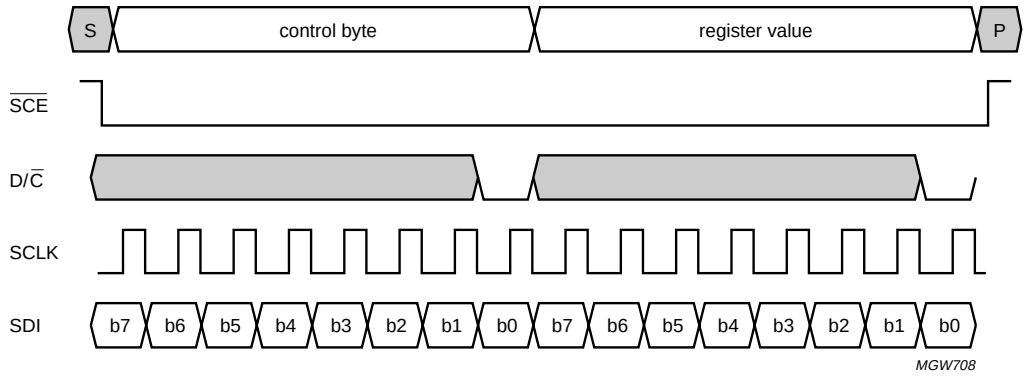


Fig.35 Serial bus protocol, write to register.

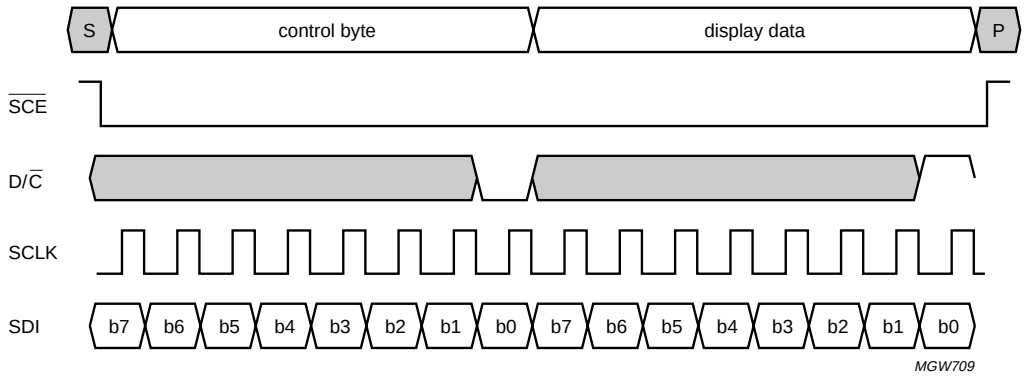


Fig.36 Serial bus protocol, write to RAM.

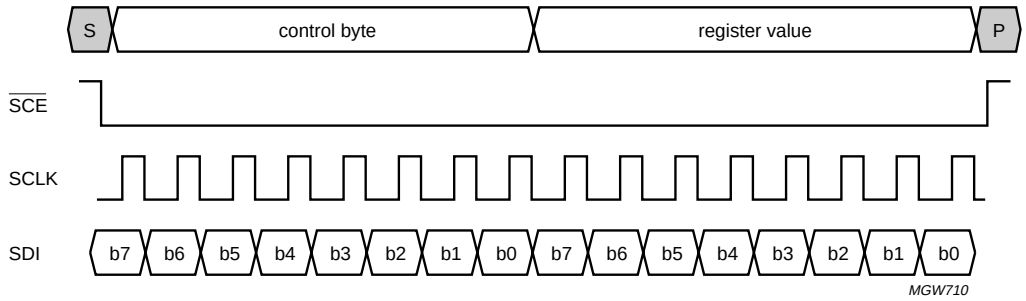


Fig.37 Serial bus protocol, write to register (D/$\overline{C}$ = 0 set into control byte).

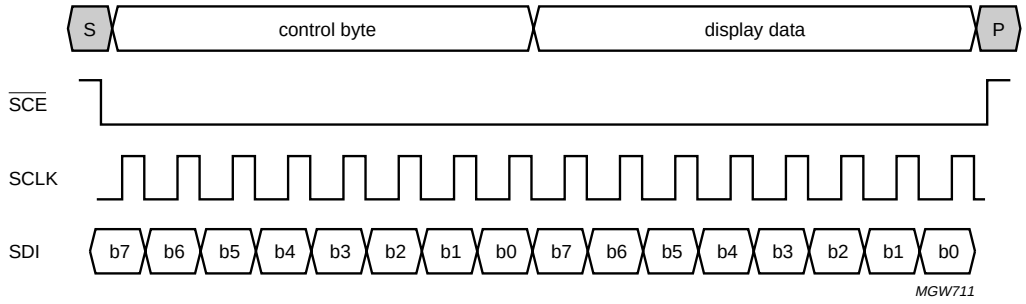


Fig.38 Serial bus protocol, write to RAM (DC = 1 set into control byte).

11.1.2 READ MODE (ONLY COMMAND REGISTER)

The read mode of the interface means that the microcontroller reads data from the PCF8832. To do so, the microcontroller first sends a command sequence, the PCF8832 then responds by transmitting data on the SDO line. After that, $\overline{SCE}$ is required to go HIGH (see Fig.39) and this resets the RSTA bit to write operation.

The PCF8832 samples the SDI data at rising edges, but shifts SDO data at falling SCLK edges. Thus the microcontroller should read SDO data at rising SCLK edges.

After the read command sequence has been sent, the SDI line must be set to 3-state not later than the falling SCLK edge of the last bit (see Fig.39).

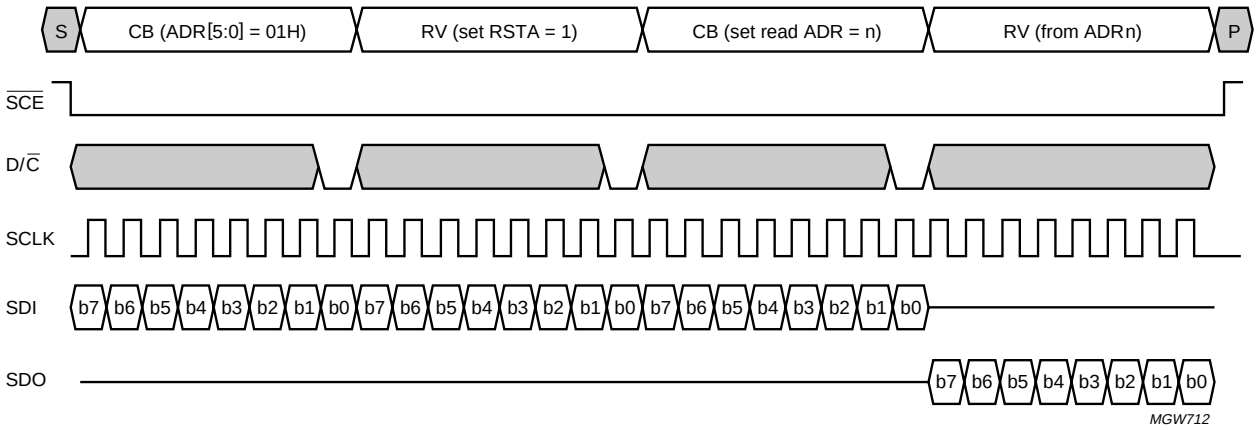


Fig.39 Serial bus protocol, read from register.

11.2 Serial interface (3-line)

The serial interface is also a 3-line bidirectional interface for communication between the microcontroller and the LCD driver chip. The three lines are: $\overline{SCE}$ (chip enable), SCLK (serial clock) and SDI/SDO (serial data).

11.2.1 WRITE MODE

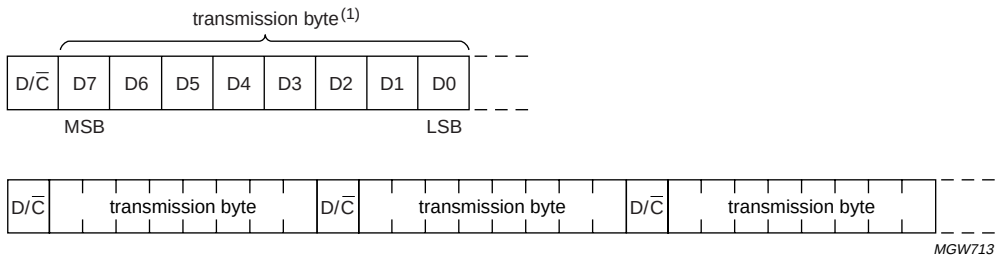
The interface write mode means that the microcontroller writes commands and data to the PCF8832. Each data packet contains a control bit D/$\overline{C}$ and a transmission byte. If D/$\overline{C}$ is LOW, the byte that follows is interpreted as a control byte.

The basic and the advanced protocols are supported. The command set is given in Table 6. If D/$\overline{C}$ is HIGH, the byte that follows is stored in the display data RAM. After every data byte the address counter is incremented automatically.

The serial interface is initialized when $\overline{SCE}$ is HIGH. In this state, SCLK clock pulses have no effect and no power is consumed by the serial interface. A falling edge on $\overline{SCE}$ enables the serial interface and indicates the start of data transmission.

Serial bus protocol (see Fig.41):

- When $\overline{SCE}$ is HIGH, SCLK clocks are ignored. During the HIGH time of $\overline{SCE}$, the serial interface is initialized.
- At the falling edge of $\overline{SCE}$, SCLK must be LOW
- SDI is sampled on the rising edge of SCLK
- D/$\overline{C}$ indicates whether the byte is a command (D/$\overline{C}$ = 0) or RAM data (D/$\overline{C}$ = 1); D/$\overline{C}$ is sampled with the first rising edge of SCLK
- If $\overline{SCE}$ stays LOW after the last bit of a command/data byte, the serial interface expects the D/$\overline{C}$ bit of the next byte at the next rising edge of SCLK
- A reset pulse with $\overline{RES}$ interrupts the transmission (the data being written into the RAM may be corrupted); the registers are cleared, then if $\overline{SCE}$ is LOW after the rising edge of $\overline{RES}$, the serial interface is ready to receive the D/$\overline{C}$ bit of a command/data byte.



(1) Transmission byte may be a command byte or a data byte.

Fig.40 Serial data stream, write mode.

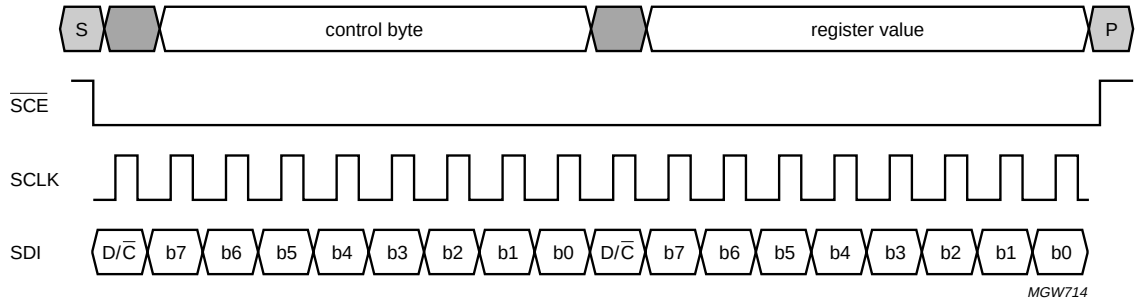


Fig.41 Serial bus protocol, write to register with control bit in transmission.

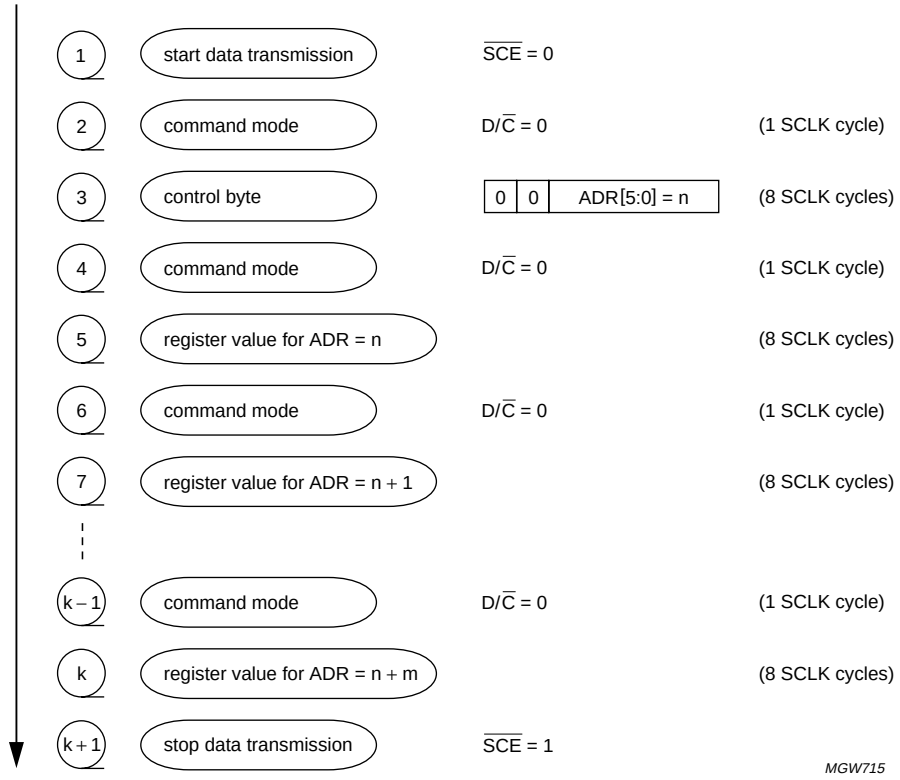


Fig.42 Write sequence to register, advanced protocol.

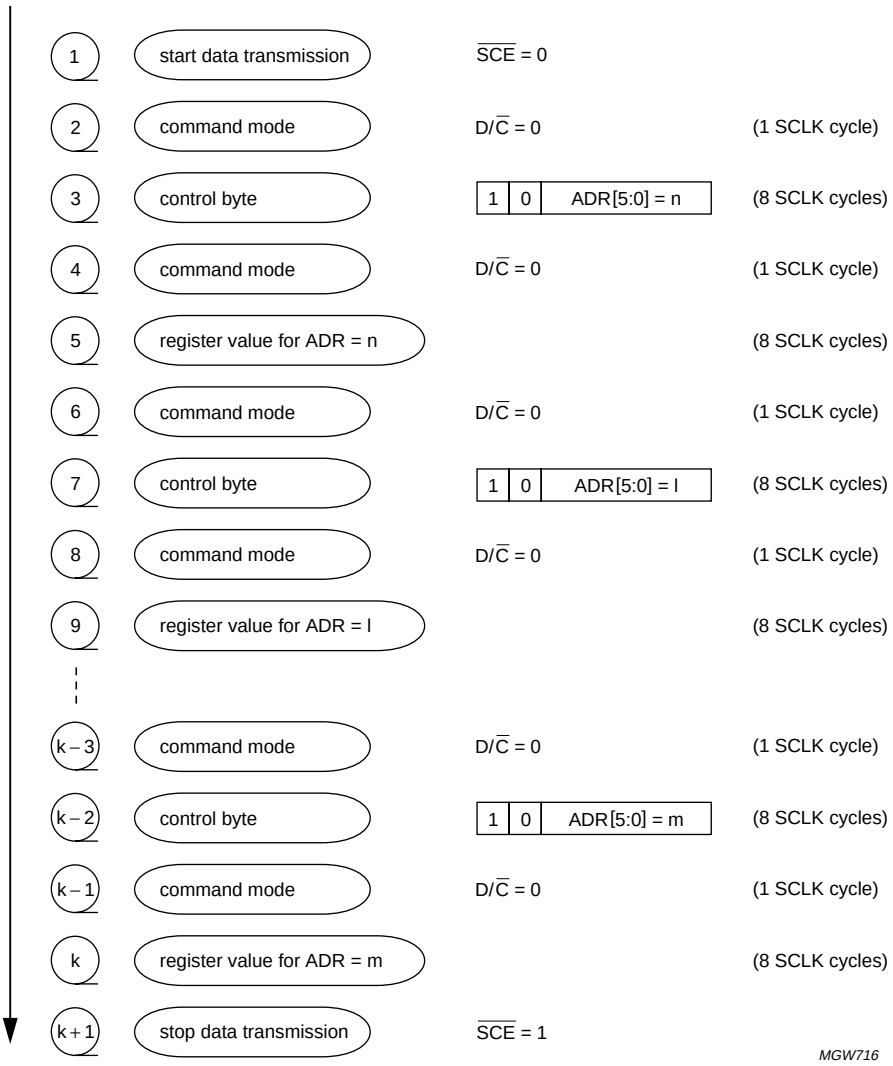


Fig.43 Write sequence to register, basic protocol.

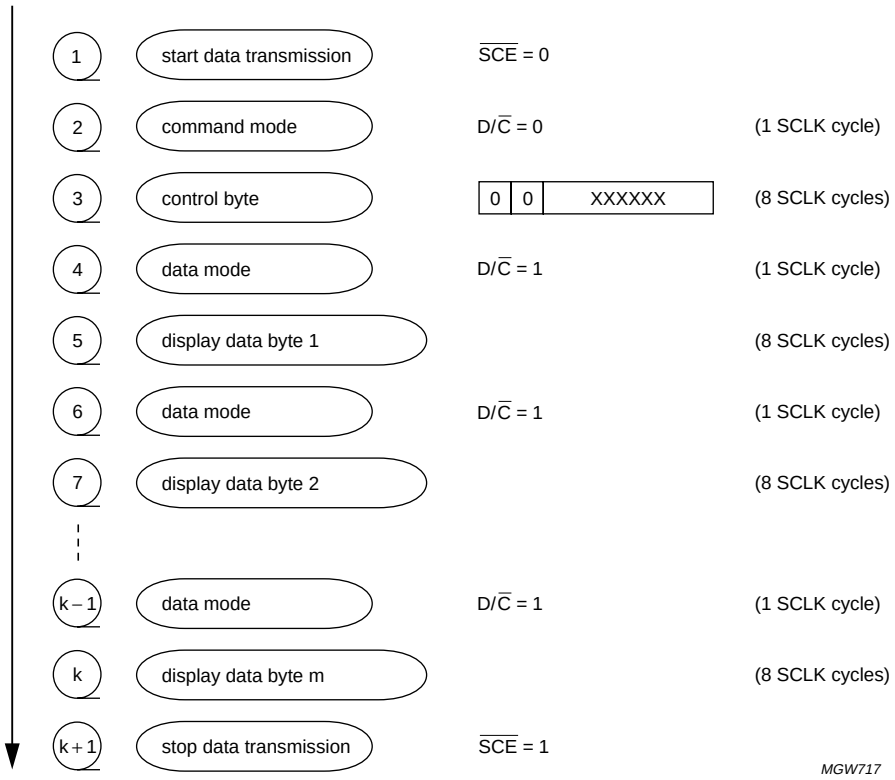


Fig.44 Write sequence to RAM, advanced protocol.

11.2.2 READ MODE (COMMAND REGISTER ONLY)

The interface read mode means the microcontroller reads data from the PCF8832. To do this the microcontroller first sends a command sequence, then transmits the following byte in the opposite direction (using SDO). After that, $\overline{SCE}$ is required to go HIGH before a new command can be sent.

The PCF8832 samples the SDI data at rising SCLK edges, but shifts SDO data at falling SCLK edges. Thus the host microcontroller must read SDO data at rising SCLK edges.

The 8th read bit is shorter than the others because it is terminated by the rising SCLK edge. The last rising SCLK edge sets SDO to 3-state after the delay time t_{ODE2}.

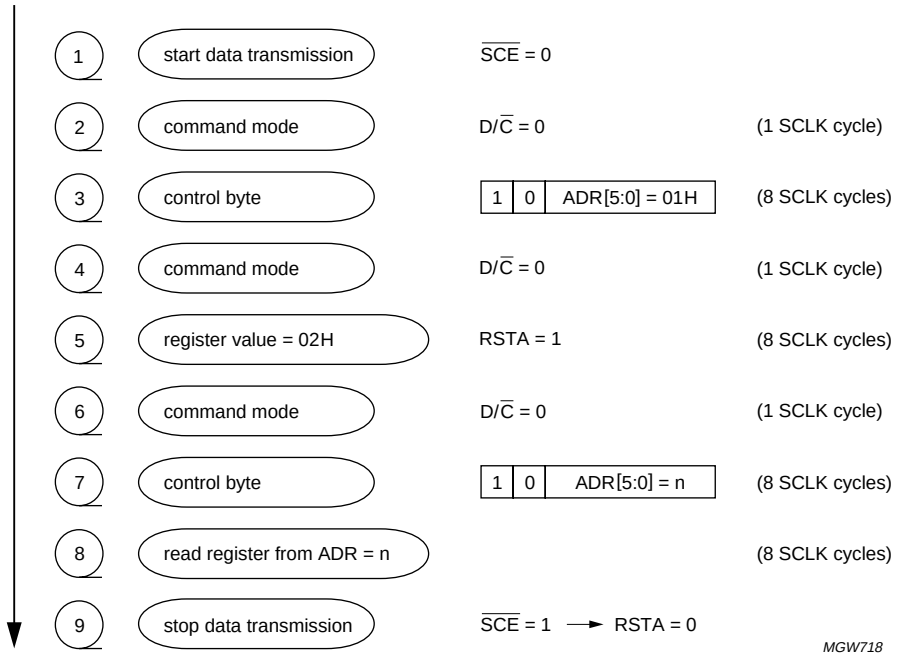


Fig.45 Read from register, basic protocol.

12 I²C-BUS INTERFACE

12.1 Characteristics of the I²C-bus (Hs-mode)

The I²C-bus Hs-mode is for bi-directional, two-line communication between different ICs or modules with speeds up to 3.4 MHz. The only difference between Hs-mode slave devices and F/S-mode slave devices is the speed at which they operate, therefore the buffers on the SCL and SDA outputs have an open drain. This is the same for I²C-bus master devices which have an open-drain SDA output and a combination of open-drain pull-down and current source pull-up circuits on the SCL output. Only the current source of one master is enabled at any one time, and only during Hs-mode. Both lines must be connected to a positive supply via a pull-up resistor.

Data transfer may be initiated only when the bus is not busy.

12.1.1 SYSTEM CONFIGURATION

Definitions of terms used:

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

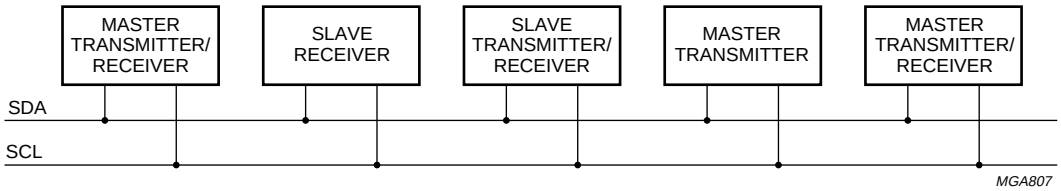


Fig.46 System configuration.

12.1.2 BIT TRANSFER

One data bit is transferred during each clock pulse (see Fig.47). The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

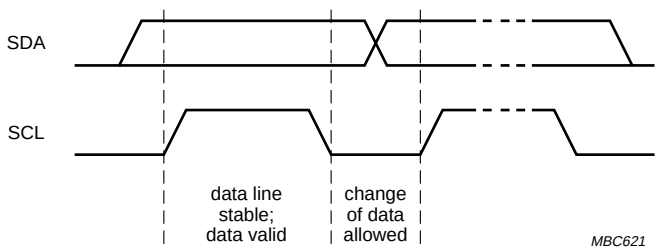


Fig.47 Bit transfer.

12.1.3 START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy (see Fig.48). A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

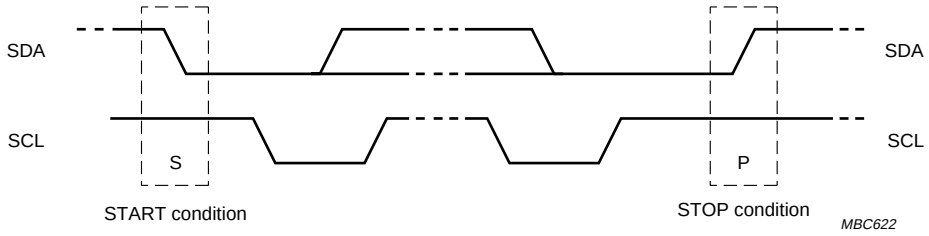


Fig.48 Definition of start and stop conditions.

12.1.4 ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit (see Fig.49). The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse.
A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

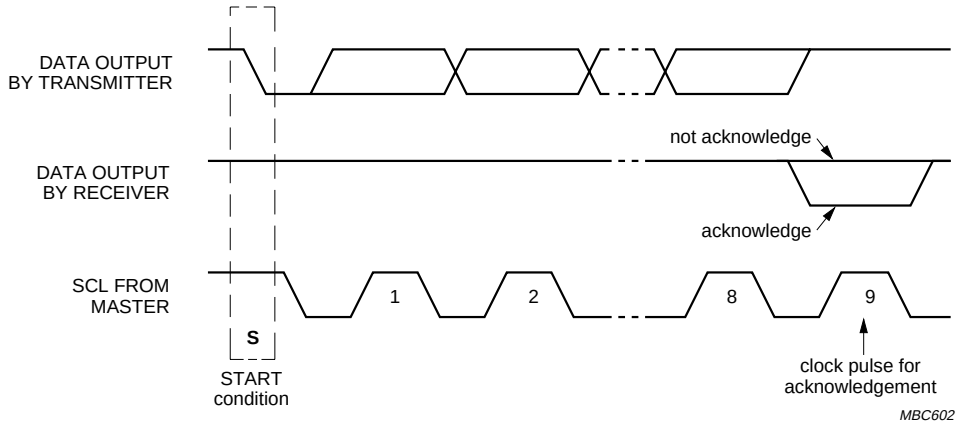


Fig.49 Acknowledge on the I^2C-bus.

12.2 I²C-bus Hs-mode protocol

The PCF8832 is a slave receiver/transmitter. If data is to be read from the device, the SDACK pin must be connected, otherwise SDACK may be unused.

Hs-mode can only commence after the following conditions:

- START condition (S)
- 8-bit master code (00001XXX)
- Not-acknowledge bit (A).

The master code has two functions, it allows arbitration and synchronization between competing masters at F/S-mode speeds, resulting in one winner. Also the master code indicates the beginning of an Hs-mode transfer. In Figs 50 and 51 these conditions are visualized.

As no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge ($\overline{A}$). After this $\overline{A}$-bit, and the SCL line has been pulled up to a HIGH level, the active master switches to Hs-mode and enables at t_H the current-source pull-up circuit for the SCL signal (see Fig.51).

The active master will then send a repeated START condition (Sr) followed by a 7-bit slave address with a R/$\overline{W}$-bit and receives an acknowledge bit (A) from the selected slave. After each acknowledge bit (A) or not-acknowledge bit ($\overline{A}$), the active master disables its current-source pull-up circuit. The active master re-enables its current source again when all devices have released and the SCL signal reaches a HIGH level. The rising of the SCL is done by a resistor pull-up and so is slower, the last part of the SCL rise time is speeded up because the current source is enabled. Data transfer only switches back to F/S-mode after a stop condition (P).

A write sequence after the Hs-mode is selected (see Fig.53) is initiated with a START condition (S) from the I²C-bus master and this is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer.

After acknowledgement of a write ($\overline{W}$) condition, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines CO and D/$\overline{C}$, plus a data byte (see Table 21, Table 22 and Fig.52).

The last control byte is tagged with a cleared most significant bit, the continuation bit CO. The control and data bytes are also acknowledged by all addressed slaves on the bus.

Table 21 Definition of CO

CO	ACTION
0	last control byte to be sent; only a stream of data bytes are allowed to follow; this stream may only be terminated by a STOP or RE-START condition
1	another control byte will follow this control byte unless a STOP or RE-START condition is received

Table 22 Definition of D/$\overline{C}$

D/$\overline{C}$	R/$\overline{W}$	ACTION
0	0	command byte will be decoded and used to set up the device
	1	command byte of requested ADR will be returned
1	0	data byte will be stored in the display RAM
	1	RAM read-back is not supported

After the last control byte, depending on the D/$\overline{C}$ bit setting, a series of display data bytes or command data bytes may follow. If the D/$\overline{C}$ bit was set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is updated automatically and the data is directed to the intended PCF8832. If the D/$\overline{C}$ bit of the last control byte was set to ‘0’, these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed PCF8832. At the end of the transmission the I²C-bus master issues a STOP condition (P) and switches back to F/S-mode, however, to reduce the overhead of the master code, it is possible for a master to link a number of Hs-mode transfers, separated by repeated START conditions (Sr).

A read sequence (Fig.53) follows after the Hs-mode is selected. The PCF8832 will immediately start to output the requested data until a NOT acknowledge is transmitted by the master. Before the read access, the user has to set the D/$\overline{C}$ bit to the appropriate value by a preceding write access. The write access should be terminated by a repeated START condition so that the Hs-mode is not disabled.

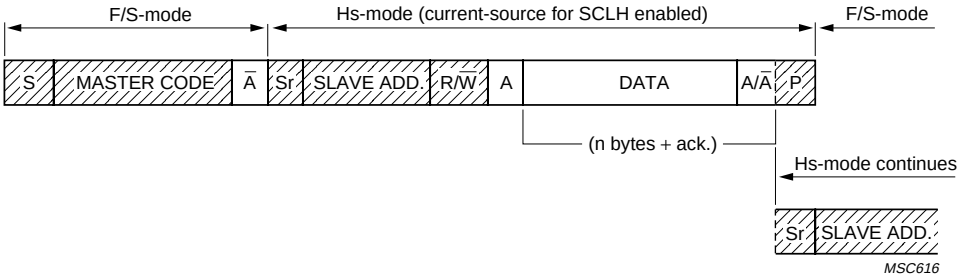


Fig.50 Data transfer format in Hs-mode.

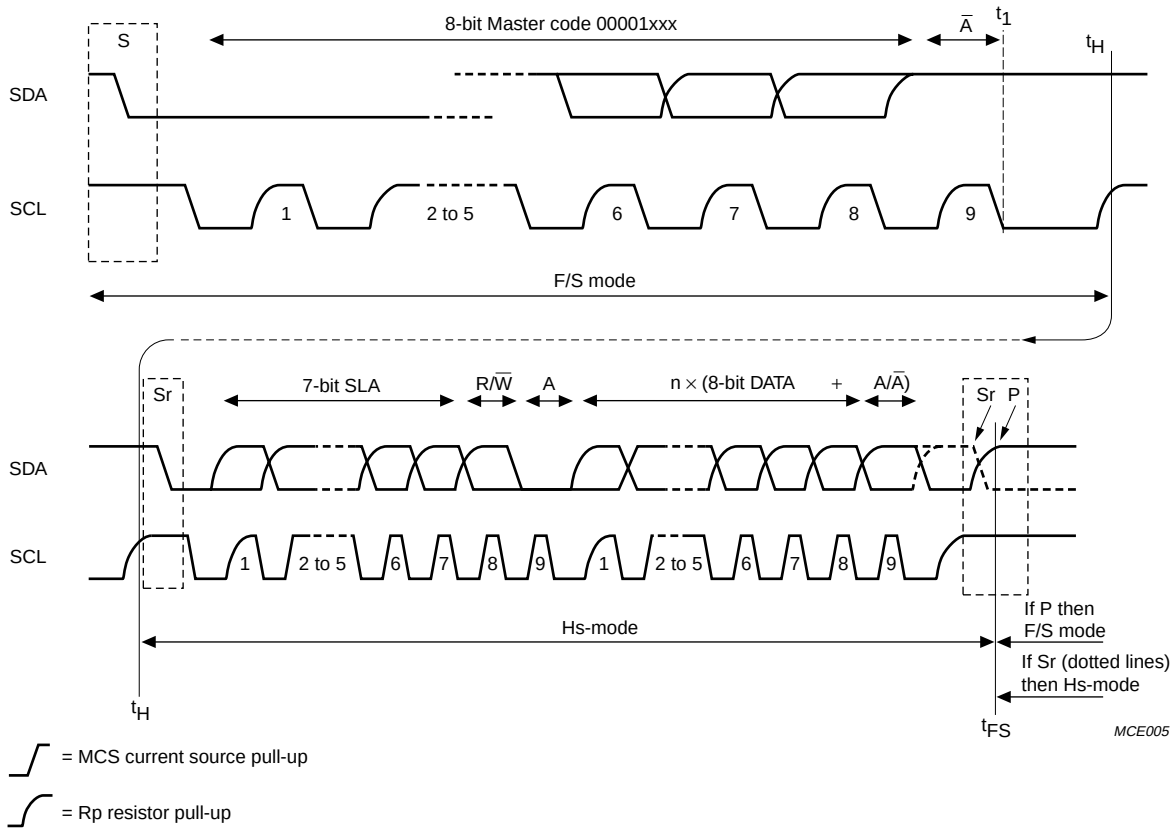


Fig.51 Complete data transfer in Hs-mode.

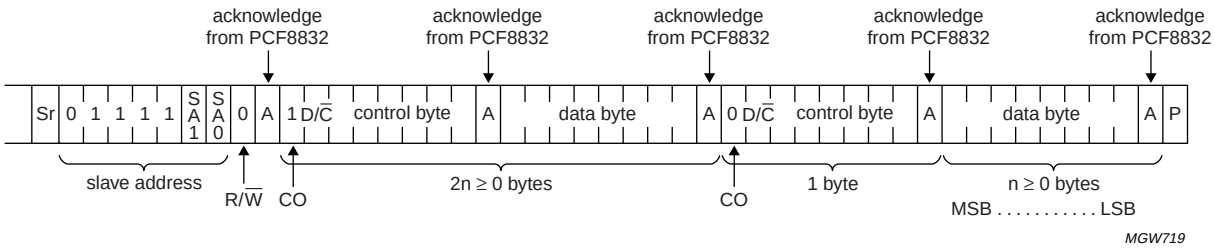


Fig.52 Master transmits in Hs-mode to slave receiver; WRITE mode.

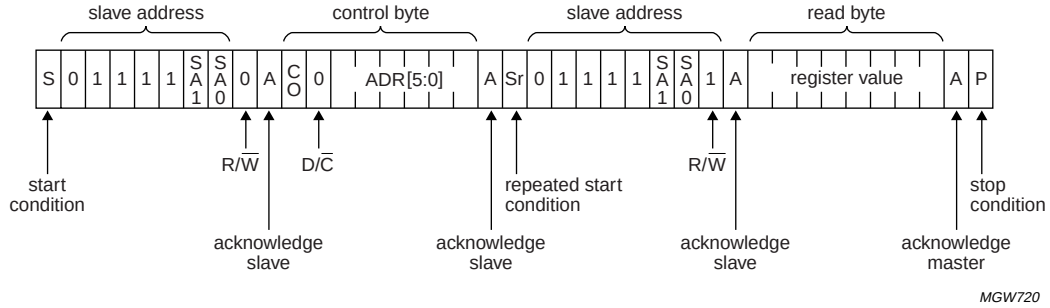


Fig.53 Master receives from slave transmitter; READ mode.

12.3 Command decoder

The command decoder identifies command words that arrive on the I²C-bus:

- Pairs of bytes
  - first byte determines whether information is display or instruction data
  - second byte contains information
- Stream of information bytes after CO = 0; display or instruction data depending on last D/$\overline{C}$ bit.

The most significant bit of a control byte is the continuation bit CO. If this bit is logic 1 it indicates that only **one** data byte, either command or RAM data, will follow. If the bit is logic 0, it indicates that a **series** of data bytes, either command or RAM data, may follow. The DB6 bit of a control byte is the RAM-data/command bit D/$\overline{C}$. When this bit is logic 1, it indicates that a RAM-data byte will be transferred next. If the bit is logic 0, it indicates that a command byte will be transferred next.

13 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}	logic supply voltage	–0.5	+4.0	V
V_{DD2}	analog supply voltage	–0.5	+4.0	V
V_{DD3}	analog supply voltage	–0.5	+4.0	V
I_{DD}	supply current	–50	+50	mA
I_{SS}	negative supply current	–50	+50	mA
V_I/V_O	input/output voltage (any input/output)	–0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
P_{tot}	total power dissipation per package	–	300	mW
T_{stg}	storage temperature	–55	+125	°C
T_j	junction temperature	–	125	°C

Note

1. Parameters are valid over the operating temperature range unless otherwise specified; all voltages are referenced to V_{SS1}; unless otherwise specified.

14 DC CHARACTERISTICS

V_{DD1} = 1.5 to 3.3 V; V_{DD2} = V_{DD3} = 2.4 to 3.5 V; V_{SS1} = V_{SS2} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD1}	logic supply voltage		1.5	–	3.3	V
V_{DD2}	analog supply voltage		2.4	–	3.5	V
V_{DD3}	analog supply voltage		2.4	–	3.5	V
V_{COL}	column driving voltage		2.5	–	4.0	V
ΔV_{COL}	V_{COL} tolerance		–100	0	+100	mV
$R_{s(CA1)}$, $R_{s(CA2)}$	series resistance of pads CA1, CA2 for external capacitor C_q connection		–	–	10	Ω
Logic						
V_{IL}	LOW-level input voltage		V_{SS1}	–	$0.2V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD1}$	–	V_{DD1}	V
$I_{OL(SDA)}$	LOW-level output current	pads SDA; V_{OL} = 0.4 V; V_{DD1} = 3.3 V	3.0	–	–	mA
I_{LI}	input leakage current	V_I = V_{DD1} or V_{SS1}	–1	–	+1	µA
$I_{DD(tot)}$	total supply current	note 1	–	260	1500	µA
$I_{DD(pd)}$	power-down mode supply current	note 1	–	25	500	µA
Column outputs						
$R_{o(COL)}$	output resistance of column driver pads C0 to C383		–	2	15	kΩ
$R_{o(Cq)}$	series resistance for external DC-to-DC converter (CA1, CA2)		–	–	10	Ω

Note

1. V_{DD1} = 1.8 V; V_{DD2} = V_{DD3} = 2.8 V; no display; display data = 0.

15 AC CHARACTERISTICS

V_{DD1} = 2.5 to 3.3 V; $V_{DD2} = V_{DD3}$ = 2.4 to 3.5 V; $V_{SS1} = V_{SS2}$ = 0 V; T_{amb} = –40 to +85 °C; note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{frame}	LCD frame frequency	internal clock; V_{DD1} = 3.0 V	20	120	400	Hz
f_{osc}	oscillator frequency	note 2	–	600	–	kHz
$f_{clk(ext)}$	external clock frequency		400	600	800	kHz
$t_{W(RESL)}$	reset LOW pulse width	see Fig.54	500	–	–	ns
$t_{SU;RESL}$	reset LOW pulse set-up time after power-on	see Fig.54	0	–	1	µs
I²C-bus interface; **Hs mode**; see Fig.55						
f_{SCL}	serial clock frequency		0	–	3.4	MHz
$t_{SU;STA}$	set-up time (repeated) START condition		160	–	–	ns
$t_{HD;STA}$	hold time (repeated) START condition		160	–	–	ns
t_{LOW}	LOW period of the SCL clock		160	–	–	ns
t_{HIGH}	HIGH period of the SCL clock		60	–	–	ns
$t_{SU;DAT}$	data set-up time		10	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	70	ns
t_{fDA}	fall time of SDA signal		20	–	80	ns
$t_{SU;STO}$	set-up time for STOP condition		160	–	–	ns
C_b	capacitive load for SDA and SCL lines	Hs-mode; note 3	–	–	100	pF
		F/S-mode	–	–	400	pF
t_{SW}	tolerable spike width on bus		–	–	5	ns
V_{nL}	noise margin at the LOW level for each connected device	including hysteresis	$0.1V_{DD1}$	–	–	V
V_{nH}	noise margin at the HIGH level for each connected device	including hysteresis	$0.2V_{DD1}$	–	–	V
8-bit parallel (8080-type) interface; note 4; see Fig.56						
t_{AH}	D/$\overline{C}$, $\overline{CS}$ address hold time		–5	–	–	ns
t_{AS}	D/$\overline{C}$, $\overline{CS}$ address set-up time		10	–	–	ns
T_{CYC}	system cycle time	note 5	160	–	–	ns
t_{CCLW}	$\overline{WR}$ control L pulse width	WRITE mode	20	–	–	ns
t_{CCLR}	$\overline{RD}$ control L pulse width	READ mode	40	–	–	ns
t_{CCHW}	$\overline{WR}$ control H pulse width	WRITE mode	15	–	–	ns
t_{CCHR}	$\overline{RD}$ control H pulse width	READ mode	15	–	–	ns
t_{DS}	D0 to D7 data set-up time		20	–	–	ns
t_{DH}	D0 to D7 data hold time		10	–	–	ns
t_{ACC}	$\overline{RD}$ access time	C_L = 50 pF		–	70	ns
t_{OH}	output disable time			–	25	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
8-bit parallel (6800-type) interface; note 6; see Fig.57						
T_{CYC}	system cycle time		160	–	–	ns
t_{AS1}	D/$\overline{C}$, $\overline{CS}$ address set-up time		50	–	–	ns
t_{AS2}	R/$\overline{W}$ address set-up time		50	–	–	ns
t_{AH1}	D/$\overline{C}$, $\overline{CS}$ address hold time		10	–	–	ns
t_{AH2}	R/$\overline{W}$ address hold time		35	–	–	ns
t_{DS}	D0 to D7 data set-up time		20	–	–	ns
t_{DH}	D0 to D7 data hold time		10	–	–	ns
t_{OH}	D0 to D7 output disable time	C_L = 50 pF	10	–	30	ns
t_{ACC}	D0 to D7 access time		–	–	70	ns
t_{EH}	E pulse width HIGH		40	–	–	ns
t_{EL}	E pulse width LOW		60	–	–	ns
Serial interface; note 7; see Figs 58**,** 59 and 60						
T_{SCYC}	serial clock SCLK period		160	–	–	ns
t_{SHW}	SCLK pulse width HIGH		60	–	–	ns
t_{SLW}	SCLK pulse width LOW		60	–	–	ns
t_{SAH}	D/$\overline{C}$ address hold time		70	–	–	ns
t_{SAS}	D/$\overline{C}$ address setup time		45	–	–	ns
t_{SDS}	SDI data set-up time		45	–	–	ns
t_{SDH}	SDI data hold time		50	–	–	ns
t_{CSS}	$\overline{SCE}$ to SCLK set-up time		30	–	–	ns
t_{CSH}	$\overline{SCE}$ to SCLK hold time		120	–	–	ns
t_{ODE1}	SDO disable time		–	–	50	ns
t_{ODE2}	SDO disable time		25	–	100	ns
t_{CEH}	SCLK to $\overline{SCE}$ hold time		50	–	–	ns
t_{ACC}	SCLK to SDO access time		–	–	50	ns

Notes

1. All timing values are valid within the operating ambient temperature and supply voltage ranges and are referred to V_{IL} and V_{IH} with an input voltage swing of V_{SS1} to V_{DD1}.
2. Not directly observable at any pin.
3. C_b = total capacitance of one bus line in pF.
4. The input signal rise time and fall time (t_r and t_f) are specified at 15 ns or less. When the cycle time is used at high-speed, the specification is $t_r + t_f \leq (T_{CYC} - t_{CCLW} - t_{CCHW})$ or $t_r + t_f \leq (T_{CYC} - t_{CCLR} - t_{CCHR})$.
5. The system cycle time can be derated for different values of V_{DD1}. For $V_{DD1} < 2.5$ V the system cycle time can be calculated as follows:
   at V_{DD1} = 2.5 V, $f_{CYC(2.5)}$ = 6.25 MHz and Δf = 0.44 MHz/V then $f_{CYC(VDD1)} = f_{CYC(2.5)} \times 0.44 \times V_{DD1}$ MHz.
6. The input signal rise time and fall time (t_r and t_f) are specified at 15 ns or less. When the cycle time is used at high-speed, the specification is $t_r + t_f \leq (T_{CYC} - t_{EH} - t_{EL})$.
7. The input signal rise time and fall time (t_r and t_f) are specified at 15 ns or less.

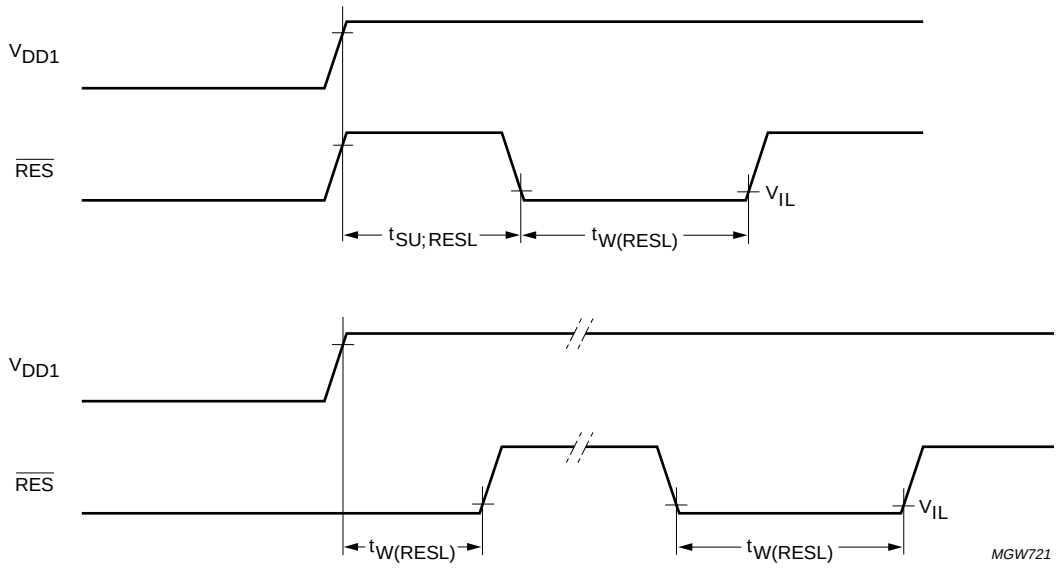
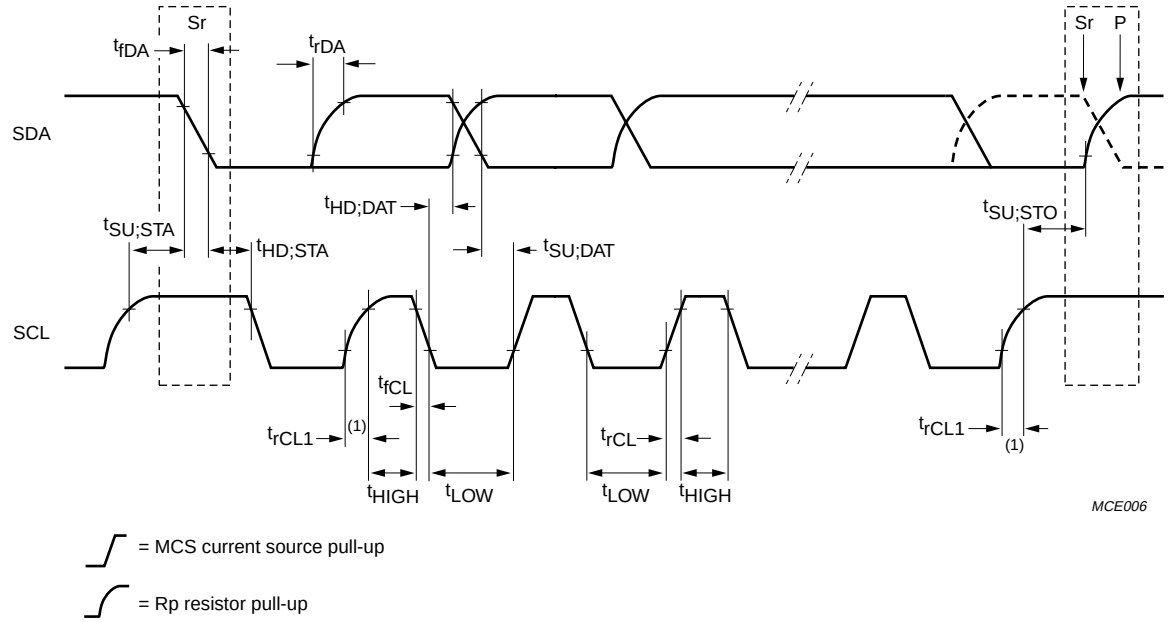


Fig.54 Reset timing.



(1) Rising edge of the first SCL clock pulse after an acknowledge bit.

Fig.55 I^2C-bus timing diagram (Hs-mode).

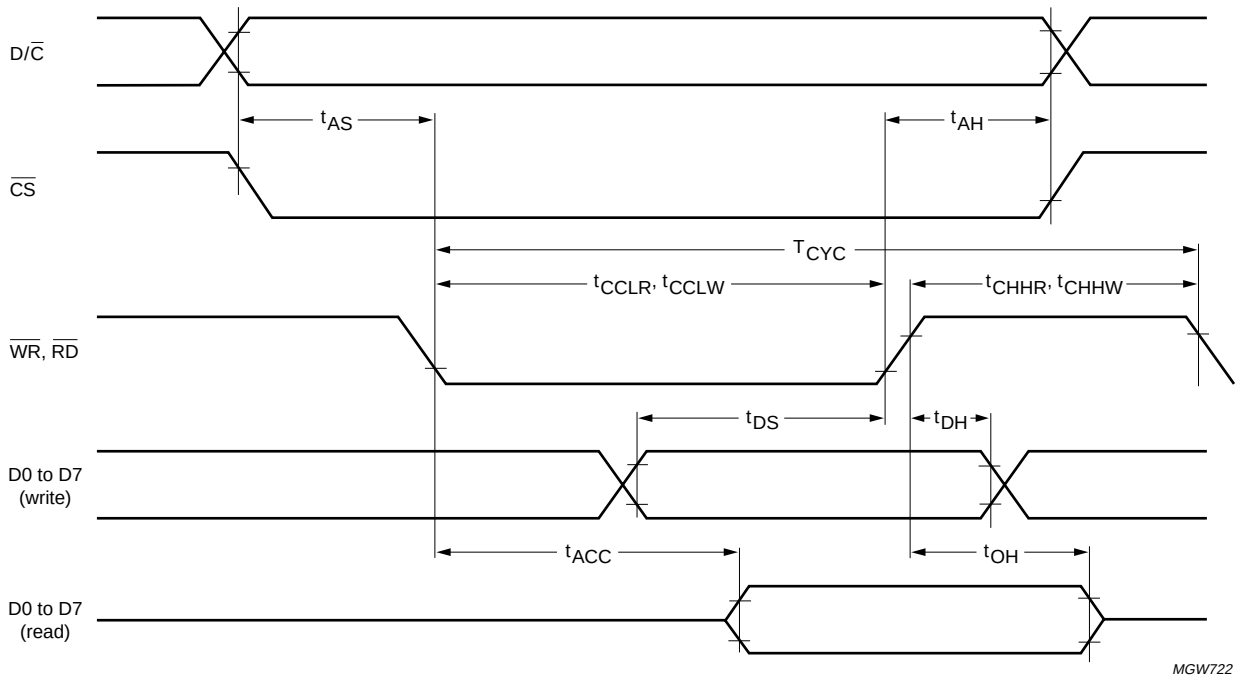


Fig.56 8080 type - parallel interface timing.

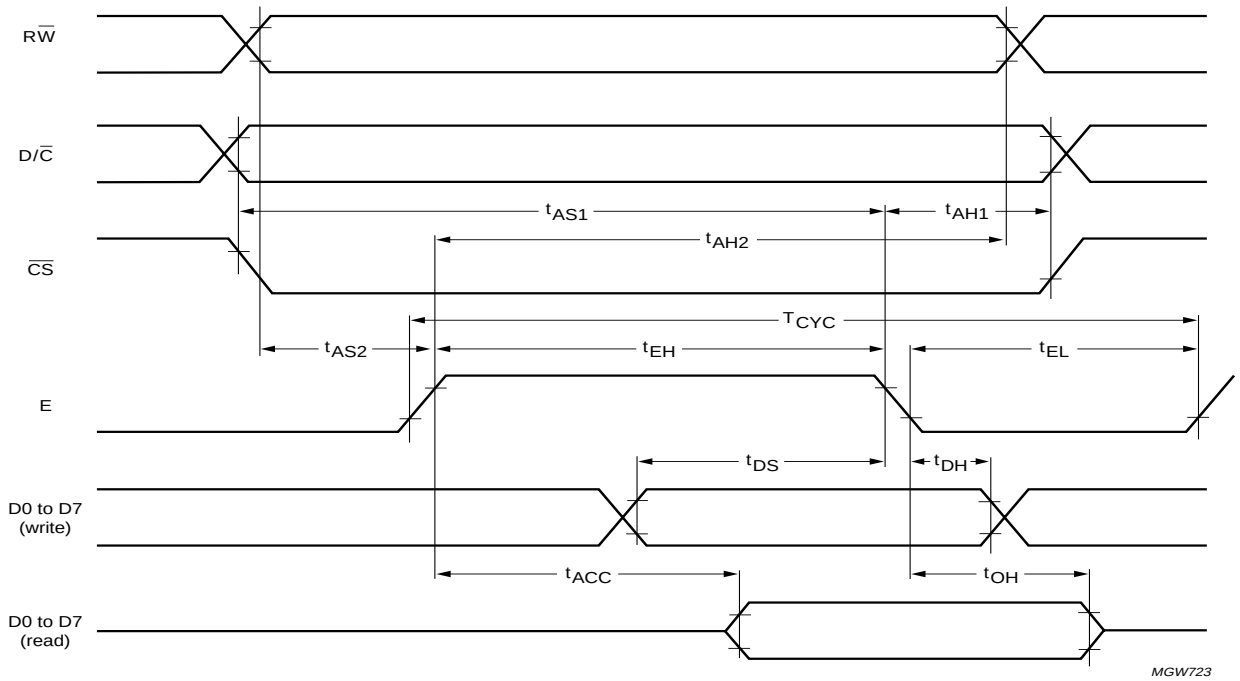


Fig.57 6800 type - parallel interface timing.

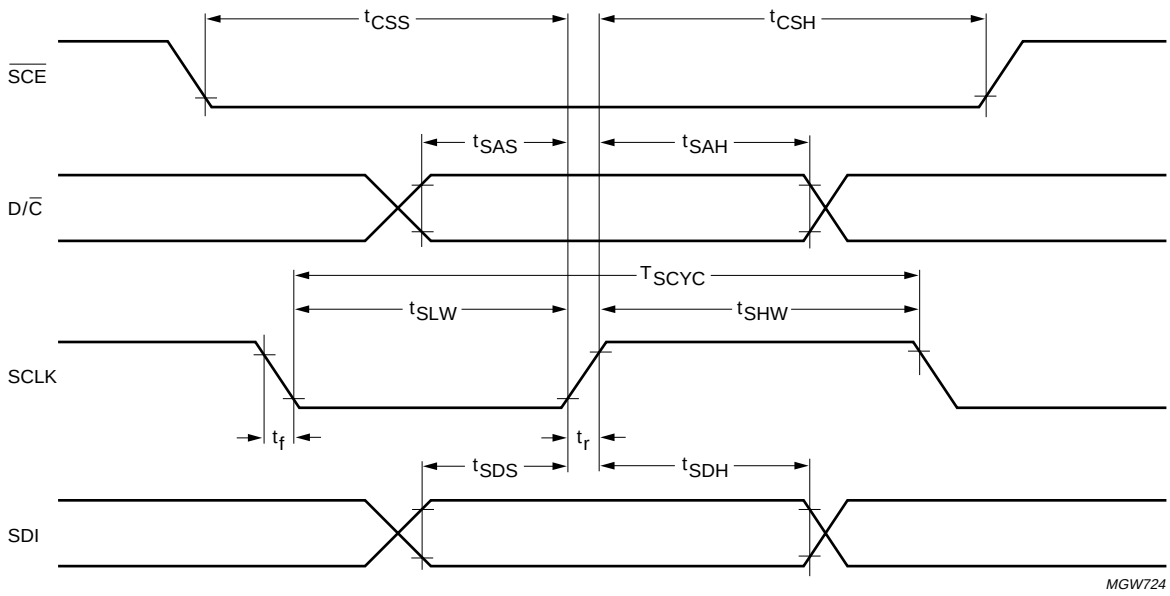


Fig.58 Serial interface timing.

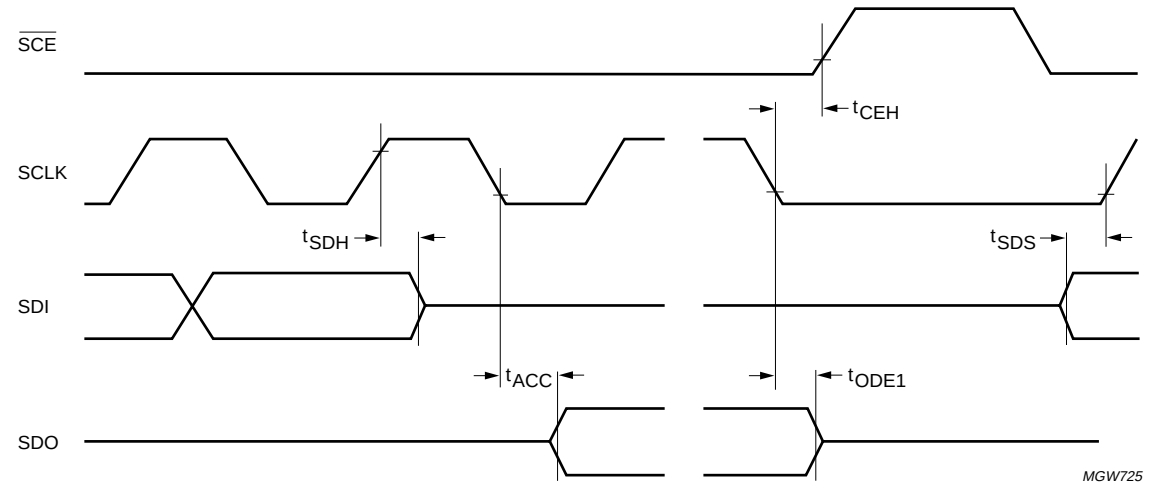


Fig.59 Serial interface timing - read mode SPI 3 or 4-line.

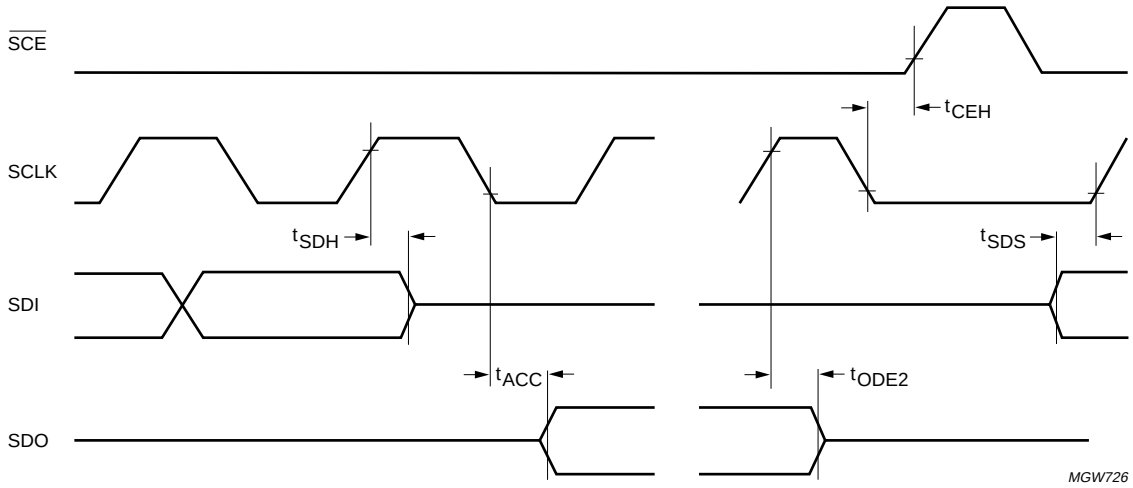


Fig.60 Serial interface timing - read mode serial interface 3-line.

16 APPLICATION INFORMATION

The pinning of the PCF8832 is organized for single plane wiring, for example chip-on-glass, TCP and COF display modules. The display size is 160 × 128 RGB STN pixels. The host microcontroller and the PCF8832 are both connected to the interface bus.

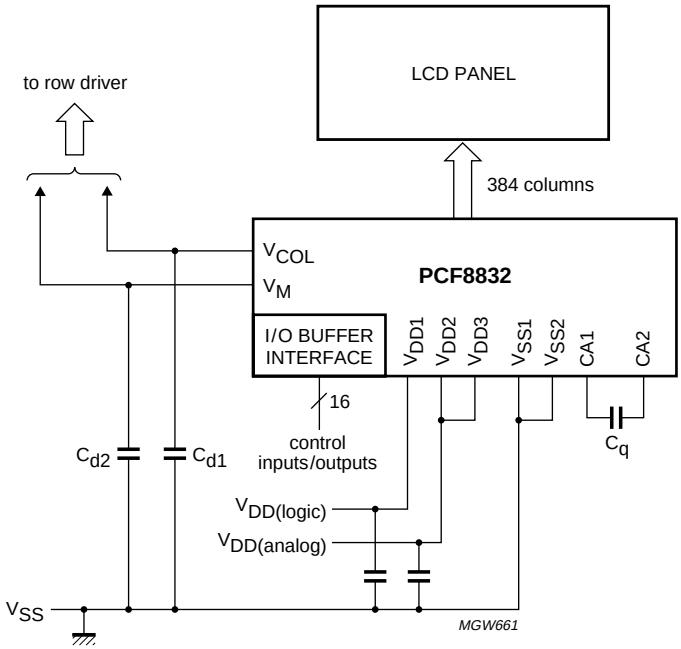
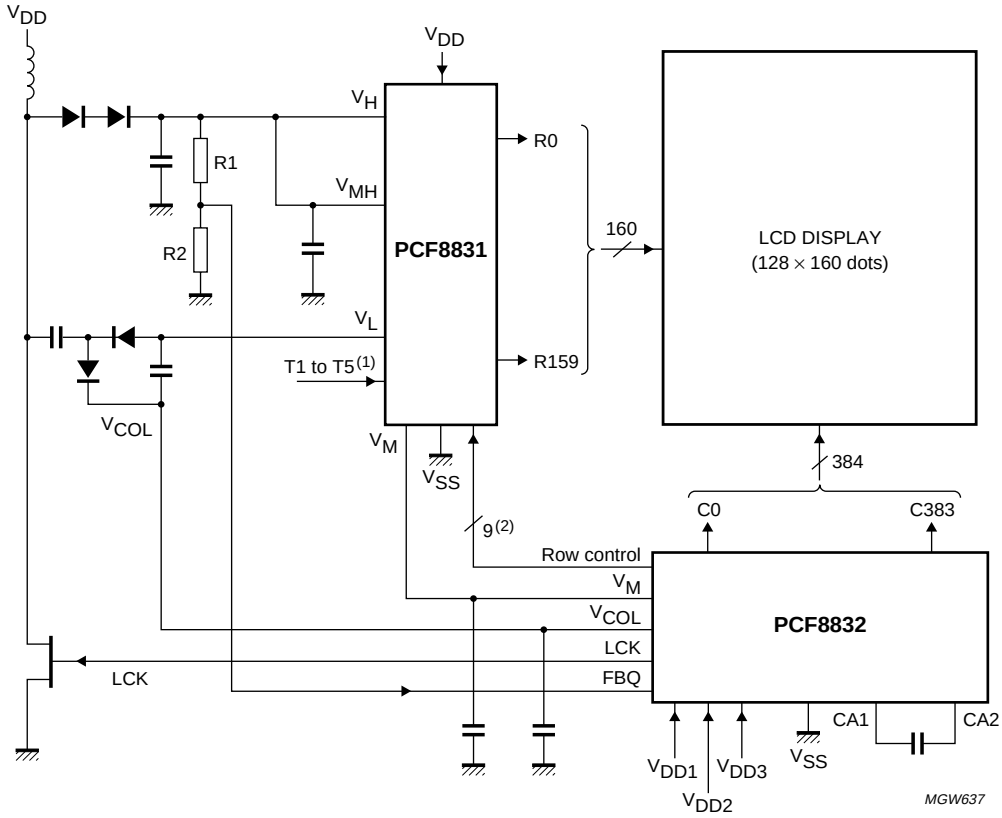


Fig.61 Application configuration (master/slave control inputs and row driver signal not shown).

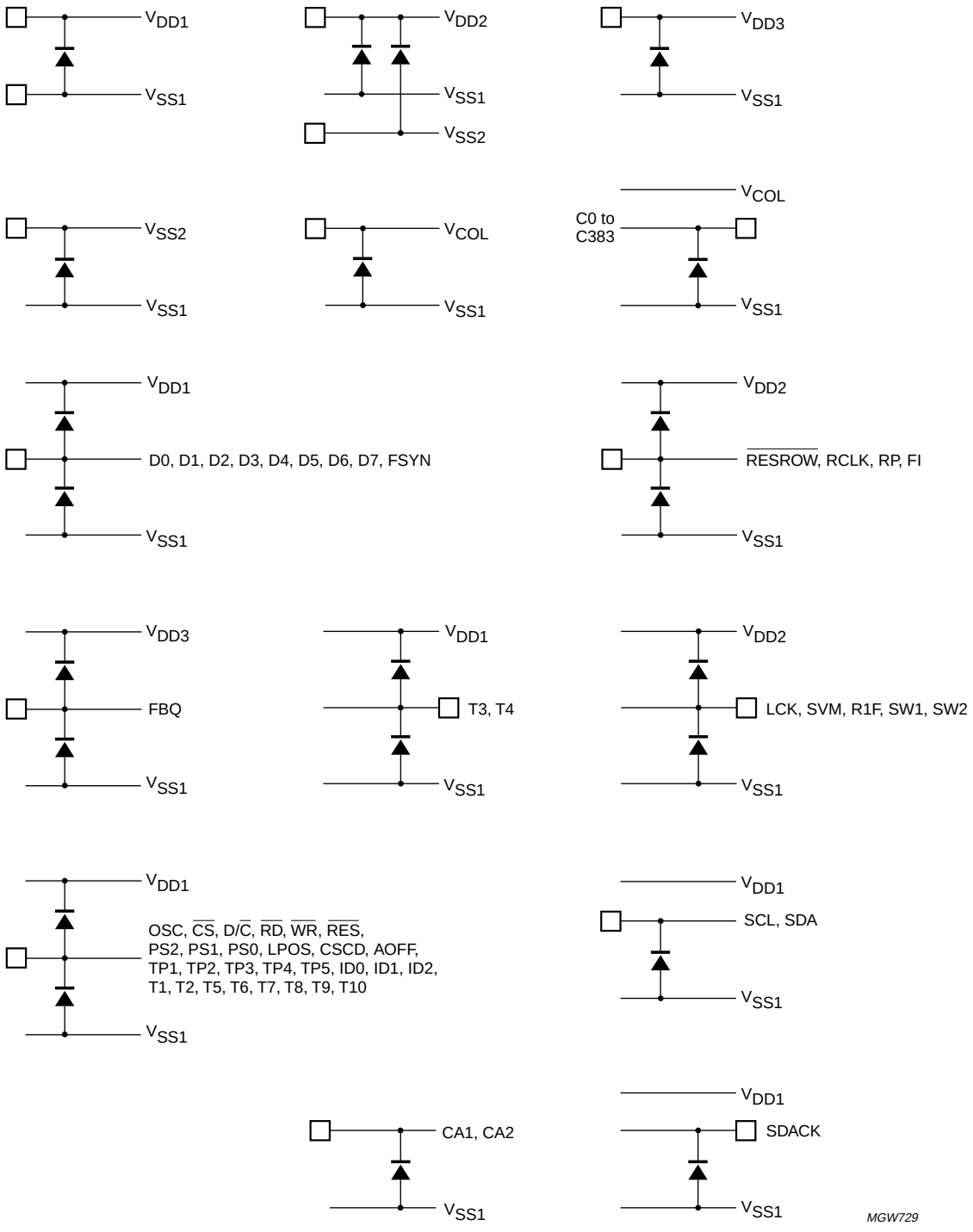


(1) Test inputs T1 to T5 have to be tied to V_{SS}.

(2) Row control signals are RCLK, RP, FI, SVM, ROWRES1, ROWRES2, SW1, SW2 and R1F.

Fig.62 Application example using PCF8831 with PCF8832.

17 INTERNAL PROTECTION CIRCUITS



Protection diode maximum forward current = 5 mA; maximum reverse voltage = 4 V.

Fig.63 Protection circuit diagrams.

18 BONDING PAD INFORMATION

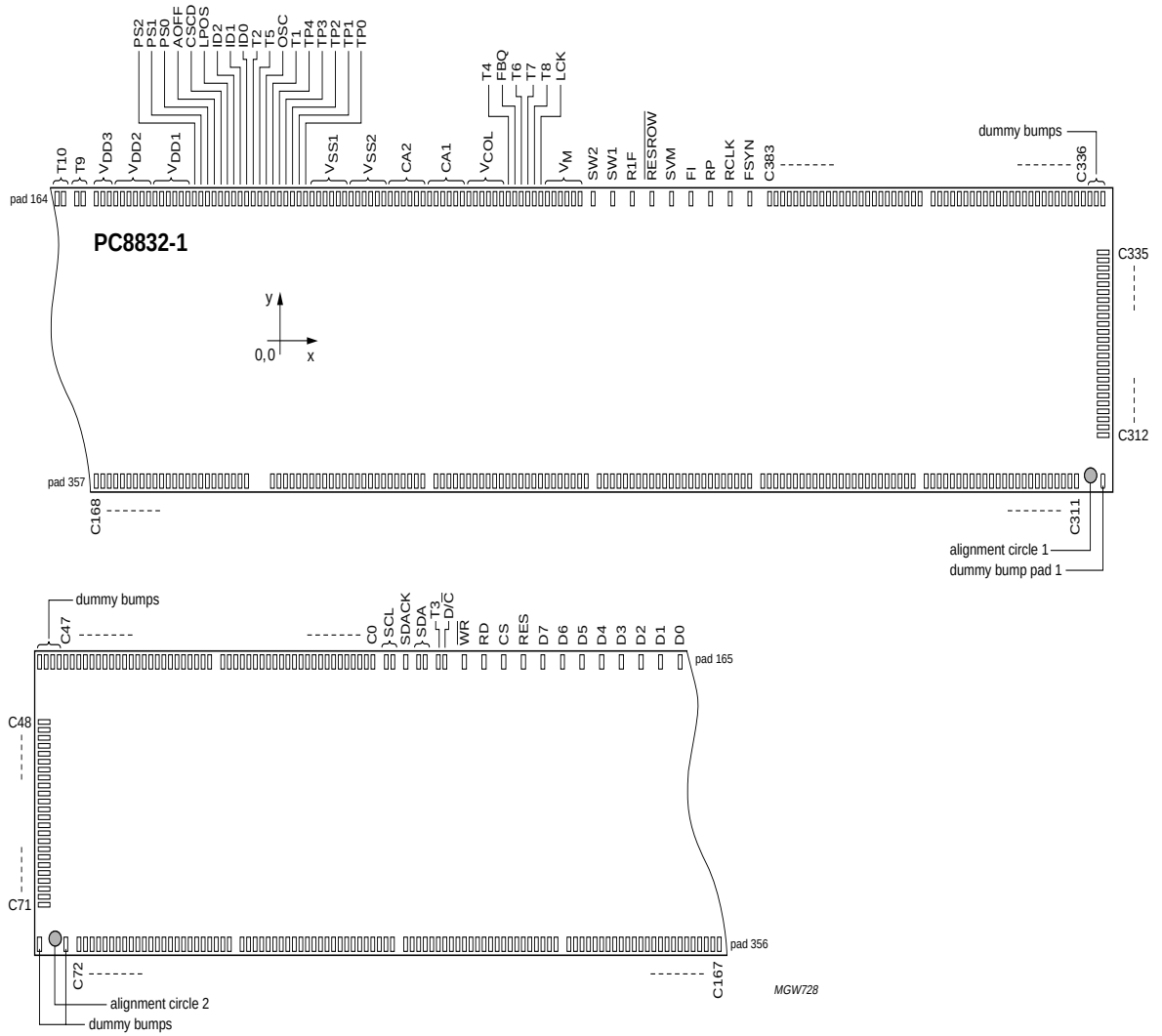


Fig.64 Location of bonding pads (refer also to Table 23).

Table 23 Bonding pad locations
All x and y coordinates are referenced to the centre of the chip (dimensions in μm; see Fig.64).

SYMBOL	PAD	COORDINATES	
		x	y
dummy 6	1	6874	−1000
C312	2	6875	−635.8
C313	3	6875	−582.8
C314	4	6875	−529.8
C315	5	6875	−476.8
C316	6	6875	−423.8
C317	7	6875	−370.8
C318	8	6875	−317.8
C319	9	6875	−264.8
C320	10	6875	−211.8
C321	11	6875	−158.8
C322	12	6875	−105.8
C323	13	6875	−52.8
C324	14	6875	0.2
C325	15	6875	53.2
C326	16	6875	106.2
C327	17	6875	159.2
C328	18	6875	212.2
C329	19	6875	265.2
C330	20	6875	318.2
C331	21	6875	371.2
C332	22	6875	424.2
C333	23	6875	477.2
C334	24	6875	530.2
C335	25	6875	583.2
dummy 7	26	6874	1000
dummy 8	27	6821	1000
dummy 9	28	6768	1000
C336	29	6715	1000
C337	30	6662	1000
C338	31	6609	1000
C339	32	6556	1000
C340	33	6503	1000
C341	34	6450	1000
C342	35	6397	1000
C343	36	6344	1000
C344	37	6291	1000
C345	38	6238	1000
C346	39	6185	1000
C347	40	6132	1000
C348	41	6079	1000
C349	42	6026	1000
C350	43	5973	1000
C351	44	5920	1000
C352	45	5867	1000
C353	46	5814	1000
C354	47	5761	1000
C355	48	5708	1000
C356	49	5655	1000
C357	50	5602	1000
C358	51	5549	1000
C359	52	5496	1000
C360	53	5390	1000
C361	54	5337	1000
C362	55	5284	1000
C363	56	5231	1000
C364	57	5178	1000
C365	58	5125	1000
C366	59	5072	1000
C367	60	5019	1000
C368	61	4966	1000
C369	62	4913	1000
C370	63	4860	1000
C371	64	4807	1000
C372	65	4754	1000
C373	66	4701	1000
C374	67	4648	1000
C375	68	4595	1000
C376	69	4542	1000
C377	70	4489	1000
C378	71	4436	1000
C379	72	4383	1000
C380	73	4330	1000
C381	74	4277	1000
C382	75	4224	1000
C383	76	4171	1000

SYMBOL	PAD	COORDINATES	
		x	y
FSYN	77	4012	1000.1
RCLK	78	3853	1000.1
RP	79	3694	1000.1
FI	80	3535	1000.1
SVM	81	3376	1000.1
$\overline{\text{RESROW}}$	82	3217	1000.1
R1F	83	3058	1000.1
SW1	84	2899	1000.1
SW2	85	2740	1000.1
V_M	86	2634	1000
V_M	87	2581	1000
V_M	88	2528	1000
V_M	89	2475	1000
V_M	90	2422	1000
V_M	91	2369	1000
LCK	92	2316	1000.1
T8	93	2263	1000.1
T7	94	2210	1000.1
T6	95	2157	1000.1
FBQ	96	2104	1000.1
T4	97	2051	1000.1
V_{COL}	98	1998	1000
V_{COL}	99	1945	1000
V_{COL}	100	1892	1000
V_{COL}	101	1839	1000
V_{COL}	102	1786	1000
V_{COL}	103	1733	1000
CA1	104	1680	1000
CA1	105	1627	1000
CA1	106	1574	1000
CA1	107	1521	1000
CA1	108	1468	1000
CA1	109	1415	1000
CA2	110	1362	1000
CA2	111	1309	1000
CA2	112	1256	1000
CA2	113	1203	1000
CA2	114	1150	1000
CA2	115	1097	1000

SYMBOL	PAD	COORDINATES	
		x	y
V_{SS2}	116	1044	1000
V_{SS2}	117	991	1000
V_{SS2}	118	938	1000
V_{SS2}	119	885	1000
V_{SS2}	120	832	1000
V_{SS2}	121	779	1000
V_{SS1}	122	726	1000
V_{SS1}	123	673	1000
V_{SS1}	124	620	1000
V_{SS1}	125	567	1000
V_{SS1}	126	514	1000
V_{SS1}	127	461	1000
TP0	128	408	1000.1
TP1	129	355	1000.1
TP2	130	302	1000.1
TP3	131	249	1000.1
TP4	132	196	1000.1
T1	133	143	1000.1
OSC	134	90	1000.1
T5	135	37	1000.1
T2	136	–16	1000.1
ID0	137	–69	1000.1
ID1	138	–122	1000.1
ID2	139	–175	1000.1
LPOS	140	–228	1000.1
CSCD	141	–281	1000.1
AOFF	142	–334	1000.1
PS0	143	–387	1000.1
PS1	144	–440	1000.1
PS2	145	–493	1000.1
V_{DD1}	146	–546	1000
V_{DD1}	147	–599	1000
V_{DD1}	148	–652	1000
V_{DD1}	149	–705	1000
V_{DD1}	150	–758	1000
V_{DD1}	151	–811	1000
V_{DD2}	152	–864	1000
V_{DD2}	153	–917	1000
V_{DD2}	154	–970	1000

SYMBOL	PAD	COORDINATES	
		x	y
V_{DD2}	155	–1023	1000
V_{DD2}	156	–1076	1000
V_{DD2}	157	–1129	1000
V_{DD3}	158	–1182	1000
V_{DD3}	159	–1235	1000
V_{DD3}	160	–1288	1000
T9	161	–1394	1000
T9	162	–1447	1000
T10	163	–1553	1000
T10	164	–1606	1000
D0	165	–1712	1000.1
D1	166	–1871	1000
D2	167	–2030	1000.1
D3	168	–2189	1000.1
D4	169	–2348	1000.1
D5	170	–2507	1000.1
D6	171	–2666	1000.1
D7	172	–2825	1000.1
$\overline{RES}$	173	–2984	1000
CS	174	–3143	1000.1
RD	175	–3302	1000.1
WR	176	–3461	1000.1
$D\overline{C}$	177	–3620	1000.1
T3	178	–3673	1000.1
SDA	179	–3779	1000
SDA	180	–3832	1000
SDACK	181	–3938	1000
SCL	182	–4044	1000
SCL	183	–4097	1000
C0	184	–4203	1000
C1	185	–4256	1000
C2	186	–4309	1000
C3	187	–4362	1000
C4	188	–4415	1000
C5	189	–4468	1000
C6	190	–4521	1000
C7	191	–4574	1000
C8	192	–4627	1000
C9	193	–4680	1000

SYMBOL	PAD	COORDINATES	
		x	y
C10	194	–4733	1000
C11	195	–4786	1000
C12	196	–4839	1000
C13	197	–4892	1000
C14	198	–4945	1000
C15	199	–4998	1000
C16	200	–5051	1000
C17	201	–5104	1000
C18	202	–5157	1000
C19	203	–5210	1000
C20	204	–5263	1000
C21	205	–5316	1000
C22	206	–5369	1000
C23	207	–5422	1000
C24	208	–5528	1000
C25	209	–5581	1000
C26	210	–5634	1000
C27	211	–5687	1000
C28	212	–5740	1000
C29	213	–5793	1000
C30	214	–5846	1000
C31	215	–5899	1000
C32	216	–5952	1000
C33	217	–6005	1000
C34	218	–6058	1000
C35	219	–6111	1000
C36	220	–6164	1000
C37	221	–6217	1000
C38	222	–6270	1000
C39	223	–6323	1000
C40	224	–6376	1000
C41	225	–6429	1000
C42	226	–6482	1000
C43	227	–6535	1000
C44	228	–6588	1000
C45	229	–6641	1000
C46	230	–6694	1000
C47	231	–6747	1000
dummy 1	232	–6800	1000

SYMBOL	PAD	COORDINATES	
		x	y
dummy 2	233	–6853	1000
dummy 3	234	–6906	1000
C48	235	–6875	540.2
C49	236	–6875	487.2
C50	237	–6875	434.2
C51	238	–6875	381.2
C52	239	–6875	328.2
C53	240	–6875	275.2
C54	241	–6875	222.2
C55	242	–6875	169.2
C56	243	–6875	116.2
C57	244	–6875	63.2
C58	245	–6875	10.2
C59	246	–6875	–42.8
C60	247	–6875	–95.8
C61	248	–6875	–148.8
C62	249	–6875	–201.8
C63	250	–6875	–254.8
C64	251	–6875	–307.8
C65	252	–6875	–360.8
C66	253	–6875	–413.8
C67	254	–6875	–466.8
C68	255	–6875	–519.8
C69	256	–6875	–572.8
C70	257	–6875	–625.8
C71	258	–6875	–678.8
dummy 4	259	–6906	–1000
dummy 5	260	–6694	–1000
C72	261	–6588	–1000
C73	262	–6535	–1000
C74	263	–6482	–1000
C75	264	–6429	–1000
C76	265	–6376	–1000
C77	266	–6323	–1000
C78	267	–6270	–1000
C79	268	–6217	–1000
C80	269	–6164	–1000
C81	270	–6111	–1000
C82	271	–6058	–1000

SYMBOL	PAD	COORDINATES	
		x	y
C83	272	–6005	–1000
C84	273	–5952	–1000
C85	274	–5899	–1000
C86	275	–5846	–1000
C87	276	–5793	–1000
C88	277	–5740	–1000
C89	278	–5687	–1000
C90	279	–5634	–1000
C91	280	–5581	–1000
C92	281	–5528	–1000
C93	282	–5475	–1000
C94	283	–5422	–1000
C95	284	–5369	–1000
C96	285	–5263	–1000
C97	286	–5210	–1000
C98	287	–5157	–1000
C99	288	–5104	–1000
C100	289	–5051	–1000
C101	290	–4998	–1000
C102	291	–4945	–1000
C103	292	–4892	–1000
C104	293	–4839	–1000
C105	294	–4786	–1000
C106	295	–4733	–1000
C107	296	–4680	–1000
C108	297	–4627	–1000
C109	298	–4574	–1000
C110	299	–4521	–1000
C111	300	–4468	–1000
C112	301	–4415	–1000
C113	302	–4362	–1000
C114	303	–4309	–1000
C115	304	–4256	–1000
C116	305	–4203	–1000
C117	306	–4150	–1000
C118	307	–4097	–1000
C119	308	–4044	–1000
C120	309	–3938	–1000
C121	310	–3885	–1000

SYMBOL	PAD	COORDINATES	
		x	y
C122	311	–3832	–1000
C123	312	–3779	–1000
C124	313	–3726	–1000
C125	314	–3673	–1000
C126	315	–3620	–1000
C127	316	–3567	–1000
C128	317	–3514	–1000
C129	318	–3461	–1000
C130	319	–3408	–1000
C131	320	–3355	–1000
C132	321	–3302	–1000
C133	322	–3249	–1000
C134	323	–3196	–1000
C135	324	–3143	–1000
C136	325	–3090	–1000
C137	326	–3037	–1000
C138	327	–2984	–1000
C139	328	–2931	–1000
C140	329	–2878	–1000
C141	330	–2825	–1000
C142	331	–2772	–1000
C143	332	–2719	–1000
C144	333	–2613	–1000
C145	334	–2560	–1000
C146	335	–2507	–1000
C147	336	–2454	–1000
C148	337	–2401	–1000
C149	338	–2348	–1000
C150	339	–2295	–1000
C151	340	–2242	–1000
C152	341	–2189	–1000
C153	342	–2136	–1000
C154	343	–2083	–1000
C155	344	–2030	–1000
C156	345	–1977	–1000
C157	346	–1924	–1000
C158	347	–1871	–1000
C159	348	–1818	–1000
C160	349	–1765	–1000

SYMBOL	PAD	COORDINATES	
		x	y
C161	350	–1712	–1000
C162	351	–1659	–1000
C163	352	–1606	–1000
C164	353	–1553	–1000
C165	354	–1500	–1000
C166	355	–1447	–1000
C167	356	–1394	–1000
C168	357	–1288	–1000
C169	358	–1235	–1000
C170	359	–1182	–1000
C171	360	–1129	–1000
C172	361	–1076	–1000
C173	362	–1023	–1000
C174	363	–970	–1000
C175	364	–917	–1000
C176	365	–864	–1000
C177	366	–811	–1000
C178	367	–758	–1000
C179	368	–705	–1000
C180	369	–652	–1000
C181	370	–599	–1000
C182	371	–546	–1000
C183	372	–493	–1000
C184	373	–440	–1000
C185	374	–387	–1000
C186	375	–334	–1000
C187	376	–281	–1000
C188	377	–228	–1000
C189	378	–175	–1000
C190	379	–122	–1000
C191	380	–69	–1000
C192	381	143	–1000
C193	382	196	–1000
C194	383	249	–1000
C195	384	302	–1000
C196	385	355	–1000
C197	386	408	–1000
C198	387	461	–1000
C199	388	514	–1000

SYMBOL	PAD	COORDINATES	
		x	y
C200	389	567	–1000
C201	390	620	–1000
C202	391	673	–1000
C203	392	726	–1000
C204	393	779	–1000
C205	394	832	–1000
C206	395	885	–1000
C207	396	938	–1000
C208	397	991	–1000
C209	398	1044	–1000
C210	399	1097	–1000
C211	400	1150	–1000
C212	401	1203	–1000
C213	402	1256	–1000
C214	403	1309	–1000
C215	404	1362	–1000
C216	405	1468	–1000
C217	406	1521	–1000
C218	407	1574	–1000
C219	408	1627	–1000
C220	409	1680	–1000
C221	410	1733	–1000
C222	411	1786	–1000
C223	412	1839	–1000
C224	413	1892	–1000
C225	414	1945	–1000
C226	415	1998	–1000
C227	416	2051	–1000
C228	417	2104	–1000
C229	418	2157	–1000
C230	419	2210	–1000
C231	420	2263	–1000
C232	421	2316	–1000
C233	422	2369	–1000
C234	423	2422	–1000
C235	424	2475	–1000
C236	425	2528	–1000
C237	426	2581	–1000
C238	427	2634	–1000

SYMBOL	PAD	COORDINATES	
		x	y
C239	428	2687	–1000
C240	429	2793	–1000
C241	430	2846	–1000
C242	431	2899	–1000
C243	432	2952	–1000
C244	433	3005	–1000
C245	434	3058	–1000
C246	435	3111	–1000
C247	436	3164	–1000
C248	437	3217	–1000
C249	438	3270	–1000
C250	439	3323	–1000
C251	440	3376	–1000
C252	441	3429	–1000
C253	442	3482	–1000
C254	443	3535	–1000
C255	444	3588	–1000
C256	445	3641	–1000
C257	446	3694	–1000
C258	447	3747	–1000
C259	448	3800	–1000
C260	449	3853	–1000
C261	450	3906	–1000
C262	451	3959	–1000
C263	452	4012	–1000
C264	453	4118	–1000
C265	454	4171	–1000
C266	455	4224	–1000
C267	456	4277	–1000
C268	457	4330	–1000
C269	458	4383	–1000
C270	459	4436	–1000
C271	460	4489	–1000
C272	461	4542	–1000
C273	462	4595	–1000
C274	463	4648	–1000
C275	464	4701	–1000
C276	465	4754	–1000
C277	466	4807	–1000

SYMBOL	PAD	COORDINATES	
		x	y
C278	467	4860	–1000
C279	468	4913	–1000
C280	469	4966	–1000
C281	470	5019	–1000
C282	471	5072	–1000
C283	472	5125	–1000
C284	473	5178	–1000
C285	474	5231	–1000
C286	475	5284	–1000
C287	476	5337	–1000
C288	477	5443	–1000
C289	478	5496	–1000
C290	479	5549	–1000
C291	480	5602	–1000
C292	481	5655	–1000
C293	482	5708	–1000
C294	483	5761	–1000
C295	484	5814	–1000
C296	485	5867	–1000
C297	486	5920	–1000
C298	487	5973	–1000
C299	488	6026	–1000
C300	489	6079	–1000
C301	490	6132	–1000
C302	491	6185	–1000
C303	492	6238	–1000
C304	493	6291	–1000
C305	494	6344	–1000
C306	495	6397	–1000
C307	496	6450	–1000
C308	497	6503	–1000
C309	498	6556	–1000
C310	499	6609	–1000
C311	500	6662	–1000
Alignment marks (see Fig.66)			
Alignment circle 1		–6800	–1000
Alignment circle 2		6777.5	–1000

Table 24 Bonding pad dimensions

ITEM	DIMENSIONS	UNIT
Minimum pad pitch	53	µm
Pad size; aluminium	43 × 105	µm
Bump dimensions	33 × 95 × 15 (±5)	µm
Wafer thickness (excluding bumps)	381	µm

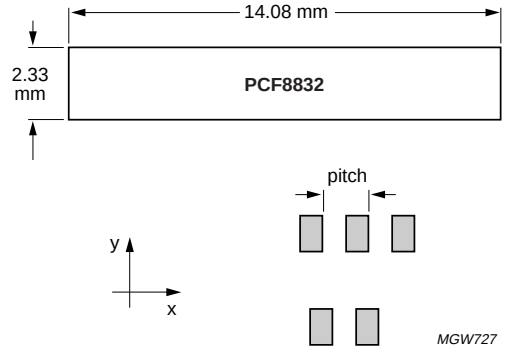


Fig.65 Bonding pad dimensions.

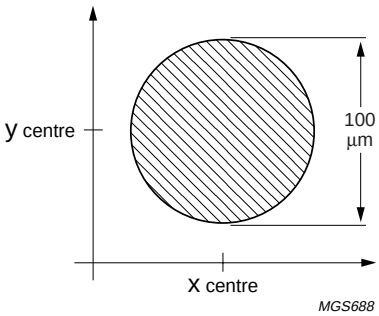
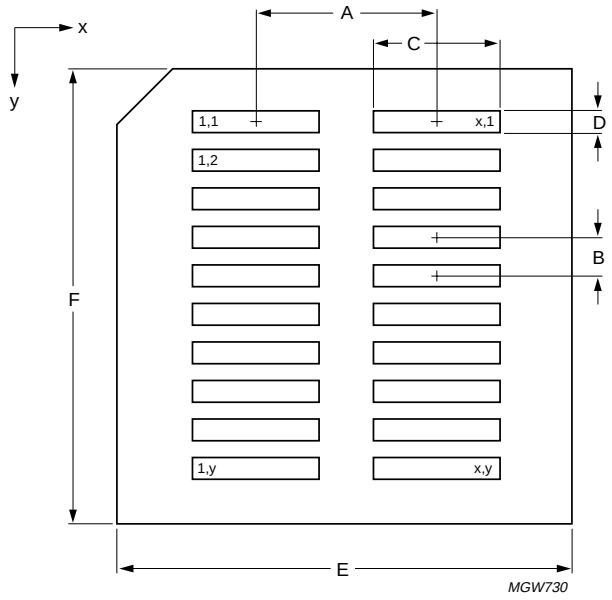


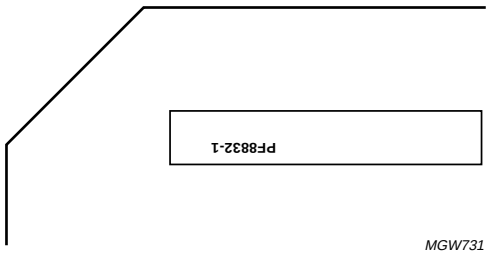
Fig.66 Alignment circle detail.

19 TRAY INFORMATION



The dimensions are given in Table 25.

Fig.67 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to Fig.64 for the orientation and position of the type name on the die surface.

Fig.68 Tray alignment.

Table 25 Tray dimensions

DIMENSION	DESCRIPTION	VALUE
A	pocket pitch x direction	20.32 mm
B	pocket pitch y direction	4.32 mm
C	pocket width x direction	14.18 mm
D	pocket width y direction	2.44 mm
E	tray width x direction	50.8 mm
F	tray width y direction	50.8 mm
–	number of pockets in x direction	2
-	number of pockets in y direction	10

20 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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