DATA SHEET

PCF8811
80 × 128 pixels matrix LCD driver

Product specification
Supersedes data of 2002 Dec 04

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Philips
Semiconductors

PHILIPS

CONTENTS

80 × 128 pixels matrix LCD driver PCF8811

1 FEATURES

- Single-chip LCD controller/driver
- 80 row and 128 column outputs
- Display data RAM 80 × 128 bits
- 128 icons (row 80 can be used for icons in extended command set and when icon rows are enabled)
- An 8-bit parallel interface, 3 or 4-line Serial Peripheral Interface (SPI) and high-speed I²C-bus
- On-chip:
  - Configurable voltage multiplier generating V_{LCD}; external V_{LCD} also possible
  - Linear temperature compensation of V_{LCD}; 8 programmable temperature coefficients (extended command set); one fixed temperature coefficient which default can be set by OTP programming (basic command set)
  - Generation of intermediate LCD bias voltage
  - Oscillator requires no external components; external clock input also possible.
- OTP calibration for V_{LCD} and accurate frame frequency
- External reset input pin
- CMOS compatible inputs
- Mux rate: 1 : 16 to 1 : 80 in steps of 8 when no icon row is used, with the icon row steps of 16 can be used
- Logic supply voltage range $V_{DD1} - V_{SS}$:
  - 1.7 V to 3.3 V.
- High voltage generator supply voltage range V_{DD2},$V_{DD3} - V_{SS}$:
  - 1.8 V to 3.3 V.
- Display supply voltage range $V_{LCD} - V_{SS}$:
  - 3 V to 9 V.
- Low power consumption; suitable for battery operated systems
- Programmable bottom row pads mirroring; for compatibility with both Tape Carrier Packages (TCP) and Chip On Glass (COG) applications (extended command set)
- Status read which allows for chip recognition and content checking of some registers
- Start address line which allows, for instance, the scrolling of the displayed image
- Programmable display RAM pointers for variable display sizes
- Slim chip layout, suited for COG applications
- Temperature range: T_{amb} = –40 °C to +85 °C.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

3 GENERAL DESCRIPTION

The PCF8811 is a low power CMOS LCD controller driver, designed to drive a graphic display of 80 rows and 128 columns or a graphic display of 79 rows and 128 columns and a icon row of 128 symbols. All necessary functions for the display are provided in a single chip, including on-chip generation of the LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The PCF8811 can interface to microcontrollers via a parallel bus, serial bus or I²C-bus interface.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8811U/2DA/1	–	chip with bumps in tray, not covered under Philips/Motif license agreement	–
PCF8811MU/2DA/1	–	chip with bumps in tray, sold under license from Motif	–

5 BLOCK DIAGRAM

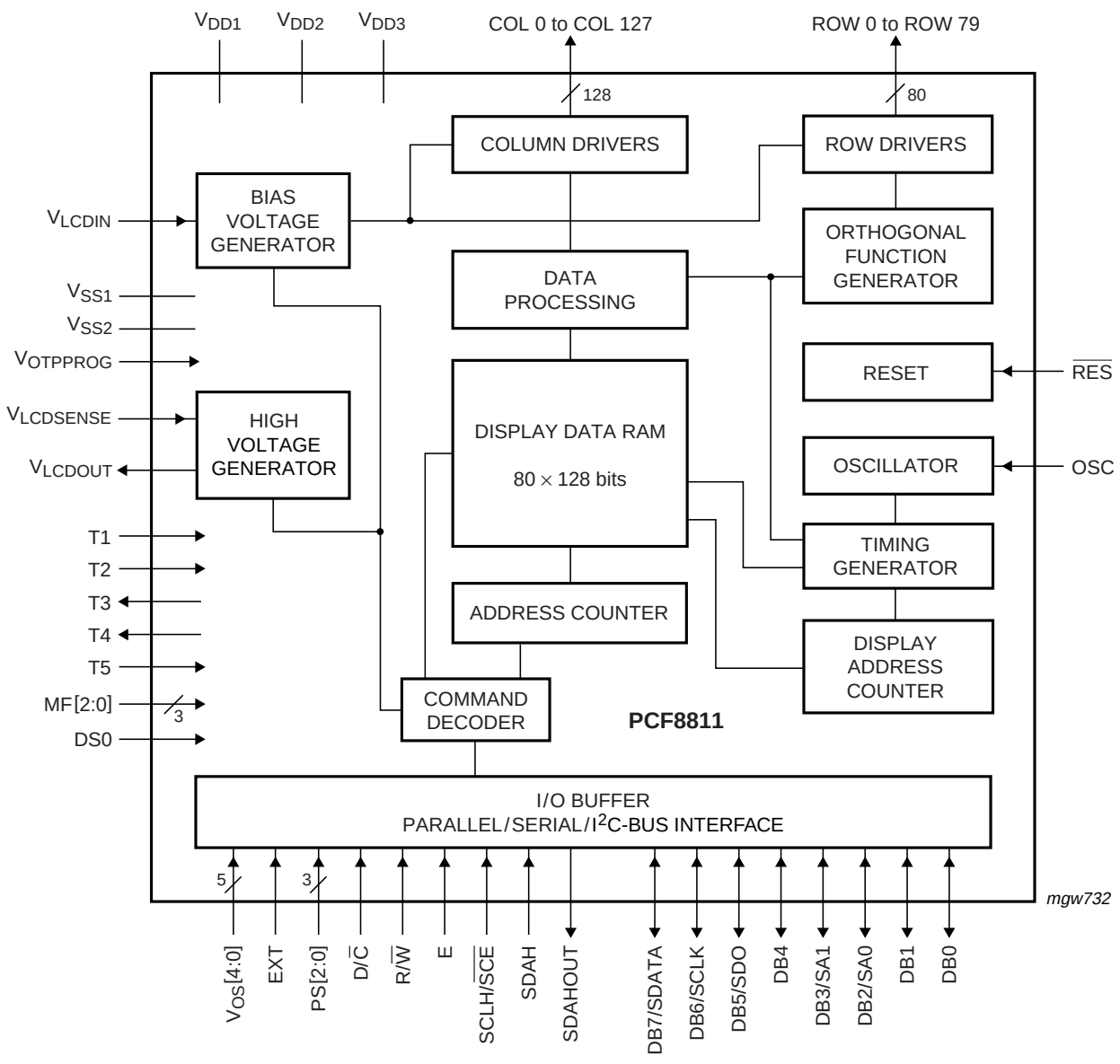


Fig.1 Block diagram.

6 PINNING

SYMBOL	PAD	DESCRIPTION
MF2	9	manufacturer device ID input
MF1	10	manufacturer device ID input
MF0	11	manufacturer device ID input
DS0	12	device recognition input
OSC	13	oscillator input
EXT	14	extended command set input
PS0	15	parallel/serial/I^2C-bus data selection input
PS1	16	parallel/serial/I^2C-bus data selection input
PS2	17	parallel/serial/I^2C-bus data selection input
$V_{SS(tie\ off)}$	18	
SDAHOUT	19	I^2C-bus data output
SDAH	20 and 21	I^2C-bus data input
SCLH/$\overline{SCE}$	22 and 23	I^2C-bus clock input/$\overline{chip\ enable}$ (6800 interface)
$V_{OTPPROG}$	24 to 26	supply voltage for OTP programming (can be combined with SCLH/$\overline{SCE}$)
$\overline{RES}$	27	external reset input
D/$\overline{C}$	28	data/$\overline{command}$ input
R/$\overline{W}$	29	read/$\overline{write}$ (6800 interface) input
E	30	clock enable (6800 interface) input
$V_{DD(tie\ off)}$	31	
DB0	32	parallel data input/output
DB1	33	parallel data input/output
DB2/SA0	34	parallel data input/output or I^2C-bus slave address input
DB3/SA1	35	parallel data input/output or I^2C-bus slave address input
DB4	36	parallel data input/output
DB5/SDO	37	parallel data input/output or serial data output
DB6/SCLK	38	parallel data input/output or serial clock input
DB7/SDATA	39	parallel data input/output or serial data input
V_{DD1}	40 to 45	general supply voltage
V_{DD2}	46 to 55	supply voltage for the internal voltage generator
V_{DD3}	56 to 60	supply voltage for the internal voltage generator
V_{SS1}	61 to 70	ground
V_{SS2}	71 to 80	ground
T5	81	test input 5
T2	82	test input 2
T1	83	test input 1
T4	84	test output 4
T3	85	test output 3
V_{OS4}	86	V_{LCD} offset input pad 4
V_{OS3}	87	V_{LCD} offset input pad 3
V_{OS2}	88	V_{LCD} offset input pad 2

SYMBOL	PAD	DESCRIPTION
V_{OS1}	89	V_{LCD} offset pad 1
V_{OS0}	90	V_{LCD} offset pad 0
V_{LCDOUT}	91 to 99	voltage multiplier output
$V_{LCDSENSE}$	100	voltage multiplier regulation input
V_{LCDIN}	101 to 107	LCD supply voltage
ROW 79 to ROW 40	115 to 154	LCD row driver outputs; ROW 79 is the icon row when the icon row is enabled
ROW 80	155	duplicate of ROW 79
COL 0 to COL 127	156 to 283	LCD column driver outputs
ROW 0 to ROW 39	284 to 323	LCD row driver outputs
	1, 3 to 8, 109 to 114, 324 to 333	dummy pads
	2 and 108	alignment marks

7 PIN FUNCTIONS

7.1 ROW 0 to ROW 79: row driver outputs

These pads output the display row signals.

7.2 COL 0 to COL 127: column driver outputs

These pads output the display column signals.

7.3 V_{SS1} and V_{SS2}: negative power supply rails

The 2 supply rails must be connected together.

7.4 V_{DD1} to V_{DD3}: positive power supply rails

V_{DD2} and V_{DD3} are the supply voltage for the internal voltage generator. Both have the same voltage and may be connected together outside of the chip. V_{DD1} is used as supply for the rest of the chip. V_{DD1} can be connected together with V_{DD2}, V_{DD3} but in this case care must be taken to respect the supply voltage range; see Chapter 16.

If the internal voltage generator is not used then pins V_{DD2} and V_{DD3} must be connected to V_{DD1}.

7.5 $V_{OTPPROG}$: OTP programming power supply

Supply voltage for the OTP programming; see Chapter 22. V_{OTPROG} can be combined with the SCLH/$\overline{SCE}$ pin in order to reduce the external connections.

7.6 V_{LCDOUT}, V_{LCDIN} and $V_{LCDSENSE}$: LCD power supply

Positive power supply for the liquid crystal display. If the internal V_{LCD} generator is used, then all three inputs must be connected together. If not (V_{LCD} generator is disabled and an external voltage is supplied to V_{LCDIN}), then V_{LCDOUT} must be left open-circuit, $V_{LCDSENSE}$ must be connected to V_{LCDIN}, V_{DD2} and V_{DD3} should be applied according to the specified voltage range. An external LCD supply voltage can be supplied using the V_{LCDIN} pad. In this case, V_{LCDOUT} should not be connected to V_{LCDIN}, and the internal voltage generator must be switched off. If the PCF8811 is in power-save mode, the external LCD supply voltage can be switched off.

7.7 T1 to T5: test pads

T1, T2 and T5 must be connected to V_{SS}, T3 and T4 must be left open-circuit. Not accessible to user.

7.8 MF2 to MF0

Manufacturer device ID pads. (manufacturer ID 100 = Philips).

7.9 DS0

Device recognition pad; see Table 10.

7.10 V_{OS4} to V_{OS0}

These 5 input pins enable the calibration of the programmed V_{LCD} (can be connected on the module to V_{DD1} or V_{SS1}).

7.11 EXT: extended command set

Input to select the basic command set or the extended command set. Must be connected on the module to have only one command set enabled.

Table 1 Command set

PIN	LEVEL	DESCRIPTION
EXT	LOW	basis command set
	HIGH	extended command set

Note: Philips strongly recommends that the extended command set be used.

7.12 PS0, PS1 and PS2

Parallel/serial/I²C-bus interface selection.

Table 2 Interface selection

PS[2:0]	INTERFACE
000	3-line SPI
001	4-line SPI
010	no operation
011	6800 parallel interface
100 or 110	high-speed I²C-bus interface
101 or 111	3-line serial interface

7.13 D/$\overline{C}$

Input to select either $\overline{\text{command}}$/data or data input. Not used in the 3-line serial interface, 3-line SPI and I²C-bus interface and must be connected to V_{DD1} or V_{SS1}.

7.14 R/$\overline{W}$

Input to select read or write mode when the 6800 parallel interface is selected. Not used in the serial and I²C-bus mode and must be connected to V_{DD1} or V_{SS1}.

7.15 E

E is the clock enable input for the 6800 parallel bus. Not used in the serial or I²C-bus interface and must be connected to V_{DD1} or V_{SS1}.

7.16 SCLH/$\overline{SCE}$

Input to select the chip and so allowing data/$\overline{\text{commands}}$ to be clocked in or serial clock input when the I²C-bus interface is selected.

7.17 SDAH

I²C-bus serial data input. When not used it must be connected to V_{DD1} and V_{SS1}.

7.18 SDAHOUT

SDAHOUT is the serial data acknowledge output for the I²C-bus interface. By connecting SDAHOUT to SDAH externally, the SDAH line becomes fully I²C-bus compatible. Having the acknowledge output separated from the serial data line is advantageous in COG applications. In COG applications where the track resistance from the SDAHOUT pad to the system SDAH line can be significant, a potential divider is generated by the bus pull-up resistor and the ITO track resistance. It is possible that during the acknowledge cycle the PCF8811 will not be able to create a valid logic 0 level. By splitting the SDAH input from the SDAHOUT output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDAHOUT pad to the system SDAH line to guarantee a valid low level. When not used it must be connected to V_{DD1} or V_{SS1}.

7.19 DB7 to DB0

These input/output lines are used by the several interfaces as described below. When not used in the serial interface or the I²C-bus interface it must be connected to V_{DD1} or V_{SS1}.

7.19.1 DB7 TO DB0 (PARALLEL INTERFACE)

8-bit bidirectional bus. DB7 is the MSB.

7.19.2 DB7, DB6 AND DB5 (SERIAL INTERFACE)

DB7 is used for serial input data (SDATA) when the serial interface is selected. DB6 (SCLK) is used for the serial input clock when the serial interface is selected. DB5 is used as the serial output of the serial interface (SDO).

7.19.3 DB3 AND DB2 (I²C-BUS INTERFACE)

DB3 and DB2 are respectively the SA1 and SA0 inputs when the I²C-bus interface is selected and can be used so that up to four PCF8811s can be distinguished on one I²C-bus interface.

7.20 OSC: oscillator

When the on-chip oscillator is used this input must be connected to V_{DD1}. An external clock signal, if used, is connected to this input. If the oscillator and external clock are both inhibited by connecting the OSC pin to V_{SS1}, the display is not clocked and may be left in a DC state. To avoid this the chip should always be put into Power-down mode before stopping the clock.

7.21 $\overline{RES}$: reset

This signal will reset the device and must be applied to properly initialize the chip. The signal is active LOW.

8 BLOCK DIAGRAM FUNCTIONS

8.1 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to V_{DD1}. An external clock signal, if used, is connected to this input.

8.2 Address Counter (AC)

The address counter assigns addresses to the display data RAM for writing. The X address X[6:0] and the Y address Y[3:0] are set separately.

8.3 Display Data RAM (DDRAM)

The PCF8811 contains an 80 × 128-bit static RAM which stores the display data. The RAM is divided into 10 banks of 128 bytes (10 × 8 × 128 bits). The icon row when enabled is always ROW 79 and therefore located in bank 9. During RAM access, data is transferred to the RAM via the parallel, serial interface or I^2C-bus interface. There is a direct correspondence between the X address and the column output number.

8.4 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not affected by operations on the data bus.

8.5 Display address counter

The display is generated by simultaneously reading out the RAM content for 2, 4 or 8 rows depending on the selected current display size. This content will be processed with the corresponding set of 2, 4 or 8 orthogonal functions and so generating the signals for switching the pixels in the display on or off according to the RAM content. The possibility exists to set the p value for the display sizes 64 and 80 manually to p = 4.

The display status (all dots on/off and normal/inverse video) is set by the bits DON, DAL and E in the command display control; see Table 6.

8.6 LCD row and column drivers

The PCF8811 contains 80 row and 128 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed.

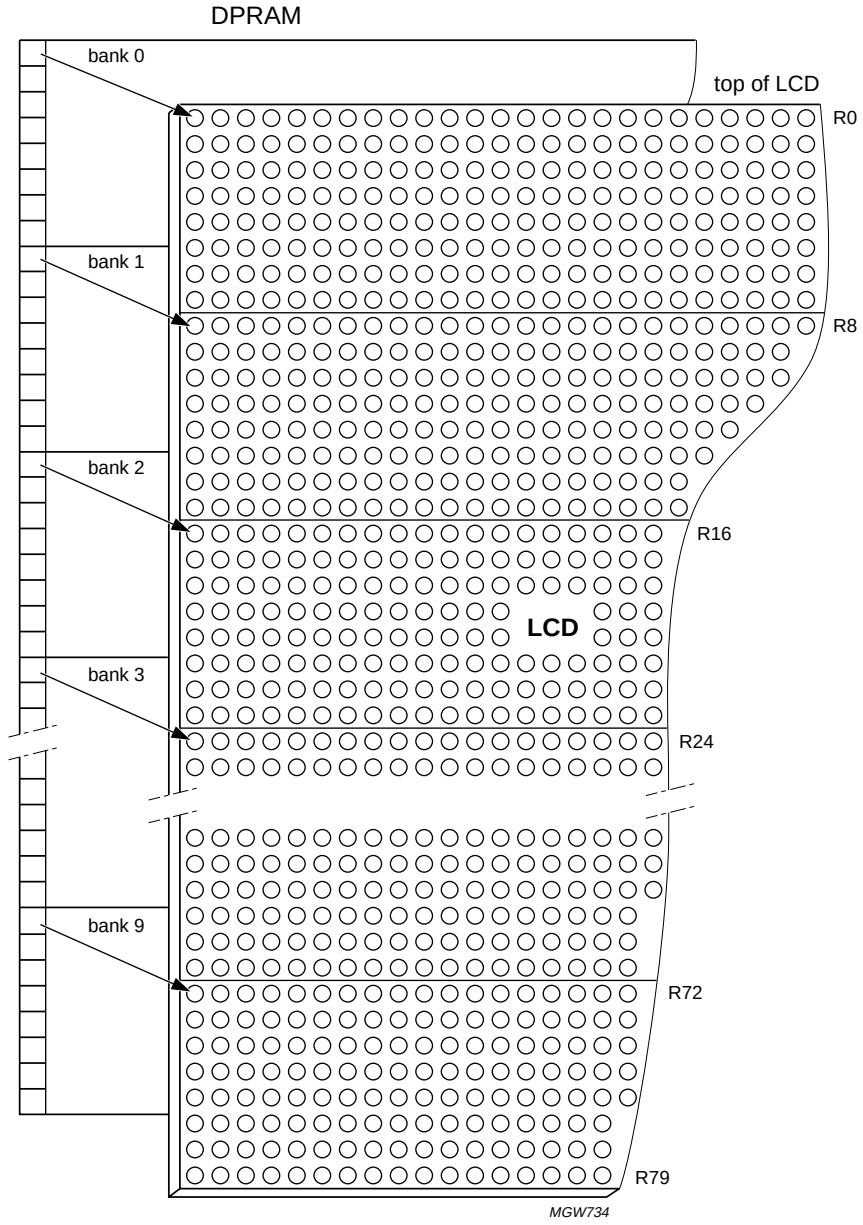


Fig.2 DDRAM to display mapping.

9 ADDRESSING

Data is downloaded in bytes into the RAM matrix of the PCF8811 as indicated in Fig.2. The display RAM has a matrix of 80 by 128 bits. The columns are addressed by the address pointer. The address ranges are: X = 0 to 127 (1111111), Y = 0 to 9 (1001). The Y address represents the bank number. The X and Y address which are effectively used can be programmed thus in order to use the PCF8811 with different display sizes without additional loading of the microprocessor. Addresses outside these ranges are not allowed. The icon row when enabled is always ROW 79 and therefore located in bank 9.

9.1 Display data RAM structure

The mode for storing data into the data RAM is dependent on the selected command set.

9.1.1 BASIC COMMAND SET

After a write operation the column address counter (X address) auto-increments by one, and wraps to zero after the last column is written. The number of columns (X address) after which the wrap around must occur can be programmed. The Y address counter does not auto-increment in the basic command set, the counter stops when a complete bank has been written to. In this case the Y address counter must be set (Y address see Table 5) to write the next bank (see Fig.3). When only a part of the RAM is used both X (X max) and Y (Y max) addresses can be set.

The data order in the basic command set is as defined in Fig.3.

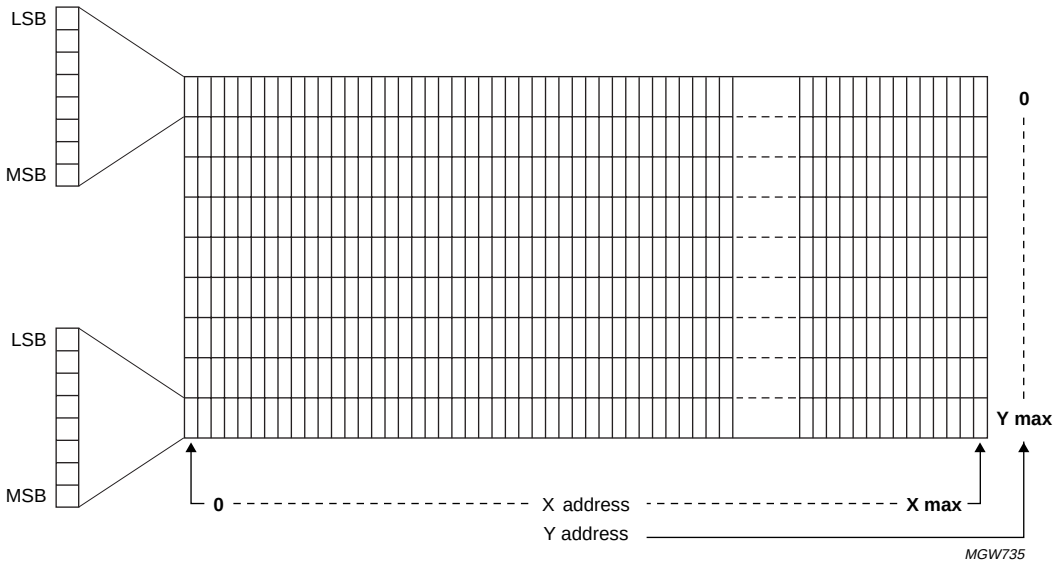


Fig.3 Sequence of writing data bytes into the RAM (basic command set).

9.1.2 EXTENDED COMMAND SET

9.1.2.1 Horizontal/vertical addressing

Two different addressing modes are possible with the extended command set: horizontal addressing mode and vertical addressing mode.

In the horizontal addressing mode (V = 0) the X address increments after each byte. After the last X address, X wraps around to 0 and Y increments to address the next row (see Fig.4). The number of columns (last X address) after which the wrap around must occur can be programmed. In Fig.4 it can be seen that the X address is programmed to be 127, and the Y address is programmed to be 9. With X max and Y max the X and Y addresses can be programmed while the whole RAM is not being used.

In the vertical addressing mode (V = 1) the Y address increments after each byte. After the last Y address (Y = 9), Y wraps around to 0 and X increments to address the next column (see Fig.5). The last Y address after which Y wraps to 0 can be programmed. In Fig.5 it can be seen that the X address is programmed to be 127, and the Y address is programmed to be 9. With X max and Y max the X and Y addresses can be programmed while the whole RAM is not being used.

After the very last address the address pointers wrap around to address X = 0 and Y = 0 in both horizontal and vertical addressing modes.

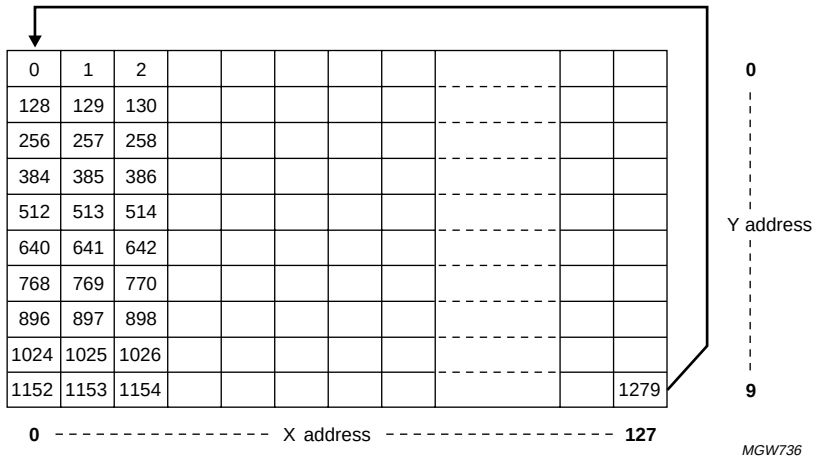


Fig.4 Sequence of writing data bytes into RAM with horizontal addressing (V = 0) (extended command set).

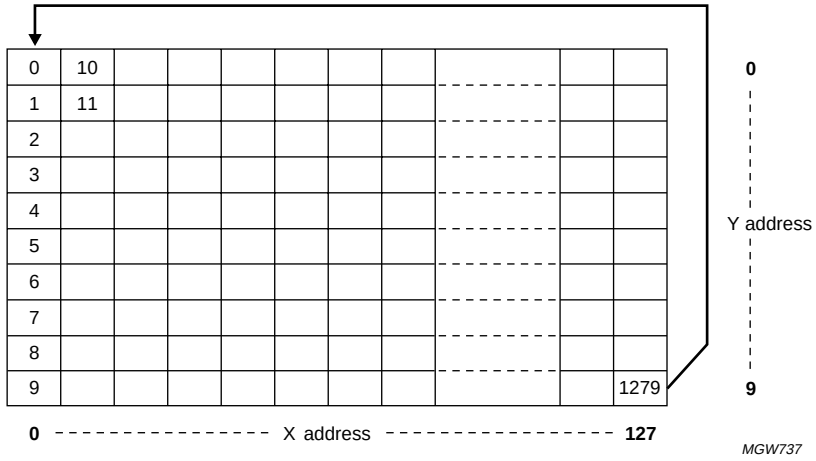


Fig.5 Sequence of writing data bytes into the RAM with vertical addressing (V = 1) (extended command set).

9.1.2.2 Data order

The data order bit (DOR) defines the bit order (LSB or MSB on top) for writing into the RAM (see Figs 6 and 7). This feature is only available in the extended command set.

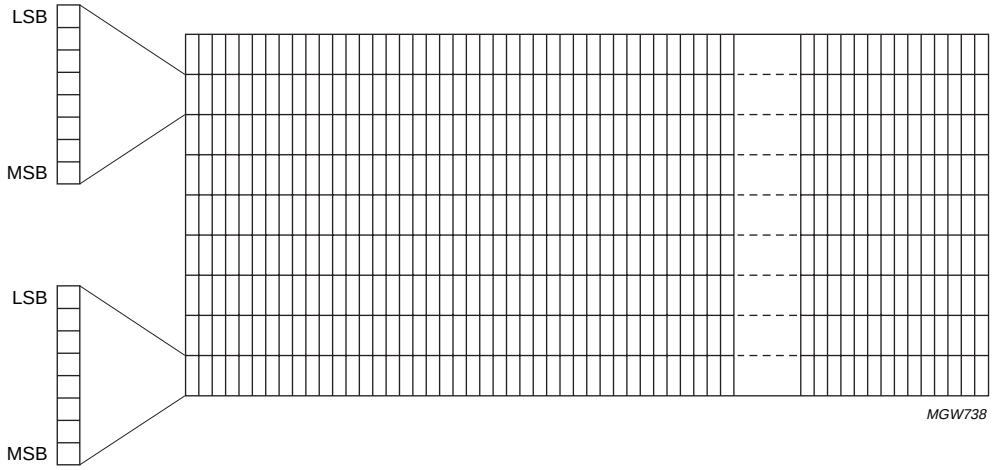


Fig.6 RAM byte organisation, if DOR = 0 (extended command set).

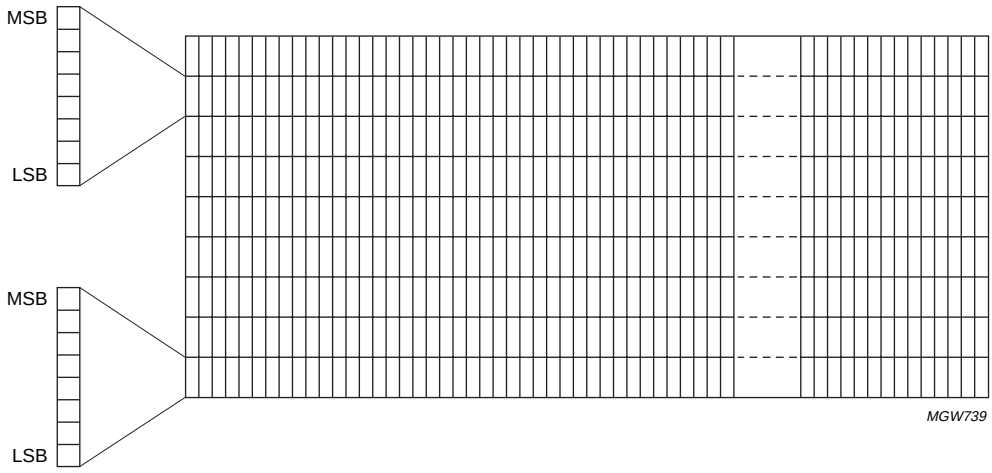


Fig.7 RAM byte organisation, if DOR = 1 (extended command set).

9.1.3 Features available in both command sets

9.1.3.1 Mirror X (MX)

The MX bit allows horizontal mirroring: when MX = 1 the X address space is mirrored; the address X = 0 is then located at the right side (X max) of the display (see Fig.8). When MX = 0 the mirroring is disabled and the address X = 0 is located at the left side (column 0) of the display (see Fig.9).

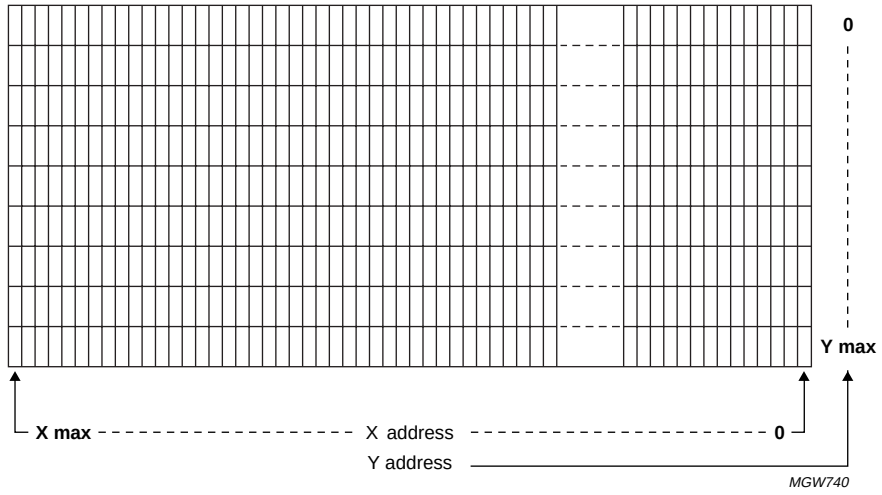


Fig.8 RAM format addressing (MX = 1) (both command sets).

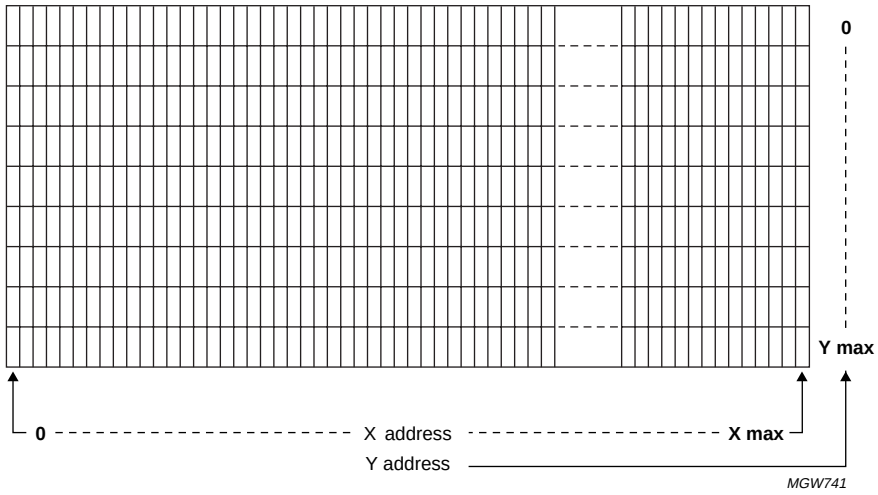


Fig.9 RAM format addressing (MX = 0) (both command sets).

9.1.3.2 Mirror Y (MY)

The MY bit allows vertical mirroring: when MY = 1 the Y address space is mirrored; the address Y = 0 is then located at the bottom of the display (see Fig.10). When MY = 0 the mirroring is disabled and the address Y = 0 is located at top of the display (see Fig.11).

The icon row, when enabled, will always be located in bank 9 and ROW 79.

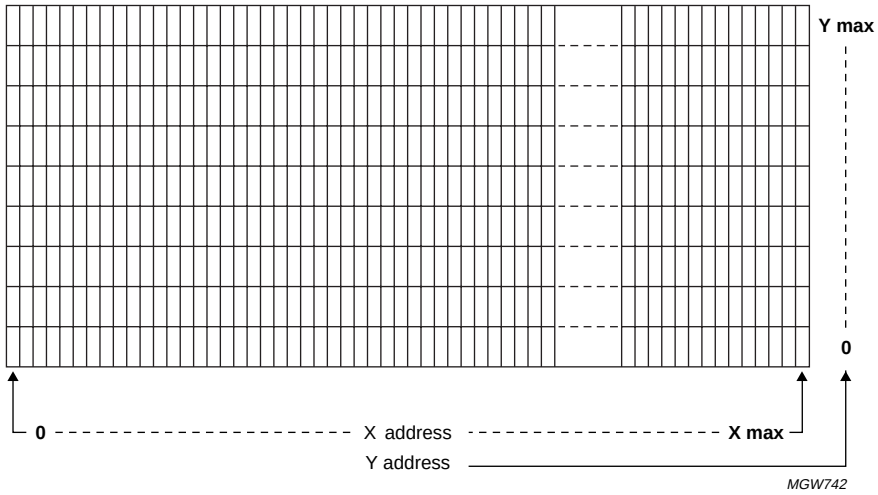


Fig.10 RAM format addressing (MY = 1) (both command sets).

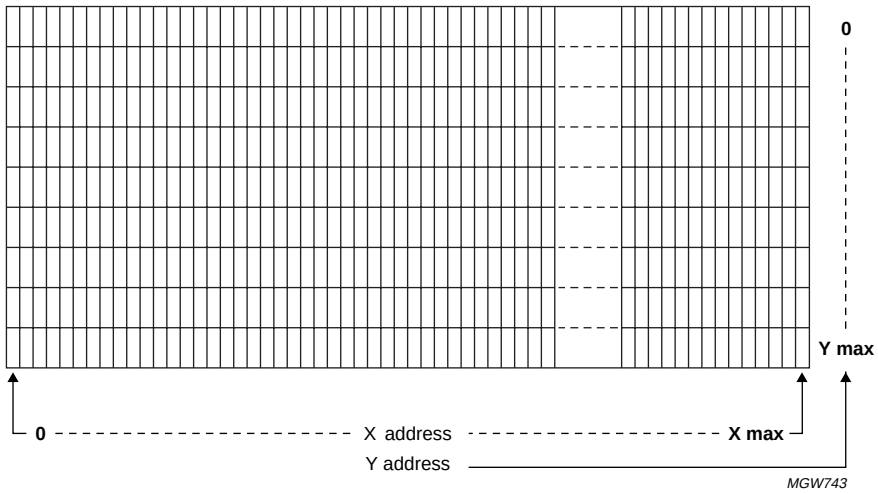


Fig.11 RAM format addressing (MY = 0) (both command sets).

10 PARALLEL INTERFACE

The parallel interfaces which can be selected is the 6800 series 8-bit bidirectional interface for communication between the microcontroller and the LCD driver chip. The selection of these interfaces is achieved with pins PS[2:0]; see Section 7.12.

10.1 6800 series parallel interface

The interface functions of the 6800 series parallel interface are given in Table 3.

Table 3 6800 series parallel interface function

D/$\overline{C}$	R/$\overline{WR}$	OPERATION
0	0	command data write
0	1	read status register
1	0	display data write
1	1	none

The parallel interface timing diagram for the 6800 series is given in Chapter 18 (see Figs 35 and 36).

The timing diagrams differ because the clock is connected (in Fig.35) to the enable (E) input. In Fig.36 the clock is connected to the chip select input ($\overline{SCE}$) and the enable input (E) is tied HIGH.

11 SERIAL INTERFACING (SPI AND SERIAL INTERFACE)

Communication with the microcontroller can also occur via a clock-synchronized Serial Peripheral Interface (SPI). It is possible to select two different 3-line (SPI and serial interface) or a 4-line serial interface. Selection is achieved via PS[2:0]; see Section 7.12.

11.1 Serial peripheral interface

The serial peripheral interface is a 3-line or 4-line interface for communication between the microcontroller and the LCD driver chip. The 3 lines are: $\overline{SCE}$ (chip enable), SCLK (serial clock) and SDATA (serial data). For the 4-line serial interface a separate D/$\overline{C}$ line is added. The PCF8811 is connected to the serial data I/O (SDA) of the microcontroller by two pins: SDATA (data input) and SDO (data output) connected together.

11.1.1 WRITE MODE

The display data/$\overline{command}$ indication may be controlled either via software or the D/$\overline{C}$ select pin. When the D/$\overline{C}$ pin is used, display data is transmitted when D/$\overline{C}$ is HIGH, and command data is transmitted when D/$\overline{C}$ is LOW (see Figs 12 and 13). When pin D/$\overline{C}$ is not used, the display data length instruction is used to indicate that a specific number of display data bytes (1 to 255) are to be transmitted (see Fig.14). The next byte after the display data string is handled as an instruction command.

When the 3-line SPI interface is used the display data/$\overline{command}$ is controlled by software.

If $\overline{SCE}$ is pulled HIGH during a serial display data stream, the interrupted byte is invalid data but all previously transmitted data is valid. The next byte received will be handled as an instruction command (see Fig.15).

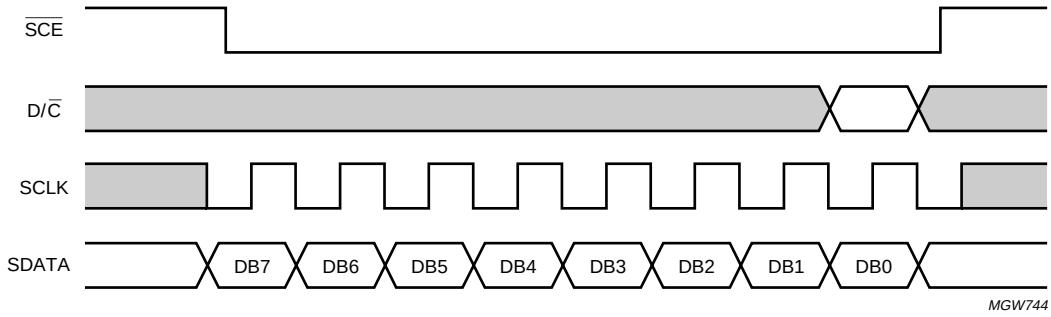


Fig.12 Serial bus protocol: transmission of one byte.

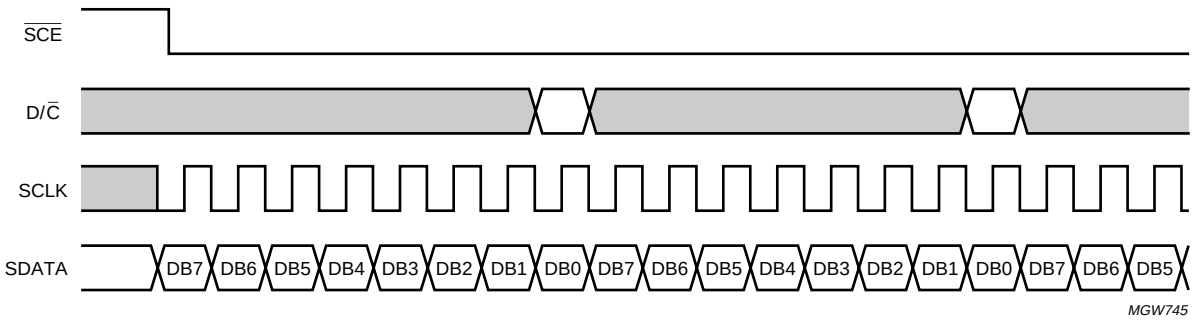


Fig.13 Serial bus protocol: transmission of several bytes.

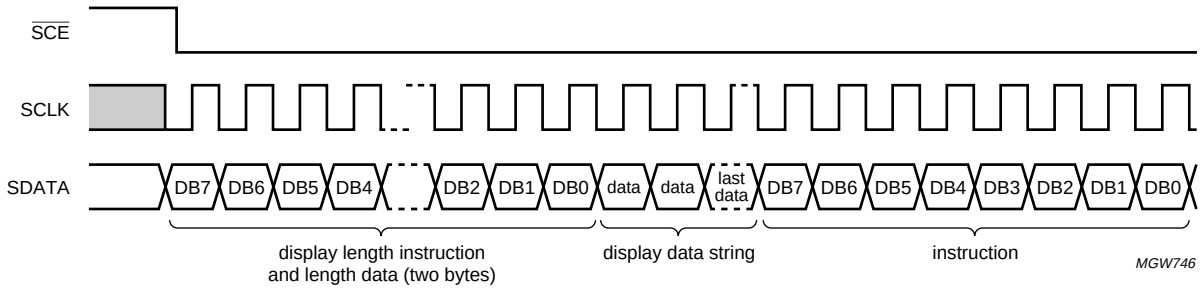


Fig.14 Transmission of several bytes.

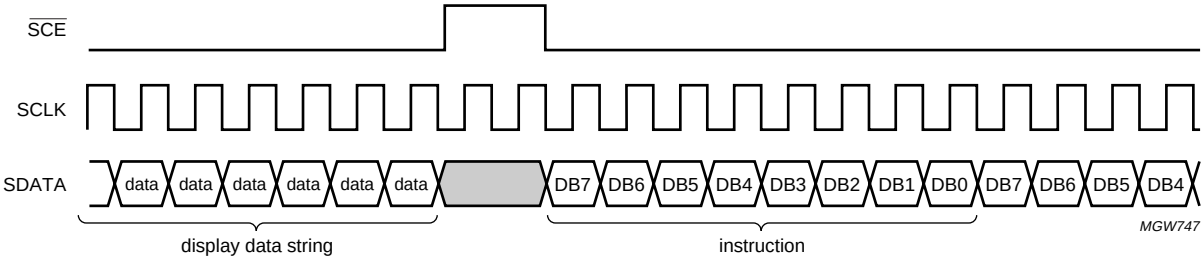


Fig.15 Transmission interrupted by $\overline{SCE}$.

11.1.2 Read mode (only extended command set)

The read mode of the interface means that the microcontroller reads data from the PCF8811. To do so the microcontroller first has to send a command (the read status command) and then the PCF8811 will respond by transmitting data on the SDO line. After that $\overline{SCE}$ is required to go HIGH (see Fig.16).

The PCF8811 samples the SDIN data on rising SCLK edges, but shifts SDO data on falling SCLK edges. Thus the microcontroller is supposed to read SDO data on rising SCLK edges.

After the read status command has been sent, the SDIN line must be set to 3-state not later then the falling SCLK edge of the last bit (see Fig.16).

The serial interface timing diagram is given in Chapter 19.

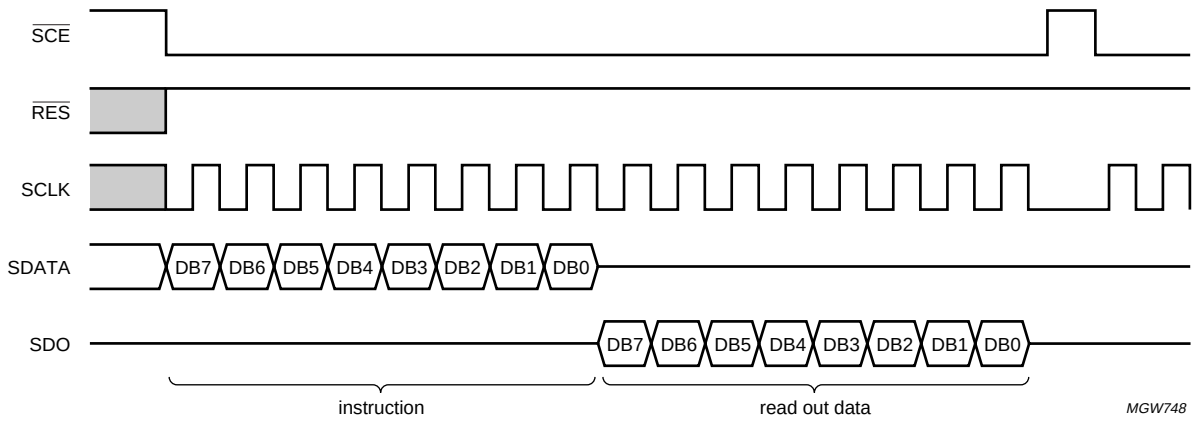


Fig.16 Read mode SPI 3-line and 4-line.

11.2 Serial interface (3-line)

The serial interface is also a 3-line bidirectional interface for communication between the microcontroller and the LCD driver chip. The 3 lines are: $\overline{SCE}$ (chip enable), SCLK (serial clock) and SDATA (serial data). The PCF8811 is connected to the SDA of the microcontroller by two pins: SDATA (data input) and SDO (data output) which are connected together.

11.2.1 WRITE MODE

The write mode of the interface means that the microcontroller writes commands and data to the PCF8811. Each data packet contains a control bit (D/$\overline{C}$) and a transmission byte. If D/$\overline{C}$ is LOW, the following byte is interpreted as a command byte. The command set is given in Table 5. If D/$\overline{C}$ is HIGH, the following byte is stored in the display data RAM. After every data byte the address counter is incremented automatically. Figure 17 shows the general format of the write mode and the definition of the transmission byte.

Any instruction can be sent in any order to the PCF8811; the MSB is transmitted first. The serial interface is initialized when $\overline{SCE}$ is HIGH. In this state, SCLK clock pulses have no effect and no power is consumed by the serial interface. A falling edge on $\overline{SCE}$ enables the serial interface and indicates the start of data transmission.

Figures 18, 19 and 20 show the protocol of the write mode:

- When $\overline{SCE}$ is HIGH, SCLK clocks are ignored; during the HIGH time of $\overline{SCE}$ the serial interface is initialized
- SCLK must be LOW on the falling $\overline{SCE}$ edge (see Fig.37)
- SDATA is sampled on the rising edge of SCLK
- D/$\overline{C}$ indicates, whether the byte is a command (D/$\overline{C}$ = 0) or RAM data (D/$\overline{C}$ = 1); it is sampled on the first rising SCLK edge
- If $\overline{SCE}$ stays LOW after the last bit of a $\overline{command}$/data byte, the serial interface receives the D/$\overline{C}$ bit of the next byte on the next rising edge of SCLK (see Fig.19)
- A reset pulse $\overline{RES}$ interrupts the transmission. The data being written into the RAM may be corrupted. The registers are cleared. If $\overline{SCE}$ is LOW after the rising edge of $\overline{RES}$, the serial interface is ready to receive the D/$\overline{C}$ bit of a $\overline{command}$/data byte (see Fig.20).

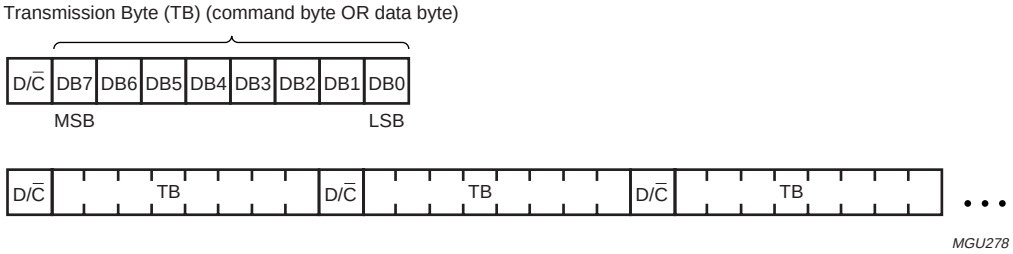


Fig.17 Serial data stream; write mode.

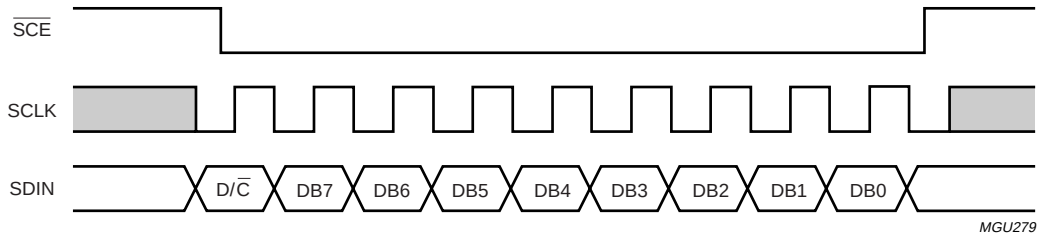


Fig.18 Write mode: a control bit followed by a transmission byte.

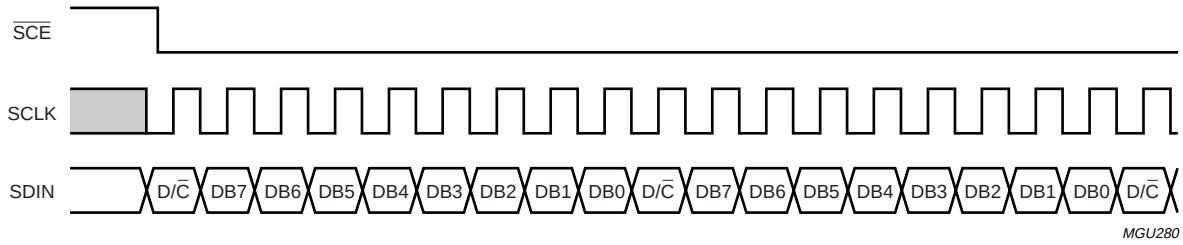


Fig.19 Write mode: transmission of several bytes.

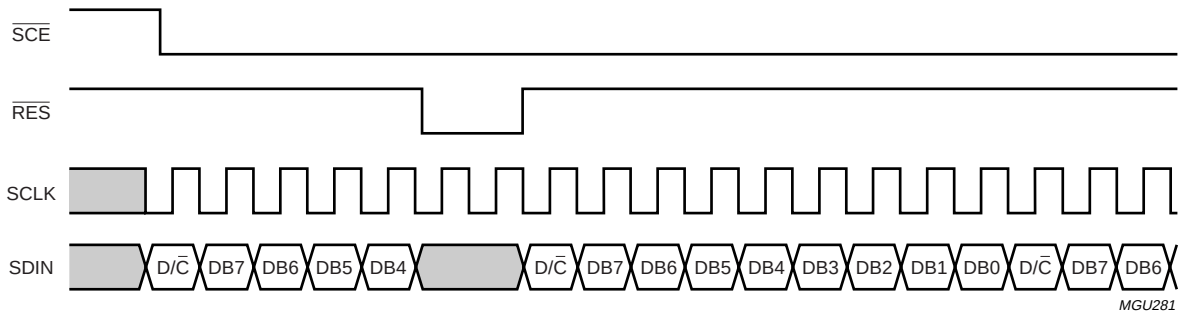


Fig.20 Write mode: interrupted by reset ($\overline{RES}$).

11.2.2 Read mode (only extended command set)

The read mode of the interface means that the microcontroller reads data from the PCF8811. To do so the microcontroller first has to send a command (the read status command) and then the following byte is transmitted in the opposite direction (using SDO) (see Fig.21). After that, $\overline{SCE}$ is required to go HIGH before a new command is sent.

The PCF8811 samples the SDATA data on the rising SCLK edges, but shifts SDO data on the falling SCLK edges. Thus the microcontroller is supposed to read SDO data on rising SCLK edges.

After the read status command has been sent, the SDATA line must be set to 3-state not later then the falling SCLK edge of the last bit (see Fig.21).

The 8th read bit is shorter than the others because it is terminated by the rising SCLK edge (see Fig.40). The last rising SCLK edge sets SDO to 3-state after the delay time t4.

The serial interface timing diagram is given in Chapter 19.

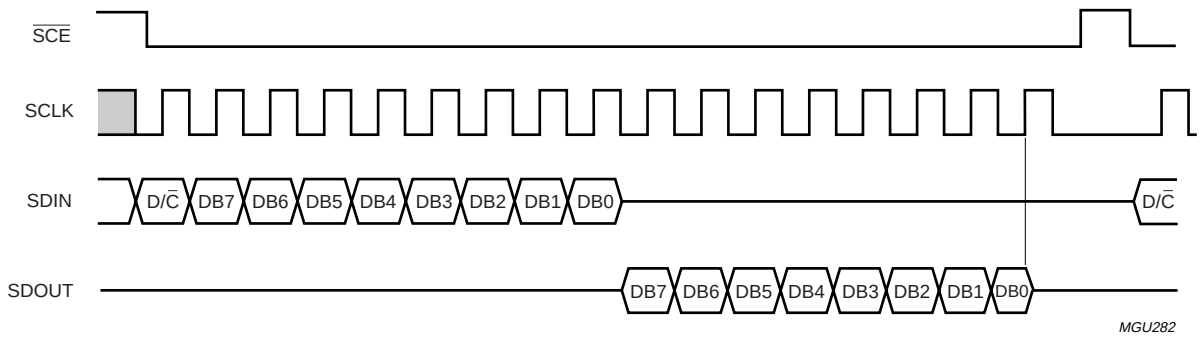


Fig.21 Read mode serial interface 3-line.

12 I²C-BUS INTERFACE

12.1 Characteristics of the I²C-bus (Hs-mode)

The I²C-bus Hs-mode is for bidirectional, two-line communication between different ICs or modules with speeds of up to 3.4 MHz. The only difference between Hs-mode slave devices and F/S-mode slave devices is the speed at which they operate, therefore the buffers on the SCLH and SDAH have open-drain outputs. This is the same for I²C-bus master devices which have an open-drain SDAH output and a combination of an open-drain, pull-down and current source pull-up circuits on the SCLH output. Only the current source of one master is enabled at any one time, and only during Hs-mode. Both lines must be connected to a positive supply via a pull-up resistor.

Data transfer may be initiated only when the bus is not busy.

12.1.1 System configuration

The system configuration is illustrated in Fig.22.

Definitions of the I²C-bus terminology:

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

12.1.2 Bit transfer

One data bit is transferred during each clock pulse (see Fig.23). The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

12.1.3 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S).
A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.24.

12.1.4 Acknowledge

Each byte of eight bits is followed by an acknowledge bit; see Fig.25. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge-related clock pulse.
A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

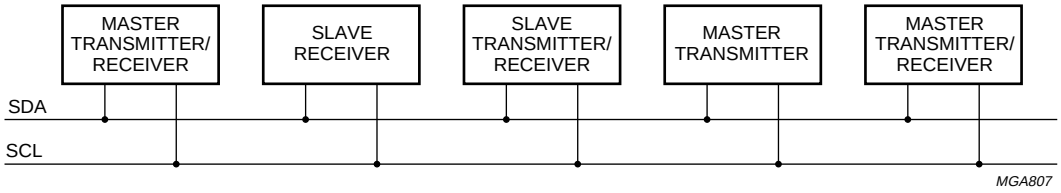


Fig.22 System configuration.

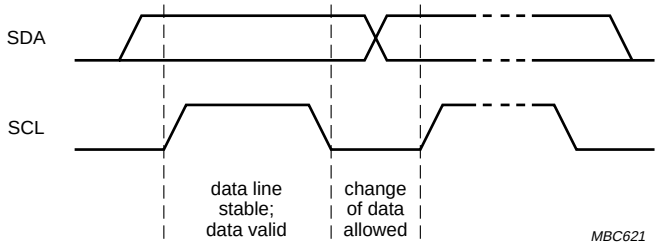


Fig.23 Bit transfer.

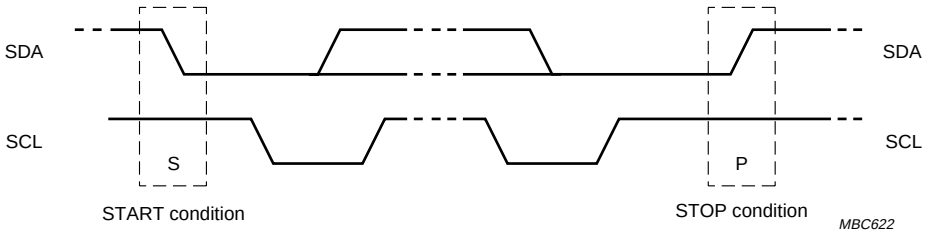


Fig.24 Definition of START and STOP conditions.

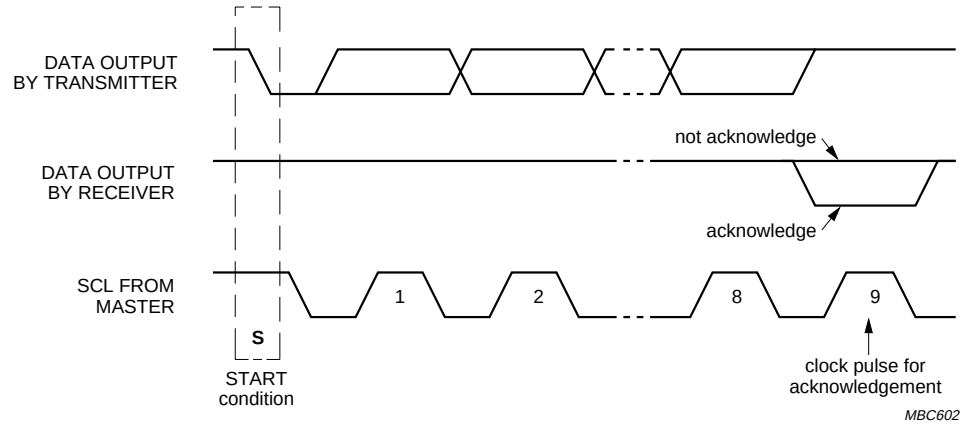


Fig.25 Acknowledge on the I²C-bus.

12.2 I²C-bus Hs-mode protocol

The PCF8811 is a slave receiver/transmitter. If data is to be read from the device, the SDAH pin must be connected, otherwise SDAH may be unused.

Hs-mode can only commence after the following conditions:

- START condition (S)
- 8-bit master code (00001XXX)
- Not-acknowledge bit ($\overline{A}$).

The master code has two functions: it allows arbitration and synchronization between competing masters at F/S-mode speeds, resulting in one winner. The master code also indicates the beginning of an Hs-mode transfer. These conditions are illustrated in Figs 26 and 27.

As no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge ($\overline{A}$). After this $\overline{A}$ bit, and the SCLH line has been pulled up to a HIGH level, the active master switches to Hs-mode and enables at t_H the current-source pull-up circuit for the SCLH signal (see Fig.27).

The active master will then send a repeated START condition (Sr) followed by a 7-bit slave address with a R/$\overline{W}$ bit, and receives an acknowledge bit (A) from the selected slave.

After each acknowledge bit (A) or not-acknowledge bit ($\overline{A}$) the active master disables its current source pull-up circuit. The active master re-enables its current source again when all devices have been released and the SCLH signal reaches a HIGH level. The rising of the SCLH signal is done by a pull-up resistor and therefore is slower, the last part of the SCLH rise time is speeded up because the current source is enabled. Data transfer only switches back to F/S mode after a STOP condition (P).

A write sequence after the Hs-mode is selected is illustrated in Fig.28. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, the remainder will ignore the I²C-bus transfer.

After the acknowledgement cycle of a write ($\overline{W}$), one or more command words will follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and D/$\overline{C}$, plus a data byte (see Fig.28 and Table 4).

The last control byte is tagged with a cleared MSB, the continuation bit Co. The control and data bytes are also acknowledged by all addressed slaves on the bus.

Table 4 Co and D/$\overline{C}$ definition

BIT	LOGIC LEVEL	R/$\overline{W}$	ACTION
Co	0	N/A	last control byte to be sent; only a stream of data bytes are allowed to follow; this stream may only be terminated by a STOP or RE-START condition
	1		another control byte will follow the data byte unless a STOP or RE-START condition is received
D/$\overline{C}$	0	0	data byte will be decoded and used to set-up the device
		1	data byte will return the status byte
	1	0	data byte will be stored in the display RAM
		1	RAM read back is not supported

A read sequence is given in Fig.29 and again this sequence follows after the Hs-mode is selected. The PCF8811 will immediately start to output the requested data until a not-acknowledge is transmitted by the master. Before the read access, the user has to set the D/$\overline{C}$ bit to the appropriate value by a preceding write access. The write access should be terminated by a RE-START condition so that the Hs-mode is not disabled.

After the last control byte, depending on the D/$\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the D/$\overline{C}$ bit was set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer.

The data pointer is automatically updated and the data is directed to the intended PCF8811 device. If the D/$\overline{C}$ bit of the last control byte was set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed PCF8811. At the end of the transmission the I^2C-bus master issues a STOP condition (P) and switches back to the F/S-mode, however, to reduce the overhead of the master code, it is possible that a master can link a number of Hs-mode transfers, separated by repeated START conditions (Sr).

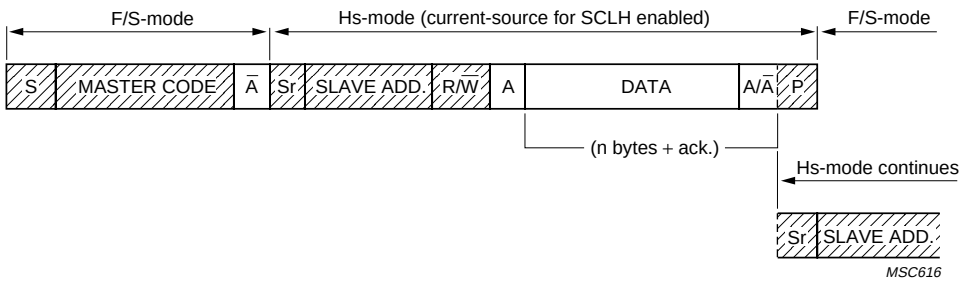


Fig.26 Data transfer format in Hs-mode.

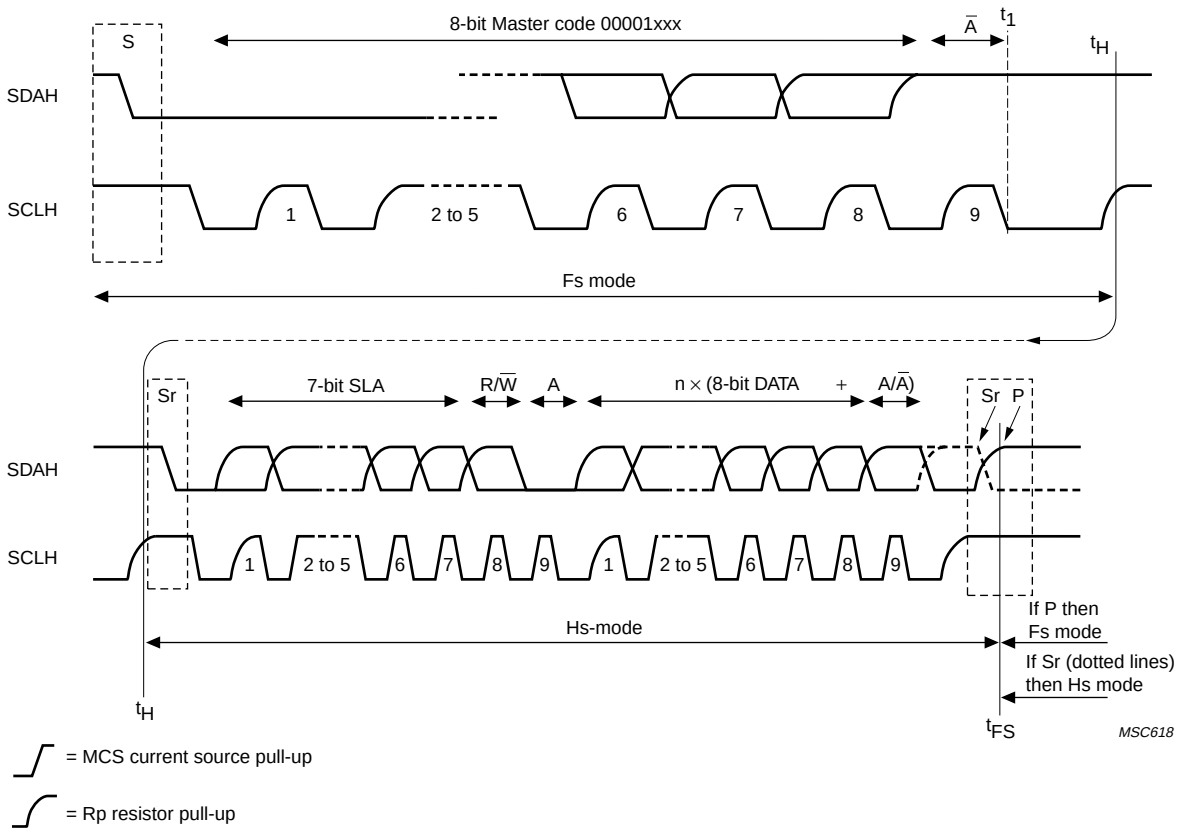


Fig.27 Data transfer timing format in Hs-mode.

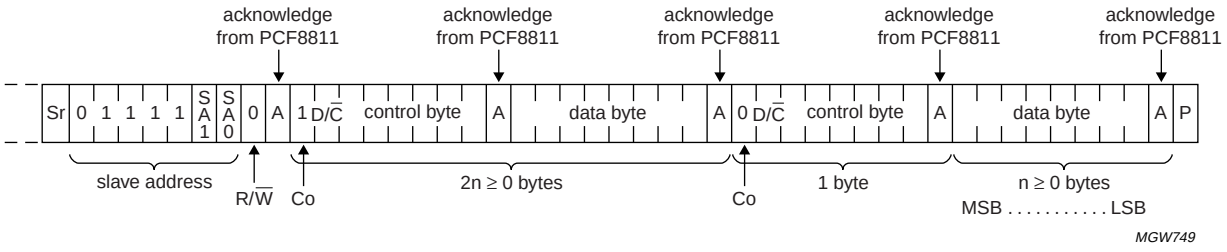


Fig.28 Master transmits in Hs-mode to slave receiver; write mode.

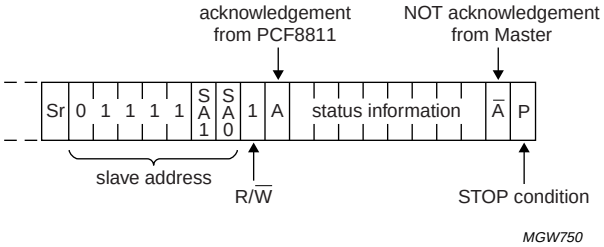


Fig.29 Master receives from slave transmitter (status register is read); read mode.

12.3 Command decoder

The command decoder identifies command words that are received on the I²C-bus:

- Pairs of bytes: information in 2nd byte, first byte determines whether information is display or instruction data
- Stream of information bytes after Co = 0: display or instruction data depending on last D/$\overline{C}$.

The most significant bit of a control byte is the continuation bit Co. If this bit is at logic 1, it indicates that only one data byte, either command or RAM data, will follow. If this bit is at logic 0, it indicates that a series of data bytes, either command or RAM data, may follow. The DB6 bit of a control byte is the RAM data/$\overline{\text{command}}$ bit D/$\overline{C}$. When this bit is at logic 1, it indicates that a RAM data byte will be transferred next. If the bit is at logic 0, it indicates that a command byte will be transferred next.

13 INSTRUCTIONS

The PCF8811 interfaces via an 8-bit parallel interface, two different 3-line serial interfaces, a 4-wire serial interface or an I²C-bus interface. Processing of the instructions does not require the display clock.

Data accesses to the PCF8811 can be broken down into two areas; those that define the operating mode of the device, and those that fill the display RAM.

In the case of the parallel and 4-wire SPI interfaces, the distinction is the D/$\overline{C}$ pin. When the D/$\overline{C}$ pin is at logic 0, the chip will respond to instructions as defined in Table 5. When the D/$\overline{C}$ bit is at logic 1, the chip will send data to the RAM.

When the 3-wire SPI, the 3-wire serial interface or the I²C-bus interface is used, the distinction between instructions which define the operating mode of the device and those that fill the display RAM, is made respectively by the display data length instruction (3-line SPI) or by the D/$\overline{C}$ bit in the data stream (3-line serial interface and I²C-bus interface).

There are 4 types of instructions. Those which:

1. Define the PCF8811 functions, such as display configuration etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently.

A basic and an extended instruction set is available: if the EXT pin is set LOW the basic command set is used. If the EXT pin is set HIGH the extended command set is used.

Both command sets are detailed in Table 5.

Table 5 Instruction set; note 1

INSTRUCTION	EXT[2]	D/$\overline{C}$	R/$\overline{W}$	COMMAND BYTE								DESCRIPTION
				D7[3]	D6	D5	D4	D3	D2	D1	D0	
NOP	X	0	0	0	1	0	0	1	1	X	X	no operation
NOP	X	0	0	1	1	1	0	0	1	0	0	no operation
Reset	X	0	0	1	1	1	0	0	0	1	0	soft reset
Write data	X	1	0	D7	D6	D5	D4	D3	D2	D1	D0	write data to display RAM
Display data length	X X	0 0	0 0	1 D7	1 D6	1 D5	0 D4	1 D3	0 D2	0 D1	0 D0	only used in 3-line SPI
Status read	X	0	1	BUSY	DON	$\overline{RES}$	MF2	MF1	MF0	DS1	DS0	read status byte
	X	0	X	1	1	0	1	1	0	1	X	read status byte
Display control	X	0	0	1	0	1	0	1	1	1	DON	display on or off
	X	0	0	1	0	1	0	0	1	1	E	normal or reverse mode
	X	0	0	1	0	1	0	0	1	0	DAL	all pixels on or off
	X	0	0	1	0	1	0	0	0	0	MX	mirror X
	X	0	0	1	1	0	0	MY	X	X	X	mirror Y
	1	0	0	1	1	1	0	1	1	1	IC	icon enable or disable; note 4
	1	0	0	1	0	1	0	0	0	1	V	vertical or horizontal addressing; note 4
	1	0	0	1	1	1	0	1	0	1	DOR	data order; note 4
	1	0	0	1	1	1	0	1	1	0	BRS	bottom row swap; note 4
ADR commands	X	0	0	1	0	1	1	Y_3	Y_2	Y_1	Y_0	set Y address; 0 ≤ Y ≤ 9
	X	0	0	0	0	0	1	0	X_6	X_5	X_4	set X address; 0 ≤ X ≤ 127
	X	0	0	0	0	0	0	X_3	X_2	X_1	X_0	
	X	0 0	0 0	0 X	0 X	0 X	1 X	1 Y max3	0 Y max2	0 Y max1	1 Y max0	set Y max; 0 ≤ Y ≤ 9
	X	0	0	0 X	0 X max6	0 X max5	1 X max4	1 X max3	0 X max2	0 X max1	0 X max0	set X max; 0 ≤ X ≤ 127
Set initial display line	X X	0 0	0 0	0 X	1 L_6	0 L_5	0 L_4	0 L_3	0 L_2	X L_1	X L_0	set initial display line; 0 ≤ L ≤ 79; note 5
Set initial row	X X	0 0	0 0	0 X	1 C_6	0 C_5	0 C_4	0 C_3	1 C_2	X C_1	X C_0	set start row; 0 ≤ C ≤ 79; note 6

INSTRUCTION	EXT[2]	D/$\overline{C}$	R/$\overline{W}$	COMMAND BYTE								DESCRIPTION
				D7[3]	D6	D5	D4	D3	D2	D1	D0	
Set partial display	X X	0 0	0 0	0 X	1 P_6	0 P_5	0 P_4	1 P_3	0 P_2	X P_1	X P_0	set partial display 1 : 16 to 1 : 80
V_{OP} setting	0 0	0 0	0 0	1 X	0 X	0 V_{PR5}	0 V_{PR4}	0 V_{PR3}	0 V_{PR2}	0 V_{PR1}	1 V_{PR0}	set V_{OP}; notes 7 and 8
	0	0	0	0	0	1	0	0	V_{OFF2}	V_{OFF1}	V_{OFF0}	offset for the programming range V_{OP}; notes 7 and 8
	1 1	0 0	0 0	1 V_{PR7}	0 V_{PR6}	0 V_{PR5}	0 V_{PR4}	0 V_{PR3}	0 V_{PR2}	0 V_{PR1}	1 V_{PR0}	set V_{OP}; note 4
Power control	X	0	0	0	0	1	0	1	PC_1	PC_0	1	switch HVgen on/off
HVgen stages	0	0	0	0	1	1	0	0	1	S_1	S_0	set multiplication factor
	1	0	0	0	1	1	0	0	S_2	S_1	S_0	set multiplication factor; note 4
FR	1	0	0	0	0	0	1	1	1	FR_1	FR_0	set frame rate frequency; note 4
TC[9]	1	0	0	0	0	1	1	1	TC_2	TC_1	TC_0	set temperature coefficient; note 4
Bias system	0	0	0	0	1	0	1	0	BS_2	BS_1	BS_0	set bias system; note 10
Manual p value (p = 4)	1	0	0	0	0	0	1	1	0	1	MP	set manual p value; notes 4 and 11
Power-save on	X	0	0	1	0	1	0	1	0	0	1	power-save mode
Power-save off	X	0	0	1	1	1	0	0	0	0	1	exit power-save mode
Internal oscillator	X	0	0	1	0	1	0	1	0	1	OS	switch internal oscillator on/off
Internal oscillator	1	0	0	1	1	1	0	0	1	1	EC	enable or disable the internal or external oscillator; note 4
Enter CALMM mode	X	0	0	1	0	0	0	0	0	1	0	enter CALMM mode
Reserved	X	0	0	0	0	1	0	1	X	X	0	reserved
Reserved	X	0	0	0	1	1	1	X	X	X	X	reserved
Test	X	0	0	1	1	1	1	X	X	X	X	do not use; reserved for testing

Notes

1. X = don't care.
2. Philips strongly recommends that the extended command set be used.
3. D7 = MSB.
4. Commands only available with the extended command set, EXT = 1. If EXT = 0 these commands have no effect.
5. When icon mode is enabled the set initial display line is $0 \leq L \leq 78$.
6. When icon mode is enabled the set initial row is $0 \leq C \leq 78$.
7. Commands only used for the basic command set, EXT = 0. If EXT = 1 these commands have no effect. Care should be taken when setting V_{OP} in the basic command set, it must be followed by another command.
8. The programming of V_{OP} in the basic command set must be done in the following order:
   a) V_{PR}[5:0]
   b) V_{OFF}[2:0]
   c) Must be followed by another command.
9. One fixed TC is set automatically if the basic command set is used.
10. Bias system settings which can be received when the chip is used as replacement of Alth and Pleskho driving method (NOP).
11. Only for mux rates 1 : 64 and 1 : 80 the number of simultaneous rows can be manually set to p = 4.

13.1 Explanation of the symbols

13.1.1 COMMON INSTRUCTIONS OF THE BASIC AND EXTENDED COMMAND SET

Table 6 Explanation of the symbols

BIT	LOGIC 0	LOGIC 1	RESET STATE
DON	display off	display on	0
E	normal display	inverse video mode	0
DAL	normal display	all pixels on	0
MX	no X mirroring	X mirroring	0
MY	no Y mirroring	Y mirroring	0
OC	stop frame frequency calibration	start frame frequency calibration	0
OS	internal oscillator off	start internal oscillator	0
X[6:0]	sets X address (column) for writing in the RAM		0000000
Y[3:0]	sets Y address (bank) for writing in the RAM		0000
Xmax[6:0]	set wrap around X address (column)		1111111
Ymax[3:0]	set wrap around Y address (bank)		1001
L[6:0]	sets line address of the display RAM to be displayed on the initial ROW 0		0000000
C[6:0]	sets the initial ROW 0 of the display; this command cannot access the icon driver row ROW 80; if icon row is enabled		0000000
P[6:0]	partial display mode 1 : 16 to 1 : 80; note 1		1010000 (1 : 80)/1000000 (1 : 64)
PC[1:0]	switch HV generator on/off		00
S[1:0]	charge pump multiplication factor		00

Note

1. Partial displays can be selected in steps of 8 when the icon mode is not selected. When the icon mode is selected partial displays can be selected in steps of 16. For example, without icons the available partial display sizes are 8, 16, 24, 32, 40, 48, 56, 64 or 72 lines. With icons there are 16, 32, 48 or 64 lines possible.

Table 7 Power control

PC[1:0]	DESCRIPTION
00	HVgen off
01	HVgen on
10	HVgen on
11	HVgen on

Table 8 Power-Save Mode (PSM), OS, DON, DAL and E combinations; note 1

PSM	OS	DON	DAL	E	DESCRIPTION
0	0	X	X	X	oscillator off; HVgen disabled
0	1	X	0	X	oscillator on; HVgen enabled
0	1	0	1	X	display off, ROW/COL at V_{SS}; oscillator off; HVgen disabled; note 2
0	1	1	0	0	normal display mode
0	1	1	0	1	inverse display mode
0	1	1	1	X	all pixels on; note 3
1	X	X	X	X	power-save mode: display off; ROW/COL at V_{SS}; oscillator off; HVgen disabled

Notes

1. X = don’t care.
2. The DON bit can only be addressed after DAL is activated.
3. The DAL bit has priority over the E bit.

Table 9 Read status byte

BIT	DESCRIPTION
BUSY	if BUSY = 0 the chip is able to accept new commands
DON	same bit as in Table 4
$\overline{RES}$	if $\overline{RES}$ = 1 a reset is in progress
MF[2:0]	device manufacturer ID
DS0	device recognition; see Table 10

Table 10 Device recognition; note 1

DS0	DESCRIPTION
0	64 row driver
1	80 row driver

Note

1. This is the only default setting after reset, another setting can be selected with the ‘set partial display mode’ command.

Table 11 Multiplication settings

S[1:0]	DESCRIPTION
00	4 × voltage multiplier
01	5 × voltage multiplier
10	6 × voltage multiplier
11	7 × voltage multiplier

Table 12 V_{OS} values in twos complement notation

DECIMAL	BINARY
0	00000
+1	00001
+2	00010
+3	00011
+4	00100
+5	00101
+6	00110
+7	00111
+8	01000
+9	01001
+10	01010
+11	01011
+12	01100
+13	01101
+14	01110
+15	01111
–1	11111
–2	11110
–3	11101
–4	11100
–5	11011
–6	11010
–7	11001
–8	11000
–9	10111
–10	10110
–11	10101
–12	10100
–13	10011
–14	10010
–15	10001
–16	10000

13.1.2 Specific commands of the basic command set

Table 13 Explanation of symbols

BIT	LOGIC 0	LOGIC1	RESET STATE
V_{PR}[5:0]	programming value of V_{LCD}		000000
V_{OFF}[2:0]	offset for the programming value of V_{LCD}		000

13.1.3 SPECIFIC COMMANDS OF THE EXTENDED COMMAND SET

Table 14 Explanation of symbols

BIT	LOGIC 0	LOGIC 1	RESET STATE
$V_{PR}[7:6] + V_{PR}[5:0]$	programming value of V_{LCD}		00000000
FR[1:0]	frame-rate frequency		11
TC[2:0]	temperature coefficient		(TC2) 010
V	horizontal addressing	vertical addressing	0
DOR	LSB at top	MSB at top	0
IC	no Icon row (1/16 to 1/80)	Icon row (1/16 to 1/80)	0
BRS	bottom rows are not mirrored	bottom rows are mirrored	0
MP(1)	mux rate driven p value (automatic)	p = 4 selected for mux rate 1 : 64 and 1 : 80	0
EC	use internal oscillator	use external oscillator	0
S[2:0]	charge pump multiplication factor		100

Note

1. It is strongly recommended to use the p = 4 setting.

Table 15 Frame-rate frequency

FR[1:0]	FRAME-RATE FREQUENCY
00	30 Hz
01	40 Hz
10	50 Hz
11	60 Hz

Table 16 Temperature coefficient

TC[2:0]	TEMPERATURE COEFFICIENT
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Table 17 Multiplication settings

S[2:0]	DESCRIPTION
000	2 × voltage multiplier
001	3 × voltage multiplier
010	4 × voltage multiplier
011	5 × voltage multiplier
100	4 × voltage multiplier
101	5 × voltage multiplier
110	6 × voltage multiplier
111	7 × voltage multiplier

13.2 Initialization

Reset is accomplished by applying an external reset pulse (active LOW) at pad $\overline{RES}$. When reset occurs within the specified time, all internal registers are reset, however the RAM is still undefined. The state after reset is described in Section 13.3. Pad $\overline{RES}$ must be $\leq 0.3V_{DD1}$ when V_{DD1} reaches $V_{DD(min)}$ (or higher) within a maximum time t_{VHRL} after V_{DD1} goes high (see Fig.43).

A reset can also be achieved by sending a reset command. This command can be used during normal operation but not to initialize the chip after power-on.

13.3 Reset function

13.3.1 BASIC COMMAND SET

After reset the LCD driver has the following state:

- Display setting E = 0 and DAL = 0
- Address commands X[6:0] = 0 and Y[3:0] = 0
- V_{LCD} is equal to 0, the HV generator is switched off (PC[1:0] = 00)
- No offset of the programming range (V_{OFF}[2:0] = 0)
- HV generator programming (V_{PR}[5:0] = 0)
- 4 × voltage multiplier (S[1:0] = 00)
- After power-on, RAM data is undefined, the reset signal does not change the content of the RAM
- All LCD outputs at V_{SS} (display off)
- Initial display line set to line 0 (L[6:0] = 0)
- Initial row set to ROW 0 (C[6:0] = 0)
- Full display selected (P[6:0] = mux 1 : 80 or 1 : 64)
- Display is not mirrored (MX = 0 and MY = 0)
- Internal oscillator is off
- Power-save mode is on
- No frame calibration is running.

13.3.2 EXTENDED COMMAND SET

After reset the LCD driver has the following state:

- Display settings E = 0 and DAL = 0
- Icons disabled (IC = 0)
- Address counter X[6:0] = 0 and Y[3:0] = 0
- Temperature control mode TC2 (TC[2:0] = 010)
- V_{LCD} is equal to 0; the HV generator is switched off (PC[1:0] = 0)
- HV generator programming (V_{PR}[7:0] = 0)
- 4 × voltage multiplier (S[2:0] = 100)
- Frame-rate frequency (FR[1:0] = 11)
- After power-on, RAM data is undefined, the reset signal does not change the content of the RAM
- All LCD outputs at V_{SS} (display off)
- Full display selected (P[6:0] = mux 1 : 80 or 1 : 64)
- Initial display line set to line 0 (L[6:0] = 0)
- Initial row set to ROW 0 (C[6:0] = 0)
- Display is not mirrored (MX = 0; MY = 0)
- Internal oscillator is off
- Power-save mode is on
- Horizontal addressing enabled (V = 0)
- No data order swap (DOR = 0)
- No bottom row swap (BRS = 0)
- Internal oscillator enabled (EC = 0)
- No frame calibration running (OC = 0).

13.4 Power-save mode

In the power-save mode the LCD driver has the following state:

- All LCD outputs at V_{SS} (display off)
- Bias generator and V_{LCD} generator switched off; external V_{LCD} can be disconnected
- Oscillator off (external clock possible)
- RAM contents not cleared; RAM data can be written
- V_{LCD} discharged to V_{SS} in Power-down mode.

There are two ways to put the chip into power-save mode:

- The display must be off (DON = 0) and all the pixels on (DAL = 1)
- The power-save mode command is activated.

13.5 Display control

The bits DON, E and DAL select the display mode; see Table 8.

13.5.1 MX

When MX = 0 the display RAM is written from left to right (X = 0 is on the left side and X = X max is on the right side of the display).

When MX = 1 the display RAM is written from right to left (X = 0 is on the right side and X = X max is on the left side of the display).

The MX bit has an impact on the way the RAM is written to. So if a horizontal mirroring of the display is desired, the RAM must first be rewritten, after changing the MX bit.

13.5.2 MY

When MY = 1, the display is mirrored vertically.

A change of this bit has an immediate effect on the display.

13.6 Set Y address of RAM

Y[3:0] defines the Y address of the display RAM.

Table 18 X/Y address range

Y3	Y2	Y1	Y0	CONTENT	ALLOWED X RANGE
0	0	0	0	bank 0 (display RAM)	0 to 127
0	0	0	1	bank 1 (display RAM)	0 to 127
0	0	1	0	bank 2 (display RAM)	0 to 127
0	0	1	1	bank 3 (display RAM)	0 to 127
0	1	0	0	bank 4 (display RAM)	0 to 127
0	1	0	1	bank 5 (display RAM)	0 to 127
0	1	1	0	bank 6 (display RAM)	0 to 127
0	1	1	1	bank 7 (display RAM)	0 to 127
1	0	0	0	bank 8 (display RAM)	0 to 127
1	0	0	1	bank 9 (display RAM)	0 to 127

When the icon row is enabled this icon row (ROW 79) will always be in bank 9 independent of the mux rate which is programmed.

13.7 Set X address of RAM

The X address points to the columns. The range of X is 0 to 127 (7FH).

13.8 Set display start line

L[6:0] is used to select the display line address of the display RAM to be displayed on the initial row, ROW 0. The selection of L is limited to steps of 8. When the icon row is selected, the selection of L is limited to steps of 16. When a partial mode is selected, the selection of L is also limited in steps. In addition, the selection of L = 72 is not allowed when the icon row is enabled or disabled.

The initial row can, in turn, be set by C[6:0]. ROW 0 cannot be set to the icon row ROW 79 when enabled.

An example of the mapping from the RAM content to the display is illustrated in Fig.30. The content of the RAM is not modified. This feature allows, for instance, screen scrolling without rewriting the RAM.

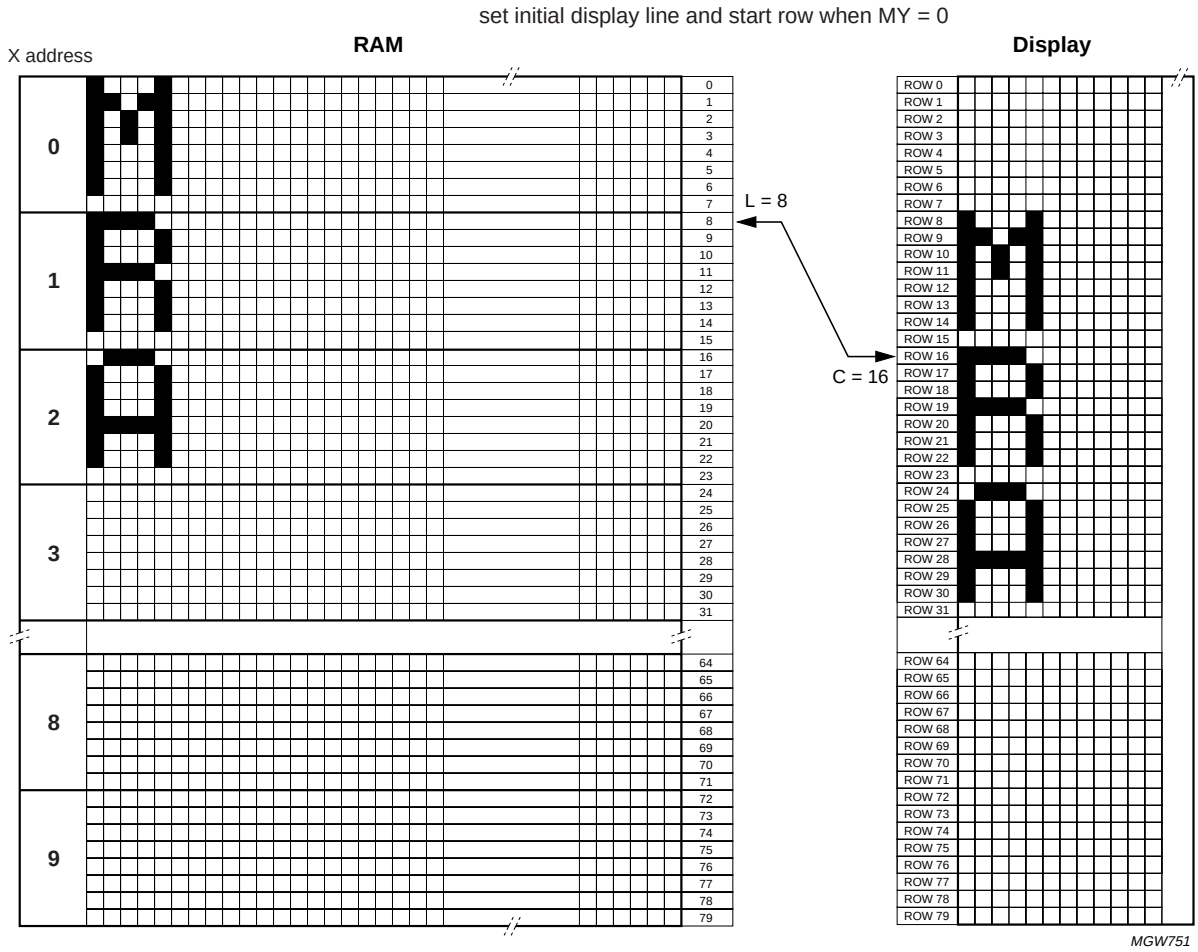


Fig.30 Programming the L address and C address when MY = 0.

13.9 Bias levels

The bias levels for an MRA driving method with p = 8 are given in Fig.31 when G_{max} and F have the same value. The value p defines the number of rows which are simultaneously selected.

Fig.31 Bias levels for a MRA system with p = 8 and G_{max} = F.

The row voltage F depends on the mux rate selected (number of rows N), the threshold voltage of the liquid (V_{TH}), the number of simultaneously selected rows (p) and the multiplexibility (m):

$$F = \frac{1}{\sqrt{p}} \times V_{TH} \times \sqrt{\frac{N}{2} \times \frac{\sqrt{m} \pm \sqrt{m-N}}{\sqrt{m}-1}} \quad (1)$$

The column voltages are situated around the common level V_C. The column voltage levels are equidistant from each other. In Table 19 the column voltage levels are given as a function of F.

Table 19 Bias levels for MRA driving method

SYMBOL	BIAS VOLTAGES	DC SHIFTED BIAS VOLTAGES
$F = G_{max}$		
V_{LCD}	F	V_{LCD}
V3_H	$(p-2)\times\frac{F}{\sqrt{m}-\sqrt{m-N}}$	$\frac{V_{LCD}}{2}\times\left(1+\frac{(p-2)}{\sqrt{m}-\sqrt{m-N}}\right)$
V2_H	$(p-4)\times\frac{F}{\sqrt{m}-\sqrt{m-N}}$	$\frac{V_{LCD}}{2}\times\left(1+\frac{(p-4)}{\sqrt{m}-\sqrt{m-N}}\right)$
V1_H	$(p-6)\times\frac{F}{\sqrt{m}-\sqrt{m-N}}$	$\frac{V_{LCD}}{2}\times\left(1+\frac{(p-6)}{\sqrt{m}-\sqrt{m-N}}\right)$
V_C	0	$^1/_2V_{LCD}$
V1_L	$-(p-6)\times\frac{F}{\sqrt{m}-\sqrt{m-N}}$	$\frac{V_{LCD}}{2}\times\left(1-\frac{(p-6)}{\sqrt{m}-\sqrt{m-N}}\right)$
V2_L	$-(p-4)\times\frac{F}{\sqrt{m}-\sqrt{m-N}}$	$\frac{V_{LCD}}{2}\times\left(1-\frac{(p-4)}{\sqrt{m}-\sqrt{m-N}}\right)$
V3_L	$-(p-2)\times\frac{F}{\sqrt{m}-\sqrt{m-N}}$	$\frac{V_{LCD}}{2}\times\left(1-\frac{(p-2)}{\sqrt{m}-\sqrt{m-N}}\right)$
V_{SS}	–F	V_{SS}

The row voltages (F) are not necessarily larger then the column voltages. This depends on the number of rows which are selected, the multiplexibility and the value of p. However, the PCF8811 is designed in such a way that the maximum column voltages are always equal to the row voltages. In Table 20 the V_{LCD} and the different bias levels are given for the PCF8811. The V_{LCD} voltage is defined as:

$$V_{LCD} = 2\times F \qquad (2)$$

Where F is defined in (1)

The bias system settings for different display modes are given in Table 20. All bias levels can be calculated by using the third column of Table 19 and the variables given in Table 20. Programming of the bias levels is not necessary in the PCF8811. The selection of the appropriate bias level voltages for each display mode is done automatically. Only the appropriate V_{LCD} voltage must be programmed according to equations (1) and (2) for the display modes listed in Table 20.

The variables for calculating V_{LCD}, when the icon row is enabled, are given in Table 21. The icon row can only be addressed in the extended command set.

The PCF8811 allows the value of p, for certain mux rates, to be chosen manually.

This is only possible for the mux rates 1 : 64 and 1 : 80. If other mux rates are chosen the PCF8811 determines the optimum value of p. By setting the value of p manually a compromise can be made between contrast and power consumption with certain liquids for the high mux rates 1 : 64 and 1 : 80. However, care must be taken that the liquid which is chosen ensures that the row voltages (F) and the maximum column voltages are equal.

Table 20 Relationship between mux rates and bias setting variables without icon row

MUX RATE	N	m	p
1 : 16	16	25	2
1 : 24	24	49	2
1 : 32	32	81	2
1 : 40	40	49	4
1 : 48	48	64	4
1 : 56	56	81	4
1 : 64	64	64	8
1 : 72	72	81	8
1 : 80	80	81	8

Table 21 Relationship between mux rates and bias setting variables with the icon row (only extended command set)

MUX RATE	N	m	p
1 : 16	24	49	2
1 : 32	40	49	4
1 : 48	56	81	8
1 : 64	80	81	8
1 : 80	80	81	8

13.10 Set V_{OP} value

For mux rate 1 : 80 the optimum operation voltage of a liquid can be calculated with the variables given in Table 21 and equations (1) and (2).

$$V_{LCD} = \frac{2}{\sqrt{8}} \times V_{TH} \times \sqrt{\frac{80}{2} \times \frac{\sqrt{81} - \sqrt{81 - 80}}{\sqrt{81} - 1}} = 4.472 \times V_{TH} \quad (3)$$

Where V_{TH} is the threshold voltage of the liquid crystal material used.

The way of programming the V_{OP} value is implemented differently in the basic command set in comparison to the extended command set. In the basic command set two commands are sent to the PCF8811: namely V_{PR}[5:0] and V_{OFF}[2:0]. In the extended command set only one command V_{PR}[7:0] is sent to the PCF8811. This V_{OP} programming is illustrated in Fig.32. The programming of V_{OP} in the basic command set can be used when the PCF8811 is used as a replacement for an IAPT LCD driver. A conversion table (ROM) can be provided which transfers the programming of an IAPT V_{OP} value to a MRA V_{OP} value.

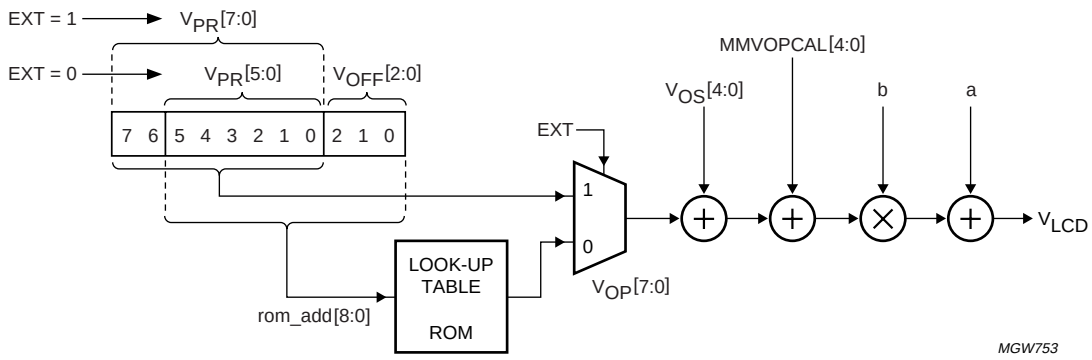


Fig.32 Setting of V_{OP} in the basic and extended command set.

13.10.1 Basic command set

The V_{LCD} at T = T_{CUT} in the basic command set is determined by the conversion in the ROM look-up table with the programmed values of V_{PR}[5:0] and V_{OFF}[2:0]. It can, additionally, be adjusted with the V_{LCD} offset pads V_{OS}[4:0] to obtain the optimum optical performance. Instead of using the V_{LCD} offset pads (V_{OP}[4:0]) the V_{LCD} can be adjusted with the module maker calibration setting MMVOPCAL[4:0]; see Chapter 22.

$$V_{LCD(T = T_{CUT})} = a + (V_{OS}[4:0] + V_{OP}[7:0]) \times b \quad (4)$$

Where:

- T_{CUT} is a reference temperature; see Section 13.11
- a is a fixed constant value; see Table 22
- b is a fixed constant value; see Table 22
- V_{OP}[7:0] is the result of the conversion table
- V_{OS}[4:0]/MMVOPCAL[4:0] is the value of the offset V_{LCD} offset pads or the value stored in the OTP cells.

Table 22 Parameters of V_{LCD} for the basic and extended command set

SYMBOL	VALUE	UNIT
T_{CUT}	40	°C
b	0.03	V
a	3	V

13.10.2 Extended Command set

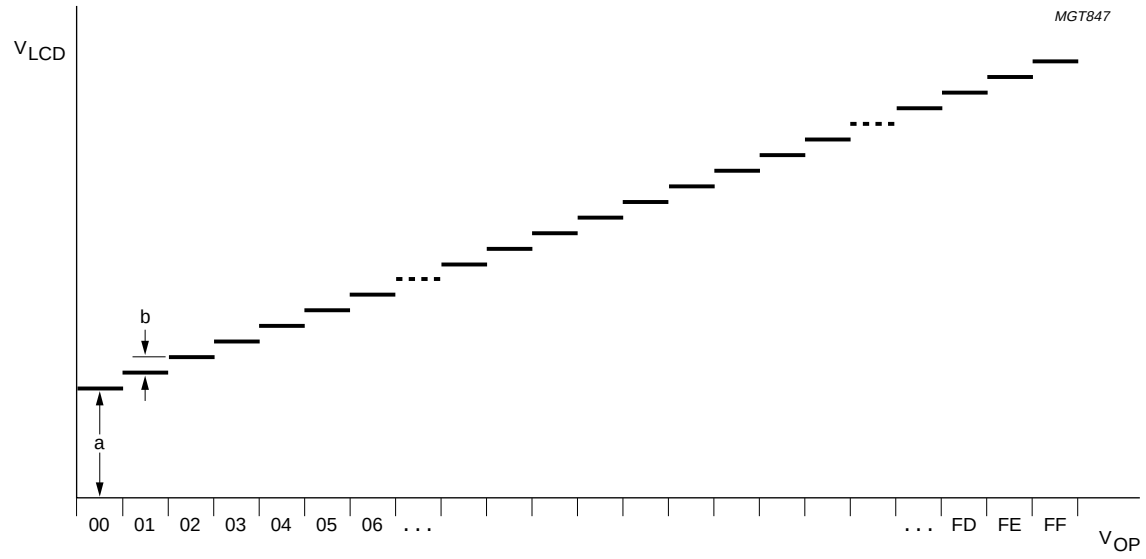
The V_{LCD} at T = T_{CUT} can be calculated with equation (5). In the extended command set V_{PR}[7:0] is the same value as V_{OP}[7:0]. It can additionally be adjusted with the V_{LCD} offset pads V_{OS}[4:0] to obtain the optimum optical performance. Instead of using the V_{LCD} offset pads (V_{OP}[4:0]) the V_{LCD} can be adjusted with the module maker calibration setting MMVOPCAL[4:0]; see Chapter 22.

$$V_{LCD(T = T_{CUT})} = a + (V_{OS}[4:0] + V_{PR}[7:0]) \times b \quad (5)$$

Where:

- T_{CUT} is a reference temperature (see Section 13.11)
- a is a fixed constant value (see Table 22)
- b is a fixed constant value (see Table 22)
- V_{PR}[7:0] is the programmed V_{OP} value
- V_{OS}[4:0]/MMVOPCAL[4:0] is the value of the offset V_{LCD} offset pads or the value stored in the OTP cells.

As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD} (9 V) the user has to ensure while setting the V_{PR} register and selecting the Temperature Compensation (TC), that under all conditions and including all tolerances the V_{LCD} remains below 9.0 V. This is valid for the two different command sets.



V_{OP}[7:0] programming, (00H to FFH).

Fig.33 V_{LCD} programming of PCF8811.

13.11 Temperature control

Due to the temperature dependency of the liquid crystals viscosity the LCD controlling voltage V_{LCD} might have to be increased at lower temperature to maintain optimum contrast.

The V_{LCD} at a specific temperature is calculated as follows for both command sets. V_{LCD} (at $T = T_{CUT}$) is given by equations (4) or (5), depending on the command set which is used.

$$V_{LCD_{(T)}} = V_{LCD_{(T = T_{CUT})}} \times [1 + (T - T_{CUT}) \times TC] \quad (6)$$

In the extended command set and basic command set 8 different temperature coefficients are available (see Fig.34). The typical values of the different temperature coefficients are given in Chapter 16. The coefficients are proportional to the programmed V_{LCD}.

The basic and extended command set differ in the way that the temperature coefficients can be accessed. In the basic command set only one temperature coefficient is available. However, the possibility exists to program the default temperature coefficient by means of OTP programming; see Chapter 22. In the extended command set the different temperature coefficients are selected by the interface with three bits TC[2:0].

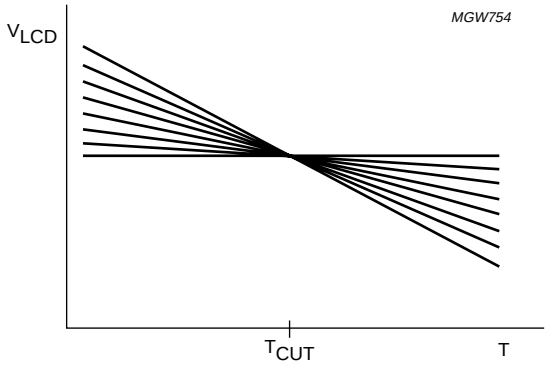


Fig.34 Temperature coefficients.

14 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); notes 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}	general supply voltage	–0.5	+6.5	V
V_{DD2}, V_{DD3}	supply voltage for the internal voltage generator	–0.5	+4.5	V
V_{LCD}	LCD supply voltage	–0.5	+10.0	V
V_i	all input voltages	–0.5	V_{DD1} + 0.5	V
I_{SS}	ground supply current	–50	+50	mA
I_i, I_o	DC input or output current	–10	+10	mA
P_{tot}	total power dissipation	–	300	mW
P_{out}	power dissipation per output	–	30	mW
T_{stg}	storage temperature	–65	+150	°C

Notes

1. Stresses above those listed under limiting values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are referenced to V_{SS} unless otherwise specified.

15 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

16 DC CHARACTERISTICS

V_{DD1} = 1.7 V to 3.3 V; V_{SS} = 0 V; V_{LCD} = 3.0 V to 9.0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	general supply voltage		1.7	–	3.3	V
		basic command set; when using ROM look-up table (see Section 13.10)	2.0	–	3.3	V
V_{DD2}, V_{DD3}	supply voltage for the internal voltage generator		1.8	–	3.3	V
V_{LCDIN}	LCD supply voltage	LCD voltage externally supplied (voltage generator disabled)	–	–	9.0	V
V_{LCDOUT}	voltage multiplier output voltage	LCD voltage internally generated (voltage generator enabled); note 1	–	–	9.0	V
$V_{LCD(tol)}$	tolerance of generated V_{LCD}	without calibration	–300	–	+300	mV
		with calibration; note 2	–70	–	+70	mV
I_{DD1}	general supply current	notes 3 and 4	0.5	1.5	5	µA
		notes 4 and 5	15	25	50	µA
I_{DD2}, I_{DD3}	supply current for the internal voltage generator	notes 3 and 4	0	0.5	1	µA
		notes 5 and 4	130	150	200	µA
$I_{DD(tot)}$	total supply current (V_{DD1} + V_{DD2} + V_{DD3})	notes 5 and 4	145	175	250	µA
Logic inputs; MF[2:0], V_{OS}[4:0], DS0, EXT, PS[2:0], $\overline{RES}$ and OSC						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.2V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD1}$	–	V_{DD1}	V
I_L	leakage current	V_I = V_{DD} or V_{SS}	–1	–	+1	µA
Column and row outputs						
R_{col}	column output resistance COL 0 to COL 127	V_{LCD} = 5 V	–	–	5	kΩ
R_{row}	row output resistance ROW 0 to ROW 79	V_{LCD} = 5 V	–	–	5	kΩ
$V_{bias(col)}$	bias tolerance voltage COL 0 to COL 127		–100	0	+100	mV
$V_{bias(row)}$	bias tolerance voltage ROW 0 to ROW 80		–100	0	+100	mV
LCD supply voltage generator						
TC0	V_{LCD} temperature coefficient 0		–	0	–	/°C
TC1	V_{LCD} temperature coefficient 1		–	$–0.16 \times 10^{–3}$	–	/°C
TC2	V_{LCD} temperature coefficient 2		–	$–0.33 \times 10^{–3}$	–	/°C
TC3	V_{LCD} temperature coefficient 3		–	$–0.50 \times 10^{–3}$	–	/°C
TC4	V_{LCD} temperature coefficient 4		–	$–0.66 \times 10^{–3}$	–	/°C
TC5	V_{LCD} temperature coefficient 5		–	$–0.833 \times 10^{–3}$	–	/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TC6	V_{LCD} temperature coefficient 6		–	-1.25×10^{-3}	–	/°C
TC7	V_{LCD} temperature coefficient 7	note 6	–	-1.66×10^{-3}	–	/°C
Parallel interface; V_{DD1} = 1.8 V to 3.3 V						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.2V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD1}$	–	V_{DD1}	V
Serial interface; V_{DD1} = 1.7 V to 3.3 V						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.2V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD1}$	–	V_{DD1}	V
I^2C-bus interface; V_{DD1} = 1.8 V to 3.3 V						
$I_{OL(SDA)}$	LOW-level output current at pin SDA	V_{OL} = 0.4 V; V_{DD1} > 2 V	–	–	3	mA
		$V_{OL} = 0.2V_{DD1}$; V_{DD1} < 2 V	–	–	2	mA
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	–	V_{DD1}	V
Output levels for all interfaces						
V_{OL}	LOW-level output voltage	I_{OL} = 0.5 mA	V_{SS}	–	$0.2V_{DD1}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = –0.5 mA	$0.8V_{DD1}$	–	V_{DD1}	V

Notes

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Valid for values of temperature, V_{PR} and TC used at calibration.
3. During power-down all static currents are switched off.
4. Conditions are: V_{DD1} = 1.8 V, V_{DD2} = 2.7 V, V_{LCD} = 8.05 V, voltage multiplier $4V_{DD2}$, inputs at V_{DD1} or V_{SS}, interface inactive, internal V_{LCD} generation, V_{LCD} output is loaded by 10 μA and T_{amb} = 25 °C.
5. Normal mode.
6. TC7 can only be used when $V_{DD2} = V_{DD3}$ = 2.4 V or higher.

17 AC CHARACTERISTICS

V_{DD1} = 1.7 V to 3.3 V; V_{SS} = 0 V; V_{LCD} = maximum 9.0 V; T_{amb} = –40 °C to +85 °C; note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{ext}	external clock frequency		–	200	–	kHz
f_{frame}	frame frequency	T_{amb} = 25 °C; V_{DD1} = 2.4 V	54	60	66	Hz
			43	58	73	Hz
t_{VHRL}	V_{DD} to $\overline{RES}$ LOW	see Fig.43	0(2)	–	1	μs
t_{RW}	$\overline{RES}$ LOW pulse width	see Fig.43	500	–	–	ns

Notes

1. All specified timings are based on 20 % and 80 % of V_{DD}.
2. $\overline{RES}$ may be LOW before V_{DD} goes HIGH.

18 PARALLEL INTERFACE TIMING CHARACTERISTICS

V_{DD1} = 1.8 V to 3.3 V; V_{SS} = 0 V; V_{LCD} = maximum 9.0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Parallel bus timing; see Figs 35 and 36				
6800 SERIES				
$t_{SU;DC}$	data/$\overline{\text{command}}$ set-up time	40	–	ns
$t_{HD;DC}$	data/$\overline{\text{command}}$ hold time	20	–	ns
$T_{cyc(DS)}$	data strobe cycle time	1000	–	ns
$t_{DS(L)}$	data strobe LOW time	320	–	ns
$t_{DS(H)}$	data strobe HIGH time	300	–	ns
$t_{SU;RW}$	read/$\overline{\text{write}}$ set-up time	280	–	ns
$t_{HD;RW}$	read/$\overline{\text{write}}$ hold time	20	–	ns
$t_{SU;CE}$	chip enable set-up time	280	–	ns
$t_{HD;CE}$	chip enable hold time	0	–	ns
$t_{SU;DAT}$	data set-up time	20	–	ns
$t_{HD;DAT}$	data hold time	40	–	ns
$t_{DAT;ACC}$	data output access time	–	280	ns
$t_{DAT;OH}$	data output disable time	–	20	ns

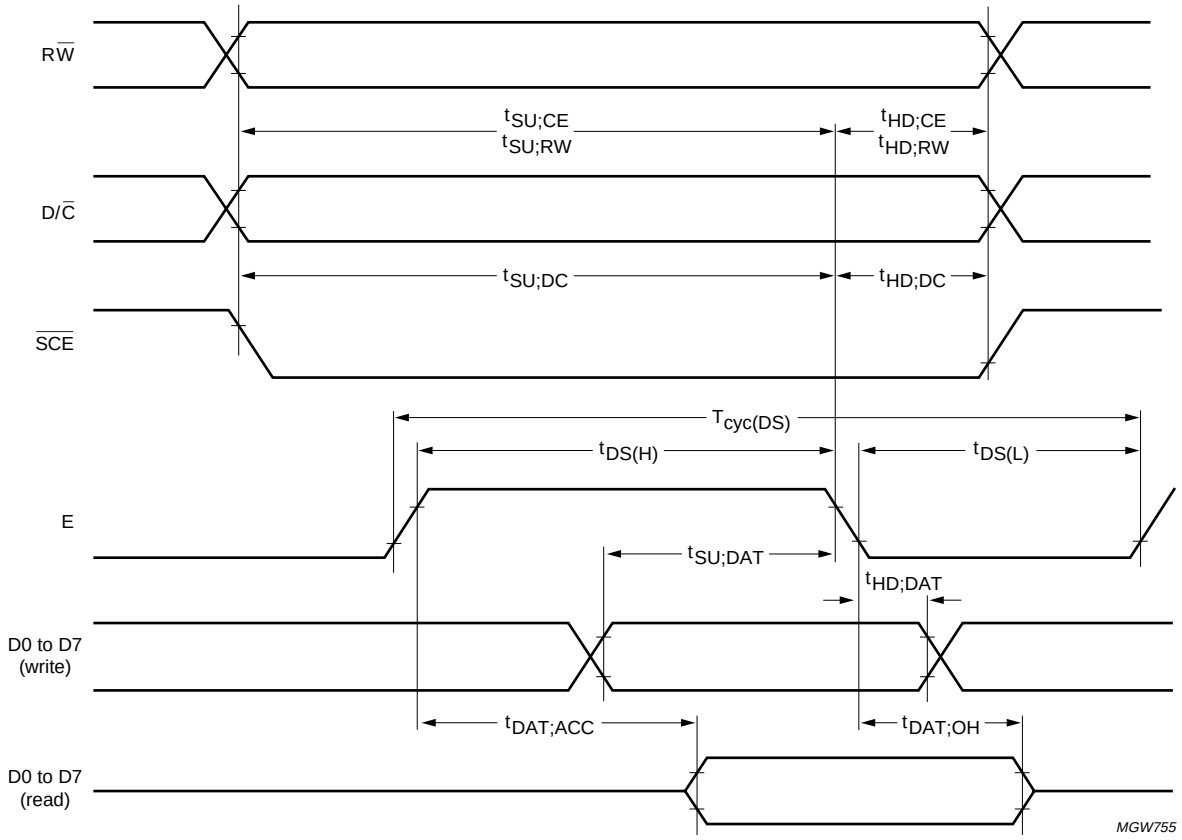


Fig.35 Parallel interface timing (6800-series) (read).

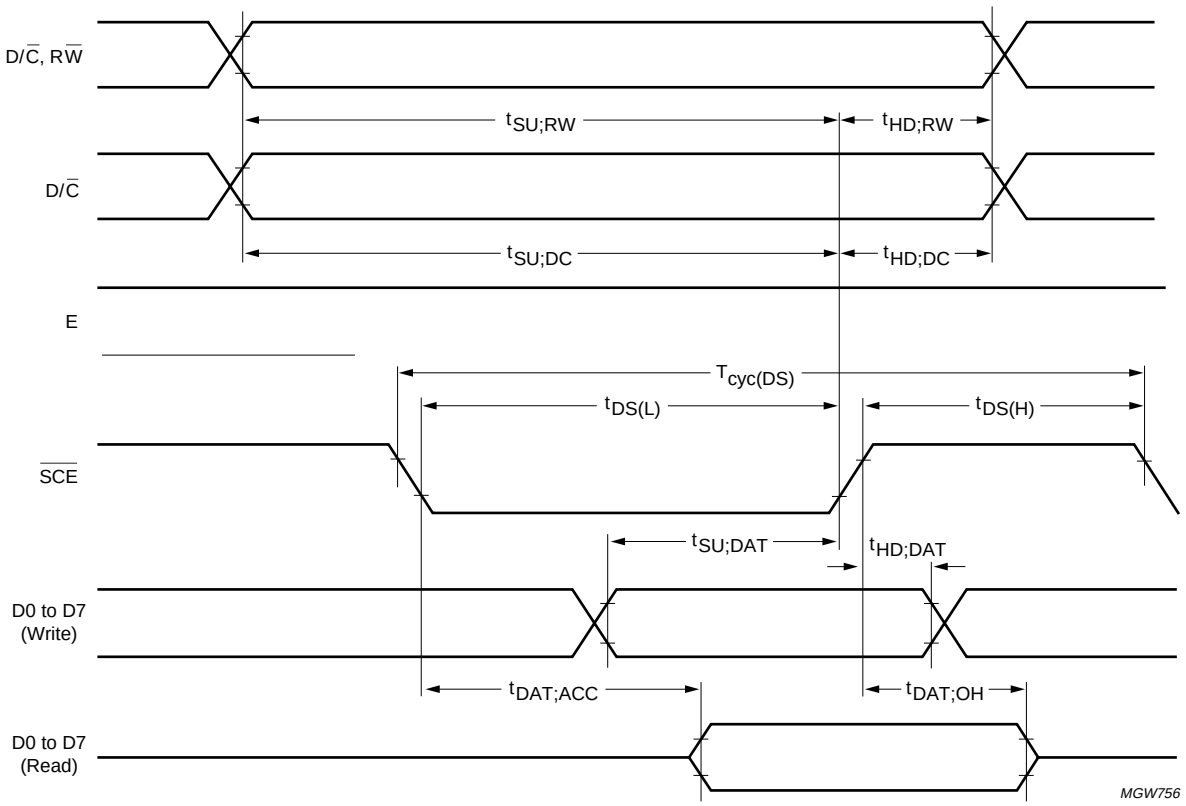


Fig.36 Parallel interface timing (6800-series) (write).

19 SERIAL INTERFACE TIMING CHARACTERISTICS

V_{DD1} = 1.8 V to 3.3 V; V_{SS} = 0 V; V_{LCD} = maximum 9.0 V; T_{amb} = –40 °C to +85 °C; note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
3-line and 4-line (SPI and serial interface); see Fig.37 to Fig.40					
f_{SCLK}	clock frequency		9.00	–	MHz
T_{cyc}	clock cycle SCLK		111	–	ns
t_{PWH1}	SCLK pulse width HIGH		45	–	ns
t_{PWL1}	SCLK pulse width LOW		45	–	ns
t_{S2}	$\overline{SCE}$ set-up time		50	–	ns
t_{H2}	$\overline{SCE}$ hold time		45	–	ns
t_{PWH2}	$\overline{SCE}$ minimum high time		50	–	ns
t_{H5}	$\overline{SCE}$ start hold time	note 2	50	–	ns
t_{S4}	SDIN set-up time		50	–	ns
t_{H4}	SDIN hold time		50	–	ns
t_{S3}	data/$\overline{command}$ set-up time		50	–	ns
t_{H3}	data/$\overline{command}$ hold time		50	–	ns
t_{S1}	SDIN set-up time		50	–	ns
t_{H1}	SDIN hold time		50	–	ns
t_1	SDOUT access time		–	50	ns
t_2	SDOUT disable time	note 3	–	50	ns
t_3	$\overline{SCE}$ hold time		50	–	ns
t_4	SDOUT disable time	note 4	25	100	ns
C_b	capacitive load for SDO	note 5	–	30	pF
R_b	series resistance for SDO	note 5	–	500	Ω

Notes

1. All specified timings are based on 20 % and 80 % of V_{DD}.
2. t_{H5} is the time from the previous SCLK rising edge (irrespective of the state of $\overline{SCE}$) to the falling edge of $\overline{SCE}$.
3. SDOUT disable time for SPI 3-line or 4-line interface.
4. SDOUT disable time for serial interface 3-line.
5. Maximum values are for f_{SCLK} = 9 MHz. Series resistance includes ITO track + connector resistance + printed-circuit board.

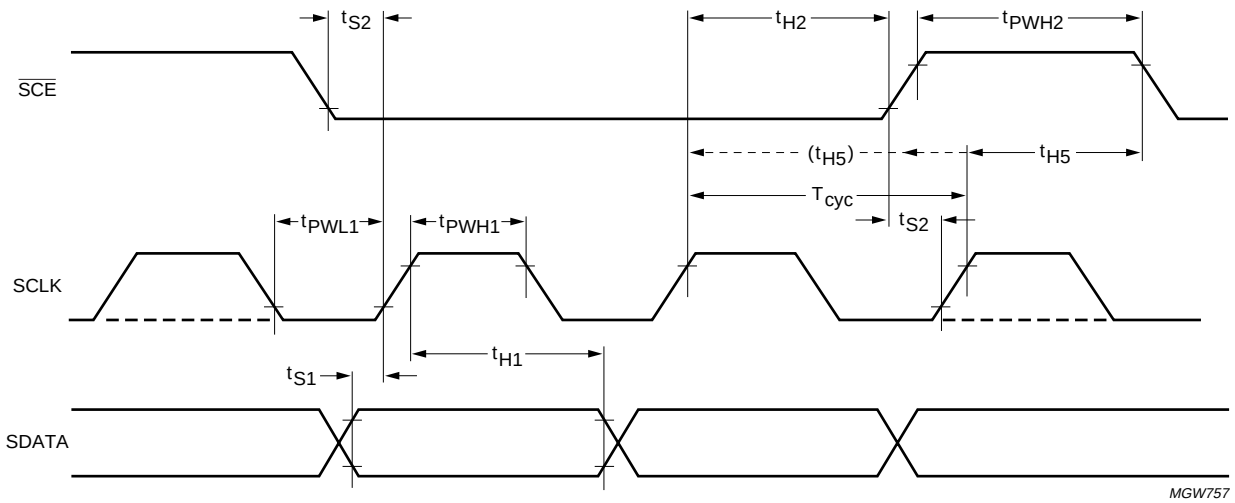


Fig.37 3-line serial interface timing.

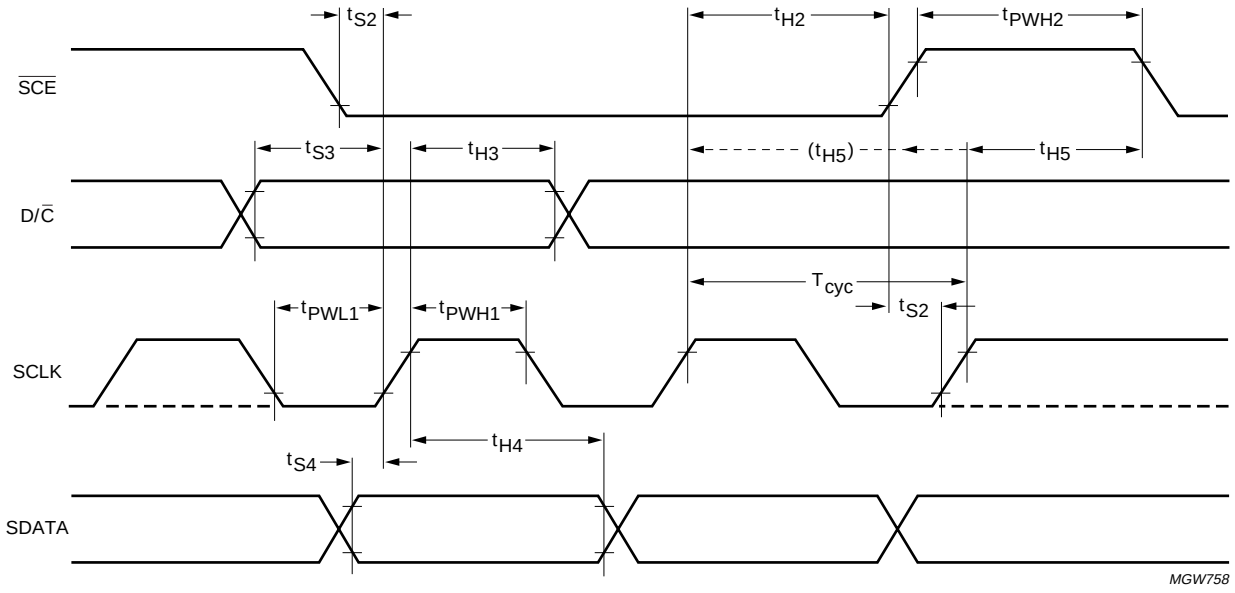


Fig.38 4-line serial interface timing.

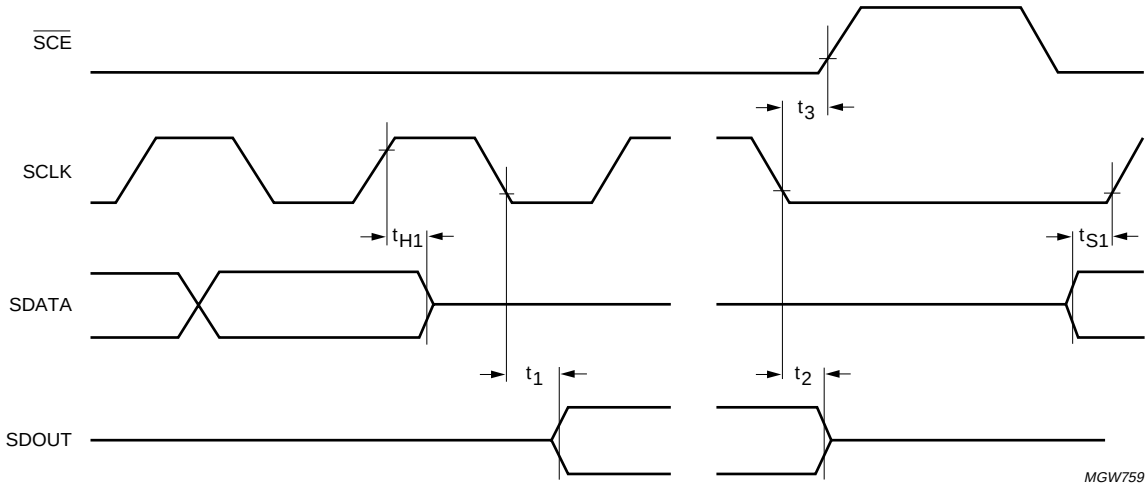


Fig.39 Serial interface timing; read mode SPI 3- or 4-line.

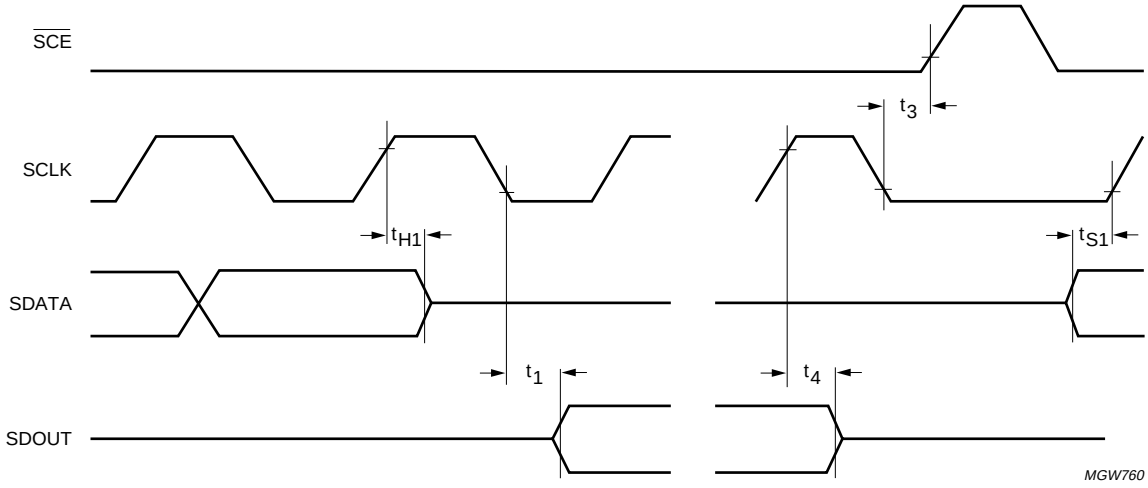


Fig.40 Serial interface timing; read mode serial interface 3-line.

20 I²C-BUS INTERFACE TIMING CHARACTERISTICS

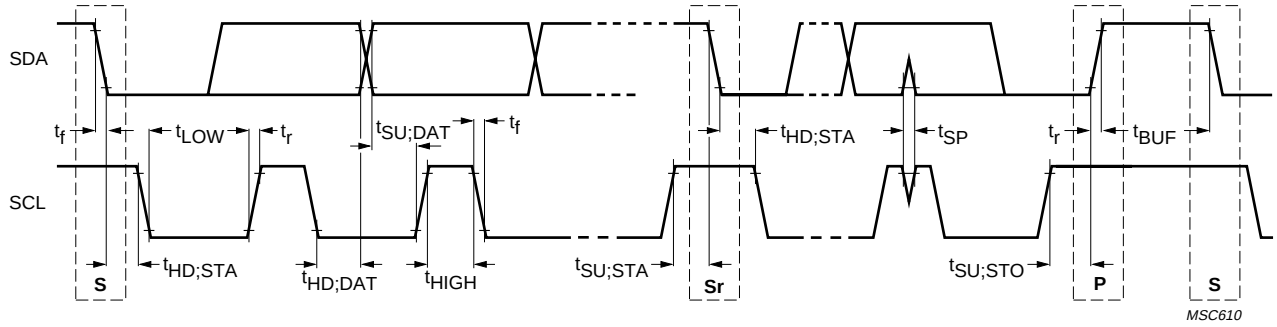
V_{DD1} = 1.8 V to 3.3 V; V_{SS} = 0 V; V_{LCD} = maximum 9.0 V; T_{amb} = −40 °C to +85 °C; note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fs-mode; see Fig.41						
f_{SCLH}	SCLH clock frequency		0	–	400	kHz
$t_{SU;STA}$	set-up time (repeated) START condition		600	–	–	ns
$t_{HD;STA}$	hold time (repeated) START condition		600	–	–	ns
t_{LOW}	LOW period of the SCLH clock		1300	–	–	ns
t_{HIGH}	HIGH period of the SCLH clock		600	–	–	ns
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	900	ns
t_r	SCL and SDA rise time	note 2	$20 + 0.1C_b$	–	300	ns
t_f	SCL and SDA fall time	note 2	$20 + 0.1C_b$	–	300	ns
C_b	capacitive load represented by each bus line		–	–	400	pF
$t_{SU;STO}$	set-up time for STOP condition		600	–	–	ns
t_{SP}	tolerable spike width on bus		–	–	50	ns
t_{BUF}	bus free time between START and STOP condition		1300	–	–	ns
V_{nL}	noise margin at the LOW level for each connected device (including hysteresis)		$0.1V_{DD1}$	–	–	V
V_{nH}	noise margin at the HIGH-level for each connected device (including hysteresis)		$0.2V_{DD1}$	–	–	V
Hs-mode; see Fig.42						
f_{SCLH}	SCLH clock frequency		0	–	3.4	MHz
$t_{SU;STA}$	set-up time (repeated) START condition		160	–	–	ns
$t_{HD;STA}$	hold time (repeated) START condition		160	–	–	ns
t_{LOW}	LOW period of the SCLH clock		160	–	–	ns
t_{HIGH}	HIGH period of the SCLH clock		60	–	–	ns
$t_{SU;DAT}$	data set-up time		10	–	–	ns
$t_{HD;DAT}$	data hold time		20	–	70	ns
t_{rCL}	rise time of the SCLH signal		10	–	40	ns
t_{rCL1}	rise time of the SCLH signal after the acknowledge bit		10	–	80	ns
t_{fCL}	fall time of the SCLH signal		10	–	40	ns
t_{rDA}	rise time of the SDAH signal		10	–	80	ns
t_{fCL1}	fall time of the SCLH signal		10	–	80	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{SU;STO}$	set-up time for STOP condition		160	–	–	ns
C_{b2}	capacitive load for the SDAH and SCLH lines	note 2	–	–	100	pF
C_b	capacitive load for the SDAH + SDA line and SCLH + SCL line	note 2	–	–	400	pF
t_{SP}	tolerable spike width on bus		–	–	5	ns
V_{nL}	noise margin at the LOW-level for each connected device (including hysteresis)		$0.1V_{DD1}$	–	–	V
V_{nH}	noise margin at the HIGH-level for each connected device (including hysteresis)		$0.2V_{DD1}$	–	–	V

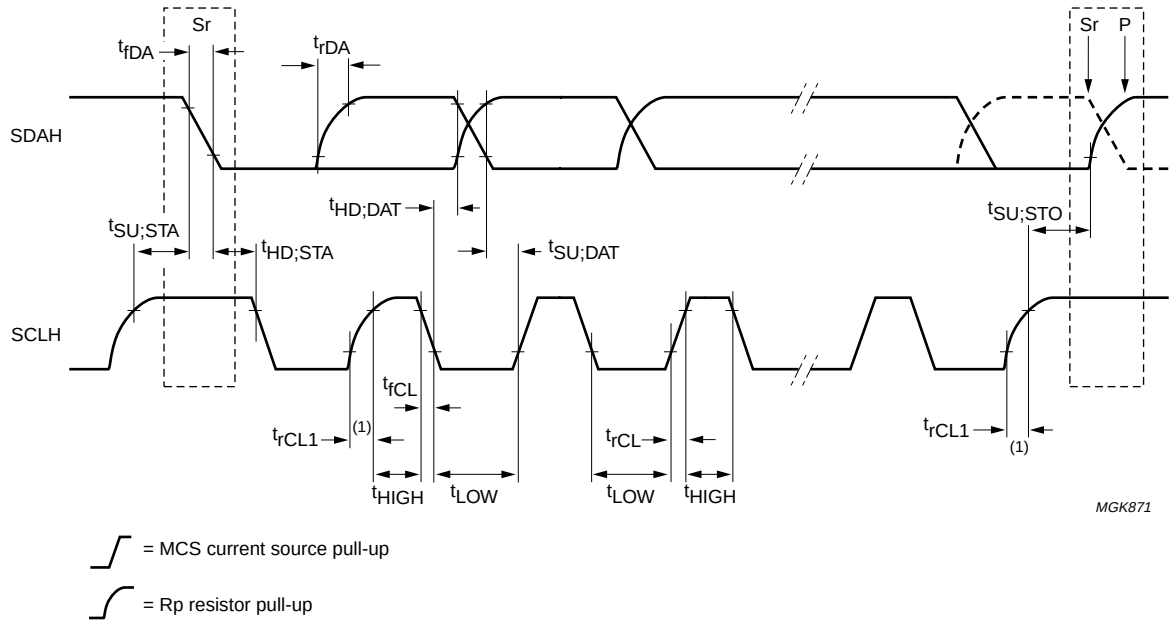
Notes

1. All specified output timings are based on 20 % and 80 % of V_{DD1}.
2. C_b = 100 pF total capacitance of one bus line.



S = Start.
Sr = Start repeated.
P = Stop.

Fig.41 I^2C-bus timing diagram (Fs-mode).



(1) Rising edge of the first SCLH clock pulse after an acknowledge bit.

Fig.42 I^2C-bus timing diagram (Hs-mode).

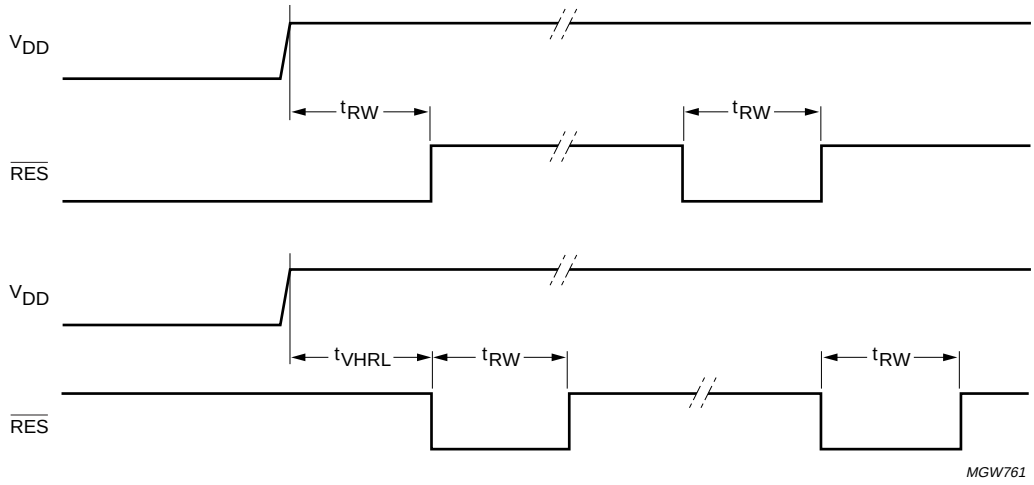


Fig.43 Reset timing.

21 APPLICATION INFORMATION

Semiconductors are light sensitive. Exposure to light sources can cause malfunction of the IC. In the application it is therefore required to protect the IC from light. The protection has to be done on all sides of the IC, i.e. front, rear and all edges.

The pinning of the PCF8811 has an optimum design for single plane wiring e.g. for chip-on-glass display modules. Display size: 80 × 128 pixels.

For further application information refer to Philips Application note AN10170.

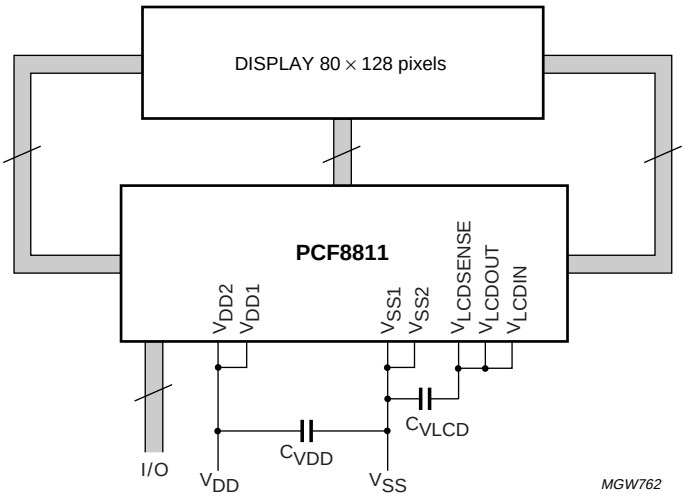


Fig.44 Application diagram: internal charge pump is used and a single supply.

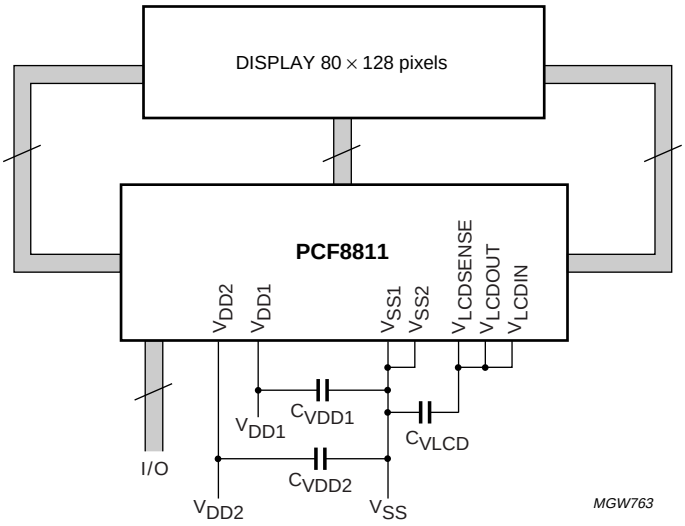


Fig.45 Application diagram: internal charge pump is used and two separate supplies (V_{DD1} and V_{DD2}).

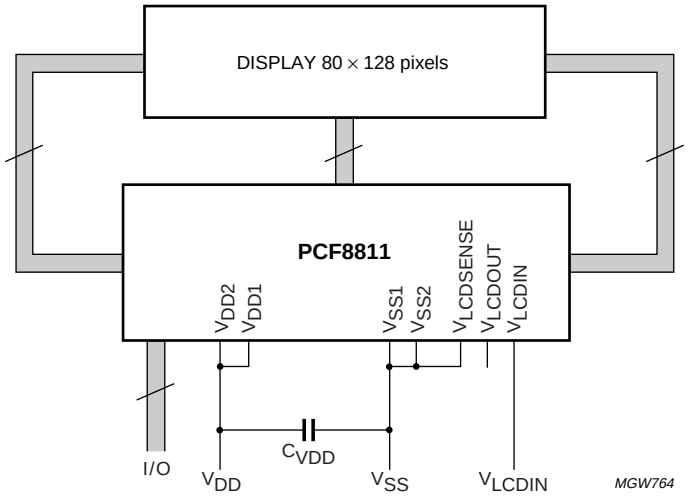


Fig.46 Application diagram: external high voltage is used.

The required minimum value for the external capacitors in an application with the PCF8811 are:

C_{VLCD} = 1 μF to 4.7 μF depending on the application

C_{VDD}, C_{VDD1} and C_{VDD2} = 1 μF. For these capacitors higher values can be used.

22 MODULE MAKER PROGRAMMING

The One Time Programmable (OTP) technology is implemented on the PCF8811. It enables the module maker to program some extended features of the PCF8811 after it has been assembled on an LCD module. Programming is made under the control of the interfaces and the use of one special pin. This pin must be made available on the module glass but need not to be accessed by the set maker.

The PCF8811 features 3 module maker programmable parameters:

- V_{LCD} calibration
- Temperature coefficient selection
- Seal bit.

22.1 V_{LCD} calibration

The first feature included is the ability to adjust the V_{LCD} voltage with a 5-bit code (MMVOPCAL). This code is implemented in twos complement notation giving rise to a positive or negative offset to the V_{PR} register. This is in the same manner as the on-glass calibration pins V_{OS}.

In theory, both may be used together but it is recommended that the V_{OS} pins are tied to V_{SS} when OTP calibration is being used. This will set them to a default offset of zero. If both are used then the addition of the two 5-bit numbers must not exceed a 5-bit result otherwise the resultant value will be undefined. The final adder in the circuit has underflow and overflow protection. In the event of an overflow, the output will be clamped to 255; during an underflow the output will be clamped to 0.

The final control to the high voltage generator, V_{OP}, will be the sum of all the calibration registers and pins. The V_{LCD} equation (4) or (5) given in Section 13.10 must be extended to include the OTP calibration, as follows;

$$V_{LCD(T = T_{CUT})} = a + (V_{OS}[4:0] + MMVOPCAL[4:0] + V_{OP}[7:0]) \times b \quad (7)$$

The possible MMVOPCAL[4:0] values are the same as the V_{OS}[4:0] values; see Table 12.

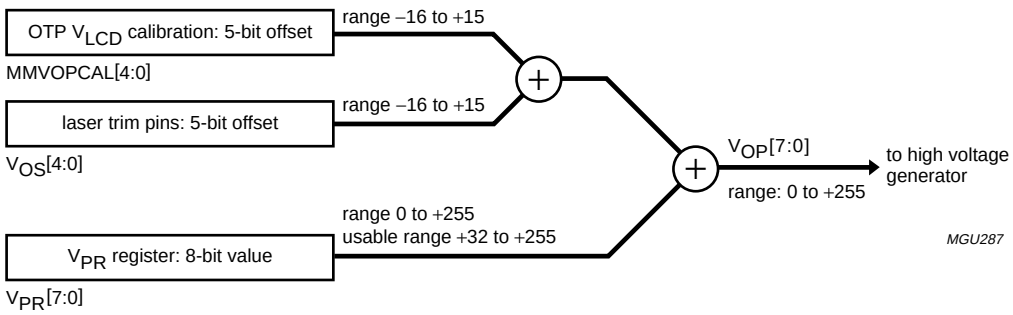


Fig.47 V_{LCD} calibration.

22.2 Temperature coefficient selection

The second feature is an OTP factory default setting for the temperature coefficient selection (MMTC) in the basic command set. This 3-bit value will be loaded from OTP after leaving the power-save mode or by the refresh command. The idea of this feature is to provide, in the basic command set, the complete set of temperature coefficients without an additional command. In the extended command set the temperature coefficient can be programmed as given in Table 16.

22.3 Seal bit

The module maker programming is performed in a special mode: the calibration mode (CALMM). This mode is entered via a special interface command, CALMM.
To prevent wrongful programming, a seal bit has been implemented which prevents the device from entering the calibration mode. This seal bit, once programmed, can not be reversed, thus further changes in programmed values are not possible.

Applying the programming voltages when not in CALMM mode will have no effect on the programmed values.

Table 23 Seal bit definition

SEAL BIT	ACTION
0	possible to enter calibration mode
1	calibration mode disabled

22.4 OTP architecture

The OTP circuitry in the PCF8811 contains 9 bits of data: 5 for V_{LCD} calibration (MMVOPCAL), 3 for the temperature coefficient default setting in the basic command set MMTC and 1 seal bit. The circuitry for 1-bit is called an OTP slice. Each OTP slice consists of 2 main parts: the OTP cell (a non-volatile memory cell) and the shift register cell (a flip-flop). The OTP cells are only accessible through their shift register cells: on the one hand both reading from and writing to the OTP cells is performed with the shift register cells, on the other hand only the shift register cells are visible to the rest of the circuit. The basic OTP architecture is shown in Fig.48.

This OTP architecture allows the following operations:

1. Reading data from the OTP cells. The content of the non-volatile OTP cells is transferred to the shift register where upon it may affect the PCF8811 operation.
2. Writing data to the OTP cells. First, all 9 bits of data are shifted into the shift register via the interface. The content of the shift register is then transferred to the OTP cells (there are some limitations related to storing data in these cells; see Section 22.7).
3. Checking calibration without writing to the OTP cells. Shifting data into the shift register allows the effects on the V_{LCD} voltage to be observed.

The reading of data from the OTP cells is initiated by either:

- Exit from power-save mode
- The ‘Refresh’ command (power control).

It should be noted that in both cases the reading operation needs up to 5 ms to complete.

The shifting of data into the shift register is performed in the special mode CALMM. In the PCF8811 the CALMM mode is entered by the CALMM command. Once in the CALMM mode the data is shifted into the shift register via the interface at the rate of 1-bit per command. After transmitting the last (9th) bit and exiting the CALMM mode, the serial interface will return to the normal mode and all other commands can be sent. Care should be taken that 9 bits of data (or a multiple of 9) are always transferred before exiting the CALMM mode, otherwise the bits will be in the wrong positions.

In the shift register the value of the seal bit is, like the others, always zero at reset. To ensure that the security feature works correctly, the CALMM command is disabled until a refresh has been performed. Once the refresh is completed, the seal bit value in the shift register will be valid and permission to enter the CALMM mode can thus be determined.

The 9 bits are shifted into the shift register in a predefined order: first 5 bits of MMVOPCAL[4:0], 3 bits for MMTC[2:0] and lastly the seal bit. The MSB is always first, thus the first bit shifted is MMVOPCAL[4] and the two last bits are MMTC[0] and the seal bit.

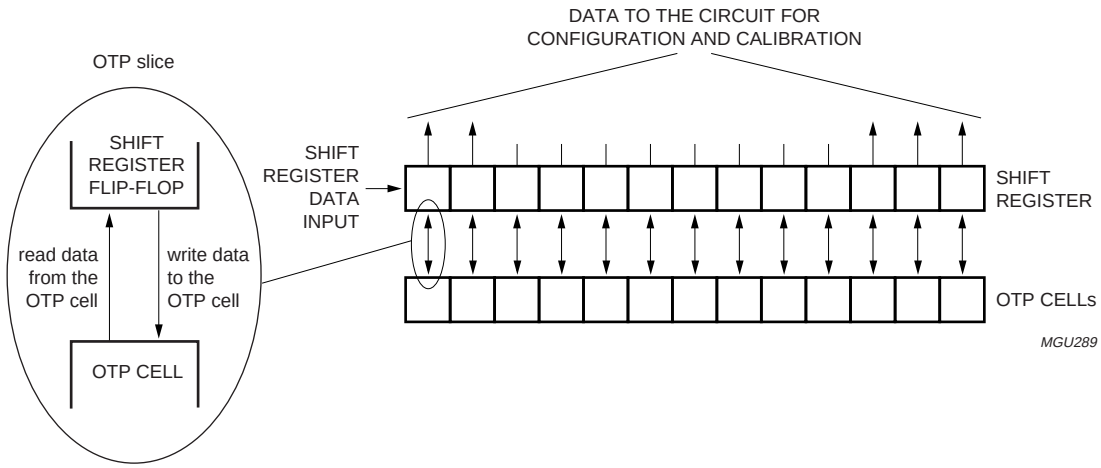


Fig.48 Basic OTP architecture.

22.5 Interface commands

These instructions are in addition to those indicated in Table 5.

Table 24 Additional instructions; note 1

NAME	EXT	D/$\overline{C}$	R/$\overline{W}$	COMMAND BYTE								ACTION
				D7	D6	D5	D4	D3	D2	D1	D0	
CALMM	X	0	0	1	0	0	0	0	0	1	0	enter CALMM mode
Power control (‘Refresh’)	X	0	0	0	0	1	0	1	PC1	PC0	1	switch HVgen on/off to force a refresh of the shift register

Note

1. X = don’t care.

22.5.1 CALMM

This instruction puts the device in calibration mode. This mode enables the shift register for loading and allows programming of the non-volatile OTP cells to take place. If the seal bit is set then this mode cannot be accessed and the instruction will be ignored. Once in calibration mode all commands are interpreted as shift register data. The mode can only be exited by sending data with bit D7 set to logic 0. Reset will also clear this mode. Each shift register data byte is preceded by D/$\overline{C}$ = 0 and has only 2 significant bits, thus the remaining 6 bits are ignored. Bit D7 is the continuation bit (D7 = 1 remain in CALMM mode, D7 = 0 exit CALMM mode). Bit D0 is the data bit and its value is shifted into the OTP shift register (on the falling edge of SCLK).

22.5.2 REFRESH

The action of the ‘Refresh’ instruction is to force the OTP shift register to re-load from the non-volatile OTP cells. This instruction takes up to 5 ms to complete. During this time all other instructions may be sent.

In the PCF8811 the ‘Refresh’ instruction is associated with the ‘Power control’ instruction so that the shift register is automatically refreshed every time the high voltage generator is enabled or disabled. It should be noted however, that if this instruction is sent while in the power-save mode, the PC[1:0] bits will be updated but the refreshing will be ignored.

22.6 Example of filling the shift register

An example of the sequence of commands and data is shown in Table 25. In this example the shift register is filled with the following data: MMVOPCAL = –4 (11100 BIN), MMTC = 2 (010 BIN) and the seal bit is 0.

It is assumed that the PCF8811 has just been reset. After transmitting the last bit the PCF8811 can exit or remain in the CALMM mode (see step 1). It should be noted that while in CALMM mode the interface does not recognize commands in the normal sense.

After this sequence has been applied it is possible to observe the impact of the data shifted in. The described sequence is, however, not useful for OTP programming because the number of bits with the value logic 1 is greater than that allowed for programming; see Section 22.7. Figure 49 shows the shift register after this action.

Table 25 Example sequence for filling the shift register; note 1

STEP	EXT	D/$\overline{C}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	ACTION
1	X	0	0	1	1	1	0	0	0	0	1	exit Power-down
2												wait 5 ms for refresh to take effect
3	X	0	0	1	0	0	0	0	0	1	0	enter CALMM mode
4	X	0	0	1	X	X	X	X	X	X	1	shift in data. MMVOPCAL[4] is first bit; note 2
5	X	0	0	1	X	X	X	X	X	X	1	MMVOPCAL[3]
6	X	0	0	1	X	X	X	X	X	X	1	MMVOPCAL[2]
7	X	0	0	1	X	X	X	X	X	X	0	MMVOPCAL[1]
8	X	0	0	1	X	X	X	X	X	X	0	MMVOPCAL[0]
9	X	0	0	1	X	X	X	X	X	X	0	MMTC[2]
10	X	0	0	1	X	X	X	X	X	X	1	MMTC[1]
11	X	0	0	1	X	X	X	X	X	X	0	MMTC[0]
12	X	0	0	0	X	X	X	X	X	X	0	seal bit; exit CALMM mode
An alternative ending could be to stay in CALMM mode												
13	X	0	0	1	X	X	X	X	X	X	0	seal bit; remain in CALMM mode

Notes

1. X = don’t care.
2. The data for the bits is not in the correct shift register position until all bits have been sent.

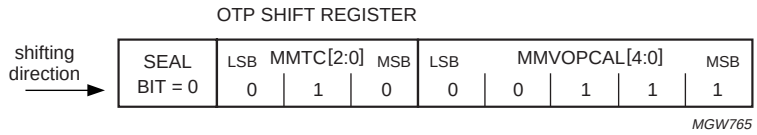


Fig.49 Shift register contents after example sequence of Table 25.

22.7 Programming flow

Programming is achieved whilst in CALMM mode and with the application of the programming voltages. As mentioned previously, the data for programming the OTP cell is contained in the corresponding shift register cell. The shift register cell must be loaded with a logic 1 in order to program the corresponding OTP cell. If the shift register cell contains a logic 0, then no action will take place when the programming voltages are applied.

Once programmed, an OTP cell cannot be de-programmed. An already programmed cell, i.e. an OTP cell containing a logic 1, must not be re-programmed.

During programming a substantial current flows in the V_{LCDIN} pin. For this reason it is recommended to program only one OTP cell at a time. This is achieved by filling all but one shift register cells with logic 0.

It should be noted that the programming specification refers to the voltages at the chip pins, contact resistance must therefore be considered by the user.

An example sequence of commands and data for OTP programming is given in Table 26.

The order for programming cells is not significant. However, it is recommended that the seal bit is programmed last. Once this bit has been programmed it will not be possible to re-enter the CALMM mode.

It is assumed that the PCF8811 has just been reset.

Table 26 Sequence for OTP programming; note 1

STEP	EXT	D/$\overline{C}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	ACTION
1	X	0	0	1	1	1	0	0	0	0	1	exit power-save
2												wait 5 ms for refresh to take effect
3	X	0	0	1	0	1	0	1	0	0	1	re-enter Power-down (DON = 0)
4	X	0	0	1	0	0	0	0	0	1	0	enter CALMM mode
5	X	0	0	1	0	X	X	X	X	X	1	shift in data; MMVOPCAL[4] is first bit
6	X	0	0	1	0	X	X	X	X	X	1	MMVOPCAL[3]
7	X	0	0	1	0	X	X	X	X	X	1	MMVOPCAL[2]
9	X	0	0	1	0	X	X	X	X	X	0	MMVOPCAL[1]
10	X	0	0	1	0	X	X	X	X	X	0	MMVOPCAL[0]
11	X	0	0	1	0	X	X	X	X	X	0	MMTC[2]
12	X	0	0	1	0	X	X	X	X	X	1	MMTC[1]
13	X	0	0	1	0	X	X	X	X	X	0	MMTC[0]
14	X	0	0	1	1	X	X	X	X	X	0	seal bit; remain in CALMM mode
15												apply programming voltage at pins $V_{OTPPROG}$ and V_{LCDIN} according to Section 22.8
Repeat steps 5 to 14 for each bit that should be programmed to 1												
16												apply external reset

Note

1. X = don't care.

22.8 Programming specification

Table 27 Programming specification; see Fig.50

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{OTPPROG}$	voltage applied to pin $V_{OTPPROG}$ relative to V_{SS1}	programming active; note 1	11.0	11.5	12.0	V
		programming inactive; note 1	V_{SS} − 0.2	0	+0.2	V
V_{LCDIN}	voltage applied to pin V_{LCDIN} relative to V_{SS1}	programming active; notes 1 and 2	9	9.5	10	V
		programming inactive; notes 1 and 2	V_{DD2} − 0.2	V_{DD2}	4.5	V
I_{LCDIN}	current drawn by V_{LCDIN} during programming	when programming a single bit to logic 1	–	850	1000	µA
$I_{VOTPPROG}$	current drawn by $V_{OTPPROG}$ during programming		–	100	200	µA
$T_{amb(PROG)}$	ambient temperature during programming		0	25	40	°C
$t_{SU;SCLK}$	set-up time of internal data after last clock		1	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{HD;SCLK}$	hold time of internal data before next clock		1	–	–	µs
$t_{SU;VOTPPROG}$	set-up time of $V_{OTPPROG}$ prior to programming		1	–	10	µs
$t_{HD;VOTPPROG}$	hold time of $V_{OTPPROG}$ after programming		1	–	10	ms
t_{PW}	pulse width of programming voltage		100	120	200	ms

Notes

1. The voltage drop across the ITO track and zebra connector must be taken into account to guarantee a sufficiently high voltage at the chip pins.
2. The Power-down mode (DON = 0 and DAL = 1) and CALMM mode must be active while the V_{LCDIN} pin is being driven.

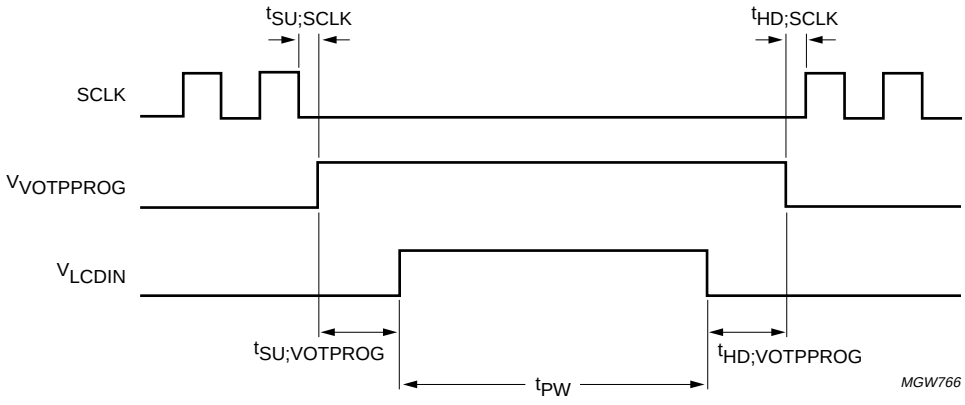


Fig.50 Programming waveforms.

23 CHIP INFORMATION

The PCF8811 is manufactured in n-well CMOS technology. The substrate is at V_{SS} potential.

24 BONDING PAD LOCATIONS

Table 28 Bonding pad information

PAD	ROWS/COLS SIDE	INTERFACE SIDE	UNIT
Pad pitch	min. 51.84	min. 54	μm
Pad size (aluminium)	42.84 × 105	50 × 100	μm
Bump dimensions	31.9 × 100 × 17.5 (±5)	34 × 95 × 17.5 (±5)	μm
Wafer thickness (excluding bumps)	381 (±25)		μm

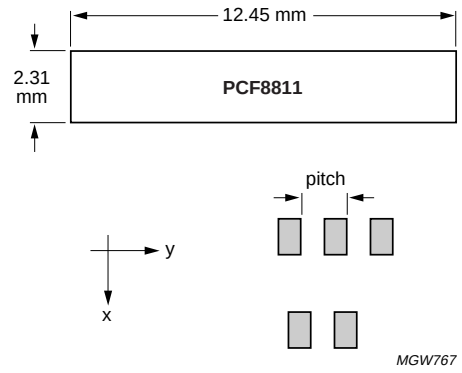


Fig.51 Chip size and pad pitch.

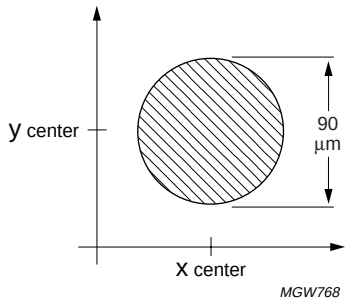


Fig.52 Shape of alignment mark (90 μm diameter).

Table 29 Bonding pad locations
All x and y co-ordinates are referenced to the centre of the chip (dimensions in μm; see Fig.53).

SYMBOL	PAD	CO-ORDINATES	
		x	y
dummy_slanted	1	6092	1030
alignment mark	2	5995	1017
dummy	3	5876	1030
dummy	4	5822	1030
dummy	5	5768	1030
dummy	6	5714	1030
dummy	7	5660	1030
dummy	8	5390	1030
MF2	9	5012	1030
MF1	10	4850	1030
MF0	11	4688	1030
DS0	12	4526	1030
OSC	13	4364	1030
EXT	14	4094	1030
PS0	15	3932	1030
PS1	16	3770	1030
PS2	17	3608	1030
$V_{SS(tie\ off)}$	18	3446	1030
SDAHOUT	19	2960	1030
SDAH	20	2420	1030
SDAH	21	2366	1030
SCLH/$\overline{SCE}$	22	1826	1030
SCLH/$\overline{SCE}$	23	1772	1030
$V_{OTPPROG}$	24	1664	1030
$V_{OTPPROG}$	25	1610	1030
$V_{OTPPROG}$	26	1556	1030
$\overline{RES}$	27	1448	1030
D/$\overline{C}$	28	1232	1030
R/$\overline{W}$	29	962	1030
E	30	800	1030
$V_{DD(tie\ off)}$	31	638	1030
DB0	32	476	1030
DB1	33	314	1030
DB2	34	152	1030
DB3	35	−10	+1030
DB4	36	−172	+1030
DB5	37	−334	+1030
DB6	38	−550	+1030
DB7	39	−712	+1030
V_{DD1}	40	−874	+1030
V_{DD1}	41	−928	+1030
V_{DD1}	42	−982	+1030
V_{DD1}	43	−1036	+1030
V_{DD1}	44	−1090	+1030
V_{DD1}	45	−1144	+1030
V_{DD2}	46	−1198	+1030
V_{DD2}	47	−1252	+1030
V_{DD2}	48	−1306	+1030
V_{DD2}	49	−1360	+1030
V_{DD2}	50	−1414	+1030
V_{DD2}	51	−1468	+1030
V_{DD2}	52	−1522	+1030
V_{DD2}	53	−1576	+1030
V_{DD2}	54	−1630	+1030
V_{DD2}	55	−1684	+1030
V_{DD3}	56	−1738	+1030
V_{DD3}	57	−1792	+1030
V_{DD3}	58	−1846	+1030
V_{DD3}	59	−1900	+1030
V_{DD3}	60	−1954	+1030
V_{SS1}	61	−2062	+1030
V_{SS1}	62	−2116	+1030
V_{SS1}	63	−2170	+1030
V_{SS1}	64	−2224	+1030
V_{SS1}	65	−2278	+1030
V_{SS1}	66	−2332	+1030
V_{SS1}	67	−2386	+1030
V_{SS1}	68	−2440	+1030
V_{SS1}	69	−2494	+1030
V_{SS1}	70	−2548	+1030
V_{SS2}	71	−2602	+1030
V_{SS2}	72	−2656	+1030

SYMBOL	PAD	CO-ORDINATES	
		x	y
V_{SS2}	73	−2710	+1030
V_{SS2}	74	−2764	+1030
V_{SS2}	75	−2818	+1030
V_{SS2}	76	−2872	+1030
V_{SS2}	77	−2926	+1030
V_{SS2}	78	−2980	+1030
V_{SS2}	79	−3034	+1030
V_{SS2}	80	−3088	+1030
T5	81	−3250	+1030
T2	82	−3304	+1030
T1	83	−3466	+1030
T4	84	−3628	+1030
T3	85	−3790	+1030
V_{OS4}	86	−4060	+1030
V_{OS3}	87	−4222	+1030
V_{OS2}	88	−4384	+1030
V_{OS1}	89	−4654	+1030
V_{OS0}	90	−4816	+1030
V_{LCDOUT}	91	−4924	+1030
V_{LCDOUT}	92	−4978	+1030
V_{LCDOUT}	93	−5032	+1030
V_{LCDOUT}	94	−5086	+1030
V_{LCDOUT}	95	−5140	+1030
V_{LCDOUT}	96	−5194	+1030
V_{LCDOUT}	97	−5248	+1030
V_{LCDOUT}	98	−5302	+1030
V_{LCDOUT}	99	−5356	+1030
$V_{LCDSENSE}$	100	−5410	+1030
V_{LCDIN}	101	−5464	+1030
V_{LCDIN}	102	−5518	+1030
V_{LCDIN}	103	−5572	+1030
V_{LCDIN}	104	−5626	+1030
V_{LCDIN}	105	−5680	+1030
V_{LCDIN}	106	−5734	+1030
V_{LCDIN}	107	−5788	+1030
alignment mark	108	−5904	+1017
dummy	109	−6004	+1030

SYMBOL	PAD	CO-ORDINATES	
		x	y
dummy	110	−6058	+1030
dummy	111	−6112	+1030
dummy	112	−6129.24	−1032.5
dummy	113	−6077.40	−1032.5
dummy	114	−6025.56	−1032.5
R79	115	−5973.72	−1032.5
R78	116	−5921.88	−1032.5
R77	117	−5870.04	−1032.5
R76	118	−5818.20	−1032.5
R75	119	−5766.36	−1032.5
R74	120	−5714.52	−1032.5
R73	121	−5662.68	−1032.5
R72	122	−5610.84	−1032.5
R71	123	−5559.00	−1032.5
R70	124	−5507.16	−1032.5
R69	125	−5455.32	−1032.5
R68	126	−5403.48	−1032.5
R67	127	−5351.64	−1032.5
R66	128	−5299.80	−1032.5
R65	129	−5247.96	−1032.5
R64	130	−5196.12	−1032.5
R63	131	−5144.28	−1032.5
R62	132	−5092.44	−1032.5
R61	133	−5040.60	−1032.5
R60	134	−4988.76	−1032.5
R59	135	−4936.92	−1032.5
R58	136	−4885.08	−1032.5
R57	137	−4833.24	−1032.5
R56	138	−4781.40	−1032.5
R55	139	−4729.56	−1032.5
R54	140	−4677.72	−1032.5
R53	141	−4625.88	−1032.5
R52	142	−4574.04	−1032.5
R51	143	−4522.20	−1032.5
R50	144	−4470.36	−1032.5
R49	145	−4418.52	−1032.5
R48	146	−4366.68	−1032.5

SYMBOL	PAD	CO-ORDINATES	
		x	y
R47	147	–4314.84	–1032.5
R46	148	–4263	–1032.5
R45	149	–4211.16	–1032.5
R44	150	–4159.32	–1032.5
R43	151	–4107.48	–1032.5
R42	152	–4055.64	–1032.5
R41	153	–4003.80	–1032.5
R40	154	–3951.96	–1032.5
R80 (duplicate R79)	155	–3900.12	–1032.5
C0	156	–3640.92	–1032.5
C1	157	–3589.08	–1032.5
C2	158	–3537.24	–1032.5
C3	159	–3485.40	–1032.5
C4	160	–3433.56	–1032.5
C5	161	–3381.72	–1032.5
C6	162	–3329.88	–1032.5
C7	163	–3278.04	–1032.5
C8	164	–3226.20	–1032.5
C9	165	–3174.36	–1032.5
C10	166	–3122.52	–1032.5
C11	167	–3070.68	–1032.5
C12	168	–3018.84	–1032.5
C13	169	–2967	–1032.5
C14	170	–2915.16	–1032.5
C15	171	–2863.32	–1032.5
C16	172	–2811.48	–1032.5
C17	173	–2759.64	–1032.5
C18	174	–2707.80	–1032.5
C19	175	–2655.96	–1032.5
C20	176	–2604.12	–1032.5
C21	177	–2552.28	–1032.5
C22	178	–2500.44	–1032.5
C23	179	–2448.60	–1032.5
C24	180	–2396.76	–1032.5
C25	181	–2344.92	–1032.5
C26	182	–2293.08	–1032.5
C27	183	–2241.24	–1032.5

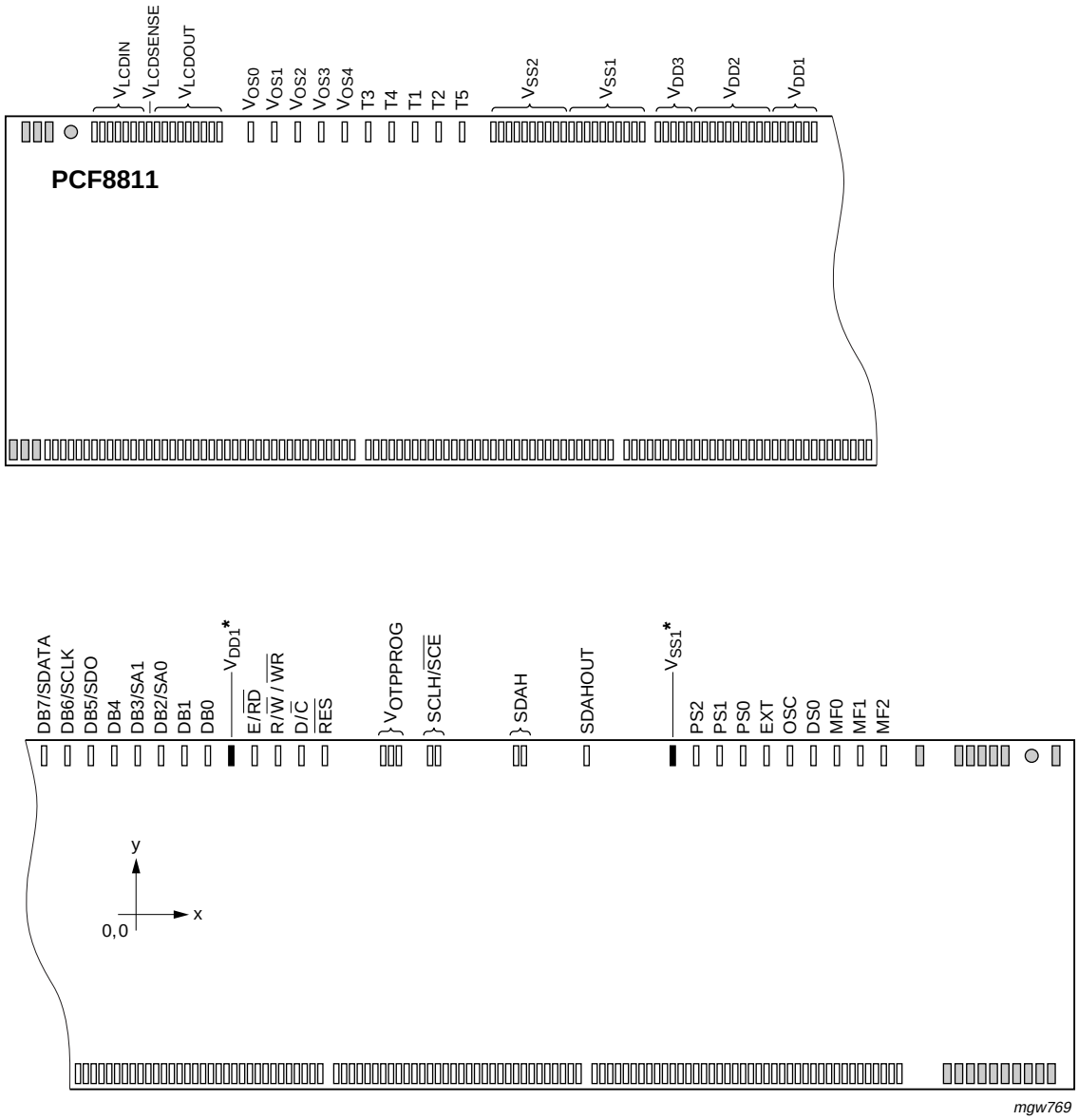
SYMBOL	PAD	CO-ORDINATES	
		x	y
C28	184	–2189.40	–1032.5
C29	185	–2137.56	–1032.5
C30	186	–2085.72	–1032.5
C31	187	–2033.88	–1032.5
C32	188	–1878.36	–1032.5
C33	189	–1826.52	–1032.5
C34	190	–1774.68	–1032.5
C35	191	–1722.84	–1032.5
C36	192	–1671.00	–1032.5
C37	193	–1619.16	–1032.5
C38	194	–1567.32	–1032.5
C39	195	–1515.48	–1032.5
C40	196	–1463.64	–1032.5
C41	197	–1411.80	–1032.5
C42	198	–1359.96	–1032.5
C43	199	–1308.12	–1032.5
C44	200	–1256.28	–1032.5
C45	201	–1204.44	–1032.5
C46	202	–1152.60	–1032.5
C47	203	–1100.76	–1032.5
C48	204	–1048.92	–1032.5
C49	205	–997.08	–1032.5
C50	206	–945.24	–1032.5
C51	207	–893.40	–1032.5
C52	208	–841.56	–1032.5
C53	209	–789.72	–1032.5
C54	210	–737.88	–1032.5
C55	211	–686.04	–1032.5
C56	212	–634.20	–1032.5
C57	213	–582.36	–1032.5
C58	214	–530.52	–1032.5
C59	215	–478.68	–1032.5
C60	216	–426.84	–1032.5
C61	217	–375	–1032.5
C62	218	–323.16	–1032.5
C63	219	–271.32	–1032.5
C64	220	–115.80	–1032.5

SYMBOL	PAD	CO-ORDINATES	
		x	y
C65	221	–63.96	–1032.5
C66	222	–12.12	–1032.5
C67	223	+39.72	–1032.5
C68	224	+91.56	–1032.5
C69	225	+143.40	–1032.5
C70	226	+195.24	–1032.5
C71	227	+247.08	–1032.5
C72	228	+298.92	–1032.5
C73	229	+350.76	–1032.5
C74	230	+402.60	–1032.5
C75	231	+454.44	–1032.5
C76	232	+506.28	–1032.5
C77	233	+558.12	–1032.5
C78	234	+609.96	–1032.5
C79	235	+661.80	–1032.5
C80	236	+713.64	–1032.5
C81	237	+765.48	–1032.5
C82	238	+817.32	–1032.5
C83	239	+869.16	–1032.5
C84	240	+921.00	–1032.5
C85	241	+972.84	–1032.5
C86	242	+1024.68	–1032.5
C87	243	+1076.52	–1032.5
C88	244	+1128.36	–1032.5
C89	245	+1180.20	–1032.5
C90	246	+1232.04	–1032.5
C91	247	+1283.88	–1032.5
C92	248	+1335.72	–1032.5
C93	249	+1387.56	–1032.5
C94	250	+1439.40	–1032.5
C95	251	+1491.24	–1032.5
C96	252	+1646.76	–1032.5
C97	253	+1698.60	–1032.5
C98	254	+1750.44	–1032.5
C99	255	+1802.28	–1032.5
C100	256	+1854.12	–1032.5
C101	257	+1905.96	–1032.5

SYMBOL	PAD	CO-ORDINATES	
		x	y
C102	258	+1957.80	–1032.5
C103	259	+2009.64	–1032.5
C104	260	+2061.48	–1032.5
C105	261	+2113.32	–1032.5
C106	262	+2165.16	–1032.5
C107	263	+2217.00	–1032.5
C108	264	+2268.84	–1032.5
C109	265	+2320.68	–1032.5
C110	266	+2372.52	–1032.5
C111	267	+2424.36	–1032.5
C112	268	+2476.20	–1032.5
C113	269	+2528.04	–1032.5
C114	270	+2579.88	–1032.5
C115	271	+2631.72	–1032.5
C116	272	+2683.56	–1032.5
C117	273	+2735.40	–1032.5
C118	274	+2787.24	–1032.5
C119	275	+2839.08	–1032.5
C120	276	+2890.92	–1032.5
C121	277	+2942.76	–1032.5
C122	278	+2994.60	–1032.5
C123	279	+3046.44	–1032.5
C124	280	+3098.28	–1032.5
C125	281	+3150.12	–1032.5
C126	282	+3201.96	–1032.5
C127	283	+3253.80	–1032.5
R0	284	+3461.16	–1032.5
R1	285	+3513.00	–1032.5
R2	286	+3564.84	–1032.5
R3	287	+3616.68	–1032.5
R4	288	+3668.52	–1032.5
R5	289	+3720.36	–1032.5
R6	290	+3772.20	–1032.5
R7	291	+3824.04	–1032.5
R8	292	+3875.88	–1032.5
R9	293	+3927.72	–1032.5
R10	294	+3979.56	–1032.5

SYMBOL	PAD	CO-ORDINATES	
		x	y
R11	295	+4031.40	–1032.5
R12	296	+4083.24	–1032.5
R13	297	+4135.08	–1032.5
R14	298	+4186.92	–1032.5
R15	299	+4238.76	–1032.5
R16	300	+4290.60	–1032.5
R17	301	+4342.44	–1032.5
R18	302	+4394.28	–1032.5
R19	303	+4446.12	–1032.5
R20	304	+4497.96	–1032.5
R21	305	+4549.80	–1032.5
R22	306	+4601.64	–1032.5
R23	307	+4653.48	–1032.5
R24	308	+4705.32	–1032.5
R25	309	+4757.16	–1032.5
R26	310	+4809	–1032.5
R27	311	+4860.84	–1032.5
R28	312	+4912.68	–1032.5
R29	313	+4964.52	–1032.5
R30	314	+5016.36	–1032.5

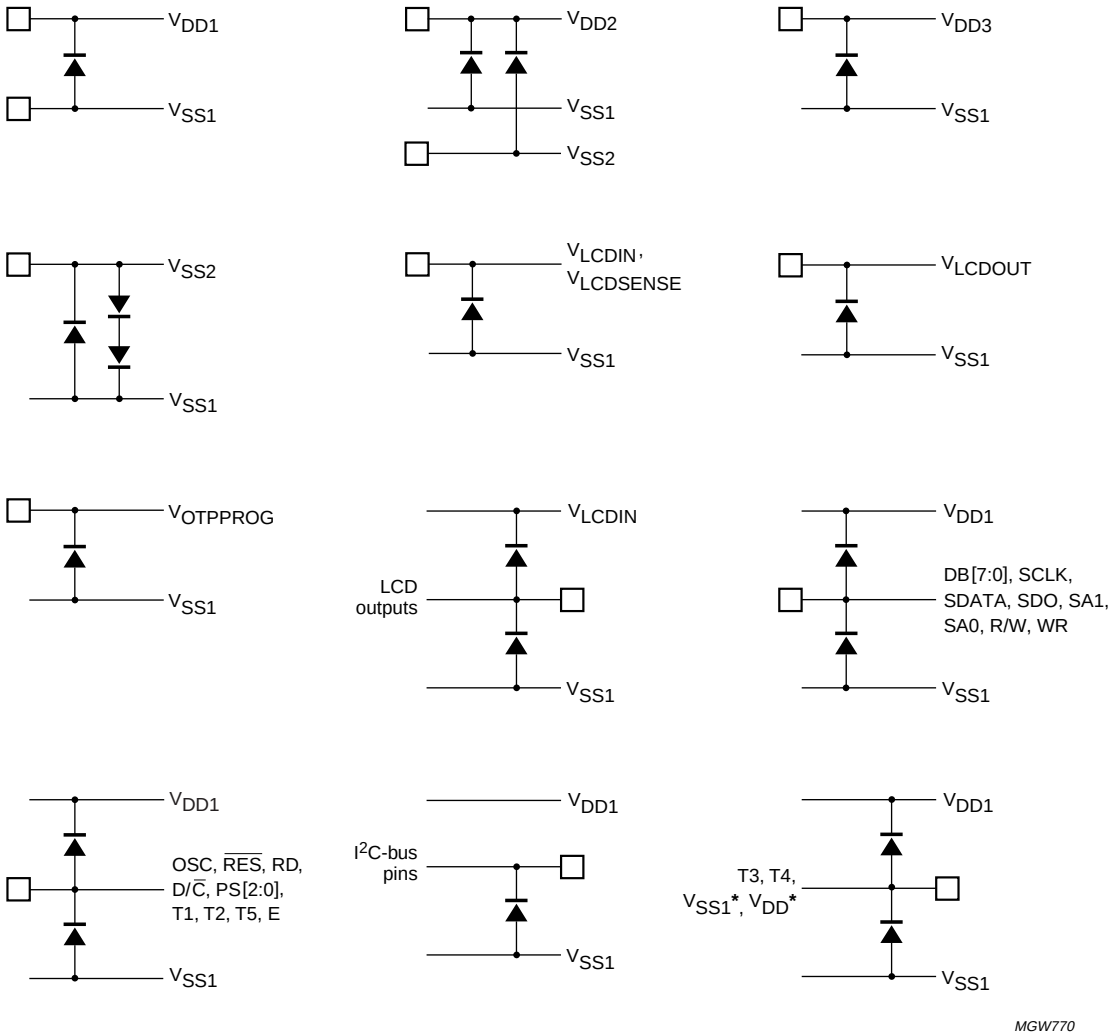
SYMBOL	PAD	CO-ORDINATES	
		x	y
R31	315	+5068.20	–1032.5
R32	316	+5120.04	–1032.5
R33	317	+5171.88	–1032.5
R34	318	+5223.72	–1032.5
R35	319	+5275.56	–1032.5
R36	320	+5327.40	–1032.5
R37	321	+5379.24	–1032.5
R38	322	+5431.08	–1032.5
R39	323	+5482.92	–1032.5
dummy	324	+5638.44	–1032.5
dummy	325	+5690.28	–1032.5
dummy	326	+5742.12	–1032.5
dummy	327	+5793.96	–1032.5
dummy	328	+5845.80	–1032.5
dummy	329	+5897.64	–1032.5
dummy	330	+5949.48	–1032.5
dummy	331	+6001.32	–1032.5
dummy	332	+6053.16	–1032.5
dummy	333	+6105.00	–1032.5



* V_{SS1*} and V_{DD1*} for local tie offs.

Fig.53 Bonding pad location (viewed from bump side).

25 DEVICE PROTECTION DIAGRAM



For test purposes only:
The maximum forward current is 5 mA.
The maximum reverse voltage is 5 V.

Fig.54 Device protection diagram.

26 TRAY INFORMATION

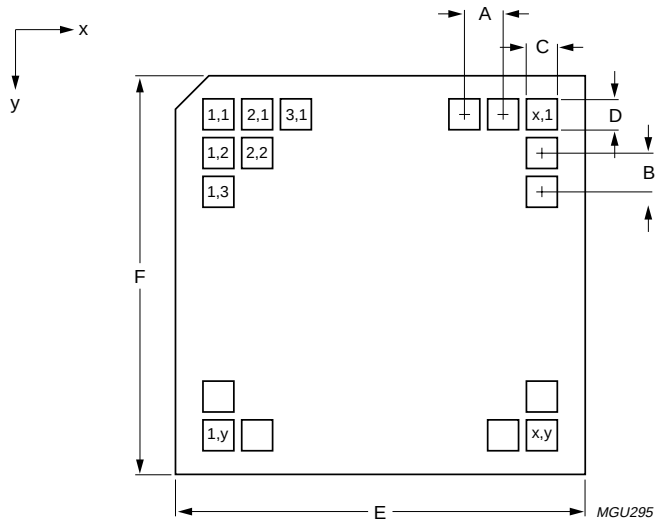
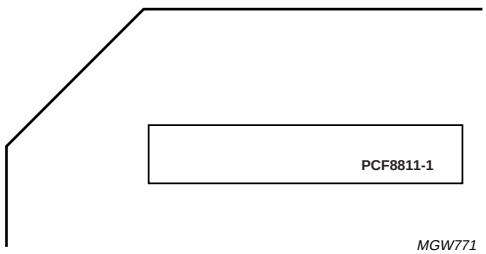


Fig.55 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientation and position of the type name on the die surface.

Fig.56 Tray alignment.

Table 30 Tray dimensions

DIM.	DESCRIPTION	VALUE
A	pocket pitch; x direction	13.77 mm
B	pocket pitch; y direction	4.45 mm
C	pocket width; x direction	12.55 mm
D	pocket width; y direction	2.41 mm
E	tray width; x direction	50.80 mm
F	tray width; y direction	50.80 mm
x	number of pockets in x direction	3
y	number of pockets in y direction	10

27 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

28 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

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For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

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