



PCF85162

Universal LCD driver for low multiplex rates

Rev. 01 — 7 January 2010

Product data sheet

1. General description

The PCF85162 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)¹ with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 32 segments. It can be cascaded for larger LCD applications. The PCF85162 is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing, and by display memory switching (static and duplex drive modes).

2. Features

- Single chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, 1/2, or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 32 segment drives:
 - ◆ Up to sixteen 7-segment alphanumeric characters
 - ◆ Up to eight 14-segment alphanumeric characters
 - ◆ Any graphics of up to 128 elements
- 32 × 4-bit RAM for display data storage
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide logic LCD supply range:
 - ◆ From 2.5 V for low-threshold LCDs
 - ◆ Up to 6.5 V for guest-host LCDs and high-threshold twisted nematic LCDs
- Low power consumption
- 400 kHz I²C-bus interface
- No external components required
- Manufactured in silicon gate CMOS process

1. The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 16](#).

3. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
PCF85162T/1	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Marking

Table 2. Marking codes

Type number	Marking code
PCF85162T/1	PCF85162T

5. Block diagram

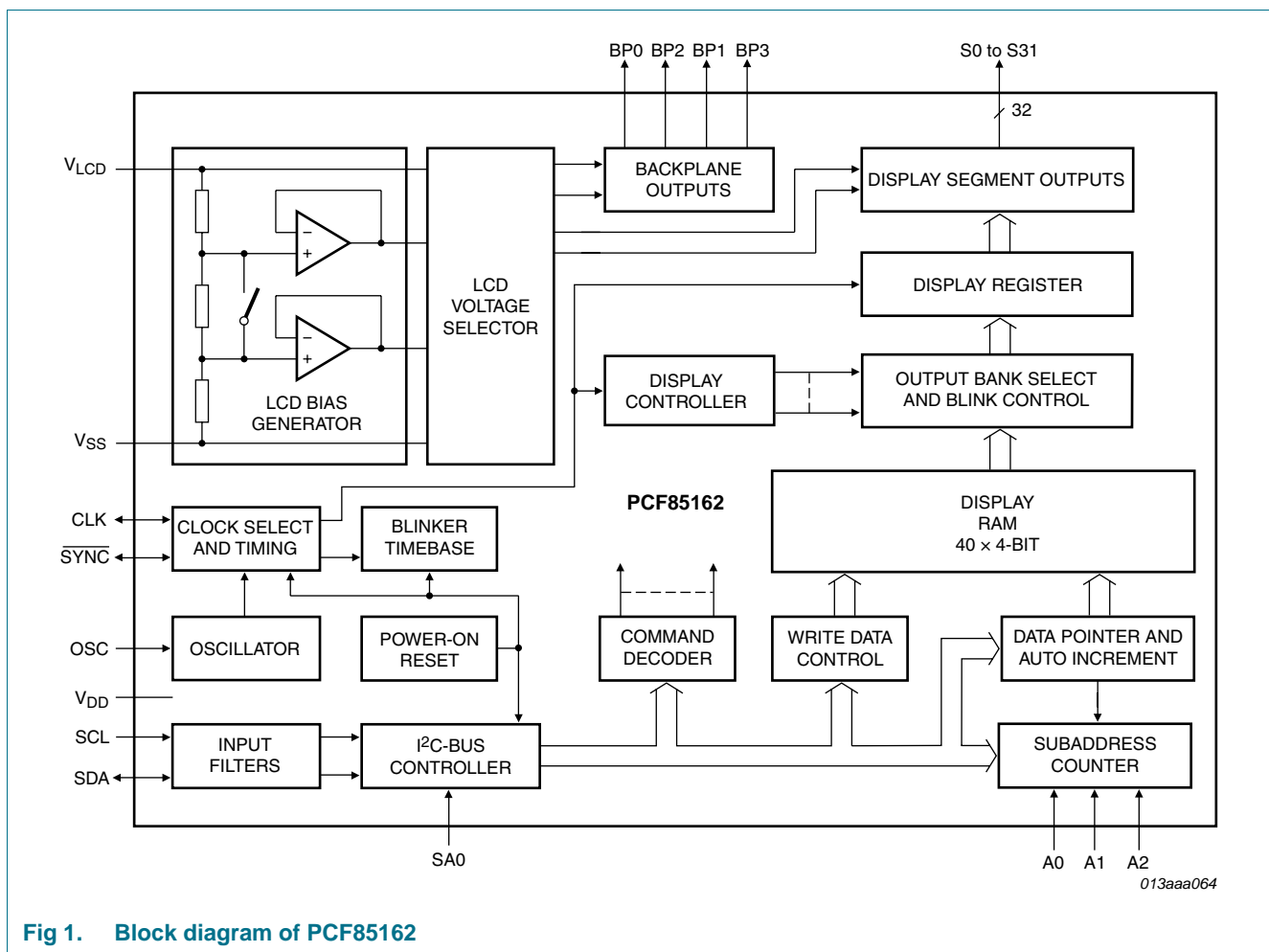
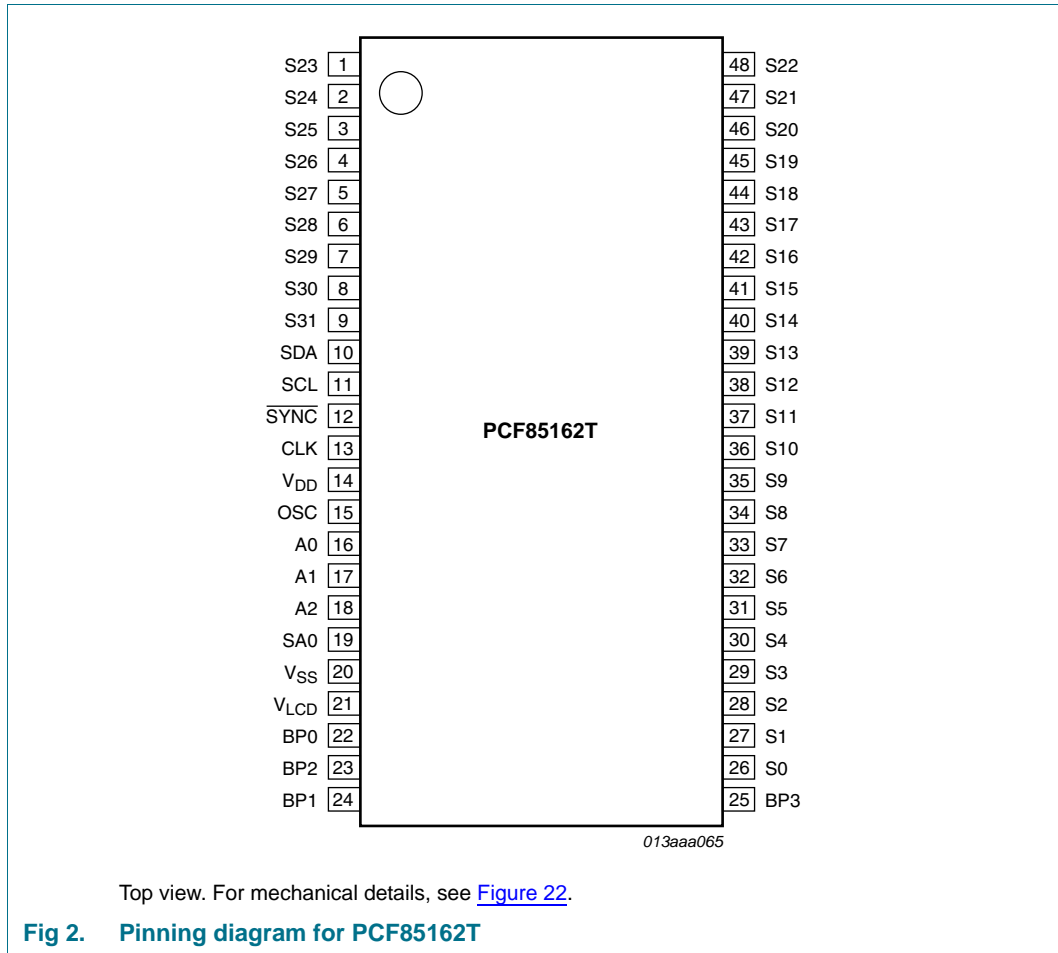


Fig 1. Block diagram of PCF85162

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SDA	10	I ² C-bus serial data input and output
SCL	11	I ² C-bus serial clock input
$\overline{\text{SYNC}}$	12	cascade synchronization input or output
CLK	13	external clock input or output
V _{DD}	14	supply voltage
OSC	15	internal oscillator enable input
A0 to A2	16 to 18	subaddress inputs
SA0	19	I ² C-bus address input
V _{SS}	20	ground supply voltage
V _{LCD}	21	LCD supply voltage
BP0 to BP3	22 to 25	LCD backplane outputs
S0 to S22, S23 to S31	26 to 48, 1 to 9	LCD segment outputs

7. Functional description

The PCF85162 is a versatile peripheral device designed to interface almost any microprocessor or microcontroller with a wide variety of LCDs. It can directly drive static or multiplexed LCD containing up to four backplanes and up to 32 segments.

The possible display configurations of the PCF85162 depend on the number of active backplane outputs required. A selection of display configurations is shown in [Table 4](#). All of these configurations can be implemented in the typical system shown in [Figure 3](#).

Table 4. Display configurations

Number of:		7-segment alphanumeric		14-segment alphanumeric		Dot matrix
Backplanes	Elements	Digits	Indicator symbols	Characters	Indicator symbols	
4	128	16	16	8	16	128 dots (4 × 32)
3	96	12	12	6	12	96 dots (3 × 32)
2	64	8	8	4	8	64 dots (2 × 32)
1	32	4	4	2	4	32 dots (1 × 32)

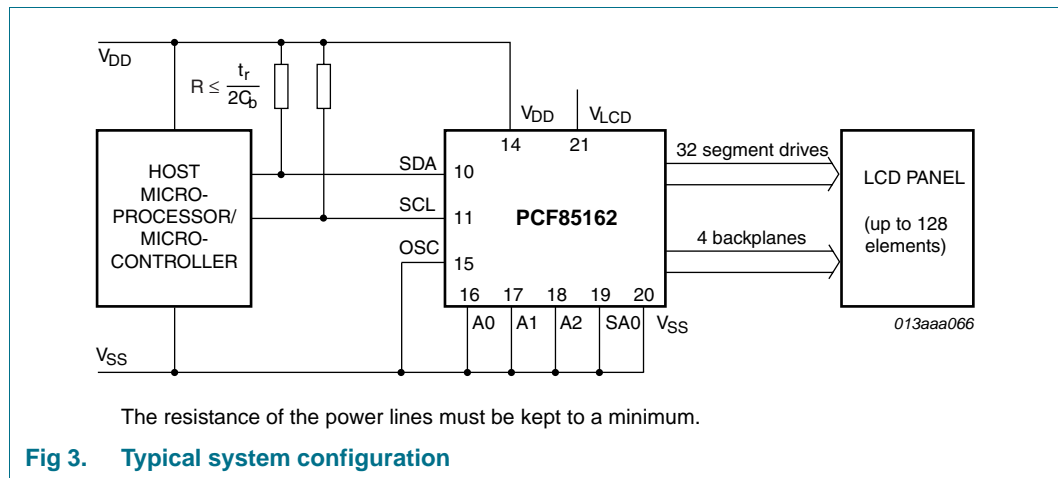


Fig 3. Typical system configuration

The host microprocessor or microcontroller maintains the 2-line I²C-bus communication channel with the PCF85162. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel chosen for the application.

7.1 Power-on reset

At power-on the PCF85162 resets to the following starting conditions:

- All backplane outputs are set to V_{LCD}
- All segment outputs are set to V_{LCD}
- The selected drive mode is: 1:4 multiplex with 1/3 bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I²C-bus interface is initialized

- The data pointer and the subaddress counter are cleared (set to logic 0)
- Display is disabled

Remark: Do not transfer data on the I²C-bus for at least 1 ms after a power-on to allow the reset action to complete.

7.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider consisting of three resistors connected in series between V_{LCD} and V_{SS}. The center resistor is bypassed by switch if the 1/2 bias voltage level for the 1:2 multiplex drive mode configuration is selected. The LCD voltage can be temperature compensated externally using the supply to pin V_{LCD}.

7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command (see [Table 10](#)) from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in [Table 5](#).

Table 5. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	1/2	0.354	0.791	2.236
1:2 multiplex	2	4	1/3	0.333	0.745	2.236
1:3 multiplex	3	4	1/3	0.333	0.638	1.915
1:4 multiplex	4	4	1/3	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating V_{off(RMS)} with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is V_{LCD} > 3V_{th}.

Multiplex drive modes of 1:3 and 1:4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for 1/2 bias

a = 2 for 1/3 bias

The RMS on-state voltage (V_{on(RMS)}) for the LCD is calculated with [Equation 1](#):

$$V_{on(RMS)} = V_{LCD} \sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \tag{1}$$

where the values for n are

- n = 1 for static drive mode
- n = 2 for 1:2 multiplex drive mode
- n = 3 for 1:3 multiplex drive mode
- n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with [Equation 2](#):

$$V_{off(RMS)} = V_{LCD} \sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from [Equation 3](#):

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a + 1)^2 + (n - 1)}{(a - 1)^2 + (n - 1)}} \quad (3)$$

Using [Equation 3](#), the discrimination for an LCD drive mode of 1:3 multiplex with $\frac{1}{2}$ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with $\frac{1}{2}$ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \left[\frac{4 \times \sqrt{3}}{3} \right] = 2.309 V_{off(RMS)}$

These compare with $V_{LCD} = 3 V_{off(RMS)}$ when $\frac{1}{3}$ bias is used.

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in [Figure 4](#).

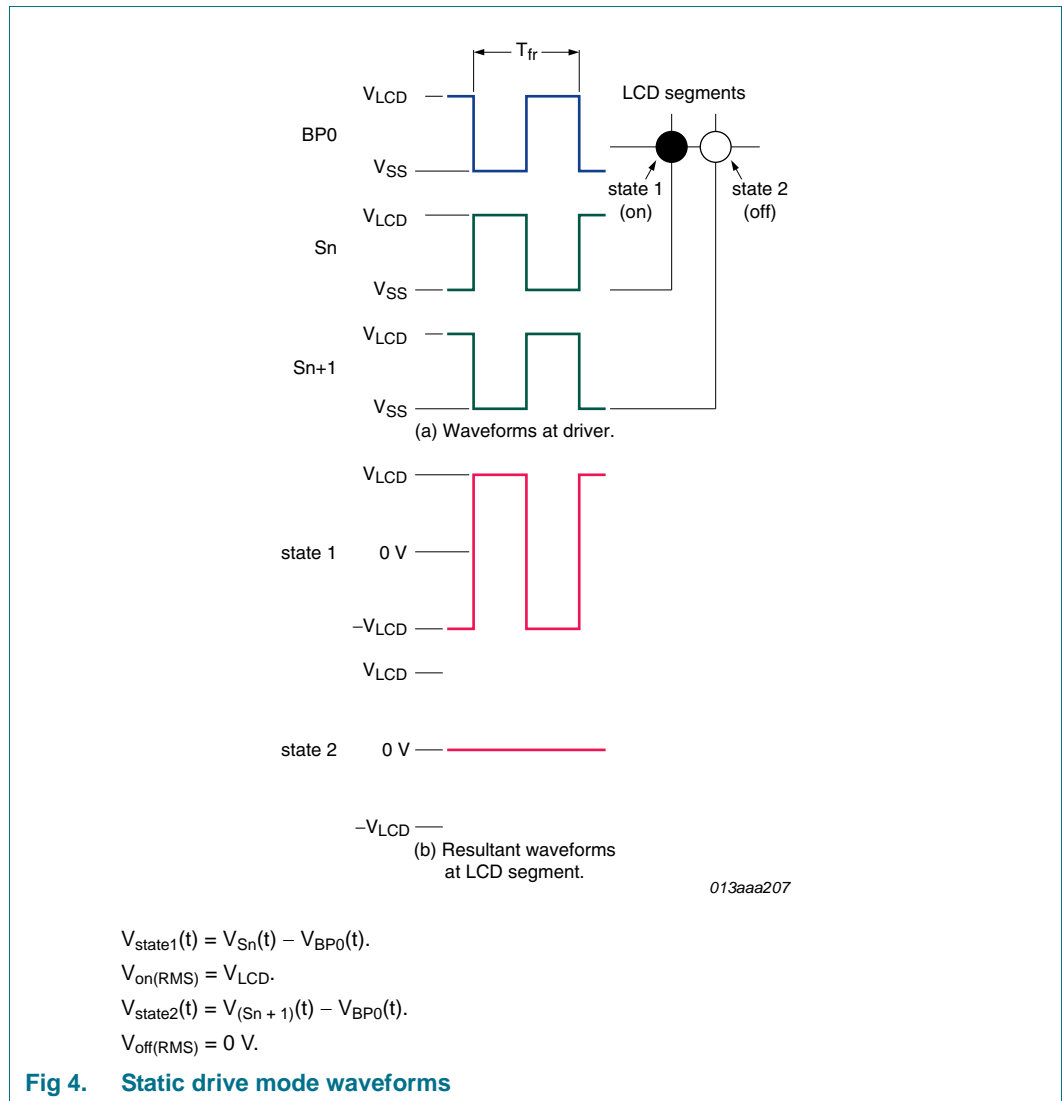


Fig 4. Static drive mode waveforms

7.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF85162 allows the use of 1/2 bias or 1/3 bias in this mode as shown in Figure 5 and Figure 6.

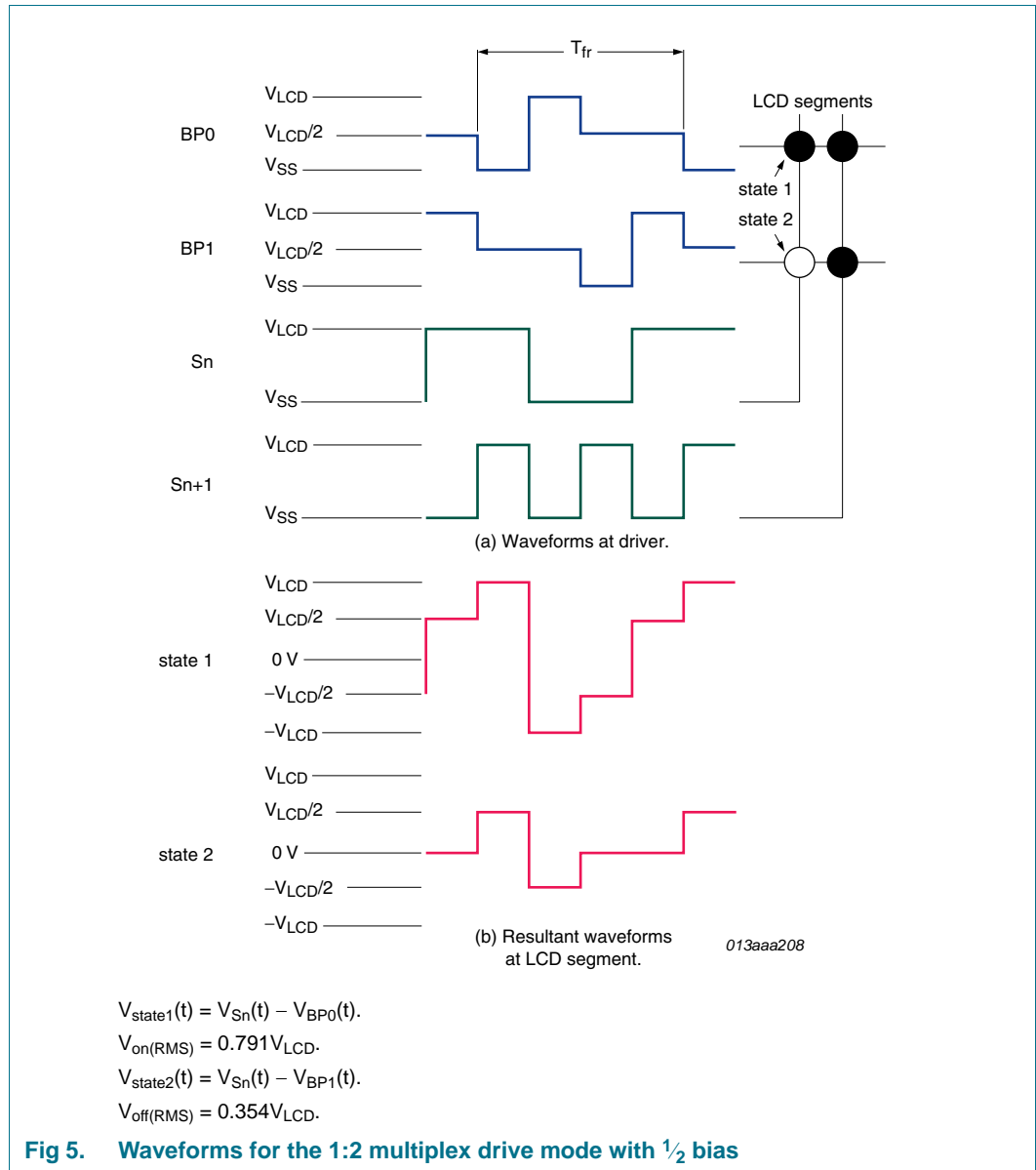


Fig 5. Waveforms for the 1:2 multiplex drive mode with 1/2 bias

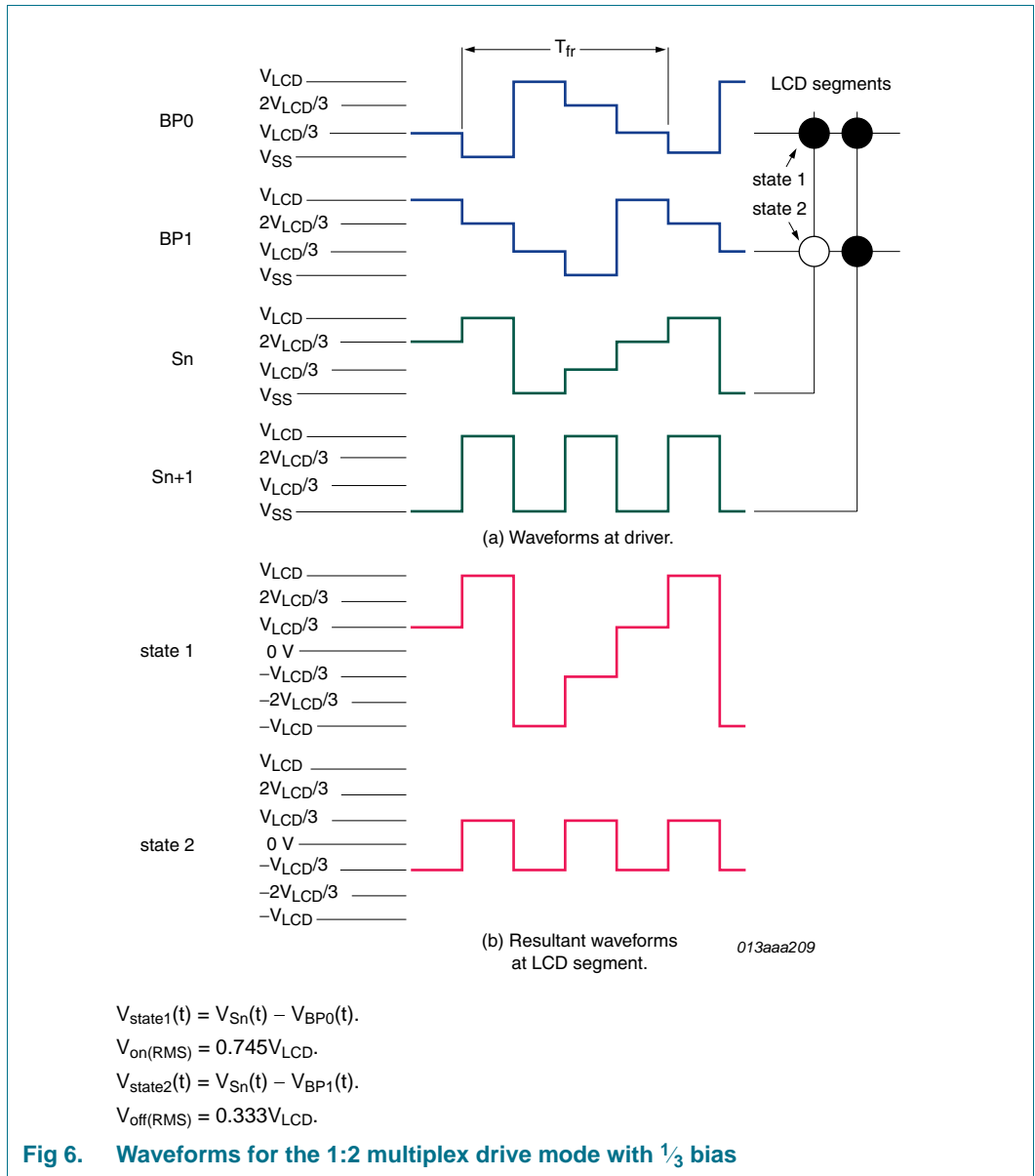
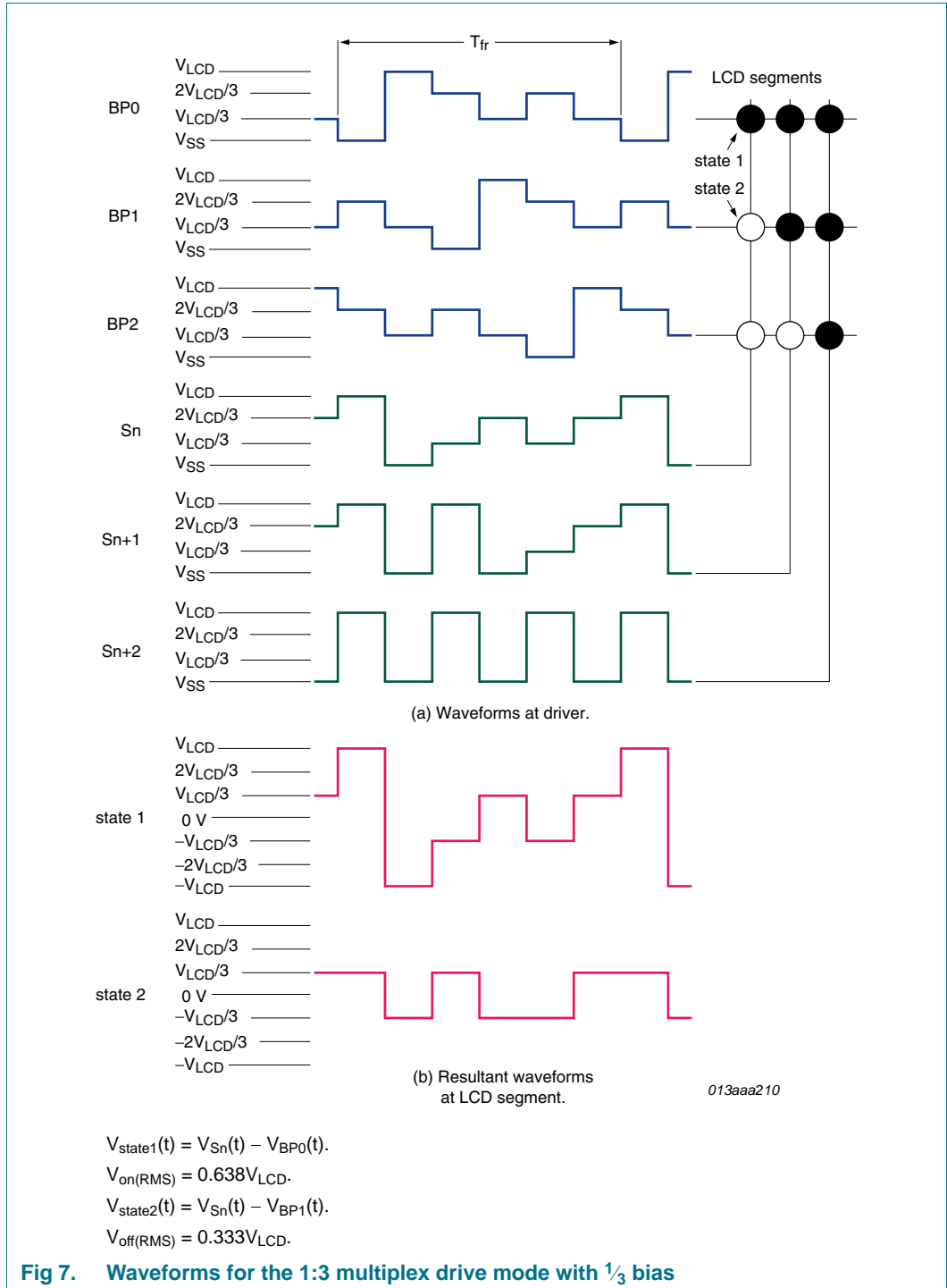


Fig 6. Waveforms for the 1:2 multiplex drive mode with 1/3 bias

7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 7.



7.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 8.

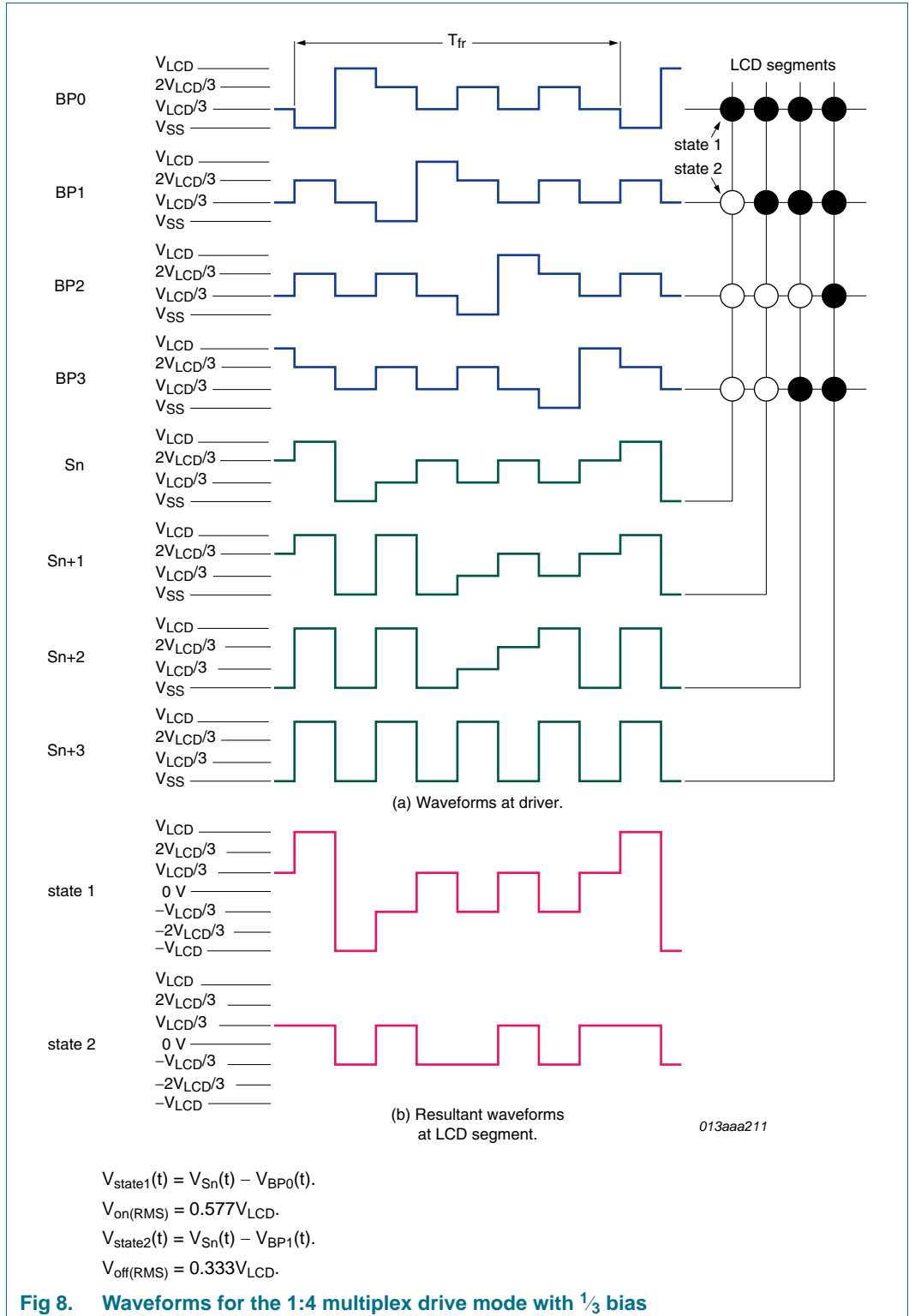


Fig 8. Waveforms for the 1:4 multiplex drive mode with 1/3 bias

7.5 Oscillator

7.5.1 Internal clock

The internal logic of the PCF85162 and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. If the internal oscillator is used, the output from pin CLK can be used as the clock signal for several PCF85162 in the system that are connected in cascade.

7.5.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}. In this case the LCD frame frequency is determined by the clock frequency (f_{clk}).

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which can damage the liquid crystals.

7.6 Timing

The PCF85162 timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each PCF85162 in the system is maintained by the synchronization signal at pin \overline{SYNC} . The timing also generates the LCD frame frequency from the clock frequency. The frame frequency is a fixed division of the

clock frequency from either the internal or an external clock: $f_{fr} = \frac{f_{clk}}{24}$

7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display register, the LCD segment outputs, and each column of the display RAM.

7.8 Segment outputs

The LCD drive section includes 32 segment outputs S0 to S31 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 32 segment outputs are required, the unused segment outputs should be left open-circuit.

7.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In the 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In the 1:2 multiplex drive mode, BP0 and BP2 respectively BP1 and BP3 carry the same signal. For increased drive capacity BP0 and BP2 respectively BP1 and BP3 may therefore be tied together.

- In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.10 Display RAM

The display RAM is a static 32 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The display RAM bit map [Figure 9](#) shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 31 which correspond with the segment outputs S0 to S31. In multiplexed LCD applications the segment data of the first, second, third, and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.

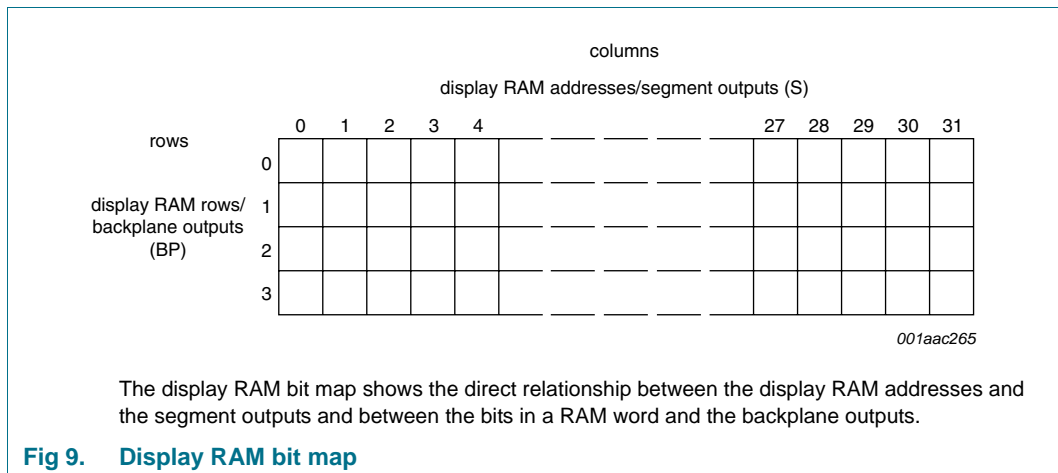


Fig 9. Display RAM bit map

When display data is transmitted to the PCF85162, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for an acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triples, or quadruples. To illustrate the filling order, an example of a 7-segment display showing all drive modes is given in [Figure 10](#); the RAM filling organization depicted applies equally to other LCD types.

drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte																																																	
static			<p>columns display RAM address/segment outputs (s) byte1</p> <table border="1"> <tr> <td></td> <td>n</td> <td>n + 1</td> <td>n + 2</td> <td>n + 3</td> <td>n + 4</td> <td>n + 5</td> <td>n + 6</td> <td>n + 7</td> </tr> <tr> <td>rows display RAM rows/backplane outputs (BP)</td> <td>0</td> <td>c</td> <td>b</td> <td>a</td> <td>f</td> <td>g</td> <td>e</td> <td>d</td> <td>DP</td> </tr> <tr> <td>1</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> </tr> <tr> <td>2</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> </tr> <tr> <td>3</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> </tr> </table>		n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7	rows display RAM rows/backplane outputs (BP)	0	c	b	a	f	g	e	d	DP	1	x	x	x	x	x	x	x	x	x	2	x	x	x	x	x	x	x	x	x	3	x	x	x	x	x	x	x	x	x	<p>MSB</p> <p>LSB</p> <p>c b a f g e d DP</p>
	n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7																																													
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2	x	x	x	x	x	x	x	x	x																																												
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2	b	g																																																			
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x = data bit unchanged.

Fig 10. Relationship between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I²C-bus

The following applies to [Figure 10](#):

- In static drive mode the eight transmitted data bits are placed in row 0 of eight successive 4-bit RAM words.
- In 1:2 multiplex mode the eight transmitted data bits are placed in pairs into row 0 and 1 of four successive 4-bit RAM words.
- In 1:3 multiplex mode the eight bits are placed in triples into row 0, 1, and 2 of three successive 4-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted.
- In the 1:4 multiplex mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 of two successive 4-bit RAM words.

7.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see [Table 11](#)). Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in [Figure 10](#). After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight.
- In 1:2 multiplex drive mode by four.
- In 1:3 multiplex drive mode by three.
- In 1:4 multiplex drive mode by two.

If an I²C-bus data access terminates early, the state of the data pointer is unknown. Consequently, the data pointer must be rewritten prior to further RAM accesses.

7.12 Subaddress counter

The storage of display data is conditioned by the content of the subaddress counter. Storage is allowed only when the content of the subaddress counter matches with the hardware subaddress applied to A0, A1, and A2. The subaddress counter value is defined by the device-select command (see [Table 12](#)). If the content of the subaddress counter and the hardware subaddress do not match, then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

In cascaded applications each PCF85162 in the cascade must be addressed separately. Initially, the first PCF85162 is selected by sending the device-select command matching the first device's hardware subaddress. Then the data pointer is set to the preferred display RAM address by sending the load-data-pointer command.

Once the display RAM of the first PCF85162 has been written, the second PCF85162 is selected by sending the device-select command again. This time however the command matches the second device's hardware subaddress. Next the load-data-pointer command is sent to select the preferred display RAM address of the second PCF85162.

This last step is very important because during writing data to the first PCF85162, the data pointer of the second PCF85162 is incremented. In addition, the hardware subaddress should not be changed whilst the device is being accessed on the I²C-bus interface.

7.13 Output bank selector

The output bank selector (see [Table 13](#)) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, 2, and then 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The PCF85162 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command can be used to select the contents of row 2 instead of the contents of row 0 to be displayed. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

7.14 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command (see [Table 13](#)). The input bank selector functions independently to the output bank selector.

7.15 Blinker

The display blinking capabilities of the PCF85162 are very versatile. The whole display can blink at a frequencies selected by the blink-select command (see [Table 14](#)). The blink frequencies are fractions of the clock frequency. The ratio between the clock and blink frequencies depends on the blink mode selected (see [Table 6](#)).

An additional feature is for an arbitrary selection of LCD elements to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternative RAM bank is available, groups of LCD elements can blink by selectively changing the display RAM data at fixed time intervals.

Table 6. Blink frequencies^[1]

Blink mode	Blink frequency equation	Blink frequency range			Unit
		Min $f_{clk} = 960 \text{ Hz}$	Typ $f_{clk} = 1970 \text{ Hz}$	Max $f_{clk} = 2640 \text{ Hz}$	
off	-	blinking off			-
1	$f_{blink} = \frac{f_{clk}}{768}$	1.25	2.57	3.44	Hz
2	$f_{blink} = \frac{f_{clk}}{1536}$	0.63	1.28	1.72	Hz
3	$f_{blink} = \frac{f_{clk}}{3072}$	0.31	0.64	0.86	Hz

[1] The blink frequency is proportional to the oscillator frequency (f_{clk}). For the range of the oscillator frequency see [Table 17](#).

The entire display can blink at a frequency other than the nominal blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see [Table 10](#)).

7.16 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data Line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.16.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see [Figure 11](#)).

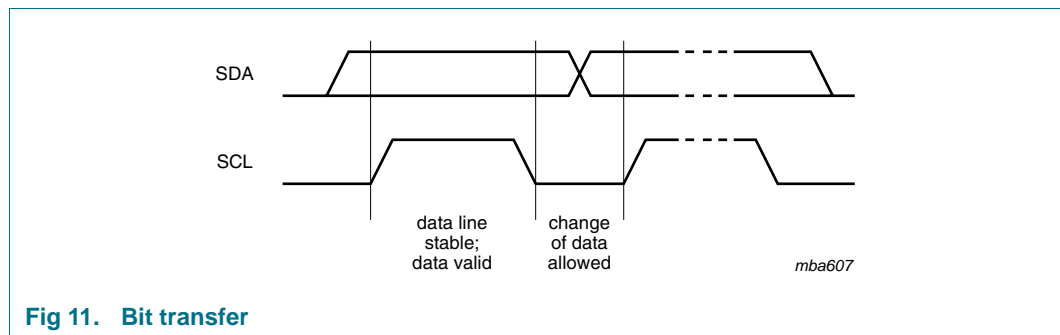


Fig 11. Bit transfer

7.16.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S).

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 12](#)).

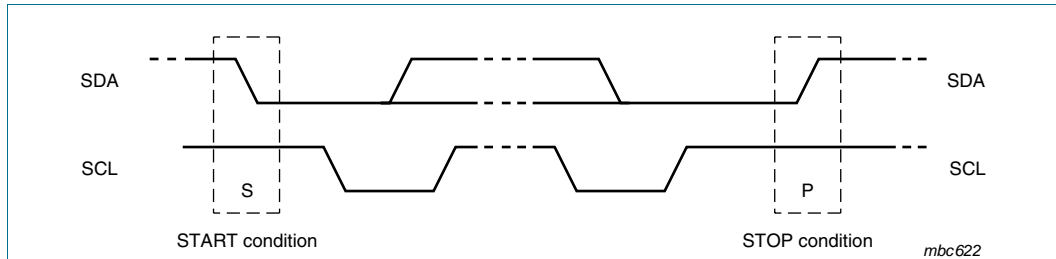


Fig 12. Definition of START and STOP conditions

7.16.3 System configuration

A device which sends data to the bus is a transmitter, a device which receives data from the bus is a receiver. The device which initiates and terminates a transfer is the master; and the devices which are addressed by the master are the slaves (see [Figure 13](#)).

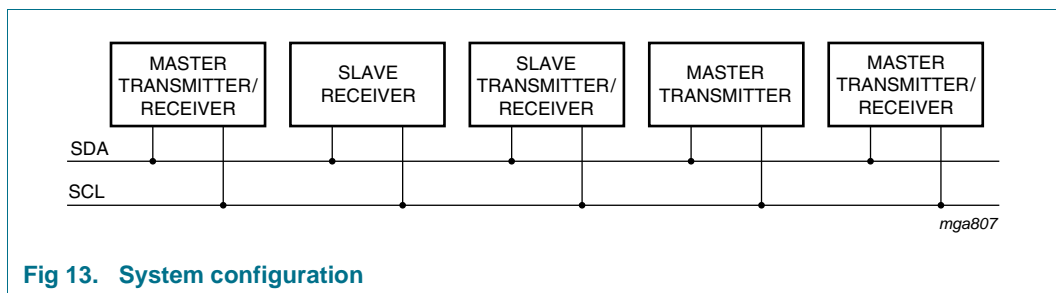


Fig 13. System configuration

7.16.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I²C-bus is illustrated in [Figure 14](#).

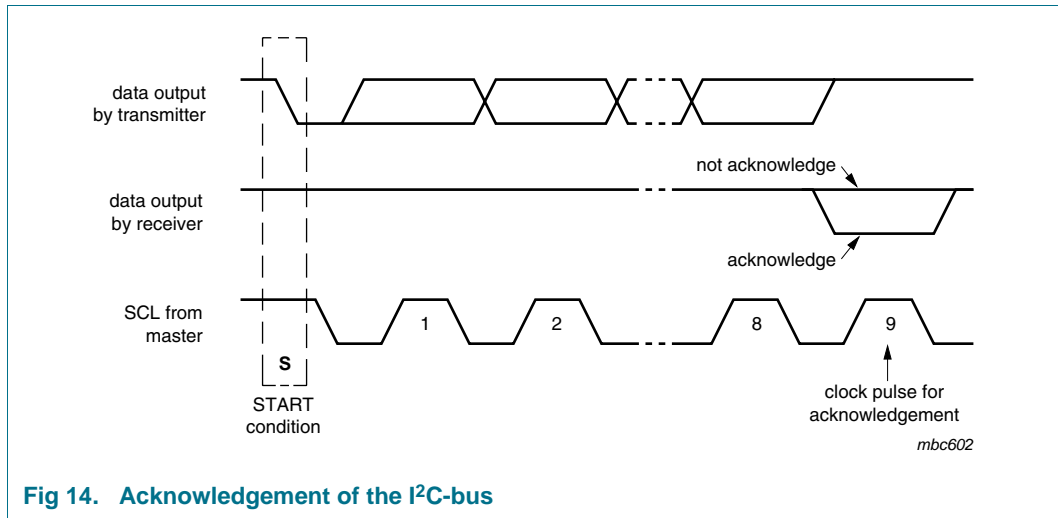


Fig 14. Acknowledgement of the I²C-bus

7.16.5 I²C-bus controller

The PCF85162 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF85162 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, the transferred command data and the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1, and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1, and A2 are tied to V_{SS} or V_{DD} using a binary coding scheme, so that no two devices with a common I²C-bus slave address have the same hardware subaddress.

7.16.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.16.7 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are used to address the PCF85162. The entire I²C-bus slave address byte is shown in [Table 7](#).

Table 7. I²C slave address byte

Bit	Slave address							0 LSB
	7 MSB	6	5	4	3	2	1	
	0	1	1	1	0	0	SA0	R/W

The PCF85162 is a write-only device and will not respond to a read access, therefore bit 0 should always be logic 0. Bit 1 of the slave address byte, that a PCF85162 will respond to, is defined by the level tied to its SA0 input (V_{SS} for logic 0 and V_{DD} for logic 1).

Having two reserved slave addresses allows the following on the same I²C-bus:

- Up to 16 PCF85162 for very large LCD applications
- The use of two types of LCD multiplex drive modes

The I²C-bus protocol is shown in [Figure 15](#). The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of two possible PCF85162 slave addresses available. All PCF85162 whose SA0 inputs correspond to bit 0 of the slave address respond by asserting an acknowledge in parallel. This I²C-bus transfer is ignored by all PCF85162 whose SA0 inputs are set to the alternative level.

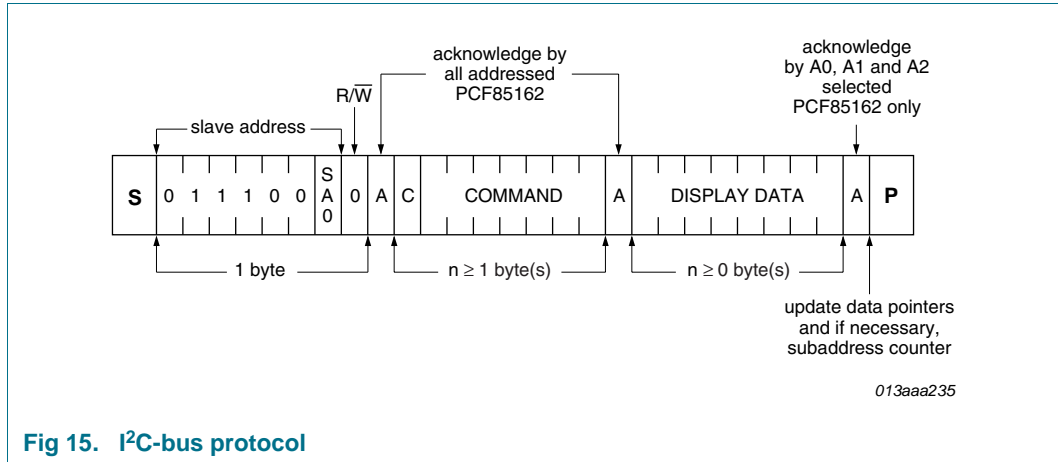


Fig 15. I²C-bus protocol

After an acknowledgement, one or more command bytes follow, that define the status of each addressed PCF85162.

The last command byte sent is identified by the continuation bit C set logic 0 (see [Figure 16](#)). The command bytes are also acknowledged by all addressed PCF85162 on the bus.

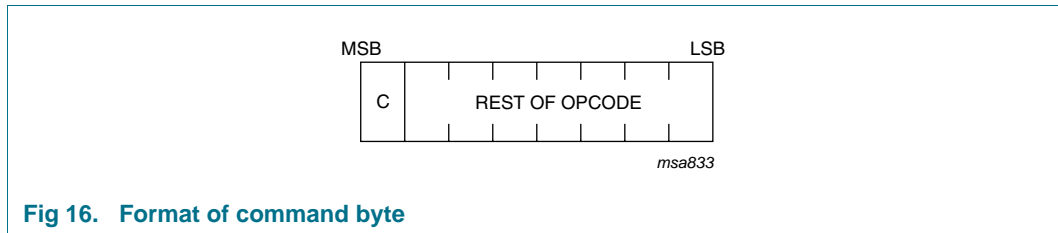


Fig 16. Format of command byte

After the last command byte, one or more display data bytes may follow. Display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data directed to the intended PCF85162 device.

An acknowledgement after each byte is asserted only by the PCF85162 that are addressed via address lines A0, A1, and A2. After the last display byte, the I²C-bus master asserts a STOP condition (P). Alternately a START may be asserted to restart an I²C-bus access.

7.17 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus.

The commands available to the PCF85162 are defined in [Table 8](#).

Table 8. Definition of PCF85162 commands

Bit position labeled as - is not used.

Command	Operation Code								Reference
	7	6	5	4	3	2	1	0	
mode-set	C	1	0	-	E	B	M1	M0	Table 10
load-data-pointer	C	0	0	P4	P3	P2	P1	P0	Table 11
device-select	C	1	1	0	0	A2	A1	A0	Table 12
bank-select	C	1	1	1	1	0	I	O	Table 13
blink-select	C	1	1	1	0	A	BF1	BF0	Table 14

All available commands carry a continuation bit C in their most significant bit position as shown in [Figure 16](#). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data (see [Table 9](#)).

Table 9. C bit description

Bit	Symbol	Value	Description
7	C		continue bit
		0	last control byte in the transfer; next byte will be regarded as display data
		1	control bytes continue; next byte will be a command too

Table 10. Mode-set command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 9
6 to 5	-	10	fixed value
4	-	-	unused
3	E		display status
		0	disabled (blank) ^[1]
		1	enabled
2	B		LCD bias configuration
		0	1/3 bias
		1	1/2 bias
1 to 0	M[1:0]		LCD drive mode selection
		01	static; BP0
		10	1:2 multiplex; BP0, BP1
		11	1:3 multiplex; BP0, BP1, BP2
		00	1:4 multiplex; BP0, BP1, BP2, BP3

[1] The possibility to disable the display allows implementation of blinking under external control.

Table 11. Load-data-pointer command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 9
6 to 5	-	00	fixed value
4 to 0	P[4:0]	00000 to 11111	5 bit binary value, 0 to 31; transferred to the data pointer to define one of 32 display RAM addresses

Table 12. Device-select command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 9
6 to 3	-	1100	fixed value
2 to 0	A[2:0]	000 to 111	3 bit binary value, 0 to 7; transferred to the subaddress counter to define one of eight hardware subaddresses

Table 13. Bank-select command bit description

Bit	Symbol	Value	Description	
			Static	1:2 multiplex ^[1]
7	C	0, 1	see Table 9	
6 to 2	-	11110	fixed value	
1	I		input bank selection ; storage of arriving display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3
0	O		output bank selection ; retrieval of LCD display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

Table 14. Blink-select command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 9
6 to 3	-	1110	fixed value
2	A		blink mode selection
		0	normal blinking ^[1]
		1	alternate RAM bank blinking ^[2]
1 to 0	BF[1:0]		blink frequency selection
		00	off
		01	1
		10	2
		11	3

[1] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[2] Alternating RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

7.18 Display controller

The display controller executes the commands identified by the command decoder. It contains the device's status registers and coordinates their effects. The display controller is also responsible for loading display data into the display RAM in the correct filling order.

8. Internal circuitry

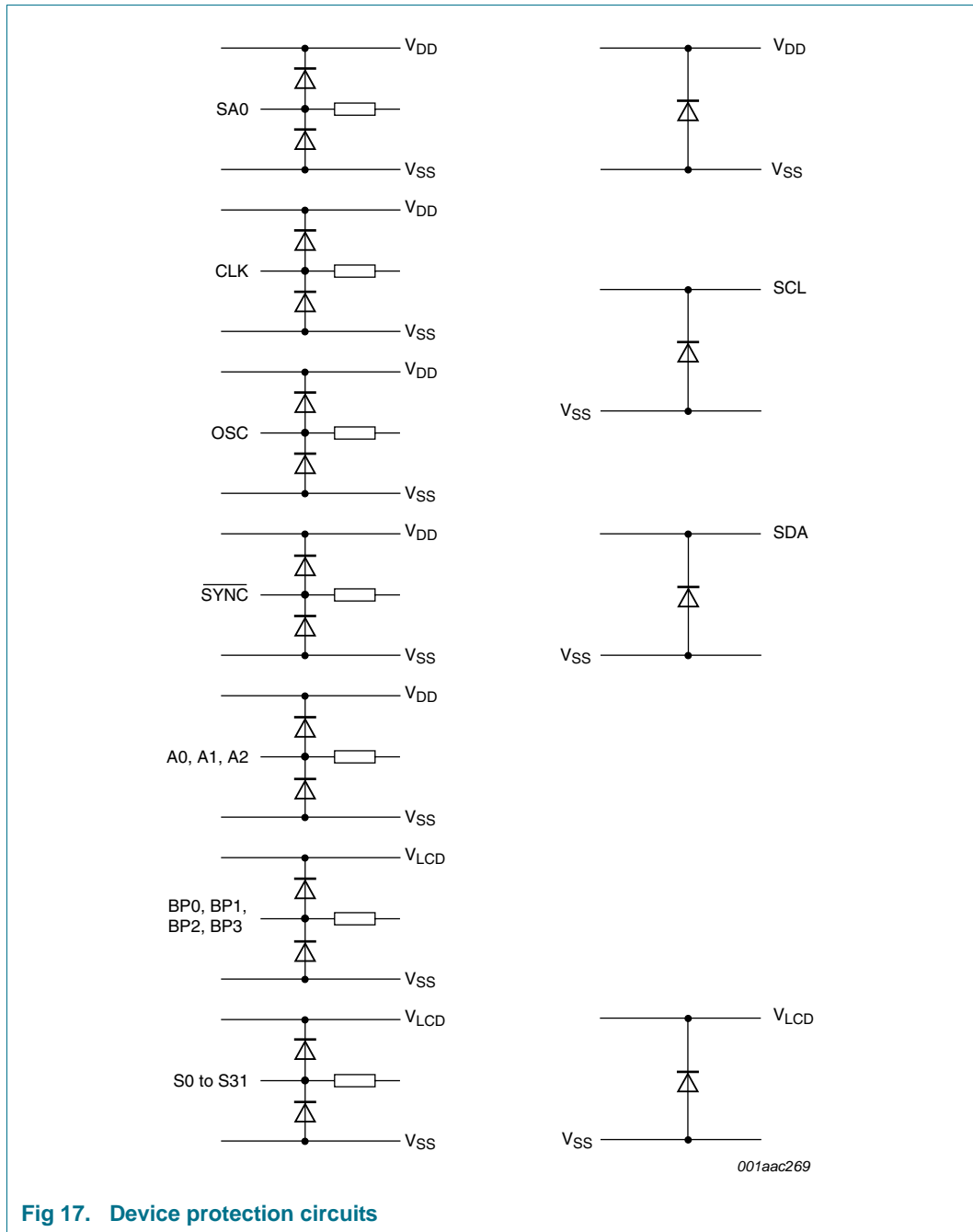


Fig 17. Device protection circuits

9. Limiting values

CAUTION



Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

Table 15. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DD}	supply voltage		-0.5	+6.5	V	
V_{LCD}	LCD supply voltage		-0.5	+7.5	V	
V_I	input voltage	on each of the pins CLK, SDA, SCL, SYNC, SA0, OSC, A0 to A2	-0.5	+6.5	V	
V_O	output voltage	on each of the pins S0 to S31, BP0 to BP3	-0.5	+7.5	V	
I_I	input current		-10	+10	mA	
I_O	output current		-10	+10	mA	
I_{DD}	supply current		-50	+50	mA	
$I_{DD(LCD)}$	LCD supply current		-50	+50	mA	
I_{SS}	ground supply current		-50	+50	mA	
P_{tot}	total power dissipation		-	400	mW	
P_o	output power		-	100	mW	
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±3500	V
		CDM	[2]	-	±1500	V
I_{lu}	latch-up current		[3]	-	100	mA
T_{stg}	storage temperature		[4]	-65	+150	°C

[1] Pass level; Human Body Model (HBM), according to [Ref. 5 "JESD22-A114"](#).

[2] Pass level; Charged-Device Model (CDM), according to [Ref. 6 "JESD22-C101"](#).

[3] Pass level; latch-up testing according to [Ref. 7 "JESD78"](#) at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the NXP store and transport requirements (see [Ref. 9 "NX3-00092"](#)) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

10. Static characteristics

Table 16. Static characteristics

$V_{DD} = 1.8\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $V_{LCD} = 2.5\text{ V to }6.5\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		1.8	-	5.5	V
V_{LCD}	LCD supply voltage	[1]	2.5	-	6.5	V
I_{DD}	supply current	$f_{clk(ext)} = 1536\text{ Hz}$	[2]	8	20	μA
$I_{DD(LCD)}$	LCD supply current	$f_{clk(ext)} = 1536\text{ Hz}$	[2]	24	60	μA
Logic						
$V_{P(POR)}$	power-on reset supply voltage		1.0	1.3	1.6	V
V_{IL}	LOW-level input voltage	on pins CLK, $\overline{\text{SYNC}}$, OSC, A0 to A2, SA0, SCL, SDA	V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	on pins CLK, $\overline{\text{SYNC}}$, OSC, A0 to A2, SA0, SCL, SDA	[3]	$0.7V_{DD}$	-	V_{DD}
I_{OL}	LOW-level output current	output sink current; $V_{OL} = 0.4\text{ V}$; $V_{DD} = 5\text{ V}$				
		on pins CLK and $\overline{\text{SYNC}}$	1	-	-	mA
		on pin SDA	3	-	-	mA
$I_{OH(CLK)}$	HIGH-level output current on pin CLK	output source current; $V_{OH} = 4.6\text{ V}$; $V_{DD} = 5\text{ V}$	1	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS} ; on pins CLK, SCL, SDA, A0 to A2, and SA0	-1	-	+1	μA
$I_{L(OSC)}$	leakage current on pin OSC	$V_I = V_{DD}$	-1	-	+1	μA
C_I	input capacitance	[4]	-	-	7	pF
LCD outputs						
ΔV_O	output voltage variation	on pins BP0 - BP3 and S0 - S31	-100	-	+100	mV
R_O	output resistance	$V_{LCD} = 5\text{ V}$	[5]			
		on pins BP0 to BP3	-	1.5	-	$\text{k}\Omega$
		on pins S0 to S31	-	6.0	-	$\text{k}\Omega$

[1] $V_{LCD} > 3\text{ V}$ for $\frac{1}{3}$ bias.

[2] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD} ; external clock with 50 % duty factor; I²C-bus inactive.

[3] I²C pins SCL and SDA have no diode to V_{DD} and when tested may therefore be driven to the V_I limiting values given in [Table 15](#) (see also [Figure 17](#)).

[4] Periodically sampled, not 100 % tested.

[5] Outputs measured one at a time.

11. Dynamic characteristics

Table 17. Dynamic characteristics

$V_{DD} = 1.8\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $V_{LCD} = 2.5\text{ V to }6.5\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock						
$f_{\text{clk(int)}}$	internal clock frequency	[1]	1440	1970	2640	Hz
$f_{\text{clk(ext)}}$	external clock frequency		960	-	2640	Hz
$t_{\text{clk(H)}}$	HIGH-level clock time		60	-	-	μs
$t_{\text{clk(L)}}$	LOW-level clock time		60	-	-	μs
Synchronization						
$t_{\text{PD(SYNC_N)}}$	$\overline{\text{SYNC}}$ propagation delay		-	30	-	ns
$t_{\text{SYNC_NL}}$	$\overline{\text{SYNC}}$ LOW time		1	-	-	μs
$t_{\text{PD(drv)}}$	driver propagation delay	$V_{\text{LCD}} = 5\text{ V}$ [2]	-	-	30	μs
I²C-bus[3]						
Pin SCL						
f_{SCL}	SCL clock frequency		-	-	400	kHz
t_{LOW}	LOW period of the SCL clock		1.3	-	-	μs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	μs
Pin SDA						
$t_{\text{SU;DAT}}$	data set-up time		100	-	-	ns
$t_{\text{HD;DAT}}$	data hold time		0	-	-	ns
Pins SCL and SDA						
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	μs
$t_{\text{SU;STO}}$	set-up time for STOP condition		0.6	-	-	μs
$t_{\text{HD;STA}}$	hold time (repeated) START condition		0.6	-	-	μs
$t_{\text{SU;STA}}$	set-up time for a repeated START condition		0.6	-	-	μs
t_{r}	rise time of both SDA and SCL signals	$f_{\text{SCL}} = 400\text{ kHz}$	-	-	0.3	μs
		$f_{\text{SCL}} < 125\text{ kHz}$	-	-	1.0	μs
t_{f}	fall time of both SDA and SCL signals		-	-	0.3	μs
C_{b}	capacitive load for each bus line		-	-	400	pF
$t_{\text{w(spike)}}$	spike pulse width	on the I ² C-bus	-	-	50	ns

[1] Typical output duty factor: 50 % measured at the CLK output pin.

[2] Not tested in production.

[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD} .

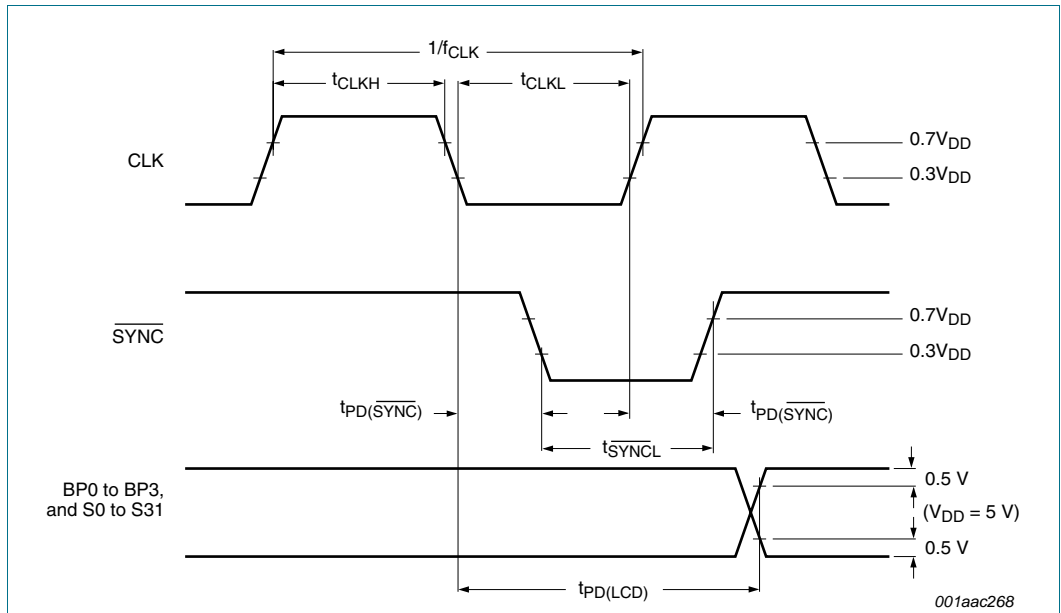


Fig 18. Driver timing waveforms

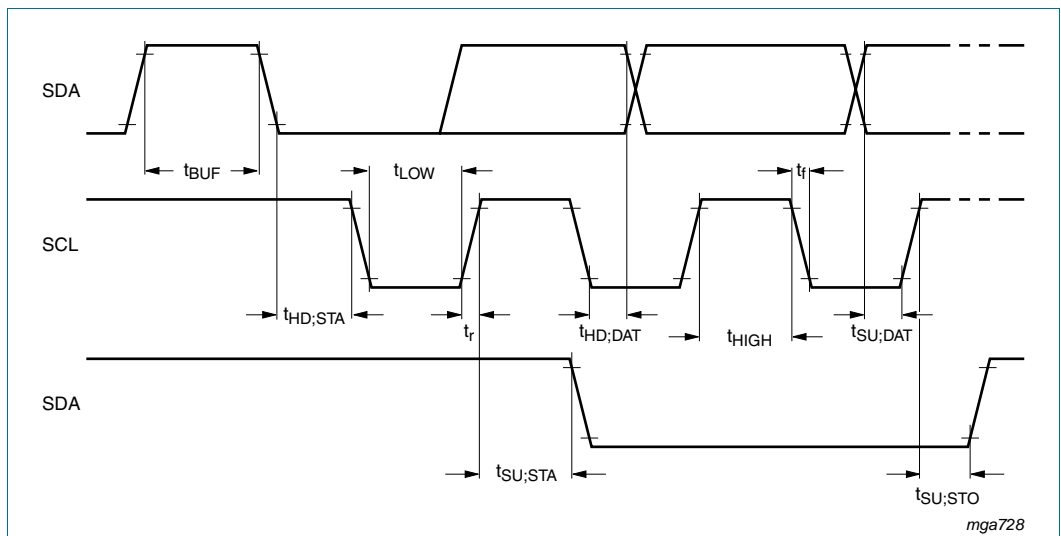


Fig 19. I²C-bus timing waveforms

12. Application information

12.1 Cascaded operation

The PCF85162 allows to be cascaded to drive larger display configurations with up to 16 PCF85162 devices on the same I²C-bus. In such a configuration, if no external clock source is used, one PCF85162 must act as the clock master, generating the clock, whereas all remaining PCF85162 in the cascade must act as clock slaves, receiving the clock from the master (see [Figure 20](#)). Alternatively, if an external clock source is used, all PCF85162 in the cascade must act as clock slaves, receiving the clock from the external clock source.

A PCF85162 is configured as a clock master by connecting pin OSC to V_{SS} (see [Section 7.5.1](#)). In this case the internal oscillator of the PCF85162 is generating the clock signal which is output on pin CLK.

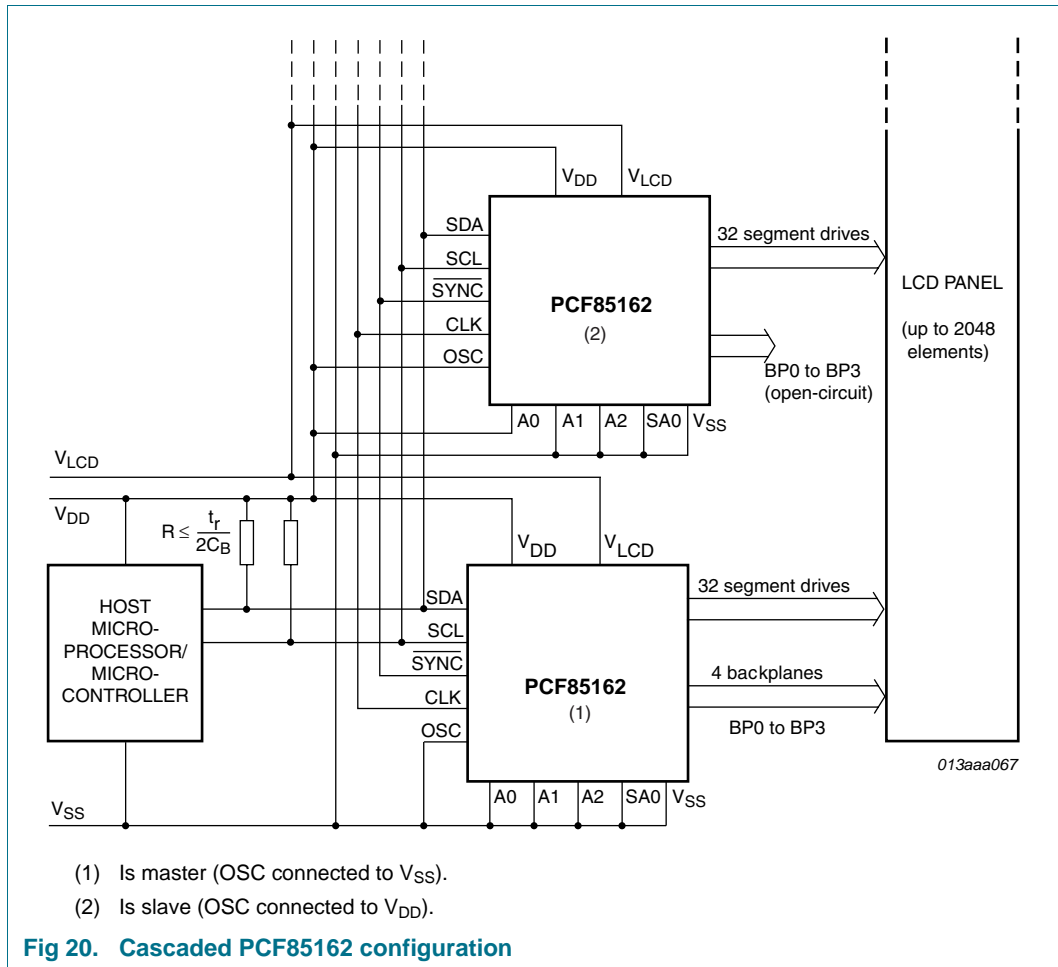
The other way round a PCF85162 is configured as clock slave by connecting pin OSC to V_{DD} (see [Section 7.5.2](#)). In this case the PCF85162 is expecting a clock signal on pin CLK.

Up to 16 PCF85162 can be distinguished by using the 3-bit hardware subaddress (A0, A1, and A2) and the programmable I²C-bus slave address (SA0).

Table 18. Addressing cascaded PCF85162

Cluster	Bit SA0	Pin A2	Pin A1	Pin A0	Device
1	0	0	0	0	0
		0	0	1	1
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
2	1	0	0	0	8
		0	0	1	9
		0	1	0	10
		0	1	1	11
		1	0	0	12
		1	0	1	13
		1	1	0	14
		1	1	1	15

When cascaded PCF85162 are synchronized, they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF85162 of the cascade contribute additional segment outputs, but their backplane outputs are left open-circuit (see [Figure 20](#)).



The SYNC line of all PCF85162 in the cascade must be connected to maintain the correct synchronization between all cascaded PCF85162. Synchronization is guaranteed after a Power-On Reset (POR). The only time that SYNC is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments or by defining a multiplex drive mode when PCF85162 with different SA0 levels are cascaded).

SYNC is organized as an input/output pin. The output selection is realized as an open-drain driver with an internal pull-up resistor. A PCF85162 asserts the SYNC line at the onset of its last active backplane signal and monitors the SYNC line at all other times. If synchronization in the cascade is lost, it is restored by the first PCF85162 to assert SYNC. The timing relationship between the backplane waveforms and the SYNC signal for the various drive modes of the PCF85162 are shown in [Figure 21](#).

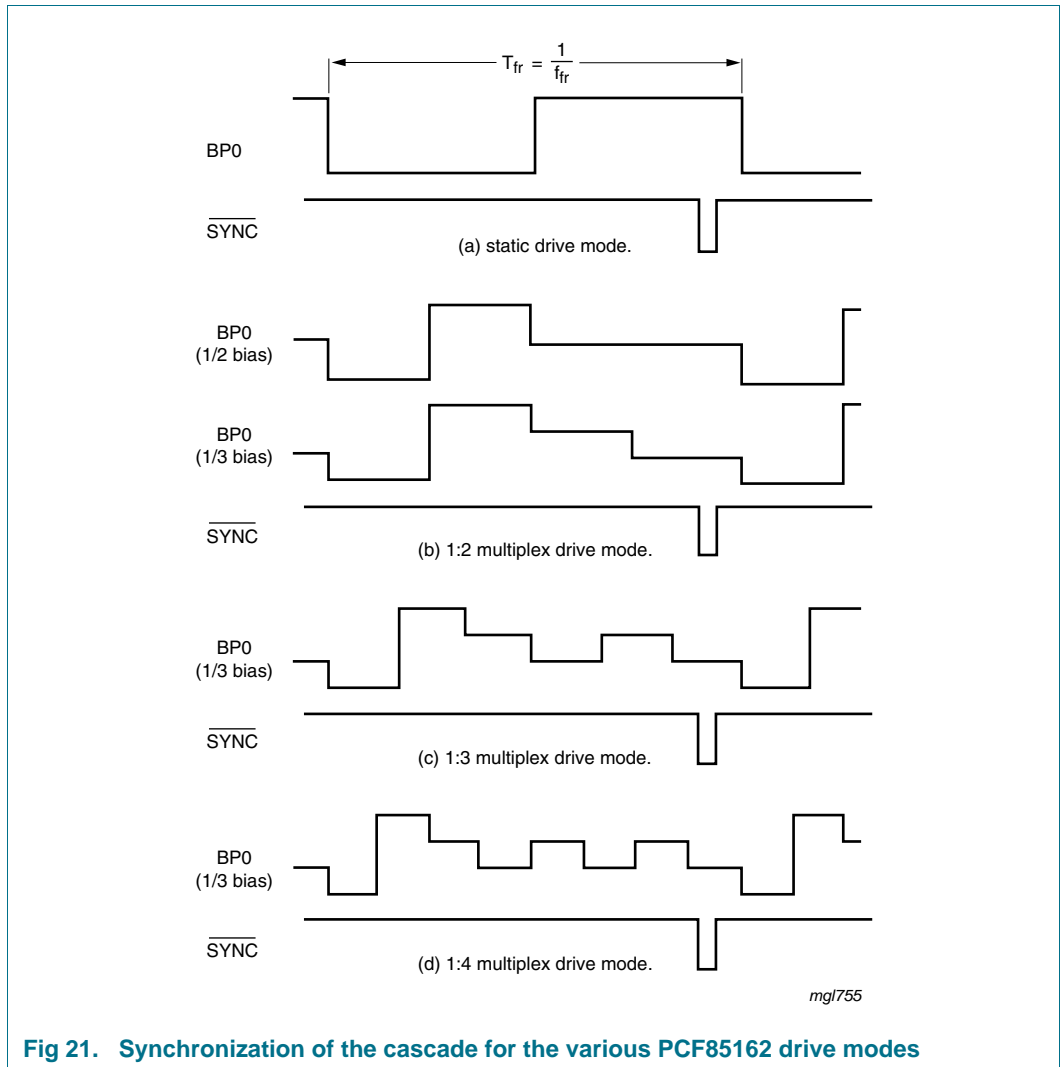


Fig 21. Synchronization of the cascade for the various PCF85162 drive modes

13. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

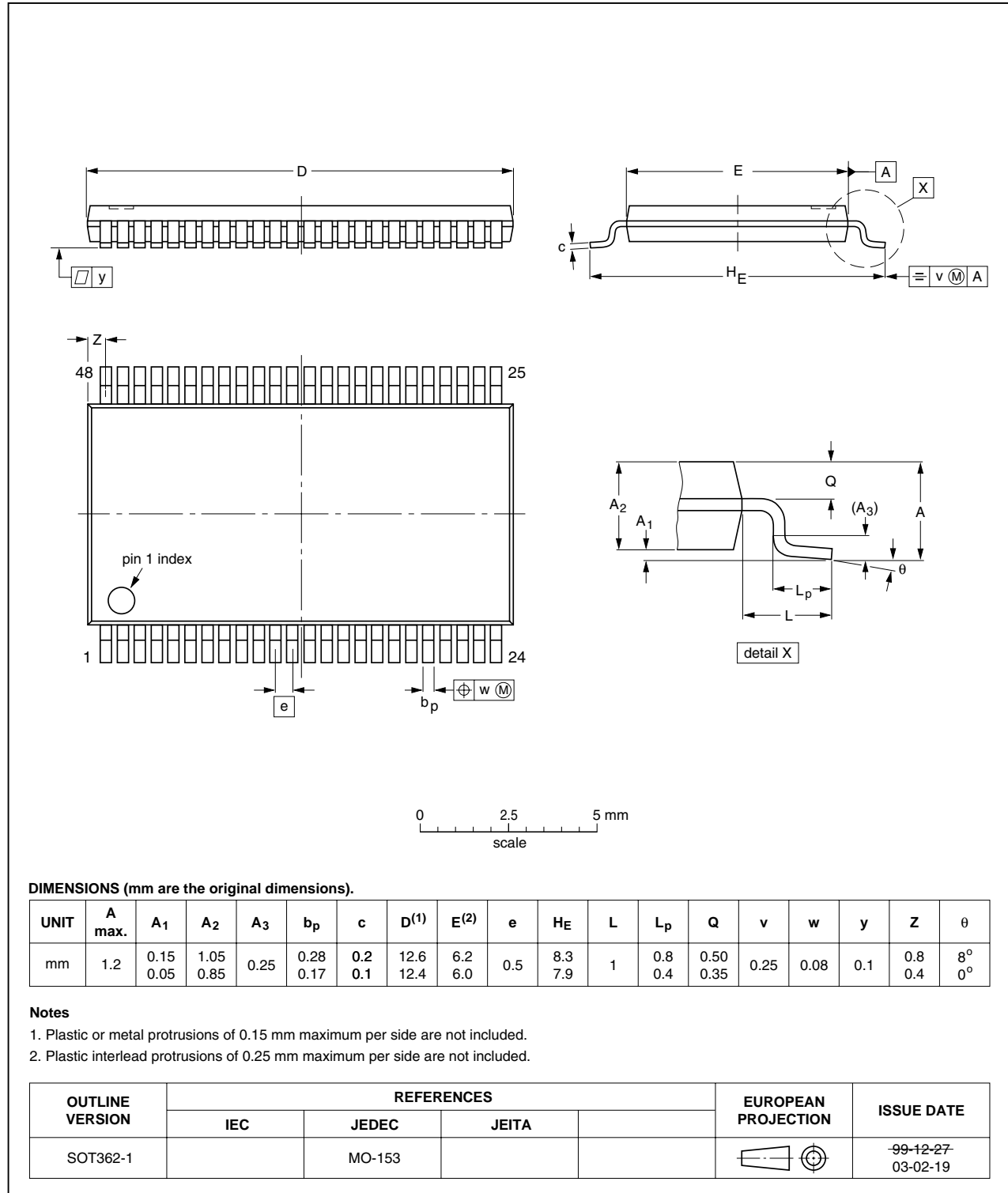


Fig 22. Package outline SOT362-1 (TSSOP48)

14. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 23](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 19](#) and [20](#)

Table 19. SnPb eutectic process (from J-STD-020C)

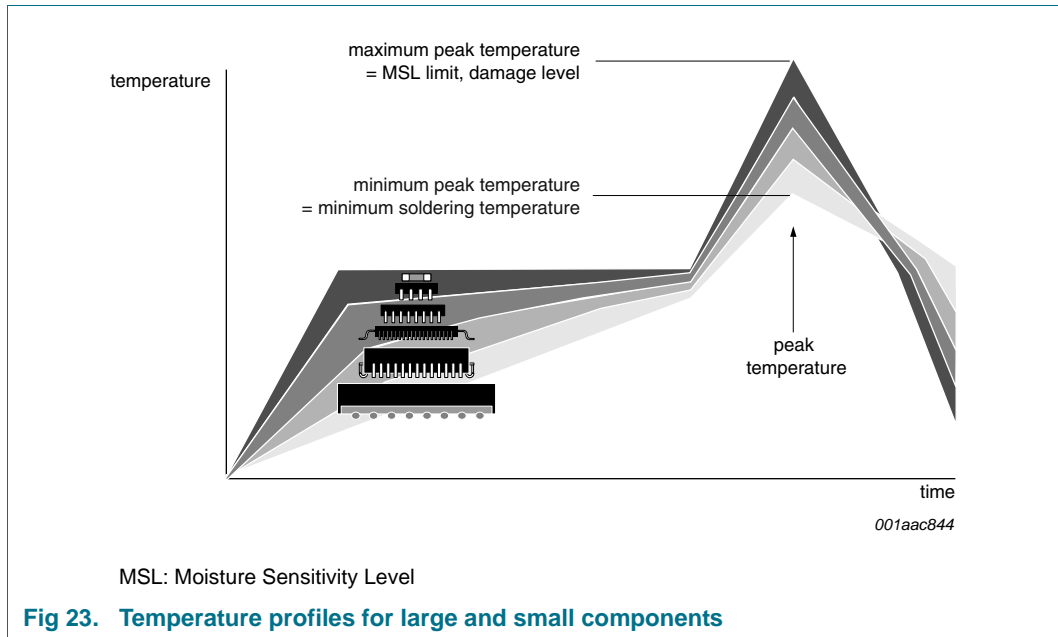
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 20. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 23](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

16. Abbreviations

Table 21. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
CDM	Charged-Device Model
HBM	Human Body Model
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
RAM	Random Access Memory
RC	Resistor Capacitor
RMS	Root Mean Square
SMD	Surface Mount Device

17. References

- [1] **AN10365** — Surface mount reflow soldering description
- [2] **IEC 60134** — Rating systems for electronic tubes and valves and analogous semiconductor devices
- [3] **IEC 61340-5** — Protection of electronic devices from electrostatic phenomena
- [4] **IPC/JEDEC J-STD-020D** — Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- [5] **JESD22-A114** — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [6] **JESD22-C101** — Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
- [7] **JESD78** — IC Latch-Up Test
- [8] **JESD625-A** — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- [9] **NX3-00092** — NXP store and transport requirements
- [10] **SNV-FA-01-02** — Marking Formats Integrated Circuits
- [11] **UM10204** — I²C-bus specification and user manual

18. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF85162_1	20100107	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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