General Information

The Frame and Line Interface Component PEB 2254 (FALC54) is a high sophisticated single chip solution for primary rate PCM carriers. It may be programmed to operate in 1.544-Mbit/s (T1) or 2.048-Mbit/s (CEPT) carrier systems. The FALC54 provides the complete functionality of a line interface-, a framing-, clock generation (2 VCOs) and signaling unit on one chip with greatly increased functionalities.

The FALC54 recovers clock and data using an integrated digital phase-locked loop. It shapes the output pulse following the AT&T Technical Advisory #34 or CCITT G.703 and generates a variety of systems clocks. The jitter tolerance of the device meets the newest CCITT recommendations and many other specifications by AT&T/ BELLCORE.

The FALC54 features include: selectable multiframe (six multiframe formats), error checking (CRC4, CRC6), multiple line codes (HDB3, B8ZS, AMI, CMI, NRZ), alarm reporting, maintenance and performance monitoring. The circuit contains a two-frame elastic memory which ensures wander absorption between the PCM carrier and a synchronous, system internal highway.

All signaling types – CCS, CAS and bit robbed signaling in conjunction with Clear Channel Capability – are controlled by the integrated LAPD/CAS signaling controller. In addition, the FALC54 allows flexible access to facility data link and service channels. All signaling and data link access can be handled via 64-byte FIFOs.

The device includes functions which meet newest CCITT, ETSI and FTZ recommendations for primary rate interfaces and the AT&T Digital Multiplexed Interface specifications (DMI). Controlling and monitoring of the device is performed via a parallel 16-bit data bus interface which is directly compatible with the most popular 8/16-bit microprocessors (Intel or Motorola type).

Below a list of equipment as described by the CCITT which potential FALC54 applications.

2048-kbit/s Applications

- PCM-multiplex equipment according to G.732 G.735, G.738
- Digital multiplex equipment according to G.736, G.742, G.745
- External access equipment according to G.737, G.739
- Digital exchange equipment according to G.705, Q.511 Q.512
- Transmultiplex equipment according to G.793
- Video conferencing according to H.120, H.130
- Transcoder equipment according to G.761
- Digital circuit multiplication equipment according to G.763
- Digital section/line system according to G.921, G.952, G.956

Type	Package
PEB 2254-H	P-MQFP-80-1 (SMD)

1544-kbit/s Applications

- PCM-multiplex equipment according to G.733
- Digital multiplex equipment according to G.734, G.743
- Digital exchange equipment according to G.705, Q.511, Q.512
- Transmultiplex equipment according to G.793
- Video conferencing according to H.120, H.130
- Transcoder equipment according to G.762
- Digital circuit multiplication equipment according to G.763
- Digital section/line system according to G.951, G.955
- ADPCM-multiplex equipment according to G.724

Features

Line Interface

- Data and clock recovery
- Low transmitter output impedance for a high return loss with reasonable protection resistors (CCITT G.703 requirements for the line input return loss fulfilled)
- Adaptively controlled receiver threshold
- Programmable pulse shape for T1 and CEPT
- Transmit line monitor
- Jitter specifications of CCITT I.431 and AT&T publications 62411 met
- Maximum line attenuation more than 16 dB (CCITT I.431)
- Wander and jitter attenuation
- Implements local and remote loops for diagnostic purposes
- Selectable line codes (H DB3, B8ZS, AMI, AMI with ZCS)
- Analog and digital loss of signal indication
- On-chip clock generator for system clocks
- TRISTATE function of transmit line outputs
- Jitter attenuator

Frame Aligner

- Frame alignments/synthesis for 2048 kbit/s (CEPT, PCM30) and 1544 kbit/s (T1, PCM24)
- Meets newest CCITT Rec's, ETSI Rec's, FTZ Rec's, and AT&T Technical References
- Programmable formats for
  PCM30: Doubleframe, CRC Multiframe
  PCM24: 4-Frame Multiframe (F4),12-Frame Multiframe (F12, D3/4), Extended Superframe (ESF), Remote Switch Mode (F72, SLC96)
- Selectable conditions for loss of sync
- Fully implementation of the CRC4 Non-CRC4
- Interworking of CCITT G.706
- Error checking via CRC4 or CRC6 procedures
- Error monitoring via E-bit and SA6-bit in CEPT mode
- Performance monitoring
- Insertion and extraction of alarms (AIS, RRA, AUXP…)
- IDLE-code insertion for selectable channels
- System clock frequency different for receive and transmit
- Selectable 2048/4096-kbit/s system internal highway with programmable receive/transmit shifts
- Programmable TRISTATE function of 4096 kbit/s output via RDO
- Two-frame deep elastic receive memory for receive route clock wander and jitter compensation (can be reduced to one frame length for PCM30 master-slave applications)
- One frame elastic transmit memory (PCM24 mode only) for transmit route clock wander and jitter compensation
- Support for different data link schemes
- Flexible transparent modes
- Channel- and line loop back capabilities

Signaling Controller

- LAPD controller
- Support DL-channel protocol for ESF format according to T1-403-1989 ANSI specification or according to AT&T specification TR54016 september 1989
- Handling of bit-oriented functions
- Programmable maximum packet size checking
- Programmable preamble
- Extended address masking
- Programmable FIFO size (32,16, …)
- CAS controller
- Multiframe synchronization and synthesis
- Alarm detection and generation
- Bit robbing support
- Clear channel capabilities in PCM24 mode
- Transparent Mode

MP Interface

- 8/16-bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte or word access)
- Extended interrupt capabilities

General

- Boundary scan standard IEEE 1149.1
- Advanced CMOS technology
- P-MQFP-80 package
- Power consumption less than 400 mW
  Note: The FALC54's power consumption is mainly determined by the line length and type of the cable.

Block Diagram

ITB06095

DR = Dual Rail   RL = Remote Loop   XS = Xslicer