Data Sheet, DS4, February 2001

QuadLIU™

Quad Line Interface Unit for E1/T1/J1

PEB 22504 Version 1.1

Datacom

Infineon technologies

Never stop thinking.

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Revision History:	**2001-02**	DS4
Previous Version:	Data Sheet, DS3, 2000-09	
Page	Subjects (major changes since last revision)	
	5 V supply mode is not supported	
7	**e-mail address changed**	
60	**Global Configuration Register**	
99	**Power Supply Range**	
121	**External Line Frontend Calculator**	
100	**Transmiter output current**	
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Preface

The Quad Line Interface Unit PEB 22504 (QuadLIU™) is a flexible line interface unit for a wide area of telecommunication and data communication applications. The device contains four complete channels on one chip to save board space and power consumption. This document provides complete reference information to configure E1, T1, and J1 applications.

Organization of this Document

This Data Sheet is organized as follows:

- **Chapter 1, Overview**
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.

- **Chapter 2, Pin Descriptions**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3, Functional Description**
  This chapter describes the functional blocks and principal operation modes.

- **Chapter 4, Interface Description**
  Describes the various device interfaces.

- **Chapter 5, Operational Description**
  Shows the operation modes and how they are to be initialized.

- **Chapter 6, Register Description**
  Gives a detailed description of all implemented registers and how to use them in different applications/configurations.

- **Chapter 7, Electrical Characteristics**
  Specifies maximum ratings, DC and AC characteristics.

- **Chapter 8, Package Outlines**
  Shows the mechanical values of the device package.

- **Chapter 9, Appendix**
  Gives an example for overvoltage protection and information about application notes and other support.

- **Chapter 10**, **Glossary**
- **Index**

Related Documentation

This document refers to the following international standards (in alphabetical/numerical order):

ANSI/EIA-656 (**page 119**)
ANSI T1.102 (**page 115**)
ANSI T1.231 (**page 71**, **page 89**, **page 90**)
ANSI T1.403 (**page 50**, **page 90**)
AT&T TR43802 (**page 40**)
AT&T TR62411 (**page 40**, **page 44**, **page 49**)
ESD Ass. Standard EOS/ESD-5.1-1993 (**page 98**)
ETSI ETS 300 011 (**page 40**)
ETSI ETS 300 233 (**page 39**, **page 40**, **page 89**)
ETSI TBR12 (**page 40**, **page 42**)
ETSI TBR13 (**page 40**, **page 42**)
FCC68 (**page 47**)
IEEE 1149.1 (**page 33**)
ITU-T G.703 (**page 40**)
ITU-T G.736-739 (**page 40**)
ITU-T G.775 (**page 39**, **page 39**, **page 89**, **page 89**)
ITU-T G.823 (**page 40**)
ITU-T G.824 (**page 40**)
ITU-T I.431 (**page 40**, **page 42**, **page 44**, **page 47**)
MIL-Std. 883D (**page 98**)
Telcordia TR-NWT-1089
TR-TSY 009 (**page 40**)
TR-TSY 253 (**page 40**)
TR-TSY 499 (**page 40**)
UL 1459

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Please provide in the *subject* of your e-mail:
device name (QuadLIU™), device number (PEB 22504), device version (Version 1.1),

and in the *body* of your e-mail:
document type (Data Sheet), issue date (2001-02) and document revision number (DS4).

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1 Overview

The QuadLIU™ PEB 22504 Quad Line Interface Unit is a device to connect four E1/T1/J1 framer devices to four analog or digital lines. The line interface is selectable for long-haul or short-haul applications and fulfills the relevant standards for E1, T1, and J1 systems.

The QuadLIU™ comes in a high-density P-TQFP-100-3 package (SMD) to save a significant amount of board space compared to a configuration using single line-interface circuits.

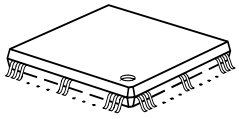
Crystal-less jitter attenuation with only one master clock source further reduces the amount of required external components.

Equipped with a flexible microcontroller interface, it fits to any control processor environment.

Quad Line Interface Unit for E1/T1/J1 **PEB 22504**
QuadLIU™

Version 1.1 **CMOS**

1.1 Features



P-TQFP-100-3

- High-density generic interface for all E1/T1/J1 applications
- Quad analog receive and transmit circuitry for long- and short-haul applications
- Clock and data recovery using an integrated digital phase-locked loop
- Programmable transmit pulse shapes for E1, T1 and J1 signals
- Maximum line attenuation up to -36 dB at 1024 kHz (E1) and up to -36 dB at 772 kHz (T1/J1)
- Noise- and crosstalk-filter, line attenuation status
- Programmable Line Build-Out for CSU signals according to ANSI T1.403 and FCC68 0dB, -7.5dB, -15dB, -22.5 dB
- Low transmitter output impedances for high transmit return loss
- Tristate function of the analog transmit line outputs
- Transmit line monitor protecting the device from damage
- Jitter specifications of ITU-T I.431 , G.703 , G.736, G.823, ETS 300011, TBR12/13 and AT&T TR62411 met
- Tolerates more than 0.4 UI high frequency input jitter
- Crystal-less wander and jitter attenuation/compensation
- Flexible master clock frequency in the range of 1.02 to 20 MHz
- Power-down function per channel
- Dual- or single-rail digital inputs and outputs to the framer interface
- Unipolar CMI for interfacing fiber-optical transmission routes
- Selectable line codes (HDB3, B8ZS, AMI with zero code suppression)
- Loss-of-signal indication with programmable thresholds according to ITU-T G.775, ETS300233, ANSI T1. 403 and T1.231
- Clock generator for jitter-free system/transmit clocks per channel
- Local loop, remote loop and digital loop back for diagnostic purposes

Type	Package
PEB 22504	P-TQFP-100-3

- Alarm and performance monitoring per second
- Two 16-bit counters for code violations and PRBS bit errors
- Insertion and extraction of Alarm Indication Signals (AIS)
- Elastic store for receive or transmit clock wander and jitter compensation
- Controlled slip capability and slip indication
- Programmable elastic buffer size: 256 bits/128 bits/64 bits/32 bits/bypass
- Programmable in-band loop code detection and generation according to TR 62411
- Pseudo-Random Bit Sequence (PRBS) generator and monitor
- Flexible software controlled device configuration

Microprocessor Interface Mode

- 8-bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible
- Multiplexed and non-multiplexed address bus operations
- Hardware and software reset options
- One-second timer

General

- Boundary scan standard IEEE 1149.1
- P-TQFP-100-3 package (body size 14 mm $\times$ 14 mm)
- Single power supply: 3.3 V
- Temperature range: -40°C to +85° C
- Low power device, typical power consumption 100 mW per channel

Applications

- Wireless Basestations
- ATM and frame relay gateways
- CSUs, DSUs
- Internet access equipment
- LAN/WAN Router
- ISDN-PRI, PABX
- Digital Access Cross-connect Systems (DACS)
- SDH/SONET ADD/DROP Multiplexer

1.2 Logic Symbol

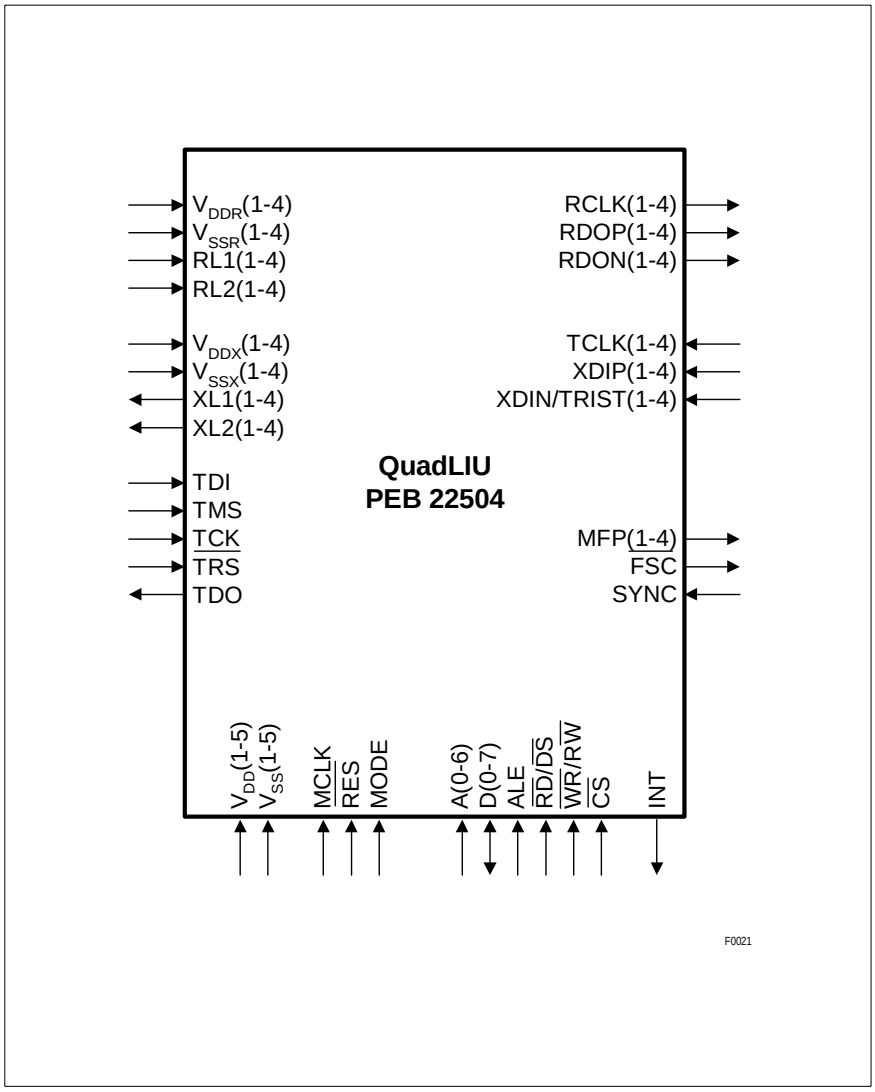


Figure 1 Logic Symbol

1.3 Typical Applications

Figure 2 shows a multiple link application using the QuadLIU™. **Figure 3** shows a repeater application.

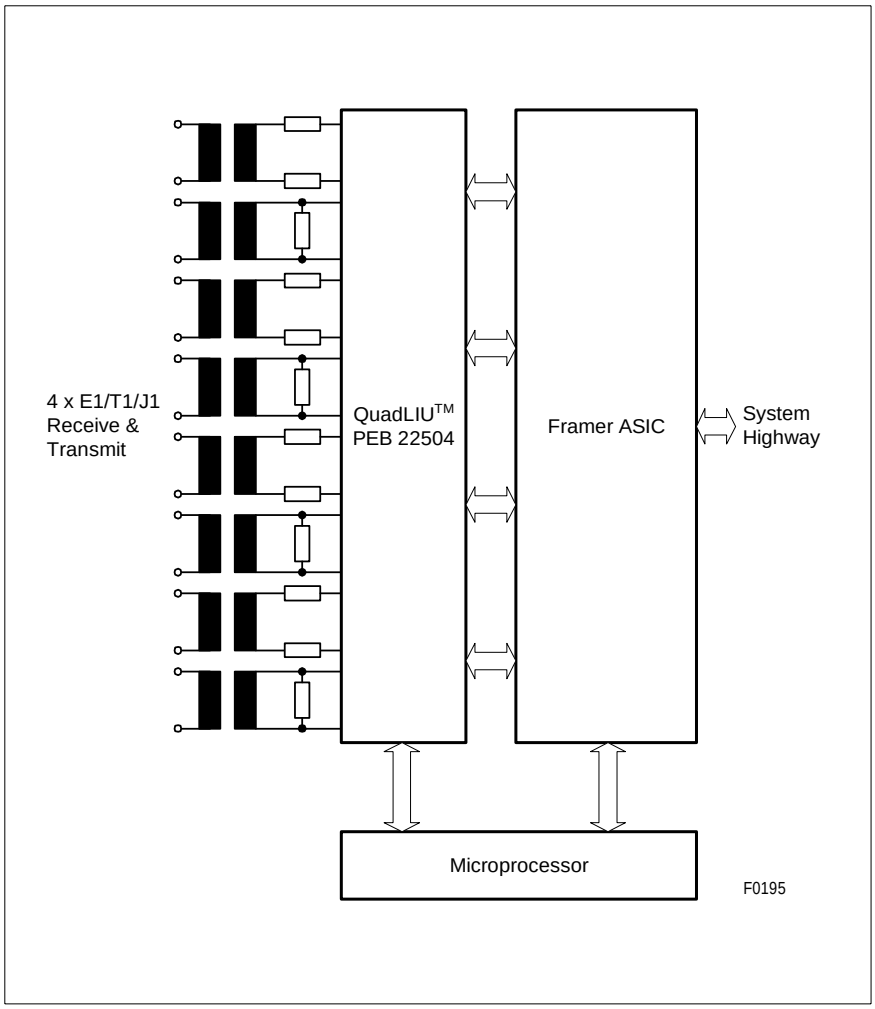


Figure 2 QuadLIU Application

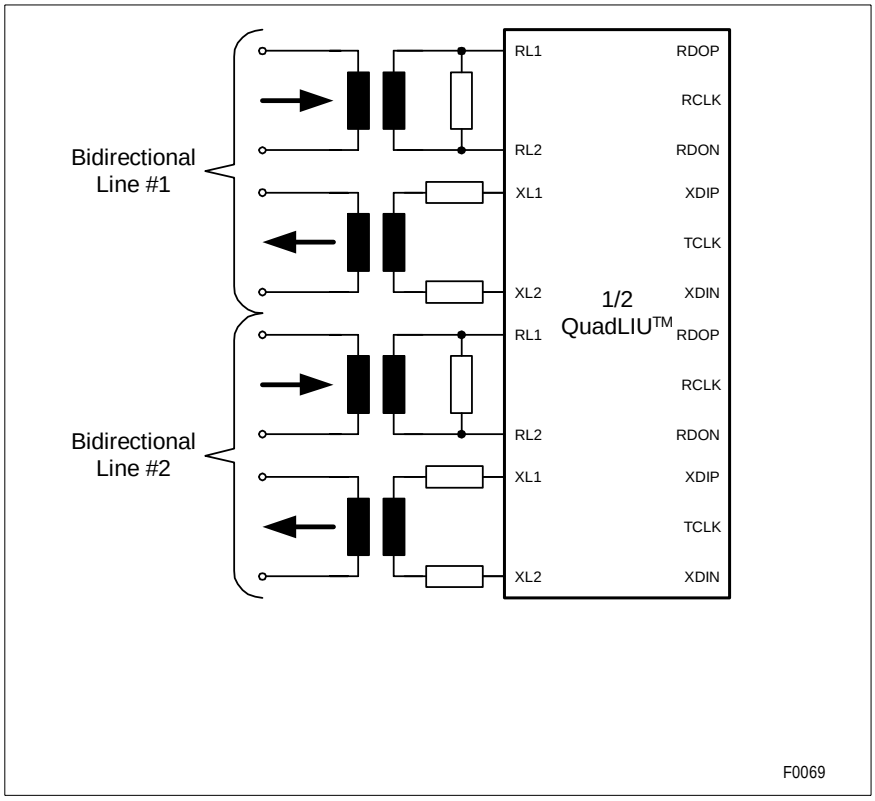


Figure 3 QuadLIU Repeater Application

2 Pin Descriptions

2.1 Pin Diagram

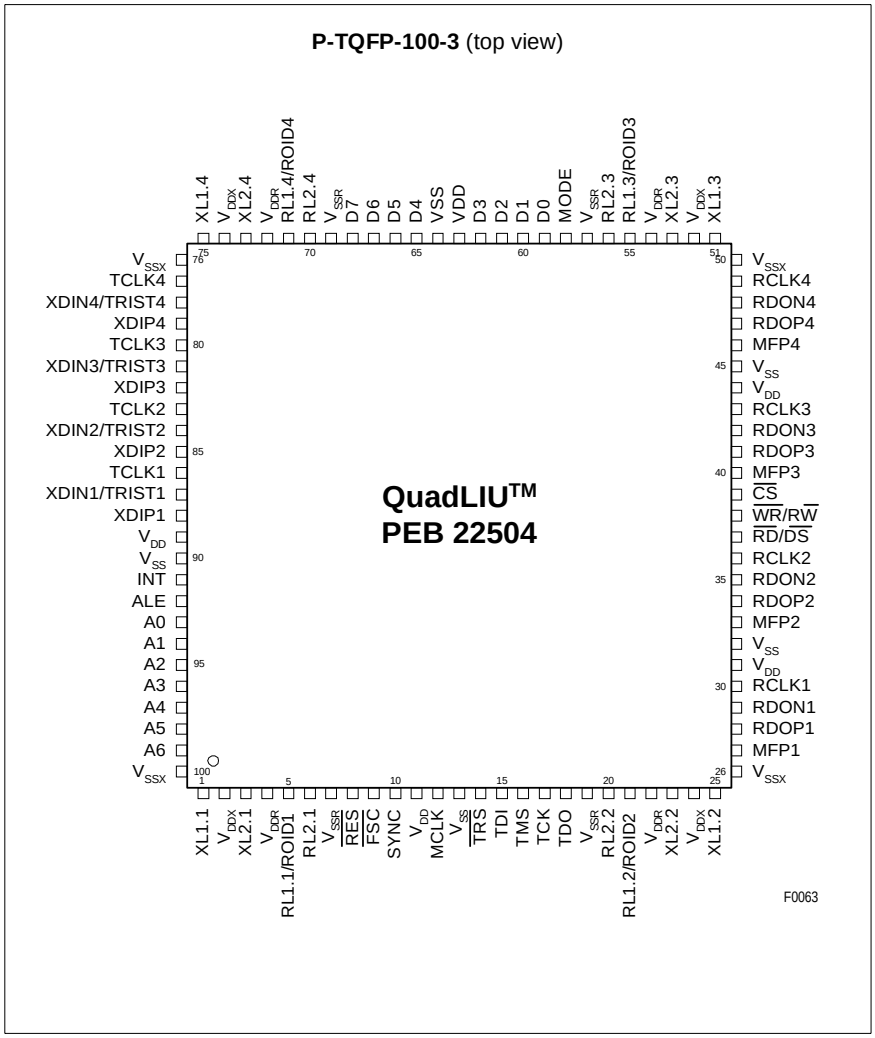


Figure 4 Pin Configuration

2.2 Pin Definitions and Functions

Table 1 Control Pin Functions

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
93...99	A(0:6)	I + PU	**Address Bus** Selects one of the internal registers for read or write.
59...62 65...68	D(0:3) D(4:7)	I/O + PU	**Data Bus** Eight-bit-wide bi-directional bus to be connected to the microprocessor data bus.
92	ALE	I + PU	**Address Latch Enable** A high on this line indicates an address on the external address/data bus. The address information provided on lines A(6:0) is internally latched with the falling edge of ALE. This function allows the device to be connected directly to a multiplexed address/data bus. In this case, pins A(6:0) must be connected externally to the data bus pins. In case of demultiplexed mode, this pin has to be connected to V_{SS} or V_{DD} directly.
39	$\overline{CS}$	I + PU	**Chip Select** A low signal selects the device for read/ write operations
37	$\overline{RD}$	I + PU	**Read Enable/Data Strobe** (Intel bus mode, MODE=low) This signal indicates a read operation. When the device is selected via $\overline{CS}$, the $\overline{RD}$ signal enables the bus drivers to output data from an internal register addressed via A(6:0) on to Data Bus.
	$\overline{DS}$	I + PU	**Data Strobe** (Motorola bus mode, MODE=high) This pin serves as input to control read/ write operations.

Table 1 Control Pin Functions (cont'd)

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
38	$\overline{WR}$	I + PU	**WRite Enable/Read-Write Select** (Intel bus mode, MODE=low) This signal indicates a write operation. When $\overline{CS}$ is active the device loads an internal register with data provided via the Data Bus.
	$R\overline{W}$	I + PU	**Read/Write Enable** (Motorola bus mode, MODE=high) This signal distinguishes between read and write operations.
91	INT	O/oD	**INTerrupt Request** General interrupt request output for all interrupt sources. These interrupt sources can be masked individually via register IMR0/1. Interrupt status is reported via register CIS (Channel Interrupt Status) and ISR0/1. Output characteristics of this pin can be defined to be push-pull (active high or active low) or open-drain (active low) by using register IPC.

Table 1 Control Pin Functions (cont'd)

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
27, 33, 40, 46	MFP(1:4)		**Multi Function Port** Depending on programming of bits LIM4.PC(2:0) this multifunction port provides different status information of the device as shown in this table below. MFP1 corresponds to channel 1, MFP4 to channel 4.
	LOS(1:4)	O	**Loss-of-Signal Indication** LIM4.PC(2:0) = 000 Active high, if a loss-of-signal alarm is detected. This signal corresponds directly to bit LSR0.LOS.
	ALOS(1:4)	O	**Analog Loss-of-Signal Indication** LIM4.PC(2:0) = 001 Active high, if the input level at RL1/2 drops below the programmed receive input threshold which is defined by register LIM2.RIL(2:0).
	PRBSS (1:4)	O	**PRBS Synchronization Status** LIM4.PC(2:0) = 010 Active high if the Pseudo-Random Bit Sequence (PRBS) synchronization is achieved. This signal corresponds directly to bit LSR0.PRBSS.
	BPV(1:4)	O	**Bipolar Violation Indication** LIM4.PC(2:0) = 011 Active high if a bipolar violation is detected. This signal corresponds directly to the increment signal of the code violation error counter.

Table 1 Control Pin Functions (cont'd)

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
27, 33, 40, 46 (cont'd)	XLS(1:4)	O	**Transmit Line Status** LIM4.PC(2:0) = 100 Active high if the transmit line current limiter exceeds its maximum value. Pins XL1/2 are automatically tristated until the current drops below its maximum value (or the "short" disappears). This signal corresponds directly to bit LSR1.XLS.
	AIS(1:4)	O	**Alarm Indication Signal** LIM4.PC(2:0) = 101 Active high if the alarm indication signal is detected. This signal corresponds directly to bit LSR0.AIS.
10	SYNC	I + PU	**Clock Synchronization** Reference clock for the internal DCOs of the device. Selectable via register GCR.SSF(1:0). Active high pulse input.
9	$\overline{\text{FSC}}$	O	**Frame Synchronization Pulse** The synchronization pulse is active low for one 2.048 (E1)/1.544 MHz (T1/J1) cycle (pulse width = 488/648 ns). $\overline{\text{FSC}}$ is derived from the jitter attenuation DCO, which must be active for $\overline{\text{FSC}}$ output (8-kHz master mode only, GCR.SSF(1:0) = 10). Active low pulse output.
87, 84, 81, 78	TRIST(1:4)	I + PU	**Transmit Line Tristate** If the single-rail data stream is selected by bit LIM0.XC(1:0), a high at these pins set the appropriate XL1/2 outputs into tristate. TRISTi sets XL1.i/2.i of channel i into tristate, where i = 1 to 4.

Table 2 Signal Pin Functions

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
5, 21, 55, 71	RL1(1:4)	I (analog)	**Line Receiver 1** (LIM1.ECMIR = 0, default) Analog input from the external transformer (receive bipolar ring).
	ROID(1:4)	I	**Receive Optical Interface Data** (LIM1.ECMIR = 1) CMI data received from fiber-optical interface with 2048 (E1)/ 1544 kbit/s (T1/ J1). An internal DPLL extracts the receive route clock from the incoming data pulse. The duty cycle of the receiving signal has to be closely to 50 %. RL2 has to be connected to V_{SS} or V_{DD}.
6, 20, 56, 70	RL2(1:4)	I (analog)	**Line Receiver 2** (LIM1.ECMIR = 0, default) Analog input from the external transformer (receive bipolar tip).
1, 25, 51, 75	XL1(1:4)	O (analog)	**Transmit Line 1** (transmit bipolar ring) (LIM1.ECMIX = 0, default) Analog output to the external transformer.
	XOID(1:4)	O	(LIM1.ECMIX = 1) Single-ail CMI output
3, 23, 53, 73	XL2 (1:4)	O (analog)	**Transmit Line 2** (transmit bipolar tip) (LIM1.ECMIX = 0, default) Analog output to the external transformer. If single-rail CMI output is selected (LIM1.ECMIX = 1), this pis is undefined and has to be left open.

Table 2 Signal Pin Functions (cont'd)

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
28, 34, 41, 47	RDOP(1:4)	O	**Receive Data Output/Positive** Received data at RL1/2 is sent on RDOP/ RDON in NRZ format to the framer interface. Clocking of data is done with the rising or falling edge of RCLK(1:4), selected by bit LIM4.RPE. RDOP/RDON are set low if a loss-of-signal alarm is detected. The source of the received data is selected by bit LIM2.RD(1:0).
			LIM2.RD(1:0) = 00: Data recovered by the DPLL is AMI/HDB3/B8ZS decoded and output on RDOP; RDON is not defined.
			LIM2.RD(1:0) = 01: Dual-rail data recovered by the DPLL, not AMI/HDB3/ B8ZS decoded, is output on RDOP/RDON.
			LIM2.RD(1:0) = 10: Sliced data, not recovered by the DPLL is output on RDOP/ RDON. A "1" on RDOP corresponds to a positive pulse on RL1/RL2. A "1" on RDON corresponds to a negative pulse on RL1/ RL2.
29, 35, 42, 48	RDON(1:4)	O	**Receive Data Output/Negative** LIM1.RDON(1:0) = 00 (see above)
	BPV(1:4)	O	**Bipolar Violation Indication** LIM1.RDON(1:0) = 01
	SCLKO	O	**System Clock Output** LIM1.RDON(1:0) = 10
	SCLKI	I + PU	**System Clock Input** LIM1.RDON(1:0) = 11 Read clock for jitter attenuater buffer if internal DCO is not used (see **Figure 10** on **page 38**).

Table 2 Signal Pin Functions (cont'd)

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
88, 85, 82, 79	XDIP(1:4)	I + PU	**Transmit Data In Positive** Transmit data received from the framer interface is output on XL1/2. NRZ data has to be provided on XDIP. Latching of data is done with the rising or falling transitions of TCLK according to LIM4.TPE.
87, 84, 81, 78	XDIN(1:4)	I + PU	**Transmit Data In Negative** If the dual-rail data stream is selected by bits LIM0.XC(1:0) transmit data received from the framer interface is output on XL1/2. NRZ data (AMI negative data) has to be provided on XDIN. Latching of data is done with rising or falling transitions of TCLK according to bit LIM4.TPE.
30, 36, 43, 49	RCLK(1:4)	O	**Receive Clock** The output functions of these ports are defined by register CMR.RS(1:0): CMR.RS(1:0) = 00: Receive Clock extracted from the incoming data pulses. CMR.RS(1:0) = 01: Receive Clock extracted from the incoming data pulses. RCLK is set high in case of loss-of-signal (LSR0.LOS=1). Selected by GCR.R1S(1:0), one of the four RCLK(1:4) is output on RCLK1. The clock frequency is 2.048 (E1)/ 1.544 MHz (T1/J1)
	SCLKO (1:4)	O	CMR.RS(1:0) = 10: Output of de-jittered system clock sourced by DCO. Clock frequency: 2.048 (E1) or 1.544 MHz (T1/J1). See **Figure 10** on **page 38**.

Table 2 Signal Pin Functions (cont'd)

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
86, 83, 80, 77	TCLK(1:4)	I + PU	**Transmit Clock** Input of the working clock for the transmitter with a frequency of 2.048 (E1)/ 1.544 MHz (T1/J1).
12	MCLK	I	**Master Clock** A reference clock between 1.02 MHz and 20 MHz must be provided on this pin (32 ppm accuracy).
8	$\overline{\text{RES}}$	I	**Hardware Reset** A low signal on this pin forces the device into reset state. During reset, an active clock is needed on pin MCLK.
58	MODE	I + PU	**Operation Mode Select** 0 = Intel bus 1 = Motorola bus

Table 3 Power Supply Pins

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
4, 22, 54, 72	V_{DDR}	S (analog)	**Positive Power Supply** for the analog receiver
7, 19, 57, 69	V_{SSR}	S (analog)	**Power Supply Ground** for the analog receiver
2, 24, 52, 74	V_{DDX}	S (analog)	**Positive Power Supply** for the analog transmitter
26, 50, 76, 100	V_{SSX}	S (analog)	**Power Supply Ground** for the analog transmitter
11, 31, 44, 63, 89	V_{DD}	S	**Positive Power Supply** for digital subcircuits
13, 32, 45, 64, 90	V_{SS}	S	**Power Supply Ground** for digital subcircuits

Table 4 Boundary Scan Pins

Pin No.	Signal	Input (I) Output (O) Supply (S)	Function
14	$\overline{TRS}$	I + PU	**Test Reset** (Boundary Scan) active low; if the JTAG boundary scan is not used, this pin must be connected to $\overline{RES}$ or V_{SS}.
15	TDI	I + PU	**Test Data Input** (Boundary Scan)
16	TMS	I + PU	**Test Mode Select** (Boundary Scan)
17	TCK	I + PU	**Test Clock** (Boundary Scan)
18	TDO	O	**Test Data Output** (Boundary Scan)

Note: oD = open-drain output
PU = input or input/output comprising an internal pullup device
To override the internal pullup by an external pulldown, a resistor value of 22 kΩ is recommended.

Unused pins containing pullups can be left open. Unused receive channels have to be connected to a fixed level (V_{DDR} or V_{SSR}).

3 Functional Description

3.1 Functional Overview

The QuadLIU™ device contains analog and digital function blocks that are configured and controlled by an external microprocessor or microcontroller.

The main interfaces are

- Receive-line Interface
- Transmit-line Interface
- Framer interface
- Microprocessor interface
- Boundary scan interface

as well as several control lines for reset and clocking purpose.

The main internal functional blocks are

- Analog line receiver with equalizer network and clock/data recovery
- Analog line driver with programmable pulse shaper and line build out
- Central clock-generation module
- Jitter attenuator in receive or transmit direction
- Test functions (e.g., loop switching local - remote - digital)
- Register access interface
- Boundary scan control

3.2 Block Diagram

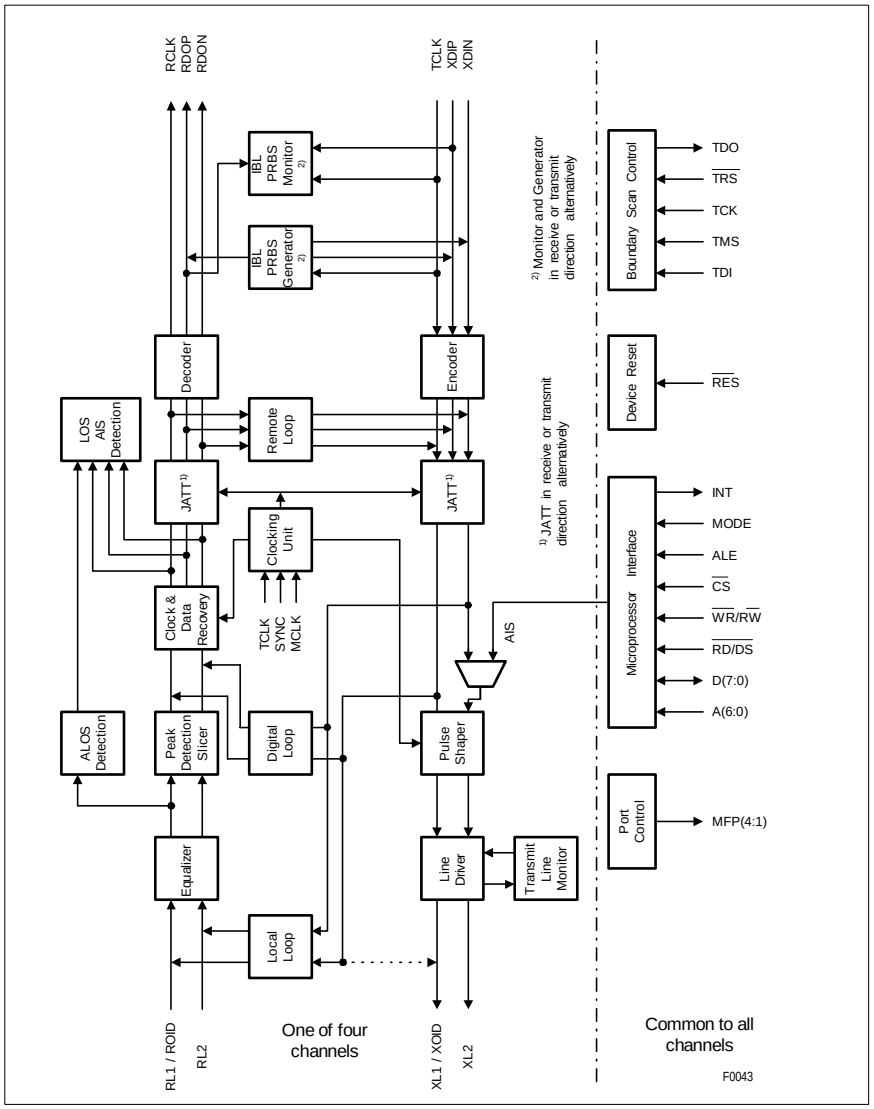


Figure 5 Block Diagram

3.3 Functional Blocks

3.3.1 Microprocessor Control Unit

The communication between the CPU and the QuadLIU™ is done via a set of directly accessible registers. The interface may be configured as Intel or Motorola type (by control pin MODE) with a data bus width of 8 bits.

The CPU transfers data to/from the QuadLIU™, sets the operating modes, controls function sequences, and gets status information by writing or reading control/status registers. **Table 5** shows how the ALE (**A**ddress **L**atch **E**nable) and MODE lines are used to control the interface type. Switching of ALE allows the QuadLIU™ to be connected directly to a multiplexed address/data bus.

Table 5 Selectable Bus and Microprocessor Interface Configuration

ALE	MODE	Microprocessor interface	Bus Structure
V_{SS} or V_{DD}	high	Motorola	demultiplexed
V_{SS} or V_{DD}	low	Intel	demultiplexed
switching	low	Intel	multiplexed

3.3.1.1 Interrupt Interface

Special events in the QuadLIU™ are indicated by means of a single interrupt output, which requests the CPU to read status information from the QuadLIU™, or to transfer data to the QuadLIU™. The pin characteristic (open drain, push-pull) is programmable.

Since only one INT request output is provided, the cause of an interrupt must be determined by the CPU by reading the QuadLIU™'s interrupt status registers CIS and ISR(1:0). The interrupt on pin INT and the interrupt status bits are reset by reading the interrupt status registers. Registers ISR0 and ISR1 are “cleared on read“.

The structure of the interrupt status registers is shown in **Figure 6**.

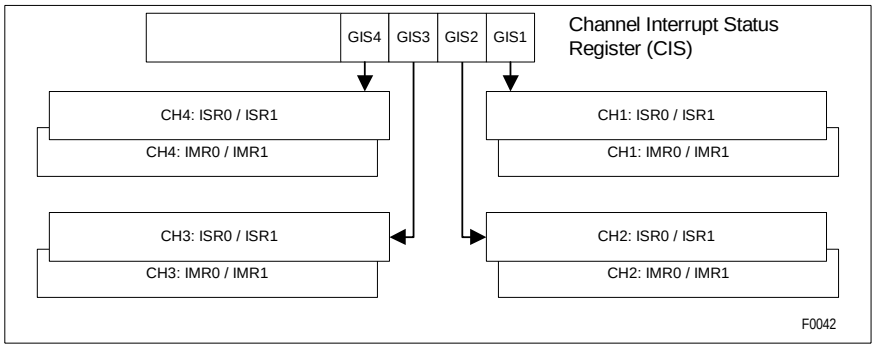


Figure 6 Interrupt Status Registers

Each interrupt indication of register ISR0 and ISR1 can be masked selectively by setting the corresponding bit in the mask registers IMR0 and IMR1. If the interrupt status bits are masked, they neither generate an interrupt on pin INT nor are they visible in ISR(1:0).

The non-maskable **C**hannel **I**nterrupt **S**tatus (CIS) register serves as a pointer to pending ISRs. After the QuadLIU™ has requested an interrupt by activating its INT pin, the CPU should first read the CIS register to identify the requesting channel by bit GISx (**G**lobal **I**nterrupt **S**tatus bit of channel x) After that the corresponding interrupt status register ISR(1:0) of the requesting channel should be examined. After reading the interrupt status registers ISR(1:0), the pointer in CIS is cleared or updated if another interrupt requires service.

If **all** pending interrupts are acknowledged by reading the ISRs, CIS is reset and pin INT goes inactive.

Updating of ISR(1:0) and CIS is prohibited only during read access.

Masked Interrupts Visible in Status Registers

The CIS register indicates those channels with active interrupt indications.

An additional mode (“visible mode”) may be selected via bit LIM4.VIS. In this mode, masked interrupt status bits neither generate an interrupt on pin INT nor are they visible in CIS, **but are displayed in the corresponding ISR(s) ISR(1:0)**.

This mode is useful when some interrupt status bits are to be polled in the individual ISRs.

Note: In the visible mode, all active interrupt status bits, whether the corresponding actual interrupt is masked or not, are reset when the interrupt status register is read. Thus, when polling of some interrupt status bits is desired, care must be taken that unmasked interrupts are not lost in the process.

All unmasked interrupt statuses are treated as in normal mode.

Please note that whenever polling is used, all interrupt status registers concerned have to be polled individually (no “hierarchical” polling is possible), since CIS contains information on only those interrupts that were actually generated, i.e., unmasked interrupts.

3.3.2 Boundary Scan Unit

In the QuadLIU™ a **T**est **A**ccess **P**ort (TAP) controller is implemented. The essential part of the TAP is a finite state machine (16 states) controlling the different operational modes of the boundary scan. Both, TAP controller and boundary scan, meet the requirements in the JTAG standard IEEE 1149.1. **Figure 7** gives an overview.

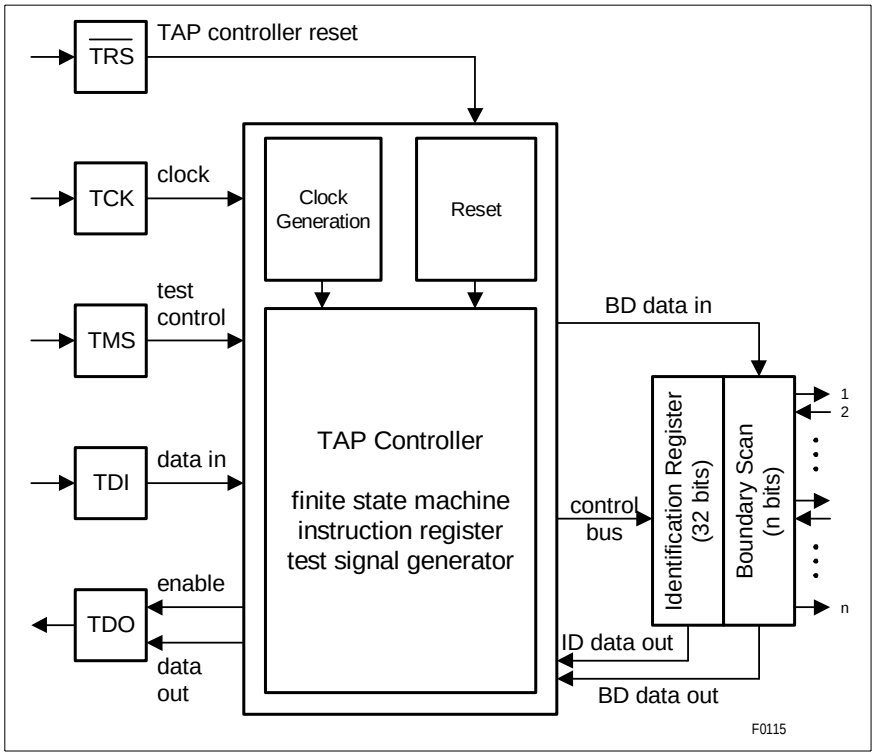


Figure 7 Block Diagram of Test Access Port and Boundary Scan

After switching on the device (power-on), a reset signal has to be applied to $\overline{\text{TRS}}$, which forces the TAP controller into test logic reset state.

For normal operation without boundary scan access, the boundary reset pin $\overline{\text{TRS}}$ can be tied to the device reset pin $\overline{\text{RES}}$.

The boundary length is 150.

If no boundary scan operation is used, $\overline{TRS}$ has to be connected to $\overline{RST}$ or V_{SS}. TMS, TCK and TDI do not need to be connected since pullup transistors ensure high input levels in this case.

Test handling (boundary scan operation) is performed via the pins TCK (Test Clock), TMS (Test Mode Select), TDI (Test Data Input) and TDO (Test Data Output) when the TAP controller is not in its reset state, that means $\overline{TRS}$ is connected to V_{DD} or it remains unconnected due to its internal pull up. Test data at TDI is loaded with a clock signal connected to TCK. "1" or "0" on TMS causes a transition from one controller state to another; constant "1" on TMS leads to normal operation of the chip.

An input pin (I) uses one boundary scan cell (data in), an output pin (O) uses two cells (data out and enable) and an I/O-pin (I/O) uses three cells (data in, data out and enable). Note that most functional output and input pins of the QuadLIU™ are tested as I/O pins in boundary scan, hence using three cells. The desired test mode is selected by serially loading a 8-bit instruction code into the instruction register via TDI (LSB first).

EXTEST is used to examine the interconnection of the devices on the board. In this test mode at first all input pins capture the current level on the corresponding external interconnection line, whereas all output pins are held at constant values ("0" or "1"). Then the contents of the boundary scan is shifted to TDO. At the same time the next scan vector is loaded from TDI. Subsequently all output pins are updated according to the new boundary scan contents and all input pins again capture the current external level afterwards, and so on.

SAMPLE is a test mode which provides a snapshot of pin levels during normal operation.

IDCODE: A 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to "1".

The ID code field is set to: 0001 0000 0000 0101 1010 0000 1000 0011

Version = 1_H, Part Number = $005A_H$, Manufacturer = 083_H (including LSB, fixed to "1")

BYPASS: A bit entering TDI is shifted to TDO after one TCK clock cycle.

An alphabetical overview of all TAP controller operation codes is given in **Table 6**.

Table 6 TAP Controller Instruction Codes

TAP Instruction	Instruction Code
BYPASS	11111111
EXTEST	00000000
IDCODE	00000100
SAMPLE	00000001
reserved for device test	01010011

3.3.3 Master Clocking Unit

The QuadLIU™ provides a flexible clocking unit that can use a stable reference clock in the range of 1.02 MHz to 20 MHz supplied on pin MCLK.

The clocking unit has to be tuned to the selected reference frequency by setting the **G**lobal **C**lock **M**ode registers (GCM(6:1)) accordingly.

The calculation formulas for the appropriate register settings can be found in **Chapter 6.2** on **page 87**. All required clocks for E1 and T1/J1 operation are generated internally by this circuit. The global setting depends only on the selected master clock frequency, and is the same for E1 and T1/J1 because both clock rates are provided simultaneously.

The flexible master clock unit can be disabled (GCM2.VFREQ_EN = 0, which is the default configuration after hardware reset). In this case, a fixed reference clock of 2.048 MHz (E1) or 1.544 MHz (T1/J1) has to be supplied on pin MCLK.

Note: E1 or T1/J1 mode can be selected independently for each channel if flexible clocking is selected (GCM2.VFREQ_EN = 1).

To meet the transmit clock and data accuracy requirements of E1/T1 in free running mode, the MCLK reference clock itself must have an accuracy of ± 32 ppm. The synthesized clock can be controlled on pin RCLK.

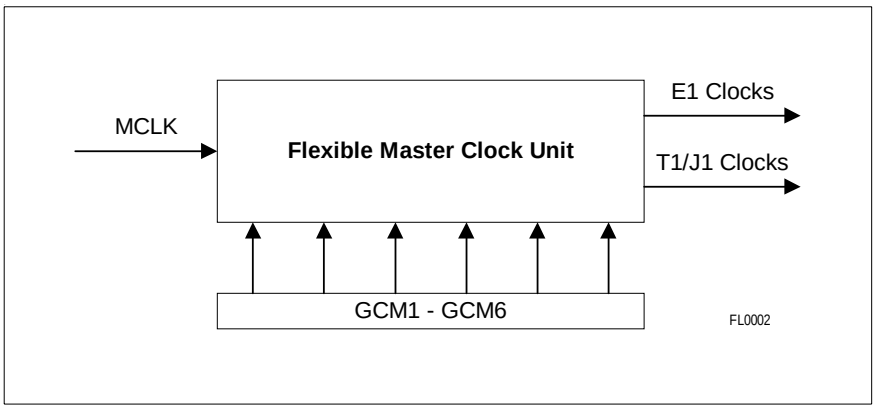


Figure 8 Flexible Master Clock Unit

4 Interface Description

4.1 Receiver

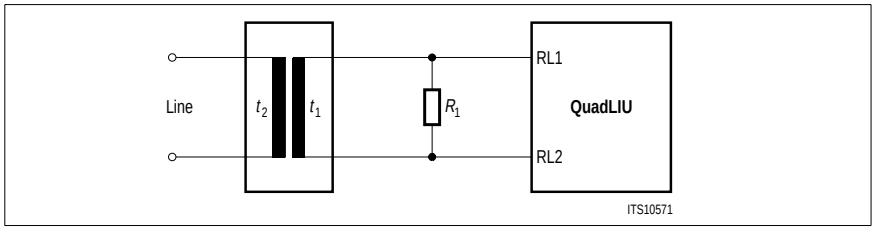


Figure 9 Receiver Configuration

Table 7 Examples of External Component Values (Receive)

Parameter		Characteristic Impedance [Ω]			
		E1		T1	J1
		75	120	100	110
	R_1 (± 1 %) [Ω]	75	120	100	110
	$t_2 : t_1$	1 : 1	1 : 1	1 : 1	1 : 1

4.1.1 Receive Line Interface

Several data input types are supported:

- Ternary coded signals received at multifunction ports RL1 and RL2 from a - 10 dB or -36 dB (E1)/-36 dB (T1/J1) ternary interface. The ternary interface is selected if LIM1.ECMIR is reset.
- CMI coded data on port ROID received from a fiber-optical interface. The optical interface is selected if LIM1.ECMIR is set.

The signal at the ternary interface is received on both ends of a transformer.

The line termination impedance 75 Ω/120 Ω/100 Ω is selectable by switching resistors in parallel. This selection does not require a change of transformers.

4.1.2 Short-haul/Long-haul Interface

The QuadLIU™ has an integrated short- and long-haul line interface consisting of a receive equalization network and noise filtering.

4.1.3 Receive Equalization Network

The QuadLIU™ automatically recovers the signals received on pins RL1/2 in a range of up to -36 dB. The maximum reachable length with a 22 AWG twisted-pair cable is 6000 feet (T1/J1). After reset the QuadLIU™ is in short-haul mode, and received signals are recovered up to a cable attenuation of -10 dB. Switching to long-haul mode is done by setting of register bit LIM1.EQON.

Noise filters eliminate the higher frequency part of the received signals. The incoming data is peak-detected and sliced at 45, 50, 55, or 67% of the peak value (programmable in four steps by LIM2.SLT(1:0)) to produce the digital data stream. The received data is then forwarded to the clock and data recovery unit (DPLL) or optionally transferred to ports RDOP/RDON directly (see LIM2.RD(1:0)).

The current equalizer status is indicated by register RES (**R**eceive **E**qualizer **S**tatus).

4.1.4 Receive Line Attenuation Indication

RES reports the current receive line attenuation in 25 steps of approximately 1.7 dB (E1)/ 1.4 dB (T1/J1) each. The least significant five bits of this register indicate the cable attenuation in dB. These five bits are only valid together with the most significant two bits (RES.EV(1:0) = 01) .

4.1.5 Receive Clock and Data Recovery

The analog received signal on port RL1/2 is equalized and then peak-detected to produce a digital signal. The receive clock and data recovery subcircuit extracts the route clock RCLK from the data stream received on the RL1/2 or ROID lines, and converts the data stream into a dual-rail bit stream. The clock and data recovery works with the internally generated high-frequency clock based on MCLK. Normally, the clock that is output on pin RCLK is the recovered clock from the signal provided on RL1/2, and has a duty cycle close to 50 %. The free run frequency is defined by the master clock setting [2.048 MHz (E1)/1.544 MHz (T1/J1)] in periods with no signal. The intrinsic jitter generated in the absence of any input jitter is not more than 0.02 UI (**U**nit **I**ntervals).

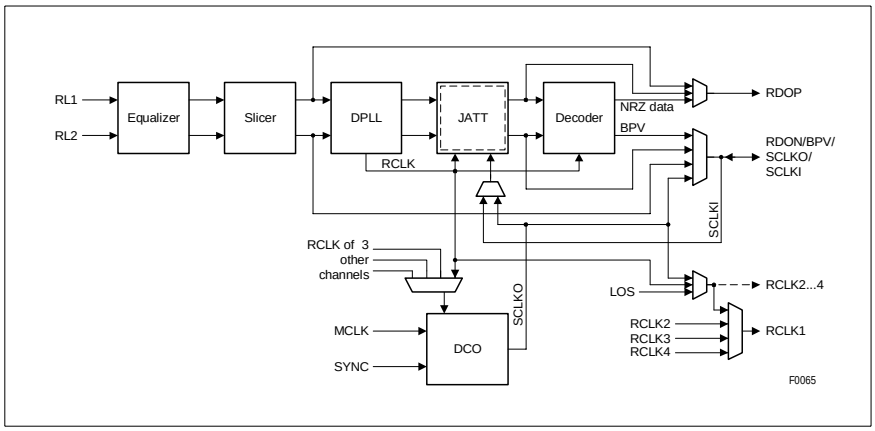


Figure 10 Receive Clock System

4.1.6 Receive Line Coding

In E1 applications, HDB3 and AMI coding is provided for the data received from the ternary interface. In T1 mode, B8ZS and AMI code is supported. In case of the optical interface, CMI Code (1T2B) with HDB3/B8ZS postprocessing is provided. If the DPLL is not bypassed, the receive route clock is recovered from the data stream. The CMI decoder does not correct any errors. The HDB3 code is used along with double violation detection or extended code violation detection (optional, see LIM0.EXZE). In B8ZS or AMI, code all code violations are detected.

Detected errors increment the code violation counter (16 bits length).

4.1.7 Pulse-Density Detector

Pulse-density violations of the received signal are detected according to ANSI T1.403. Violations are indicated (LSR0.PDEN, ISR0.PDENI) if the incoming signal contains:

- More than 15 consecutive zeros *or*
- Fewer than N ones in each and every time window of 8 × (N+1) digit time slots with N taking on all values of 1 to 23.

The indication is cleared, if the pulse-density fulfills the requirement within 23 received ones.

4.1.8 Alarm Handling

The receive line interface includes alarm detection for AIS (**A**larm **I**ndication **S**ignal) and LOS (**L**oss **O**f **S**ignal).

4.1.8.1 AIS (Blue Alarm) Detection

The AIS is detected according to ITU-T G.775 and ANSI T1.231.

In E1 applications, the alarm is set when the incoming signal has fewer than three zeros in each of two consecutive 512-bit periods. In T1 applications, the AIS alarm is set when fewer than 6 zeros are detected within a time interval of 3 ms received on RL1/2. AIS detection also works in the presence of a bit error rate of up to 10^{-3}.
An AIS alarm is indicated in a **L**ine **S**tatus **R**egister (LSR0.AIS) and an **I**nterrupt **S**tatus **R**egister (ISR0.AIS).

4.1.8.2 LOS (Red Alarm) Detection

There are different definitions for detecting LOS alarms in the ITU-T G.775, ETS 300233, ANSI T1.403 and T1.231. The QuadLIU™ covers all these standards. The LOS indication is performed by generating an interrupt (if not masked) and activating a status bit. Additionally, a LOS status change interrupt is programmable via register LIM4.SCI.

- Detection:

  In digital receive interface mode (LIM1.ECMIR = 1), an alarm is generated if the incoming data stream has no pulses (no transitions) for a certain number (N) of consecutive pulse periods. “No pulse” means a logical zero on pin ROID.

  In analog receive interface mode (LIM1.ECMIR = 0), a pulse with an amplitude less than Q dB below nominal is the criteria for “no pulse”. The receive signal level Q is programmable via three control bits, LIM2.RIL(2:0), related to the differential voltage between pins RL1 and RL2 (see DC Characteristics on page **100**). The number N can be set via an 8-bit register, PCD. The contents of the PCD register is multiplied by 16; the product equals the number of pulse periods until the alarm has to be detected (16

to 4096 pulse periods). ETS 300233, which requires detection intervals of at least 1 ms, can be fulfilled.

- Recovery:

  The recovery procedure starts after detection of a logical "one" (digital receive interface) or a pulse (analog receive interface) with an amplitude more than Q dB (defined by LIM2.RIL(2:0)) of the nominal pulse. The value in the 8 bit register PCR defines the number of pulses (1 to 255) required to clear the LOS alarm. Additional recovery conditions may be programmed by register LIM5.LOSR(1:0).

4.1.9 Jitter Attenuator

The internal PLL (**P**hase-**L**ocked **L**oop) circuitry called DCO (**D**igitally **C**ontrolled **O**scillator) generates a “jitter-free“ output clock which is directly depending on the phase difference between the incoming clock and the jitter-attenuated clock. The jitter attenuator can be placed on the receive or transmit path of each channel individually. The working clock is an internally generated high-frequency clock based on the clock provided on pin MCLK. The jitter attenuator meets the requirements of ITU-T I.431, G.703, G.736-739, G.823, G.824, ETSI 300011, ETSI TBR12/13, AT&T TR62411, AT&T TR43802, TR-TSY 009, TR-TSY 253 and TR-TSY 499. The receive jitter attenuator can be synchronized either to the extracted receive clock RCLK, or to a 2.048 (E1)/1.544 MHz (T1/J1)/8 KHz (E1/T1/J1) clock provided on pin SYNC. The transmit jitter attenuator synchronizes with either the clock provided on pin TCLK, or the receive clock RCLK (remote loop/loop-timed).

Received data is written into the elastic buffer with RCLK and is read out with the de-jittered clock sourced by DCO (if JATT in receive direction is selected). The jitter attenuated clock can be output on pin RCLK. An 8-kHz clock is provided on pin $\overline{\text{FSC}}$.

Transmit data is written into the elastic buffer with TCLK and is read out with the de-jittered clock sourced by DCO (if JATT in transmit direction is selected). In the loop-timed clock configuration (CMR.ELT) the DCO circuitry generates a transmit clock that is frequency synchronized to RCLK.

The DCO circuitry attenuates the incoming jittered clock starting at 2 Hz (E1)/6 Hz (T1/J1) jitter frequency with 20 dB/decade fall-off. Wander with a jitter frequency below 2/6 Hz is passed unattenuated. The intrinsic jitter in the absence of any input jitter is less than 0.02 UI.

The DCO accepts gapped clocks, which are used in ATM or SDH/SONET applications.

For some applications, it might be useful to start jitter attenuation at lower frequencies. Therefore the corner frequency is switchable by the factor of ten down to 0.2/0.6 Hz (CMR.SCF).

The jitter attenuator works in two different modes:

- Slave mode
  In slave mode (CMR.MAS = 0), the DCO is synchronized with the recovered route clock. In case of LOS (receive mode) or transmit clock is lost (transmit mode, bit LSR1.TCS = 1), the DCO switches to master mode automatically. If bit CMR.DCS is set, automatic switching from RCLK/TCLK to SYNC is disabled.
- Master mode
  In master mode (CMR.MAS = 1) the jitter attenuator is in free-running mode if no clock is supplied on pin SYNC . If there is a clock with a frequency of 2.048 (E1)/1.544 MHz (T1/J1)/8 kHz (E1/T1/J1) on the SYNC input, the DCO is synchronized with this input signal.
  In some applications, it might be useful to synchronize to a gapped clock sourced by pin SYNC. In this case, the DCO circuitry would be centered to the nominal frequency. Optionally the QuadLIU™ offers the ability to disable the centering the DCO circuitry (LIM4.DCF = 1).

Table 8 shows the clock modes with the corresponding synchronization sources.

Table 8 Clocking Modes

Mode	Internal LOS active or TCS set	SYNC Input	DCO[1] Output Clock
Master	no	V_{DD}	Free-running (DCO centered)
Master	no	1.544 MHz	Synchronized with SYNC input [2] GCR.SSF(1:0) = 01
Master	no	2.048 MHz	Synchronized with SYNC input [2] GCR.SSF(1:0) = 00
Master	no	8 kHz	Synchronized with SYNC input GCR.SSF(1:0) = 10
Slave	no	V_{DD}	Synchronized with line RCLK/TCLK(4:1), selected by CMR.DSS(1:0)
Slave	no	1.544 MHz	Synchronized with line RCLK/TCLK(4:1), selected by CMR.DSS(1:0) [2]
Slave	no	2.048 MHz	Synchronized with line RCLK/TCLK(4:1) , selected by CMR.DSS(1:0) [2]
Slave	yes	V_{DD}	Free running (DCO centered)

Table 8 Clocking Modes (cont'd)

Mode	Internal LOS active or TCS set	SYNC Input	DCO[1] Output Clock
Slave	yes	1.544 MHz	Synchronized with SYNC input [2] GCR.SSF(1:0) = 01
Slave	yes	2.048 MHz	Synchronized with SYNC input [2] GCR.SSF(1:0) = 00

1) The DCO can be used either in receive or transmit direction (see **Figure 10** and **Figure 14**)

2) If flexible clocking mode is selected (GCM2.VFREQ_EN = 1), the SYNC frequency can be selected independent of E1 or T1/J1 mode.

The jitter attenuator meets the jitter transfer requirements of ITU-T I.431 and G.735-739 (refer to **Figure 11**).

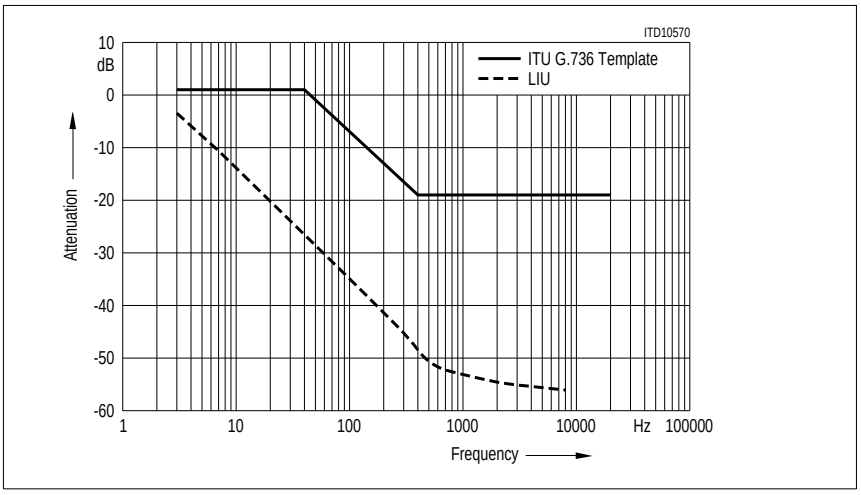


Figure 11 Jitter Attenuation Performance

Also the requirements of ETSI TBR12/13 are satisfied. The DCO starts jitter attenuation at about 2 Hz to ensure adequate margin against TBR12/13 output jitter limit with 15 UI input at 20 Hz.

4.1.10 Jitter Tolerance

The QuadLIU™ receiver's tolerance to input jitter complies with ITU for CEPT applications. **Figure 12** shows the curves of different input jitter specifications as well as the QuadLIU™ performance.

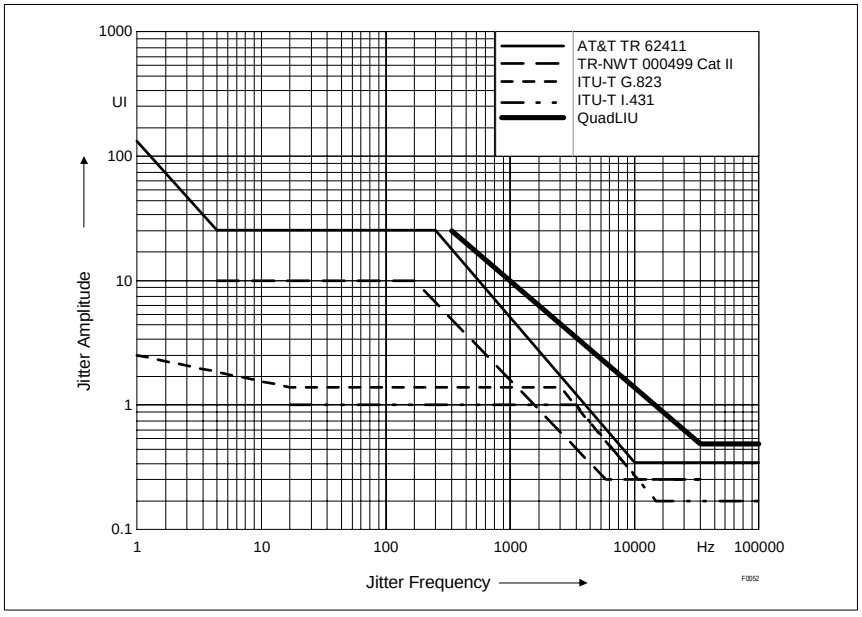


Figure 12 Jitter Tolerance

4.1.11 Output Jitter

In the absence of any input jitter, the QuadLIU™ generates the output jitter as specified in **Table 9**.

Table 9 Output Jitter

Specification	Measurement Filter Bandwidth		Output Jitter (UI peak to peak)
	Lower Cutoff	Upper Cutoff	
AT&T TR62411	10 Hz	8 kHz	< 0.015
	8 kHz	40 kHz	< 0.015
	10 Hz	40 kHz	< 0.015
ITU-T I.431	20 Hz	100 kHz	< 0.015
	700 Hz	100 kHz	< 0.015
	Broadband		< 0.02

4.1.12 Elastic Buffer

The elastic buffer can be placed in receive or transmit direction to generate a “jitter-free” data stream. Different buffer sizes can be programmed by LOOP.BS(1:0):

- 00: 256 bits
- 01: 128 bits
- 10: 64 bits
- 11: 32 bits

Slips are performed in all buffer modes. After a slip is detected, the read pointer is adjusted to one half of the current buffer size.

A slip condition is detected when the write pointer and the read pointer of the memory are nearly coincident. If a slip condition is detected, a negative slip or a positive slip is performed. For a negative slip, one half of the current buffer size is skipped. For a positive slip, one half of the current buffer size is read out twice. A positive or negative slip is indicated in the interrupt status bits ISR0.SLP and ISR0.SLN.
When bit CMDR.CEB is set, the data delay through the elastic buffer is set to half of the current buffer size.

4.2 Transmitter

The serial bit stream is then processed by the transmitter which has the following functions:

- AIS generation (**A**larm **I**ndication **S**ignal)
- Generation of AMI, B8ZS, HDB3 or CMI coded signals
- Generation of IBL (**I**n-**B**and **L**oop) code
- Generation of PRBS (**P**seudo-**R**andom **B**inary **S**equence)

4.2.1 Transmit Line Interface

The analog transmitter transforms the unipolar bit stream to ternary (alternate bipolar) return-to-zero signals of the appropriate programmable pulse shape. The unipolar data is provided by the digital transmitter.

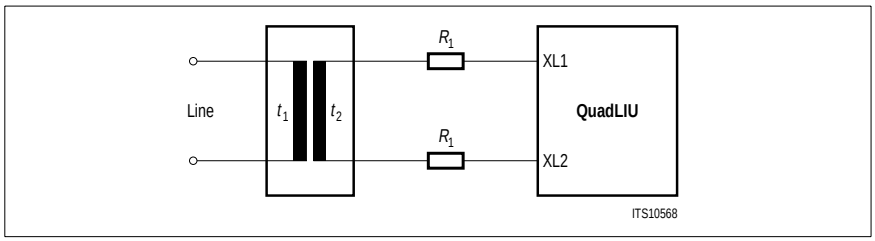


Figure 13 Transmitter Configuration

Table 10 Examples of External Component Values (Transmit)

Parameter		Characteristic Impedance [Ω]			
		E1		T1	J1
		75	120	100	110
	R_1 (± 1 %) [Ω]	7.5	7.5	2	2
	t2 : t1	1 : 2.4	1 : 2.4	1 : 2.4	1 : 2.4
	XPM2.XLHC	1	1	1	1

In transmit direction, only the ternary or CMI interface is supported:

- Ternary signal
  The received data stream on pins XDIP or XDIP/N is converted into a ternary signal which is output on pins XL1 and XL2. In E1 mode the HDB3 and AMI line code is employed. In T1 mode, B8ZS and AMI with or without zero code suppression is supported (selected by LIM0.XC(1:0); the encoder can also be disabled).
- CMI signal
  The received data stream is converted into a CMI signal with HDB3 (E1) or B8ZS (T1/J1) precoding.

4.2.2 Transmit Clock System

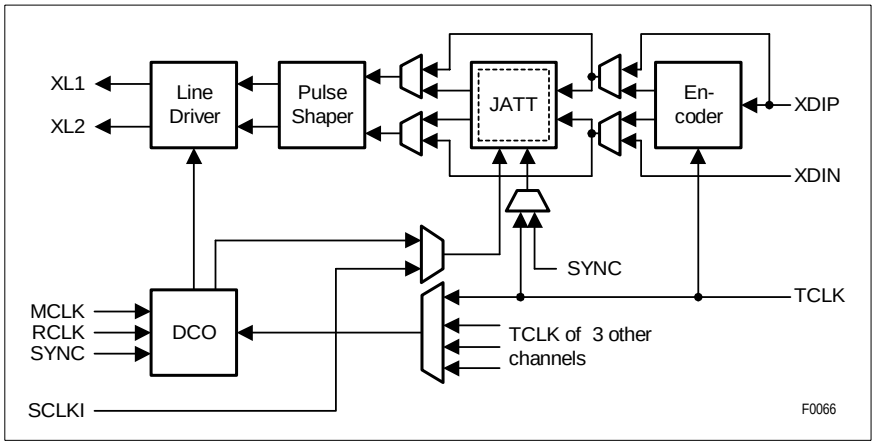


Figure 14 Transmit Clock System

The jitter attenuator can be placed in the receive or transmit path. If placed in the transmit path, data is clocked into the JATT buffer with the transmit clock TCLK. If automatic clock-switching is enabled (LIM5.ACS = 1), TCLK is replaced by the SYNC clock automatically, if TCLK is missing. The active edge of TCLK (or SYNC, if TCLK is missing) can be programmed by LIM4.TPE.

4.2.3 Pulse-Density Enforcer

The integrated pulse-density enforcer can be activated (LIM0.PDE = 1) to ensure the outgoing signal fulfills the pulse-density requirements of ANSI T1.403:

- No more than 15 consecutive zeros
- At least N ones in every time window of 8 × (N+1) digit time slots, with N taking on all values of 1 to 23.

4.2.4 Programmable Pulse Shaper and Line Build-Out

In long-haul applications, the transmit pulse masks are optionally generated according to FCC68 and ANSI T1.403 for T1 applications. To reduce the crosstalk on the received signals, the QuadLIU™ can place a transmit attenuator in the data path (LBO, **L**ine **B**uild **O**ut). Transmit attenuation is selectable to be 0 , -7.5, -15 or -22.5 dB (selected by register LIM3.LBO(2:1)). ANSI T1.403 defines only 0 to -15 dB (T1/J1 mode only).

The QuadLIU™ includes a programmable pulse shaper to satisfy the requirements of ITU-T I.431 , ANSI T1. 102, and various DS1, DSX-1 specifications are met. The amplitude of the pulse shaper is programmable individually via the microprocessor interface to allow a large number of different pulse templates. Adaption to the line length is selected by programming the registers XPM(2:0) as shown on **page 77**. To reduce power consumption, the output stage biasing can be reduced (LIM5.XLB = 1). This leads to slightly reduced slopes.

4.2.5 Transmit Line Monitor

The transmit line monitor compares the transmit line current on XL1 and XL2 with an on-chip transmit line current limiter. The monitor detects faults on the primary side of the transformer indicated by a highly-increased transmit line current (more than about 120 mA for at least three "1" pulses), and protects the device from damage by automatically setting the transmit line driver XL1/2 in a high-impedance state. The current limiter checks the actual current value of XL1/2, and if the transmit line current drops below the detection limit, the high-impedance state is cleared.

Two conditions are detected by the monitor: transmit line ones density (more than 31 consecutive zeros) indicated by LSR1.XLO and transmit line high currrent indicated by LSR1.XLS. In both cases a transmit line monitor status change interrupt is provided.

The transmit line monitor function can be disabled by LIM5.XLM = 0 to reduce power consumption.

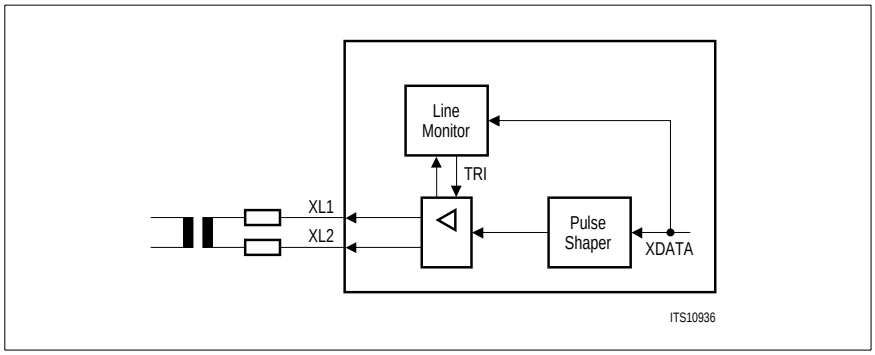


Figure 15 Transmit Line Monitor Configuration

4.3 Framer Interface

The system side interface to the receive framer interface is realized by RDOP, RDON and RCLK. Data on RDOP/N is clocked with either the rising or falling edge of RCLK (LIM4.RPE, see **Figure 10** on **page 38**).

Data from the framer interface is sampled at XDIP and XDIN on the active edge of TCLK. The active edge can be the rising or falling edge of TCLK (LIM4.TPE). An automatic clock-switching mode can be enabled (LIM5.ACS = 1) to switch automatically to the clock provided on pin SYNC if TCLK is missing. The selected edge (rising/falling) also applies to SYNC, if selected by automatic switching.

4.4 Maintenance Functions

4.4.1 Error Counter

The QuadLIU™ offers two error counters. Each of them is 16 bits long. They record code violations and PRBS errors. Both error counters are buffered. Updating of the buffer is done in two modes:

- Every one-second interval
- On demand via handshake by writing to register CMDR

In the one-second-mode an internal/external one-second timer updates these buffers and resets the counter to accumulating the error events. The error counter cannot overflow. Error events occuring during reset don't get lost.

4.4.2 One-Second Timer

A one-second timer interrupt can be generated per channel internally to indicate that the enabled alarm status bits or the error counters have to be checked. The one-second timer is part of the monitor block and is related to the selected clock source (RCLK, SCLKO, SCLKI or TCLK).

4.4.3 Pseudo-Random Bit Sequence Generation and Monitor

The QuadLIU™ has the ability to generate and monitor a 2^{15}-1 or 2^{20}-1 PRBS with maximum zero restriction according to ITU-T O.151 and AT&T TR62411. The generated PRBS pattern is transmitted directly or inverted.

The PRBS monitor senses the PRBS pattern in the receive or transmit data stream. Synchronization is done with inverted and non-inverted PRBS patterns. The current synchronization status is reported in status and interrupt status registers. Data streams consisting of continuous ones or zeros also lead to the indication of synchronous state. Each PRBS bit error increments the PRBS error counter (BECL/H). Synchronization is reached within 400 ms at a probability of 99.9 % in the presence of a bit error rate of $\leq 10^{-1}$.

4.4.4 In-Band Loop Generation and Detection

The QuadLIU™ generates an unframed IBL (**I**n-**B**and **L**oop) pattern and detects a framed or unframed IBL pattern according to ANSI T1. 403. The detection works even in the presence of bit errors at a rate of up to 10^{-2}. The loop-up and loop-down patterns are programmable individually from 2 to 8 bits in length (LCR1.LAC(1:0) and LCR1.LDC(1:0)). Programming of loop codes is done in registers LCR2 and LCR3, using default values 00001 for activation and 001 for deactivation of the loop. The in-band loop generator and monitor can be placed either on the receive or transmit path independently (LIM3.GTP, LIM3.MTP). The monitor is enabled by setting LIM3.EPRM = 1. If the in-band loop code has been detected for at least 5 s, the QuadLIU™ optionally switches the remote loop on or off according to ANSI T1.403 (LIM0.ARL = 1). The current state of the remote loop is indicated in a status register. Replacing the receive or transmit data with the in-band loop codes is done by LCR1.XLD/XLA.

Status and interrupt-status bits inform the user whether loop-up or loop-down code was detected.

4.4.5 Remote Loop

In the remote loop-back mode, the clock and data recovered from the line inputs RL1/2 or ROID are routed back to the line outputs XL1/2 or XOID via the analog or digital transmitter. As in normal mode, they are also processed by the synchronizer and then sent to the system interface. The remote loop-back mode is selected by setting the control bits LOOP.RL, LOOP.EJATT and LOOP.XJATT. Received data may be looped with or without the transmit jitter attenuator (JATT).

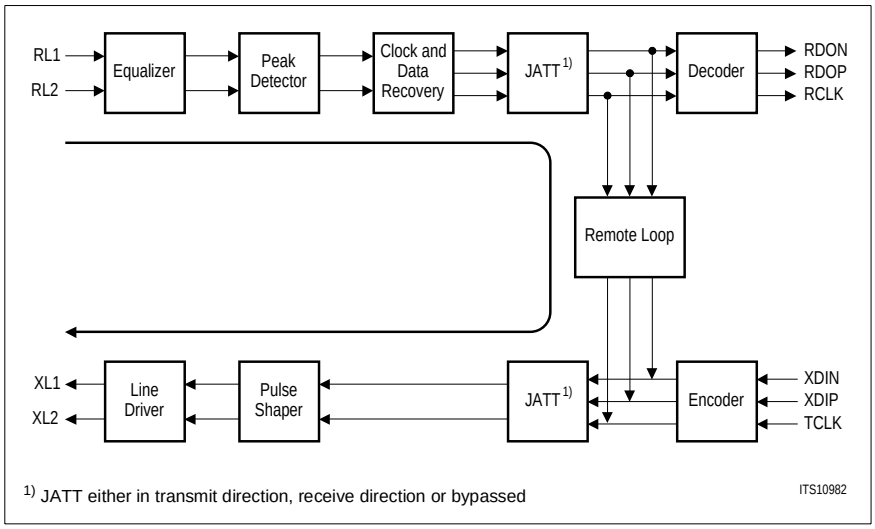


Figure 16 Remote Loop Signal Flow

Note: If an external loop shall be switched between RDON/RDOP/RCLK and XDIN/ XDIP/TCLK, the setup/hold time requirements described in the AC characteristics have to be observed. To relax the timing, the edge selection of either the receive or transmit path can be inverted (see register description of LIM4), or an inverter can be placed between RCLK and TCLK externally.

4.4.6 Local Loop

The local loop-back mode, selected by LOOP.LL = 1, disconnects the receive lines RL1⁄2 or ROID from the receiver. It is used in analog input applications (LIM1.ECMIR = 0). Instead of the signals coming from the line, data provided by the system interface is routed through the analog receiver back to the framer interface. The bit stream is transmitted without disturbance on the transmit line. An AIS to the distant end can be enabled by setting LIM1.XAIS without influencing the data looped back to the system interface.

The signal codes for transmitter and receiver have to be programmed to be identical.

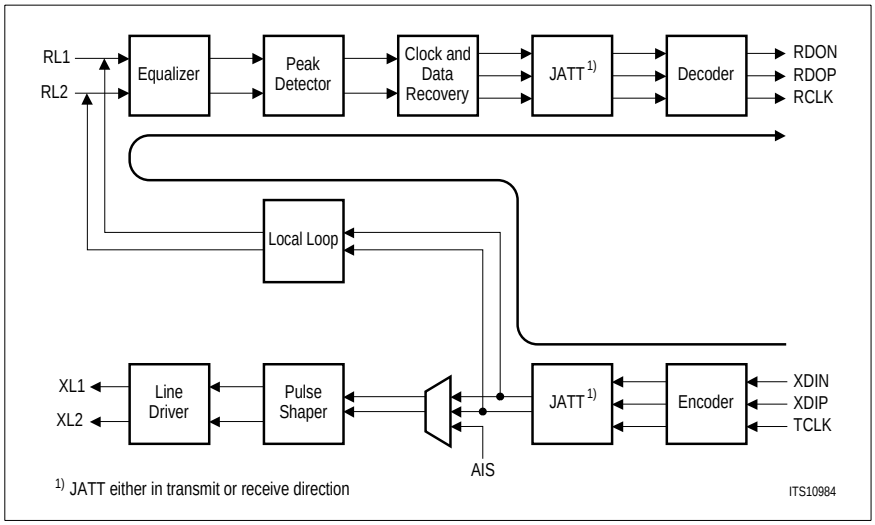


Figure 17 Local Loop Signal Flow

4.4.7 Digital Loop

The digital loop-back mode, selected by LOOP.DLB = 1, also disconnects the receive lines RL1/2 from the receiver. It is used in digital input applications (LIM1.ECMIR = 1). Instead of the signals coming from the line, the data provided by framer interface is routed through the clock and data recovery circuit back to the framer interface without touching the analog receiver part. The bit stream is transmitted on XL1/2 without disturbance. An AIS to the distant end can be enabled by setting LIM1.XAIS without influencing the data looped back to the framer interface.

The serial codes for transmitter and receiver have to be programmed identically.

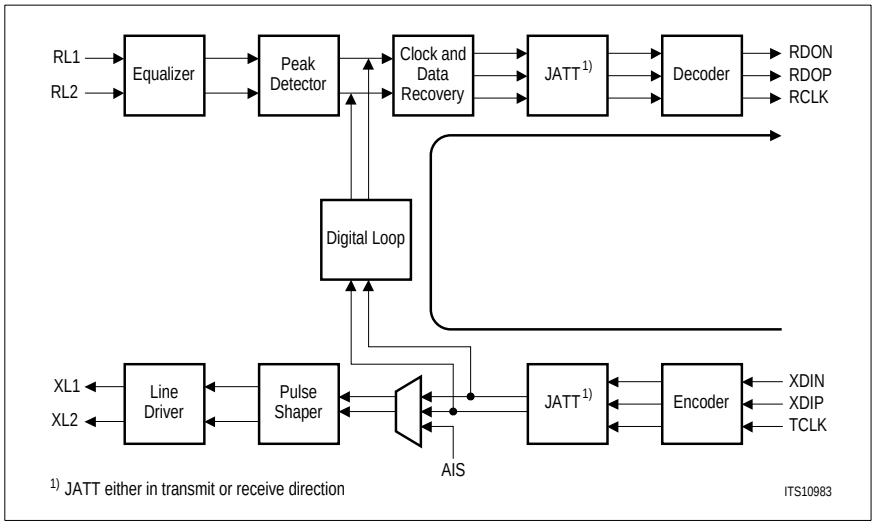


Figure 18 Digital Loop Signal FLow

4.4.8 Alarm Simulation

Alarm simulation does not affect the normal operation of the device. However, real alarm conditions are not reported to the processor or to the remote end when the device is in the alarm simulation mode.

The alarm simulation is initiated by setting the bit LIM0.SIM. The following alarms are simulated:

- Loss of Signal LOS (red alarm)
- Alarm Indication Signal AIS (blue alarm)
- Slip indication
- Code violation counter (AMI, B8ZS, HDB3 Code) increment
- Pulse-density violation
- Transmit clock (TCLK) lost
- PRBS synchronous state indication and PRBS error counter increment

Setting of the bit LIM0.SIM initiates alarm simulation, interrupt status bits are set. Error counting and indication occurs while this bit is set. After it is reset, all simulated error conditions disappear, but the generated interrupt statuses are still pending until the corresponding interrupt status register is read. Alarms such as AIS and LOS are cleared automatically. Interrupt status register and error counters are cleared automatically on read.

4.4.9 Transmit Data Performance Monitoring

Alternatively to the receive data performance monitoring (BPV, EXZ, LOS), this function can be switched into the transmit direction to supervise data received on pins XDIP and XDIN (LIM5.XDPM = 1).

Transmit data performance monitoring is available only in bypass mode (LIM2.RD(1:0) = 10), and is not available in remote loop configuration. The principle data flow is shown in **Figure 19**.

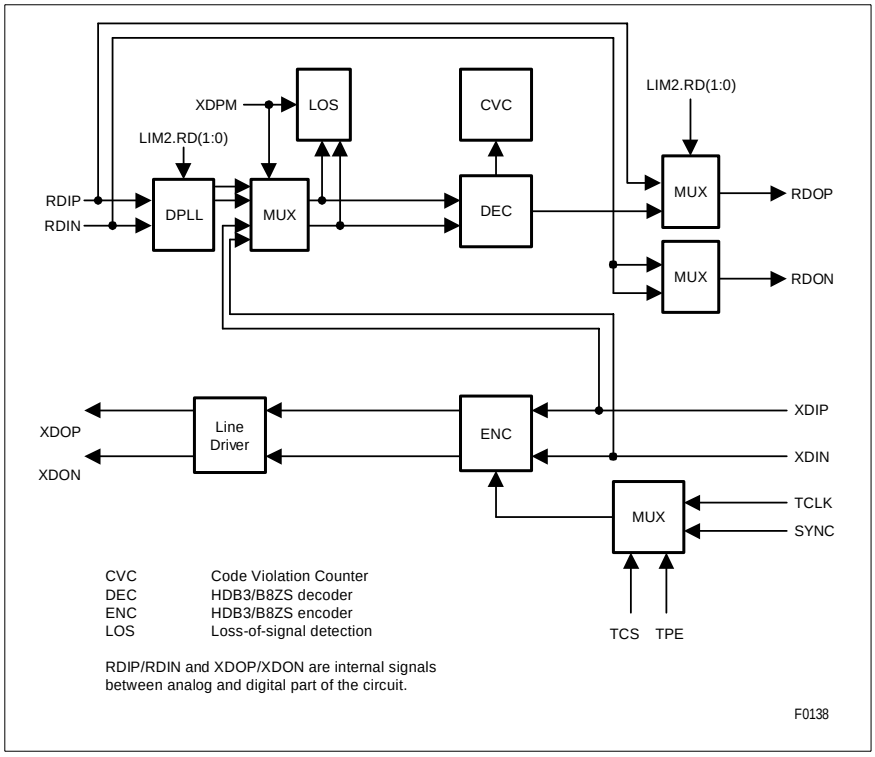


Figure 19 Transmit Data Performance Monitoring

5 Operational Description

5.1 Operational Overview

The QuadLIU™ can be operated in one of two modes, which is either E1 mode or T1/J1 mode.

The device is programmable via a microprocessor interface which enables byte access to all control and status registers.

The QuadLIU™ must be initially programmed after reset. General guidelines for initialization are described in **“Basic Initialization Settings” on page 57**.

The status registers are read-only and are updated continuously. Usually the processor reads the status registers periodically to analyze the alarm status.

SIgnals (for example RL1/2 receive line) should not be applied before the device is powered up.

5.2 Device Reset

The QuadLIU™ is forced to the reset state if a low signal is input on pin $\overline{\text{RES}}$ (for minimum period, see **“Reset” on page 105**). During reset, the QuadLIU™ needs an active clock on pin MCLK. All output stages are in a high-impedance state, all internal flip-flops are reset, and most of the control registers are initialized to default values.

After reset, the device is initialized to E1 operation.

5.3 Device Initialization

5.3.1 Reset Values

After reset, the QuadLIU™ is initialized with register values listed in **Table 11**.

Table 11 Initial Values after Reset

Register	Reset Value	Meaning
GCR	80_H	$\overline{\text{FSC}}$ is sourced by channel 1, RCLK1 clock source: Channel 1
GCR2	00_H	E1 mode for all four channels, INT function is open drain
LIM0	00_H	AMI coding
LIM1	00_H	Power up
LIM2	40_H	LOS threshold -20 dB, receive threshold 55%

Table 11 Initial Values after Reset (cont'd)

Register	Reset Value	Meaning
LIM5	04_H	Detailed mode selection
LOOP	00_H	Elastic buffer size: 256 bit Local loop off, remote loop off
PCD	$C0_H$	Pulse count "0" for LOS detection is 192
PCR	18_H	Pulse count "1" for LOS recovery is 24 in 192-bit interval
LCR1	40_H	Down code 6 bit, up code 5 bit length
LCR2	09_H	In band loop deactivate code is 001
LCR3	01_H	In band loop activate code is 00001
XPM(2:0)	73_H,02_H,00_H	E1 transmit pulse mask for 120 Ohm
IMR0, IMR1	FF_H, FF_H	All interrupts are disabled
CMR	08_H	DCO reference clock: channel 1, RCLK output: DPLL clock, DCO enabled, DCO internal reference clock, Slave mode

5.3.2 Basic Initialization Settings

For a correct start up of the primary access interface, a set of parameters specific to the system and hardware environment must be programmed after $\overline{RES}$ goes inactive. Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T and ETSI recommendations (e.g. fault conditions and consequent actions). Setting optional parameters makes sense mainly when basic operation via the PCM line is guaranteed. **Table 12** gives an overview of the most important parameters in terms of signals and control bits that are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Parameters for the basic and operational set up, for example, may be programmed simultaneously.

Table 12 Initialization Parameters

Basic Set Up		Registers to be Programmed
Mode select	T1/J1 E1 Short-haul Long-haul	GCR2.PMODx = 1; x = 1 to 4 GCR2.PMODx = 0; x = 1 to 4 LIM1.EQON = 0 LIM1.EQON = 1
Master clock frequency select		GCM(6:1)
Specification of line interface, clock generation and pulse mask		LIM0 LIM1 XPM(2:0)
Output driver enable		XPM2.XLT = 0
Line interface coding		LIM0.XC(1:0) LIM0.RC(1:0)
Loss-of-signal detection/recovery conditions		PCD PCR
Jitter attenuation		LOOP.EJATT LOOP.XJATT

Note: Read access to unused register addresses might return random values and therefore must not be done.

Undefined bit positions at defined register addresses might return random values and must be masked before the register value is used for further computing.

Writing to unused register addresses or reserved registers may produce unpredictable results.

6 Register Description

6.1 Control Register Addresses

Table 13 Control Register Addresses

Address (hexadecimal)				Register	Type	Comment	Page
Ch 1	Ch 2	Ch 3	Ch 4				
00				GCR	R/W	Global Configuration Register	60
20				GCR2	R/W	Global Configuration Register 2	61
01	21	41	61	LIM0	R/W	Line Interface Mode 0	62
02	22	42	62	LIM1	R/W	Line Interface Mode 1	64
03	23	43	63	LIM2	R/W	Line Interface Mode 2	66
04	24	44	64	LIM3	R/W	Line Interface Mode 3	67
05	25	45	65	LIM4	R/W	Line Interface Mode 4	68
06	26	46	66	LIM5	R/W	Line Interface Mode 5	70
07	27	47	67	CMR	R/W	Clock Mode Register	72
08	28	48	68	LOOP	R/W	Loop Register	74
09	29	49	69	XPM0	R/W	Transmit Pulse Mask 0	76
0A	2A	4A	6A	XPM1	R/W	Transmit Pulse Mask 1	76
0B	2B	4B	6B	XPM2	R/W	Transmit Pulse Mask 2	76
0C	2C	4C	6C	PCD	R/W	Pulse Count Detection	79
0D	2D	4D	6D	PCR	R/W	Pulse Count Recovery	79
0E	2E	4E	6E	LCR1	R/W	Loop Code Register 1	80
0F	2F	4F	6F	LCR2	R/W	Loop Code Register 2	81
10	30	50	70	LCR3	R/W	Loop Code Register 3	81
11	31	51	71	IMR0	R/W	Interrupt Mask Register 0	82
12	32	52	72	IMR1	R/W	Interrupt Mask Register 1	82
13	33	53	73	CMDR	R/W	Command Register	83
3D				GCM1	R/W	Global Clock Mode 1	84
3E				GCM2	R/W	Global Clock Mode 2	84
3F				GCM3	R/W	Global Clock Mode 3	85
5D				GCM4	R/W	Global Clock Mode 4	85

Table 13 Control Register Addresses (cont'd)

Address (hexadecimal)				Register	Type	Comment	Page
Ch 1	Ch 2	Ch 3	Ch 4				
5E				GCM5	R/W	Global Clock Mode 5	86
5F				GCM6	R/W	Global Clock Mode 6	86

6.2 Detailed Description of Control Registers

Global Configuration Register (Read/Write)

Address: 00_H

Value after reset: 80_H

	7							0
GCR	0	0	SSF1	SSF0	FSC1	FSC0	R1S1	R1S0

GCR.(7:6) **reserved**, *must* be cleared

SSF(1:0) **Select SYNC Frequency**

The frequency of the reference clock for the DCO circuitry provided on pin SYNC is selected by these bits.

00 = External SYNC frequency: 2.048 MHz (default)

01 = External SYNC frequency: 1.544 MHz

10 = External SYNC frequency: 8 kHz (master mode only)

11 = Not defined

FSC(1:0) **$\overline{\text{FSC}}$ Source**

One of the four internally generated de-jittered 8-kHz clocks is output on port $\overline{\text{FSC}}$.

00 = Sourced by channel 1 (default)

01 = Sourced by channel 2

10 = Sourced by channel 3

11 = Sourced by channel 4

R1S(1:0) **RCLK1 Source**

One of the four internally generated receive route clocks is output on port RCLK1 (available for RCLK1 only, not for RCLK(2:4)).

00 = Extracted receive clock of channel 1 (default)

01 = Extracted receive clock of channel 2

10 = Extracted receive clock of channel 3

11 = Extracted receive clock of channel 4

Global Configuration Register 2 (Read/Write)

Address: 20_H

Value after reset: 00_H

	7							0
GCR2	0	0	IC1	IC0	PMOD4	PMOD3	PMOD2	PMOD1

Note: Unused bits have to be cleared.

GCR2.7 **reserved**

GCR2.6 **reserved**

IC(1:0) **Interrupt Pin Control**

x0 = Open drain, active low (default)

01 = Push-pull, active low

11 = Push-pull, active high

PMOD(4:1) **E1 or T1/J1 Mode of channel (4:1)**

0 = E1 mode (default)

1 = T1/J1 mode

Line Interface Mode 0 (Read/Write)

Addresses: 01_H, 21_H, 41_H, 61_H

Value after reset: 00_H

	7							0
LIM0	XC1	XC0	RC1	RC0	EXZE	PDE	ARL	SIM

XC(1:0) **Transmit Code**

Serial codes for transmitter and receiver can be programmed independently. The single-rail data stream received on port XDIP is encoded as follows:

00 = AMI

01 = HDB3 code for E1 applications

10 = B8ZS code for T1/J1 applications

11 = Encoder is bypassed, XDIN is used as “data input negative"

After any modification of bits XC(1:0), a software reset is required (CMDR.RES = 1). If the encoder is bypassed, hardware tristate function is not available.

RC(1:0) **Receive Code**

The recovered data is decoded and transmitted on pin RDOP in **N**on-**R**eturn-to-**Z**ero (NRZ) format (single-rail or unipolar data).

00 = AMI

01 = HDB3 code for E1 applications

10 = B8ZS code for T1 applications

11 = Decoder is bypassed; RDON is used as "data output negative"

CMI coding is selected by setting LIM1.ECMIR = 1.

After any modification of bits RC(1:0), a software reset is required (CMDR.RES = 1).

EXZE **Excessive Zeros Detection Enable**

Selects line code error detection mode.

E1 mode (GCR2.PMODx = 0):

0 = Only double violations are detected.

1 = Extended code violation detection: 0000 strings are detected additionally. Thereafter, incrementation of code violation counter CVC is done after receiving an additional four zeros.

T1/J1 mode (GCR2.PMODx = 1):

0 = Only bipolar violations are detected.

1 = Bipolar violations and zero strings of 8 or more contiguous zeros in B8ZS code, or more than 15 contiguous zeros in AMI code, are detected additionally and counted in the CVC.

PDE **Pulse-Density Enforcer**

Selects pulse-density enforcement mode for AMI signals. Pulse-density according to ANSI T1.403 is enforced automatically.

0 = Disabled

1 = Enabled

ARL **Automatic Remote Loop**

0 = Disables automatic on/off switching for the remote loop upon detecting the in-band loop activate/deactivate code.

1 = Enables automatic on/off switching for the remote loop upon detecting the in-band loop activate/deactivate code. Activate and deactivate codes are user-programmable. When the in-band loop activate code (e.g. 00001) is detected for at least 5 s, the remote loop is automatically switched on until the deactivate code (e.g. 001) is detected for 5 s or the bit LIM0.ARL is cleared.
Automatic remote loop switching can be activated with or without jitter attenuation, depending on bit LOOP.EJATT.

SIM **Alarm Simulation**

0 = Internal alarm simulation inactive.

1 = Internal alarm simulation active. Initiates internal error simulation of alarm indication signal, loss-of-signal, slip, code violations, PRBS errors and loss of transmit clock. The CVC and BECL/H error counters are incremented.

Line Interface Mode 1 (Read/Write)

Addresses: 02_H, 22_H, 42_H, 62_H

Value after reset: 00_H

	7							0
LIM1	PD	EQON	ECMIR	RDON1	RDON0	ECM	ECMIX	XAIS

PD **Power Down**

Switches the appropriate channel between power-up and power-down mode.

0 = Power up

1 = Power down

EQON **Receive Equalizer On**

0 = -10 dB Receiver: short-haul mode

1 = -43 dB Receiver: long-haul mode (E1)

-36 dB Receiver: long-haul mode (T1/J1)

ECMIR **Enable CMI Receive Interface**

0 = The ternary interface is selected. Multifunction ports RL1/2 become analog inputs.

1 = The digital CMI receive interface is selected. Received data is latched on multifunction port ROID.

RDON(1:0) **RDON Pin Input/Output Multiplexer Select**

00 = RDON output

01 = BPV output (bipolar violations)

10 = SCLKO output

11 = SCLKI input

ECM **Error Counter Mode**

The function of the error counters is determined by this bit.

0 = Before reading an error counter, the corresponding bit in the command register (CMDR) has to be set. The low byte of the error counter should always be read before the high byte. The error counter is reset with the rising edge of the corresponding bits (DBEC, DCVC) in the CMDR register.

1 = Every second the error counter is latched and then reset automatically. The latched error counter state must be read within the next second, otherwise data is overwritten. Avoid reading the error counter during updating.

ECMIX **Enable CMI Transmit Interface**

0 = The ternary interface is selected. XL1/2 are used as analog outputs.

1 = The digital CMI receive interface is selected. Transmitted data is output on port XOID.

XAIS **Transmit AIS towards Remote End**

0 = Normal transmit operation.

1 = Sends AIS via ports XL1/XL2 towards the remote end. The outgoing data stream which can be looped back via the local loop to the framer interface is not affected.

Line Interface Mode 2 (Read/Write)

Addresses: 03_H, 23_H, 43_H, 63_H

Value after reset: 40_H

	7							0
LIM2	RIL2	RIL1	RIL0	SLT1	SLT0	0	RD1	RD0

RIL(2:0) **Receive Input Threshold**

Only valid if analog line interface is selected (LIM1.ECMIR = 0).

"No signal" is declared if the voltage between pins RL1 and RL2 drops below the limit programmed through bits RIL(2:0) and the received data stream has no transition for a period defined in the PCD register.

Please see the selectable voltage levels in chapter **Chapter 7.3** on **page 102**.

Note: LIM2.RIL(2:0) must be programmed before LIM1.EQON = 1 is set (long-haul mode).

SLT(1:0) **Receive Slicer Threshold**

00 = The receive slicer generates a mark (digital one) if the voltage on RL1/2 exceeds 55% of the peak amplitude (default).

01 = The receive slicer generates a mark (digital one) if the voltage on RL1/2 exceeds 67% of the peak amplitude.

10 = The receive slicer generates a mark (digital one) if the voltage on RL1/2 exceeds 50% of the peak amplitude.

11 = The receive slicer generates a mark (digital one) if the voltage on RL1/2 exceeds 45% of the peak amplitude.

RD(1:0) **Select Receive Data Output**

These bits select the different stages of the received data path.

00 = Received data is decoded (HDB3/B8ZS/AMI) and output on RDOP/N.

01 = Data recovered by the DPLL (not decoded) is output on RDOP/N.

10 = Sliced data is transferred directly to RDOP/N.

11 = Sliced data is directly transferred to RDOP/N and the bypassed receive path logic is switched off to reduce power consumption unless remote loop is activated.

Line Interface Mode 3 (Read/Write)

Addresses: 04_H, 24_H, 44_H, 64_H

Value after reset: 00_H

	7							0
LIM3	LBO2	LBO1	GTP	MTP	EPRM	XPRBS	IPRBS	SPRBS

LBO(2:1) **Line Build-Out (T1 mode only)**

In long-haul applications, LIM1.EQON = 1, a transmit filter can be optionally placed in the transmit path to attenuate the signal level on pins XL1/2. Selecting the transmitter attenuation is possible in steps of 7.5 dB at 772kHz, which meets FCC Part 68 and ANSI T1.403.

To meet the line build-out characteristics defined by ANSI T1.403, registers XPM(2:0) should be programmed as follows:

00 = 0 dB

01 = -7.5 dB -->XPM(0:2) = 11_H , 02_H , 20_H

10 = -15 dB -->XPM(0:2) = $8E_H$, 01_H , 20_H

11 = -22.5 dB -->XPM(0:2) = 09_H , 01_H , 20_H

GTP **PRBS/IBL Generator in Transmit Path**

0 = The PRBS/IBL generator is placed in the receive path.

1 = The PRBS/IBL generator is placed in the transmit path.

MTP **PRBS/IBL Monitor in Transmit Path**

0 = The PRBS/IBL monitor is placed in the receive path.

1 = The PRBS/IBL monitor is placed in the transmit path.

EPRM **Enable PRBS Monitor**

0 = The PRBS monitor is disabled.

1 = The PRBS monitor is enabled.

XPRBS **Transmit Pseudo-Random Bit Sequence (PRBS)**

0 = Normal transmit operation

1 = A “1” in this bit position enables transmission of a pseudo-random bit sequence. Depending on bit SPRBS, the PRBS is generated according to 2^{15} -1 or 2^{20}-1 (ITU-T O.151).

IPRBS **Invert Pseudo-Random Bit Sequence PRBS**

0 = The generated PRBS data is not inverted.

1 = The PRBS data is inverted.

SPRBS **Select Pseudo-Random Bit Sequence Algorithm**

0 = Pseudo-random bit sequence algorithm: 2^{15} -1

1 = Pseudo-random bit sequence algorithm: 2^{20} -1 with maximum 14 consecutive zeros restriction.

Line Interface Mode 4 (Read/Write)

Addresses: 05_H, 25_H, 45_H, 65_H

Value after reset: 00_H

	7							0
LIM4	RPE	TPE	VIS	SCI	DCF	PC2	PC1	PC0

RPE **RCLK Positive Edge**

0 = RDOP/N are output with the falling edge of the RCLK clock.

1 = RDOP/N are output with the rising edge of the RCLK clock.

TPE **Positive Sample Edge of TCLK**

0 = XDIP/N are latched with the falling edge of the TCLK clock.

1 = XDIP/N are latched with the rising edge of the TCLK clock.

VIS **Masked Interrupts Visible**

0 = Masked interrupt status bits are not visible in registers ISR(0:1).

1 = Masked interrupt status bits are visible in ISR(0:1), but they are not visible in register CIS. Interrupt request pin INT stays inactive.

SCI **Status Change Interrupt**

0 = Interrupts are generated either at the beginning or end of the internal interrupt event.

1 = The following interrupts are activated if enabled upon detection and recovering of the internal interrupt source:
ISR0.LOS , ISR0.AIS, ISR0.PDENI, ISR1.LTC

DCF **Disable Center Frequency of DCO circuitry**

Only valid if master mode (CMR.MAS = 1) is selected.

0 = Automatic centering of the DCO circuitry is enabled.

1 = Automatic centering of the DCO circuitry is disabled.

PC(2:0) **MFP Port Configuration**

These bits select the output pin function of multifunction port MFP.

000 = Loss-of-signal (red alarm) indication

001 = Analog loss-of-signal indication

010 = Pseudo-random bit sequence synchronization status

011 = Bipolar violation indication

100 = Transmit line short status

101 = Alarm indication signal

110 = Not defined

111 = Not defined

Line Interface Mode 5 (Read/Write)

Addresses: 06_H, 26_H, 46_H, 66_H

Value after reset: 04_H

	7							0
LIM5			ACS	XDPM	XLB	XLM	LOSR1	LOSR0

ACS **Automatic Clock-Switching**

If TCLK is missing, the transmit clock can optionally be switched to the SYNC clock automatically.

0 = Automatic switching is disabled (default); if TCLK is missing, XL1/2 are undefined.

1 = Automatic switching is enabled; if TCLK is missing, SYNC is used, if SYNC is also missing, XL1/2 are undefined.

XDPM **Transmit Data Performance Monitoring**

To verify transmit data, the receive line supervision circuitry can be switched to the transmit path. If selected, data input on pins XDIP/ XDIN is checked for **B**i**P**olar **V**iolations (BPV), **EX**zessive **Z**eros (EXZ) and **L**oss **O**f **S**ignal (LOS).

0 = Receive path (default)

1 = Transmit path

Note: Transmit data performance monitoring is not possible in remote loop configuration. LIM2.RD(1:0) = 10 is required.

XLB **Transmit Line Biasing**

The analog circuit of the transmit line driver can be switched into a power saving mode. This slightly reduces the output slopes on XL1/2.

0 = Normal operation (default)

1 = Power-saving operation

XLM **Transmit Line Monitor Enable**

The transmit line monitor circuit can be switched off to reduce power consumption.

0 = Transmit line monitor is off.

1 = Transmit line monitor is active (default).

LOSR(1:0) **Loss-of-Signal Recovery Condition**

00 = The LOS alarm is cleared if the predefined pulse-density (register PCR) is detected during the time interval which is defined by register PCD.

01 = In addition to the recovery condition described above a LOS alarm is cleared only if the pulse-density requirement (defined by PCR and PCD) is fulfilled and no more than 15 contiguous zeros are detected during the recovery interval.

10 = A LOS alarm is not terminated, if at the end of the pulse position interval any subinterval of 100 pulse positions contains no pulses of either polarity (ANSI T1.231). This means, clearing a LOS alarm is done only if the pulse-density requirement (defined by PCR and PCD) is fulfilled and no more than 99 contiguous zeros are detected during the recovery interval.

11 = In addition to the recovery condition described for "00" a LOS alarm is cleared only if the pulse-density requirement (defined by PCR and PCD) is fulfilled and no more than 8 contiguous zeros are detected during the recovery interval.

Clock Mode Register (Read/Write).

Addresses: 07_H, 27_H, 47_H, 67_H

Value after reset: 08_H , 58_H, $A8_H$, $F8_H$

	7							0
CMR	DSS1	DSS0	RS1	RS0	DCS	SCF	ELT	MAS

DSS(1:0) **DCO Synchronization Clock Source**

DCO in receive path:
These bits select the reference clock source for the DCO circuitry.

00 = Receive reference clock generated by the DPLL of channel 1

01 = Receive reference clock generated by the DPLL of channel 2

10 = Receive reference clock generated by the DPLL of channel 3

11 = Receive reference clock generated by the DPLL of channel 4

DCO in transmit path:
These bits select the reference clock source for the DCO circuitry.

00 = Reference clock for the DCO is TCLK1

01 = Reference clock for the DCO is TCLK2

10 = Reference clock for the DCO is TCLK3

11 = Reference clock for the DCO is TCLK4

Note: After Reset all DCO circuitries synchronize with the clock sourced by the DPLL of channel 1 . Each channel has to be configured individually.
If CMR.MAS is set, the DCO circuitry synchronizes with the clock applied on port SYNC.

RS(1:0) **Select RCLK Source**

These bits select the source of RCLK.

00 = Extracted receive clock generated by the DPLL is used

If jitter attenuation is selected in receive direction and external SCLKI is not used (LOOP.XJATT = 0, LOOP.EJATT = 1, LIM1.RDON(1:0) ≠ 11), de-jittered 2.048 (E1)/1.544 MHz (T1/J1) clock generated by the internal DCO circuitry is used.

01 = Extracted receive clock; in case of an active LOS alarm RCLK is set high.

10 = De-jittered 2.048 (E1)/1.544 MHz (T1/J1) clock generated by the internal DCO circuitry is used.

11 = Not defined

DCS **Disable Clock-Switching**

In slave mode (CMR.MAS = 0), the DCO is synchronized with the recovered route clock. In case of LOS (receive mode) or LSR1.TCS = 1 (transmit mode), the DCO switches to the clock sourced by port SYNC. If this bit is set, automatic switching from RCLK (receive mode) or TCLK (transmit mode) to SYNC is disabled (default).

SCF **Select Corner Frequency of DCO**

Setting this bit reduces the corner frequency of the DCO circuit by the factor of ten from 2 Hz (E1)/6 Hz (T1/J1) to 0.2 Hz (E1)/0.6 Hz (T1).

Note: Reduction of the corner frequency of the DCO circuitry increases the time required for synchronization.

ELT **Enable Loop-Timed**

0 = Normal operation

1 = Transmit clock is generated from the clock supplied by MCLK, which is synchronized with the extracted receive route clock. In this configuration, the transmit elastic buffer has to be enabled.

MAS **Master Mode**

0 = Slave mode

1 = Master mode on. Setting this bit the DCO circuitry is frequency synchronized with the clock (2.048 MHz, 1.544 MHz or 8 kHz) supplied on pin SYNC. If this pin is connected to V_{SS} or V_{DD}, the DCO circuitry is centered and no receive jitter attenuation is performed. The generated clocks are stable.

Loop Register (Read/Write)

Addresses: 08_H, 28_H, 48_H, 68_H

Value after reset: 00_H

	7							0
LOOP	XJATT	EJATT	RL	LL	DLB	LOSDAT	BS1	BS0

XJATT **Jitter Attenuator Position**

0 = The elastic buffer is placed in the receive path.

1 = The elastic buffer is placed in the transmit path.

EJATT **Enable Jitter Attenuator**

0 = The elastic buffer is disabled.

1 = The elastic buffer is enabled.

RL **Remote Loop**

0 = Remote loop is switched off.

1 = Remote loop is switched on. The remote loop-back mode disconnects the transmit data received on XDIP/N from the transmitter. Received data on pins RL1/2 is looped back to the line interface with or without jitter attenuation. The decoder and encoder are ignored.
If LIM0.ARL (automatic remote loop) is selected and no valid ARL condition is decoded, the remote loop stays active until RL is reset (higher priority of RL compared to ARL)

LL **Local Loop**

Analog line applications (LIM1.ECMIR = 0)

0 = Local loop is switched off.

1 = Local loop is switched on. Data received on ports XDIP/N is looped back through the analog receiver to pins RDOP/N. An alarm indication signal (blue signal) can be sent to the remote end (LIM1.XAIS). Data received on ports RL1/2 is ignored. Receiver and transmitter coding must be identical.

DLB **Digital Loop-Back**

Digital line applications (LIM1.ECMIR = 1)

0 = Digital loop-back disabled.

1 = Digital loop-back enabled. Data received on ports XDIP/N is looped back to pins RDOP/N. Optinally an alarm indication signal (blue signal) can be sent to the remote end (LIM1.XAIS).

Data received on ports RL1/2 is ignored. Receiver and transmitter coding must be identical.

LOSDAT **Data Stream Clear in Case of LOS**

0 = If LOS is detected, data is processed, bit errors may occur

1 = If LOS is detected, data is cleared to avoid bit errors

BS(1:0) **Buffer Size**

00 = 256 bits

01 = 128 bits

10 = 64 bits

11 = 32 bits

Transmit Pulse Mask (0:2) (Read/Write)

Addresses XPM0: 09_H, 29_H, 49_H, 69_H
Addresses XPM1: $0A_H$, $2A_H$, $4A_H$, $6A_H$
Addresses XPM2: $0B_H$, $2B_H$, $4B_H$, $6B_H$

Value after reset: 73_H, 02_H, 00_H

	7							0
XPM0	XP12	XP11	XP10	XP04	XP03	XP02	XP01	XP00
XPM1	XP30	XP24	XP23	XP22	XP21	XP20	XP14	XP13
XPM2	XLLP	XLT	DAXLT	XLHC	XP34	XP33	XP32	XP31

The transmit pulse shape is output on pins XL1 and XL2. The level of the pulse shape is programmed via registers XPM(2:0) to create a custom waveform. In order to get an optimized pulse shape for the external transformers, each pulse shape is internally devided into four sub-pulse shapes. In each sub-pulse shape, a programmable 5-bit value defines the level of the analog voltage on pins XL1 and XL2. Together four 5-bit values have to be programmed to form one complete transmit pulse shape. The four 5-bit values are sent in the following sequence:

XP04 to 00: First pulse shape level
XP14 to 10: Second pulse shape level
XP24 to 20: Third pulse shape level
XP34 to 30: Fourth pulse shape level

Changing the LSB of each subpulse in registers XPM(2:0) changes the amplitude of the differential voltage on XL1/2 by approximately 80 mV.

Example for E1 mode:

120 Ω interface and wired as shown in **Figure 13** on **page 45**.

XPM04 to 00: $1B_H$
XPM14 to 10: $1B_H$
XPM24 to 20: 00_H
XPM34 to 30: 00_H

Programming values for XPM(0:2): $7B_H$, 03_H, 00_H

Example for T1 mode

The XPM values are valid for the following external circuitry:

Transformer ratio: 1:2.4;

Cable: PULB 22AWG (100 Ω);

Serial resistors: 2 Ω.

Table 14 Pulse Shaper Programming

Range in m	Range in ft.	XPM0	XPM1	XPM2	XP04-XP00	XP14-XP10	XP24-XP20	XP34-XP30
		hexadecimal			decimal			
0 to 40	0 to 133	D7	1E	11	23	22	7	2
40 to 81	133 to 266	D8	22	11	24	22	8	2
81 to 122	266 to 399	FC	2A	11	28	23	10	2
122 to 162	399 to 533	FD	C6	11	29	23	17	3
162 to 200	533 to 655	DF	D6	11	31	22	21	3

XLLP **Reserved**

0 = Normal operation

1 = Reserved (not to be used)

XLT **Transmit Line Tristate**

0 = Normal operation

1 = Transmit line XL1/XL2 is switched into high-impedance state. If this bit is set, the transmit line monitor status information is frozen. This bit is functionally ored with pin TRIST unless XDIN function is used during decoder bypass.

DAXLT **Disable Automatic Tristating of XL1/2**

0 = Normal operation. If a short is detected on pins XL1/2, the transmit line monitor sets the XL1/2 outputs into a high-impedance state.

1 = If a short is detected on XL1/2 pins, automatically setting these pins into a high-impedance (by the XL-monitor) state is disabled.

XLHC **Transmit Line High Current**

0 = Output current less than 50 mA

1 = Output current more than 50 mA
To be selected for T1/J1 mode or E1 mode.

Pulse Count Detection Register (Read/Write)

Addresses: $0C_H$, $2C_H$, $4C_H$, $6C_H$

Value after reset: $C0_H$

	7						0
PCD	PCD7						PCD0

PCD(7:0) **Pulse Count Detection**

An LOS alarm is detected if the incoming data stream has no transitions for a programmable number T of consecutive pulse positions. The number T is programmable via the PCD register and can be calculated as follows:
$T = 16 \times (PCD+1)$; with $0 \leq PCD \leq 255$.

The maximum time is $256 \times 16 \times 488$ ns = 2 ms in E1 mode, or $256 \times 16 \times 648$ ns = 2.65 ms in T1 mode. Every detected pulse resets the internal pulse counter. The counter is clocked with the receive clock RCLK.

Pulse Count Recovery (Read/Write)

Addresses: $0D_H$, $2D_H$, $4D_H$, $6D_H$

Value after reset: 18_H

	7						0
PCR	PCR7						PCR0

PCR(7:0) **Pulse Count Recovery**

An LOS alarm is cleared if a pulse-density is detected in the received bit stream. The number of pulses M which must occur in the predefined PCD time interval is programmable via the PCR register, and can be calculated as follows:

$M = N + 1$; with $0 \leq N \leq 255$.

The time interval starts with the first detected pulse transition. With every received pulse, a counter is incremented and the actual counter is compared with the contents of PCR register. If the pulse number is greater or equal to the PCR value, the LOS alarm is reset. Otherwise the alarm stays active. In this case, the next detected pulse transition starts a new time interval.

Loop Code Register 1 (Read/Write)[1)]

Addresses: $0E_H$, $2E_H$, $4E_H$, $6E_H$

Value after reset: 40_H

	7							0
LCR1	LDCL1	LDCL0	LACL1	LACL0			XLD	XLA

LDCL(1:0) **Length Deactivate (Down) Code**

These bits defines the length of the user-programmable LLB deactivate code, which is programmable in register LCR2.

00 = 5 bit

01 = 6 bit (default)

10 = 7 bit

11 = 8 bit

If a shorter pattern length is required, select a multiple of the required length and repeat the pattern in LCR2.

LACL(1:0) **Length Activate (Up) Code**

These bits defines the length of the user-programmable LLB activate code, which is programmable in register LCR3.

00 = 5 bit (default)

01 = 6 bit

10 = 7 bit

11 = 8 bit

If a shorter pattern length is required, select a multiple of the required length and repeat the pattern in LCR3.

XLD **Transmit LLB Deactivate (Down) Code**

0 = Normal operation (default)

1 = Normal data is replaced by the LLB deactivation code continuously until this bit is reset.
LCR1.XLA and LIM3.XPRBS must be cleared. LLB deactivate code can be inserted in receive (LIM3.GTP = 0) or transmit direction (LIM3.GTP = 1).

1) Terms "**L**ine **L**oop **B**ack" (LLB) and "**I**n **B**and **L**oop" (IBL) are synonyms.

XLA **Transmit LLB Activate (Up) Code**

0 = Normal operation (default)

1 = Normal data is replaced by the LLB activate code continuously until this bit is reset.
LCR1.XLD and LIM3.XPRBS must be cleared. LLB activate code can be inserted in receive (LIM3.GTP = 0) or transmit direction (LIM3.GTP = 1).

Loop Code Register 2 (Read/Write)

Addresses: $0F_H$, $2F_H$, $4F_H$, $6F_H$

Value after reset: 09_H

	7						0
LCR2	LDC7						LDC0

LDC(7:0) **Line Loop-Back Deactivate Code**

If enabled by bit LCR1.XLD, the LLB deactivate code is repeated automatically until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LDC0 is transmittted last. If the selected code length is less than 8 bits, the leftmost bits of LCR2 are ignored. For correct operations, bit LIM3.XPRBS has to be cleared. The default setting is (00)001001 (6-bit mode is default in LCR1). This generates the standard deactivation code "001".

Loop Code Register 3 (Read/Write)

Addresses: 10_H, 30_H, 50_H, 70_H

Value after reset: 01_H

	7						0
LCR3	LAC7						LAC0

LAC(7:0) **Line Loop-Back Activate Code**

If enabled by bit LCR1.XLA, the LLB activate code is repeated automatically until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LAC0 is transmittted last. If the selected code length is less than 8 bits, the leftmost bits of LCR3 are ignored. For correct operations, bit LIM3.XPRBS has to be cleared. The

default setting is (000)00001 (5-bit mode is default in LCR1). This generates the standard activate code "00001".

Example:

Transmit LLB/IBL activate Code = 00001

Register setting LCR1: xx00xx01

Register setting LCR3: xxx00001

Interrupt Mask Register (0:1) (Read/Write)

Addresses IMR0: 11_H, 31_H, 51_H, 71_H
Addresses IMR1: 12_H, 32_H, 52_H, 72_H

Value after reset: FF_H, FF_H

	7							0
IMR0	LLBSCM	XLSCM	PRBSSCM	SLNM	SLPM	PDENM	AISM	LOSM
IMR1							LTCM	SECM

IMR(0:1) **Interrupt Mask Register**

Each interrupt source can generate an interrupt signal on port INT. A "1" in a bit position of IMR(0:1) sets the mask active for the interrupt status in ISR(0:1). Masked interrupt statuses neither generate a signal on INT, nor are they visible in register CIS. Moreover, they are

– not displayed in the ISR if bit LIM4.VIS is cleared

– displayed in the ISR if bit LIM4.VIS is set

*Note: After reset, all interrupts are **dis**abled.*
See register ISR0/1 for detailed description of bit functions.

Command Register (Read/Write)

Addresses: 13_H, 33_H, 53_H, 73_H

Value after reset: 00_H

	7							0
CMDR	RES			IBV	IPE	CEB	DBEC	DCVC

Note: The maximum time between writing to the CMDR register and the execution of the command takes 2.5 periods of the current line data rate. Register bits are set by software and reset by hardware automatically after the required operation has been completed. Register bits in CMDR cannot be reset by software.

RES **Reset Receiver and Transmitter**

The receive and the transmit line interface (except the clock and data recovery unit DPLL) are reset. The contents of the control registers is not deleted.

IBV **Insert Bipolar Violations**

Setting this bit forces a bipolar violation in the transmit data stream. Violations are inserted at the next possible position. Ones preceded by two or more zeros are not converted into violations.

Example (V = inserted violation):

001000010100 is converted to 001000010V00

IPE **Insert PRBS Error**

Setting this bit forces a PRBS error in the outgoing data stream (if PRBS transmission is enabled).

CEB **Center Elastic Buffer**

Setting this bit forces the delay through the elastic buffer to half of the current buffer size (LOOP.BS1/0).

DBEC **Disable Pseudo-Random Binary Sequence Error Counter**

This bit is only valid if LIM1.ECM is cleared. It must be set before reading the error counter. This bit is reset automatically if the corresponding error counter high byte has been read. With the rising edge of this bit the error counter is latched and then cleared.

DCVC **Disable Code Violation Counter**

See bit DBEC.

Global Clock Mode Register 1 (Read/Write)

Address: $3D_H$

Value after reset: 00_H

	7							0
GCM1	PHD_E17	PHD_E16	PHD_E15	PHD_E14	PHD_E13	PHD_E12	PHD_E11	PHD_E10

PHD_E1(0:7) **Frequency Adjust for E1**

For details, see "**Flexible Clock Mode Settings**" on **page 87**.

Global Clock Mode Register 2 (Read/Write)

Address: $3E_H$

Value after reset: 00_H

	7							0
GCM2	DVM_E12	DVM_E11	DVM_E10	VFREQ_EN	PHD_E111	PHD_E110	PHD_E19	PHD_E18

DVM_E1(0:2) **Divider Mode for E1**

000 = Not valid
001 = DIV_E1 = 3
010 = DIV_E1 = 4 1/6
011 = DIV_E1 = 4
100 = DIV_E1 = 5.5
101 = DIV_E1 = 5 1/3
110 = DIV_E1 = 5 2/3
111 = Not valid

VFREQ_EN **Variable Frequency Enable**

0 = Fixed clock frequency of 2.048 (E1) or 1.544 MHz (T1/J1)
1 = Variable master clock frequency

PHD_E1(8:11) **Frequency Adjust for E1**

For details, see "**Flexible Clock Mode Settings**" on **page 87**.

Global Clock Mode Register 3 (Read/Write)

Address: $3F_H$

Value after reset: 00_H

	7							0
GCM3	PHD_T1 7	PHD_T1 6	PHD_T1 5	PHD_T1 4	PHD_T1 3	PHD_T1 2	PHD_T1 1	PHD_T1 0

PHD_T1(0:7) **Frequency Adjust for T1**

For details, see "**Flexible Clock Mode Settings**" on **page 87**.

Global Clock Mode Register 4 (Read/Write)

Address: $5D_H$

Value after reset: 00_H

	7							0
GCM4	DVM_T12	DVM_T11	DVM_T10	0	PHD_T1 11	PHD_T1 10	PHD_T1 9	PHD_T1 8

DVM_T1(0:2) **Divider Mode for T1**

000 = Not valid
001 = DIV_T1 = 3
010 = DIV_T1 = 4 1/6
011 = DIV_T1 = 4
100 = DIV_T1 = 5.5
101 = DIV_T1 = 5 1/3
110 = DIV_T1 = 5 2/3
111 = Not valid

PHD_T1(8:11) **Frequency Adjust for T1**

For details, see "**Flexible Clock Mode Settings**" on **page 87**.

Global Clock Mode Register 5 (Read/Write)

Address: $5E_H$

Value after reset: 00_H

	7							0
GCM5	MCLK_ LOW			PLL_M 4	PLL_M 3	PLL_M 2	PLL_M 1	PLL_M 0

MCLK_LOW **Master Clock Range Low**

0 = Master clock frequency divided by (PLL_M + 1) is greater than or equal to 1.5 MHz

1 = Master clock frequency divided by (PLL_M + 1) is less than 1.5 MHz

PLL_M(0:4) **PLL Dividing Factor M**

For details, see "**Flexible Clock Mode Settings**" on **page 87**.

Note: Write operations to GCM5 initiate a PLL reset (see below).

Global Clock Mode Register 6 (Read/Write)

Address: $5F_H$

Value after reset: 00_H

	7							0
GCM6				PLL_N 4	PLL_N 3	PLL_N 2	PLL_N 1	PLL_N 0

PLL_N(0:4) **PLL Dividing Factor N**

For details, see "**Flexible Clock Mode Settings**" on **page 87**.

Note: Write operations to GCM6 initiate a PLL reset (see below).

Flexible Clock Mode Settings

If flexible master clock mode is used (VFREQ_EN = 1), the according register settings can be calculated as follows (a windows-based program for automatic calculation is available, see **Chapter 9.2** on **page 119**). For some of the standard frequencies see the table below.

1. PLL_M and PLL_N must satisfy the equations:

a. 1.5 MHz ≤ f_{MCLK}/(PLL_M + 1) ≤ 2.048 MHz

b. If a. is not possible, set MCLK_LOW and fulfill
1.02 MHz ≤ f_{MCLK}/(PLL_M + 1) ≤ 1.5 MHz

c. 65 MHz ≤ f_{MCLK} × (2×PLL_N + 2)/(PLL_M + 1) ≤ 69.7 MHz
(as high as possible within this range)

2. Selection of best dividing mode:

f_{outE1} = (f_{MCLK} × (2×PLL_N+2)/(PLL_M+1))/DIV_E1 (target E1: 16.384 MHz)
f_{outT1} = (f_{MCLK} × (2×PLL_N+2)/(PLL_M+1))/DIV_T1 (target T1: 12.352 MHz)

If the target frequency cannot be reached exactly, the dividing mode has to be selected to reach a frequency that is as near as possible to the target frequency.

3. Calculation of correction value (frequency mismatch correction)

PHD_E1 = 6 × 4096 × [DIV_E1 - (2×PLL_N+2)/(PLL_M+1) × (f_{MCLK}/16.384 MHz)]

PHD_T1 = 6 × 4096 × [DIV_T1 - (2×PLL_N+2)/(PLL_M+1) × (f_{MCLK}/12.352 MHz)]

The result of these equations is between -2048 and +2047. Negative values are represented in 2s-complement format (e.g., $-2000_D = 830_H$; $+2000_D = 7D0_H$).

Table 15 Clock Mode Register Settings for E1 or T1/J1

f_{MCLK} [MHz]	GCM1	GCM2	GCM3	GCM4	GCM5	GCM6
1.544	$F0_H$	51_H	00_H	80_H	00_H	15_H
2.048	00_H	58_H	$D2_H$	$C2_H$	00_H	10_H
8.192	00_H	58_H	$D2_H$	$C2_H$	03_H	10_H
10.000	90_H	51_H	81_H	$8F_H$	04_H	10_H
12.352	$F0_H$	51_H	00_H	80_H	07_H	15_H

6.3 Status Register Addresses

Table 16 Status Register Addresses

Address (hexadecimal)				Register	Type	Comment	Page
Ch 1	Ch 2	Ch 3	Ch 4				
14	34	54	74	LSR0	R	Line Status Register 0	89
15	35	55	75	LSR1	R	Line Status Register 1	91
16	36	56	76	RES	R	Receive Equalizer Status	92
17	37	57	77	ISR0	R	Interrupt Status Register 0	93
18	38	58	78	ISR1	R	Interrupt Status Register 1	94
19	39	59	79	CVCL	R	Code Violation Counter Low	96
1A	3A	5A	7A	CVCH	R	Code Violation Counter High	96
1B	3B	5B	7B	BECL	R	PRBS Bit Error Counter Low	97
1C	3C	5C	7C	BECH	R	PRBS Bit Error Counter High	97
60				CIS	R	Channel Interrupt Status	95
7F				VSTR	R	Version Status Register[1)]	97

[1)] The device version number for PEB 22504 V1.1 is 00_h.

6.4 Detailed Description of Status Registers

Line Status Register 0 (Read)

Addresses: 14_H, 34_H, 54_H, 74_H

	7							0
LSR0	LOS	AIS	PDEN	EXZD	RLS	PRBSS	LLBAD	LLBDD

LOS **Loss-of-Signal (Red Alarm)**

The loss-of-signal (LOS) detection offers the flexibility to fulfill allmost all LOS requirements on the market (e.g. ANSI T1.403/231, TR-WT-499, ITU-T G.775, ETS 300233).

Detection:
This bit is set when the incoming signal has no transitions in a time interval of T consecutive pulses, where T is programmable via PCD register.
Total count of consecutive pulses: 16 < T < 4096.

The receive signal level where “no transition” is declared is defined by the programmed value of LIM2.RIL(2:0).

Recovery:
The bit is reset when the incoming signal has transitions with signal levels greater than the programmed receive input level (LIM2.RIL(2:0)) for at least M pulse periods defined by register PCR in the PCD time interval.
An interrupt status bit (ISR0.LOS) is set with the rising edge of this bit. For additional recovery conditions according to ANSI T1.231, refer also to register LIM5.LOSR(1:0).
The bit is also set during alarm simulation, and is reset if LIM0.SIM is cleared and no alarm condition exists.

AIS **Alarm Indication Signal (Blue Alarm)**

The AIS alarm is detected according to ITU-T G.775 and ANSI T1.231 standards.

E1 mode:

This bit is set when the incoming signal has fewer than three zeros in each of two consecutive 512-bit periods. This bit is cleared when each of two consecutive 512-bit periods contains three or more zeros.

T1/J1 mode:

This bit is set when fewer than six zeros are detected within a time interval of 3 ms received on RL1/2.

The bit is also set during alarm simulation, and reset if LIM0.SIM is cleared and no alarm condition exists.

An interrupt status bit (ISR0.AIS) is set with the rising edge of this bit.

PDEN **Pulse-Density Violation**

This bit indicates that the pulse-density of the received data stream defined by ANSI T1.403 is violated. More than 15 consectuive zeros or fewer than N ones are detected in each time window of $8 \times (N+1)$ digit time slots with N taking on all values of 1 to 23.

The bit is cleared if the pulse-density fulfills the above requirement within 23 received ones or automatically after a read access.

The bit is also set during alarm simulation.

EXZD **Exzessive Zeros Detected**

Significant only if exzessive zero detection is enabled by setting LIM0.EXZE = 1. Detection is done according to ANSI T1.231 requirements.
The bit is set after detection of more than three (HDB3;E1), seven (B8ZS ;T1/J1) or 15 (AMI;T1/J1) contiguous zeros in the received bit stream. This bit is cleared when read.

RLS **Remote Loop Status**

Any change of this bit causes an ISR0.LLBSC interrupt.

0 = The remote loop is inactive. If enabled by bit LIM0.ARL, the remote loop is switched off automatically upon detection of the in-band loop deactivate code for at least 5 s, according to ANSI T1. 403 requirements.

1 = The remote loop is active (closed). If enabled by bit LIM0.ARL, the remote loop is switched on automatically upon detection of the in-band loop activate code for at least 5 s.

PRBSS **Pseudo-Random Binary Sequence Status**

The current status of the PRBS synchronizer is indicated in this bit. It is set if the synchronous state is reached, even in the presence of a bit error rate less than or equal to 10^{-1}. A data stream containing all zeros with or without framing bits is also a valid pseudo-random bit sequence. The bit is also set during alarm simulation.

LLBDD **Line Loop-Back Deactivation Signal Detected**

This bit is set if the LLB deactivate signal is detected and then received over a period of more than 25 ms (E1) or 33.16 ms (T1) ,with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}.

If automatic remote loop switching is disabled (LIM0.ARL = 0), any change of this bit causes an LLBSC interrupt.

LLBAD **Line Loop-Back Activation Signal Detected**

This bit is set if the LLB activate signal is detected and then received over a period of more than 25 ms (E1) or 33.16 ms (T1), with a bit error rate less than 10^{-2}. The bit remains set as long as the bit error rate does not exceed 10^{-2}.

If automatic remote loop switching is disabled (LIM0.ARL = 0), any change of this bit causes an LLBSC interrupt.

Line Status Register 1 (Read)

Addresses: 15_H, 35_H, 55_H, 75_H

	7							0
LSR1						TCS	XLS	XLO

TCS **Transmit Clock Status**

This bit is set if the transmit clock derived from TCLK failed to occur for at least eight TCLK periods. The DCO reference is switched to SYNC if not disabled by CMR.DCS. The transmit lines XL1/2 are tristated automatically. With the first detected edge of the transmit clock, this bit is cleared and tristating of XL1/2 is disabled. Additionally, the interrupt status bit ISR1.LTC is set. MCLK must be active because the reference frequency to detect a TCLK loss is derived from this clock. The bit is also set during alarm simulation.

XLS **Transmit Line Short**

Significant only if the ternary line interface is selected by LIM1.ECMIX = 0.

0 = Normal operation. No short is detected.

1 = The XL1 and XL2 are shortened for at least three pulses. As a reaction of the short, pins XL1 and XL2 are automatically forced into a high-impedance state if bit XPM2.DAXLT is reset. After 128 consecutive pulse periods, outputs XL1/2 are activated again and the

internal transmit current limiter is checked. If a short between XL1/2 is still active, outputs XL1/2 are in high-impedance state again. When the short disappears, pins XL1/2 are activated automatically and this bit is reset. With any change of this bit, an interrupt ISR0.XLSC is generated. If XPM2.XLT is set, this bit is frozen.

XLO **Transmit Line Open**

0 = Normal operation

1 = This bit is set if at least 32 consecutive zeros were sent via pins XL1/XL2. This bit is reset with the first transmitted pulse. An interrupt ISR0.XLSC is set with the rising edge of this bit. If XPM2.XLT is set, this bit is frozen.

Receive Equalizer Status (Read)

Addresses: 16_H, 36_H, 56_H, 76_H

	7							0
RES	EV1	EV0		RES4	RES3	RES2	RES1	RES0

EV(1:0) **Equalizer Status Valid**

These bits inform the user about the current state of the receive equalization network. Only valid if LIM1.EQON is set.

00 = Equalizer status not valid, still adapting

01 = Equalizer status valid

10 = Equalizer status not valid

11 = Equalizer status valid but high noise floor

RES(4:0) **Receive Equalizer Status**

These bits display current line attenuation status in steps of approximately 1.4 (T1/J1)/1.7 (E1) dB. Only valid if bits EV(1:0) = 01. Accuracy: ± 2 digits, based on temperature influence and noise amplitude variations.

00000 = Minimum gain (0 dB)

...

11001 = Maximum equalizer gain

Note: For maximum receiver sensitivity set bits LIM2.RIL(2:0) = 110

Interrupt Status Register 0 (Read)

Addresses: 17_H, 37_H, 57_H, 77_H

Value after reset: 00_H

	7							0
ISR0	LLBSC	XLSC	PRBSSC	SLN	SLP	PDENI	AIS	LOS

All bits are reset when ISR0 is read.

If bit LIM4.VIS is set, interrupt statuses in ISR0 may be flagged although they are masked via register IMR0. However, these masked interrupt statuses neither generate a signal on INT, nor are they visible in register CIS.

LLBSC **Line Loop Back Status Change**

Depending on bit LIM0.ARL the interrupt source is changed.

LIM0.ARL = 0 : This bit is set if the LLB activate signal or the LLB deactivate signal is detected over a period of 25 ms/33.16 ms (E1/T1) with a bit error rate less than 10^{-2}.

The LLBSC bit is also set if the current detection status is left, i.e., if the bit error rate exceeds 10^{-2}.

LIM0.ARL = 1 : This bit is set high with any change of state of bit LSR0.RLS.

XLSC **Transmit Line Status Change**

XLSC is set with the rising edge of the bit LSR1.XLO or with any change of bit LSR1.XLS.

The actual status of the transmit line monitor can be read from LSR1.XLS and LSR1.XLO.

PRBSSC **PRBS Status Change**

This bit is set with any change of state of the PRBS synchronizer. The current status of the PRBS synchronizer is indicated in LSR0.PRBSS.

SLN **Slip Negative**

The frequency of the receive route clock is greater than the frequency of the receive framer interface working clock based on 2.048 MHz (E1)/1.544 MHz (T1/J1). Data is skipped. SLN is also set during alarm simulation.

SLP **Slip Positive**

The frequency of the receive route clock is less than the frequency of the receive framer interface working clock, which is a multiple of or equal to 2.048 MHz (E1)/1.544 MHz (T1/J1). Data is repeated. SLP is also set during alarm simulation.

PDENI **Pulse-Density Violation Interrupt**

This bit is set if a pulse-density violation is detected(LSR0.PDEN = 1). The bit is set during alarm simulation.

AIS **Alarm Indication Signal (Blue Alarm)**

This bit is set when an alarm indication signal is detected and bit LSR0.AIS is set. It is also set during alarm simulation.
If LIM4.SCI is set, this interrupt status bit is set with every change of LSR0.AIS.

LOS **Loss-of-Signal (Red Alarm)**

This bit is set when a loss-of-signal alarm is detected in the received bit stream and LSR0.LOS is set. It is also set during alarm simulation.
If LIM4.SCI is set, this interrupt status bit is set with every change of LSR0.LOS.

Interrupt Status Register 1 (Read)

Addresses: 18_H, 38_H, 58_H, 78_H

	7							0
ISR1							LTC	SEC

All bits are reset when ISR1 is read.

If bit LIM4.VIS is set, interrupt statuses in ISR1 may be flagged although they are masked via register IMR1. However, these masked interrupt statuses neither generate a signal on INT, nor are they visible in register CIS.

LTC **Loss of Transmit Clock**

This bit is set when a loss of transmit clock is detected and bit LSR1.TCS is set. It is also set during alarm simulation.
If LIM4.SCI is set, this interrupt status bit is set with every change of LSR1.TCS.

SEC **One-Second Timer**

The internal one-second timer has expired. The timer is derived from clock RCLK, SCLKO, SCLKI or TCLK, depending on the monitor block configuration. The selected clock source has to supply a constant clock to ensure the correct function of the second timer.

Channel Interrupt Status Register (Read)

Address: 60_H

Value after reset: 00_H

	7							0
CIS					GIS4	GIS3	GIS2	GIS1

This status register points to pending interrupts sourced by ISR1 and ISR0 of each channel.

GIS4 Global interrupt status of register ISR1/0 of channel 4

GIS3 Global interrupt status of register ISR1/0 of channel 3

GIS2 Global interrupt status of register ISR1/0 of channel 2

GIS1 Global interrupt status of register ISR1/0 of channel 1

Code Violation Counter (Read)

Addresses CVCL: 19_H, 39_H, 59_H, 79_H

Addresses CVCH: $1A_H$, $3A_H$, $5A_H$, $7A_H$

	7						0
CVCL	CV7						CV0

	7						0
CVCH	CV15						CV8

CV(15:0) **Code Violations**

E1 mode:

If the HDB3 or the CMI code is selected, the 16-bit counter is incremented if violations of the HDB3 code are detected. The error detection mode is determined by programming the bit LIM0.EXZE.

If simple AMI coding is enabled (LIM0.RC(1:0) = 00), all bipolar violations are counted.

T1 mode:

If the B8ZS code (bit LIM0.RC(1:0) = 10, GCR2.PMODx = 1) is selected, the 16-bit counter is incremented upon detection of violations that are not due to zero substitution. If LIM0.EXZE is set, excessive zero strings (more than seven contiguous zeros) are detected and counted.

If simple AMI coding is enabled (LIM0.RC(1:0) = 00), all bipolar violations are counted. If LIM0.EXZE is set, excessive zero strings (more than 15 contiguous zeros) are detected and counted.

During alarm simulation, the counter is incremented every four bits received up to its saturation.

Clearing and updating the counter is done according to bit LIM1.ECM. If this bit is cleared, the error counter buffer is permanently updated. For correct read access of the error counter, bit CMDR.DCVC has to be set. With the rising edge of this bit, updating of the buffer is stopped and the error counter is cleared. Bit CMDR.DCVC is reset automatically with a read access to the error counter high byte.

If LIM1.ECM is set every second (interrupt ISR1.SEC), the error counter is latched and then reset automatically. The latched error counter state has to be read within the next second.

PRBS Bit Error Counter (Read)

Addresses CVCL: $1B_H$, $3B_H$, $5B_H$, $7B_H$

Addresses CVCH: $1C_H$, $3C_H$, $5C_H$, $7C_H$

	7							0
BECL	BEC7							BEC0

	7							0
BECH	BEC15							BEC8

BEC(15:0) **PRBS Bit Error Counter**

This 16-bit counter is incremented with every received PRBS bit error in the PRBS synchronous state LSR0.PRBSS = 1.

Clearing and updating of the counter is done according to bit LIM1.ECM. If this bit is cleared, the error counter buffer is permanently updated. For correct read access of the error counter bit CMDR.DBEC has to be set. With the rising edge of this bit, updating the buffer is stopped and the error counter is cleared. Bit CMDR.DBEC is reset automatically with a read access to the error counter high byte.

If LIM1.ECM is set every second (interrupt ISR1.SEC) the error counter is latched and then cleared automatically. The latched error counter state has to be read within the next second.

Version Status Register (Read)

Address: $7F_H$

	7							0
VSTR	VN7	VN6	VN5	VN4	VN3	VN2	VN1	VN0

VN(7:0) **Version Number of the Chip**

00_H =Version 1.1

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 17 Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	– 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 150	°C
IC supply voltage (digital)	V_{DD}	– 0.4 to 6.5	V
IC supply voltage receive (analog)	V_{DDR}	– 0.4 to 6.5	V
IC supply voltage transmit (analog)	V_{DDX}	– 0.4 to 6.5	V
Voltage on any pin with respect to ground	V_S	– 0.4 to 6.5	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	2000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

Note: Stresses greater than those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may reduce device reliability.

7.2 Operating Range

Table 18 Power Supply Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	-40	85	°C	
Supply voltages	V_{DD} V_{DDR} V_{DDX}	3.13	3.46	V	1)
Digital input voltages	V_{ID}	0	5.25	V	
Ground	V_{SS} V_{SSR} V_{SSX}	0	0	V	

1) Voltage ripple on analog supply less than 50 mV

Note: In the operating range, the functions given in the circuit description are fulfilled. V_{DD}, V_{DDR} and V_{DDX} have to be connected to the same voltage level, V_{SS}, V_{SSR} and V_{SSX} have to be connected to ground level.

7.3 DC Characteristics

Table 19 DC Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{ILSW}	– 0.4	0.8	V	1)
Input high voltage	V_{IHSW}	2.0	5.25	V	1)
Output low voltage	V_{OL}		0.45	V	I_{OL} = + 2 mA 1)
Output high voltage	V_{OH}	2.4		V	I_{OH} = - 2 mA 1)
Average power supply current (Analog line interface)	I_{DDE1}		165	mA	E1 application2)
	I_{DDT1}		200	mA	T1/J1 application3)
Average power supply current (Digital line interface)	I_{DD}		35	mA	
Input leakage current	I_{IL11}		1	µA	$V_{IN} = V_{DD}$ 4)
Input leakage current	I_{IL12}		1	µA	$V_{IN} = V_{SS}$ 4
Input leakage current	I_{IL21}		2.5	µA	$V_{IN} = V_{DD}$; only XL1, XL2
Input leakage current	I_{IL22}		2.5	µA	$V_{IN} = V_{SS}$; only XL1, XL2
Input pullup current	I_{IPU}	2	25	µA	$V_{IN} = V_{SS}$; V_{DD} = 5.0V (typ.: 12 µA)
		2	25	µA	$V_{IN} = V_{SS}$; V_{DD} = 3.3V (typ.: 12 µA)
Output leakage current	I_{OZ}		1	µA	V_{OUT} = *tristate*1) $V_{SS} < V_{meas} < V_{DD}$ measures against V_{DD} and V_{SS}
Transmitter output impedance	R_X		3	Ω	applies to XL1and XL2 5)
Transmitter output current	I_X		105	mA	XL1, XL2
Transmitter output voltage	V_X		2.5	V	V_{DD} = 3.3V 6)

Table 19 DC Parameters (cont'd)

Parameter (cont'd)	**Symbol**	**Limit Values**		**Unit**	**Notes**
		min.	**max.**		
Differential peak voltage of a mark (between XL1 and XL2)	V_{DX}		2.15	V	XL1, XL2 V_{DD} = 3.3V
Receiver differential peak voltage of a mark (between RL1 and RL2)	V_R		V_{DDR} + 0.3	V	RL1, RL2
Receiver input impedance	Z_R	50 (typical value)		kΩ	5)
Receiver sensitivity	S_{RSH}	0	-10	dB	RL1, RL2 LIM0.EQON = 0 (short-haul)
Receiver sensitivity	S_{RLH}	0	-36	dB	RL1, RL2 LIM0.EQON = 1 (T1/J1, long-haul)
			-36		RL1, RL2 LIM0.EQON = 1 (E1, long-haul)
Receiver input threshold	V_{RTH}	45 50 55 67 (typical value)		%	LIM2.SLT(1:0) = 11 = 10 = 00 = 01 5)

Table 19 DC Parameters (cont'd)

Parameter (cont'd)	**Symbol**	**Limit Values**		**Unit**	**Notes**
		min.	**max.**		
Loss-**O**f-**S**ignal (LOS) detection limit in short-haul mode	V_{LOSSH}	0.90 0.70 0.60 0.40 0.30 0.20 0.15 0.10 (typical values)		V	RIL(2:0) = 000 RIL(2:0) = 001 RIL(2:0) = 010 RIL(2:0) = 011 RIL(2:0) = 100 RIL(2:0) = 101 RIL(2:0) = 110 RIL(2:0) = 111 5) 7)
LOS detection limit in long-haul mode	V_{LOSLH}	1.70 0.85 0.85 0.45 0.45 0.20 0.10 not defined (typical values)		V	RIL(2:0) = 000 RIL(2:0) = 001 RIL(2:0) = 010 RIL(2:0) = 011 RIL(2:0) = 100 RIL(2:0) = 101 RIL(2:0) = 110 RIL(2:0) = 111 5) 7)

1) Applies to all pins except analog pins RLx, TLx

2) Wiring conditions and external circuit configuration according to **Figure 13** on **page 45** for E1 mode 120 Ω; PRBS signal; four channels active; values of registers XPM(2:0) = 00_H, 03_H, $7B_H$

3) Wiring conditions and external circuit configuration according to **Figure 13** on **page 45** for T1 mode; PRBS signal; four channels active; values of registers XPM(2:0) = 11_H, $1E_H$, $D7_H$

4) Applies to all pins except RCLK, SCLKR, RL1, RL2, XL1, XL2

5) Parameter not tested in production

6) Depending on external configuration

7) Differential input voltage between pins RL1 and RL2; depends on programming of register LIM2.RIL(2:0)

Note: Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and 3.3V supply voltage.

7.4 AC Characteristics

7.4.1 Master Clock Timing

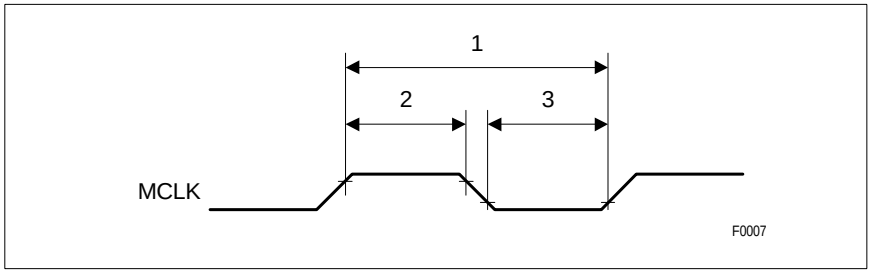


Figure 20 MCLK Timing

Table 20 MCLK Timing Parameter Values

No.	Parameter	Limit Values			Unit	Condition
		min.	typ.	max.		
1	Clock period of MCLK		488		ns	E1, fixed mode
			648		ns	T1/J1, fixed mode
		50		980.4	ns	flexible mode
2	High phase of MCLK	40			%	
3	Low phase of MCLK	40			%	
	Clock accuracy	32		28	ppm	1) 2)

1) to reach an internal clock accuracy of 32 ppm

2) depends on master clock frequency selection / rounding of clock divider setting

7.4.2 JTAG Boundary Scan Interface

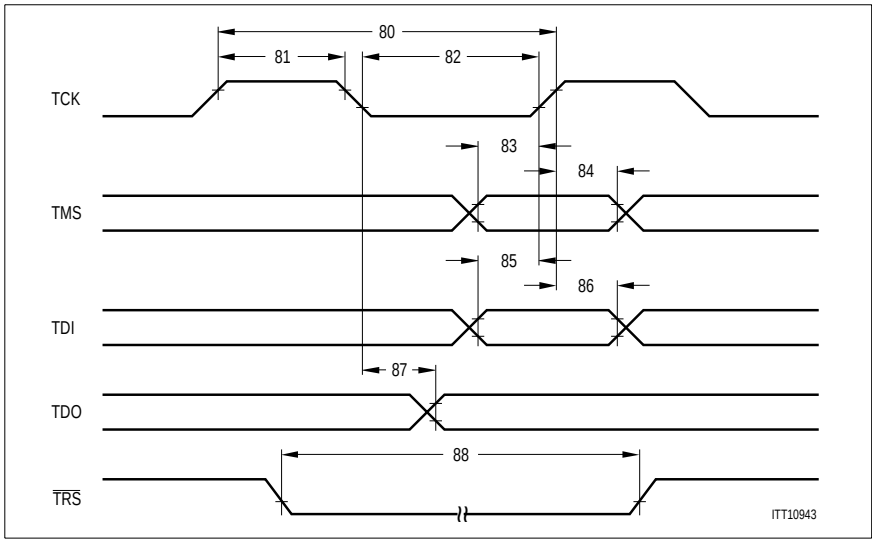


Figure 21 JTAG Boundary Scan Timing

Table 21 JTAG Boundary Scan Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
80	TCK period	250		ns
81	TCK high time	80		ns
82	TCK low time	80		ns
83	TMS setup time	40		ns
84	TMS hold time	40		ns
85	TDI setup time	40		ns
86	TDI hold time	40		ns
87	TDO valid delay		100	ns
88	$\overline{\text{TRS}}$ active low	200		ns

Identification Register : 32 bit; Version: $1_{H;}$ Part Number: 59_{H}, Manufacturer: 083_{H}

7.4.3 Reset

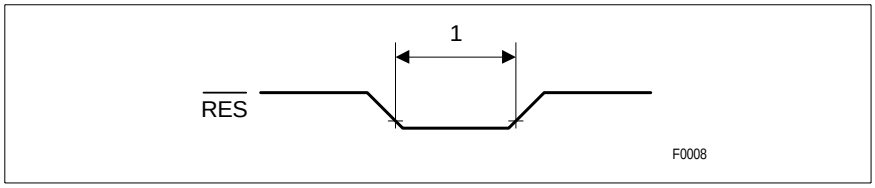


Figure 22 Reset Timing

Table 22 Reset Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
1	$\overline{RES}$ pulse width low	10[1)]		µs

1) while MCLK is running

7.4.4 Microprocessor Interface

7.4.4.1 Intel Bus Interface Mode

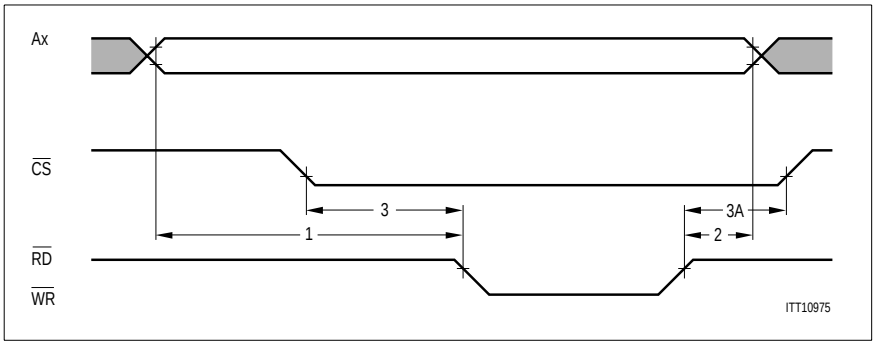


Figure 23 Intel Non-Multiplexed Address Timing

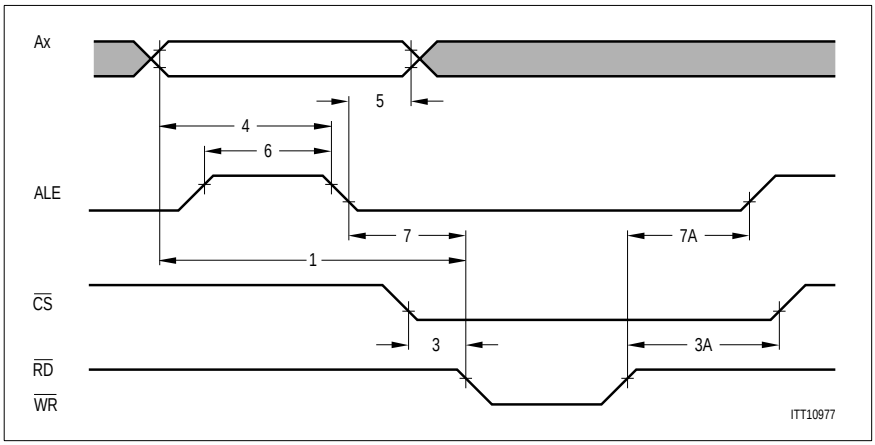


Figure 24 Intel Multiplexed Address Timing

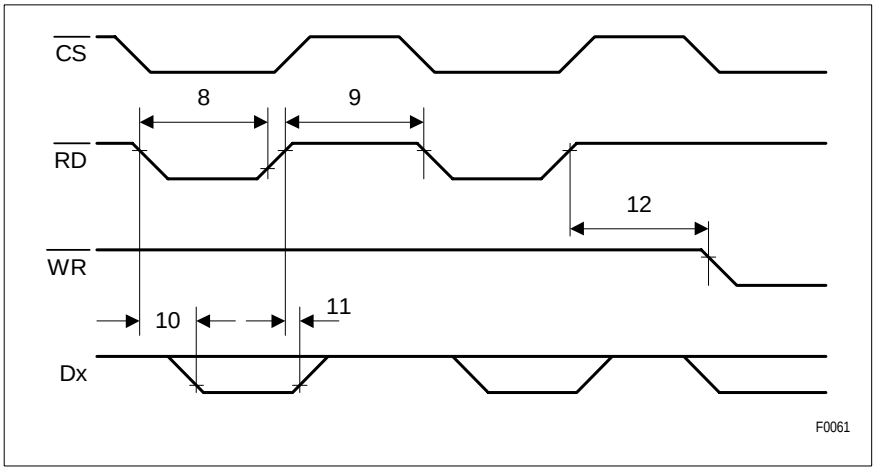


Figure 25 Intel Read Cycle Timing

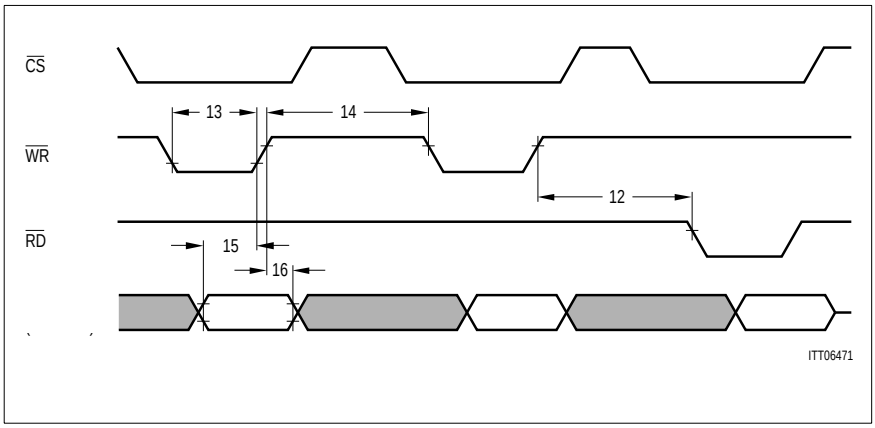


Figure 26 Intel Write Cycle Timing

Table 23 Intel Bus Interface Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
1	Address[1] setup time	15		ns
2	Address hold time	0		ns
3	$\overline{CS}$ setup time	0		ns
3A	$\overline{CS}$ hold time	0		ns
4	Address stable before ALE inactive	20		ns
5	Address hold after ALE inactive	10		ns
6	ALE pulse width	30		ns
7	Address latch setup time before cmd active	0		ns
7A	ALE to command inactive delay	30		ns
8	$\overline{RD}$ pulse width	80		ns
9	$\overline{RD}$ control interval	70		ns
10	Data[2] valid after $\overline{RD}$ active		75	ns
11	Data hold after $\overline{RD}$ inactive	10		ns
12	$\overline{WR}$ to $\overline{RD}$ or $\overline{RD}$ to $\overline{WR}$ control interval	70		ns
13	$\overline{WR}$ pulse width	80		ns
14	$\overline{WR}$ control interval	70		ns

Table 23 Intel Bus Interface Timing Parameter Values (cont'd)

No.	Parameter	Limit Values		Unit
		min.	max.	
15	Data stable before $\overline{WR}$ inactive	30		ns
16	Data hold after $\overline{WR}$ inactive	10		ns

1) Ax refers to address lines A(6:0)

2) Dx refers to data line D(7:0)

7.4.4.2 Motorola Bus Interface Mode

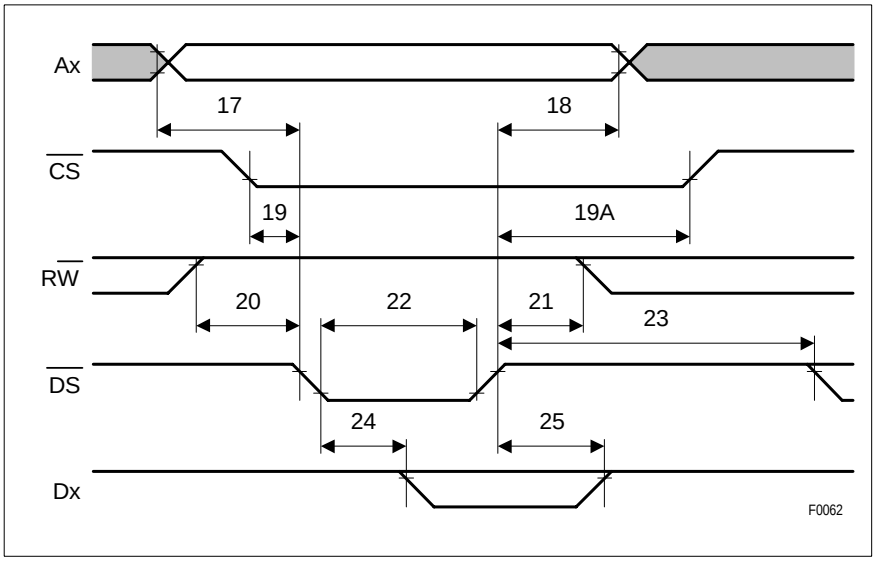


Figure 27 Motorola Read Cycle Timing

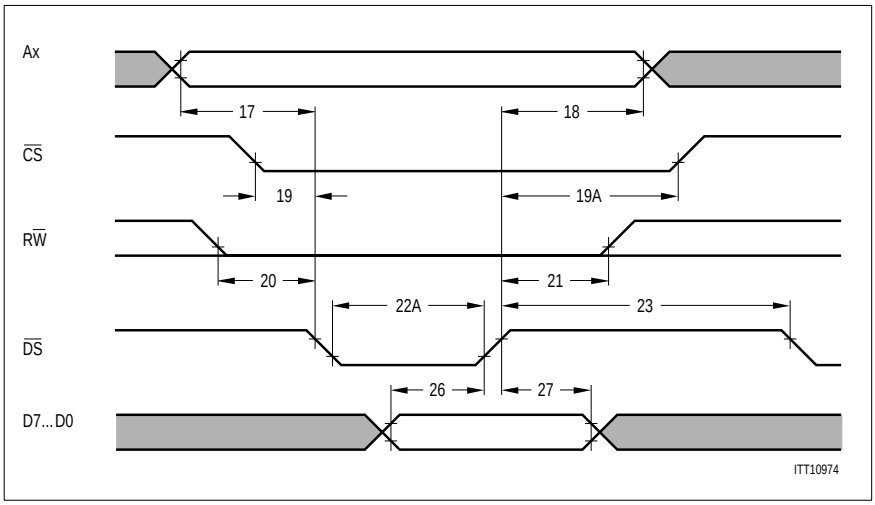


Figure 28 Motorola Write Cycle Timing

Table 24 Motorola Bus Interface Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
17	Address setup time before $\overline{DS}$ active	15		ns
18	Address hold after $\overline{DS}$ inactive	0		ns
19	$\overline{CS}$ active before $\overline{DS}$ active	0		ns
19A	$\overline{CS}$ hold after $\overline{DS}$ inactive	0		ns
20	R$\overline{W}$ stable before $\overline{DS}$ active	10		ns
21	R$\overline{W}$ hold after $\overline{DS}$ inactive	0		ns
22	$\overline{DS}$ pulse width (read access)	80		ns
22A	$\overline{DS}$ pulse width (write access)	70		ns
23	$\overline{DS}$ control interval	70		ns
24	Data valid after $\overline{DS}$ active (read access)		75	ns
25	Data hold after $\overline{DS}$ inactive (read access)	10		ns
26	Data stable before $\overline{DS}$ active (write access)	30		ns
27	Data hold after $\overline{DS}$ inactive (write access)	10		ns

7.4.5 Framer Interface

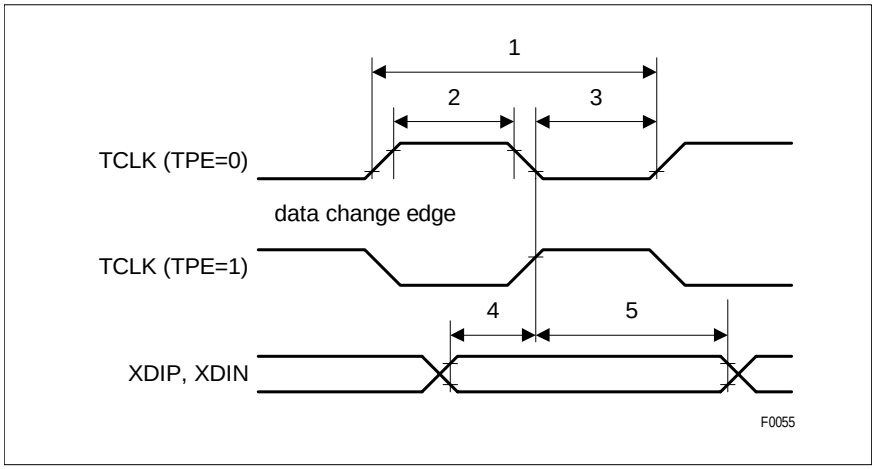


Figure 29 TCLK Input Timing

Table 25 TCLK Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	TCLK period E1 (2.048 MHz)		488		ns
	TCLK period T1/J1 (1.544 MHz)		648		ns
2	TCLK high	40			%
3	TCLK low	40			%
4	XDIP, XDIN setup time	20			ns
5	XDIP, XDIN hold time	20			ns

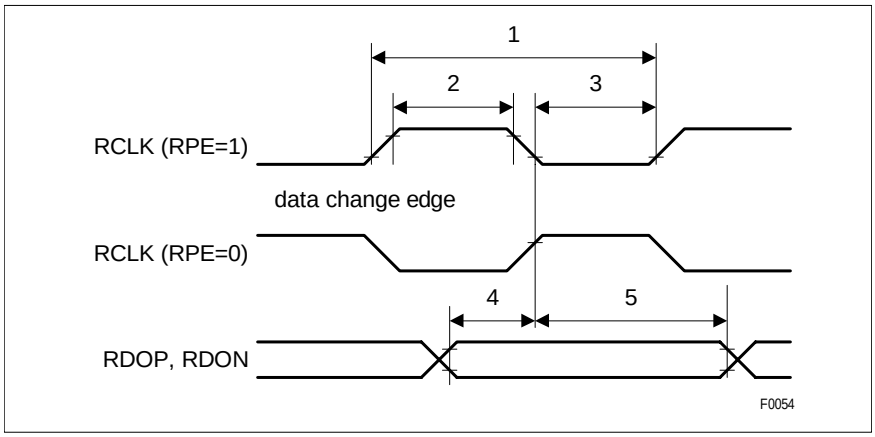


Figure 30 RCLK Output Timing

Table 26 RCLK Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	RCLK period E1 (2.048 MHz)		488		ns
	RCLK period T1/J1 (1.544 MHz)		648		ns
2	RCLK high	40			%
3	RCLK low	40			%
4	RDOP, RDON setup time	-10			ns
5	RDOP, RDON hold time	200			ns

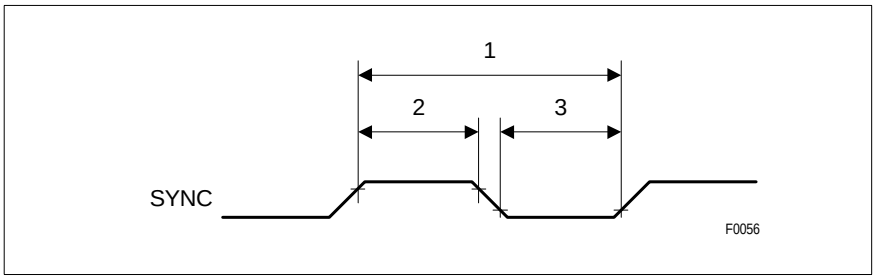


Figure 31 SYNC Timing

Table 27 SYNC Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	SYNC period (SYNC = 2.048 MHz)		488		µs
	SYNC period (SYNC = 1.544 MHz)		648		µs
	SYNC period (SYNC = 8 kHz)		125		ms
2	SYNC low time	20			%
2	SYNC low time	20			%

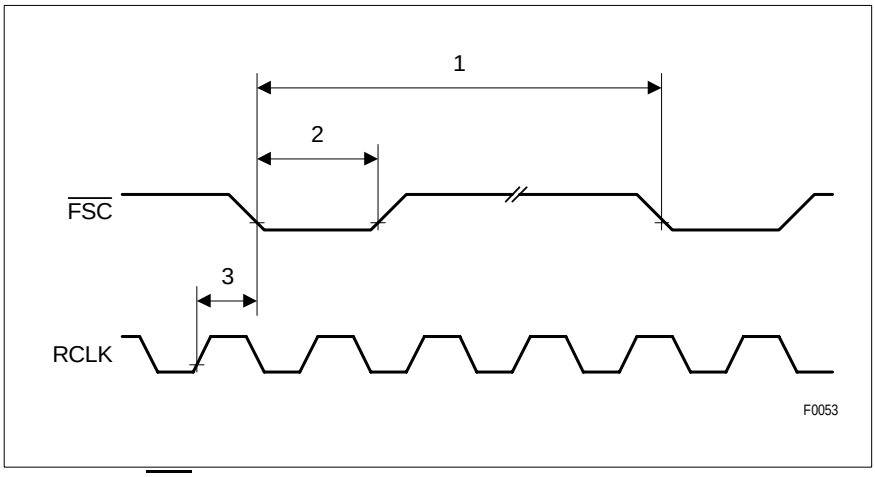


Figure 32 $\overline{\text{FSC}}$ Timing

Table 28 $\overline{\text{FSC}}$ Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	$\overline{\text{FSC}}$ period		125		µs
2	$\overline{\text{FSC}}$ low time E1		488		ns
	$\overline{\text{FSC}}$ low time T1/J1		648		ns
3	RCLK to $\overline{\text{FSC}}$ delay E1			370	ns
	RCLK to $\overline{\text{FSC}}$ delay T1/J1			280	ns

7.4.6 Pulse Templates - Transmitter

7.4.6.1 Pulse Template E1

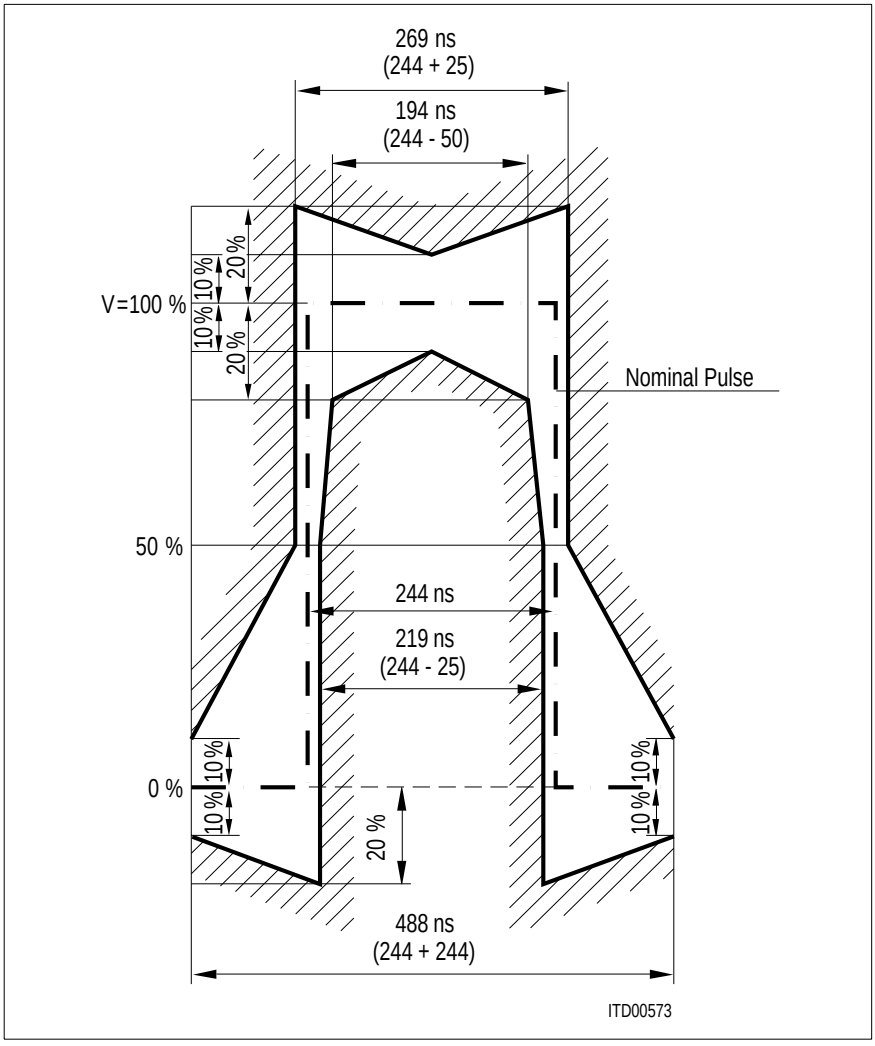


Figure 33 E1 Pulse Shape at Transmitter Output

7.4.6.2 Pulse Template T1

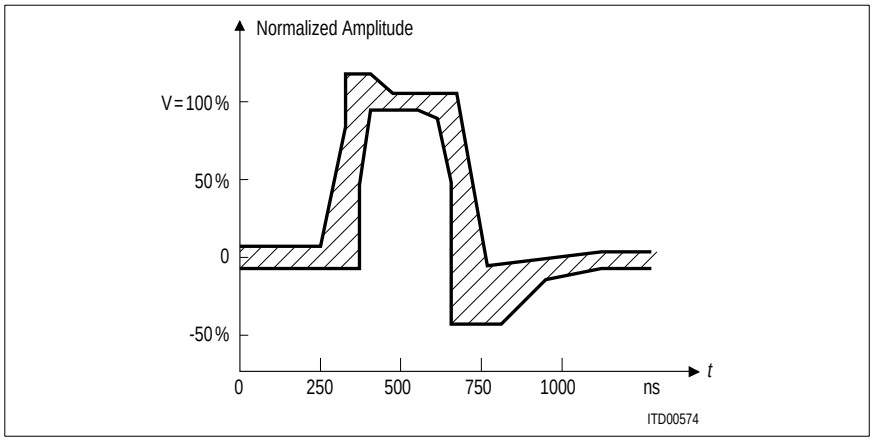


Figure 34 T1 Pulse Shape

Table 29 T1 Pulse Template (ANSI T1.102)

Maximum Curve		Minimum Curve	
Time [ns]	**Level [%][1)]**	**Time [ns]**	**Level [%]**
0	5	0	-5
250	5	350	-5
325	80	350	50
325	115	400	95
425	115	500	95
500	105	600	90
675	105	650	50
725	-7	650	-45
1100	5	800	-45
1250	5	925	-20
		1100	-5
		1250	-5

1) 100 % value must be in the range of 2.4 V and 3.6 V;
tested at 0 ft and 655 ft using PIC 22AWG cable characteristics.

7.5 Capacitances

Table 30 Pin Capacitances

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input capacitance[1)]	C_{IN}	5	10	pF	
Output capacitance[1)]	C_{OUT}	8	15	pF	all except XLx.y
Output capacitance[1)]	C_{OUT}	8	20	pF	XLx.y

1) not tested in production

7.6 Package Characteristics

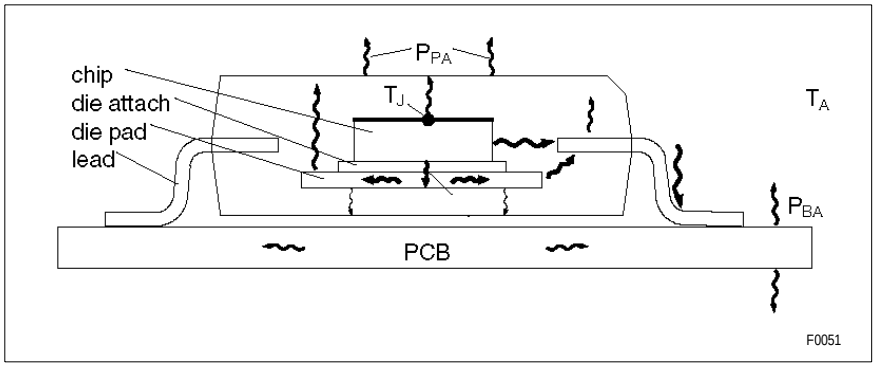


Figure 35 Thermal Behaviour of Package

Table 31 Package Characteristic Values

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Thermal resistance[1)]	R_{th}		44		K/W	single layer PCB, no convection
			36		K/W	air flow 200 LFPM
			32		K/W	air flow 500 LFPM
Junction temperature	R_j			125	°C	

1) $R_{th} = (T_{junction} - T_{ambient})/Power$
Not tested in production.

7.7 Test Configuration

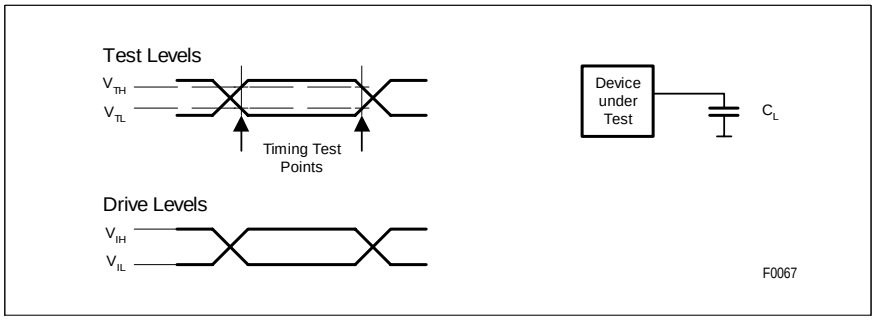


Figure 36 Input/Output Waveforms for AC Testing

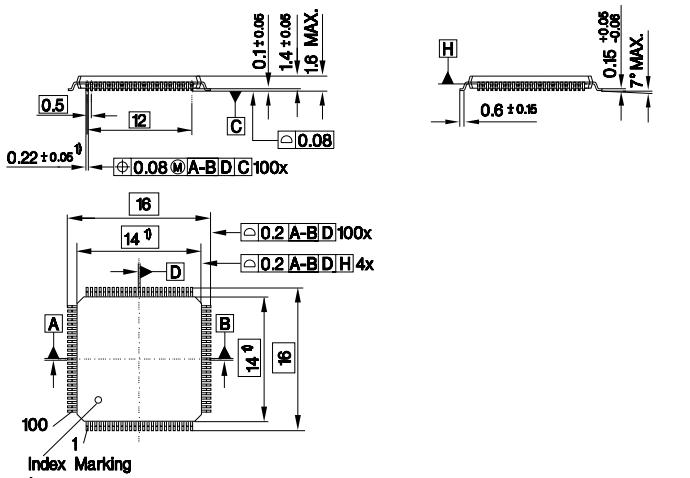
Table 32 AC Test Conditions

Parameter	Symbol	Test Values	Unit	Notes
Load capacitance	C_L	50	pF	
Input voltage high	V_{IH}	2.4	V	all except RLx.y
Input voltage low	V_{IL}	0.4	V	all except RLx.y
Test voltage high	V_{TH}	2.0	V	all except XLx.y
Test voltage low	V_{TL}	0.8	V	all except XLx.y

Typical characteristics are mean values expected over the production spread. If not specified otherwise, typical characteristics apply at T_A = 25 °C and V_{DD} = 3.3V.

8 Package Outlines

P-TQFP-100-3
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side at max. material condition

GPP09189

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

9 Appendix

9.1 Application Notes

Online access to supporting information is available on the internet page:

http://www.infineon.com/falc

On the same page you find as well the

- Boundary Scan File for QuadLIU™ Version 1.1 (BSDL File)

9.2 Software Support

The following tool package is provided together with the QuadLIU™ Evaluation System EASY22504:

- Flexible Master Clock Calculator
- External Line Front End Calculator
- IBIS Model for QuadLIU™ V1.1 (according to ANSI/EIA-656)

To make system design easier, two software tools are available. The first is the “Master Clock Frequency Calculator", which calculates the required register settings depending on the external master clock frequency (**Figure 37**). The second is the “External Line Front End Calculator” which provides an easy method to optimize the external components depending on the selected application type. Calculation results are traced and can be stored in a file or printed out for documentation (**Figure 38**).

The tools run under a Windows® environment. Screenshots of the programs are shown in the figures below.

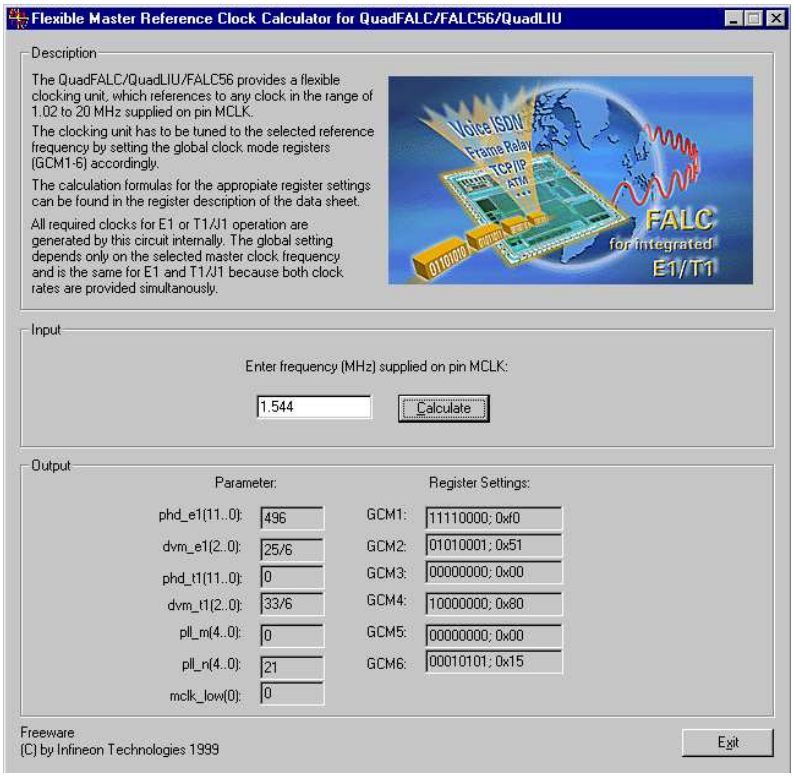


Figure 37 Master Clock Frequency Calculator

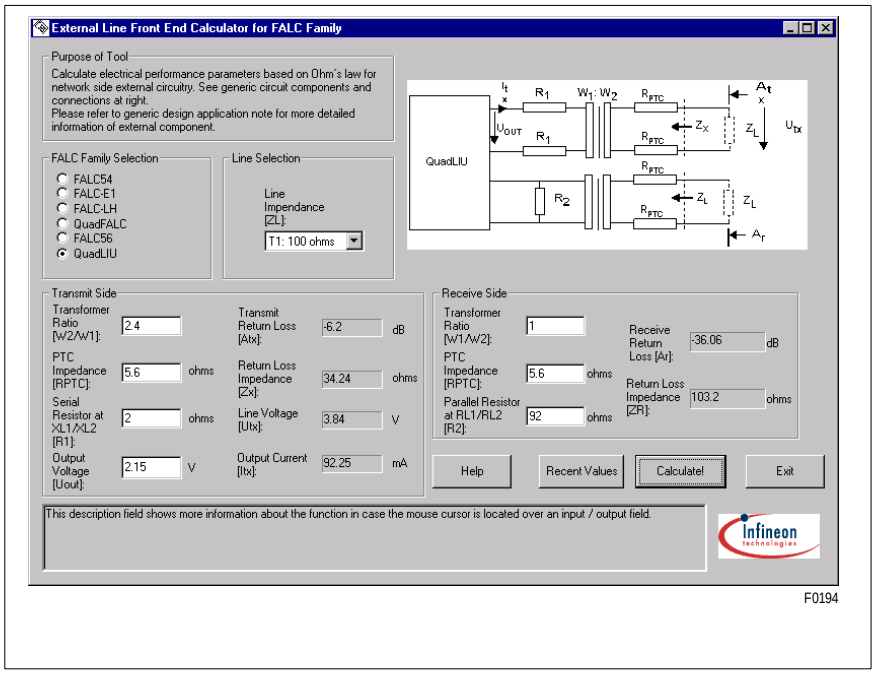


Figure 38 External Line Frontend Calculator

10 Glossary

A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AIS	Alarm Indication Signal (blue alarm)
AGC	Automatic Gain Control
ALOS	Analog Loss-Of-Signal
AMI	Alternate Mark Inversion
ANSI	American National Standards Institute
ATM	Asynchronous Transfer Mode
B8ZS	Line coding to avoid too long strings of consecutive ’0’
BER	Bit Error Rate
Bellcore	BELL COmmunications REsearch (see: Telcordia)
BPV	BiPolar Violation
CVC	Code Violation Counter
DCO	Digitally Controlled Oscillator
DL	Digital Loop
DPLL	Digitally controlled Phase-Locked Loop
DS1	Digital Signal level 1
ESD	ElectroStatic Discharge
EASY	EvAluation SYstem for FALC/LIU products
EQ	EQualizer
ETSI	European Telecommunication Standards Institute
FALC®	Framing And Line interface Component
FCC	US Federal Communication Commission
HBM	Human Body Model for ESD classification
HDB3	High-Density Bipolar of order 3
IBIS	I/O Buffer Information Specification (ANSI/EIA-656)
IBL	In Band Loop (=LLB)
ISDN	Intergrated sevices digital network
ITU	International Telecommunications Union
JATT	Jitter ATTenuator

JTAG	Joined Test Action Group
LBO	Line Build Out
LCV	Line Code Violation
LIU	Line Interface Unit
LL	Local Loop
LLB	Line Loop Back (= IBL)
LOS	Loss-Of-Signal (red alarm)
LSB	Least Significant Bit
MSB	Most Significant Bit
NRZ	Non Return to Zero signal
PDV	Pulse-Density Violation
PLL	Phase-Locked Loop
PRBS	Pseudo Ramdom Binary Sequence
P-TQFP	Plastic Thin metric Quad Flat Pack (device package)
RAI	Remote Alarm Indication (yellow alarm)
RL	Remote Loop
Sidactor	Overvoltage protection device for transmission lines
TAP	Test Access Port
Telcordia	New organization name, former ’Bellcore’
UI	Unit Interval

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Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

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