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S1R72805

IEEE1394 Link/Transaction USB1.1 Controller

■ DESCRIPTION

S1R72805 has the built-in Link/Transaction and USB1.1 Controller conforming to IEEE Std. 1394-1995, P1394a Draft 2.0 and enables to bridge either of both Interface and IDE. If a CPU/Flash ROM is provided to this IC and part of the transaction is made as Hardware and if the address and the sized of Page Table in SBP-2 are set to this IC, This IC will come to automatically following Page Table Fetch and transmit data. When this IC is assembled with a Cable PHY Transceiver/Arbiter conforming to the same standard, this IC will provide with an 1394/USB interface optimum to computer peripheral devices.
The IDE Interface is suitable to Ultra DMA mode5 (ATA100) and realizes high-speed transfer rates.

■ FEATURES

«Built-in CPU»

- 32bit RISC CPU S1C33. Operation at 25MHz (CPU cycle operation with minimum 2τ)
- Built-in SRAM : 8KB, No-wait operation
- Built-in Flash ROM : 64KB, No-wait operation
- Programmable timer : Built-in 3 channels

«IEEE1394 Interface»

- Link/Transaction Controller

  Link Layer

  Suitable to all two-way data transfer in the Asynchronous and Isochronous modes. The built-in SRAM enables to realize stable two-way data transfers up to the MaxPayload in 100Mbps, 200Mbps or 400Mbps. This enables the Hardware to automatically detect the Isochronous Resources Manager.

  Transaction Layer

  Part of the transaction function was made Hardware in order to prevent the actual transfer rate with overhead from being reduced. Communications with upper layers can be simplified by distinguishing the header area from the data area. In addition, the data area can be subdivided into a Stream area and an ORB area. A ring buffer is adopted for the receive header area and the receive data area (receive ORB area). Sizes of respective areas can be set optionally. The Hardware controls Busy states at the time of receive automatically.

- SBP-2 Support
  When the address and the size of Page Table are set to SBP-2, following Page Table Fetch and data can be transferred in the automatic mode.

- PHY/LINK Interface
  Conforming to P1394a. Suitable to the transfer rates of 100, 200, and 400Mbps. Suitable to Isolation (in case of built-in bus holder).
- Built-in SRAM for data packets : 8KB

«USB Interface»

- Suitable to transfer in the full speed mode (12Mbps).
- Suitable to control transfer at the Endpoint 0 and to bulk, interrupt and Iso transfers at three individual Endpoints. For these three Endpoints, the following can be set individually: the IN/OUT direction, four types (8-, 16-, 32- and 64-byte) of maximum packet lengths, optional Endpoint number and single or double buffer size (for isochronous transfer, however, only single is available).
- The built-in SRAM (2KB) can be divided into programmable ones according to user definition.

«IDE Interface»

- Suitable to PIO Modes 0, 1, 2, 3 and 4, to Multi Word DMA Modes 0, 1 and 2 and to Ultra-DMA Modes 0, 1, 2, 3, 4, and 5.

«Others»

- 48MHz is input by the crystal oscillation for the USB.
- The built-in Flash ROM (64KB) is suitable to ICP (In Circuit Programming).
- QFP-100pin (0.5mm pitch)
- Supply voltage 3.3V±0.3V
- Radiation-resistant design has not been provided for this specification.
- This IC is a lead-free package.

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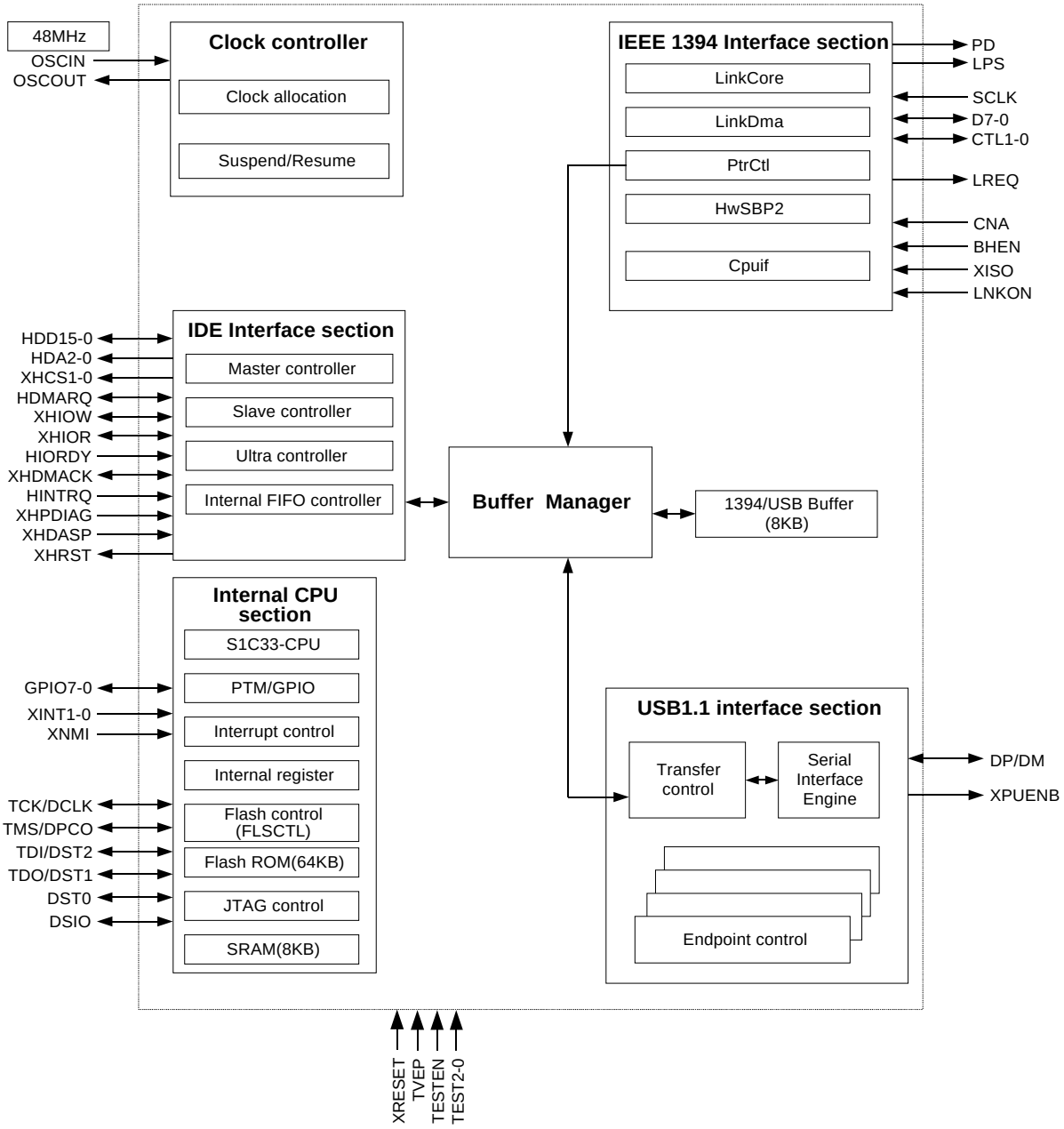
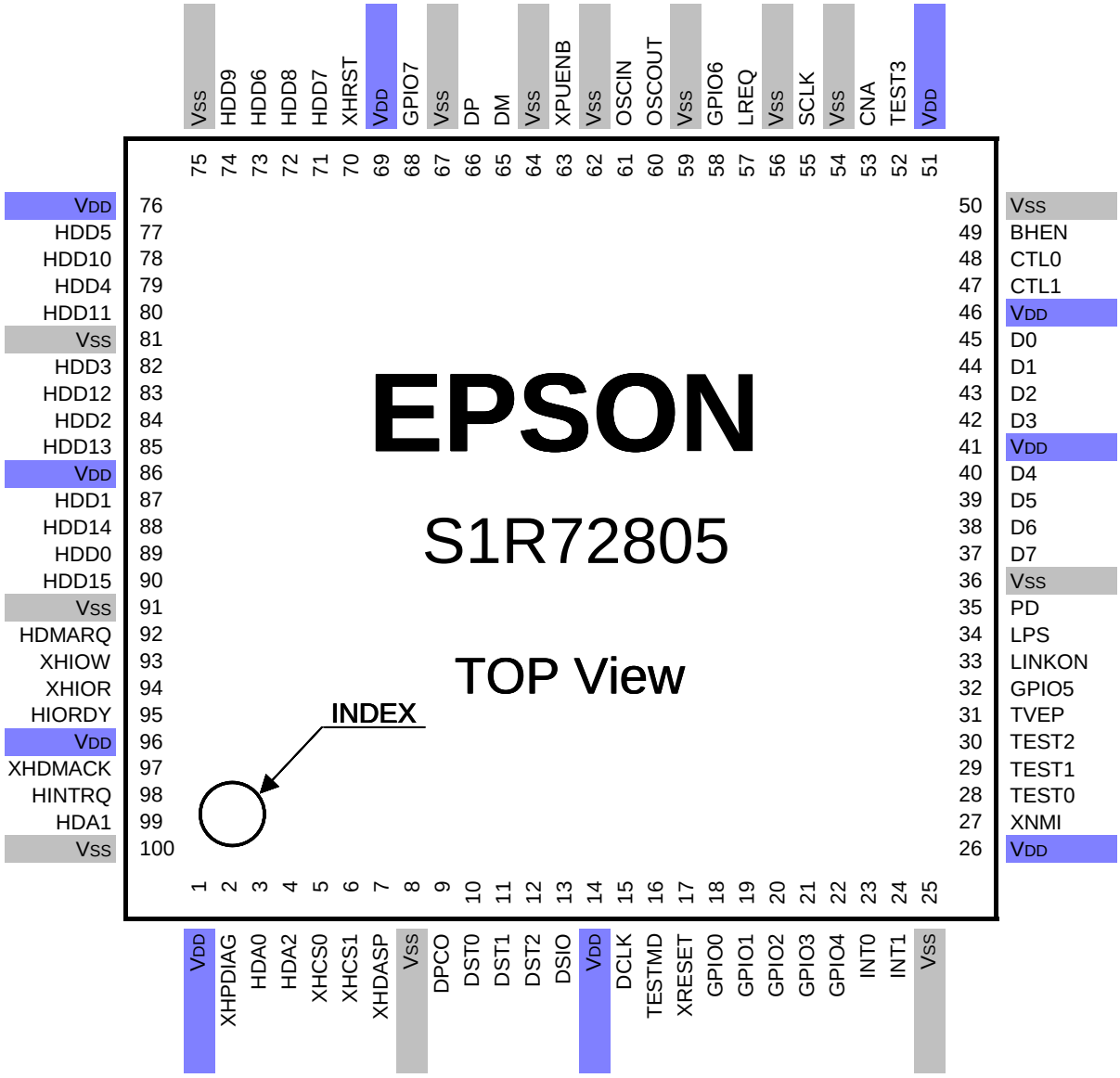
■ BLOCK DIAGRAM



■ PIN ASSIGNMENT

S1R72805 (QFP15-100pin)



■ PIN DESCRIPTION

Control signals with “X” prefixed to pin names are low active.

Pin No.	Signal	I/O	Reset	Functional description	Remarks
Relation to IEEE1394 PHY Interface (18)					
37	D7	Is/O	HI-Z	(MSB)	Drive capability 6mA Schmitt input (bus holder)
38	D6				
39	D5				
40	D4				
42	D3			Data bus with PHY	
43	D2				
44	D1				
45	D0			(LSB)	
47	CTL1	Is/O	HI-Z	Control signal with PHY	Drive capability 6mA Schmitt input (bus holder)
48	CTL0				
57	LREQ	O	LOW	Request signal to PHY	Drive capability 6mA
34	LPS	O	HIGH	Link power status signal to PHY	Drive capability 6mA
33	LINKON	Is	—	Link on signal from PHY	Schmitt input (bus holder)
49	BHEN	Is	—	Bus holder enable signal. At the time of DC connection, set this to the LOW level. At the time of single capacitor AC connection, set this to the HIGH level.	Schmitt input
53	CNA	Is	—	Cable Not Active	Schmitt input (bus holder)
35	PD	O	LOW	Power Down Enable	Drive capability 6mA
55	SCLK	Is	—	Clock signal (49.152MHz) from PHY	Schmitt input (bus holder)
Relation to USB1.1 Interface (5)					
65	DM	I/O	HI-Z	USB data port	Conformance to USB standard
66	DP			USB data port Arrange the configuration so as to pull up to 3.3V with an external resistance of 1.5kΩ. A register control is possible by using the pin “XPUENB.”	
63	XPUENB	Ood	HI-Z	The pull-up resistance control pin EnpullUp bit of the pin “DP” becomes LOW at the time of HIGH.	Drive capability 6mA
61	OSCIN	I	—	Crystal oscillation input pin	48.0MHz
60	OSCOUT	O	—	Clock output pin	48.0MHz
Relation to IDE Interface (29) All inputs are of 5V tolerance.					
90	HDD15	I/O	HI-Z	(MSB)	Drive capability 2mA
88	HDD14				
85	HDD13				
83	HDD12				
80	HDD11				
78	HDD10				
74	HDD9				
72	HDD8			IDE data bus	
71	HDD7				
73	HDD6				
77	HDD5				
79	HDD4				
82	HDD3				
84	HDD2				
87	HDD1				
89	HDD0			(LSB)	
92	HDMARQ	Is/O	HI-Z	IDE DMA Request Signal	Drive capability 6mA
93	XHIOW	Is/O	HI-Z	IDE Write Signal	Drive capability 2mA
94	XHIOR	Is/O	HI-Z	IDE Read Signal	Drive capability 2mA

Pin No.	Signal	I/O	Reset	Functional description	Remarks
95	HIORDY	Is	—	IDE IORDY Signal	—
97	XHDMACK	Is/O	HI-Z	IDE DMA Acknowledge Signal	Drive capability 2mA
98	HINTRQ	Is	—	IDE Interrupt signal	—
2	XHPDIAG	Is	—	IDE PDIAG Signal	—
7	XHDASP	Is	—	IDE DASP Signal	—
4	HDA2	Otr	HI-Z	(MSB) IDE Address Signal (LSB)	Drive capability 2mA
99	HDA1				
3	HDA0				
6	XHCS1	Otr	HI-Z	IDE Chip Select Signal	Drive capability 2mA
5	XHCS0	Otr	HI-Z	IDE Chip Select Signal	Drive capability 2mA
70	XHRST	Otr	HI-Z	IDE Reset Signal	Drive capability 2mA
CPU Macro (4)					
17	XRESET	Is	—	Initial Reset Signal (It must be pulled up externally.)	5V tolerance, Schmitt input
27	XNMI	Is	—	NMI Input signal (It must be pulled up externally.)	5V tolerance, Schmitt input
23	XINT0	Ipu	—	External Input Interrupt Signal	5V tolerance
24	XINT1	Ipu	—	External Input Interrupt Signal	5V tolerance
JTAG/ICD Interface (6)					
15	TCK/DCLK	Ipu/O	HI-Z	ICD Interface	Drive capability 6mA, 5V tolerance
9	TDI/DPCO	Ipu/O	HI-Z	ICD Interface	Drive capability 6mA, 5V tolerance
12	TDO/DST2	I/O	LOW	ICD Interface	Drive capability 6mA, 5V tolerance
11	DST1	I/O	HIGH	ICD Interface	Drive capability 6mA, 5V tolerance
10	DST0	I/O	HIGH	ICD Interface	Drive capability 6mA, 5V tolerance
13	TMS/DSIO	Ipu/O	HI-Z	ICD Interface	Drive capability 6mA, 5V tolerance
Others (4)					
18	GPIO0	Ipu/O	HI-Z	General-purpose I/O port	Drive capability 2mA, 5V tolerance
19	GPIO1				
20	GPIO2				
21	GPIO3				
22	GPIO4				
32	GPIO5				
58	GPIO6				
68	GPIO7				
Others (5)					
28	TEST0	I	—	Test Mode Set Pin (Connect this pin to GND usually.)	—
29	TEST1	I	—		—
30	TEST2	I	—		—
52	TEST3	I	—	Test Mode Set Pin (Connect this pin to V_{DD} usually.)	—
16	TESTMD	Ipd	—	I/O pin test control signal (Connect this pin to GND usually.)	—
31	TVEP	—	—	Internal Flash ROM Test Signal (Connect this pin to V_{DD} usually.)	—
V_{DD}:3.3V (10)					
1,14,26, 41,46,51, 69,76,86, 96	V_{DD}	—		Power supply	—
V_{SS}:0V (16)					
8,14,25, 36,50,54, 56,59,62, 64,67,75, 81,91,100	V_{SS}	—		GND	—

Note : I : Input
Is : Schmitt input
Ipu : Pull-up input
O : Output
Ood : Open drain output
Otr : Tristate output
Ispu : Pull-up Schmitt input
Ipd : Pull-down input

■ MEMORY MAP

● Total Memory Space

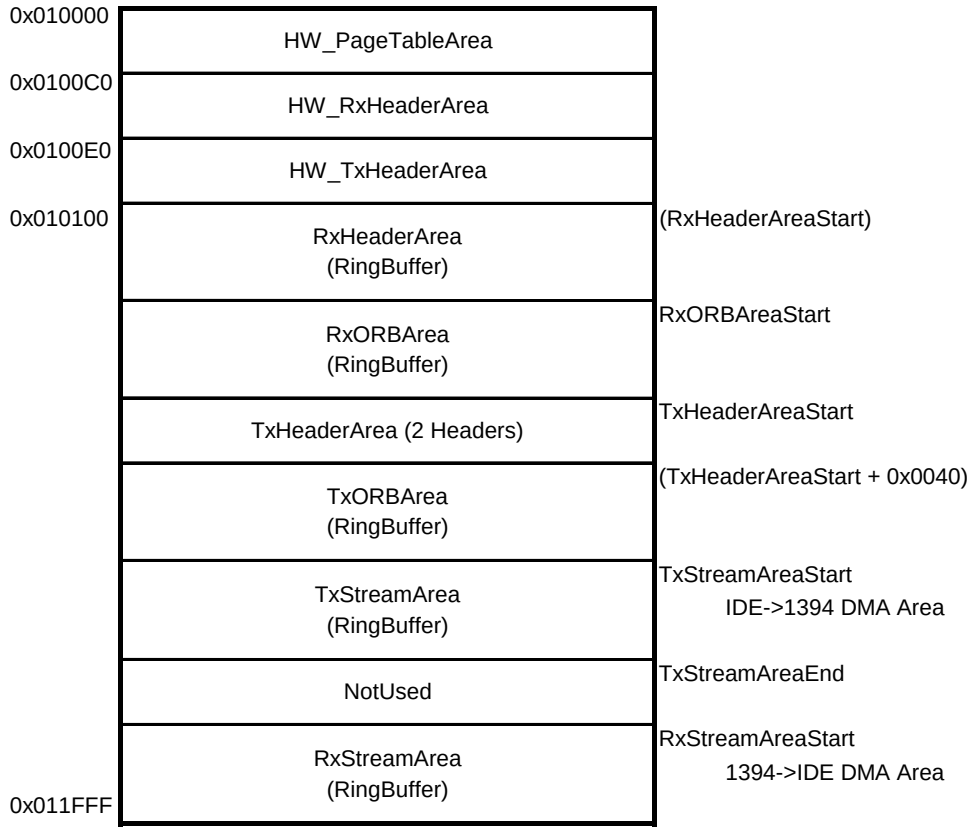
The memory map of this IC is shown in the figure blow. (For the built-in S1C33, 2-Clock is the minimum cycle.)

Address		Area	Device Size	Wait	Cycle
0xC0FFFF	Flash ROM	64KB	16bit	0Wait	2Clock
0xC00000					
	Reserved				
0x05FFFF	S1C33-Mini Core Reg		8/16bit	0Wait	2Clock
0x030000					
	Reserved				
0x011FFF	1394/USB Buffer	8KB	32bit	1Wait +Ext.Wait	4+nClock
0x010000					
0x002100	Reserved				
0x0020FF	Internal Reg	256B	8bit	0Wait +Ext.Wait Note 1	2+nClock
0x002000					
0x001FFF	IRAM (Work area)	8KB	32bit	0Wait	2Clock
0x000000					

Note 1 : At the time of 0x20070-0x2007F or USB-FIFO access by USB Window Register, Ext Wait is input. In other cases, Wait is 0.

● Memory Map of 1394/USB Buffer Area

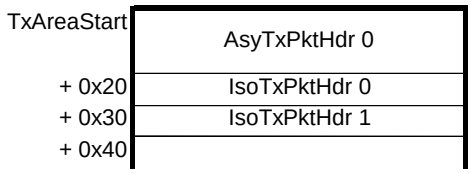
8KB



TxHeaderArea

① used Asyncronouse only

② used Isocronouse



- Direct Addressing makes it possible to access all the RAM area from the CPU.
- For RxStreamArea and TxStreamArea, Hardware DMA is possible to IDE Interface.
- HW_PageTableArea (for 24 pages), HW_RxHeaderArea and HW_TxHeaderArea respectively secure areas for a header as the Hardware areas. Firmware can independently use both the RxORB and TxORB areas.
- RxHeaderArea, RxORBArea, TxORB, TxStreamArea and RxStreamArea have become ring buffers and guarantee data among areas in the Hardware at the times of receiving 1394 and of executing IDE DMA. (The sizes of respective ring buffer areas can be changed if set by RxORBAreaStart, TxHeaderAreaStart, TxStreamAreaStart, TxStreamAreaEnd or RxStreamAreaStart in the internal register.)
- TxStreamArea and RxStreamArea can be overlapped and can be used as a single StreamArea.
- Post**Ptr and Used**Ptr of RxHeaderArea, RxORBArea, TxStreamArea or RxStreamArea monitor how each area is used. (Rx of 1394 monitors the both free capacities and controls busy_A, B and X in the Hardware.)
- When the above functions are controlled from the TRANS & SBP2 control block, PageTable Fetch in SBP-2 and data transfer can be operated by the Hardware.

When USB is used in this area, only 2KB (0x011800-0x011FFF) in the latter half is secured for USB-FIFO and other areas can be used for general purposes in the firm but compete with USB operation at the time of access.

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