EPSON

S1R72803F00A

IEEE1394 LINK/ Transaction Controller

Preliminary

- SBP-2 LINK Engine on chip
- High-speed transfer(Ultra ATA66)
- Built-in CPU and Flash

■ DESCRIPTION

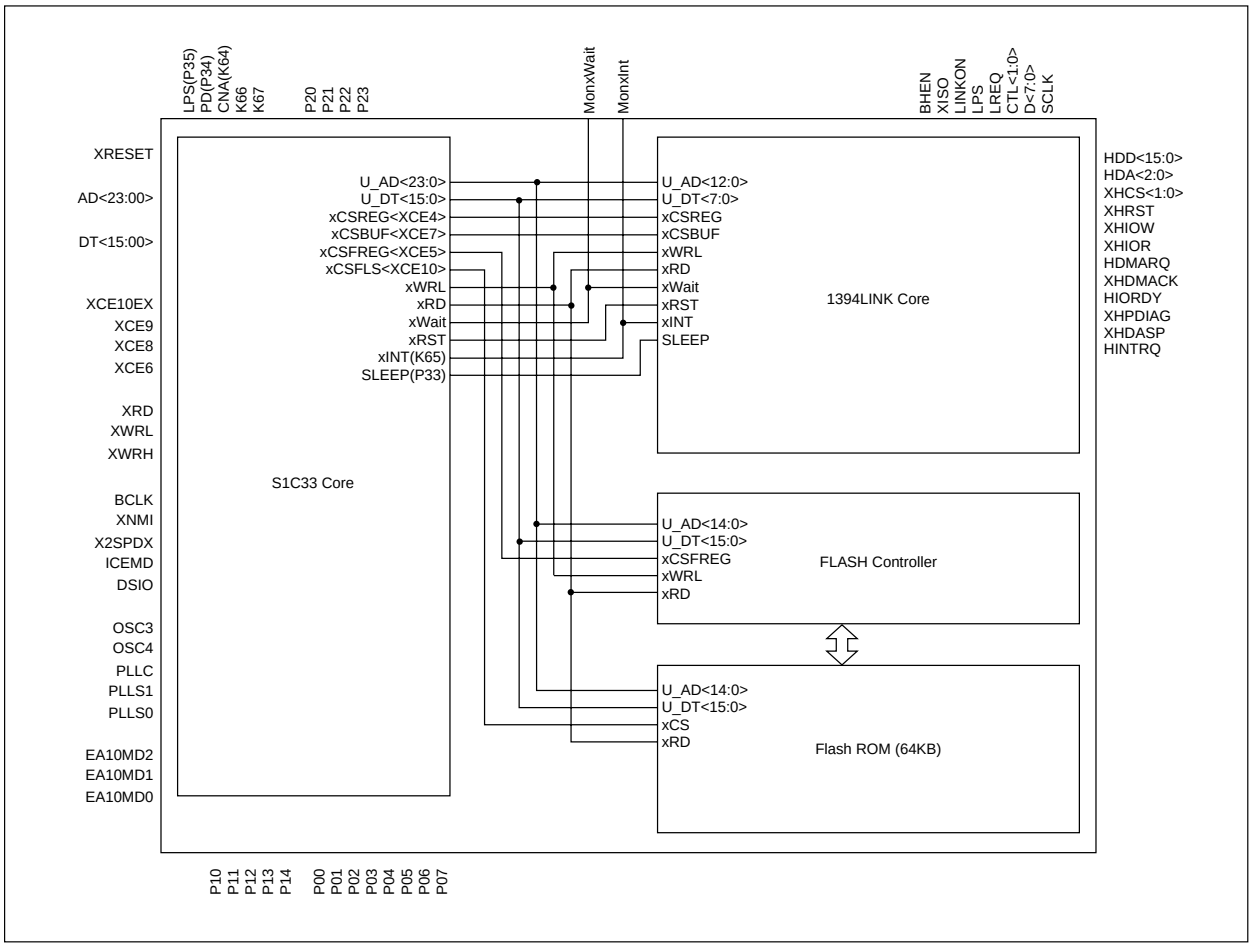
The S1R72803F00A is an IEEE Standard 1394-1995, P1394a Draft2.1 compliant LINK/Transaction Controller. Since some of the transaction functions of this controller have become hardware, the later PageTable fetch and data transmission can be executed automatically by setting the PageTable address and size in SBP-2.
In addition, thanks to a built-in MPU (SEIKO EPSON's original 32-bit RISC processor S1C33) called a Flash ROM which is necessary for the conversion system, the controller can provide peripheral devices with the optimum 1394 interfaces by simply adding a Cable PHY Transceiver/Arbiter that complies with the standard.

■ FEATURES

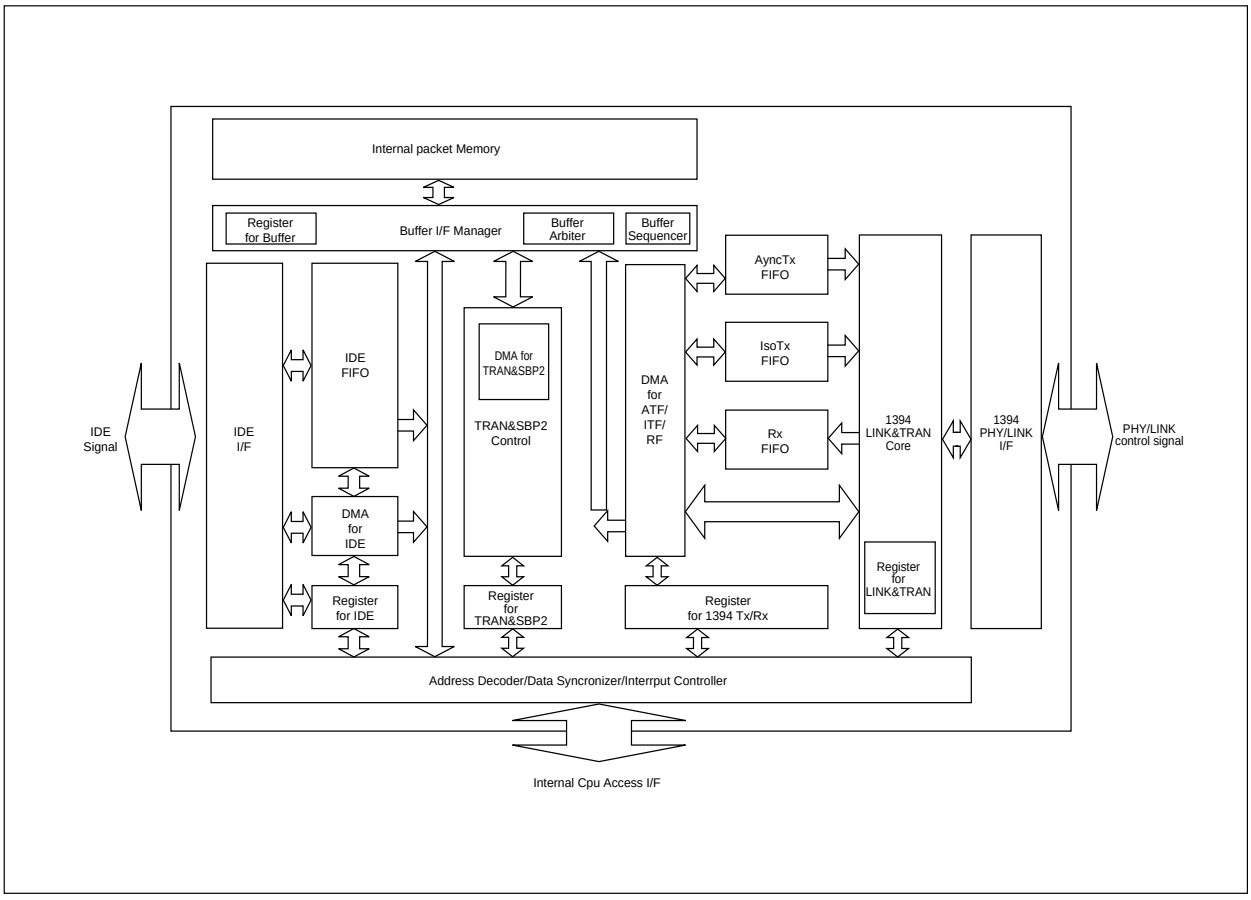
- LINK/Transaction Controller
  - All interactive data transmissions in both asynchronous and isochronous transfer modes are supported.
  - Stable interactive data transmissions of 100 Mbps, 200 Mbps and 400 Mbps of MaxPayload were made possible by the built-in SRAM.
  - The hardware can detect IsocronousResourceManager automatically.
  - Some of the transaction functions have become hardware to prevent the actual data transmission rate from declining due to overhead (to secure the dedicated partition).
  - Communication with the upper layers has been simplified by separating the header and data partitions.
  - The data partition has been subdivided into Stream and ORB partitions.
  - A ring buffer is employed for the recipient header, recipient data (recipient Stream and recipient ORB partitions) and sending data partitions.
  - The sizes of all partitions can be set freely.
  - The busy state during data reception is controlled by the hardware automatically.
- SBP-2 Support
  By setting the PageTable address and size in SBP-2, the later Page Table fetch and data transmission can be executed automatically.
- PHY/LINK Interface
  The P1394a is supported.
  Transmission rate 100/200/400 Mbps are supported.
  Isolation is supported (a bus holder is built in).
- CPU
  SEIKO EPSON's original 32-bit Microsoft Controller Unit is built in.
  Booting using both internal and external Flash ROMs is possible.
- IDE Interface
  PIO mode 0/1/2/3/4, Multiword DMA mode 0/1/2 and Ultra-DMA mode 0/1/2/3/4 are supported.
- I/O baffer with 5V tolerance
- Built-in SRAM
  For the data packet : 8-Kbyte
  For the MCU work : 8-Kbyte
- Built-in Flash ROM
  An 64-Kbyte Flash ROM is built-in.
- 3.3 V/ 5.0 V power supply
- 184-pin flat package (Pin pitch: 0.4 mm)

■ The package is not designed to be radiation-proof.

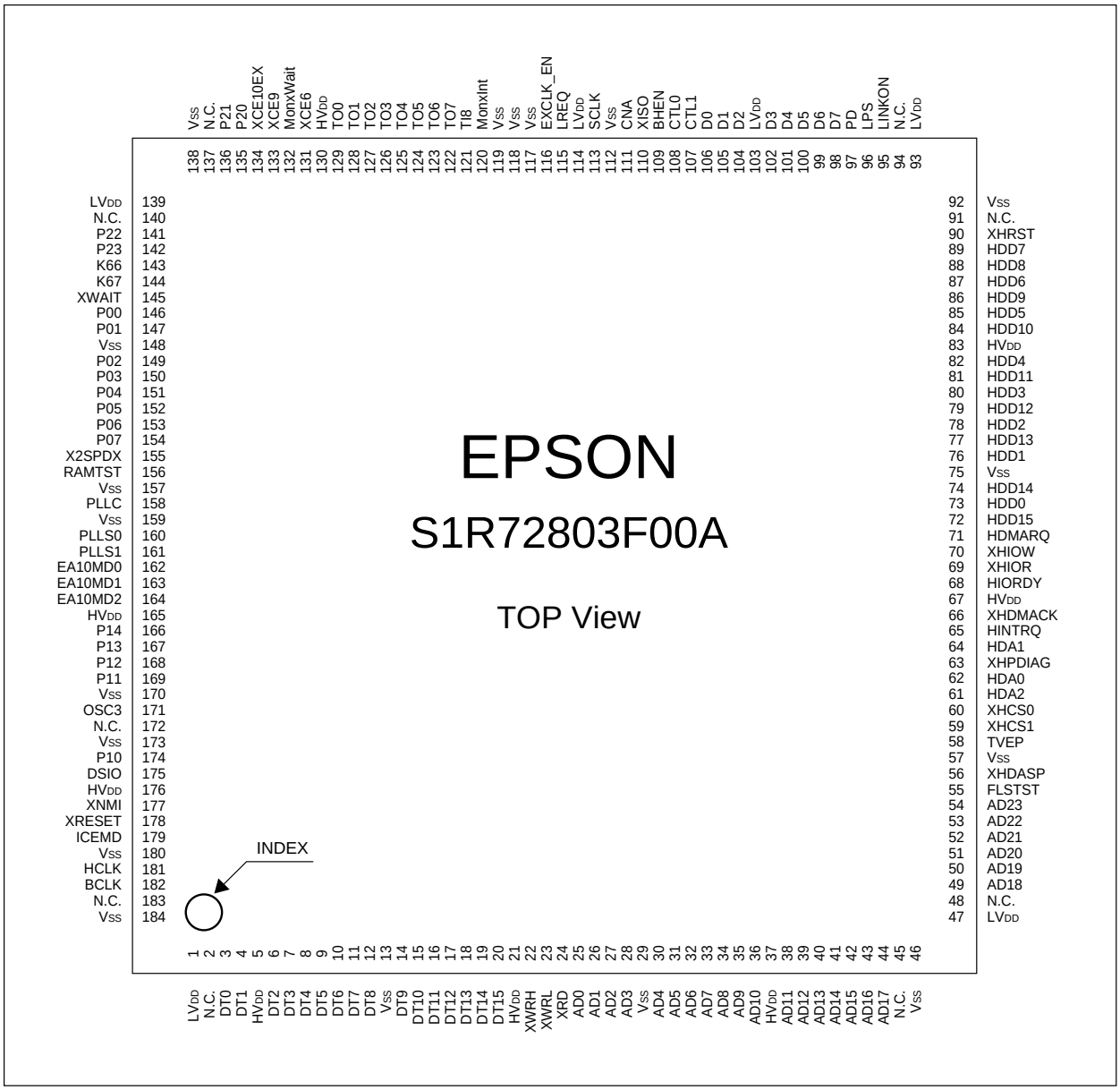
■ BLOCK DIAGRAM



■ LINK CORE BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ PIN DESCRIPTION

Pin Name	Pin No.	I/O	Reset	Functional Description	Remarks
1394PHY Interface (LV_{DD})					
D7	98	B	Hi-Z	(LSB)	
D6	99	B	Hi-Z		
D5	100	B	Hi-Z		Try state output
D4	101	B	Hi-Z	Data bus to PHY	Drive capacity: 12 mA
D3	102	B	Hi-Z		
D2	104	B	Hi-Z		Schmidt input (bus holder)
D1	105	B	Hi-Z		
D0	106	B	Hi-Z	(MSB)	
CTL1	107	B	Hi-Z	Control signal to PHY	Try state output Drive capacity: 12 mA
CTL0	108	B	Hi-Z		Schmidt input (bus holder)
LREQ	115	O	Lo	LINK request signal to PHY	Drive capacity: 12 mA
LPS	96	O	Lo	LINK power status singal to PHY	Drive capacity: 12 mA
LINKON	95	I	-	LINK ON signal from PHY	Schmidt input (bus holder)
XISO	110	I	-	Selects connection to PHY (LOW:Annex-J Isolation)	CMOS input
BHEN	109	I	-	Busholder enable signal (HIGH:Enable)	CMOS Schmidt input
CNA	111	I		Cabele Not Active	
PD	97	O		Power Down Enable	
SCLK	113	I	-	Clock signal from PHY (49.152 MHz)	Schmidt input (bus holder)

Pin Name	Pin No.	I/O	Reset	Functional Description	Remarks
IDE Interface (LV_{DD}, 5V tolerant)					
HDD15	72	B	Hi-Z	(LSB)	
HDD14	74	B	Hi-Z		
HDD13	77	B	Hi-Z		
HDD12	79	B	Hi-Z		
HDD11	81	B	Hi-Z		
HDD10	84	B	Hi-Z		
HDD9	86	B	Hi-Z		
HDD8	88	B	Hi-Z	IDE data bus	Drive capacity: 3 mA
HDD7	89	B	Hi-Z		
HDD6	87	B	Hi-Z		
HDD5	85	B	Hi-Z		
HDD4	82	B	Hi-Z		
HDD3	80	B	Hi-Z		
HDD2	78	B	Hi-Z		
HDD1	76	B	Hi-Z		
HDD0	73	B	Hi-Z	(MSB)	
HDMARQ	71	B	Hi-Z	IDE DMA request signal	Drive capacity: 6 mA
XHIOW	70	B	Hi-Z	IDE write signal	Drive capacity: 3 mA
XHIOR	69	B	Hi-Z	IDE read signal	Drive capacity: 3 mA
HIORDY	68	I	Hi-Z	IDE IORDY signal	
XHDMACK	66	B	Hi-Z	IDE DMA acknowledge signal	
HINTRQ	65	I	-	IDE interruption signal	
XHPDIAG	63	I	-	IDE PDIAG signal	
HDA2	61	Otr	Hi-Z	(LSB)	
HDA1	64	Otr	Hi-Z	IDE address signal	
HDA0	62	Otr	Hi-Z	(MSB)	
XHCS1	59	Otr	Hi-Z	IDE chip select signal	
XHCS0	60	Otr	Hi-Z	IDE chip select signal	
XHDASP	56	I	-	IDE DASP signal	Drive capacity: 3 mA
XHRST	90	Otr	Hi-Z	IDE reset signal	Drive capacity: 6 mA

Pin Name	Pin No.	I/O	Reset	Functional Description	Remarks
SIC33 External Interface (HV_{DD})					
AD23	54	O		(MSB)	
AD22	53	O			
AD21	52	O			
AD20	51	O			
AD19	50	O			
AD18	49	O			
AD17	44	O			
AD16	43	O			
AD15	42	O		CPU address bus	
AD14	41	O			
AD13	40	O			
AD12	39	O			
AD11	38	O			
AD10	36	O			
AD9	35	O			
AD8	34	O			
AD7	33	O			
AD6	32	O			
AD5	31	O			
AD4	30	O			
AD3	28	O			
AD2	27	O			
AD1	26	O			
AD0	25	O		(LSB)	
DT15	20	B		(MSB)	
DT14	19	B			
DT13	18	B			
DT12	17	B			
DT11	16	B			
DT10	15	B			
DT9	14	B			
DT8	12	B			Built-in pull up resistors
DT7	11	B			
DT6	10	B			
DT5	9	B		CPU data bus	
DT4	8	B			
DT3	7	B			
DT2	6	B			
DT1	4	B			
DT0	3	B		(LSB)	
P07	154	B		General input/output port 07	Built-in pull up resistors
P06	153	B		General input/output port 06	Built-in pull up resistors
P05	152	B		General input/output port 05	Built-in pull up resistors
P04	151	B		General input/output port 04	Built-in pull up resistors
SRDY(P03)	150	B		Serial interface ready signal input pin and general input/output port 03	Built-in pull up resistors
SCLK(P02)	149	B		Serial interface clock input pin and general input/output port 02	Built-in pull up resistors
SOUT(P01)	147	B		Serial interface data output pin and general input/output port 01	Built-in pull up resistors
SIN(P00)	164	B		Serial interface data input pin and general input/output port 00	Built-in pull up resistors
K67	144	I			Built-in pull up resistors
K66	143	I			Built-in pull up resistors
P23	142	B			Built-in pull up resistors
P22	141	B			Built-in pull up resistors
P21	136	B			Built-in pull up resistors
P20	135	B			Built-in pull up resistors
XCE10_EX	134	O		Area 10 chip enable for the external memory	
XCE9	133	O		Area 9 chip enable	

Pin Name	Pin No.	I/O	Reset	Functional Description	Remarks
SIC33 External Interface (HV_{DD})					
XCE6	131	O		Area 6 chip enable	
EA10M2	164	I		Area 10 boot mode selection 2	HIGH:Built-in flash boot mode LOW:External memory mode
EA10M1	163	I		Area 10 boot mode selection 1	HIGH is fixed
EA10M0	162	I		Area 10 boot mode selection 0	HIGH is fixed
XWAIT	145	I		Wait cycle input	
XRD	24	O		Read signal	
XWRH	22	O		Upper byte write signal	
XWRL	23	O		Lower byte write signal	
BCLK	182	O		Bus clock signal	
SIC33 External Interface (LV_{DD})					
P14	166	B		General input/output port 14 (for ICD)	
P13	167	B		General input/output port 13 (for ICD)	
P12	168	B		General input/output port 12 (for ICD)	
P11	169	B		General input/output port 11 (for ICD)	
P10	174	B		General input/output port 10 (for ICD)	
DSIO	175	B		Serial input/output pin for debugging : Used when communicating with ICD33	Built-in pull up resistors

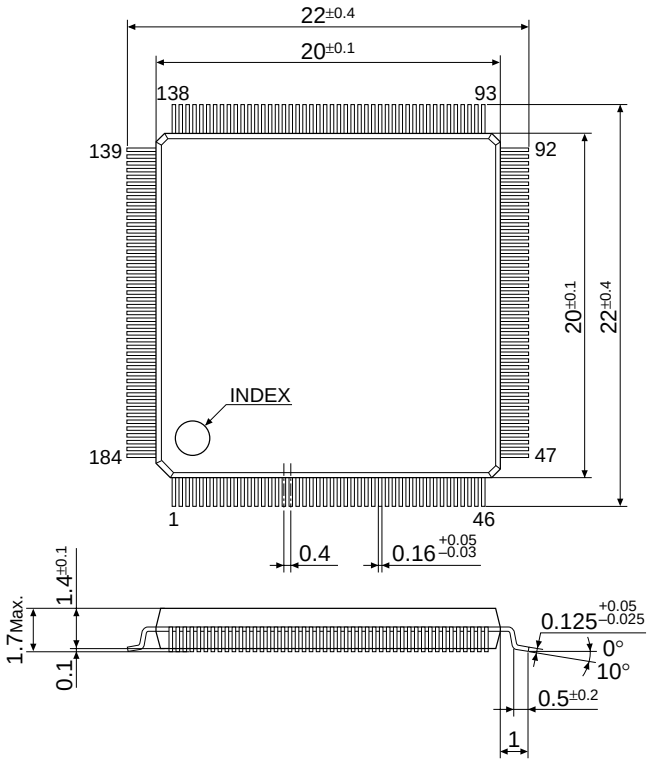
Pin Name	Pin No.	I/O	Reset	Functional Description	Remarks
Clock Generator Pin					
OSC3	171	I		High speed oscillation input (external clock input)	EXCLK_EN=Input when LOW
EXCLK_EN	116	I		CPU clock internal supply/External input setting terminal	HIGH:Internal supply LOW:External input
PLLS1	161	I		PLL setting pin 1	PLL circuit can not be used Connect to GND
PLLS0	160	I		PLL setting pin 0	
PLLC	158	-		Capacitor connection pin for PLL	N.C.

Pin Name	Pin No.	I/O	Reset	Functional Description	Remarks
Other pins					
ICEMD	179	I		High impedance control: makes all outputs Hi-Z	A pull-down resistor is built in.
X2PSDX	155	I		Double speed mode setting pin HIGH: CPU clock=BCLK×1 LOW: CPU clock=BCLK×2	
XNMI	177	I		NMI input pin	
XRESET	178	I		Initial reset	
HCLK	181	O		Dividing output which is 1/2 that of SCLK	
TVEP	58	-		FLASH test pin. Connect it to HV_{DD} when mounting.	

Pin Name	Pin No.	I/O	Reset	Functional Description	Remarks
Test Pin					
TI8	121	I	-		Schmidt input (bus holder)
TO7	122	O	-	(MSB)	
TO6	123	O	-		
TO5	124	O	-		
TO4	125	O	-	Output pin for testing	Drive capacity: 1 mA
TO3	126	O	-		
TO2	127	O	-		
TO1	128	O	-		
TO0	129	O	-	(LSB)	
FLSTST	55	I	-	Built-in FLASH test pin	A pull-down resistor is built in.
RAMTST	156	I	-	Built-in SRAM test pin	A pull-down resistor is built in.
MonxWait	132	O	-	Internal logic xWait monitor pin	
MonxInt	120	O	-	Internal logic xInt monitor pin	
Power Supply Pin					
HV_{DD}	-	P		HIGH power supply (5V) 5,21,37,67,83,130,165,176 (8pins)	
LV_{DD}	-	P		LOW power supply (3.3V) 1,47,93,103,114,139 (6pins)	
V_{SS}	-	P		GND 148,157,159,170,173,180,184 13,29,46,57,75,92,112,117,118,119,138(18pins)	
N.C. Pin					
N.C.	-	-		2,45,48,91,94,137,140,172,183 (9pins)	

■ DIMENSIONAL OUTLINE DRAWING

Plastic QFP20-184 pin (S1R72803F00A)



unit:mm

SEIKO EPSON CORPORATION

ELECTRONIC DEVICES MARKETING DIVISION

IC Marketing & Engineering Group

ED International Marketing Department
421-8 Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: 042-587-5814 FAX: 042-587-5117

■ EPSON Electronic Devices Website

http://www.epsondevice.com/

ENERGY SAVING EPSON

First issue January, 2001
Printed June, 2003 in Japan Ⓗ