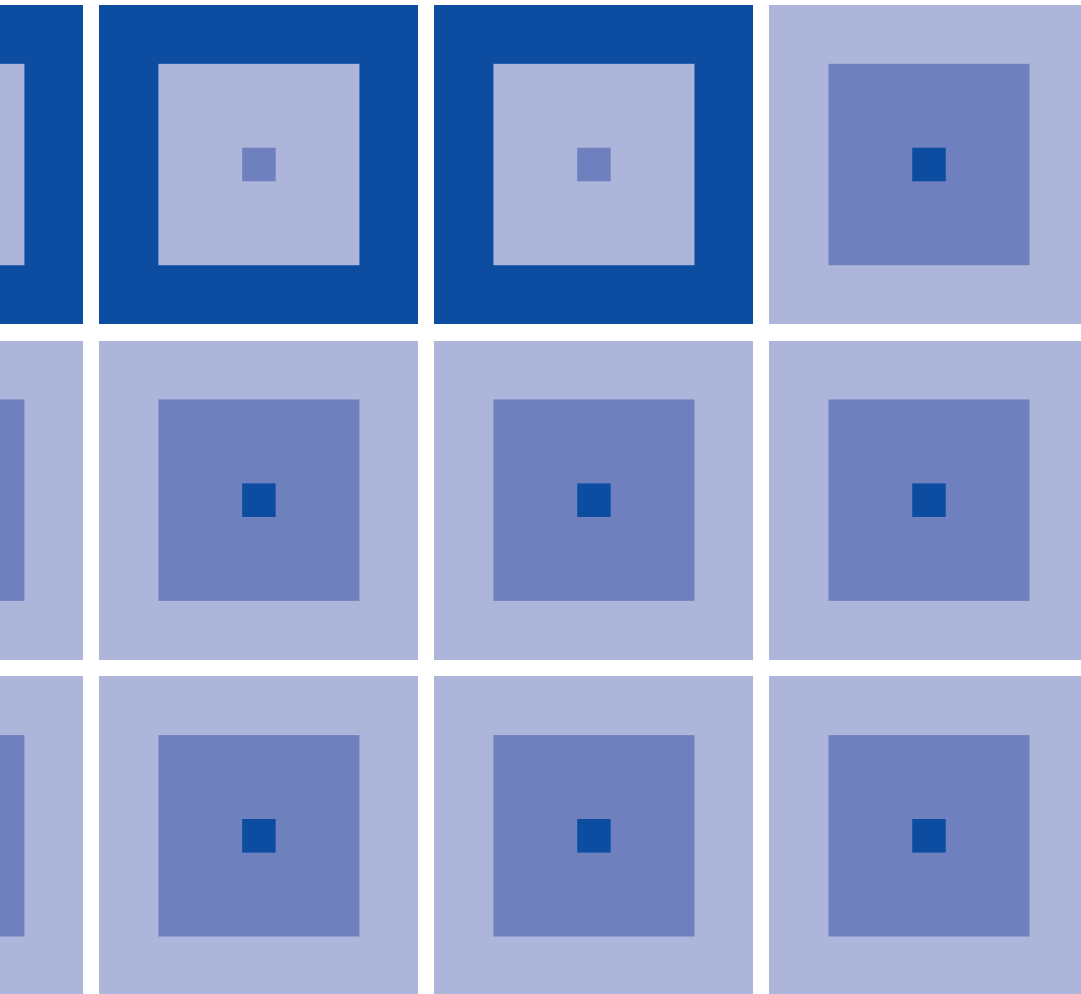


Controller

# 72900F00A

## Technical Manual



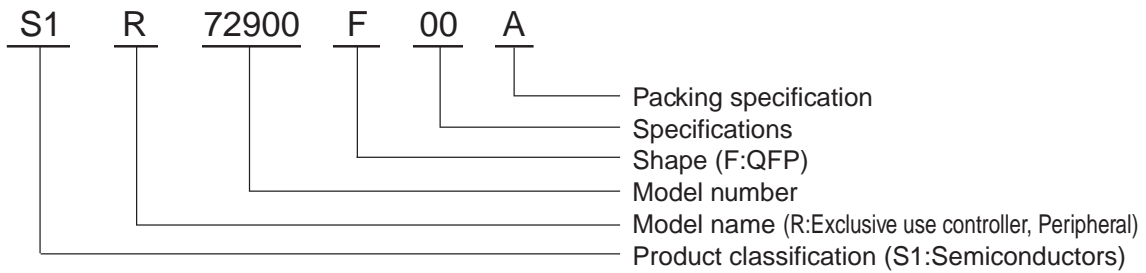


## The information of the product number change

Starting April 1, 2001 the product number has been changed as listed below. Please use the new product number when you place an order. For further information, please contact Epson sales representative.

## Configuration of product number

### ●DEVICES



# Contents

|  |    |
|--|----|
| 1. DESCRIPTION .....                       | 1  |
| 2. FEATURES .....                          | 1  |
| 3. BLOCK DIAGRAM .....                     | 2  |
| 4. PIN LAYOUT .....                        | 3  |
| 5. PIN ASSIGNMENT TABLE .....              | 4  |
| 6. PIN DESCRIPTION .....                   | 7  |
| 7. FUNCTIONAL DESCRIPTION .....            | 9  |
| 7.1 Control Register .....                 | 9  |
| 7.2 Data Format .....                      | 24 |
| 7.3 Cable Port Interface .....             | 27 |
| 7.4 Link Layer Controller Interface .....  | 30 |
| 7.5 Oscillating Circuit .....              | 42 |
| 7.6 Power Down .....                       | 42 |
| 8. ELECTRICAL CHARACTERISTICS .....        | 43 |
| 8.1 Absolute Maximum Ratings .....         | 43 |
| 8.2 Recommended Operating Conditions ..... | 43 |
| 8.3 DC Characteristics .....               | 44 |
| 8.4 AC Characteristics .....               | 47 |
| 9. EXAMPLE OF EXTERNAL CONNECTION .....    | 49 |
| 10. OUTLINE DIMENSIONS .....               | 50 |

## 1. DESCRIPTION

The SIR72900F00A is a physical layer IC compliant with the IEEE 1394-1995 and IEEE 1394a-2000 standards.

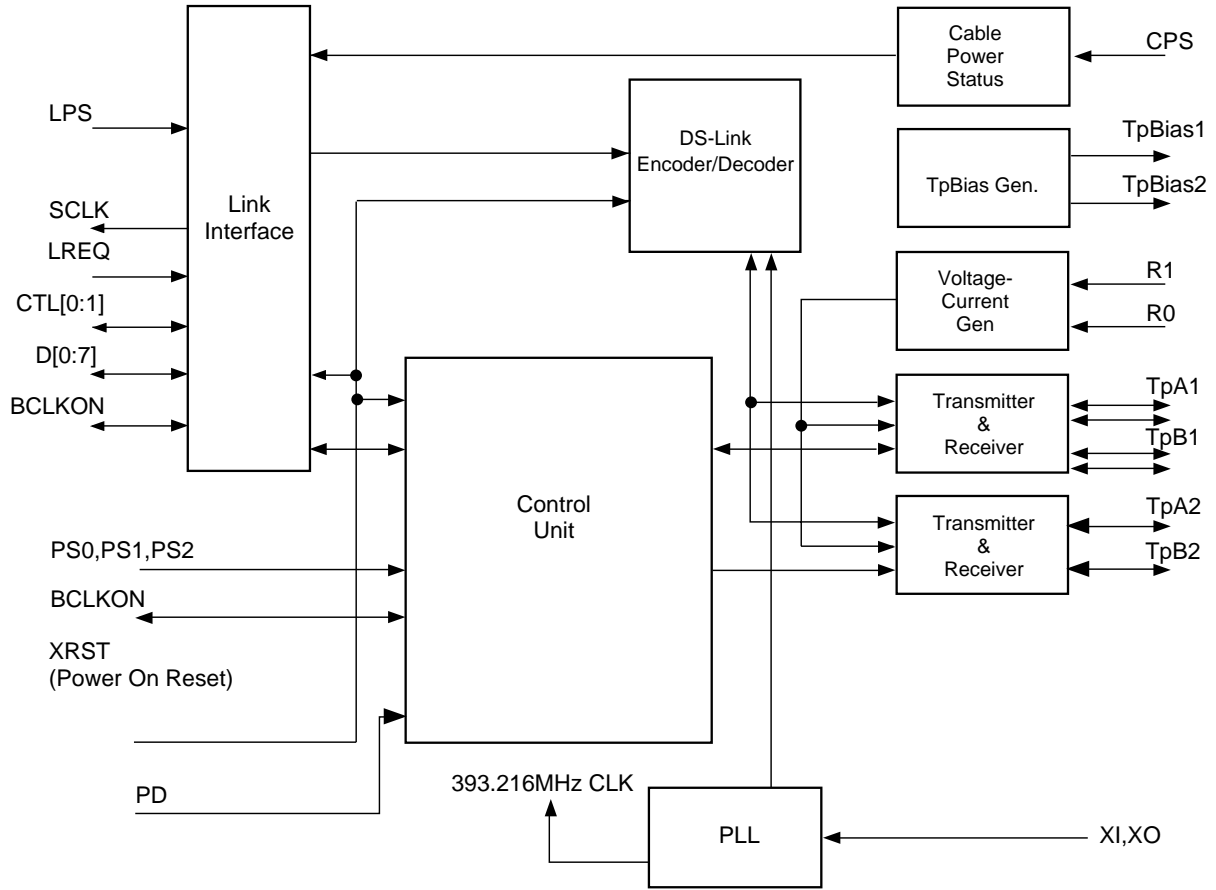
With the two 1394 ports, the SIR72900F00A supports transmission speeds of 400/200/100 Mbit/sec. The product incorporates a 400-MHz PLL, reference voltage generating circuit, high-speed transceiver, LINK layer interface, and a state machine circuit for bus initialization and arbitration.

## 2. FEATURES

- Complies with the IEEE 1394-1995 and IEEE 1394a-2000 standards.
- Supports transmission speeds of S400 (393.216 Mbit/sec), S200 (196.608 Mbit/sec), and S100 (98.304 Mbit/sec).
- Incorporates a 400-MHz PLL for transmission at S400/S200/S100 and 50-MHz SCLK output.
- Offers independent TpBias output for each port.
- Supports the Cable Power Status function that detects a cable power drop.
- Supports DC and AC connections of the PHY/LINK interface.
- Built-in oscillating circuit
- High-accuracy, low-amplitude differential high-speed transceiver
- Bus initialization, arbitration, port connection, and control state machine circuits
- PHY/LINK interface circuit
- High-speed DS encoder
- Supports the short bus reset function at detection of LINK layer IC power-off.
- Single 3.3-V power supply
- 64-Pin Plastic QFP
- Designed with the low-power CMOS technology.

\* This product is not radioresistant.

3. BLOCK DIAGRAM





### 5. PIN ASSIGNMENT TABLE

The items listed on the pin assignment table are as follows:

|             |  |
|-------------|--|
| PIN No.     | Pin number   |
| PIN NAME    | Pin name of the SIR72900F00A   |
| POWER PLANE | Supply voltage for each I/O cell<br>V <sub>DD</sub> : 3.3-V power supply for the digital circuit<br>AV <sub>DD</sub> : 3.3-V power supply for the analog circuit<br>PV <sub>DD</sub> : 3.3-V power supply for the PLL circuit<br>OSCV <sub>DD</sub> : 3.3-V power supply for the oscillating circuit |
| I/O ATTR    | Type of I/O cells<br>I : Input pin<br>O : Output pin<br>I/O : Input/output pin<br>P : Power pin  |
| DRIVE       | Drivability of output pins   |
| TERM        | Resistance of the pull-up or pull-down resistor provided on the pin  |



| PIN No. | PIN NAME   | POWER PLANE | I/O ATTR | DRIVE(mA) |     | TERM( $\Omega$ ) |
|---------|------------|-------------|----------|-----------|-----|------------------|
|         |            |             |          | 3.3V      |     | 3.3V             |
|         |            |             |          | IOL       | IOH |                  |
| 1       | LREQ       | VDD         | I        | -         | -   | -                |
| 2       | SCLK       | VDD         | O        | -6        | 6   | -                |
| 3       | BNC        | VDD         | O        | -2        | 2   | -                |
| 4       | CTL0       | VDD         | I/O      | -6        | 6   | -                |
| 5       | CTL1       | VDD         | I/O      | -6        | 6   | -                |
| 6       | D0         | VDD         | I/O      | -6        | 6   | -                |
| 7       | D1         | VDD         | I/O      | -6        | 6   | -                |
| 8       | D2         | VDD         | I/O      | -6        | 6   | -                |
| 9       | D3         | VDD         | I/O      | -6        | 6   | -                |
| 10      | D4         | VDD         | I/O      | -6        | 6   | -                |
| 11      | D5         | VDD         | I/O      | -6        | 6   | -                |
| 12      | D6         | VDD         | I/O      | -6        | 6   | -                |
| 13      | D7         | VDD         | I/O      | -6        | 6   | -                |
| 14      | PD         | VDD         | I        | -         | -   | -                |
| 15      | LPS        | VDD         | I        | -         | -   | -                |
| 16      | VDD        | VDD         | -        | -         | -   | -                |
| 17      | Vss        | Vss         | -        | -         | -   | -                |
| 18      | Vss        | Vss         | -        | -         | -   | -                |
| 19      | BCLKON     | VDD         | I/O      | -6        | 6   | -                |
| 20      | PS2        | VDD         | I        | -         | -   | -                |
| 21      | PS1        | VDD         | I        | -         | -   | -                |
| 22      | PS0        | VDD         | I        | -         | -   | -                |
| 23      | DIRECT     | VDD         | I        | -         | -   | -                |
| 24      | CPS        | VDD         | I        | -         | -   | -                |
| 25      | VDD        | VDD         | -        | -         | -   | -                |
| 26      | VDD        | VDD         | -        | -         | -   | -                |
| 27      | XTEST_MODE | VDD         | I        | -         | -   | -                |
| 28      | TEST0      | VDD         | I        | -         | -   | -                |
| 29      | TEST1      | VDD         | I        | -         | -   | -                |
| 30      | AVDD       | AVDD        | -        | -         | -   | -                |
| 31      | AVDD       | AVDD        | -        | -         | -   | -                |
| 32      | AVss       | AVss        | -        | -         | -   | -                |
| 33      | AVss       | AVss        | -        | -         | -   | -                |
| 34      | TPB0_N     | AVDD        | I/O      | -         | -   | -                |
| 35      | TPB0_P     | AVDD        | I/O      | -         | -   | -                |
| 36      | TPA0_N     | AVDD        | I/O      | -         | -   | -                |
| 37      | TPA0_P     | AVDD        | I/O      | -         | -   | -                |
| 38      | TPBIAS0    | AVDD        | O        | -         | -   | -                |
| 39      | AVss       | AVss        | -        | -         | -   | -                |
| 40      | R0         | AVDD        | O        | -         | -   | -                |
| 41      | R1         | AVDD        | O        | -         | -   | -                |
| 42      | AVDD       | AVDD        | -        | -         | -   | -                |
| 43      | TPB1_N     | AVDD        | I/O      | -         | -   | -                |
| 44      | TPB1_P     | AVDD        | I/O      | -         | -   | -                |
| 45      | TPA1_N     | AVDD        | I/O      | -         | -   | -                |
| 46      | TPA1_P     | AVDD        | I/O      | -         | -   | -                |
| 47      | TPBIAS1    | AVDD        | O        | -         | -   | -                |
| 48      | AVss       | AVss        | -        | -         | -   | -                |

| PIN No. | PIN NAME | POWER PLANE | I/O ATTR | DRIVE(mA) |     | TERM( $\Omega$ ) |
|---------|----------|-------------|----------|-----------|-----|------------------|
|         |          |             |          | 3.3V      |     | 3.3V             |
|         |          |             |          | IOL       | IOH |                  |
| 49      | AVSS     | AVSS        | –        | –         | –   | –                |
| 50      | AVSS     | AVSS        | –        | –         | –   | –                |
| 51      | AVDD     | AVDD        | –        | –         | –   | –                |
| 52      | AVDD     | AVDD        | –        | –         | –   | –                |
| 53      | XRST     | VDD         | I        | –         | –   | 100              |
| 54      | FC0      | PVDD        | –        | –         | –   | –                |
| 55      | FC1      | PVDD        | –        | –         | –   | –                |
| 56      | PVDD     | PVDD        | –        | –         | –   | –                |
| 57      | PVSS     | PVSS        | –        | –         | –   | –                |
| 58      | OSCVSS   | OSCVSS      | –        | –         | –   | –                |
| 59      | XI       | OSCVDD      | I        | –         | –   | –                |
| 60      | XO       | OSCVDD      | O        | –         | –   | –                |
| 61      | OSCVDD   | OSCVDD      | –        | –         | –   | –                |
| 62      | VDD      | VDD         | –        | –         | –   | –                |
| 63      | VSS      | VSS         | –        | –         | –   | –                |
| 64      | VSS      | VSS         | –        | –         | –   | –                |

## 6. PIN DESCRIPTION

| Pin name          | Function  | Pin No.                 | Pin typ.     | I/O |
|-------------------|---|-------------------------|--------------|-----|
| AVDD              | Analog circuit power supply pin   | 30,31,42,51,52          | Supply       | –   |
| AVSS              | Analog circuit ground pin   | 32,33,39,48,49,50       | Supply       | –   |
| PVDD              | PLL circuit power supply pin  | 56                      | Supply       | –   |
| PVSS              | PLL circuit ground pin  | 57                      | Supply       | –   |
| VDD               | Digital circuit power supply pin  | 16,25,26,62             | Supply       | –   |
| VSS               | Digital circuit ground pin  | 17,18,63,64             | Supply       | –   |
| OSCVDD            | Oscillating circuit power supply pin  | 61                      | Supply       | –   |
| OSCVSS            | Oscillating circuit ground pin  | 58                      | Supply       | –   |
| TPA0_P            | Port 0, TPA+ I/O signal   | 37                      | Differential | I/O |
| TPA0_N            | Port 0, TPA– I/O signal   | 36                      | Differential | I/O |
| TPB0_P            | Port 0, TPB+ I/O signal   | 35                      | Differential | I/O |
| TPB0_N            | Port 0, TPB– I/O signal   | 34                      | Differential | I/O |
| TPBIAS0           | Port 0, TP bias voltage supply pin  | 38                      | Supply       | O   |
| TPA1_P            | Port 1, TPA+ I/O signal   | 46                      | Differential | I/O |
| TPA1_N            | Port 1, TPA– I/O signal   | 45                      | Differential | I/O |
| TPB1_P            | Port 1, TPB+ I/O signal   | 44                      | Differential | I/O |
| TPB1_N            | Port 1, TPB– I/O signal   | 43                      | Differential | I/O |
| TPBIAS1           | Port 1, TP bias voltage supply pin  | 47                      | Supply       | O   |
| R1, R0            | Connect 6.0kΩ(1.0%) between the external reference resistor connecting pins R1 and R0.  | 41,40                   | Analog       | O   |
| PD                | Power down input pin<br>Connect this pin to VSS during normal operation.  | 14                      | Hysteresis   | I   |
| BCLKON            | Bus Manager Contender/Link-On pin<br>The status of this pin determines whether the bus manager function is used at the time of hard reset. See 7.4.3.         | 19                      | CMOS         | I/O |
| LREQ              | Request signal from the Link layer controller IC  | 1                       | Hysteresis   | I   |
| CTL0, CTL1        | PHY/LINK interface bidirectional control signal   | 4,5                     | Hysteresis   | I/O |
| D0 to D7          | PHY/LINK interface bidirectional data signal  | 6,7,8,9,<br>10,11,12,13 | Hysteresis   | I/O |
| SCLK              | 49.152 MHz system clock to the Link layer controller IC   | 2                       |              | O   |
| LPS               | Link power status pin.<br>A signal used to monitor whether the Link layer controller IC is active.  | 15                      | Hysteresis   | I   |
| PS2<br>PS1<br>PS0 | Power status pin<br>These pins configure the POWER CLASS bit of the Self-ID packet. PS0, PS1, and PS2 are respectively bits 21, 22, 23 of the Self-ID packet. | 20,21,22                | CMOS         | I   |
| DIRECT            | Configured according to the isolation barrier configuration between PHY and LINK.<br>Connect this pin to VDD for DC or single capacitor AC connection.        | 23                      | CMOS         | I   |

| Pin name   | Function   | Pin No.    | Pin typ.   | I/O |
|------------|--|------------|------------|-----|
| XTEST_MODE | Test pin<br>Connect this pin to V <sub>DD</sub> during normal operation.   | 27         | CMOS       | I   |
| XRST       | Reset pin<br>The SIR72900F00A is initialized when this pin is set to 0.<br>After turning on the power supply, for at least 2ms, maintain XRST = 0.<br>Set this pin to 1 during normal operation. | 53         | Hysteresis | I   |
| CPS        | Cable Power Status detection pin<br>Connect this pin to the cable power through a 240k $\Omega$ resistor.<br>Also, connect a diode (V <sub>F</sub> = 0.4V) between the PHY-V <sub>DD</sub> .     | Hysteresis | I          |     |
| BNC        | Signal indicating the cable status.<br>Outputs HIGH when all the ports do not receive bias voltage from the node on the other side.  | 3          | CMOS       | O   |
| FC0        | Connection pin for PLL filter<br>The SIR72900F00A does not need external capacitor. Set this pin to open.  | 54         | Analog     | O   |
| FC1        | Connection pin for PLL filter<br>The SIR72900F00A does not need external capacitor. Set this pin to open.  | 55         | Analog     | O   |
| XI         | Pin for a 24.576MHz crystal oscillator   | 59         |            |     |
| XO         | Pin for a 24.576MHz crystal oscillator   | 60         |            |     |
| TEST0      | Test pin<br>Connect this pin to V <sub>SS</sub> during normal operation.   | 28         | CMOS       | I   |
| TEST1      | Test pin<br>Connect this pin to V <sub>SS</sub> during normal operation.   | 29         | CMOS       | I   |

## 7. FUNCTIONAL DESCRIPTION

### 7.1 Control Register

#### 7.1.1 Accessing the register

The registers on the SIR72900F00A are accessed from the Link layer controller IC. For details, see Section 7.4.4 Link interface.

Table 7.1 Registers

| Name      | Address | 0           | 1         | 2         | 3           | 4           | 5           | 6          | 7          |    |
|-----------|---------|-------------|-----------|-----------|-------------|-------------|-------------|------------|------------|----|
| Register0 | 0000    | Physical_ID |           |           |             |             |             |            | R          | PS |
| Register1 | 0001    | RHB         | IBR       | Gap_count |             |             |             |            |            |    |
| Register2 | 0010    | Extended    |           |           | Total_ports |             |             |            |            |    |
| Register3 | 0011    | Max_speed   |           |           |             | Delay       |             |            |            |    |
| Register4 | 0100    | LCtrl       | Contender | Jitter    |             |             | Power_class |            |            |    |
| Register5 | 0101    | Watchdog    | ISBR      | Loop      | Pwr_fail    | Timeout     | Port_event  | Enab_accel | Enab_multi |    |
| Register6 | 0110    |             |           |           |             |             |             |            |            |    |
| Register7 | 0111    | Page_Select |           |           |             | Port_Select |             |            |            |    |
| –         | 1000    | Register8   |           |           |             |             |             |            |            |    |
| –         | 1001    | Register9   |           |           |             |             |             |            |            |    |
| –         | 1010    | RegisterA   |           |           |             |             |             |            |            |    |
| –         | 1011    | RegisterB   |           |           |             |             |             |            |            |    |
| –         | 1100    | RegisterC   |           |           |             |             |             |            |            |    |
| –         | 1101    | RegisterD   |           |           |             |             |             |            |            |    |
| –         | 1110    | RegisterE   |           |           |             |             |             |            |            |    |
| –         | 1111    | RegisterF   |           |           |             |             |             |            |            |    |

#### 7.1.2 Register bits

This section explains the control register bits of the SIR72900F00A. In the R/W column, R means read only and R/W means readable/writable. The Power Reset Value column shows the initial value (0 or 1) which each bit takes after power-on reset.

##### 7.1.2.1 Register 0

| Address | Bit Symbol       | R/W | Power Reset Value | Description        |
|---------|------------------|-----|-------------------|--------------------|
| 0x01    | 0: RHB           | R/W | 0                 | Root Hold Bit      |
|         | 1: IBR           | R/W | 0                 | Initiate Bus Reset |
|         | 2: Gap_count [0] | R/W | 1                 | Gap Count_bit0     |
|         | 3: Gap_count [1] | R/W | 1                 | Gap Count_bit1     |
|         | 4: Gap_count [2] | R/W | 1                 | Gap Count_bit2     |
|         | 5: Gap_count [3] | R/W | 1                 | Gap Count_bit3     |
|         | 6: Gap_count [4] | R/W | 1                 | Gap Count_bit4     |
|         | 7: Gap_count [5] | R/W | 1                 | Gap Count_bit5     |

##### Bits 0 to 5: Physical Node ID

This register address 00h is output as a status to the PHY/LINK interface after transmission of a Self-ID packet. These bits indicate Node IDs that were determined during a Self-ID period and they are determined when transmitting a Self-ID packet during a Self-ID period. These bits are initialized by bus reset (BR).

##### Bit 6: Root Indicator

This bit is determined during a Tree-ID period and it indicates the root setting for its node. When this bit is '1', this node is set as the root and initialized by bus reset.

##### Bit 7: Cable Power Status

This bit indicates the cable power supply status reflecting the status of the CPS pin. When this bit is '1', it indicates that the power is supplied through the cable.

## 7.1.2.2 Register 1

| Address | Bit Symbol       | R/W | Power Reset Value | Description        |
|---------|------------------|-----|-------------------|--------------------|
| 0x01    | 0: RHB           | R/W | 0                 | Root Hold Bit      |
|         | 1: IBR           | R/W | 0                 | Initiate Bus Reset |
|         | 2: Gap_count [0] | R/W | 1                 | Gap Count_bit0     |
|         | 3: Gap_count [1] | R/W | 1                 | Gap Count_bit1     |
|         | 4: Gap_count [2] | R/W | 1                 | Gap Count_bit2     |
|         | 5: Gap_count [3] | R/W | 1                 | Gap Count_bit3     |
|         | 6: Gap_count [4] | R/W | 1                 | Gap Count_bit4     |
|         | 7: Gap_count [5] | R/W | 1                 | Gap Count_bit5     |

## Bit 0: Root Hold Bit

This bit is set automatically by PHY configuration packet transmission.

When this bit is '1', it is a request that the node should be the root at the next bus reset.

## Bit 1: Initiate Bus Reset

Setting this bit immediately issues a bus reset command.

When this bit is '1', a bus reset is issued. This bit is initialized by bus reset.

## Bits 2 to 7: Gap Count

These bits are also set automatically by PHY Configuration packet transmission indicating Gap Count values. They retain the value at the first bus reset after configuration, and are initialized at the second bus reset.

## 7.1.2.3 Register 2

| Address | Bit Symbol       | R/W | Power Reset Value | Description |
|---------|------------------|-----|-------------------|-------------|
| 0x03    | 0: Max_speed [0] | R   | 0                 | Speed       |
|         | 1: Max_speed [1] | R   | 1                 | Speed       |
|         | 2: Max_speed [2] | R   | 0                 | Speed       |
|         | 3: Reserved      | R   | 0                 |             |
|         | 4: Delay [0]     | R   | 0                 | Delay       |
|         | 5: Delay [1]     | R   | 0                 | Delay       |
|         | 6: Delay [2]     | R   | 1                 | Delay       |
|         | 7: Delay [3]     | R   | 0                 | Delay       |

## Bits 0 to 2: Extended register

The register map that the SIR72900F00A supports. '111b' is read.

## Bits 3 to 7: Total of Port

The number of ports on the SIR72900F00A. Normally, 2 ('00010b') is read.

## 7.1.2.4 Register 3

| Address | Bit Symbol         | R/W | Power Reset Value | Description  |
|---------|--------------------|-----|-------------------|--------------|
| 0x04    | 0: LCtrl           | R/W | 1                 | Link Control |
|         | 1: Contender       | R/W | See discription   | Contender    |
|         | 2: Jitter [0]      | R   | 0                 | Jitter       |
|         | 3: Jitter [1]      | R   | 0                 | Jitter       |
|         | 4: Jitter [2]      | R   | 0                 | Jitter       |
|         | 5: Power_class [0] | R/W | 0                 | Power Class  |
|         | 6: Power_class [1] | R/W | 0                 | Power Class  |
|         | 7: Power_class [2] | R/W | 0                 | Power Class  |

**Bits 0 to 2: Speed**

The maximum transmission speed the SIR72900F00A supports. Normally, 2 ('010b') is read.

**Bit 3: Reserved****Bits 4 to 7: Delay**

The SIR72900F00A's repeat delay in the worst cases. Normally, 2 ('0010b') is read.

The maximum repeat delay time of the SIR72900F00A is 0.184  $\mu$ s.

**7.1.2.5 Register 4**

| Address | Bit Symbol         | R/W | Power Reset Value | Description  |
|---------|--------------------|-----|-------------------|--------------|
| 0x04    | 0: LCtrl           | R/W | 1                 | Link Control |
|         | 1: Contender       | R/W | See discription   | Contender    |
|         | 2: Jitter [0]      | R   | 0                 | Jitter       |
|         | 3: Jitter [1]      | R   | 0                 | Jitter       |
|         | 4: Jitter [2]      | R   | 0                 | Jitter       |
|         | 5: Power_class [0] | R/W | 0                 | Power Class  |
|         | 6: Power_class [1] | R/W | 0                 | Power Class  |
|         | 7: Power_class [2] | R/W | 0                 | Power Class  |

**Bit 0: Link Control**

This bit controls the value of the L (link\_active) field of the Self-ID packet. The L (link\_active) field of the Self-ID packet reflects the logical multiplication between this bit and LPS signal.

This bit is initialized to '1' as bus reset occurs.

**Bit 1: Contender**

This bit reflects the c (CONTENDER) field of the Self-ID packet. This bit has the same meaning as the c (CONTENDER) field of the Self-ID packet.

This bit reflects the value of the BCLKON pin when hardware reset occurs.

**Bits 2 to 4: Jitter**

A difference between the maximum and minimum repeat delays of the SIR72900F00A. Normally, 0'000b' is read.

The repeat jitter of the SIR72900F00A is 20 ns.

**Bits 5 to 7: Power Class**

These bits reflect the pwr (POWER\_CLASS) field of the Self-ID packet. They have the same meaning as the pwr (POWER\_CLASS) field of the Self-ID packet.

These bits are initialized to the value of pins PS0, PS1, and PS2 when hardware reset occurs.

The relationships between the bits and pins PS0, PS1, and PS2 are as follows:

bit5:PS0(Pin22)

bit6:PS1(Pin21)

bit7:PS2(Pin20)

## 7.1.2.6 Register 5

| Address | Bit Symbol    | R/W | Power Reset Value | Description                             |
|---------|---------------|-----|-------------------|---|
| 0x05    | 0: Watchdog   | R/W | 0                 | Watchdog                                |
|         | 1: ISBR       | R/W | 0                 | Initiate Short Bus Reset                |
|         | 2: Loop       | R/W | 0                 | Loop detect                             |
|         | 3: Pwr_fail   | R/W | 1                 | Cable power failure detect              |
|         | 4: Timeout    | R/W | 0                 | Arbtration state machine timeout        |
|         | 5: Port_event | R/W | 0                 | Port_event detect                       |
|         | 6: Enab_accel | R/W | 0                 | Enable arbitration acceleration         |
|         | 7: Enab_multi | R/W | 0                 | Enable multi-speed packet concatenation |

## Bit 0: Watchdog

When set to '1,' this bit communicates the status of Loop, Power\_fail, and Arb\_timeout to the Link layer controller IC, regardless of the status of the PHY/LINK interface. When a resume action starts on any port, this bit sends a resume interrupt signal regardless of the value of Int\_enable.

## Bit 1: Initiate Short (Arbitrated) Bus Reset

Setting this bit to '1' issues short bus reset.

This bit is cleared when the short bus reset completes.

## Bit 2: Loop detect

When this bit is '1,' the bus is looped.

This bit is cleared when hardware reset occurs or '1' is written.

## Bit 3: Cable power failure detect

When this bit is '1,' it means that the PC bit has changed from 1 to 0.

This bit is cleared when '1' is written.

## Bit 4: Arbitration state machine timeout

When this bit is '1,' it means that the node had been in a state other than Tree\_IDStart longer than MAX\_ARB\_STATE\_TIME.

This bit is cleared when hardware reset occurs or '1' is written.

## Bit 5: Port\_event detect

When Int\_enable is '1,' detection of a change in the Connected, Bias, Disabled, or Fault bit sets this bit to '1.' Also, when Watchdog is '1,' a Resume process sets this bit to '1.'

This bit is cleared when hardware reset occurs or '1' is written.

## Bit 6: Enable arbitration acceleration

Setting this bit to '1' causes Ack-acceleration arbitration and fly-by arbitration. When this bit is set to '0,' no acceleration arbitration occurs.

This bit is initialized as hardware reset occurs.

## Bit 7: Enable multi-speed packet concatenation

When this bit is set to '1,' a joint packet transmission request requires a speed code. When this bit is set to '0,' joint packet transmission is done at the same speed as the first packet transmission.

This bit is initialized as hardware reset occurs.



## 7.1.2.7 Register 6

| Address | Bit Symbol  | R/ $\overline{W}$ | Power Reset Value | Description |
|---------|-------------|-------------------|-------------------|-------------|
| 0x06    | 0: Reserved | R                 | 0                 |             |
|         | 1: Reserved | R                 | 0                 |             |
|         | 2: Reserved | R                 | 0                 |             |
|         | 3: Reserved | R                 | 0                 |             |
|         | 4: Reserved | R                 | 0                 |             |
|         | 5: Reserved | R                 | 0                 |             |
|         | 6: Reserved | R                 | 0                 |             |
|         | 7: Reserved | R                 | 0                 |             |

Bits 0 to 7: Reserved

## 7.1.2.8 Register 7

| Address | Bit Symbol         | R/ $\overline{W}$ | Power Reset Value | Description |
|---------|--------------------|-------------------|-------------------|-------------|
| 0x07    | 0: Page_select [0] | R/ $\overline{W}$ | 0                 |             |
|         | 1: Page_select [1] | R/ $\overline{W}$ | 0                 |             |
|         | 2: Page_select [2] | R/ $\overline{W}$ | 0                 |             |
|         | 3: Reserved        | R                 | 0                 |             |
|         | 4: Port_select [0] | R/ $\overline{W}$ | 0                 |             |
|         | 5: Port_select [1] | R/ $\overline{W}$ | 0                 |             |
|         | 6: Port_select [2] | R/ $\overline{W}$ | 0                 |             |
|         | 7: Port_select [3] | R/ $\overline{W}$ | 0                 |             |

Bits 0 to 2: Page Select

These bits specify what page between 1000b and 1111b of the PHY register should be accessed.

Bit 3: Reserved

Bits 4 to 7: Port Select

When the Page\_select bit selects Port Status Page, these bits specify what port between 1000b and 1111b of the PHY register should be accessed.

Table 7.2 Registers of Page\_Select 0

| Name       | Address | 0                | 1 | 2     | 3          | 4     | 5         | 6    | 7        |
|------------|---------|------------------|---|-------|------------|-------|-----------|------|----------|
| Register00 | 1000    | AStat            |   | BStat |            | Child | Connected | Bias | Disabled |
| Register01 | 1001    | Negotiated_speed |   |       | Int_enable | Fault |           |      |          |
| Register02 | 1010    |                  |   |       |            |       |           |      |          |
| Register03 | 1011    |                  |   |       |            |       |           |      |          |
| Register04 | 1100    |                  |   |       |            |       |           |      |          |
| Register05 | 1101    |                  |   |       |            |       |           |      |          |
| Register06 | 1110    |                  |   |       |            |       |           |      |          |
| Register07 | 1111    |                  |   |       |            |       |           |      |          |

### 7.1.3 Page\_select 0 bits

#### 7.1.3.1 Register 00

| Address | Bit Symbol   | R/W | Power Reset Value | Description   |
|---------|--------------|-----|-------------------|---------------|
| 0x08    | 0: Astat [0] | R   | 0                 | Status of TPA |
|         | 1: Astat [1] | R   | 0                 | Status of TPA |
|         | 2: Bstat [0] | R   | 0                 | Status of TPB |
|         | 3: Bstat [1] | R   | 0                 | Status of TPB |
|         | 4: Child     | R   | 0                 | Child         |
|         | 5: Connected | R   | 0                 | Connected     |
|         | 6: Bias      | R   | 0                 | Cable Bias    |
|         | 7: Disabled  | R/W | See description   | Port Disabled |

#### Bits 0 to 1: Status of TPA

These bits indicate the status of TPA. The meaning of these bits is as follows:

'11b':Z  
 '01b':1  
 '10b':0  
 '00b':invalid

#### Bits 2 to 3: Status of TPB

These bits indicate the status of TPB. The meaning of these bits is as follows:

'11b':Z  
 '01b':1  
 '10b':0  
 '00b':invalid

#### Bit 4: Child

When this bit is '1,' the port is a Child. When this bit is '0,' the port is a Parent.  
 This bit is initialized by bus reset, and determined during a Tree-ID period.

#### Bit 5: Connected

When this bit is '1,' it indicates that the port recognizes a node is connected.

#### Bit 6: Cable Bias

This bit reflects the cable bias detected at the port. When this bit is '1,' it indicates that TpBias is detected at the port.

#### Bit 7: Port Disabled

When this bit is set to '1,' the port is disabled.  
 This bit is initialized as hardware reset occurs.

### 7.1.3.2 Register 01

| Address | Bit Symbol              | R/W | Power Reset Value | Description                 |
|---------|-------------------------|-----|-------------------|-----------------------------|
| 0x09    | 0: Negotiated_speed [0] | R   | 0                 | Negotiated speed            |
|         | 1: Negotiated_speed [1] | R   | 0                 | Negotiated speed            |
|         | 2: Negotiated_speed [2] | R   | 0                 | Negotiated speed            |
|         | 3: Int_enable           | R/W | 0                 | Enable port event interrupt |
|         | 4: Fault                | R/W | 0                 | fault                       |
|         | 5: Reserved             | R   | 0                 |                             |
|         | 6: Reserved             | R   | 0                 |                             |
|         | 7: Reserved             | R   | 0                 |                             |

#### Bits 0 to 2: Negotiated speed

These bits indicate the speed of the node connected to the port.

They are initialized by bus reset, and determined during a Self-ID period.

The meaning of these bits is as follows:

'000b': The maximum transmission speed is 100 Mbps.

'001b': The maximum transmission speed is 200 Mbps.

'010b': The maximum transmission speed is 400 Mbps.

#### Bit 3: Enable port event interrupt

When this bit is set to '1,' the Port\_event bit is set to '1' when a change in the Connected, Bias, Disabled, or Fault bit occurs.

This bit is initialized as hardware reset occurs.

#### Bit 4: Fault

When this bit is '1,' it indicates that an error has occurred during suspend/resume operation.

This bit is cleared when hardware reset occurs or '1' is written.

Bits 5 to 7: Reserved

### 7.1.3.3 Register 02

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x0A    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

## 7.1.3.4 Register 03

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x0B    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

## 7.1.3.5 Register 04

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x0C    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

## 7.1.3.6 Register 05

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x0D    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

## 7.1.3.7 Register 06

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x0E    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

## 7.1.3.8 Register 07

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x0F    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

Table 7.3 Registers of Page\_Select 1

| Name       | Address | 0                  | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|------------|---------|--------------------|---|---|---|---|---|---|---|
| Register10 | 1000    | Compliance_level   |   |   |   |   |   |   |   |
| Register11 | 1001    |                    |   |   |   |   |   |   |   |
| Register12 | 1010    | Vendor_ID [16:23]  |   |   |   |   |   |   |   |
| Register13 | 1011    | Vendor_ID [8:15]   |   |   |   |   |   |   |   |
| Register14 | 1100    | Vendor_ID [0:7]    |   |   |   |   |   |   |   |
| Register15 | 1101    | Product_ID [16:23] |   |   |   |   |   |   |   |
| Register16 | 1110    | Product_ID [8:15]  |   |   |   |   |   |   |   |
| Register17 | 1111    | Product_ID [0:7]   |   |   |   |   |   |   |   |

### 7.1.4 Page\_select 1 bits

#### 7.1.4.1 Register 10

| Address | Bit Symbol              | R/W | Power Reset Value | Description      |
|---------|-------------------------|-----|-------------------|------------------|
| 0x08    | 0: Compliance_level [0] | R   | 0                 | Compliance_level |
|         | 1: Compliance_level [1] | R   | 0                 | Compliance_level |
|         | 2: Compliance_level [2] | R   | 0                 | Compliance_level |
|         | 3: Compliance_level [3] | R   | 0                 | Compliance_level |
|         | 4: Compliance_level [4] | R   | 0                 | Compliance_level |
|         | 5: Compliance_level [5] | R   | 0                 | Compliance_level |
|         | 6: Compliance_level [6] | R   | 0                 | Compliance_level |
|         | 7: Compliance_level [7] | R   | 1                 | Compliance_level |

Bits 0 to 7: Compliance Level

Normally, 1 ('01h') for P1394a-compliant is read.

#### 7.1.4.2 Register 11

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x09    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

## 7.1.4.3 Register 12

| Address | Bit Symbol        | R/W | Power Reset Value | Description     |
|---------|-------------------|-----|-------------------|-----------------|
| 0x0A    | 0: Vendor_ID [16] | R   | 0                 | Vendor_ID_bit16 |
|         | 1: Vendor_ID [17] | R   | 0                 | Vendor_ID_bit17 |
|         | 2: Vendor_ID [18] | R   | 0                 | Vendor_ID_bit18 |
|         | 3: Vendor_ID [19] | R   | 0                 | Vendor_ID_bit19 |
|         | 4: Vendor_ID [20] | R   | 0                 | Vendor_ID_bit20 |
|         | 5: Vendor_ID [21] | R   | 0                 | Vendor_ID_bit21 |
|         | 6: Vendor_ID [22] | R   | 0                 | Vendor_ID_bit22 |
|         | 7: Vendor_ID [23] | R   | 0                 | Vendor_ID_bit23 |

Bits 0 to 7: Vendor ID [16:23]  
For the SIR72900F00A, '00h' is read.

## 7.1.4.4 Register 13

| Address | Bit Symbol        | R/W | Power Reset Value | Description     |
|---------|-------------------|-----|-------------------|-----------------|
| 0x0B    | 0: Vendor_ID [8]  | R   | 0                 | Vendor_ID_bit8  |
|         | 1: Vendor_ID [9]  | R   | 0                 | Vendor_ID_bit9  |
|         | 2: Vendor_ID [10] | R   | 0                 | Vendor_ID_bit10 |
|         | 3: Vendor_ID [11] | R   | 0                 | Vendor_ID_bit11 |
|         | 4: Vendor_ID [12] | R   | 0                 | Vendor_ID_bit12 |
|         | 5: Vendor_ID [13] | R   | 0                 | Vendor_ID_bit13 |
|         | 6: Vendor_ID [14] | R   | 0                 | Vendor_ID_bit14 |
|         | 7: Vendor_ID [15] | R   | 0                 | Vendor_ID_bit15 |

Bits 0 to 7: Vendor ID [8:15]  
For the SIR72900F00A, '00h' is read.

## 7.1.4.5 Register 14

| Address | Bit Symbol       | R/W | Power Reset Value | Description    |
|---------|------------------|-----|-------------------|----------------|
| 0x0C    | 0: Vendor_ID [0] | R   | 0                 | Vendor_ID_bit0 |
|         | 1: Vendor_ID [1] | R   | 1                 | Vendor_ID_bit1 |
|         | 2: Vendor_ID [2] | R   | 0                 | Vendor_ID_bit2 |
|         | 3: Vendor_ID [3] | R   | 0                 | Vendor_ID_bit3 |
|         | 4: Vendor_ID [4] | R   | 1                 | Vendor_ID_bit4 |
|         | 5: Vendor_ID [5] | R   | 0                 | Vendor_ID_bit5 |
|         | 6: Vendor_ID [6] | R   | 0                 | Vendor_ID_bit6 |
|         | 7: Vendor_ID [7] | R   | 0                 | Vendor_ID_bit7 |

Bits 0 to 7: Vendor ID [0:7]  
For the SIR72900F00A, '48h' is read.

## 7.1.4.6 Register 15

| Address | Bit Symbol         | R/W | Power Reset Value | Description      |
|---------|--------------------|-----|-------------------|------------------|
| 0x0D    | 0: Product_ID [16] | R   | 0                 | Product_ID_bit16 |
|         | 1: Product_ID [17] | R   | 0                 | Product_ID_bit17 |
|         | 2: Product_ID [18] | R   | 0                 | Product_ID_bit18 |
|         | 3: Product_ID [19] | R   | 0                 | Product_ID_bit19 |
|         | 4: Product_ID [20] | R   | 0                 | Product_ID_bit20 |
|         | 5: Product_ID [21] | R   | 0                 | Product_ID_bit21 |
|         | 6: Product_ID [22] | R   | 0                 | Product_ID_bit22 |
|         | 7: Product_ID [23] | R   | 0                 | Product_ID_bit23 |

Bits 0 to 7: Product ID [16:23]  
For the SIR72900F00A, '00h' is read.

## 7.1.4.7 Register 16

| Address | Bit Symbol         | R/W | Power Reset Value | Description      |
|---------|--------------------|-----|-------------------|------------------|
| 0x0E    | 0: Product_ID [8]  | R   | 0                 | Product_ID_bit8  |
|         | 1: Product_ID [9]  | R   | 0                 | Product_ID_bit9  |
|         | 2: Product_ID [10] | R   | 0                 | Product_ID_bit10 |
|         | 3: Product_ID [11] | R   | 0                 | Product_ID_bit11 |
|         | 4: Product_ID [12] | R   | 0                 | Product_ID_bit12 |
|         | 5: Product_ID [13] | R   | 0                 | Product_ID_bit13 |
|         | 6: Product_ID [14] | R   | 1                 | Product_ID_bit14 |
|         | 7: Product_ID [15] | R   | 0                 | Product_ID_bit15 |

Bits 0 to 7: Product ID [8:15]  
For the SIR72900F00A, '02h' is read.

## 7.1.4.8 Register 17

| Address | Bit Symbol        | R/W | Power Reset Value | Description     |
|---------|-------------------|-----|-------------------|-----------------|
| 0x0F    | 0: Product_ID [0] | R   | 0                 | Product_ID_bit0 |
|         | 1: Product_ID [1] | R   | 0                 | Product_ID_bit1 |
|         | 2: Product_ID [2] | R   | 0                 | Product_ID_bit2 |
|         | 3: Product_ID [3] | R   | 0                 | Product_ID_bit3 |
|         | 4: Product_ID [4] | R   | 0                 | Product_ID_bit4 |
|         | 5: Product_ID [5] | R   | 0                 | Product_ID_bit5 |
|         | 6: Product_ID [6] | R   | 0                 | Product_ID_bit6 |
|         | 7: Product_ID [7] | R   | 1                 | Product_ID_bit7 |

Bits 0 to 7: Product ID [0:7]  
For the SIR72900F00A, '01h' is read.



Table 7.3 Registers of Page\_Select 1

| Name       | Address | 0 | 1 | 2 | 3 | 4 | 5 | 6       | 7        |
|------------|---------|---|---|---|---|---|---|---------|----------|
| Register70 | 1000    |   |   |   |   |   |   | RemSCLk | HostIsbr |
| Register71 | 1001    |   |   |   |   |   |   |         |          |
| Register72 | 1010    |   |   |   |   |   |   |         |          |
| Register73 | 1011    |   |   |   |   |   |   |         |          |
| Register74 | 1100    |   |   |   |   |   |   |         |          |
| Register75 | 1101    |   |   |   |   |   |   |         |          |
| Register76 | 1110    |   |   |   |   |   |   |         |          |
| Register77 | 1111    |   |   |   |   |   |   |         |          |

### 7.1.5 Page\_select 7 bits

#### 7.1.5.1 Register 70

| Address     | Bit Symbol  | R/W | Power Reset Value | Description |
|-------------|-------------|-----|-------------------|-------------|
| 0x08        | 0: Reserved | R   | 0                 |             |
|             | 1: Reserved | R   | 0                 |             |
|             | 2: Reserved | R   | 0                 |             |
|             | 3: Reserved | R   | 0                 |             |
|             | 4: Reserved | R   | 0                 |             |
|             | 5: Reserved | R   | 0                 |             |
|             | 6: RemSCLK  | R/W | 0                 | Remain SCLK |
| 7: HostIsbr | R/W         | 0   | Host Isbr         |             |

Bits 0 to 5: Reserved

Bit 6: Remain SCLK

When this bit is set to '1,' SCLK output continues even if LPS is deasserted.

When this bit is '0,' the IC operates as per IEEE 1394a-2000.

Bit 7: Host Isbr

When this bit is '1,' the SIR72900F00A issues short bus reset when LPS is deasserted.

When this bit is '0,' the IC operates as per IEEE 1394a-2000.

#### 7.1.5.2 Register 71

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x09    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

## 7.1.5.3 Register 72

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x0A    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

## 7.1.5.4 Register 73

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x0B    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

## 7.1.5.5 Register 74

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x0C    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

**7.1.5.6 Register 75**

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x0D    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

**7.1.5.7 Register 76**

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x0E    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

**7.1.5.8 Register 77**

| Address | Bit Symbol  | R/W | Power Reset Value | Description |
|---------|-------------|-----|-------------------|-------------|
| 0x0F    | 0: Reserved | R   | 0                 |             |
|         | 1: Reserved | R   | 0                 |             |
|         | 2: Reserved | R   | 0                 |             |
|         | 3: Reserved | R   | 0                 |             |
|         | 4: Reserved | R   | 0                 |             |
|         | 5: Reserved | R   | 0                 |             |
|         | 6: Reserved | R   | 0                 |             |
|         | 7: Reserved | R   | 0                 |             |

Bits 0 to 7: Reserved

## 7.2 Data Format

### 7.2.1 Self-ID packet

The Self-ID packets the SIR72900F00A transmits are 2-quadlet packets in the format shown in Figure 7.1. The SIR72900F00A transmits the following Self-ID packet during Self-ID period of bus initialization. The SIR72900F00A also transmits a Self-ID packet automatically as a response to a Ping packet.

|                                  |        |   |   |   |   |   |   |   |   |         |   |   |   |    |     |   |     |   |   |    |    |   |   |   |   |   |   |   |   |   |  |
|----------------------------------|--------|---|---|---|---|---|---|---|---|---------|---|---|---|----|-----|---|-----|---|---|----|----|---|---|---|---|---|---|---|---|---|--|
| 0                                | 1      | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | #       | # | # | # | #  | #   | # | #   | # | # | #  | #  | # | # | # | # | # | # | # | # | # |  |
| #                                | phy-ID |   |   |   |   |   |   | 0 | L | gap_cnt |   |   |   | sp | rsv | c | pwr |   |   | p0 | p1 | 0 | i | m |   |   |   |   |   |   |  |
| logical inverse of first quadlet |        |   |   |   |   |   |   |   |   |         |   |   |   |    |     |   |     |   |   |    |    |   |   |   |   |   |   |   |   |   |  |

Figure 7.1 Self-ID packet format

phy\_ID: physical\_ID field  
Reflects the ID node of the IC.

L: LPS, LCtrl field  
Reflects the logical multiplication of the LPS pin and the LCtrl bit of PHY Register 4 at the time of Self-ID packet transmission.

gap\_cnt: gap\_cnt field  
Reflects the value of Gap\_Count of PHY Register 1.

sp: PHY\_SPEED field  
00 = 98.304 Mbps (S100)  
01 = 98.304/196.608 Mbps (S100/S200)  
10 = 98.304/196.608/393.216 Mbps (S100/S200/S300)  
11 = Reserved  
Applicable speeds are stored. For the SIR72900F00A, this field is fixed to '10b.'

rsv: Fixed to '00b.'

C: CONTENDER field  
Reflects the value of the Contender bit of PHY Register 4.

pwr: POWER\_CLASS field  
bit21 = PS0(Pin22)  
bit22 = PS1(Pin21)  
bit23 = PS2(Pin20)  
Reflects the Pwr bit of PHY Register 4.  
The IEEE P1394a-2000 standards define this field as follows:  
000 = The node does not need a power supply. The node does not repeat the power supply.  
001 = The node has its own power supply and is able to supply a minimum of 15 W.  
010 = The node has its own power supply and is able to supply a minimum of 30 W.  
011 = The node has its own power supply and is able to supply a minimum of 45 W.  
100 = The node can consume power up to 3 W from the cable. However, it does not consume any power to enable the Link or upper layers.  
101 = Reserved  
110 = The node can consume power up to 3 W from the cable. It can consume more power up to 3 W to enable the Link or upper layers.  
111 = The node can consume power up to 3 W from the cable. It can consume more power up to 7 W to enable the Link or upper layers.

p0, p1: Port connection status field  
Indicates the port status.  
11 = The port is active and connected to a child node.  
10 = The port is active and connected to a parent node.  
01 = The port is inactive (disabled, disconnected, or suspended).

- I: initiated\_reset field  
Indicates that the node has issued BusReset.
- m: more\_packets field  
This field is set to '1' when more than one Self-ID packet is sent. However, for the S1R72900F00A, this field is fixed to '0.'

### 7.2.2 Link-on Packet

|                                  |        |      |      |      |      |      |      |
|----------------------------------|--------|------|------|------|------|------|------|
| 01                               | phy-ID | 0000 | 0000 | 0000 | 0000 | 0000 | 0000 |
| logical inverse of first quadlet |        |      |      |      |      |      |      |

Figure 7.2 Link-on packet format

### 7.2.3 PHY Configuration Packet

|                                  |         |   |   |         |      |      |      |      |
|----------------------------------|---------|---|---|---------|------|------|------|------|
| 00                               | root-ID | R | T | gap_cnt | 0000 | 0000 | 0000 | 0000 |
| logical inverse of first quadlet |         |   |   |         |      |      |      |      |

Figure 7.3 PHY Configuration packet format

### 7.2.4 Extended PHY Packet

#### 7.2.4.1 Ping Packet

|                                  |        |    |         |    |      |      |      |      |
|----------------------------------|--------|----|---------|----|------|------|------|------|
| 00                               | phy-ID | 00 | type(0) | 00 | 0000 | 0000 | 0000 | 0000 |
| logical inverse of first quadlet |        |    |         |    |      |      |      |      |

Figure 7.4 Ping packet format

#### 7.2.4.2 Remote Access Packet

|                                  |        |    |            |      |      |     |          |
|----------------------------------|--------|----|------------|------|------|-----|----------|
| 00                               | phy-ID | 00 | type(1/5h) | page | port | reg | reserved |
| logical inverse of first quadlet |        |    |            |      |      |     |          |

Figure 7.5 Remote Access packet format

**7.2.4.3 Remote Reply Packet**

|                                  |        |    |            |      |      |     |      |
|----------------------------------|--------|----|------------|------|------|-----|------|
| 00                               | phy-ID | 00 | type(3/7h) | page | port | reg | data |
| logical inverse of first quadlet |        |    |            |      |      |     |      |

Figure 7.6 Remote Reply packet format

**7.2.4.4 Remote Command Packet**

|                                  |        |    |          |     |      |      |      |
|----------------------------------|--------|----|----------|-----|------|------|------|
| 00                               | phy-ID | 00 | type(8h) | 000 | port | 0000 | data |
| logical inverse of first quadlet |        |    |          |     |      |      |      |

Figure 7.7 Remote Command packet format

**7.2.4.5 Remote Confirmation Packet**

|                                  |        |    |          |     |      |      |   |   |   |   |    |      |
|----------------------------------|--------|----|----------|-----|------|------|---|---|---|---|----|------|
| 00                               | phy-ID | 00 | type(Ah) | 000 | port | 0000 | f | c | b | d | ok | cmnd |
| logical inverse of first quadlet |        |    |          |     |      |      |   |   |   |   |    |      |

Figure 7.8 Remote Confirmation packet format

**7.2.4.6 Resume Packet**

|                                  |        |    |          |    |      |      |      |
|----------------------------------|--------|----|----------|----|------|------|------|
| 00                               | phy-ID | 00 | type(Fh) | 00 | 0000 | 0000 | 0000 |
| logical inverse of first quadlet |        |    |          |    |      |      |      |

Figure 7.9 Resume packet format

## 7.3 Cable Port Interface

### 7.3.1 Cable port interface circuit

Figure 7.10 shows a circuit diagram of the cable port interface.

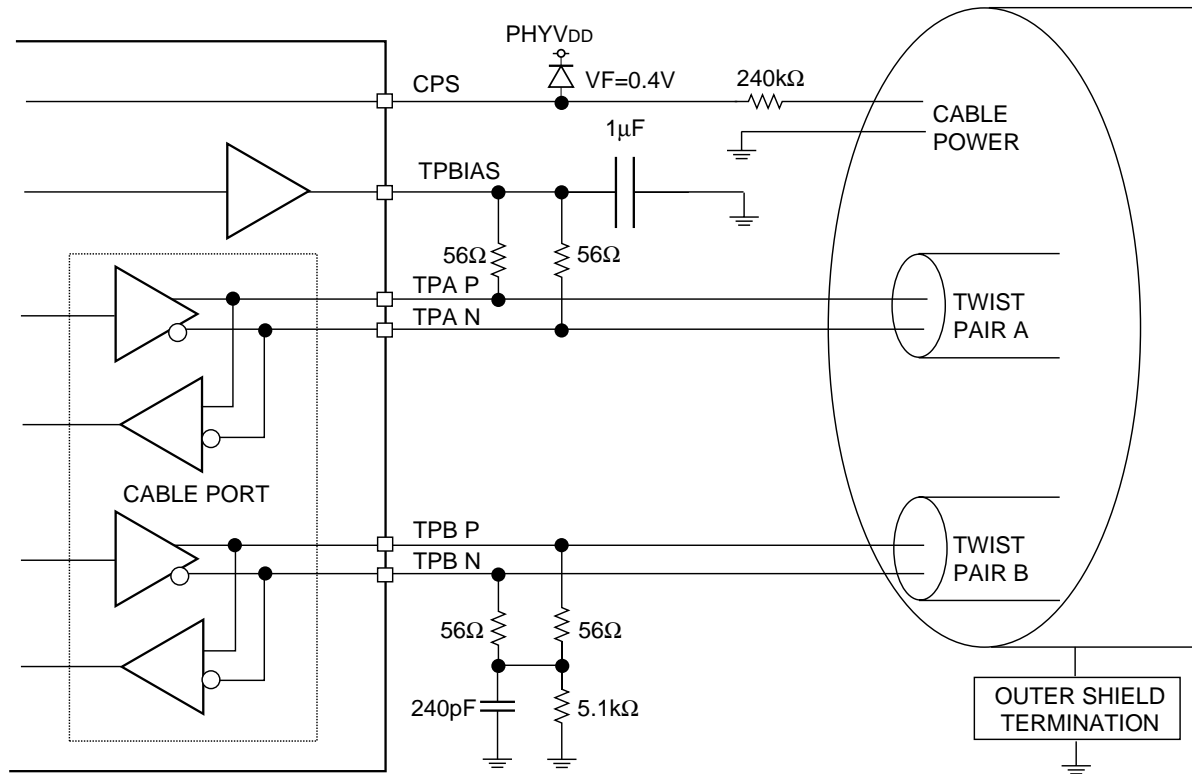


Figure 7.10 Cable port interface circuit

Figure 7.11 shows an example of outer shield circuit of the cable port.

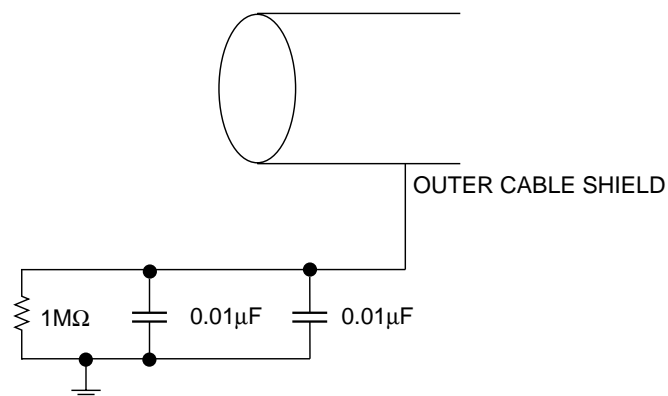


Figure 7.11 Cable port outer shield circuit

Cables specifically designed as per IEEE 1394 are used as media for the cable port interface. Data is transmitted through two shielded pairs of twisted cables. As shown in Figure 7.10, each twisted pair cable is connected to the TpB pair of the node to which the TpA pair of the own node.

Both TpA and TpB require two 56Ω terminating resistors appropriate to the cable impedance. Locate these terminating resistors as close to the IC pin as possible.

On the TpA side, TpBias is connected to the terminating resistor intermediate node to set inphase DC potential of the cable. To TpBias, connect a 1-μF capacitor for decoupling.

On the TpB side, connect a 5.1kΩ resistor and a 240-pF capacitor to the terminating resistor intermediate node for pull-down. The 240-pF capacitor is for decoupling.

Connect the CPS pin to the cable power through a 240kΩ resistor.

### 7.3.2 Port state

The SIR72900F00A complies with the IEEE 1394a-2000 standards. The IEEE P1394a-2000 standards define the following five port states.

–Disabled:

A 'disabled' port does not output signals to TpBias and TpA/TpB. And the port in this state does not detect signals input to Bias and TpA/TpB. When the connection detection circuit detects a change in cable connection, this port outputs an interrupt to the upper layer if the Int\_enable bit is set.

–Disconnected:

A 'disconnected' port has no physical cable connection to PHY on a different node and thus does not output signals to TpBias and TpA/TpB. And the port in this state does not detect signals input to Bias and TpA/TpB.

–Suspended:

A 'suspended' port does have physical cable connection to PHY on a different node but does not output signals to TpBias and TpA/TpB. And the port in this state does not detect signals input to TpA/TpB. On this port, only the bias detection and connection detection circuits are in operation.

–Resuming:

A 'resuming' port has physical cable connection to PHY on a different node and outputs signals to TpBias. On detection of bias, the port stays for a specified time and becomes active. During the resuming period, it does not detect signals input to TpA/TpB.

–Active:

An 'active' port has physical cable connection to PHY on a different node and outputs signals to TpBias and TpA/TpB. The port in this state detects signals input to Bias and TpA/TpB.

### 7.3.3 Connection detecting circuit

The SIR72900F00A is equipped with a built-in connection detecting circuit. Connection detecting circuit is a circuit to detect the connected state of the cables and is effective while the port is not outputting TpBias.



### 7.3.4 Suspend/Resume

There are two operations for the port state to transit from Active to Suspend state.

When receiving TX SUSPEND that was output by Suspend Initiator (RX SUSPEND)

The port (the Suspend Target) that received the RX SUSPEND enters the Suspend state. The node also outputs TX SUSPEND into Active ports other than the port that received RX SUSPEND, and the port is set as the Suspend Initiator. The Suspend Initiator port then also enters the Suspend state.

TX SUSPEND is transmitted until the position of this leaf node to set at the Suspend state. However, if the IEEE1394-1995 node, the Disabled port and the Suspend port are present on its way, TX SUSPEND will be transmitted to stop at their positions. Even when the port is set at Suspend state, the Fault bit is set to indicate that the Suspend state is not set normally when the Bias of the connection partner node was detected.

The conditions under which the port of the Suspend state starts the Resume operation to enter the Active state are as follows.

- The Bias of the connection partner node is detected and the Fault bit is cleared.
- The Resume packet is received.
- The Remote Command packet, which the Resume bits for the port were set to, is received.

If the Boundary node is not set, the other Suspended ports except this node will also start Resume operation simultaneously when the ports in the Suspend or Disconnected state start Resume operation with the Bias detected (other than Resume packet and Remote Command packet).

The Resume operation outputs TPBIAS, and it is terminated normally when the Bias of the connection partner node is detected. It then enters the Active state. However, it returns to the Suspended state to set the Fault bit, indicating that Resume operation was terminated normally if the Bias from the connection partner node cannot be detected.

When receiving the Resume Command packet which the Suspend bit for its own port was set to

The Remote Command packet is transferred two ways, from nodes other than its own node, and from the Link layer controller IC, which correspondent to the upper level layer of its own node. Either way, the Remote Confirmation packet is transferred to all ports and the PHY/LINK interface when the S1R72900F00A receives the Remote Command packet. Bus reset is then issued to all ports other than the port (Suspend Initiator) that the Suspend bit is set to, and the node enters the reset state. Simultaneously, the port which the Suspend bit is set to outputs TX SUSPEND and it then enters the Suspend state.

### 7.3.5 Processing Unused Ports

If there are ports to be not used out of two SiR72009F00A cable ports, the pin should be processed as shown Figure 7-12.

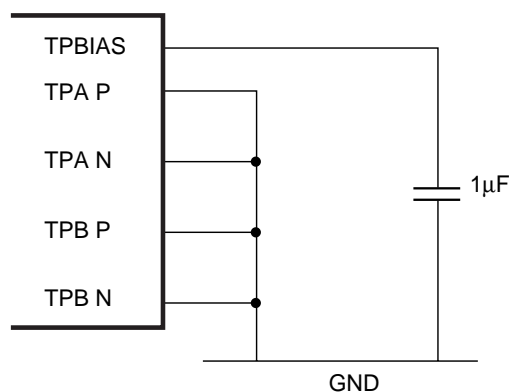


Figure 7.12 Processing Unused Ports

## 7.4 Link Layer Controller Interface

### 7.4.1 Connection

The S1R72900F00A can connect to a Link layer controller IC regardless of the existence of an isolation barrier. For DC connection, connect the DIRECT pin to VDD as shown in Figure 7.13.

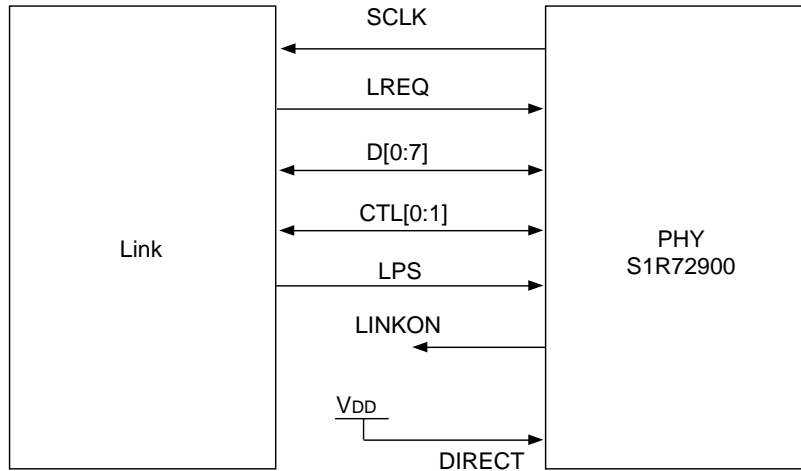


Figure 7.13 SIR72900F00A -to-Link chip connection diagram (DC connection)

The S1R72900F00A has a bus holder circuit on the interface pin for the Link layer controller IC. This enables AC connection as shown in Figure 7.14.

For AC connection (with a single capacitor), also connect the DIRECT pin to VDD.

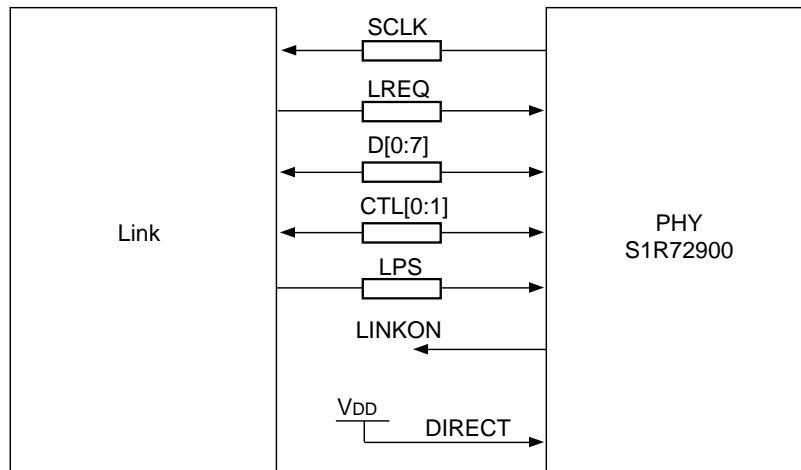


Figure 7.14 SIR72900F00A -to-Link chip connection diagram (AC connection)

As shown in Figure 7.15, use a 1000-pF coupling capacitor for AC connection.

\* The S1R72900F00A is not in support of the IEEE1394 specification Annex J isolation barrier.

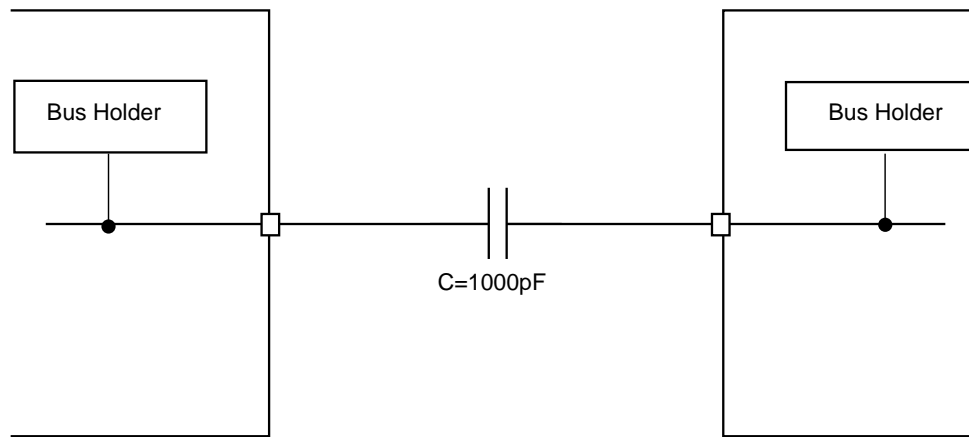


Figure 7.15 AC coupling connection

**7.4.2 LPS (Link Power Status)**

By inputting to the LPS pin, the S1R72900F00A is set to enable/disable the PHY/LINK interface. If the S1R72900F00A detects LPS = LOW during a TLPS RESET period, the PHY/LINK interface is set to the disable state to output LOW to the SCLK, CTL0-1 and D0-7. (While LOW is set when the PHY/LINK interface is DC connection, "Hi-Z" is set when it is AC connection.)

However, if Page select7 Register 70 bit 6 was set, SCLK is not terminated and continues to output a clock signal even when the PHY/LINK interface is set to disable.

If the PHY/LINK interface was reset, all bus requests and register read requests are cancelled. Also, the S1R72900F00A recognizes that the packet transfer was terminated and operates, if the Link layer controller IC reset the PHY/LINK interface during packet transfer.

When the PHY/LINK interface is set to disable period, the status output is not operated, therefore, this information is not output even after the PHY/LINK interface is set to enabled.

When the S1R72900F00A detects LPS = HIGH after the PHY/LINK interface was reset and set to disable, SCLK output starts after the disable state.

If the PHY/LINK interface uses the DC connection, the S1R72900F00A outputs LOW to the 7 SCLK cycles CTL, D after detecting LPS, and outputs Receive (CTL[0:1] = 10b, D[0.7]=ffh) for Data Prefix to the PHY/LINK interface at the 8th SCLK, returning to normal operation.

For AC connection, the S1R72900F00A outputs LOW to the 1SCLK cycle period CTL,D within 1 to 6 SCLK cycles after detecting LPS, returning to normal operation. Other periods will become "Hi-Z".

In this case, it continues to output Receive for Data Prefix to the PHY/LINK interface until packet receiving is terminated if its node is receiving a packet.

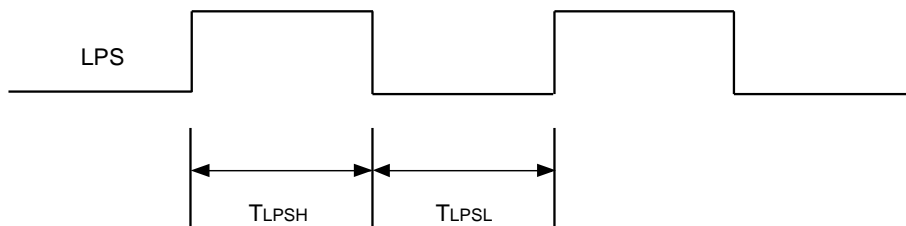


Figure 7.16 LPS waveforms in AC connection

Table 7.5 LPS timing

| Symbol       | Item  | Min. | Max. | Unit |
|--------------|---|------|------|------|
| TLPSL        | LPS low time (pulses)   | 0.09 | 1.0  | μm   |
| TLPSH        | LPS high time (pulses)  | 0.09 | 1.0  | μm   |
| TLPS_RESET   | The time required until the SIR72900F00A detects LPS = 0 and resets the PHY/LINK interface.   | 1.2  | 2.75 | μm   |
| TLPS_DISABLE | The time required until the SIR72900F00A detects LPS = 0 and disables the PHY/LINK interface. | 25   | 30   | μm   |

The S1R72900F00A issues short bus reset (SBR) against other nodes connected when detecting LPS = "1". This function makes cancellation possible by clearing Page select7 Register 70 bit 7. A typical external circuit for the LPS pin is shown in Figures 7.17, 18 and 19.

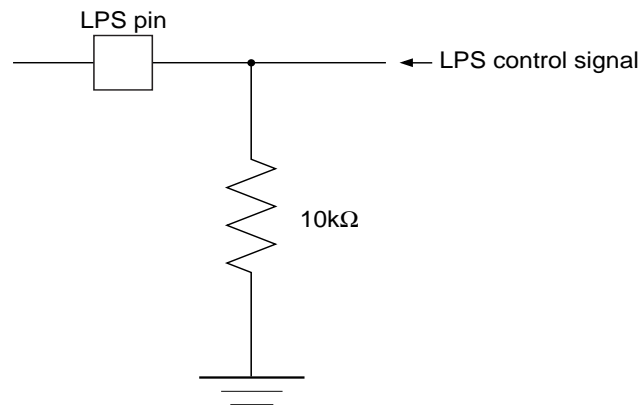


Figure 7.17 A typical direct connection and LPS external circuit 1 (with external signal control)

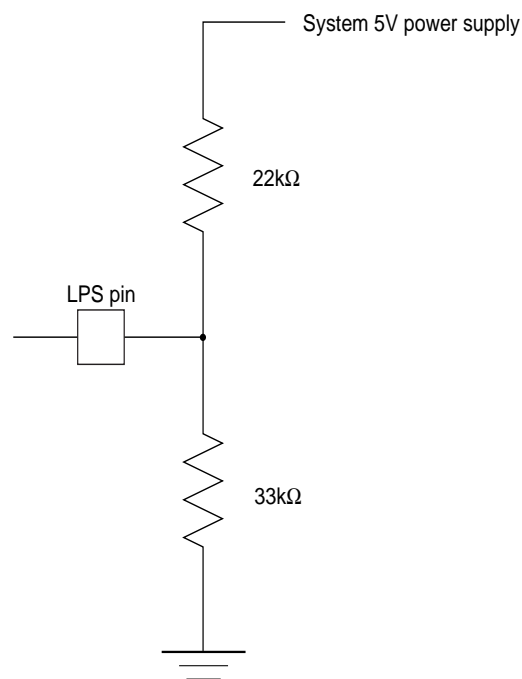


Figure 7.18 A typical direct connection and LPS external circuit 2 (without external signal control)

\* The LPS control signal shown Figure 7.17 is required to be 0.8 V lower when the power supply on the upper layer compared to the Link layer is set to OFF. For example, if the LPS control signal is output from the Link layer controller IC, LPS output is required to be GND output when the Link layer controller IC power supply is set to OFF. (For V<sub>DD</sub> output, LPS = "0" may not be recognized because the V<sub>DD</sub> potential may not become 0.8V lower.) Also, even when the system's power supply is connected to the LPS pin as shown in Figure 7.18, it is required to be 0.8V lower when the power supply on the upper layer compared to the Link layer is set to OFF. When using a 3.3V power supply for the Link layer controller IC, pay attention to the LPS connection because the V<sub>DD</sub> potential may not become 0.8V lower when the power supply is set to OFF.

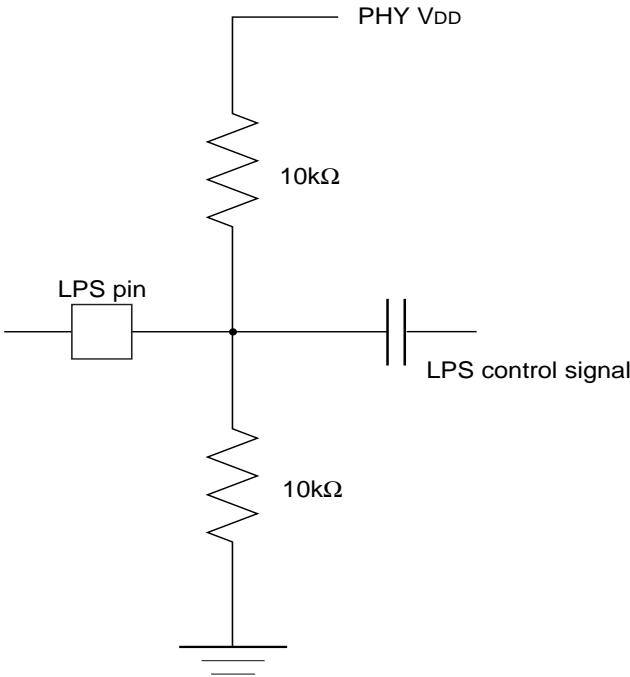


Figure 7.19 A typical AC connection and LPS external circuit

### 7.4.3 LinkOn

The SIR72900F00A recognizes that the Link layer controller IC is inactive when it recognizes that LPS is deasserted or the Link\_Active bit of the PHY register is '0.'

LinkOn normally outputs LOW. However, the SIR72900F00A outputs a LinkOn signal when it receives a LinkOn packet sent to the node while it recognizes that the Link layer controller IC is inactive.

If the Loop, Pwr\_fail, Timeout, or Port\_event bit of the PHY register changes to '1' during this period, the IC outputs a LinkOn signal as an interrupt output.

The LinkOn signal is output as long as the Link layer controller IC is inactive. When the Link layer controller IC becomes active, LOW is output as a LinkOn signal.

LinkOn signals are AC signals with a frequency of 6.144 MHz and a duty of 50%.

### 7.4.4 Link interface (LREQ, CTL[0:1], D[0:7])

The PHY/LINK interface of the SIR72900F00A complies with the IEEE 1394a-2000 standards.

The PHY/LINK interface operates in four ways, LREQ-triggered request and CTL-triggered status transmission, packet transmission, and packet reception. The CTL-triggered operation is first controlled by the PHY.

Upon receiving a packet, the SIR72900F00A starts packet reception operation.

Figures 7.6 and 7.7 show CTL statuses and their meanings.

Table 7.6 Operation in which the SIR72900F00A controls CTL

| CTL[0:1] | Operation | Description  |
|----------|-----------|--|
| 00b      | Idle      | Idle status. The CTL is doing no operation. (Default mode)                           |
| 01b      | Status    | Transmits status information.  |
| 10b      | Receive   | Transmits the received packet.   |
| 11b      | Grant     | Grants the Link the right to control the PHY/LINK interface for packet transmission. |

After the above Grant operation when the Link layer controller IC is able to control the PHY/LINK bus, the Link interface enters the operation mode as shown in Table 7.7.

Table 7.7 Operation in which the Link layer controller IC controls CTL

| CTL[0:1] | Operation | Description  |
|----------|-----------|--|
| 00b      | Idle      | Completes the packet transmission and frees the PHY/LINK interface.  |
| 01b      | Hold      | <ul style="list-style-type: none"> <li>· Holds the PHY/LINK interface until the data on the packet to be transmitted is determined.</li> <li>· Requests concatenated packet transmission.</li> </ul> |
| 10b      | Transmit  | Transmits data on the transmitted packet to the PHY.   |
| 11b      | Reserved  | Reserved.  |

7.4.4.1 LREQ

To request packet transmission, access to the PHY register, or acceleration control, the Link layer controller IC inputs a serial signal synchronized with SCLK to the LREQ pin.

The serial signal contains information on the request type, speed of the packet to be transmitted, and read/write command.

The length of the LREQ serial signal varies depending on the type of the request. It is 6 bits for acceleration control requests, 7 bits for bus requests, 9 bits for register read requests, and 17 bits for register write requests.

The serial signal must contain '0' as a stop bit at the end.

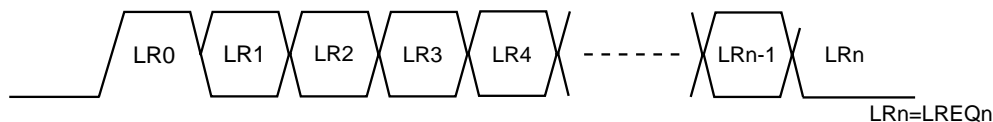


Figure 7.20 LREQ stream

A packet transmission request uses the 7-bit-long format as shown in Table 7.8.

Table 7.8 Request format

| Bit(s) | Typ.          | Description  |
|--------|---------------|--|
| 0      | Start Bit     | Represents the start of transmission. Always '1'.      |
| 1 to 3 | Request Type  | Represents the request type as shown in Figure 7.13.   |
| 4 to 5 | Request Speed | Represents the packet transmission speed.              |
| 6      | Stop Bit      | Represents the completion of transmission. Always '0'. |

Table 7.9 Speed format

| LREQ[4:5] | Data Rate |
|-----------|-----------|
| 00        | 100Mbps   |
| 01        | 200Mbps   |
| 10        | 400Mbps   |
| 11        | Reserved  |

A read PHY chip register request uses the 9-bit-long format as shown in Table 7.10. A write register request uses the 17-bit-long format as shown in Table 7.11.

Table 7.10 Read register format

| Bit(s) | Typ.         | Description   |
|--------|--------------|---|
| 0      | Start Bit    | Represents the start of transmission. Always '1'.             |
| 1 to 3 | Request Type | Represents the request type as shown in Figure 7.13.          |
| 4 to7  | Address      | Represents the address of the PHY register to be transmitted. |
| 8      | Stop Bit     | Represents the completion of transmission. Always '0'.        |



Table 7.11 Write register format

| Bit(s)  | Typ.         | Description  |
|---------|--------------|--|
| 0       | Start Bit    | Represents the start of transmission. Always '1'.                    |
| 1 to 3  | Request Type | Represents the request type as shown in Figure 7.13.                 |
| 4 to 7  | Address      | Represents the address of the PHY register to which data is written. |
| 8 to 15 | Data         | Represents the PHY register data to be written.                      |
| 16      | Stop         | Represents the completion of transmission. Always '0'.               |

An acceleration control request uses the 6-bit-long format as shown in Table 7.12.

Table 7.12 Acceleration control format

| Bit(s) | Typ.         | Description   |
|--------|--------------|---|
| 0      | Start Bit    | Represents the start of transmission. Always '1'.   |
| 1 to 3 | Request Type | Represents the request type as shown in Figure 7.13.  |
| 4      | Accelerate   | When this bit is '0,' arbitration acceleration can be disabled.<br>When this bit is '1,' arbitration acceleration can be enabled. |
| 5      | Stop Bit     | Represents the completion of transmission. Always '0'.  |

Table 7.13 Request type

| LREQ[1:3] | Typ.     | Description   |
|-----------|----------|---|
| 000       | ImmReq   | Immediate request   |
| 001       | IsoReq   | Isochronous request   |
| 010       | PriReq   | Priority request  |
| 011       | FairReq  | Fair request  |
| 100       | RdReg    | Read data from the configured register                            |
| 101       | WrReg    | Write data in the configured register                             |
| 110       | AccCtrl  | Represents that PHY arbitration acceleration is disabled/enabled. |
| 111       | Reserved | Reserved  |

With FairReq and PriReq, the Link layer controller IC must start issuing LREQ after at least 1 SCLK after CTL starts the Idle operation. When CTL starts the Receive operation during or after the Link layer controller IC's issuance of these requests, the SIR72900F00A cancels them. Therefore, the Link layer controller IC must issue these requests again next time CTL starts the Idle operation.

However, when the Enab\_accel bit of PHY Register 5 is set to '1,' acceleration arbitration (Ack-Acceleration arbitration and Fly-by arbitration) is enabled, and an Ack packet (8-bit-long packet) is to be received, these requests are not canceled if the Receive operation starts.

The cycle master Link layer controller IC issues PriReq to transmit a cycle start packet.

The Link layer controller IC issues IsoReq to transmit an isochronous packet. IsoReq must be issued during or within eight SCLK cycles of transmission of a cycle start packet or an isochronous packet, or during or within four SCLK cycles of reception of such packets.

The SIR72900F00A clears IsoReq only when it wins arbitration and transmits Grant to the Link layer controller IC, it detects a subaction gap, or when a bus request occurs.

To transmit an Ack packet, ImmReq is issued during or within four SCLK cycles of reception of a Link packet. To satisfy ACK\_RESPONSE\_TIME, the Link layer controller IC must issue ImmReq immediately as it confirms the destination\_ID of the received packet to check that the packet is sent to the node. As soon as the SIR72900F00A receives the packet, it acquires a bus, and the Link layer controller IC returns Grant. If the Link layer controller IC detects a CRC error, it must cancel the request rather than send data in response to the Grant. (See 7.4.4.3 Transmit.)

As soon as the reception of a register write request completes, the SIR72900F00A changes the data at the address. On receiving a register read request, the SIR72900F00A outputs the data at the address to the Link layer controller IC as a status transmission. If the output is interrupted by packet reception/transmission, the SIR72900F00A repeats the status output from the first bit until the output completes.

When the SIR72900F00A receives a bus request (FairReq, PriReq, IsoReq or ImmReq), it ignores the next bus request until the preceding request is canceled by packet reception, packet transmission, or subaction gap (for IsoReq and ImmReq only).

When the SIR72900F00A receives the next register read request before the preceding register read request completes, the operation becomes indefinite.

Any bus request is cleared by a bus reset.

The SIR72900F00A automatically sets an Accelerating bit with IsoReq, enabling acceleration arbitration.

**7.4.4.2 Status output**

The SIR72900F00A outputs information shown in Table 7.14 as a status output to the PHY/LINK interface. The SIR72900F00A asserts '01b' to the CTL pin and outputs information to the D[0:1] pin. The CTL pin outputs '01b' while the status output continues.

The SIR72900F00A usually outputs the first four bits (Arbitration Reset Gap, Subaction Gap, Bus Reset, and PHY interrupt) necessary for the Link state machine as a status output.

However, when it receives a register read request from the Link layer controller IC, it outputs all status information as a return value. In addition, when the SIR72900F00A has sent its Self-ID packet during the Self-ID period (when its Physical\_ID has been determined), it automatically outputs the PHY register information on address '00h' containing its Physical\_ID to the Link layer controller IC.

Status output may be interrupted by packet reception/transmission. When the status output is interrupted, the SIR72900F00A repeats the status output according to the following rules.

- The information that has been output before the interrupt is cleared and status output is not repeated.
- Status output starts with the S[0:1] bit and is done in the units of 4 bits/16 bits.

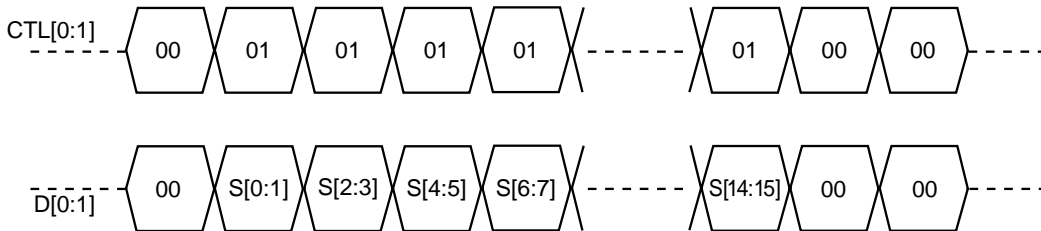


Figure 7.21 Status

Table 7.14 Status format

| Bit(s)  | Typ.                  | Description  |
|---------|-----------------------|--|
| 0       | Arbitration Reset Gap | Detects an Arbitration Reset Gap.                    |
| 1       | Subaction Gap         | Detects a Subaction Gap.                             |
| 2       | Bus Reset             | Detects a Bus Reset.                                 |
| 3       | PHY Interrupt         | Requests the host for an interrupt.                  |
| 4 to 7  | Address               | PHY register address to which the status is returned |
| 8 to 15 | Data                  | Status data  |

The SIR72900F00A outputs a status as PHY Interrupt in the following cases.

- When it detects that the bus is looped.
- When it detects that the cable voltage has dropped.
- When the state machine of the SIR72900F00A has timed out.
- When the Port\_event bit has changed to '1'.

### 7.4.4.3 Transmit

On receiving a bus request from the Link layer controller IC, the SIR72900F00A performs arbitration. When the SIR72900F00A wins the arbitration, it returns Grant ('11b') for one SCLK cycle and Idle for another SCLK cycle as Grant to the CTL pin of the Link layer controller IC

Then the Link layer controller IC inputs Transmit ('10b') or Hold ('01b') to CTL and controls the PHY/LINK interface. However, to prevent data conflict on the CTL bus, the SIR72900F00A permits the Link layer controller IC to input Idle ('00b') for 1SCLK before inputting Transmit or Hold. (See Figure 7.22.)

The Link layer controller IC can input Hold ('01b') to CTL to reserve the bus until the data to be transmitted is prepared, but the hold time must not exceed the MAX\_HOLD time. Then it inputs Transmit ('10b') to CTL to show the valid range of the transmitted data.

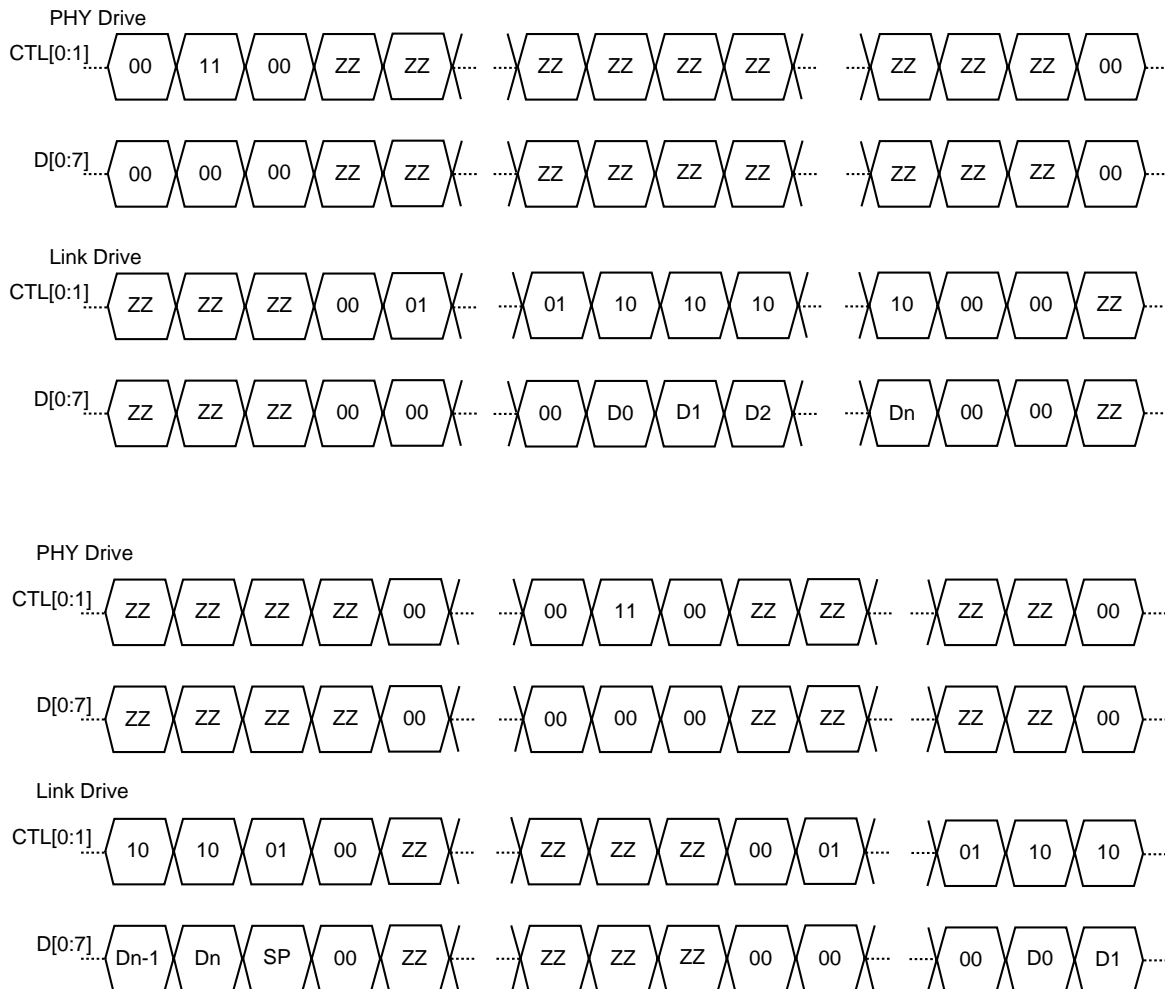


Figure 7.22 Transmit

Having input the final bit of the packet data, the Link layer controller IC inputs Idle ('00b') or Hold ('01b') for one SCLK cycle and Idle for another SCLK cycle. Then the SIR72900F00A takes over the control of the PHY/LINK interface. This Hold ('01b') bit ensures that the Link layer controller IC transmits the next packet without giving up the serial bus (concatenated packet). On detecting a Hold bit, the SIR72900F00A outputs Transmit again to the CTL pin of the Link layer controller IC after the MIN\_PACKET\_SEPARATION time. The Link layer controller IC then transmits packets. The Hold operation is used to transmit a response packet after an Ack packet or to transmit multiple isochronous packets within the same isochronous cycle (subaction concatenation).

In transmitting a Concatenated packet, the SIR72900F00A determines the Concatenated packet transmission speed according to the Enab\_multi bit of PHY Register 5. When the Enab\_multi bit is set to '0,' the SIR72900F00A recognizes that the transmission speed for the second and later packets is the same as that for the first packet.

On the other hand, when the Enab\_multi bit is set to '1,' the SIR72900F00A recognizes the transmission speed for the Concatenated packet according to the SP value input to D while Hold ('01b') is being input to CTL. Table 7.12 shows the meaning of the SP value.

However, the IEEE 1394 standards defines a transmission speed limit for Concatenated packets, prohibiting the transmission of a Concatenated packet at a speed of S100 after packet transmission at S200 or higher.

To observe the speed limit, when the SIR72900F00A receives a request for 100-Mbps Concatenated packet transmission following a request for packet transmission at 200 Mbps or higher, it gives up the 1394 bus and performs arbitration in an attempt to transmit the 100-Mbps packet as a Single packet. Therefore, this 100-Mbps Concatenated packet transmission request from the Link layer controller IC will be handled as a bus request that occurs in ordinary LREQ, which may cause the IC to return CTL other than Grant (the request may be canceled).

Packet transmission can be cancelled in the following two ways.

After the Link layer controller IC takes control of the PHY/LINK interface, input Idle ('00b') for three SCLK cycles to give up the interface. Or, after the Link layer controller IC inputs Hold ('01b') to hold the bus, input Idle for two SCLK cycles to give up the interface.

Empty packets are output to the serial bus.

#### 7.4.4.4 Receive

On receiving a packet, the SIR72900F00A outputs Receive ('10b') to the CTL pin, and 'H' to the D pin of the Link layer controller IC. Then the SIR72900F00A outputs a speed code (SP) to start packet data output. The SIR72900F00A continues to assert Receive ('10b') to the CTL terminal until the data reception completes. Then the SIR72900F00A asserts Idle ('00b') to declare that the packet reception has completed.

As Receive operation, the SIR72900F00A outputs to the Link interface the Self-ID packets it transmits during the Self-ID period.

Also as Receive operation, the SIR72900F00A outputs to the Link interface, the response packets to the Extended PHY packet sent to the node.

Once asserting Receive, the SIR72900F00A may terminate reception operation without outputting packet data.

If the Link layer controller IC supports a transmission speed of 100 Mbps only, it must confirm the speed code (SP) to make sure that packet data received at 200 or 400 Mbps is ignored.

If the Link layer controller IC supports transmission speeds of 100 and 200 Mbps only, it must confirm the speed code (SP) to make sure that packet data received at 400 Mbps is ignored.

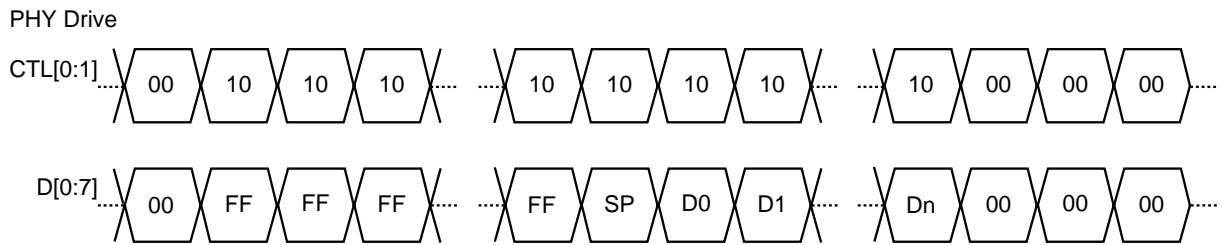


Figure 7.23 Receive

Table 7.15 Speed code (SP[0:7])

| D[0:7]    | Data Rate |
|-----------|-----------|
| 00xxxxxb  | 100Mbps   |
| 0100xxxxb | 200Mbps   |
| 01010000b | 400Mbps   |

## 7.5 Oscillating Circuit

The SIR72900F00A carries a built-in crystal oscillation circuit. The output frequency of the external quartz oscillator should be 24.576MHz ( 80ppm (including the temperature characteristics).

As the quartz oscillator, we recommend our MA-406 (24.576MHz., CL = 10pF) to secure the necessary frequency precision.

Position the quartz oscillator and capacitor in the neighborhood of this IC and maintain the wiring pattern as short as possible.

Fig. 7.24 shows an example of external connection when using the MA-406.

\* The SIR72900F00A does not support external oscillator inputs.

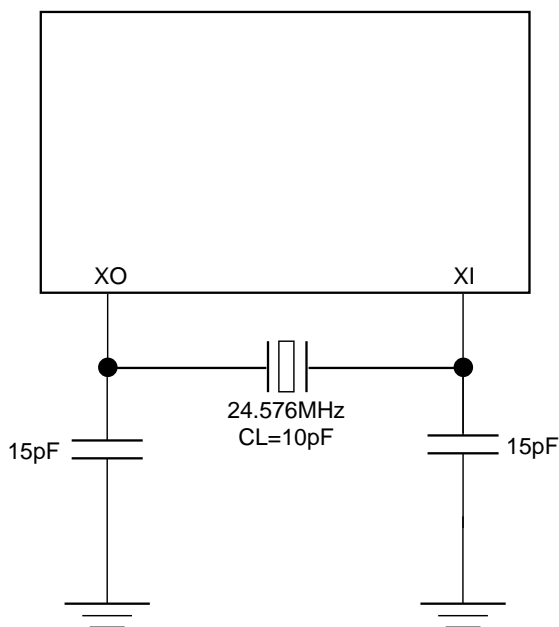


Figure 7.24 Connection of external oscillating circuit

## 7.6 Power Down

The SIR72900F00A carries the power down mode. The power down mode can be obtained by inputting "1" into the PD pin and under the power down mode, all the internal functions will stop. The power down mode can be cancelled by changing the input to the PD pin from "1" to "0" and, a few ms (the time required for initialization) after the PD pin input became "0", normal operation will be restored.

## 8. ELECTRICAL CHARACTERISTICS

### 8.1 Absolute Maximum Ratings

Table 8.1 Absolute maximum ratings

(V<sub>SS</sub>=0V)

| Item               | Symbol           | Rating                       | Unit |
|--------------------|------------------|------------------------------|------|
| Operating voltage  | V <sub>DD</sub>  | -0.3 to 4.0                  | V    |
| Input voltage      | V <sub>IN</sub>  | -0.3 to V <sub>DD</sub> +0.5 | V    |
| Output voltage     | V <sub>OUT</sub> | -0.3 to V <sub>DD</sub> +0.5 | V    |
| Output current/pin | I <sub>OUT</sub> | ±30                          | mA   |
| Storage temperatur | T <sub>STG</sub> | -65 to 150                   | °C   |

### 8.2 Recommended Operating Conditions

Table 8.2 Recommended operating conditions

| Item                  | Symbol          | Min.            | Typ. | Max.            | Unit |
|-----------------------|-----------------|-----------------|------|-----------------|------|
| Operating voltage     | V <sub>DD</sub> | 3.00            | 3.30 | 3.60            | V    |
| Input voltage         | V <sub>IN</sub> | V <sub>SS</sub> | -    | V <sub>DD</sub> | V    |
| Operating temperature | T <sub>a</sub>  | 0               | -    | 70              | °C   |

## 8.3 DC Characteristics

(AVDD, PVDD, OCSVDD, VDD=3.3V±0.3V, Ta=0 to 70°C)

| Item  | Symbol             | Condition  | Min. | Typ. | Max. | Unit |
|---|--------------------|--|------|------|------|------|
| Power supply current (S400 packet transmission together with port 0.1)                  |                    |  |      |      |      |      |
| Supply current  | I <sub>DD</sub>    | AVDD=3.6V<br>PVDD=3.6V<br>OSCVDD=3.6V<br>VDD=3.6V  |      |      | 137  | mA   |
| Static current  |                    |  |      |      |      |      |
| Supply current  | I <sub>DDSA</sub>  | V <sub>IN</sub> =AVDD or PVDD<br>or OSCVDD or VDD<br>or VSS<br>AVDD=4.0V<br>PVDD=4.0V<br>OSCVDD=4.0V<br>VDD=4.0V                 |      |      | 5.5  | μA   |
| Input leak Pin name: LREQ,CTL0,CTL1,D0 to 7,PD,LPS,BCLKON,XDIRECT,CPS,TPA*,TPB*,XRST,XI |                    |  |      |      |      |      |
| Input leak current  | I <sub>L</sub>     | AVDD=3.6V<br>PVDD=3.6V<br>VDD=3.6V<br>V <sub>IH</sub> =AVDD, PVDD,<br>OSCVDD, VDD<br>V <sub>IL</sub> =AVDD, PVDD,<br>OSCVDD, VDD | -1   |      | 1    | μA   |
| Input characteristics (CMOS) Pin name: PD,PS1 to 3,XTEST_MODE,TEST0,TEST1               |                    |  |      |      |      |      |
| High level input voltage  | V <sub>IH</sub>    | VDD=3.6V   | 1.9  |      |      | V    |
| Low level input voltage   | V <sub>IL</sub>    | VDD=3.0V   |      |      | 0.9  | V    |
| Schmidt input characteristics 1 Pin name: XRST  |                    |  |      |      |      |      |
| High level trigger voltage  | V <sub>T1+</sub>   | VDD=3.6V   | 1.2  |      | 2.3  | V    |
| Low level trigger voltage   | V <sub>T1-</sub>   | VDD=3.0V   | 0.7  |      | 1.7  | V    |
| Schmidt input characteristics 2 Pin name: LREQ,CTL0,CTL1,D0 to 7,LPS                    |                    |  |      |      |      |      |
| High level trigger voltage  | V <sub>T2+</sub>   | VDD=3.6V   | 2.1  |      | 2.7  | V    |
| Low level trigger voltage   | V <sub>T2-</sub>   | VDD=3.0V   | 0.6  |      | 1.2  | V    |
| CPS input characteristics Pin name: CPS   |                    |  |      |      |      |      |
| High level trigger voltage  | V <sub>TCPS+</sub> | VDD=3.6V   | 1.36 |      | 2.0  | V    |
| High level trigger voltage  | V <sub>TCPS-</sub> | VDD=3.0V   | 1.16 |      | 1.68 | V    |
| Input pull up characteristics Pin name: XRST  |                    |  |      |      |      |      |
| Pull up resistor  | R <sub>PLU2</sub>  | VDD=3.0V<br>V <sub>IL</sub> =VSS   | 16.8 |      | 46.4 | μA   |

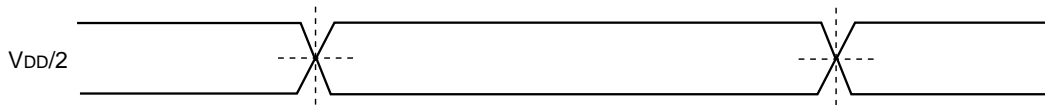


| Item   | Symbol            | Condition   | Min.                 | Typ. | Max.                 | Unit |
|--|-------------------|---|----------------------|------|----------------------|------|
| Output characteristics 1 Pin name: BNC                             |                   |   |                      |      |                      |      |
| High level output voltage  | V <sub>OH1</sub>  | V <sub>DD</sub> =3.0V<br>I <sub>OH</sub> =-2mA  | V <sub>DD</sub> -0.4 |      |                      | V    |
| Low level output voltage   | V <sub>OL1</sub>  | V <sub>DD</sub> =3.0V<br>I <sub>OL</sub> =2mA   |                      |      | 0.4                  | V    |
| Output characteristics 2 Pin name: BCLKON, SCLK, CTL0,CTL1, D0 to7 |                   |   |                      |      |                      |      |
| High level output voltage  | V <sub>OH2</sub>  | V <sub>DD</sub> =3.0V<br>I <sub>OH</sub> =-6mA  | V <sub>DD</sub> -0.4 |      |                      | V    |
| Low level output voltage   | V <sub>OL2</sub>  | V <sub>DD</sub> =3.0V<br>I <sub>OL</sub> =6mA   |                      |      | 0.4                  | V    |
| Output characteristics 3 Pin name: SCLK,R1,TPBIAS1,TPBIAS2,FC1     |                   |   |                      |      |                      |      |
| Off-state leak current   | I <sub>OZ</sub>   | V <sub>DD</sub> =3.6V<br>V <sub>OH</sub> =V <sub>DD</sub><br>V <sub>OL</sub> =V <sub>SS</sub> | -1                   |      | 1                    | μA   |
| Bus hold characteristics Pin name: LREQ,CTL0,CTL1, D0 to 7,LPS,    |                   |   |                      |      |                      |      |
| High level hold current  | I <sub>BHH</sub>  | V <sub>DD</sub> =3.0V<br>V <sub>IN</sub> =2.6V  | -0.3                 |      |                      | mA   |
| Low level hold current   | I <sub>BHL</sub>  | V <sub>DD</sub> =3.0V<br>V <sub>IN</sub> =0.4   |                      |      | 0.3                  | mA   |
| High level drive current   | I <sub>BHHO</sub> | V <sub>DD</sub> =3.6V<br>I <sub>I</sub> L=-0.9mA  |                      |      | V <sub>SS</sub> +0.4 | V    |
| Low level drive current  | I <sub>BHLO</sub> | V <sub>DD</sub> =3.6V<br>I <sub>I</sub> L=0.9mA   | V <sub>DD</sub> -0.4 |      |                      | V    |

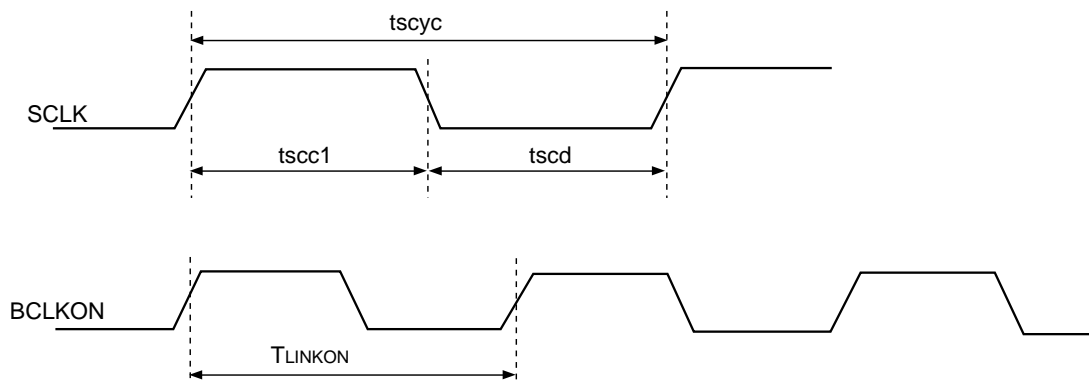
| Item                                    | Symbol | Condition                             | Min.    | Typ. | Max.    | Unit |
|---|--------|---------------------------------------|---------|------|---------|------|
| Cable interface                         |        |                                       |         |      |         |      |
| Common mode input voltage               | Vic    | TPB cable input power supply node     | 1.03    |      | 2.015   | V    |
| Common mode input voltage               | Vic    | TPB cable input non-power supply node | 0.523   |      | 2.515   |      |
| Common mode output voltage              | Voc    |                                       | 1.665   | 1.85 | 2.015   | V    |
| Common mode output current              | Iocs1  | S100                                  | -0.81   |      | 0.44    | mA   |
| Common mode output current              | Iocs2  | S200                                  | -4.84   |      | -2.53   | mA   |
| Common mode output current              | Iocs4  | S400                                  | -12.4   |      | -8.1    | mA   |
| Differential input voltage amplitude    |        |                                       | 118     |      | 265     | mV   |
| Differential output voltage amplitude   |        |                                       | 172     |      | 265     | mV   |
| Arb comparator threshold voltage (+)    |        |                                       | 89      |      | 168     | mV   |
| Arb comparator threshold voltage (-)    |        |                                       | -168    |      | -89     | mV   |
| S200 speed signal threshold voltage     |        |                                       | Voc-273 |      | Voc-138 | mV   |
| S400 speed signal threshold voltage     |        |                                       | Voc-701 |      | Voc-441 | mV   |
| BIAS detection threshold voltage        |        |                                       | 0.6     |      | 1       | V    |
| Connection detection threshold voltage  |        |                                       | 0.6     |      | 1       | V    |
| Cable power detection threshold voltage |        |                                       | 5.9     |      | 9.4     | V    |

## 8.4 AC Characteristics

### 8.4.1 DC judgment level

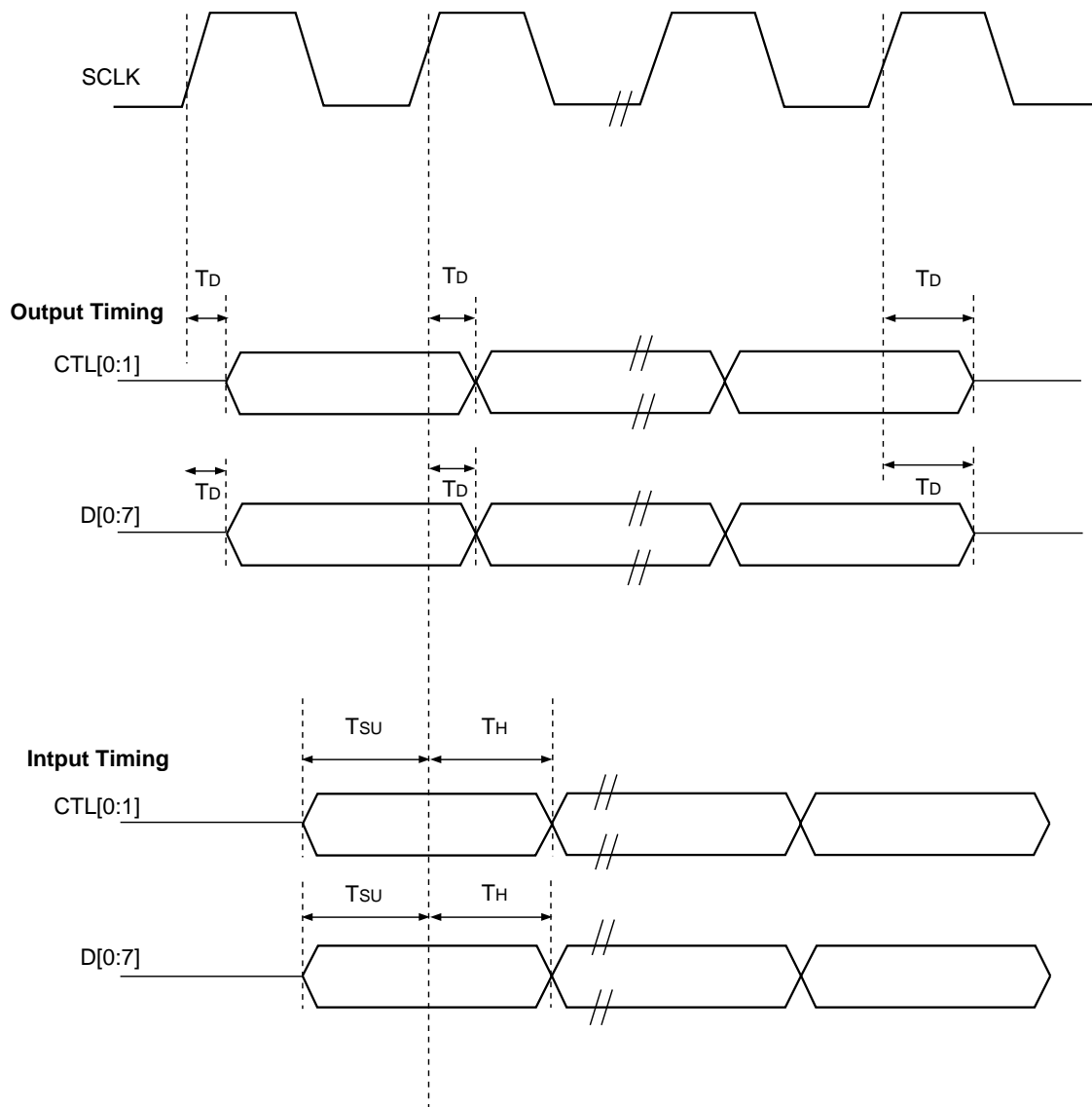


### 8.4.2 Clock timing



| Symbol       |                      | Min.   | Typ.   | Max.   | Unit |
|--------------|----------------------|--------|--------|--------|------|
| $t_{scyc}$   | SCLK cycle           | 20.343 | 20.345 | 20.346 | ns   |
| $t_{sccl}$   | SCLKHIGH pulse width | 9.16   |        | 11.18  | ns   |
| $t_{scd}$    | SCLK LOW pulse width | 9.16   |        | 11.18  | ns   |
| $T_{LINKON}$ | BCLKON cycle         | 125    |        | 250    | ns   |

8.4.3 PHY/LINK interface timing

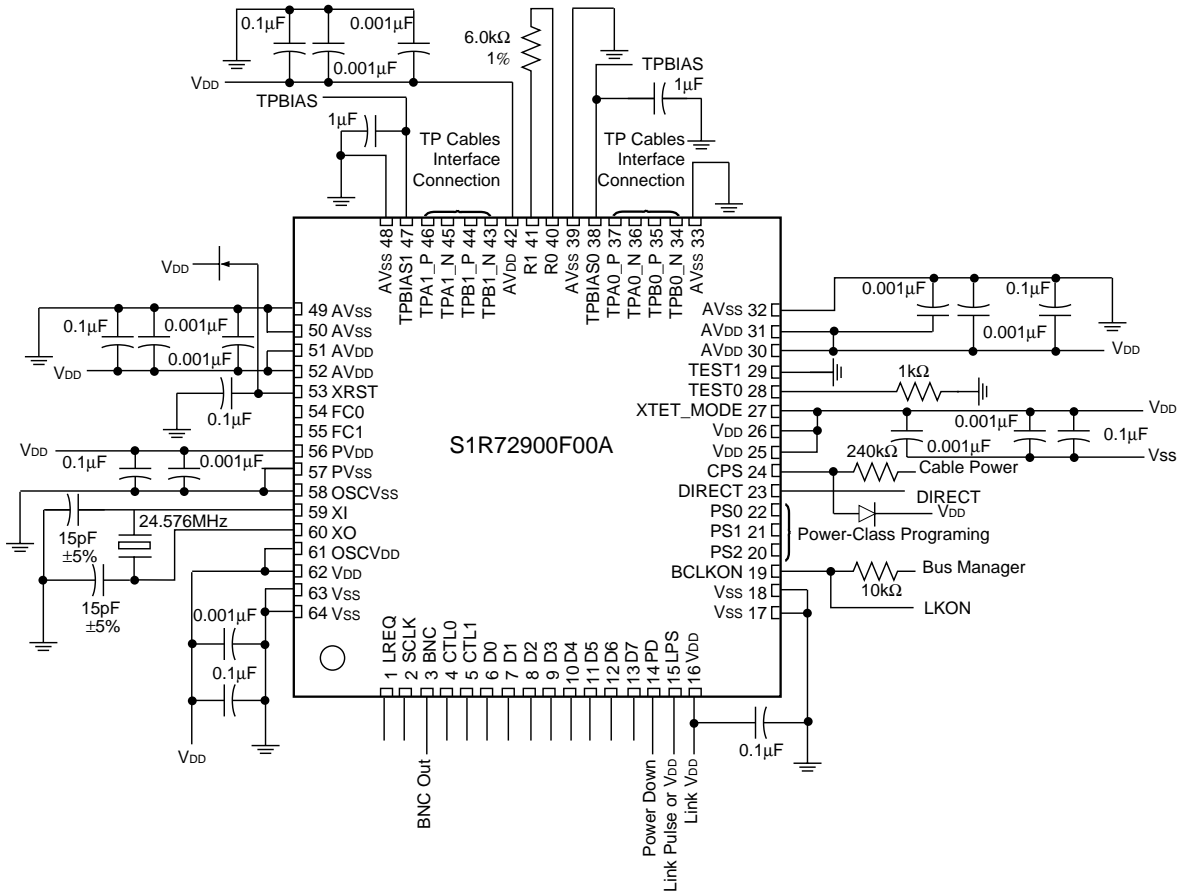


| Symbol   |                         | Min. | Typ. | Max. | Unit |
|----------|-------------------------|------|------|------|------|
| $T_D$    | CTL. D delay time       | 0.5  | 1.9  | 13.5 | ns   |
| $T_{SU}$ | CTL. D. LREQ setup time | 7    | 18   |      | ns   |
| $T_H$    | CTL. D. LREQ hold time  | 0    | 1.3  |      | ns   |

8.4.4 Cable interface timing

| Symbol        |   | Min. | Typ. | Max. | Unit |
|---------------|---|------|------|------|------|
| $T_{TJITTER}$ | $T_{pA}, T_{pB}$ transmission jitter    | -150 |      | 150  | ps   |
| $T_{TSKEW}$   | $T_{pA}/T_{pB}$ transmission skew       | -100 |      | 100  | ps   |
| $T_{TRF}$     | $T_{pA}/T_{pB}$ rise time and fall time | 0.5  |      | 1.2  | ns   |

### 9. EXAMPLE OF EXTERNAL CONNECTION





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