

MC33293A

Advance Information Quad Low Side Switch

The MC33293A is a single monolithic integrated circuit designed for quad low side switching applications. This device was initially conceived as a quad injector driver for use in the harsh automotive environment but is well suited for many other applications. The MC33293A incorporates SMARTMOS™ technology having CMOS logic, bipolar and CMOS analog circuitry and DMOS power MOSFETs. All of the device inputs are CMOS compatible. The four output devices are N-channel power MOSFETs. A Fault detect output is provided to flag the existence of open loads (outputs ON or OFF) or shorted loads. If a short circuit is detected, the fault detect circuitry turns off the shorted output, but allows the others to function normally. An overvoltage (V_{PWR}) condition will turn off all outputs for the overvoltage duration. Each output functions independently and has a drain-to-gate diode clamp for inductive flyback voltage protection. A Single/Dual select pin is incorporated to allow either individual output control or control of a pair of outputs from one input.

The MC33293A is parametrically specified over $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ ambient temperature and a $9.0\text{ V} \leq V_{PWR} \leq 14.5\text{ V}$ supply.

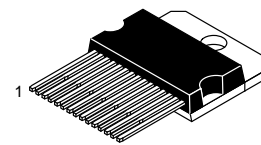
- Designed to Operate with Supply Voltages of 5.5 V to 30 V
- CMOS Compatible Inputs with Active Pull-Downs
- Maximum 5.0 mA Quiescent Current
- $R_{DS(on)}$ of 0.25 Ω Maximum at 25°C, with $V_{PWR} \geq 9.0\text{ V}$
- Each Output Clamped to 65 V for Driving Inductive Loads
- Each Output Current Limited at 3.0 A to handle Incandescent Lamp Loads
- Active Low Output Fault Status with Interrogation Capability
- Open Load Detection (Output ON or OFF)
- Capable of Withstanding Reverse Battery
- Overvoltage Shutdown
- Short Circuit Detection and Shutdown with Automatic Retry

ORDERING INFORMATION

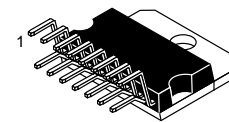
Device	Operating Temperature Range	Package
MC33293AT	$T_J = -40^{\circ}$ to $+150^{\circ}\text{C}$	15 Pin SIP
MC33293ATV		

QUAD LOW SIDE SWITCH ($R_{DS(on)} = 0.25\ \Omega$ Max per Output)

SEMICONDUCTOR TECHNICAL DATA



T SUFFIX
PLASTIC PACKAGE
CASE 821D



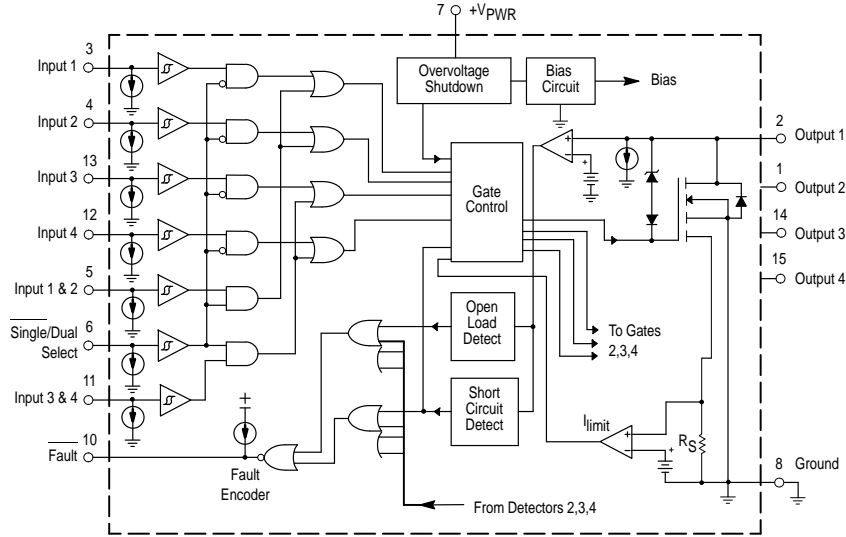
TV SUFFIX
PLASTIC PACKAGE
CASE 821C

PIN CONNECTIONS

- Pin 1. Output 2
 2. Output 1
 3. Input 1
 4. Input 2
 5. Input 1 & 2
 6. Single/Dual
 7. V_{PWR}
 8. Gnd
 9. N/C
 10. Fault
 11. Input 3 & 4
 12. Input 4
 13. Input 3
 14. Output 3
 15. Output 4

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Simplified Block Diagram



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Steady-State Transient Conditions	V_{PWR} $V_{PWR(pk)}$	-13 to 30 -13 to 60	V
Input Pin Voltage	V_{in}	-0.5 to 7.5	V
ESD Capability Human Body Model ($R = 1.5\text{ k}\Omega$, $C = 200\text{ pf}$)	V_{ESD}	2000	V
Lead Current (per Output)	I_{Out}	Internally Limited	A
Single Pulse Clamp Energy @ 25°C, 1.5 A	E_{clamp}	100	mJ
Storage Temperature	T_{stg}	-55 to +150	°C
Operating Temperature	T_J	-40 to +150	°C
Lead Temperature (Wave Solder, 10 s)	T_{solder}	260	°C
Power Dissipation @ $T_A = 105^\circ\text{C}$ Power Dissipation @ $T_A = 125^\circ\text{C}$ Derate for every °C above 25°C	P_D	11.25 6.25 0.25	W W/°C
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	35	°C/W
Thermal Resistance Junction-to-Case. Any one O/P	$R_{\theta JC}$	4.0	°C/W

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STATIC ELECTRICAL CHARACTERISTICS ($9.0\text{ V} \leq V_{PWR} \leq 14.5\text{ V}$ and $-40^\circ\text{C} \leq T_C \leq +125^\circ\text{C}$, unless otherwise noted. Typical values are at 25°C , unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT					
Turn ON Threshold	$V_{on(th)}$	—	3.4	5.5	V
Operating Voltage Range	V_{PWR}	5.5	—	30	V
Quiescent Power Supply Current (All Inputs off)	I_{PWR}	—	2.2	5.0	mA
Overshoot Shutdown Range	$V_{PWR(ov)}$	30	35	38	V
Overshoot Reset Hysteresis	$V_{PWR(hys)}$	2.0	5.0	7.0	V
Input Voltage					V
High ($I_{DS} = 1.0\text{ A}$)	V_{IH}	3.0	2.3	—	
Low ($I_{DS} = 80\ \mu\text{A}$)	V_{IL}	—	1.6	0.8	
Input High Hysteresis ($I_{DS} = 1.0\text{ A}$)	$V_{IH(hys)}$	0.4	0.7	—	V
Input Current					μA
High ($V_{IH} = 3.0\text{ V}$)	I_{IH}	—	11	50	
Low ($V_{IL} = 0.8\text{ V}$)	I_{IL}	—	11	50	
OUTPUT					
Static Drain-Source On-Resistance ($I_{DS} = 1.0\text{ A}$, $V_{PWR} = 13\text{ V}$, $T_C = -40^\circ\text{C}$ to $+25^\circ\text{C}$) ($I_{DS} = 1.0\text{ A}$, $V_{PWR} = 13\text{ V}$, $T_C = +125^\circ\text{C}$) ($I_{DS} = 0.7\text{ A}$, $V_{PWR} = 8.0\text{ V}$, $T_C = +25^\circ\text{C}$) ($I_{DS} = 0.4\text{ A}$, $V_{PWR} = 5.5\text{ V}$, $T_C = +25^\circ\text{C}$)	$R_{DS(on)}$	—	0.18	0.25	Ω
		—	0.28	0.50	
		—	0.20	0.40	
		—	0.22	0.50	
Drain-Source Clamp Voltage ($I_{DS} = 20\text{ mA}$, $V_{in} = 0\text{ V}$, $t_{clamp} = 100\ \mu\text{s}$)	BV_{DSS}	55	64	80	V
Zero Input Voltage Drain Current ($V_{DS} = 25\text{ V}$, $V_{PWR} = 14.5\text{ V}$) ($V_{DS} = 58\text{ V}$, $V_{PWR} = 14.5\text{ V}$)	$I_{DS(off)}$	10	23	80	μA
		—	0.06	2.0	mA
Source Drain Diode Forward Voltage ($I_{SD} = 1.0\text{ A}$)	V_{SD}	—	0.62	1.4	V

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STATIC ELECTRICAL CHARACTERISTICS (continued) ($9.0\text{ V} \leq V_{PWR} \leq 14.5\text{ V}$ and $-40^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$, unless otherwise noted. Typical values are at 25°C , unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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FAULT STATUS OUTPUTT

Fault Status Pin					V
Low Voltage ($V_{PWR} = 14.5\text{ V}$, $I_{stl} = 1.0\text{ mA}$, open-load on Output 1, 2, 3 or 4. All inputs = 0 V)	V_{stl}	—	0.1	0.4	
High Voltage, ($V_{PWR} = 14.5\text{ V}$, $I_{sth} = -30\text{ }\mu\text{A}$, Note 1)	V_{sth}	3.0	4.7	5.5	

FAULT DETECTION

Output Limiting Current ($V_{PWR} = 13\text{ V}$)	$I_{DS(limit)}$	3.0	4.0	6.0	A
Over-Current Detect Voltage Threshold and Output-Off Open-Load Detect Threshold Voltage	$V_{OC(limit)}$ $V_{Ooff(th)}$	2.4	3.7	5.0	V
output-on open-load Detect Current ($V_{PWR} = 13\text{ V}$, $V_{in} = 5.0\text{ V}$, $T_C = -40^{\circ}\text{C}$) ($V_{PWR} = 13\text{ V}$, $V_{in} = 5.0\text{ V}$, $T_C = +25^{\circ}\text{C}$) ($V_{PWR} = 13\text{ V}$, $V_{in} = 5.0\text{ V}$, $T_C = +125^{\circ}\text{C}$)	$I_{Oon(th)}$	20 20 20	80 75 65	190 130 100	mA

DYNAMIC ELECTRIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
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OUTPUT TIMING

Output Driver Rise Time ($V_{CC} = 13\text{ V}$, $R_L = 13\text{ }\Omega$, t_r = Output Voltage change from 90% to 10%, see Figure 2)	t_r	—	2.3	10	μs
Output Driver Fall Time ($V_{CC} = 13\text{ V}$, $R_L = 13\text{ }\Omega$, t_f = Output Voltage change from 10% to 90%, see Figure 2)	t_f	—	1.5	10	μs
Output Delay Time ($V_{CC} = 13\text{ V}$, $R_L = 13\text{ }\Omega$, $t_{on(dly)} = V_{in}$ at 3.0 V to V_O at 90%, see Figure 2) $t_{off(dly)} = V_{in}$ at 1.0 V to V_O at 10%, see Figure 2)	$t_{on(dly)}$ $t_{off(dly)}$	— —	3.2 5.9	10 15	μs

FAULT TIMING

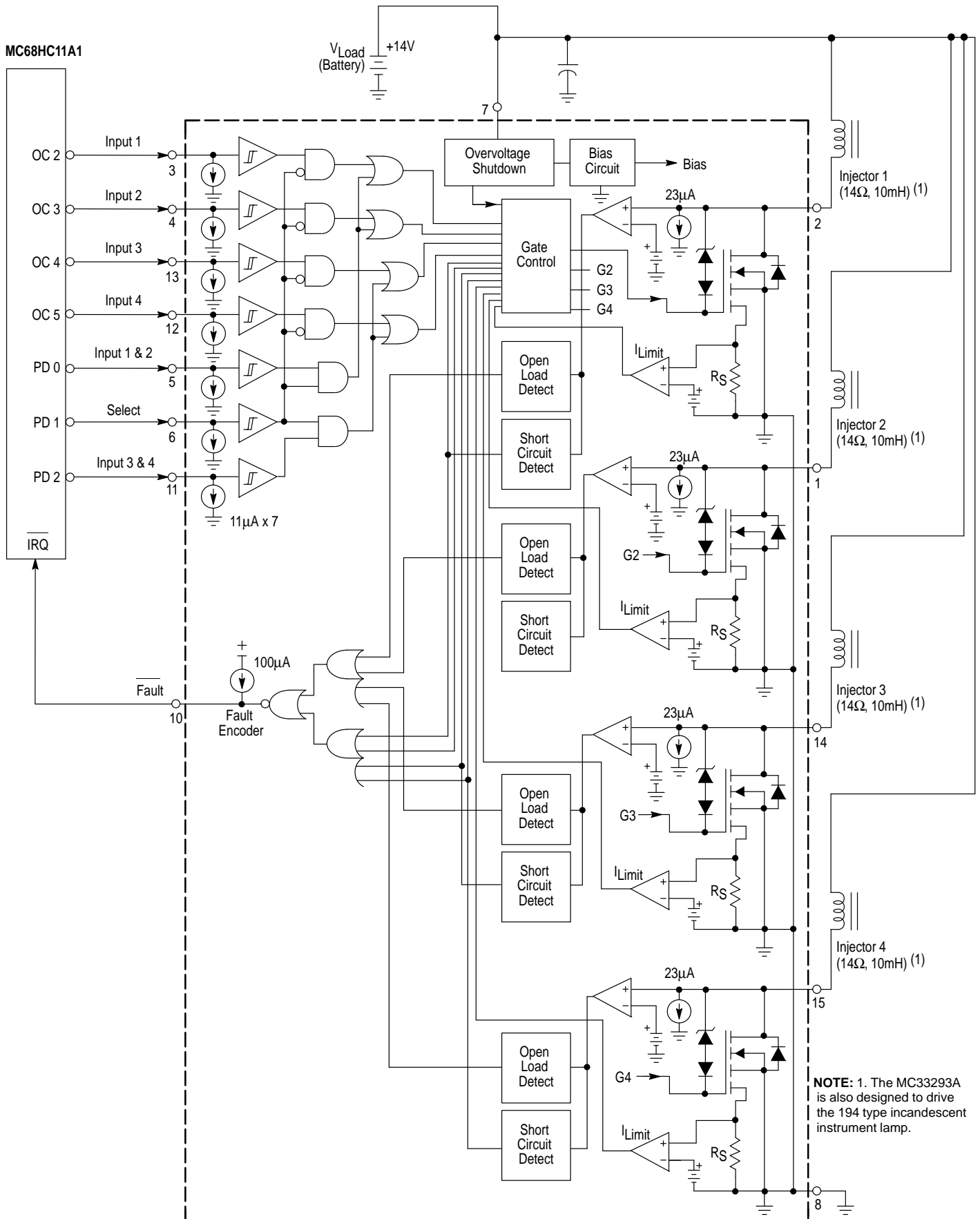
Over-Current Sense Time (See Figure 5 or 6) ($V_{in} = 5.0\text{ V}$, $R_L = 0.05\text{ }\Omega$, $V_{PWR} = 14.5\text{ V}$, over-current duty cycle $\leq 10\%$ t_{oc} = time that V_{Status} is $> 1.0\text{ V}$)	t_{oc}	10	55	250	μs
Over-Current Refresh Time (See Figures 5 or 6) ($V_{in} = 5.0\text{ V}$, $R_L = 0.05\text{ }\Omega$, $V_{PWR} = 14.5\text{ V}$, over-current duty cycle $\leq 10\%$ t_{ref} = time that V_{Status} is $< 1.0\text{ V}$)	t_{ref}	1.5	3.6	7.0	ms
Output Open-Load Fault Status Delay Time ($V_{PWR} = 13\text{ V}$, $V_{in} = 5.0\text{ V}$, open-load on Output, $t_{os(on)}$ = time from $V_{in} = 3.0\text{ V}$ to $V_{Status} = 1.0\text{ V}$, see Figure 3) ($V_{PWR} = 13\text{ V}$, $V_{in} = 0\text{ V}$, open-load on Output, $t_{os(off)}$ = time from $V_{in} = 2.5\text{ V}$ to $V_{Status} = 1.0\text{ V}$, see Figure 4)	$t_{os(on)}$ $t_{os(off)}$	1.0 1.0	2.2 19	4.0 40	ms μs
Fault Status Reset Delay Time ($V_{PWR} = 13\text{ V}$, $V_{in} = 0\text{ V}$, see Figure 4)	$t_s(reset)$	—	2.0	10	μs

NOTE: 1. Negative current signifies current flowing out of device.

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Figure 1. Fuel Injector Application Block Diagram



NOTE: 1. The MC33293A is also designed to drive the 194 type incandescent instrument lamp.

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Figure 2. Switching Speed Test Circuit and Response Times

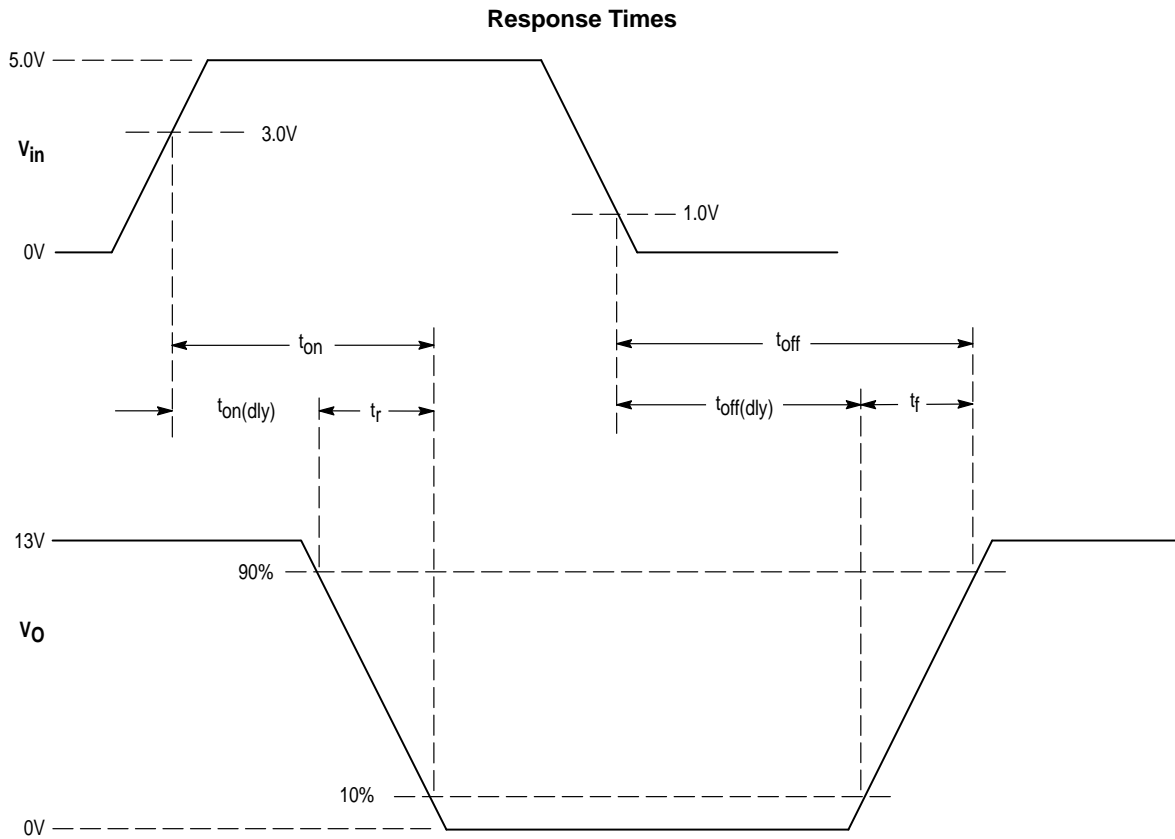
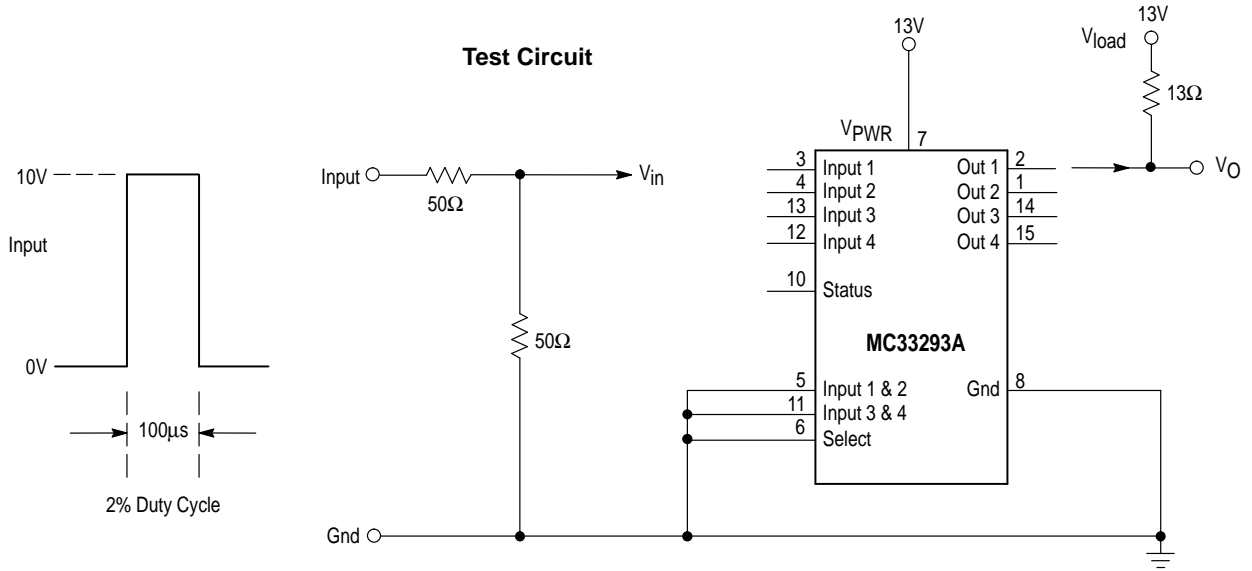
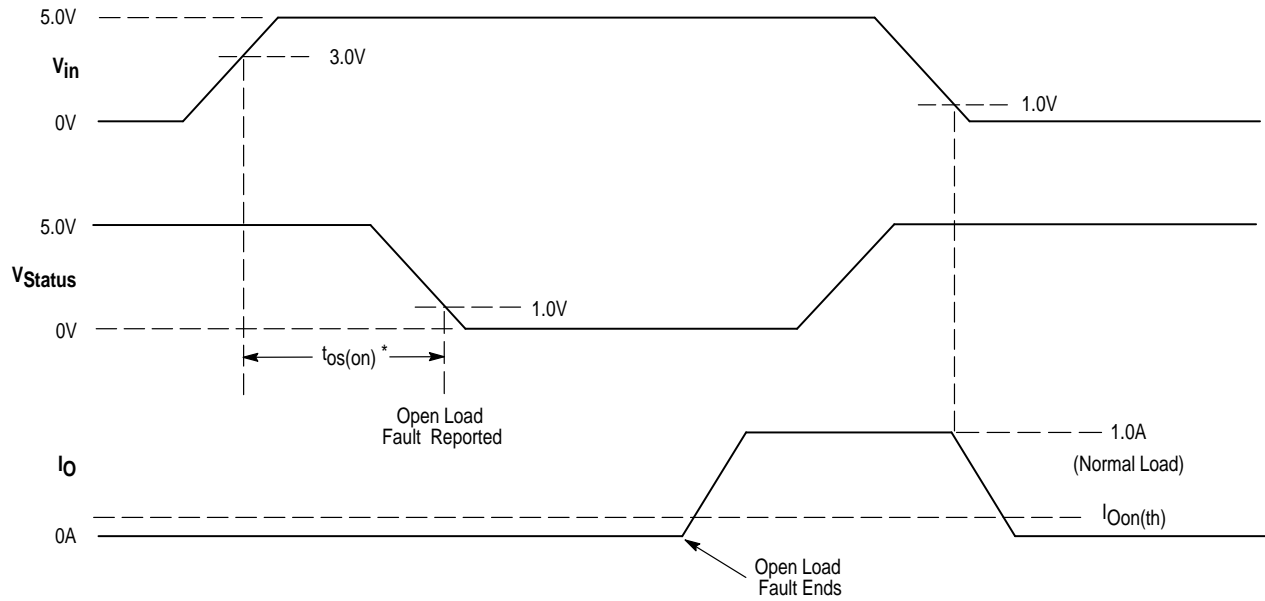


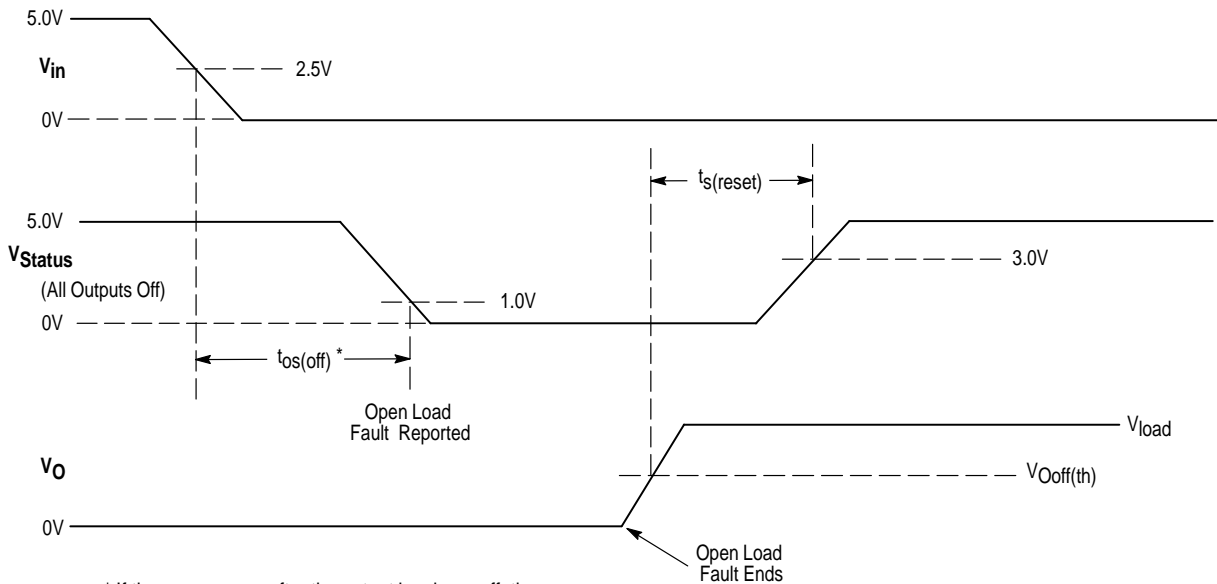
Figure 3. Fault Status Operation with an Output-On, Open-Load Fault



* If the open occurs after the output has been on, the delay time is much less than $t_{os(on)}$.

NOTE: Rise and fall times are exaggerated for emphasis.

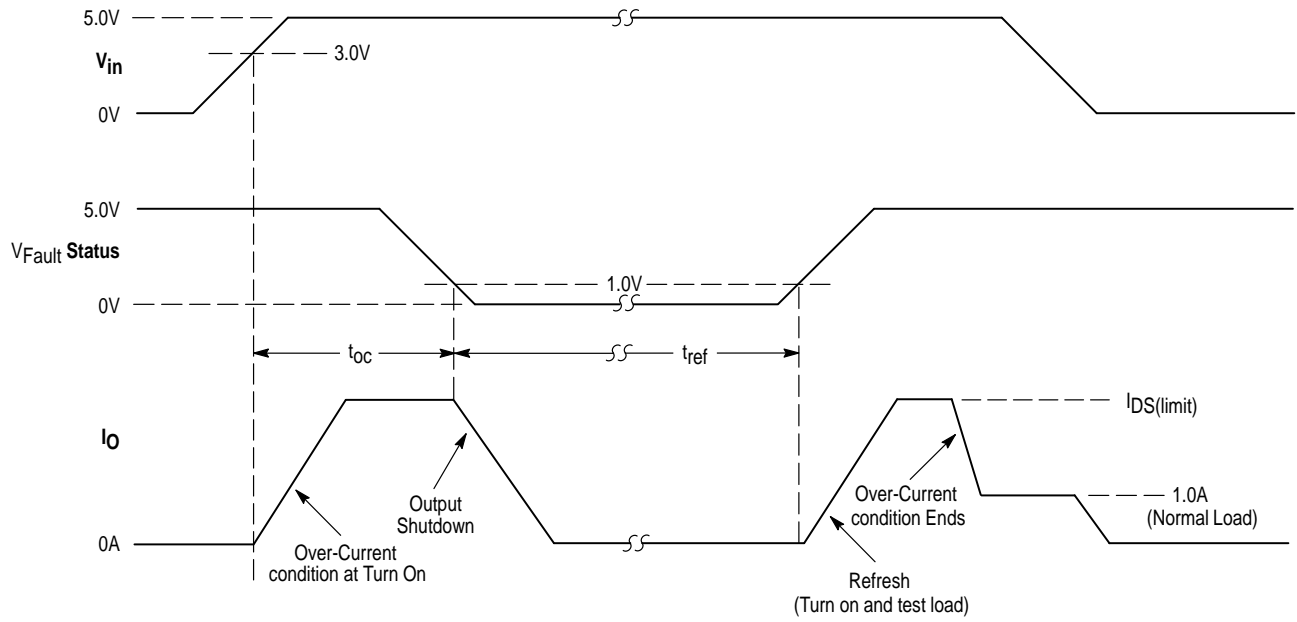
Figure 4. Fault Status Operation with an Output-Off, Open-Load Fault



* If the open occurs after the output has been off, the delay time is much less than $t_{os(off)}$.

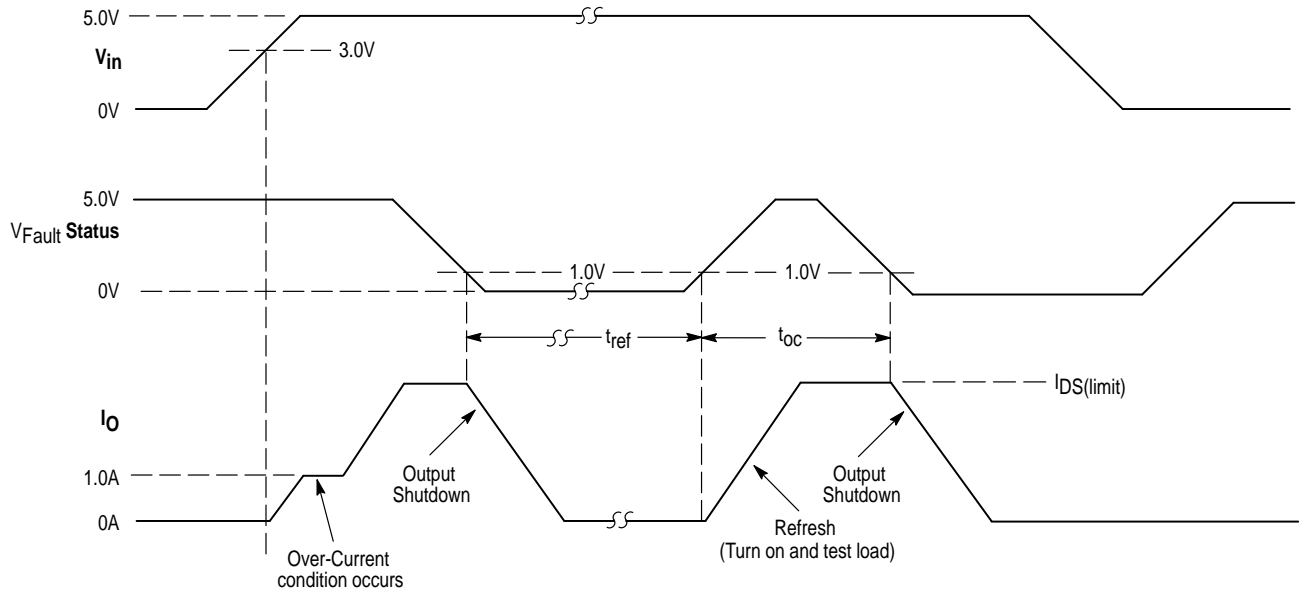
NOTE: Rise and fall times are exaggerated for emphasis.

Figure 5. Fault Status Operation with Turn On into an Over-Current Load



NOTE: Rise and fall times are exaggerated for emphasis.

Figure 6. Fault Status Operation with Over-Current Load after Turn On



NOTE: Rise and fall times are exaggerated for emphasis.

Figure 7. Turn On Threshold Voltage versus Temperature

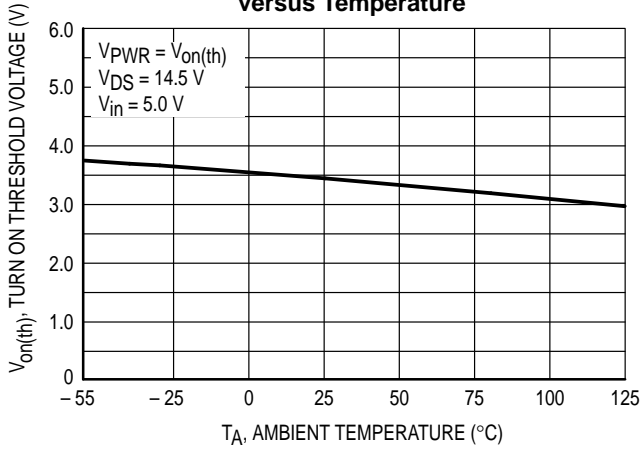


Figure 8. Output On Resistance versus Temperature

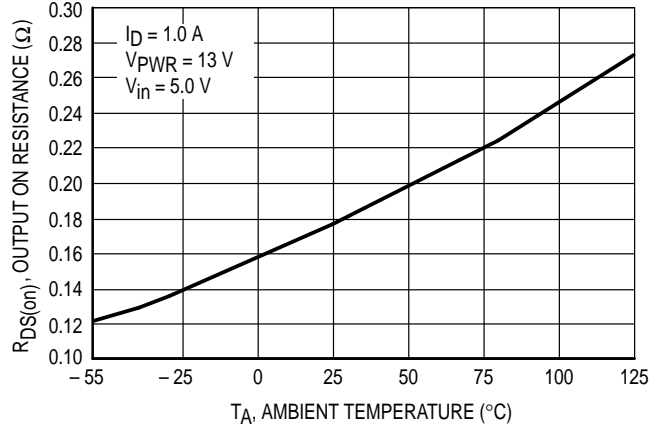


Figure 9. Drain Source Clamp Voltage versus Temperature

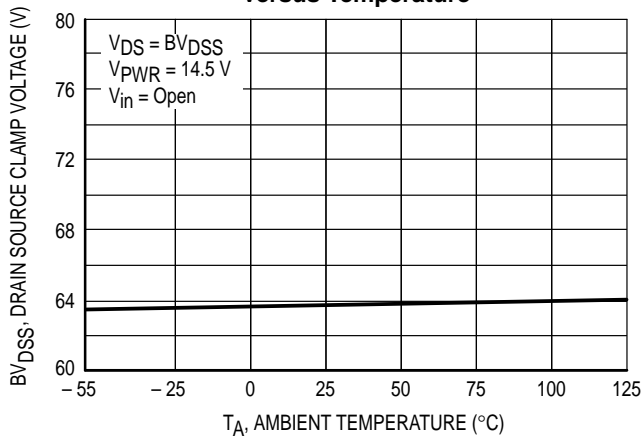


Figure 10. Zero Input Voltage Drain Current versus Temperature

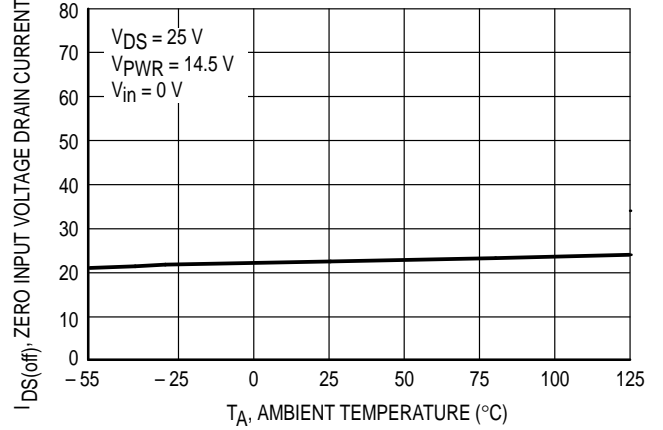


Figure 11. Current Limit versus Temperature

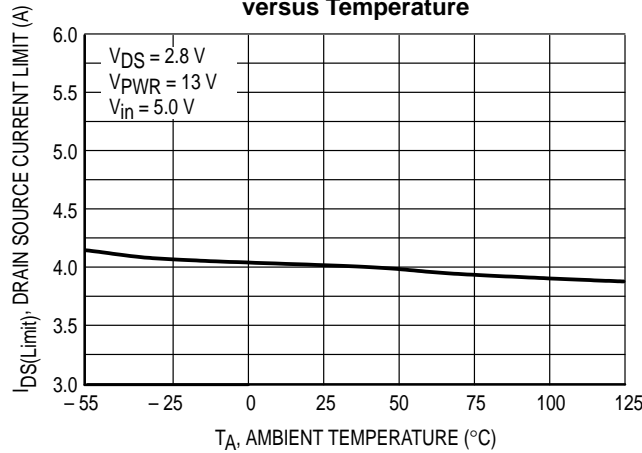
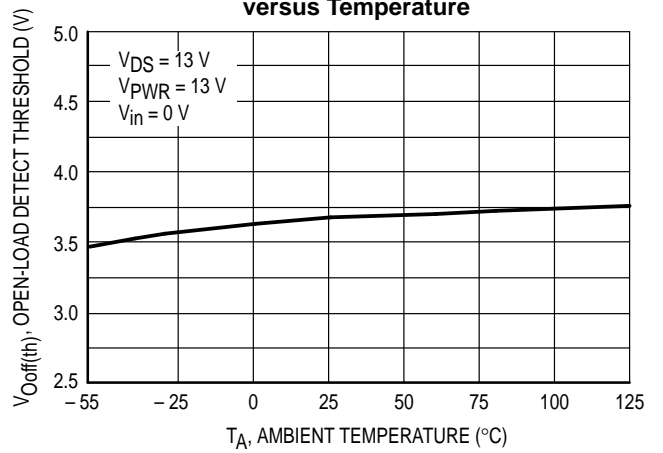


Figure 12. Open-Load Threshold versus Temperature



PIN DESCRIPTION

Pin	Function	Description
1	Output 2	This is one of four open drain power MOSFET output connections. The load is connected from this pin to the positive voltage supply.
2	Output 1	This is one of four open drain power MOSFET output connections. The load is connected from this pin to the positive voltage supply.
3	Input 1	This input controls the turn ON and turn OFF of Output 1 when the Single/Dual pin is at a logic low level. It is a CMOS input with an internal active pull-down employed for noise immunity.
4	Input 2	This input controls the turn ON and turn OFF of Output 2 when the Single/Dual pin is at a logic low level. It is a CMOS input with an internal active pull-down employed for noise immunity.
5	Input 1 & 2	This input controls the turn ON and turn OFF of Output 1 and Output 2 when the Single/Dual select pin is at a logic high level. It is a CMOS input with an internal active pull-down employed for noise immunity.
6	Single/Dual Select	This input selects between the single (one input controls one output) mode and the dual (one input controls two outputs) mode of operation.
7	V _{PWR}	The power (voltage and current) to operate the IC is supplied through this pin. The MC33293A is designed to operate over a voltage range of 5.5 V to 30 V.
8	Ground	IC ground reference pin.
9	N/C	No connection.
10	Fault	One of three fault conditions, Output-On Open-Load, Output-Off Open-Load or Over-Current are reported at this output. A logic low state signals the existence of a fault condition. This output has an internal active pull-up and does not require an external pull-up resistor.
11	Input 3 & 4	This input controls the turn ON and turn OFF of Output 3 and Output 4 when the Single/Dual select pin is at a logic high level. It is a CMOS input with an internal active pull-down employed for noise immunity.
12	Input 4	This input controls the turn ON and turn OFF of Output 4 when the Single/Dual pin is at a logic low level. It is a CMOS input with an internal active pull-down employed for noise immunity.
13	Input 3	This input controls the turn ON and turn OFF of Output 3 when the Single/Dual pin is at a logic low level. It is a CMOS input with an internal active pull-down employed for noise immunity.
14	Output 3	This is one of four open-drain power MOSFET output connections. The load is connected from this pin to the positive voltage supply.
15	Output 4	This is one of four open-drain power MOSFET output connections. The load is connected from this pin to the positive voltage supply.

CIRCUIT DESCRIPTION

Introduction

The MC33293A is a four output low side switch originally intended for use in automotive applications as a fuel injection driver. This circuit can be used in a variety of applications. It is parametrically specified over a battery voltage range of 9.0 V to 14.5 V, but is designed to operate over a considerably wider range of 5.5 V to 30 V. The design incorporates the use of logic level MOSFETs as output devices which are fully enhanced at a gate voltage of 5.0 V, eliminating the need for internal charge pumps. Each output is identically sized and is *independent* in operation. The efficiency of each output device is such that with as little as 9.0 V of V_{PWR} applied, the R_{DS(on)} is 0.18 Ω typically, at room temperature and increases to only 0.22 Ω as V_{PWR} decreases to 5.5 V.

All inputs of the MC33293A are CMOS and have individual 11 μA internal active pull-downs. This eliminates the need for external pull-down resistors to prevent false switching due to noise on the input control lines. This also ensures that at

power-up, no load is turned on before a logic high appears on an input pin. Fault reporting is through the use of an open-drain MOSFET having a 100 μA internal active pull-up.

All inputs incorporate *true logic* (or positive logic). This means that whenever an input is in a logic low state (< 0.8 V) the corresponding output will be in an OFF state. Conversely, whenever an input is in a logic high state (> 3.0 V), the corresponding output will be in an ON state.

Single/Dual Select

The Single/Dual Select pin can be used to switch between completely independent control and control of the outputs in pairs. Whenever the Single/Dual Select pin is in a logic low state, Inputs 1, 2, 3 and 4 control Outputs 1, 2, 3 and 4, respectively. In this mode, only Inputs 1, 2, 3 and 4 can exercise individual control over their respective output. Hence the term “single select” mode of operation. Input 1 & 2 (Pin 5) and Input 3 & 4 (Pin 11) have *no* control whenever the Single/Dual Select pin is in a logic low state.

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When the Single/Dual Select pin is held at a logic high state, Control Inputs 1, 2, 3 and 4 are turned OFF and can *not* exercise any control over the outputs. In this mode, input control transfers from a single to a dual mode of operation, wherein only Input 1 & 2 and Input 3 & 4 have control of Output 1 plus Output 2, and Output 3 plus Output 4, respectively. Hence the term "Dual Select" mode of operation.

Paralleling Outputs

Paralleling outputs may be desirable in the event the application requires a lower $R_{DS(on)}$ or higher current switching capability than a single output. The MC33293A can

be operated with all outputs (and therefore all inputs) tied together but modified operation is to be expected. With all inputs tied together and depending on the dual or single select mode used, the paralleled input control current will either be twice (with the dual mode selected) or four times (with the single mode selected) that of any single input. Other expected differences are: $R_{DS(on)}$ will decrease by a factor of four while the Output-On Open-Load Detect current and the Output Limiting current will increase by a factor of four. There will be no change in the Over-Voltage Shutdown Range or the Output-Off Output-On Open-Load Detect Threshold Voltage Range. As always, system level thermal design and verification are important when outputs are paralleled.

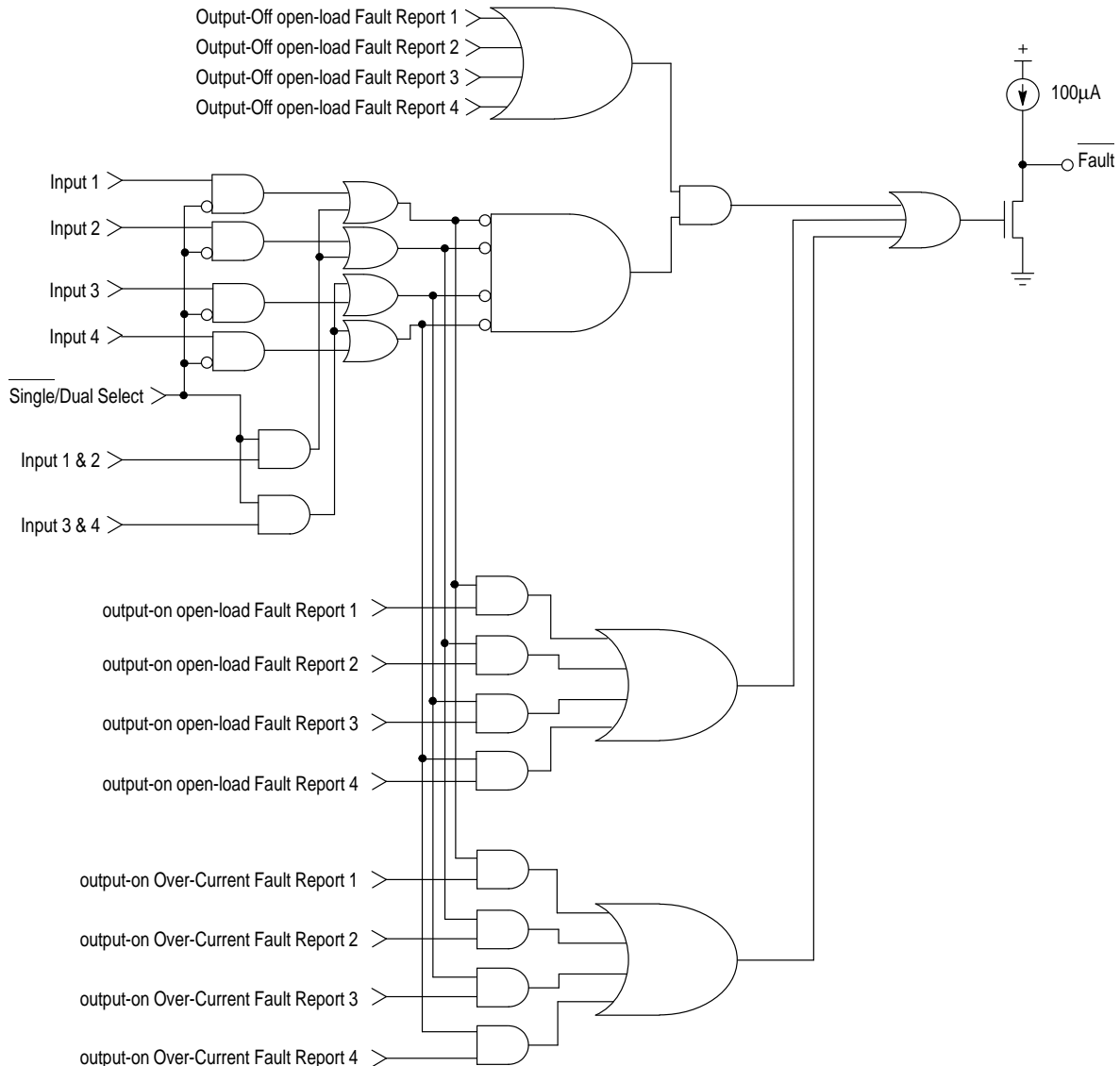
FAULT LOGIC OPERATION

General

The Fault Status output (Pin 10) on the MC33293A reports any one of three possible faults from any one of the four outputs. The three possible faults are output-on open-load

Fault, output-off open-load Fault and over-current Fault. All faults from any of the four outputs are OR'd together and reported by the single Fault Status output on Pin 10 (Figure 13).

Figure 13. MC33293A Fault Logic Diagram



Output-On open-load Fault

The MC33293A always checks for an open-load on the outputs whether the outputs are ON or OFF. An output-on open-load Fault is detected if an open-load exists when the output is ON (corresponding input at a logic high state). The output-on open-load Fault detection occurs when the load current is less than the minimum Output-On Open-Load Detect current ($I_{Oon(th)}$), specified in this data sheet. The value of $I_{Oon(th)}$ is, typically, 75 mA at room temperature. See Figure 3.

The minimum load resistance value that the MC33293A will interpret as an output-on open-load ($R_{open(on)}$) is a function of; the Output-On Open-Load Detect current ($I_{Oon(th)}$); the load supply voltage (V_{load}); and the resistance of the output ($R_{DS(on)}$), as shown below.

$$R_{open(on)} = \frac{V_{load} / I_{Oon(th)}}{R_{DS(on)}} - \frac{V_{load}}{I_{Oon(th)}} \quad (1)$$

Using Equation 1 for the steady state case,

$$\begin{aligned} \text{when: } V_{load} &= 14 \text{ V} \\ R_{DS(on)} &= 0.3 \Omega \\ I_{Oon(th)} &= 75 \text{ mA} \end{aligned}$$

an output-on open-load Fault will be detected and reported whenever $R_{load} \geq 187 \Omega$.

Each output has an output-on open-load fault detect circuit that performs real time load current monitoring. Load current is monitored immediately after any output is turned ON. Since it takes a finite amount of time for load current to begin, the MC33293A detects an output-on open-load Fault from the time the output is turned ON until the load current exceeds the Output-On Open-Load Detect current ($I_{Oon(th)}$). It is important to note that a fault will *not* be reported at the Fault Status output during this short period of time. This is due to the built-in output-on open-load Fault Status Delay Time ($t_{os(on)}$), see Figure 3. This delay time is incorporated in the MC33293A to mask the reporting of a false output-on open-load Fault at the Fault Status output. The delay is typically 2.2 ms.

The purpose for the $t_{os(on)}$ delay is to prevent false fault reporting, especially when driving inductive loads. The load inductance causes a current lag when the load is turned ON. The normal current lag of an inductive load could be misinterpreted as an open-load if it weren't for the built-in delay. This delay or masking is accomplished internally with a single timer which resets every time any input switches from a low-to-high logic state. An output-on open-load Fault will be reported by the Fault Status output as a result of turning ON an output having an open-load Fault and the most recent $t_{os(on)}$ is allowed to lapse after switching ON any input.

The time it takes the load current to reach $I_{Oon(th)}$ is a function of the load resistance (R_{load}); load inductance (L_{load}); output on resistance ($R_{DS(on)}$); load supply voltage (V_{load}); and the turn-on time (t_{on}) as shown below. The value of t_{on} is comprised of the low-to-high V_{in} propagation delay time ($t_{on(dly)}$), and the output voltage rise time (t_r). See Figure 2.

$$t_{on(\text{false fault})} = -\tau \ln \left[\frac{I_{Oon(th)} - I_{load}}{-I_{load}} \right] + t_{on} \quad (2)$$

$$\text{where: } \tau = L_{load} / R_{load} = \text{time constant} \quad (3)$$

$$I_{load} = V_{load} / [R_{load} + R_{DS(on)}] \quad (4)$$

$$t_{on} = t_{on(dly)} + t_r \quad (5)$$

Using Equation 2 for the transient case,

$$\begin{aligned} \text{when: } V_{load} &= 14 \text{ V} \\ R_{DS(on)} &= 0.3 \Omega \\ L_{load} &= 10 \text{ mH} \\ R_{load} &= 14 \Omega \\ I_{Oon(th)} &= 75 \text{ mA} \end{aligned}$$

an output-on open-load Fault will be detected, but not reported after initial turn ON for a duration of $57 \mu\text{s} + t_{on}$.

Output-Off open-load Fault

The MC33293A checks for open-loads on the outputs regardless of an output being on or off. An output-off open-load Fault is detected if an open-load exists when the output is turned OFF (corresponding input at a logic low state). When any one of the four outputs are turned OFF, an independent internal current source tied to each output tries to pull a small amount of zero input voltage drain current ($I_{DS(off)}$), typically 23 μA), through the load. If, while this zero input voltage drain current is being pulled through the load, the output voltage is less than the output-off open-load Detect Threshold Voltage ($V_{Ooff(th)}$), typically 3.7 V), an output-off open-load Fault will be detected.

The zero input voltage drain current could be provided by a large external resistor connected from the output to ground. However, if an external resistor were used to provide this zero input voltage drain current, only "opens" resulting from open-loads or output to ground shorts could be detected. The external resistor could *not* guarantee detection of an open resulting from an output wire bond failure internal to the MC33293A. Because the current source is provided internally, open loads, output to ground shorts, and loss of output wire bonds will all be detected.

The value of load resistance that will be detected as an output-off open-load ($R_{open(off)}$), is a function of the zero input voltage drain current ($I_{DS(off)}$); the load supply voltage (V_{load}); and the output-off open-load Detect Threshold Voltage ($V_{Ooff(th)}$), as shown next by:

$$R_{open(off)} = \frac{[V_{load} - V_{Ooff(th)}]}{I_{DS(off)}} \quad (6)$$

Using Equation 6 for the steady state case,

$$\begin{aligned} \text{when: } V_{load} &= 14 \text{ V} \\ I_{DS(off)} &= 23 \mu\text{A} \\ V_{Ooff(th)} &= 3.7 \text{ V} \end{aligned}$$

an output-off open-load Fault will be detected and reported whenever $R_L \geq 448 \text{ k}\Omega$.

Each output has an output-off open-load fault detect circuit that performs real time output voltage monitoring. Output voltage is monitored immediately after any output is turned off. A finite amount of time is required for output voltage to rise. The MC33293A detects an output-off open-load Fault from when an output is turned off until the output voltage exceeds the output-off open-load Detect Threshold Voltage ($V_{Ooff(th)}$). It is important to note a fault will *not* be reported at the Fault Status output during this rise time. This is due to the built-in output-off open-load Fault Status Delay Time, $t_{os(off)}$, see Figure 4. This delay time is incorporated in the MC33293A to delay the reporting of an output-off open-load Fault at the Fault Status Output. The delay is typically 19 μs .

The purpose for the $t_{OS(off)}$ delay is to prevent false fault reporting experienced with capacitance type loads. The load capacitance causes the rise in output voltage to lag even after the load has been turned OFF. The normal voltage lag caused by load capacitance could be misinterpreted as an open-load if it weren't for the built-in delay. This delay, or masking, is accomplished with four separate timers that reset independent of each other when the corresponding input is switched from a high to a low logic state. Internal logic prevents an output-off open-load Fault from being reported at the Fault pin when any input is high. An output-off open-load Fault will be reported at the Fault Status pin after an open load occurs, all inputs not corresponding to the faulted output are low and a time in excess of $t_{OS(off)}$ is exceeded after switching OFF the input corresponding to the faulted output.

An important note that bears repeating is that an output-off open-load Fault will not be reported at the Fault Status pin unless all input pins are at a logic low state (Figure 13). This is a Fault Status interrogation feature. It helps in distinguishing between an output-on open-load Fault and an output-on over-current Fault. (Fault Status interrogation is explained in greater detail in a later section).

The time the output voltage takes to reach $V_{Ooff(th)}$ after being turned OFF is t_{off} false fault. It is a function of the load resistance (R_{load}); load inductance (L_{load}); load current (I_{load}); output-on resistance ($R_{DS(on)}$), output capacitance (C_O); load supply voltage (V_{load}); and the turn OFF time (t_{off}). The value of t_{off} is comprised of the V_{in} high-to-low propagation delay time ($t_{off(dly)}$), and the output voltage fall time (t_f).

For the case when:

$$1/2 L_{load} (I_{load})^2 \gg 1/2 C_O (V_{Ooff(th)})^2 \quad (7)$$

$$t_{off \text{ false fault}} = [(C_O \Delta V) / I_{load}] + t_{off} \quad (8)$$

$$\text{where: } I_{load} = V_{load} / [R_{load} + R_{DS(on)}] \quad (9)$$

$$\Delta V = V_{Ooff(th)} - [I_{load} R_{DS(on)}] \quad (10)$$

$$t_{off} = t_{off(dly)} + t_f \quad (11)$$

Using Equation 7 for the transient case,

when: $V_{load} = 14 \text{ V}$

$R_{DS(on)} = 0.3 \Omega$

$L_{load} = 10 \text{ mH}$

$R_{load} = 14 \Omega$

$C_O = 0.001 \mu\text{F}$

$V_{Ooff(th)} = 3.7 \text{ V}$

an Output-Off open-load Fault will be detected but not reported after initial turn OFF for a duration of $3.5 \text{ ns} + t_{off}$. From Equation 7, the energy stored in the load inductor will be 4.8 mJ . This is much greater than the 68 nJ needed to charge the output capacitance. This allows the use of Equation 8 in determining the false output-off open-load Fault duration following turn OFF because it assures that the output capacitance will be charged by the energy stored in the load inductance.

Over-Current Fault

An over-current (short circuit or current limit) Fault is the detection and reporting of any output over-current condition. An over-current condition is defined as a condition where

load current exceeds the internal current limit value (typically 4.0 A). An over-current condition activates the current limit circuit. This circuit then sends an analog signal to the gate control circuit, lowering the voltage on the output transistor's gate. Lowering the gate voltage forces the output transistor to transition from the resistive (fully enhanced) mode of operation to the current limit (between fully enhanced and fully OFF) mode.

The actual detection of an over-current condition does not occur at the initial onset of current limit. The onset of current limit causes the voltage on the affected output to increase. The actual Over-Current detection occurs when the output voltage increases and exceeds the over-current Detect Voltage Threshold ($V_{OC(limit)}$, typically 3.7 V), while the corresponding input signal is in a logic high state.

After detection, the reporting of an over-current Fault at the Fault Status output is delayed by a time equal to the over-current Sense Time (t_{OC}), see Figures 5 and 6. This delay time is typically $55 \mu\text{s}$. If the over-current condition no longer exists after the over-current Sense Time has passed, then no fault is reported. The purpose of the Fault reporting delay is to blank any false faults that might be reported due to high inrush current loads such as incandescent lamps. If the over-current condition still exists after the delay time has passed, then a fault will be reported at the Fault Status output and the affected output is turned OFF.

The Over-Current Sense Time is accomplished internally with four separate timers that reset and start independent of each other whenever a corresponding output is turned ON, either due to the corresponding input turning ON or the completion of the over-current Refresh Time (t_{ref}) explained in the next paragraph, (see Figures 5 and 6). An over-current Fault will be reported at the Fault Status output when an over-current condition is detected and a lapse time in excess of t_{OC} is exceeded after turning ON the affected output.

At the same time the over-current Fault is reported, a single internal over-current refresh timer resets, causing any over-current outputs to be turned OFF for a duration of t_{ref} , typically 3.6 ms . After a time t_{ref} , the faulted output(s) will be turned ON again to check if the over-current condition still exists. If the over-current condition still exists, the output(s) will be turned OFF again after a time t_{OC} . This periodic retry continues turning ON and OFF over-current loads at a duty cycle of $t_{OC} / (t_{OC} + t_{ref})$ with a period of $t_{OC} + t_{ref}$ until either the input is turned OFF or the over-current condition is removed. Any subsequent over-current conditions will reset and restart the t_{ref} timer.

Detection of an over-current condition coincides with, but does not occur until after the onset of current limit. This allows a specific but small current limit range to go undetected. The factors that determine the value of load resistance causing an over-current condition to be detected are: the Output-Load Current Limit [$I_{DS(limit)}$]; load voltage (V_{load}); and the Over-Current Detect Threshold Voltage [$V_{OC(limit)}$] as shown below:

$$R_{load(detect)} = \frac{[V_{load} - V_{OC(limit)}]}{I_{DS(limit)}} \quad (12)$$

The factors that determine the value of load resistance that will cause the onset of current limit are: $I_{DS(limit)}$, V_{load} , and $R_{DS(on)}$, as shown below.

$$R_{load(limit)} = [V_{load} / I_{DS(limit)}] - R_{DS(on)} \quad (13)$$

For the case when: $V_{load} = 14 \text{ V}$
 $V_{OC(limit)} = 3.7 \text{ V}$
 $R_{DS(on)} = 0.3 \text{ } \Omega$
 $I_{DS(limit)} = 4.0 \text{ A}$

an over-current condition will be detected for any load resistance such that $R_{load} \leq 2.6 \text{ } \Omega$. An undetected current limit condition will occur any time $2.6 \text{ } \Omega \leq R_{load} \leq 3.2 \text{ } \Omega$. Notice that the undetected current limit range is quite small.

Fault Interrogation

Even though the MC33293A incorporates a single Fault Status Output pin for reporting three different fault conditions, a real time interrogation routine can be used to determine which one of the three Fault conditions is being reported and which single output is affected.

An important point to note about Fault interrogation is that only one fault on a single output can be interpreted. In other words, if more than one over-current or open-load Fault exists among the four outputs, it is *not* possible to distinguish which outputs have a fault and which do not. It is very unlikely, however, that more than one output will be faulted at the same time.

When a Fault is reported, the first step is to determine if it is an over-current or open-load Fault ($R_{load} \geq 447 \text{ k}\Omega$, typical). This is done by taking all the inputs (single or dual) to a logic low state. If the Fault Status resets (changes to a logic high state) after the Fault Status Reset Delay Time ($t_{s(reset)}$, see Figure 4) has lapsed, then an over-current Fault is being reported. If the Fault Status does not reset (remains

at a logic low state) after $t_{s(reset)}$ has lapsed, then an open-load Fault ($R_{load} \geq 447 \text{ k}\Omega$, typical) is being reported. This type of interrogation is possible because an output-off open-load Fault can only be reported when all the inputs are in a logic low state.

For an over-current Fault, the next step is to determine which single output is affected. After all inputs are turned OFF and the fault status resets, each input is then turned ON then OFF sequentially. A Fault will again be reported when the input to the corresponding Over-Current output is turned ON and $t_{os(on)}$ has lapsed. If the dual input mode is being used, an over-current Fault can only be interrogated down to the two outputs being driven together.

For an open-load Fault ($R_{load} \geq 447 \text{ k}\Omega$, typical) interrogation, all inputs are turned OFF and the fault status remains set. Each input is then turned ON and OFF sequentially. The Fault status will remain set when the input to the corresponding faulted output is turned ON and $t_{os(on)}$ has lapsed. If the dual input mode is used, an open-load Fault can only be interrogated down to the two outputs driven together.


From the example following Equation 1, the typical value of $R_{open(on)}$ is $187 \text{ } \Omega$. From the example following Equation 6, the typical value of $R_{open(off)}$ is $447 \text{ k}\Omega$. Therefore, if the load resistance is between $187 \text{ } \Omega$ and $447 \text{ k}\Omega$ typically, an output-on open-load Fault will be reported at the Fault Status output but an output-off open-load Fault will not. This condition is referred to as a *soft open fault*. If a soft open fault exists, it is reported at the Fault Status output the same as an over-current Fault except for the reporting delay time. A soft open fault has a reporting delay time of 2.2 ms typically, and an over-current Fault has a reporting delay time of only $55 \text{ } \mu\text{s}$ typically, after the input to the faulted output is turned ON.

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Figure 14. Truth Table

Conditions of Outputs	Inputs							Outputs					
	1	2	3	4	S/D	1 & 2	3 & 4	1	2	3	4	Fault	
Non-Faulted Operation	L	L	L	L	L	X	X	H	H	H	H	H	
	L	L	L	H	L	X	X	H	H	H	L	H	
	L	L	H	L	L	X	X	H	H	L	H	H	
	L	L	H	H	L	X	X	H	H	L	L	H	
	L	H	L	L	L	X	X	H	L	H	H	H	
	L	H	L	H	L	X	X	H	L	H	L	H	
	L	H	H	L	L	X	X	H	L	L	L	H	
	L	H	H	H	L	X	X	H	L	L	L	L	H
	H	L	L	L	L	X	X	L	H	H	H	H	H
	H	L	L	H	L	X	X	L	H	H	L	H	H
	H	L	H	L	L	X	X	L	H	L	L	L	H
	H	L	H	H	L	X	X	L	L	H	H	H	H
	H	H	L	L	L	X	X	L	L	H	L	H	H
	H	H	L	H	L	X	X	L	L	L	L	L	H
	H	H	H	L	L	X	X	L	L	L	L	H	H
	H	H	H	H	L	X	X	L	L	L	L	L	H
	X	X	X	X	H	L	L	H	H	H	H	H	H
	X	X	X	X	H	H	L	L	L	L	H	H	H
	X	X	X	X	H	L	H	H	H	H	L	L	H
	X	X	X	X	H	H	H	H	L	L	L	L	H
open-load Fault On Output 1	L	L	L	L	L	X	X	L	H	H	H	L	
	H	L	L	L	L	X	X	L	H	H	H	L	
	L	H	H	H	L	X	X	L	L	L	L	H*	
	H	H	H	H	L	X	X	L	L	L	L	L	
	X	X	X	X	H	L	L	L	H	H	H	L	
	X	X	X	X	H	H	L	L	L	H	H	L	
	X	X	X	X	H	L	H	L	H	L	L	H*	
Over-Current Fault On Output 1	L	L	L	L	L	X	X	H	H	H	H	H	
	H	L	L	L	L	X	X	H	H	H	H	L	
	L	H	H	H	L	X	X	H	L	L	L	H	
	H	H	H	H	L	X	X	H	L	L	L	L	
	X	X	X	X	H	L	L	H	H	H	H	H	
	X	X	X	X	H	H	L	H	L	H	H	L	
	X	X	X	X	H	L	H	H	H	H	L	L	H
X	X	X	X	H	H	H	H	H	L	L	L	L	

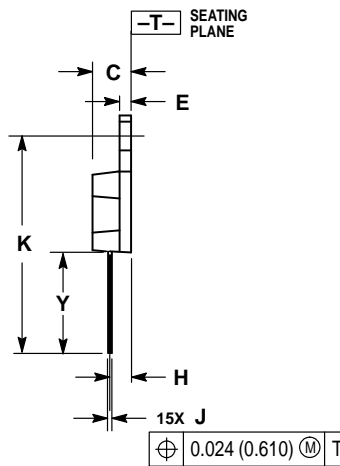
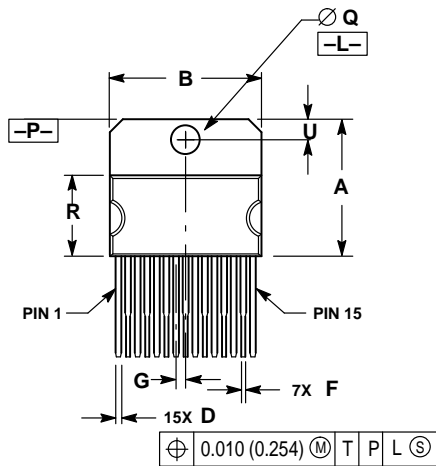
*NOTE: All inputs must be a logic low state for an Output-Off open-load Fault to be reported.

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OUTLINE DIMENSIONS

T SUFFIX PLASTIC PACKAGE CASE 821D-03 ISSUE C

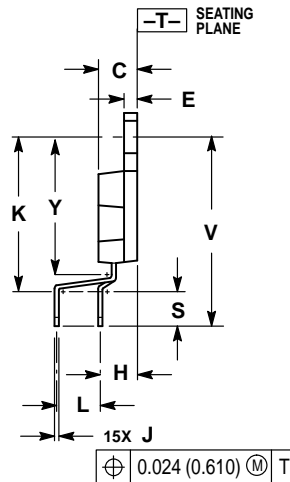
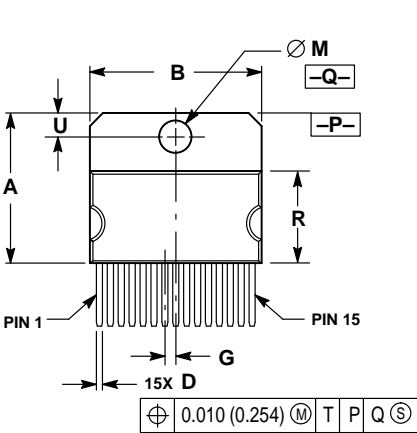


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 (0.250).
6. DELETED
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION. AT MAXIMUM MATERIAL CONDITION.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.681	0.694	17.298	17.627
B	0.784	0.792	19.914	20.116
C	0.173	0.181	4.395	4.597
D	0.024	0.031	0.610	0.787
E	0.058	0.062	1.473	1.574
F	0.016	0.023	0.407	0.584
G	0.050 BSC		1.270 BSC	
H	0.110 BSC		2.794 BSC	
J	0.018	0.024	0.458	0.609
K	1.078	1.086	27.382	27.584
Q	0.148	0.151	3.760	3.835
R	0.416	0.426	10.567	10.820
U	0.110 BSC		2.794 BSC	
Y	0.503 REF		12.776 REF	

TV SUFFIX PLASTIC PACKAGE CASE 821C-04 ISSUE D



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
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5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 (0.250).
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION. AT MAXIMUM MATERIAL CONDITION.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.684	0.694	17.374	17.627
B	0.784	0.792	19.914	20.116
C	0.173	0.181	4.395	4.597
D	0.024	0.031	0.610	0.787
E	0.058	0.062	1.473	1.574
G	0.050 BSC		1.270 BSC	
H	0.169 BSC		4.293 BSC	
J	0.018	0.024	0.458	0.609
K	0.700	0.710	17.780	18.034
L	0.200 BSC		5.080 BSC	
M	0.148	0.151	3.760	3.835
R	0.416	0.426	10.567	10.820
S	0.157	0.167	3.988	4.242
U	0.105	0.115	2.667	2.921
V	0.868 REF		22.047 REF	
Y	0.625	0.639	15.875	16.231

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