ST-NXP Wireless

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As from August 2nd 2008, the wireless operations of NXP have moved to a new company, ST-NXP Wireless.

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- **Company name - NXP B.V.** is replaced with **ST-NXP Wireless**.

- **Copyright** - the copyright notice at the bottom of each page "© NXP B.V. 200x. All rights reserved", shall now read: "© ST-NXP Wireless 200x - All rights reserved".

- **Web site** - http://www.nxp.com is replaced with http://www.stnwireless.com

- **Contact information** - the list of sales offices previously obtained by sending an email to salesaddresses@nxp.com , is now found at http://www.stnwireless.com under Contacts.

If you have any questions related to the document, please contact our nearest sales office. Thank you for your cooperation and understanding.

ST-NXP Wireless

ISP1704A

ULPI Hi-Speed USB transceiver

Rev. 01 — 28 July 2008 Product data sheet

1. General description

The ISP1704A is a UTMI+ Low Pin Interface (ULPI) Hi-Speed Universal Serial Bus (USB) transceiver that is fully compliant with *Universal Serial Bus Specification Rev. 2.0*, *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*, *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1* and *Battery Charging Specification Rev. 1.0*.

The ISP1704A can transmit and receive USB data at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s), and provides a pin-optimized, physical layer front-end attachment to the USB host, peripheral or OTG controller with Single Data Rate (SDR) ULPI link. The ISP1704A can transparently transmit and receive UART signaling.

It is ideal for use in portable electronic devices, such as mobile phones, digital still cameras, digital video cameras, Personal Digital Assistants (PDAs) and digital audio players. It allows USB Application-Specific Integrated Circuits (ASICs), Programmable Logic Devices (PLDs) or any system chip set to interface with the physical layer of the USB through a 12-pin (SDR) interface.

The ISP1704A can interface to devices with digital I/O voltages in the range of 1.65 V to 1.95 V.

The ISP1704A is available in TFBGA36 package.

2. Features

- Fully complies with:
  - USB: *Universal Serial Bus Specification Rev. 2.0*
  - OTG: *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*
  - ULPI: *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*
  - *Battery Charging Specification Rev. 1.0*
- Integrated battery charging detection circuit that operates during power-down mode to save current; the ISP1704A automatically detects if a USB battery charger is attached; this function can be disabled using external pins
- Interfaces to USB host, peripheral or OTG cores; optimized for portable devices or system ASICs with built-in ULPI link
- Complete Hi-Speed USB physical front-end solution that supports high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s)
  - Integrated 45 Ω ± 10 % high-speed termination resistors, 1.5 kΩ ± 5 % full-speed device pull-up resistor, and 15 kΩ ± 5 % host termination resistors
  - Integrated parallel-to-serial and serial-to-parallel converters to transmit and receive
  - USB clock and data recovery to receive USB data up to ±500 ppm
  - USB data synchronization from 60 MHz input to 480 MHz output during transmit

- Insertion of stuff bits during transmit and discarding of stuff bits during receive
- Non-Return-to-Zero Inverted (NRZI) encoding and decoding
- Supports bus reset, suspend, resume and high-speed detection handshake (chirp)

- Complete USB OTG physical front-end that supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
  - Supports external charge pump or external V_{BUS} power switch
  - Complete control over USB termination resistors
  - Data line and V_{BUS} pulsing session request methods
  - Integrated V_{BUS} voltage comparators
  - Integrated cable (ID) detector
- Flexible system integration and very low power consumption, optimized for portable devices
  - 3.0 V to 4.5 V supply voltage input range; charger detection operates from V_{CC} 2.4 V to 4.5 V
  - Internal voltage regulator supplies 2.7 V or 3.3 V and 1.8 V
  - Supports interfacing I/O voltage of 1.65 V to 1.95 V; separate I/O voltage supply pins minimize crosstalk
  - Both active-HIGH and active-LOW chip select pins are available
  - Power down internal regulators in power-down mode when $V_{CC(I/O)}$ is not present or when the chip is deasserted
  - Typical operating current of 13 mA to 34 mA, depending on the USB speed and bus utilization
  - Typical suspend current of 70 μA
  - Typical power-down state current of 5.5 μA
  - 3-state ULPI interface by the chip select, allowing bus reuse by other applications
- Highly optimized ULPI compliant
  - 60 MHz, 12-pin interface between the core and the transceiver, including an 8-bit SDR bus
  - Supports 60 MHz output clock configuration
  - Integrated Phase-Locked Loop (PLL) supporting clock frequencies of 19.2 MHz and 26 MHz
  - Clock frequency selectable by pin
  - Fully programmable ULPI-compliant register set
  - 3-pin or 6-pin full-speed or low-speed serial mode
  - Internal Power-On Reset (POR) circuit
- UART interface:
  - Supports transparent UART signaling on pins DP and DM for the UART accessory application
  - 2.7 V UART signaling on pins DP and DM
  - Entering UART mode by register setting
  - Exiting UART mode by asserting pin STP or by toggling chip select
- Full industrial grade operating temperature range from −40 °C to +85 °C
- ESD compliance:
  - JESD22-A114D ±2 kV contact Human Body Model (HBM)
  - JESD22-A115-A ±200 V Machine Model (MM)
  - JESD22-C101-A ±500 V Charge Device Model (CDM)

- IEC 61000-4-2, ±8.8 kV contact on the DP and DM pins
- IEC 61000-4-2 with IP4359CX4/LF, ±20 kV contact on the DP and DM pins

- Available in small TFBGA36 (3.5 mm × 3.5 mm) Restriction of Hazardous Substances (RoHS) compliant, halogen-free and lead-free package

3. Applications

- Mobile phone
- Digital still camera
- MP3 player
- PDA
- Digital TV
- Digital Video Disc (DVD) recorder
- External storage device
- Printer
- Scanner
- Set-Top Box (STB)
- Video camera

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
ISP1704AET	TFBGA36	plastic thin fine-pitch ball grid array package; 36 balls; body 3.5 × 3.5 × 0.8 mm	SOT912-1

5. Marking

Table 2. Marking codes

Type number	Marking code[1]
ISP1704AET	1704

[1] The package marking is the first line of text on the IC package and can be used for IC identification.

6. Block diagram

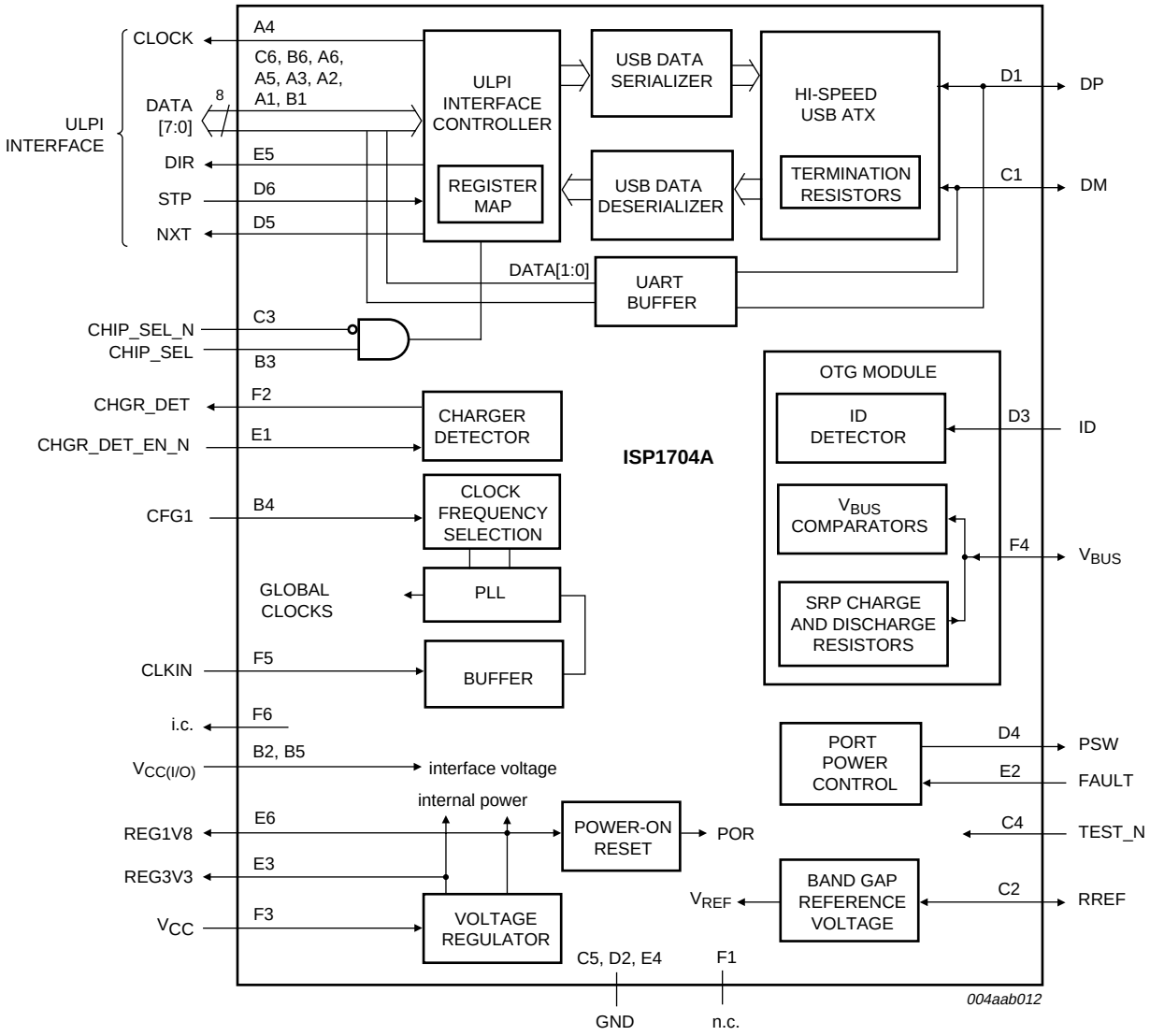


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

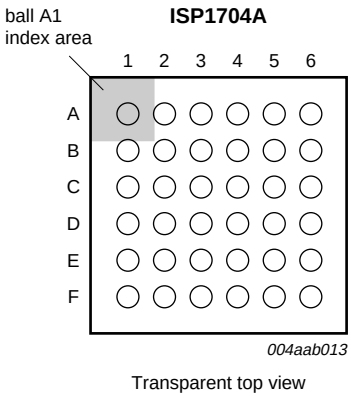


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol[1]	Pin	Type[2]	Description[3]
DATA1	A1	I/O	ULPI data pin 1 3-state output; plain input
DATA2	A2	I/O	ULPI data pin 2 3-state output; plain input
DATA3	A3	I/O	ULPI data pin 3 3-state output; plain input
CLOCK	A4	O	60 MHz clock output when clock is applied on the CLKIN pin 3-state output
DATA4	A5	I/O	ULPI data pin 4 3-state output; plain input
DATA5	A6	I/O	ULPI data pin 5 3-state output; plain input
DATA0	B1	I/O	ULPI data pin 0 3-state output; plain input
$V_{CC(I/O)}$	B2, B5	P	input I/O supply voltage; 1.65 V to 1.95 V; a 0.1 µF decoupling capacitor is recommended for each pin
CHIP_SEL	B3	I	when either the CHIP_SEL or CHIP_SEL_N pin is deasserted, ULPI pins will be in 3-state and the ISP1704A is in power-down mode; both CHIP_SEL and CHIP_SEL_N must be asserted for the ULPI interface to operate normally; when not in use, connect to $V_{CC(I/O)}$ plain input
CFG1	B4	I	select clock frequency connect to GND for 19.2 MHz or to $V_{CC(I/O)}$ for 26 MHz plain input

Table 3. Pin description *...continued*

Symbol[1]	Pin	Type[2]	Description[3]
DATA6	B6	I/O	ULPI data pin 6 3-state output; plain input
DM	C1	AI/O	connect to the D– pin of the USB connector • USB mode: D– input or output • UART mode: TXD output
RREF	C2	AI/O	resistor reference; connect through a 12 kΩ ± 1 % resistor to GND
CHIP_SEL_N	C3	I	when either the CHIP_SEL or CHIP_SEL_N pin is deasserted, ULPI pins will be in 3-state and the ISP1704A is in power-down mode; both CHIP_SEL and CHIP_SEL_N must be asserted for the ULPI interface to operate normally; when not in use, connect to GND plain input
TEST_N	C4	I	directly connect to $V_{CC(I/O)}$ for normal operation plain input
GND	C5, D2, E4	P	ground supply
DATA7	C6	I/O	ULPI data pin 7 3-state output; plain input
DP	D1	AI/O	connect to the D+ pin of the USB connector • USB mode: D+ input or output • UART mode: RXD input During UART mode, an internal 125 kΩ ± 20 % pull-up resistor is present on this pin.
ID	D3	I	identification (ID) pin of the micro-USB connector; if this pin is not in use, connect it directly to the REG3V3 pin (an internal 400 kΩ pull-up resistor is present on this pin) plain input; TTL
PSW	D4	O	external V_{BUS} power switch or external charge pump enable active-HIGH output; 5 V tolerant; external 100 kΩ pull-down resistor
NXT	D5	O	ULPI next signal 3-state output
STP	D6	I	ULPI stop signal plain input
CHGR_DET_EN_N	E1	I	charger detect enable; connect to V_{CC} when the charger detection is not required; connect to GND when the charger detection is needed to act in peripheral mode plain input
FAULT	E2	I	input for the V_{BUS} digital overcurrent or fault detector signal; if this pin is not in use, connect it to GND plain input; 5 V tolerant
REG3V3	E3	P	3.3 V regulator output for USB mode or 2.7 V regulator output for UART mode; requires parallel 0.1 µF and 4.7 µF capacitors; internally powers ATX and other analog circuits; must not be used to power external circuits
DIR	E5	O	ULPI direction signal 3-state output
REG1V8	E6	P	1.8 V regulator output; requires parallel 0.1 µF and 4.7 µF capacitors; internally powers the digital core; must not be used to power external circuits
n.c.	F1	-	not connected

Table 3. Pin description *...continued*

Symbol[1]	Pin	Type[2]	Description[3]
CHGR_DET	F2	O	active-HIGH signal to start high current charging; when not in use, leave this pin open active-HIGH output; 5 V tolerant; external 100 kΩ pull-down resistor
V_{CC}	F3	P	input supply voltage or battery source; 3.0 V to 4.5 V **Remark:** Below 3.0 V, USB full-speed and low-speed transactions are not guaranteed to work, though some devices may work with the ISP1704A at these voltages.
V_{BUS}	F4	AI/O	connect to the V_{BUS} pin of the USB connector; if this pin is not in use, leave it open (an internal 90 kΩ ± 11 % pull-down resistor is present on this pin)
CLKIN	F5	AI/O	clock input; 1.8 V peak input allowed; frequency depends on status on the CFG1 pin
i.c.	F6	AI/O	internally connected; leave open

[1] Symbol names ending with underscore N (for example, NAME_N) indicate active-LOW signals.

[2] I = input; O = output; I/O = digital input/output; AI/O = analog input/output; P = power or ground pin.

[3] A detailed description of these pins can be found in Section 8.12.

8. Functional description

8.1 ULPI interface controller

The ISP1704A provides a 12-pin interface that is compliant with *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*. This interface must be connected to a USB link.

The ULPI interface controller provides the following functions:

- ULPI-compliant interface and register set
- Allows full control over the USB peripheral or host functionality
- Parses the USB transmit and receive data
- Prioritizes the USB receive data, USB transmit data, interrupts and register operations
- Low-power mode
- Transparent UART mode
- 3-pin serial mode
- 6-pin serial mode
- Generates RXCMDs (status updates)
- Maskable interrupts
- Manual control of the charger detection process

8.2 USB serializer and deserializer

The USB data serializer prepares data to transmit on the USB bus. To transmit data, the USB link sends a transmit command and data on the ULPI bus. The serializer performs parallel-to-serial conversion, bit stuffing and NRZI encoding. For packets with a PID, the serializer adds a SYNC pattern to the start of the packet, and an EOP pattern to the end of the packet. When the serializer is busy and cannot accept any more data, the ULPI interface controller deasserts NXT.

The USB data deserializer decodes data received from the USB bus. When data is received, the deserializer strips the SYNC and EOP patterns, and then performs serial-to-parallel conversion, NRZI decoding and discarding of stuff bits on the data payload. The ULPI interface controller sends data to the USB link by asserting DIR, and then asserting NXT whenever a byte is ready. The deserializer also detects various receive errors, including bit stuff errors, elasticity buffer underrun or overrun, and byte-alignment errors.

8.3 Hi-Speed USB (USB 2.0) ATX

The Hi-Speed USB ATX block is an analog front-end containing the circuitry needed to transmit, receive and terminate the USB bus in high-speed, full-speed and low-speed, for USB peripheral, host or OTG implementations. The following circuitry is included:

- Differential drivers to transmit data at high-speed, full-speed and low-speed
- Differential and single-ended receivers to receive data at high-speed, full-speed and low-speed
- Squelch circuit to detect high-speed bus activity
- High-speed disconnect detector

- 45 Ω high-speed bus terminations on pins DP and DM
- 1.5 kΩ pull-up resistor on pin DP
- 15 kΩ bus terminations on pins DP and DM

For details on controlling resistor settings, see Table 14.

8.4 Voltage regulator

The ISP1704A contains a built-in voltage regulator that conditions the V_{CC} supply for use inside the ISP1704A. The voltage regulator:

- Supports input supply range 3.0 V < V_{CC} < 4.5 V; battery charger detection can work from 2.4 V to 4.5 V.
- Can be supplied from a battery with the voltage range mentioned above.
- Supplies internal digital circuitry with 1.8 V and analog circuitry with 3.3 V or 2.7 V.
- In USB mode, automatically bypasses the internal 3.3 V regulator when V_{CC} < 3.5 V, the internal analog circuitry directly draws power from the V_{CC} pin. In UART mode, the bypass switch will be disabled.

Table 4 shows the conditions for power down.

Table 4. Conditions for power down

V_{BUS} < $V_{th(trig)r(VBUS)}$	Chip select	$V_{CC(I/O)}$	CHGR_DET_EN_N	Power down
0 V	assert	0 V	LOW	powered down
0 V	deassert	1.65 V to 1.95 V	LOW	powered down
5 V	X	X	LOW	regulator on
X	X	0 V	HIGH	powered down
X	deassert	1.65 V to 1.95 V	HIGH	powered down
X	assert	1.65 V to 1.95 V	HIGH	regulator on

8.5 PLL

The ISP1704A has a built-in Phase-Locked Loop (PLL) for internal clock generation. The clock frequencies supported are 19.2 MHz and 26 MHz.

The PLL takes the square wave clock, and multiplies or divides it into various frequencies for internal use.

The PLL produces the following frequencies, irrespective of the clock source:

- 1.5 MHz for low-speed USB data
- 12 MHz for full-speed USB data
- 60 MHz clock for the ULPI interface controller
- 480 MHz for high-speed USB data
- Other internal frequencies for data conversion and data recovery

8.6 UART buffer

The UART buffer includes circuits to support the transparent UART signaling between the DATA0 or DATA1 pin and the DM or DP pin.

When the ISP1704A is put into UART mode, it acts as a voltage level shifter between the following pins:

- From DATA0 ($V_{CC(I/O)}$ level) to DM (2.7 V level) for the UART TXD signaling path.
- From DP (2.7 V level) to DATA1 ($V_{CC(I/O)}$ level) for the UART RXD signaling path.

8.7 OTG module

This module contains several sub-blocks that provide all the functionality required by the USB OTG specification. Specifically, it provides the following circuits:

- The ID detector to sense the ID pin of the micro-USB cable. The ID pin dictates which device is initially configured as a host and which as a peripheral.
- V_{BUS} comparators to determine the V_{BUS} voltage level. This is required for the V_{BUS} detection, SRP and HNP.
- Resistors to temporarily charge and discharge V_{BUS}. This is required for SRP.

8.7.1 ID detector

The ID detector detects which end of the micro-USB cable is plugged in. The ID detector must first be enabled by setting the ID_PULLUP register bit to logic 1. If the ISP1704A senses a value on the ID pin that is different from the previously reported value, an RXCMD status update will be sent to the USB link, or an interrupt will be asserted.

- If the micro-B end of the cable is plugged in (or nothing is plugged in), the ISP1704A will report that ID_GND is logic 1. The USB link must be in the B-device state.
- If the micro-A end of the cable is plugged in, the ISP1704A will report that ID_GND is logic 0. The USB link must be in the A-device state.

The ID pin has a weak pull-up resistor ($R_{weakPU(ID)}$) permanently enabled to avoid the floating condition.

8.7.2 V_{BUS} comparators

The ISP1704A provides three comparators to detect the V_{BUS} voltage level. The comparators are explained in the following subsections.

8.7.2.1 V_{BUS} valid comparator

This comparator is used by hosts and A-devices to determine whether the voltage on V_{BUS} is at a valid level for operation. The ISP1704A minimum threshold for the V_{BUS} valid comparator is 4.4 V. Any voltage on V_{BUS} below this threshold is considered invalid. During power-up, it is expected that the comparator output will be ignored.

8.7.2.2 Session valid comparator

The session valid comparator is a TTL-level input that determines when V_{BUS} is high enough for a session to start. Peripherals, A-devices and B-devices use this comparator to detect when a session is started. The A-device also uses this comparator to determine when a session is completed. The session valid threshold of the ISP1704A is between 0.8 V to 2.0 V.

8.7.2.3 Session end comparator

The session end comparator determines when V_{BUS} is below the B-device session end threshold of 0.2 V to 0.8 V. The B-device uses this threshold to determine when a session has ended.

8.7.3 SRP charge and discharge resistors

The ISP1704A provides on-chip resistors for short-term charging and discharging of V_{BUS}. These are used by the B-device to request a session, prompting the A-device to restore the V_{BUS} power. First, the B-device makes sure that V_{BUS} is fully discharged from the previous session by setting the DISCHRG_VBUS register bit to logic 1 and waiting for SESS_END to be logic 1. Then the B-device charges V_{BUS} by setting the CHRG_VBUS register bit to logic 1. The A-device sees that V_{BUS} is charged above the session valid threshold and starts a session by turning on the V_{BUS} power.

8.8 Port power control

For an OTG or host application, the ISP1704A uses the PSW pin to control the external power switch for the V_{BUS} 5 V supply. The overcurrent detector output of the external power switch can be connected to the FAULT pin of the ISP1704A to indicate to the ULPI link the V_{BUS} overcurrent status. For the connection scheme, see Figure 3.

When the FAULT pin is not used, connect it to GND.

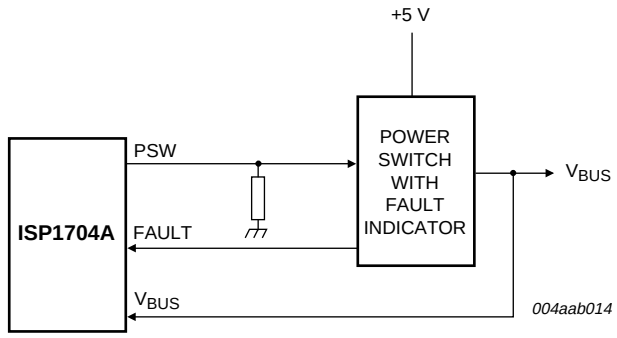


Fig 3. Digital overcurrent detection scheme

8.9 Band gap reference voltage

The band gap circuit provides a stable internal voltage reference to bias the analog circuitry. This band gap circuit requires an accurate external reference resistor. Connect a 12 kΩ ± 1 % resistor between the RREF pin and GND.

8.10 Power-On Reset (POR)

An internal POR pulse is generated when REG1V8 rises above $V_{POR(trip)}$. The internal POR pulse will be generated whenever REG1V8 drops below $V_{POR(trip)}$ for more than $t_{w(REG1V8\_L)}$.

To give a better view of the functionality, Figure 4 shows a possible curve of REG1V8. The internal POR starts with logic 0 at t0. At t1, the detector will see the passing of the trip level so that a POR pulse is generated to reset all internal circuits. If REG1V8 dips from t2

to t3 for greater than $t_{w(REG1V8\_L)}$, another POR pulse is generated. If the dip from t4 to t5 is less than $t_{w(REG1V8\_L)}$, the internal POR pulse will not be generated and will remain LOW.

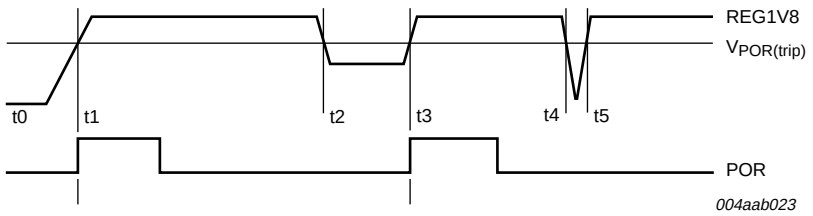


Fig 4. Internal power-on reset timing

8.11 Power-up, reset and bus idle sequence

Figure 5 shows a typical start-up sequence.

On power-up, the ISP1704A performs an internal power-on reset and asserts DIR to indicate to the link that the ULPI bus cannot be used. When the internal PLL is stable, the ISP1704A deasserts DIR and drives a 60 MHz clock on the CLOCK pin. The power-up time depends on the V_{CC} supply rise time and PLL start-up time $t_{startup(PLL)}$. When DIR is deasserted, the link must drive the data bus to a valid level. By default, the link must drive data to LOW. Before beginning USB packets, the link must set the RESET bit in the FUNC_CTRL register (see Section 10.5) to reset the ISP1704A. After the RESET bit is set, the ISP1704A will assert DIR until the internal reset completes. The ISP1704A will automatically deassert DIR and clear the RESET bit when the reset has completed. After every reset, an RXCMD is sent to the link to update USB status information. After this sequence, the ULPI bus is ready for use and the link can start USB operations.

If chip select is deasserted, the ISP1704A will be kept in power-down mode. In power-down mode, all ULPI interface pins will be put in 3-state, the internal regulator will be shut down, and the total current consumption in power-down mode will be less than that in low-power mode.

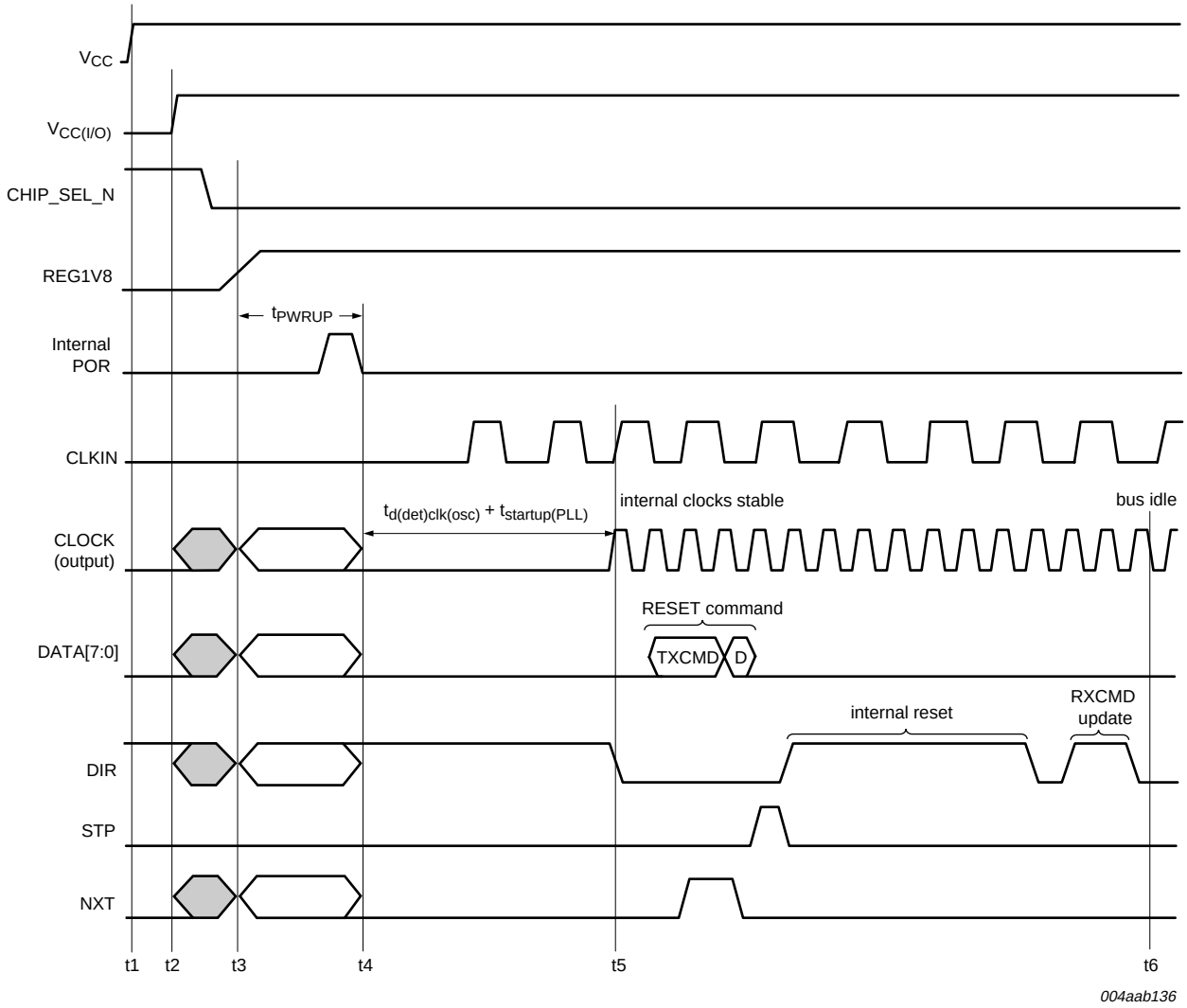
The link can do a hardware reset to the ISP1704A by powering down the regulator, see Table 4.

If the low-power mode is entered when $V_{CC(I/O)}$ is lost, see Table 8.

The recommended power-up sequence for the link is:

1. Apply the V_{CC} and $V_{CC(I/O)}$ voltage.
2. Assert chip select.
3. The link waits for at least t_{PWRUP}, ignoring all the ULPI pin status.
4. The link may start to detect the DIR status level. If DIR is detected as LOW, the link may send a RESET command.

The ULPI interface is ready for use.



t1 = V_{CC} is applied to the ISP1704A.

t2 = $V_{CC(I/O)}$ is turned on. ULPI interface pins CLOCK, DATA[7:0], DIR and NXT are in 3-state as long as chip select is deasserted.

t3 = Chip select turns from deassert to assert. The ISP1704A regulator starts to turn on. ULPI pads are not in 3-state and may drive to either LOW or HIGH. It is recommended that the link ignores the status of ULPI pins during t_{PWRUP}.

t4 = Power-on reset threshold is reached and the POR pulse is generated. After the POR pulse, ULPI pins are driven to a defined level. DIR is driven to HIGH and the other pins are driven to LOW.

t5 = The PLL is stabilized after $t_{d(det)clk(osc)} + t_{startup(PLL)}$. The CLOCK pin starts to output 60 MHz. The DIR pin will transition from HIGH to LOW. The link must drive DATA[7:0] and STP to LOW as the idle state. The link will then issue a reset command to initialize the ISP1704A.

t6 = The power-up sequence is completed and the ULPI bus interface is ready for use.

Fig 5. Power-up and reset sequence required before the ULPI bus is ready for use

8.11.1 Interface protection

By default, the ISP1704A enables a weak pull-up resistor on STP. If the STP pin is unexpectedly HIGH at any time, the ISP1704A will protect the ULPI interface by enabling weak pull-down resistors on DATA[7:0].

The interface protect feature prevents unwanted activity of the ISP1704A whenever the ULPI interface is not correctly driven by the link. For example, when the link powers up more slowly than the ISP1704A.

The interface protect feature can be disabled by setting the INTF_PROT_DIS bit to logic 1.

8.11.2 Interface behavior with respect to chip select

The use of chip select as a power-down control signal is optional. When chip select is deasserted, the ISP1704A will 3-state ULPI pins and power-down the internal circuitry. If chip select is not used as a power-down control signal, it must be connected to LOW. Figure 6 shows the ULPI interface behavior when chip select is asserted and subsequently deasserted.

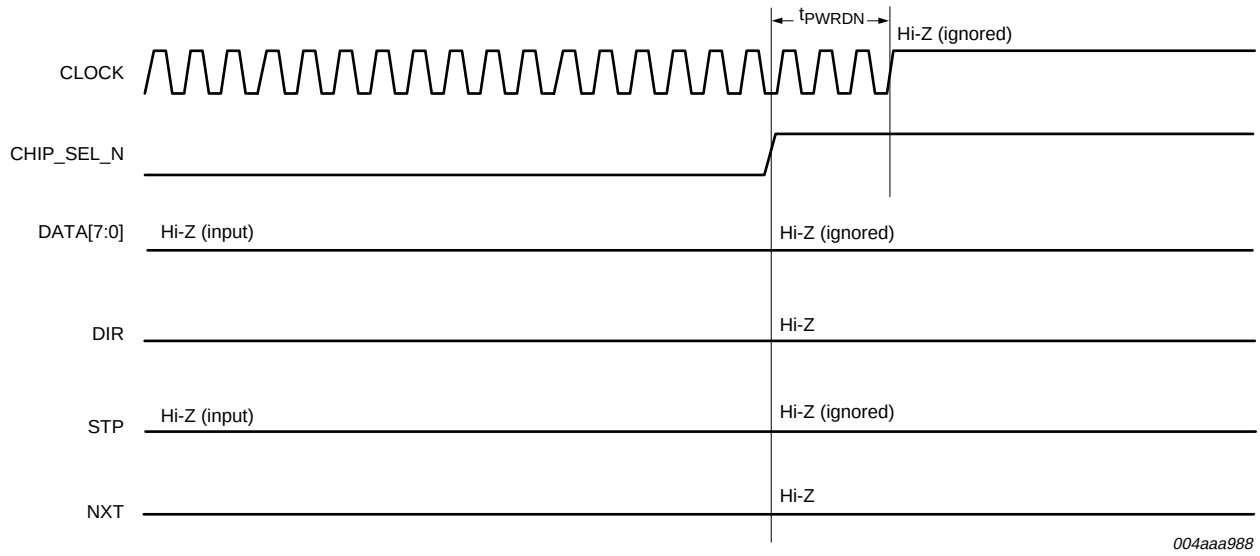


Fig 6. Interface behavior with respect to chip select

8.12 Detailed description of pins

8.12.1 DATA[7:0]

Bidirectional data bus pins. The USB link must drive DATA[7:0] to LOW when the ULPI bus is idle. When the link has data to transmit to the PHY, it drives a nonzero value. Weak pull-down resistors are incorporated into DATA[7:0] pins as part of the interface protect feature. For details, see Section 8.11.1.

DATA[7:0] pins can also be 3-stated when chip select is deasserted.

These pins can be reconfigured to carry various data types when the chip is not in synchronous mode. For details, see Section 9.2.1.

8.12.2 $V_{CC(I/O)}$

The input power pin that sets the I/O voltage level. A 0.1 µF decoupling capacitor is recommended on each $V_{CC(I/O)}$ pin.

8.12.3 RREF

Resistor reference analog I/O pin. A 12 kΩ ± 1 % resistor must be connected between the RREF pin and GND. This provides an accurate voltage reference that biases internal analog circuitry. Less accurate resistors cannot be used. It will affect the biasing current for analog circuits, thus the USB signal quality.

8.12.4 DP and DM

When the ISP1704A is in USB mode, the DP pin functions as the USB data plus line, and the DM pin functions as the USB data minus line.

When the ISP1704A is in transparent UART mode, the DP pin functions as the UART RXD input pin, and the DM pin functions as the UART TXD output pin.

The DP and DM pins must be connected to the D+ and D– pins of the USB receptacle.

8.12.5 FAULT

This pin is used to detect the V_{BUS} fault condition. If the function is not used, this pin must be connected to ground to avoid floating input.

If an external V_{BUS} overcurrent or fault detection circuit is used, the output fault indicator of that circuit can be connected to the FAULT input pin. The USE_EXT_VBUS_IND bit in the OTG_CTRL register (see Section 10.7) and the IND_PASSTHRU bit in the INTF_CTRL register (see Section 10.6) must be set to logic 1. The ISP1704A will inform the link of V_{BUS} fault events by sending RXCMDs on the ULPI bus.

The FAULT input pin is mapped to the A_VBUS_VLD bit in RXCMD. Any changes to the FAULT input will trigger RXCMD carrying the FAULT condition with A_VBUS_VLD.

8.12.6 PSW

The PSW pin is an active-HIGH output pin. It is used to control external charge pumps or V_{BUS} power switches to supply V_{BUS}. When in use, a 100 kΩ external pull-down resistor is required. This allows for per-port or ganged power control.

To enable the external power source by driving PSW to HIGH, the link must set the DRV_VBUS_EXT bit in the OTG_CTRL register (see Section 10.7) to logic 1.

Table 5 summarizes settings to drive 5 V on V_{BUS}.

Table 5. OTG_CTRL register power control bits

DRV_VBUS_EXT	Power source used
0	external 5 V V_{BUS} power source disabled (PSW = LOW)
1	external 5 V V_{BUS} power source enabled (PSW = HIGH)

8.12.7 ID

For OTG applications, the ID (identification) pin is connected to the ID pin of the micro-AB receptacle. As defined in *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*, the ID pin dictates the initial role of the link. If ID is detected as HIGH, the link must assume the role of a peripheral. If ID is detected as LOW, the link must assume a host role. Roles can be swapped at a later time by using HNP.

The ISP1704A provides an internal pull-up resistor ($R_{UP(ID)}$) to sense the value of the ID pin. The pull-up resistor must first be enabled by setting the ID_PULLUP register bit to logic 1. If the state of ID has changed, the ISP1704A will send an RXCMD or interrupt to the link. If the link does not receive any RXCMD or interrupt by time t_{ID}, then the ID state has not changed.

The ISP1704A also provides an internal weak pull-up resistor ($R_{weakPU(ID)}$). This weak pull-up resistor is always enabled to avoid a possible floating condition on the ID pin.

8.12.8 V_{CC}

Main input supply voltage for the ISP1704A. The ISP1704A operates correctly when V_{CC} is between 3.0 V and 4.5 V. The battery charger detection can operate between 2.4 V and 4.5 V. A 0.1 µF decoupling capacitor is recommended.

8.12.9 V_{BUS}

This I/O pin acts as an input to V_{BUS} comparators, and also as a power supply pin for SRP charge and discharge resistors. For details, see Figure 7.

The V_{BUS} pin requires a capacitive load. Table 6 provides the recommended capacitor values for various applications.

Table 6. Recommended V_{BUS} capacitor value

Application	V_{BUS} capacitor (C_{VBUS})
OTG	1 µF to 6.5 µF, 10 V
Standard host	120 µF ± 20 %, 10 V
Standard peripheral	1 µF to 10 µF, 10 V

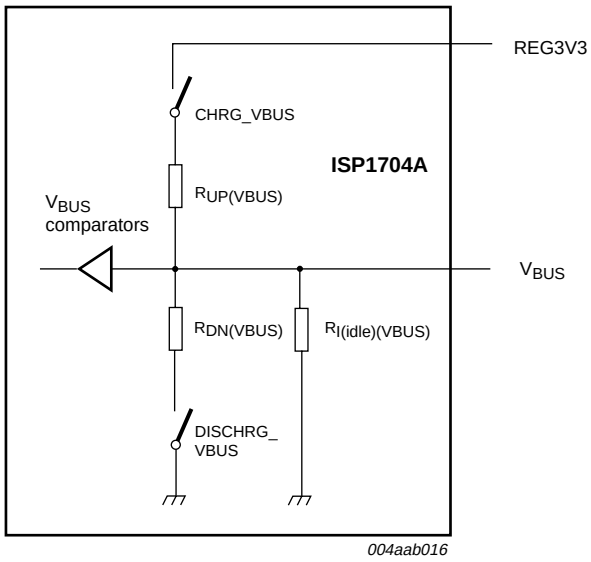


Fig 7. V_{BUS} pin internal pull-up and pull-down scheme

8.12.10 REG3V3 and REG1V8

These are output voltage pins from the internal regulator. These supplies are used internally to power digital and analog circuits.

For proper operation of the regulator, pins REG3V3 and REG1V8 must each be connected to a 0.1 µF capacitor in parallel with a 4.7 µF low ESR capacitor.

8.12.11 CLKIN

CLKIN is the clock input. The allowed clock frequency on the CLKIN pin is selectable by the CFG1 pin, as shown in Table 7.

Table 7. Allowed clock frequency on the CLKIN pin

Pin CFG1	Allowed clock frequency on the CLKIN pin
LOW	19.2 MHz
HIGH	26 MHz

8.12.12 CHIP_SEL, CHIP_SEL_N

When chip select is deasserted, ULPI pins DATA[7:0], CLOCK, DIR and NXT are 3-stated and the STP input is ignored; internal circuits are powered-down as well.

When chip select is asserted, the ISP1704A will operate normally.

Both the CHIP_SEL and CHIP_SEL_N pins must be asserted for the chip select to function. If any of the two is deasserted, the chip will enter power-down mode.

8.12.13 CHGR_DET

This pin will be driven to HIGH when a USB battery charger is detected. For details, see Section 9.1.3.

8.12.14 CHGR_DET_EN_N

This pin controls whether the ISP1704A automatically detects the presence of a USB battery charger in power-down mode. For details, see Section 9.1.3.

8.12.15 DIR

ULPI direction output pin. Synchronous to the rising edge of CLOCK. Controls the direction of the data bus. By default, the ISP1704A holds DIR at LOW, causing the data bus to be an input. When DIR is LOW, the ISP1704A listens for data from the link. The ISP1704A pulls DIR to HIGH only when it has data to send to the link, which is for one of two reasons:

- To send data (USB receive or register reads) and RXCMD status updates to the link.
- To block the link from driving the data bus during power-up, reset and low power (suspend) mode.

This pin can be 3-stated when chip select is deasserted.

8.12.16 STP

ULPI stop input pin. Synchronous to the rising edge of CLOCK. The link must assert STP to signal the end of a USB transmit packet or a register write operation. When DIR is asserted, the link can optionally assert STP for one clock cycle to abort the ISP1704A, causing it to deassert DIR in the next clock cycle.

8.12.17 NXT

ULPI next data output pin. Synchronous to the rising edge of CLOCK. The ISP1704A holds NXT at LOW, by default. When DIR is LOW and the link is sending data to the ISP1704A, NXT will be asserted to notify the link to provide the next data byte. When DIR is HIGH and the ISP1704A is sending data to the link, NXT will be asserted to notify the link that another valid byte is on the bus. NXT is not used for register read data or the RXCMD status update.

This pin can be 3-stated when chip select is deasserted.

8.12.18 CLOCK

A 60 MHz interface clock to synchronize the ULPI bus. All ULPI pins are synchronous to the rising edge of CLOCK.

8.12.19 CFG1

This input pin is used to select the clock frequency. Connect this pin to GND for 19.2 MHz frequency and to $V_{CC(I/O)}$ for 26 MHz frequency.

8.12.20 GND

Global ground signal. To ensure the correct operation of the ISP1704A, GND must be soldered to the cleanest available ground.

9. Modes of operation

9.1 Power modes

When both $V_{CC(I/O)}$ and V_{CC} are not powered, there will be no leakage from the V_{BUS} pin to all the remaining pins, including V_{CC} and $V_{CC(I/O)}$. Applying V_{BUS} within the normal range will not damage the ISP1704A chip.

When both V_{CC} and $V_{CC(I/O)}$ are powered and are within the operating voltage range, the ISP1704A will be fully functional as in normal mode.

When $V_{CC(I/O)}$ is powered and the V_{CC} voltage is below the operating range of the ISP1704A, the application system must detect the low voltage condition and set chip select to deassert (that is, put the ISP1704A in power-down mode). This is to protect the ULPI and USB interfaces from driving wrong levels. Under this condition, the $V_{CC(I/O)}$ voltage will not leak to USB pins (V_{BUS}, DP, DM and ID) and the V_{CC} pin. All the digital pins powered by $V_{CC(I/O)}$ are configured as high-impedance inputs. These pins must be driven to a defined state or terminated by using pull-up or pull-down resistors to avoid a floating input condition. Other pins are not powered.

9.1.1 Normal mode

In normal mode, both V_{CC} and $V_{CC(I/O)}$ are powered. Chip select is asserted. The ISP1704A is fully functional.

9.1.2 Power-down mode

When $V_{CC(I/O)}$ is not present or when chip select is deasserted, the ISP1704A is put into power-down mode. In this mode, internal regulators are powered down to keep the V_{CC} current to a minimum. The voltage on the V_{CC} pin will not leak to the $V_{CC(I/O)}$ and/or V_{BUS} pins. In this mode, the ISP1704A pin states are given in Table 8.

Table 8. Pin states in power-down mode

Pin name	Pin state when $V_{CC(I/O)}$ is not present	Pin state when chip select is deasserted
V_{CC}	3.0 V to 4.5 V	3.0 V to 4.5 V
$V_{CC(I/O)}$	not powered[1]	1.65 V to 1.95 V
CHIP_SEL, CHIP_SEL_N, CFG1, TEST_N, CLOCK, STP, NXT, DIR, DATA[7:0]	not powered[1]	high-Z
DP, DM, ID, REG1V8, REG3V3, CLKIN, i.c., RREF, PSW, FAULT, CHGR_DET_EN_N, CHGR_DET	not powered[1]	not powered[1]

[1] These pins must not be externally driven to HIGH. Otherwise, the ISP1704A behavior is undefined and leakage current will occur.

When $V_{CC(I/O)}$ is not present, all the digital pins that are powered by $V_{CC(I/O)}$ are not powered. Other pins are not powered.

When the ISP1704A is put into power-down mode by disabling chip select, all the digital pins that are powered by $V_{CC(I/O)}$ are configured as high-impedance inputs. These pins must be driven to defined states or terminated by using pull-up or pull-down resistors to avoid a floating input condition. Other pins are not powered. In this mode, minimum current will be drawn by $V_{CC(I/O)}$ to detect chip select status.

9.1.3 USB charger detection

The ISP1704A provides the USB charger detection function that complies with USB *Battery Charging Specification Rev. 1.0*. The ISP1704A implements the USB charger detection circuit as a peripheral. When the ISP1704A is used as a USB peripheral, it can distinguish between high-current charger (up to 1.8 A) and a standard USB host or hub (up to 500 mA). If a high-current charger is detected, the peripheral controller must determine whether the attached charger is a dedicated charger, a low-speed or full-speed host/hub charger, or a high-speed host/hub charger by turning on the DP pull-up resistor and attempting a USB connection to the charger. Depending on the attached charger type, the peripheral limits the current drawn, according to the battery charger specification. Figure 8 shows a typical system setup.

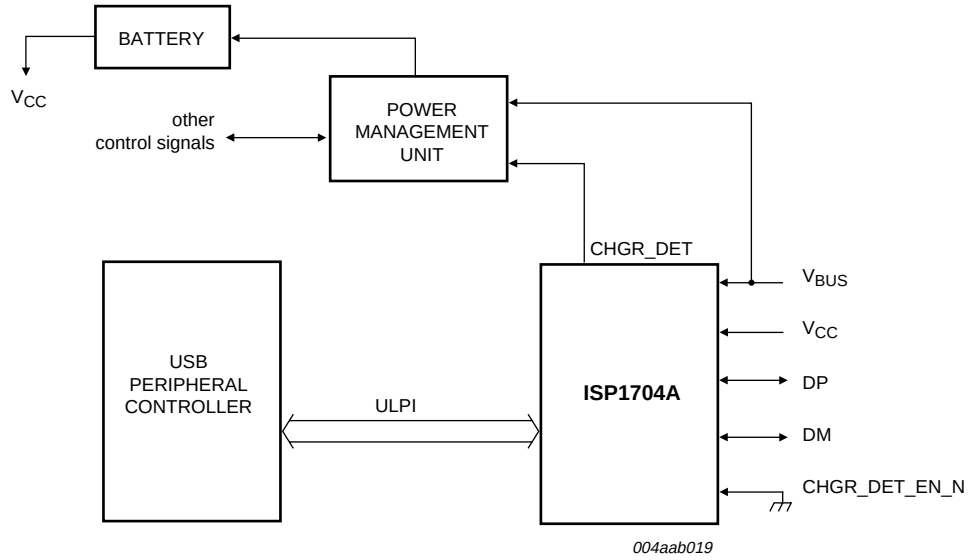


Fig 8. Charger detection setup

If a high-current charger is detected, the ISP1704A will drive the CHGR_DET pin to HIGH, communicating to the battery charger circuit to begin the charging process. This mechanism is automatically performed when the ISP1704A is in power-down mode (the chip select pin is deasserted or $V_{CC(I/O)}$ is lost), and under manual control when in synchronous mode (chip select is asserted).

During power-down mode, the ISP1704A begins charger detection after detecting that $V_{BUS} > V_{th(r)(VBUS)}$, by transmitting a sensing voltage (V_{DAT_SRC}) on DP, and monitoring if the charger drives a similar voltage on DM. If the ISP1704A detects $V_{DM} > V_{DAT\_REF}$, it sets the VDAT_DET register bit to logic 1. After internally debouncing VDAT_DET for a minimum of $t_{CHGR\_DET\_DBNC}$, the CHGR_DET pin is driven to HIGH to indicate the presence of a high-current charger.

The ISP1704A also provides the CHGR_DET_EN_N pin to enable or disable the automatic USB battery charging function. If CHGR_DET_EN_N is HIGH, the ISP1704A will not automatically try to detect the presence of an external USB battery charger during power-down mode. If CHGR_DET_EN_N is LOW, and when the ISP1704A is in power down-mode, on detecting $V_{BUS} > V_{th(r)(VBUS)}$, the ISP1704A will perform automatic USB

battery charger detection. The ISP1704A supports USB charger detection when used as a peripheral transceiver. When used as a host or an OTG A-device transceiver, it is recommended that the CHGR_DET_EN_N pin is deasserted.

When the CHGR_DET_EN_N pin is HIGH, it prevents automatic USB battery charger detection from occurring. However, if the application manually sets DPVSRC_EN = 1, the ISP1704A will still drive V_{DAT_SRC} on the DP line.

Once the charger detection procedure is completed and no charger is detected, the ISP1704A will pause for 1 second and start detection again. This procedure is repeated until a charger is detected.

While detecting the voltage on DM, the ISP1704A will perform an additional safety check by ensuring that the DM voltage is below $V_{th(se)}$ (see Table 59). If the DM voltage is greater than $V_{th(se)}$, then an illegal device is attached and the ISP1704A will not perform charger detection. The ISP1704A will wait for V_{BUS} to fall and rise again before re-attempting charger detection. An example is when a user plugs the standard-A end of the USB cable into a USB-to-PS2 adapter. This connects the B-device into the PS2 port of a PC, and causes V_{BUS} to be shorted to DP and DM, making the PS2 port act like a charger. Leakage on DP and DM when a PS2 adapter is connected is 300 µA (typical).

There is an internal RC circuit in the ISP1704A that oscillates at $f_{clk(int)lp}$. This clock is used by the state machine governing the charger detection. Frequency $f_{clk(int)lp}$ is divided down to a 1 kHz clock. The 1 kHz clock is used to meet timing requirements of the USB battery charger.

When disabling the DPVSRC_EN bit (manual charger detection is completed), the ISP1704A requires a minimum delay of 200 µs before the battery charger detection circuit is fully disabled. Software must wait 200 µs before enabling the DP pull up.

9.2 ULPI modes

The ISP1704A ULPI interface can be programmed to operate in five modes. In each mode, the signals on the data bus are reconfigured as described in the following subsections. Setting more than one mode will lead to undefined behavior.

9.2.1 Synchronous mode

This is default mode. On power-up, and when CLOCK is stable, the ISP1704A will enter synchronous mode.

In synchronous mode, the link must synchronize all ULPI signals to CLOCK, meeting the set-up and hold times as defined in Section 14.

This mode is used by the link to perform the following tasks:

- High-speed detection handshake (chirp)
- Transmit and receive USB packets
- Read and write to registers
- Receive USB status updates (RXCMDs) from the ISP1704A

Table 9. ULPI signal description

Signal name	Direction on the ISP1704A[1]	Signal description
CLOCK	O	**60 MHz interface clock**: When a clock is driven into the CLKIN pin, the ISP1704A will drive a 60 MHz output clock. During low-power, serial and UART modes, the clock can be turned off to save power.
DATA[7:0]	I/O	**8-bit data bus**: In synchronous mode, the link drives DATA[7:0] to LOW by default. The link initiates transfers by sending a nonzero data pattern called a TXCMD (transmit command). In synchronous mode, the direction of DATA[7:0] is controlled by DIR. Contents of DATA[7:0] lines must be ignored for exactly one clock cycle whenever DIR changes state. This is called a turnaround cycle. Data lines have fixed directions and different meanings in low-power, 3-pin serial and UART modes.
DIR	O	**Direction**: Controls the direction of data bus DATA[7:0]. In synchronous mode, the ISP1704A drives DIR to LOW by default, making the data bus an input so the ISP1704A can listen for TXCMD from the link. The ISP1704A drives DIR to HIGH only when it has data for the link. When DIR and NXT are HIGH, the byte on the data bus contains decoded USB data. When DIR is HIGH and NXT is LOW, the byte contains status information called an RXCMD (receive command). The only exception to this rule is when the PHY returns register read data, where NXT is also LOW, replacing the usual RXCMD byte. Every change in DIR causes a turnaround cycle on the data bus, during which DATA[7:0] are not valid and must be ignored by the link. DIR is always asserted during low-power, serial and UART modes.
STP	I	**Stop**: In synchronous mode, the link drives STP to HIGH for one cycle after the last byte of data is sent to the ISP1704A. The link can optionally assert STP to force DIR to be deasserted. In low-power, serial and UART modes, the link holds STP at HIGH to wake up the ISP1704A, causing the ULPI bus to return to synchronous mode.
NXT	O	**Next**: In synchronous mode, the ISP1704A drives NXT to HIGH to throttle data. If DIR is LOW, the ISP1704A asserts NXT to notify the link to place the next data byte on DATA[7:0] in the following clock cycle. If DIR is HIGH, the ISP1704A asserts NXT to notify the link that a valid USB data byte is on DATA[7:0] in the current cycle. The ISP1704A always drives an RXCMD when DIR is HIGH and NXT is LOW, unless register read data is to be returned to the link in the current cycle. NXT is not used in low-power, serial and UART modes.

[1] I = input; O = output; I/O = digital input/output.

9.2.2 Low-power mode

When the USB bus is idle, the link can place the ISP1704A into low-power mode (also called suspend mode). In low-power mode, the data bus definition changes to that shown in Table 10. To enter low-power mode, the link sets the SUSPENDM bit in the FUNC_CTRL register (see Section 10.5) to logic 0. To exit low-power mode, the link asserts the STP signal. After exiting low-power mode, the ISP1704A will send an RXCMD to the link if a change was detected in any interrupt source, and the change still exists. An RXCMD may not be sent if the interrupt condition is removed before exiting.

The ISP1704A will draw only suspend current from the V_{CC} supply; see Table 43.

During low-power mode, the clock on CLKIN may be stopped. The clock must be started again before asserting STP to exit low-power mode.

For more information on low-power mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 10. Signal mapping during low-power mode

Signal	Maps to	Direction[1]	Description
LINESTATE0	DATA0	O	combinatorial LINESTATE0 directly driven by the analog receiver
LINESTATE1	DATA1	O	combinatorial LINESTATE1 directly driven by the analog receiver
Reserved	DATA2	O	reserved; the ISP1704A will drive this pin to LOW
INT	DATA3	O	active-HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
Reserved	DATA[7:4]	O	reserved; the ISP1704A will drive these pins to LOW

[1] O = output.

9.2.3 6-pin full-speed or low-speed serial mode

If the link requires a 6-pin serial interface to transmit and receive full-speed or low-speed USB data, it can set the ISP1704A to 6-pin serial mode. In 6-pin serial mode, the data bus definition changes to that shown in Table 11. To enter 6-pin serial mode, the link sets the 6PIN_FSLS_SERIAL bit in the INTF_CTRL register (see Section 10.6) to logic 1. To exit 6-pin serial mode, the link asserts the STP signal. This is provided primarily for links that contain legacy full-speed or low-speed functionality, providing a more cost-effective upgrade path to high-speed functionality. An interrupt pin is also provided to inform the link of USB events. If the link requires CLOCK to be running during 6-pin serial mode, the CLOCK_SUSPENDM register bit must be set to logic 1 before entering 6-pin serial mode.

For more information on 6-pin serial mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 11. Signal mapping for 6-pin serial mode

Signal	Maps to	Direction[1]	Description
TX_ENABLE	DATA0	I	active-HIGH transmit enable
TX_DAT	DATA1	I	transmit differential data on DP and DM
TX_SE0	DATA2	I	transmit single-ended zero on DP and DM
INT	DATA3	O	active-HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
RX_DP	DATA4	O	single-ended receive data from DP
RX_DM	DATA5	O	single-ended receive data from DM
RX_RCV	DATA6	O	differential receive data from DP and DM
Reserved	DATA7	O	reserved; the ISP1704A will drive this pin to LOW

[1] I = input; O = output.

9.2.4 3-pin full-speed or low-speed serial mode

If the link requires a 3-pin serial interface to transmit and receive full-speed or low-speed USB data, it can set the ISP1704A to 3-pin serial mode. In 3-pin serial mode, the data bus definition changes to that shown in Table 12. To enter 3-pin serial mode, the link sets the 3PIN_FSLS_SERIAL bit in the INTF_CTRL register (see Section 10.6) to logic 1. To exit 3-pin serial mode, the link asserts the STP signal. This is provided primarily for links that contain legacy full-speed or low-speed functionality, providing a more cost-effective

upgrade path to high-speed functionality. An interrupt pin is also provided to inform the link of USB events. If the link requires CLOCK to be running during 3-pin serial mode, the CLOCK_SUSPENDM register bit must be set to logic 1 before entering 3-pin serial mode.

For more information on 3-pin serial mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 12. Signal mapping for 3-pin serial mode

Signal	Maps to	Direction[1]	Description
TX_ENABLE	DATA0	I	active-HIGH transmit enable
DAT	DATA1	I/O	transmit differential data on DP and DM when TX_ENABLE is HIGH receive differential data from DP and DM when TX_ENABLE is LOW
SE0	DATA2	I/O	transmit single-ended zero on DP and DM when TX_ENABLE is HIGH receive single-ended zero from DP and DM when TX_ENABLE is LOW
INT	DATA3	O	active-HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
Reserved	DATA[7:4]	O	reserved; the ISP1704A will drive these pins to LOW

[1] I = input; O = output; I/O = digital input/output.

9.2.5 Transparent UART mode

In transparent UART mode, the ISP1704A functions as a voltage level shifter between following pins:

- From pin DATA0 ($V_{CC(I/O)}$ level) to pin DM (2.7 V level).
- From pin DP (2.7 V level) to pin DATA1 ($V_{CC(I/O)}$ level).

The USB transceiver is used to drive the UART transmitting signal on the DM line. The rise time and the fall time of the transmitting signal is determined by whether a full-speed or low-speed transceiver is in use. It is recommended to use a low-speed transceiver if the UART bit rate is below 921 kbit/s for better EMI performance. If the UART bit rate is equal to or above 921 kbit/s, a full-speed transceiver can be used.

In transparent UART mode, data bus definitions change to that shown in Table 13.

Table 13. UART signal mapping

Signal	Maps to	Direction[1]	Description
TXD	DATA0	I	UART TXD signal that is routed to the DM pin
RXD	DATA1	O	UART RXD signal that is routed from the DP pin
Reserved	DATA2	O	reserved; the ISP1704A will drive this pin to LOW in UART mode
INT	DATA3	O	active-HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
Reserved	DATA[7:4]	O	reserved; the ISP1704A will drive these pins to LOW in UART mode

[1] I = input; O = output.

Transparent UART mode is entered by setting some ULPI register bits. The recommended sequence is:

1. Set the XCVRSELECT[1:0] bits in the FUNC_CTRL register (see Section 10.5) to 10b (low-speed) or 01b (full-speed). This setting affects the rise time and the fall time of the UART transmitting signal on the DM line.

2. Set the DP_PULLDOWN and DM_PULLDOWN bits in the OTG_CTRL register (see Section 10.7) to logic 0.
3. Set the TERMSELECT bit in the FUNC_CTRL register (see Section 10.5) to logic 0 (power-on default value).

   Remark: Mandatory when a full-speed driver is used and optional for a low-speed driver.
4. Set the TXD_EN and RXD_EN bits in the CARKIT_CTRL register (see Section 10.14) to logic 1. These two bits must be set together in one TXCMD.
5. Set the CARKIT_MODE bit in the INTF_CTRL register (see Section 10.6) to logic 1.

   Remark: The CARKIT_MODE, TXD_EN and RXD_EN bits must be set to logic 1. The sequence of setting these register bits is ignored.

After the register configuration is complete:

1. A weak pull-up resistor will be enabled on the DP and DATA0 pins. This is to avoid the possible floating condition on these input pins when UART mode is enabled.
2. The 39 Ω serial termination resistors on the DP and DM pins will be enabled.
3. One clock cycle after DIR goes from LOW to HIGH, the ISP1704A will drive the data bus for five clock cycles. This is to charge the DATA0 pin to a HIGH level for a slow link. However, the link can start driving DATA0 to HIGH immediately after the turnaround cycle.
4. UART buffers between DATA0 or DATA1 and DM or DP are enabled. Transparent UART mode is entered.

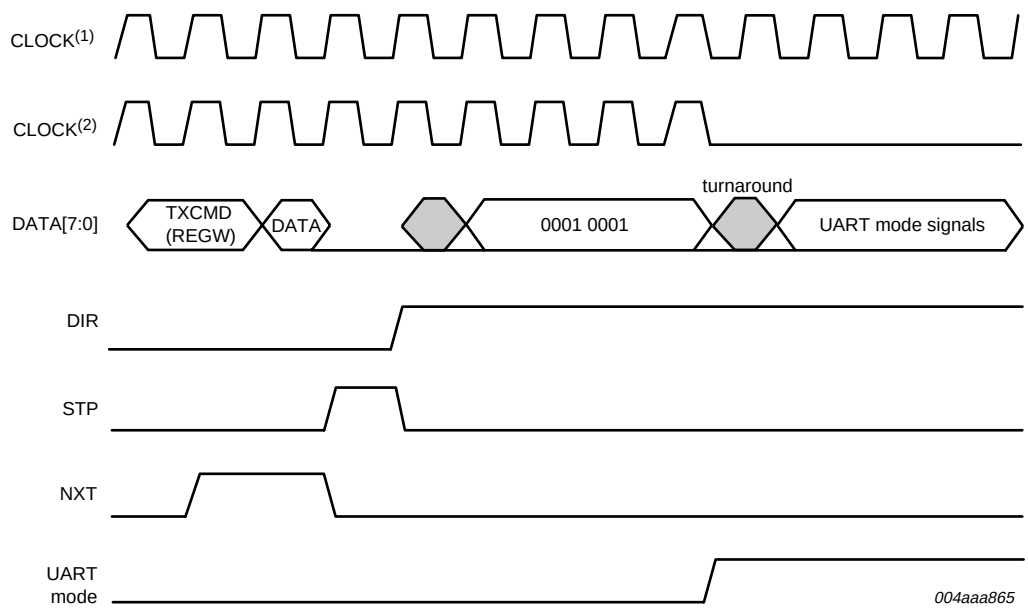
   Remark: The DP pin will be slowly charged up to HIGH by the weak pull-up resistor. The time needed depends on the capacitive loading on DP.

By default, the clock is powered down when the ISP1704A enters UART mode. If the link requires CLOCK to be running in UART mode, it can set the CLOCK_SUSPENDM bit in the INTF_CTRL register (see Section 10.6) to logic 1 before entering UART mode.

Transparent UART mode is exited by asserting the STP pin to HIGH or by toggling chip select.

The INT pin is asserted and latched whenever an unmasked interrupt event occurs. When the link detects INT as HIGH, it must wake-up the PHY from transparent UART mode by asserting STP. When the PHY is in synchronous mode, the link can read the USB_INTR_L register (see Section 10.11) to determine the source of the interrupt. Note that the ISP1704A does not implement optional Carkit Interrupt registers.

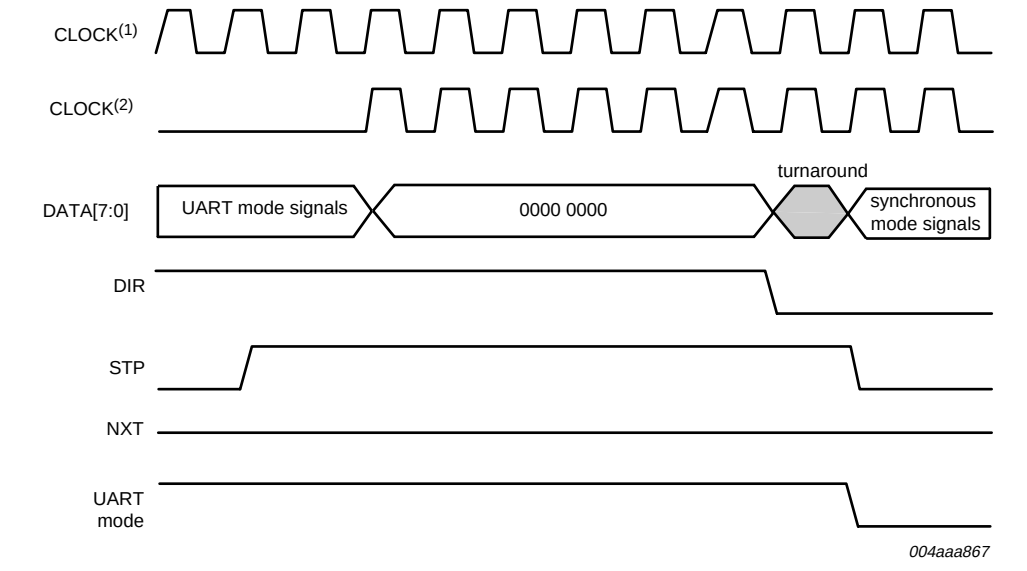
An alternative way to exit UART mode is to set chip select to deassert for more than t_{PWRDN} and then set it to assert. A power-on reset will be generated and the ULPI bus will be put in default synchronous mode.



(1) Clock remains powered when the CLOCK_SUSPENDM register bit is set to logic 1.

(2) Clock is powered down when the CLOCK_SUSPENDM register bit is logic 0 (default).

Fig 9. Interface behavior when entering UART mode



(1) Clock remains powered when the CLOCK_SUSPENDM register bit is set to logic 1.

(2) Clock is powered down when the CLOCK_SUSPENDM register bit is logic 0 (default).

Fig 10. Interface behavior when exiting UART mode

9.3 USB state transitions

A Hi-Speed USB peripheral, host or OTG device handles more than one electrical state as defined in *Universal Serial Bus Specification Rev. 2.0* and *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*. The ISP1704A accommodates various states through register settings of the XCVRSELECT[1:0], TERMSELECT, OPMODE[1:0], DP_PULLDOWN and DM_PULLDOWN bits.

Table 14 summarizes operating states. The values of register settings in Table 14 will force resistor settings as also given in Table 14. Resistor setting signals are defined as follows:

- RPU_DP_EN enables the 1.5 kΩ pull-up resistor on DP
- RPD_DP_EN enables the 15 kΩ pull-down resistor on DP
- RPD_DM_EN enables the 15 kΩ pull-down resistor on DM
- HSTERM_EN enables the 45 Ω termination resistors on DP and DM.

It is up to the link to set the desired register settings.

Table 14. Operating states and their corresponding resistor settings

Signaling mode	Register settings					Internal resistor settings			
	XCVR SELECT [1:0]	TERM SELECT	OPMODE [1:0]	DP_ PULL DOWN	DM_ PULL DOWN	RPU_DP _EN	RPD_DP _EN	RPD_ DM_EN	HS TERM_EN
General settings									
3-state drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b
Power up or V_{BUS} < $V_{B\_SESS\_END}$	01b	0b	00b	1b	1b	0b	1b	1b	0b
Host settings									
Host chirp	00b	0b	10b	1b	1b	0b	1b	1b	1b
Host high-speed	00b	0b	00b	1b	1b	0b	1b	1b	1b
Host full-speed	X1b	1b	00b	1b	1b	0b	1b	1b	0b
Host high-speed or full-speed suspend	01b	1b	00b	1b	1b	0b	1b	1b	0b
Host high-speed or full-speed resume	01b	1b	10b	1b	1b	0b	1b	1b	0b
Host low-speed	10b	1b	00b	1b	1b	0b	1b	1b	0b
Host low-speed suspend	10b	1b	00b	1b	1b	0b	1b	1b	0b
Host low-speed resume	10b	1b	10b	1b	1b	0b	1b	1b	0b
Host Test J or Test K	00b	0b	10b	1b	1b	0b	1b	1b	1b
Peripheral settings									
Peripheral chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b
Peripheral high-speed	00b	0b	00b	0b	0b	0b	0b	0b	1b
Peripheral full-speed	01b	1b	00b	0b	0b	1b	0b	0b	0b

Table 14. Operating states and their corresponding resistor settings *…continued*

Signaling mode	Register settings					Internal resistor settings			
	XCVR SELECT [1:0]	TERM SELECT	OPMODE [1:0]	DP_ PULL DOWN	DM_ PULL DOWN	RPU_DP _EN	RPD_DP _EN	RPD_ DM_EN	HS TERM_EN
Peripheral high-speed or full-speed suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b
Peripheral high-speed or full-speed resume	01b	1b	10b	0b	0b	1b	0b	0b	0b
Peripheral Test J or Test K	00b	0b	10b	0b	0b	0b	0b	0b	1b
OTG settings									
OTG device peripheral chirp	00b	1b	10b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed	00b	0b	00b	0b	1b	0b	0b	1b	1b
OTG device peripheral full-speed	01b	1b	00b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed and full-speed suspend	01b	1b	00b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed and full-speed resume	01b	1b	10b	0b	1b	1b	0b	1b	0b
OTG device peripheral Test J or Test K	00b	0b	10b	0b	1b	0b	0b	1b	1b

10. Register map

Table 15. Register map

Field name	Size (bit)	Address (6 bit)				References
		R[1]	W[2]	S[3]	C[4]	
VENDOR_ID_LOW	8	00h	-	-	-	Section 10.1 on page 29
VENDOR_ID_HIGH	8	01h	-	-	-	Section 10.2 on page 29
PRODUCT_ID_LOW	8	02h	-	-	-	Section 10.3 on page 30
PRODUCT_ID_HIGH	8	03h	-	-	-	Section 10.4 on page 30
FUNC_CTRL	8	04h to 06h	04h	05h	06h	Section 10.5 on page 30
INTF_CTRL	8	07h to 09h	07h	08h	09h	Section 10.6 on page 31
OTG_CTRL	8	0Ah to 0Ch	0Ah	0Bh	0Ch	Section 10.7 on page 32
USB_INTR_EN_R	8	0Dh to 0Fh	0Dh	0Eh	0Fh	Section 10.8 on page 33
USB_INTR_EN_F	8	10h to 12h	10h	11h	12h	Section 10.9 on page 34
USB_INTR_STAT	8	13h	-	-	-	Section 10.10 on page 35
USB_INTR_L	8	14h	-	-	-	Section 10.11 on page 35
DEBUG	8	15h	-	-	-	Section 10.12 on page 36
SCRATCH	8	16h to 18h	16h	17h	18h	Section 10.13 on page 36
CARKIT_CTRL	8	19h to 1Bh	19h	1Ah	1Bh	Section 10.14 on page 36
Reserved	8	1Ch to 3Ch				-
PWR_CTRL	8	3Dh to 3Fh	3Dh	3Eh	3Fh	Section 10.15 on page 37

[1] Read (R): A register can be read. Read-only if this is the only mode given.

[2] Write (W): The pattern on the data bus will be written over all bits of a register.

[3] Set (S): The pattern on the data bus is OR-ed with and written to a register.

[4] Clear (C): The pattern on the data bus is a mask. If a bit in the mask is set, then the corresponding register bit will be set to zero (cleared).

10.1 VENDOR_ID_LOW register

Table 16 shows the bit description of the register.

Table 16. VENDOR_ID_LOW - Vendor ID Low register (address R = 00h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	VENDOR_ID_LOW[7:0]	R	CCh*	**Vendor ID Low**: Lower byte of the NXP vendor ID supplied by USB-IF; fixed value of CCh

10.2 VENDOR_ID_HIGH register

Table 17 shows the bit description of the register.

Table 17. VENDOR_ID_HIGH - Vendor ID High register (address R = 01h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	VENDOR_ID_HIGH[7:0]	R	04h*	**Vendor ID High**: Upper byte of the NXP vendor ID supplied by USB-IF; fixed value of 04h

10.3 PRODUCT_ID_LOW register

The bit description of the register is given in Table 18.

Table 18. PRODUCT_ID_LOW - Product ID Low register (address R = 02h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	PRODUCT_ID_LOW[7:0]	R	04h*	**Product ID Low**: Lower byte of the NXP product ID number; fixed value of 04h

10.4 PRODUCT_ID_HIGH register

The bit description of the register is given in Table 19.

Table 19. PRODUCT_ID_HIGH - Product ID High register (address R = 03h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	PRODUCT_ID_HIGH[7:0]	R	17h*	**Product ID High**: Upper byte of the NXP product ID number; fixed value of 17h

10.5 FUNC_CTRL register

This register controls UTMI function settings of the PHY. The bit allocation of the register is given in Table 20.

Table 20. FUNC_CTRL - Function Control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	SUSPENDM	RESET	OPMODE[1:0]		TERM SELECT	XCVRSELECT[1:0]	
Reset	0	1	0	0	0	0	0	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 21. FUNC_CTRL - Function Control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit description

Bit	Symbol	Description
7	-	reserved
6	SUSPENDM	**Suspend LOW**: Active-LOW PHY suspend. Places the PHY into low-power mode. The PHY will power-down all blocks, except the full-speed receiver, OTG comparators and ULPI interface pins. To come out of low-power mode, the link must assert STP. The PHY will automatically clear this bit when it exits low-power mode. **0b —** Low-power mode **1b —** Powered
5	RESET	**Reset**: Active-HIGH transceiver reset. After the link sets this bit, the PHY will assert DIR and reset the digital core. This does not reset the ULPI interface or the ULPI register set. When the reset is completed, the PHY will deassert DIR and automatically clear this bit, followed by an RXCMD update to the link. The link must wait for DIR to deassert before using the ULPI bus. **0b —** Do not reset **1b —** Reset
4 to 3	OPMODE[1:0]	**Operation Mode**: Selects the required bit-encoding style during transmit. **00b —** Normal operation **01b —** Non-driving **10b —** Disable bit-stuffing and NRZI encoding **11b —** Do not automatically add SYNC and EOP when transmitting; must be used only for high-speed packets
2	TERMSELECT	**Termination Select**: Controls the internal 1.5 kΩ full-speed pull-up resistor and 45 Ω high-speed terminations. Control over bus resistors changes, depending on XCVRSELECT[1:0], OPMODE[1:0], DP_PULLDOWN and DM_PULLDOWN, as shown in Table 14.
1 to 0	XCVRSELECT [1:0]	**Transceiver Select**: Selects the required transceiver speed. **00b —** Enable the high-speed transceiver **01b —** Enable the full-speed transceiver **10b —** Enable the low-speed transceiver **11b —** Enable the full-speed transceiver for low-speed packets (full-speed preamble is automatically prefixed)

10.6 INTF_CTRL register

The INTF_CTRL register enables alternative interfaces. All of these modes are optional features provided for legacy link cores. Setting more than one of these fields results in undefined behavior. Table 22 provides the bit allocation of the register.

Table 22. INTF_CTRL - Interface Control register (address R = 07h to 09h, W = 07h, S = 08h, C = 09h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	INTF_ PROT_DIS	IND_PASS THRU	IND_ COMPL	reserved	CLOCK_ SUSPENDM	CARKIT_ MODE	3PIN_ FSLS_ SERIAL	6PIN_ FSLS_ SERIAL
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 23. INTF_CTRL - Interface Control register (address R = 07h to 09h, W = 07h, S = 08h, C = 09h) bit description

Bit	Symbol	Description
7	INTF_PROT_DIS	**Interface Protect Disable**: Controls circuitry built into the ISP1704A to protect the ULPI interface when the link 3-states STP and DATA[7:0]. When this bit is enabled, the ISP1704A will automatically detect when the link stops driving STP. **0b —** Enables the interface protect circuit. The ISP1704A attaches a weak pull-up resistor on STP. If STP is unexpectedly HIGH, the ISP1704A attaches weak pull-down resistors on DATA[7:0], protecting data inputs. **1b —** Disables the interface protect circuit, detaches weak pull-down resistors on DATA[7:0], and a weak pull-up resistor on STP.
6	IND_PASSTHRU	**Indicator Pass-through**: Controls whether the complement output is qualified with the internal A_VBUS_VLD comparator before being used in the V_{BUS} state in RXCMD. **0b —** The complement output signal is qualified with the internal A_VBUS_VLD comparator. **1b —** The complement output signal is not qualified with the internal A_VBUS_VLD comparator.
5	IND_COMPL	**Indicator Complement**: Informs the PHY to invert the FAULT input signal, generating the complement output. **0b —** The ISP1704A will not invert the FAULT signal. **1b —** The ISP1704A will invert the FAULT signal.
4	-	reserved
3	CLOCK_SUSPENDM	**Clock Suspend LOW**: Active-LOW clock suspend. Powers down the internal clock circuitry only. By default, the clock will not be powered in 6-pin serial mode or 3-pin serial mode. Valid only in 6-pin serial mode and 3-pin serial mode. Valid only when SUSPENDM is set to logic 1, otherwise this bit is ignored. **0b —** Clock will not be powered in 3-pin or 6-pin serial mode, or UART mode. **1b —** Clock will be powered in 3-pin and 6-pin serial mode, or UART mode.
2	CARKIT_MODE	**Carkit Mode**: Changes the ULPI interface to the carkit interface (UART mode). Bits TXD_EN and RXD_EN in the CARKIT_CTRL register (see Section 10.14) must change as well. The PHY must automatically clear this bit when carkit mode is exited. **0b —** Disable carkit mode. **1b —** Enable carkit mode.
1	3PIN_FSLS_SERIAL	**3-Pin Full-Speed Low-Speed Serial Mode**: Changes the ULPI interface to a 3-bit serial interface. The ISP1704A will automatically clear this bit when 3-pin serial mode is exited. **0b —** Full-speed or low-speed packets are sent using the parallel interface. **1b —** Full-speed or low-speed packets are sent using the 3-pin serial interface.
0	6PIN_FSLS_SERIAL	**6-Pin Full-Speed Low-Speed Serial Mode**: Changes the ULPI interface to a 6-bit serial interface. The ISP1704A will automatically clear this bit when 6-pin serial mode is exited. **0b —** Full-speed or low-speed packets are sent using the parallel interface. **1b —** Full-speed or low-speed packets are sent using the 6-pin serial interface.

10.7 OTG_CTRL register

This register controls various OTG functions of the ISP1704A. The bit allocation of the OTG_CTRL register is given in Table 24.

Table 24. OTG_CTRL - OTG Control register (address R = 0Ah to 0Ch, W = 0Ah, S = 0Bh, C = 0Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	USE_EXT_VBUS_IND	DRV_VBUS_EXT	reserved	CHRG_VBUS	DISCHRG_VBUS	DM_PULLDOWN	DP_PULLDOWN	ID_PULLUP[1]
Reset	0	0	0	0	0	1	1	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

[1] A weak pull up, which can detect ID correctly, is present when the ID_PULLUP bit is disabled. It is, however, mandatory that the link enables ID_PULLUP.

Table 25. OTG_CTRL - OTG Control register (address R = 0Ah to 0Ch, W = 0Ah, S = 0Bh, C = 0Ch) bit description

Bit	Symbol	Description
7	USE_EXT_VBUS_IND	**Use External V_{BUS} Indicator**: Informs the PHY to use an external V_{BUS} overcurrent indicator. **0b —** Use the internal OTG comparator **1b —** Use the external V_{BUS} valid indicator signal input from the FAULT pin
6	DRV_VBUS_EXT	**Drive V_{BUS} External**: Controls the external charge pump or 5 V supply by the PSW pin. **0b —** PSW is LOW **1b —** PSW is HIGH
5	reserved	-
4	CHRG_VBUS	**Charge V_{BUS}**: Charges V_{BUS} through a resistor. Used for the V_{BUS} pulsing of SRP. The link must first check that V_{BUS} is discharged (see bit DISCHRG_VBUS), and that both the DP and DM data lines have been LOW (SE0) for 2 ms. **0b —** Do not charge V_{BUS} **1b —** Charge V_{BUS}
3	DISCHRG_VBUS	**Discharge V_{BUS}**: Discharges V_{BUS} through a resistor. If the link sets this bit to logic 1, it waits for an RXCMD indicating that SESS_END has changed from logic 0 to logic 1, and then resets this bit to logic 0 to stop the discharge. **0b —** Do not discharge V_{BUS} **1b —** Discharge V_{BUS}
2	DM_PULLDOWN	**DM Pull Down**: Enables the 15 kΩ pull-down resistor on DM. **0b —** Pull-down resistor is not connected to DM **1b —** Pull-down resistor is connected to DM
1	DP_PULLDOWN	**DP Pull Down**: Enables the 15 kΩ pull-down resistor on DP. **0b —** Pull-down resistor is not connected to DP **1b —** Pull-down resistor is connected to DP
0	ID_PULLUP	**ID Pull Up**: Connects a pull-up to the ID line and enables sampling of the ID level. Disabling the ID line sampler will reduce the PHY power consumption. **0b —** Disable sampling of the ID line **1b —** Enable sampling of the ID line

10.8 USB_INTR_EN_R register

The bits in this register enable interrupts and RXCMDs to be sent when the corresponding bits in the USB_INTR_STAT register change from logic 0 to logic 1. By default, all transitions are enabled. Table 26 shows the bit allocation of the register.

Table 26. USB_INTR_EN_R - USB Interrupt Enable Rising register (address R = 0Dh to 0Fh, W = 0Dh, S = 0Eh, C = 0Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND_R	SESS_END_R	SESS_VALID_R	VBUS_VALID_R	HOST_DISCON_R
Reset	0	0	0	1	1	1	1	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 27. USB_INTR_EN_R - USB Interrupt Enable Rising register (address R = 0Dh to 0Fh, W = 0Dh, S = 0Eh, C = 0Fh) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND_R	**ID Ground Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on ID_GND.
3	SESS_END_R	**Session End Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on SESS_END.
2	SESS_VALID_R	**Session Valid Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on SESS_VLD.
1	VBUS_VALID_R	**V_{BUS} Valid Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on A_VBUS_VLD.
0	HOST_DISCON_R	**Host Disconnect Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on HOST_DISCON.

10.9 USB_INTR_EN_F register

The bits in this register enable interrupts and RXCMDs to be sent when the corresponding bits in the USB_INTR_STAT register change from logic 1 to logic 0. By default, all transitions are enabled. See Table 28.

Table 28. USB_INTR_EN_F - USB Interrupt Enable Falling register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND_F	SESS_END_F	SESS_VALID_F	VBUS_VALID_F	HOST_DISCON_F
Reset	0	0	0	1	1	1	1	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 29. USB_INTR_EN_F - USB Interrupt Enable Falling register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND_F	**ID Ground Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on ID_GND.
3	SESS_END_F	**Session End Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on SESS_END.

Table 29. USB_INTR_EN_F - USB Interrupt Enable Falling register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit description *…continued*

Bit	Symbol	Description
2	SESS_VALID_F	**Session Valid Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on SESS_VLD.
1	VBUS_VALID_F	**V_{BUS} Valid Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on A_VBUS_VLD.
0	HOST_DISCON_F	**Host Disconnect Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on HOST_DISCON.

10.10 USB_INTR_STAT register

This register (see Table 30) indicates the current value of the interrupt source signal.

Table 30. USB_INTR_STAT - USB Interrupt Status register (address R = 13h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND	SESS_END	SESS_VALID	VBUS_VALID	HOST_DISCON
Reset	X	X	X	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 31. USB_INTR_STAT - USB Interrupt Status register (address R = 13h) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND	**ID Ground**: Reflects the current value of the ID detector circuit.
3	SESS_END	**Session End**: Reflects the current value of the session end voltage comparator.
2	SESS_VALID	**Session Valid**: Reflects the current value of the session valid voltage comparator.
1	VBUS_VALID	**V_{BUS} Valid**: Reflects the current value of the V_{BUS} valid voltage comparator.
0	HOST_DISCON	**Host Disconnect**: Reflects the current value of the host disconnect detector.

10.11 USB_INTR_L register

The bits of the USB_INTR_L register are automatically set by the ISP1704A when an unmasked change occurs on the corresponding interrupt source signal. The ISP1704A will automatically clear all bits when the link reads this register, or when the PHY enters low-power mode.

Remark: It is optional for the link to read this register when the clock is running because all signal information will automatically be sent to the link through the RXCMD byte.

The bit allocation of this register is given in Table 32.

Table 32. USB_INTR_L - USB Interrupt Latch register (address R = 14h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ID_GND_L	SESS_END_L	SESS_VALID_L	VBUS_VALID_L	HOST_DISCON_L
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 33. USB_INTR_L - USB Interrupt Latch register (address R = 14h) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	ID_GND_L	**ID Ground Latch**: Automatically set when an unmasked event occurs on ID_GND. Cleared when this register is read.
3	SESS_END_L	**Session End Latch**: Automatically set when an unmasked event occurs on SESS_END. Cleared when this register is read.
2	SESS_VALID_L	**Session Valid Latch**: Automatically set when an unmasked event occurs on SESS_VLD. Cleared when this register is read.
1	VBUS_VALID_L	**V_{BUS} Valid Latch**: Automatically set when an unmasked event occurs on A_VBUS_VLD. Cleared when this register is read.
0	HOST_DISCON_L	**Host Disconnect Latch**: Automatically set when an unmasked event occurs on HOST_DISCON. Cleared when this register is read.

10.12 DEBUG register

The bit allocation of the DEBUG register is given in Table 34. This register indicates the current value of signals useful for debugging.

Table 34. DEBUG - Debug register (address R = 15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						LINE STATE1	LINE STATE0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 35. DEBUG - Debug register (address R = 15h) bit description

Bit	Symbol	Description
7 to 2	-	reserved
1	LINESTATE1	**Line State 1**: Contains the current value of LINESTATE 1.
0	LINESTATE0	**Line State 0**: Contains the current value of LINESTATE 0.

10.13 SCRATCH register

This is a 1-byte empty register for testing purposes, see Table 36.

Table 36. SCRATCH - Scratch register (address R = 16h to 18h, W = 16h, S = 17h, C = 18h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	SCRATCH[7:0]	R/W/S/C	00h	**Scratch**: This is an empty register byte for testing purposes. Software can read, write, set and clear this register. The functionality of the PHY will not be affected.

10.14 CARKIT_CTRL register

This register controls transparent UART mode. This register is only valid when the CARKIT_MODE bit in the INTF_CTRL register (see Section 10.6) is set. When entering UART mode, set the CARKIT_MODE bit, and then set the TXD_EN and RXD_EN bits. After entering UART mode, the ULPI interface is not available. When exiting UART mode, assert the STP pin or perform a hardware reset using chip select.

For bit allocation, see Table 37.

Table 37. CARKIT_CTRL - Carkit Control register (address R = 19h to 1Bh, W = 19h, S = 1Ah, C = 1Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				RXD_EN	TXD_EN	reserved	
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 38. CARKIT_CTRL - Carkit Control register (address R = 19h to 1Bh, W = 19h, S = 1Ah, C = 1Bh) bit description

Bit	Symbol	Description
7 to 4	-	reserved; the link must never write logic 1 to these bits
3	RXD_EN	**RXD Enable**: Routes the UART RXD signal from the DP pin to the DATA1 pin. This bit will automatically be cleared when UART mode is exited.
2	TXD_EN	**TXD Enable**: Routes the UART TXD signal from the DATA0 pin to the DM pin. This bit will automatically be cleared when UART mode is exited.
1 to 0	-	reserved; the link must never write logic 1 to these bits

10.15 PWR_CTRL register

This vendor-specific register controls the power feature of the ISP1704A. The bit allocation of the register is given in Table 39.

Table 39. PWR_CTRL - Power Control register (address R = 3Dh to 3Fh, W = 3Dh, S = 3Eh, C = 3Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	HW DETECT	DPVSRC _EN	VDAT_DET	DP_WKPU _EN	BVALID_ FALL	BVALID_ RISE	DET_ COMP	SW CONTROL
Reset	0	0	X	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R	R/W/S/C	R/W/S/C	R/W/S/C	R	R/W/S/C

Table 40. PWR_CTRL - Power Control register (address R = 3Dh to 3Fh, W = 3Dh, S = 3Eh, C = 3Fh) bit description

Bit	Symbol	Description
7	HW DETECT	**Hardware Detect**: When SWCONTROL = 0: The HWDETECT bit is read only. This bit indicates if the transceiver is connected to a charger (dedicated charger, or host or hub charger). Valid only when DET_COMP is logic 1. **0b —** No charger detected. **1b —** Charger detected. When SWCONTROL = 1: The HWDETECT bit is writable. This bit allows manual control over the logic levels on the CHGR_DET pin. **0b —** CHGR_DET is pulled LOW. **1b —** CHGR_DET is driven to HIGH. Not reset by soft reset.
6	DPVSRC_EN	**DP Voltage Source Enable**: This bit controls whether DP is allowed to send V_{DAT_SRC}, which is a sensing voltage for charger detection. This bit also enables I_{DAT_SINK} on DM and V_{DAT_REF}. (Used when manual control over the charger detection is needed.) **0b —** No transmission of sensing voltage is performed. I_{DAT_SINK} and V_{DAT_REF} are disabled. **1b —** DP transmits sensing voltage; enables I_{DAT_SINK} and V_{DAT_REF}. After disabling the DP voltage source, software must wait for 200 µs before enabling DP pull up.
5	VDAT_DET	**V_{DAT} Detect**: This bit indicates the presence of voltage level higher then V_{DAT_REF} on the DM line. (Used when manual control over the charger detection is needed.) **0b —** Voltage on DM is lower then V_{DAT_REF}. **1b —** Voltage on DM is higher the V_{DAT_REF}.
4	DP_WKPU_EN	**DP Weak Pull-Up Enable**: Enables the weak pull-up resistor on the DP pin ($R_{weakUP(DP)}$) in synchronous mode when V_{BUS} is above the $V_{A\_SESS\_VLD}$ threshold. Note that when the ISP1704A is in UART mode, the DP weak pull-up will be enabled, regardless of the value of this register bit. **0b —** DP weak pull-up is disabled. **1b —** DP weak pull-up is enabled when $V_{BUS} > V_{A\_SESS\_VLD}$.
3	BVALID_FALL	**BVALID Fall**: Enables RXCMDs for HIGH-to-LOW transitions on BVALID. When BVALID changes from HIGH to LOW, the ISP1704A will send an RXCMD to the link with the ALT_INT bit set to logic 1. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.
2	BVALID_RISE	**BVALID Rise**: Enables RXCMDs for LOW-to-HIGH transitions on BVALID. When BVALID changes from LOW to HIGH, the ISP1704A will send an RXCMD to the link with the ALT_INT bit set to logic 1. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.
1	DET_COMP	**Detection Complete**: This bit indicates whether the automatic detection of a USB charger is completed. **0b —** Automatic detection of the USB charger is not completed. Manual USB battery charger detection is required. **1b —** Automatic detection of the USB charger is completed. Manual USB battery charger detection is not needed.
0	SW CONTROL	**Software Control**: This bit controls whether the CHGR_DET pin is controlled automatically or manually. When manual control is required, the software must set the SWCONTROL bit to logic 1 in the first register access, followed by issuing a second register access to set or clear the HWDETECT bit. Software must never set the SWCONTROL bit and change the HWDETECT bit in the same register access. Otherwise undefined behavior will result. **0b —** The CHGR_DET pin will be asserted or deasserted depending on the automatic USB charger detection result. **1b —** The CHGR_DET pin will be asserted or deasserted depending on the HWDETECT bit setting.

11. Limiting values

Table 41. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+5.5	V
$V_{CC(I/O)}$	input/output supply voltage			–0.5	+2.5	V
V_I	input voltage	on pins PSW, FAULT and CHGR_DET_EN_N		–0.5	+5.5	V
		on pins STP, DATA[7:0], CFG1, TEST_N, CHIP_SEL and CHIP_SEL_N		–0.5	$V_{CC(I/O)}$ + 0.5	V
		on pin ID		–0.5	+4.6	V
		on pin CLKIN		–0.5	+2.5	V
		on pins DP and DM	[1]	–0.5	+4.6	V
		on pin V_{BUS}	[2]	–0.5	+5.5	V
V_{ESD}	electrostatic discharge voltage	human body model (JESD22-A114D)		–2	+2	kV
		machine model (JESD22-A115-A)		–200	+200	V
		charge device model (JESD22-C101-A)		–500	+500	V
		IEC 61000-4-2 contact on pins DP and DM	[3]	–8	+8	kV
I_{lu}	latch-up current			-	100	mA
T_{stg}	storage temperature			–60	+125	°C

[1] The ISP1704A has been tested according to the additional requirements listed in *Universal Serial Bus Specification Rev. 2.0, Section 7.1.1*. The AC stress test was performed for 24 hours. The ISP1704A was found to be fully operational after the test completed. The ISP1704A was found to be fully functional after shorting the high-speed DP and DM pins to ground for 24 hours. Transmit and receive were occurring 50 % of the time.

[2] When an external series resistor is added to the V_{BUS} pin, it can withstand higher voltages for longer periods of time because the resistor limits the current flowing into the V_{BUS} pin. For example, with an external 1 kΩ resistor, V_{BUS} can tolerate 10 V for at least 5 seconds. Actual performance may vary depending on the resistor used and whether other components are connected to V_{BUS}.

[3] The ISP1704A has been tested in-house according to the IEC 61000-4-2 standard on the DP and DM pins. It is recommended that customers perform their own ESD tests, depending on application requirements.

12. Recommended operating conditions

Table 42. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	chip select is asserted	3.0	3.6	4.5	V
		chip select is deasserted or $V_{CC(I/O)}$ is lost; automatic charger detection will operate within this voltage range	2.4	3.6	4.5	V
$V_{CC(I/O)}$	input/output supply voltage		1.65	1.8	1.95	V
V_I	input voltage	on pins PSW, FAULT, V_{BUS} and CHGR_DET_EN_N	0	-	5.25	V
		on pins STP, DATA[7:0], CFG1, CHIP_SEL, CHIP_SEL_N and TEST_N	0	-	$V_{CC(I/O)}$	V
		on pins DP, DM and ID	0	-	3.6	V
		on pin CLKIN	0	-	1.95	V
T_j	junction temperature		–40	-	+125	°C
T_{amb}	ambient temperature		–40	+25	+85	°C

13. Static characteristics

Table 43. Static characteristics: supply pins

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{POR(trip)}$	power-on reset trip voltage	on REG1V8 pin		0.95	-	1.5	V
I_{CC}	supply current	power-down mode ($V_{CC(I/O)}$ is lost or chip select is deasserted)		-	5.5	16	µA
		full-speed transceiver; bus idle; no USB activity		-	13	-	mA
		high-speed transceiver; bus idle; no USB activity		-	34	-	mA
		low-power mode (bit SUSPENDM = 0b)	[1]	-	70	150	µA
		UART mode; low-speed transceiver; idle		-	750	-	µA
		UART mode; full-speed transceiver; idle		-	600	-	µA
		no V_{BUS} present		-	5.5	16	µA
		during charger detection; $V_{BUS} > V_{th(trig)r(VBUS)}$		-	0.9	1.7	mA
		after charger is detected or DM > $V_{th(se)}$		-	0.75	1.5	mA
I_{VBUS}	current on pin V_{BUS}	during suspend mode		-	60	90	µA
$I_{CC(I/O)}$	supply current on pin $V_{CC(I/O)}$	power-down mode (chip select is deasserted)		-	-	2	µA
		suspend mode		-	-	2	µA
		ULPI bus idle; 15 pF load on pin CLOCK	[2]	-	1.7	-	mA

[1] When the transceiver is configured as a peripheral controller, the 1.5 kΩ pull-up resistor on the device side will be connected to a 15 kΩ pull-down resistor on the host side according to *Universal Serial Bus Specification Rev. 2.0*. There will be an additional suspend current of 168.54 µA (minimum) to 229.67 µA (maximum).

[2] The actual value of $I_{CC(I/O)}$ varies depending on the capacitance loading, interface voltage and bus activity. Use the value provided here only as a reference.

Table 44. Static characteristics: digital pins

Digital pins: CLOCK, DIR, STP, NXT, DATA[7:0], CHIP_SEL, CHIP_SEL_N, CFG1 and TEST_N; unless otherwise specified.
V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC(I/O)}$	-	-	V
I_{LI}	input leakage current		−1	-	+1	µA
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = −2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = +2 mA	$V_{CC(I/O)}$ − 0.4	-	-	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{CC(I/O)}$ − 0.4 V	−4.8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4.2	-	-	mA

Table 44. Static characteristics: digital pins *...continued*

Digital pins: CLOCK, DIR, STP, NXT, DATA[7:0], CHIP_SEL, CHIP_SEL_N, CFG1 and TEST_N; unless otherwise specified.
V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Impedance						
Z_L	load impedance		45	-	65	Ω
Pull-up and pull-down						
I_{pd}	pull-down current	interface protect enabled; DATA[7:0] pins only; $V_I = V_{CC(I/O)}$	25	50	90	µA
I_{pu}	pull-up current	interface protect enabled; STP pin only; V_I = 0 V	–30	–50	–80	µA
		UART mode; DATA0 pin only	–28	–50	–80	µA
Capacitance						
C_{in}	input capacitance		2.7	3.0	3.5	pF

Table 45. Static characteristics: digital pins CHGR_DET_EN_N and FAULT

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
I_{IL}	LOW-level input current	V_I = 0 V	-	-	1	µA
I_{IH}	HIGH-level input current	V_I = 5.25 V	-	-	1	µA

Table 46. Static characteristics: digital pin PSW

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output levels						
V_{OH}	HIGH-level output voltage	external pull-down resistor connected	3.0[1]	-	5.25	V
I_{OH}	HIGH-level output current	external pull-down resistor connected	-	-	4	mA

[1] When V_{OH} is less than REG3V3, I_{CC} may increase because of the cross current.

Table 47. Static characteristics: analog pins (DP, DM)

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Original USB transceiver (full-speed and low-speed)						
Input levels						
V_{DI}	differential input sensitivity voltage	$\lvert V_{DP} - V_{DM} \rvert$	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	0.8	-	2.5	V
Input levels (single-ended receivers)						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V

Table 47. Static characteristics: analog pins (DP, DM) *…continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output levels						
V_{OL}	LOW-level output voltage	pull-up on pin DP; R_L = 1.5 kΩ to 3.6 V	0.0	-	0.3	V
V_{OH}	HIGH-level output voltage	pull-down on pins DP and DM; R_L = 15 kΩ to GND	2.8	-	3.6	V
V_{CRS}	output signal crossover voltage	excluding the first transition from the idle state	1.3	-	2.0	V
Termination						
V_{TERM}	termination voltage for upstream facing port pull-up	for 1.5 kΩ pull-up resistor	3.0	-	3.6	V
Resistance						
$R_{UP(DP)}$	pull-up resistance on pin DP		1425	1500	1575	Ω
$R_{weakUP(DP)}$	weak pull-up resistance on pin DP	bit DP_WKPU_EN = 1b and $V_{BUS} > V_{A\_SESS\_VLD}$	100	125	150	kΩ
High-speed USB transceiver (HS)						
Input levels						
V_{HSSQ}	high-speed squelch detection threshold voltage (differential signal amplitude)		100	-	150	mV
V_{HSDSC}	high-speed disconnect detection threshold voltage (differential signal amplitude)		525	-	625	mV
V_{HSDI}	high-speed differential input sensitivity	$\lvert V_{DP} - V_{DM} \rvert$	300	-	-	mV
V_{HSCM}	high-speed data signaling common mode voltage range (guideline for receiver)	includes V_{DI} range	−50	-	+500	mV
Output levels						
V_{HSOI}	high-speed idle level voltage		−10	-	+10	mV
V_{HSOL}	high-speed data signaling LOW-level voltage		−10	-	+10	mV
V_{HSOH}	high-speed data signaling HIGH-level voltage		360	-	440	mV
V_{CHIRPJ}	Chirp J level (differential voltage)		700	-	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)		−900	-	−500	mV
Leakage current						
I_{LZ}	off-state leakage current		−1.0	-	+1.0	µA
Capacitance						
C_{in}	input capacitance	pin to GND	-	-	5	pF
Resistance						
$R_{DN(DP)}$	pull-down resistance on pin DP		14.25	15	15.75	kΩ
$R_{DN(DM)}$	pull-down resistance on pin DM		14.25	15	15.75	kΩ
Termination						
$Z_{O(drv)(DP)}$	driver output impedance on pin DP	steady-state drive	40.5	45	49.5	Ω

Table 47. Static characteristics: analog pins (DP, DM) *...continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Z_{O(drv)(DM)}$	driver output impedance on pin DM	steady-state drive	40.5	45	49.5	Ω
Z_{INP}	input impedance exclusive of pull-up/pull-down (for low-/full-speed)		1	-	-	MΩ
UART mode						
Input levels						
V_{IL}	LOW-level input voltage	pin DP	0	-	0.8	V
V_{IH}	HIGH-level input voltage	pin DP	2.35	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	pin DM; I_{OL} = −4 mA	-	-	0.3	V
V_{OH}	HIGH-level output voltage	pin DM; I_{OH} = +4 mA	2.4	-	-	V

Table 48. Static characteristics: analog pin V_{BUS}

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Comparators						
$V_{A\_VBUS\_VLD}$	A-device V_{BUS} valid voltage		4.4	4.55	4.75	V
$V_{A\_SESS\_VLD}$	A-device session valid voltage	for A-device and B-device	0.8	1.6	2.0	V
$V_{hys(A\_SESS\_VLD)}$	A-device session valid hysteresis voltage	for A-device and B-device	-	100	-	mV
$V_{B\_SESS\_END}$	B-device session end voltage		0.2	-	0.8	V
Resistance						
$R_{UP(VBUS)}$	pull-up resistance on pin V_{BUS}	connect to REG3V3 when CHRG_VBUS = 1b	281	680	-	Ω
$R_{DN(VBUS)}$	pull-down resistance on pin V_{BUS}	connect to GND when DISCHRG_VBUS = 1b	656	1200	-	Ω
$R_{I(idle)(VBUS)}$	idle input resistance on pin V_{BUS}	not in power-down mode	80	90	100	kΩ
		during charger detection; chip deasserted or $V_{CC(I/O)}$ lost (power-down mode)	40	-	100	kΩ
		$V_{CC(I/O)}$ lost (power-down mode)	144	-	216	kΩ

Table 49. Static characteristics: ID detection circuit

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ID}	ID detection time		50	-	-	ms
$V_{th(ID)}$	ID detector threshold voltage		1.0	-	2.0	V
$R_{UP(ID)}$	ID pull-up resistance	bit ID_PULLUP = 1b	40	50	60	kΩ
$R_{weakPU(ID)}$	weak pull-up resistance on pin ID	bit ID_PULLUP = 0b	320	400	480	kΩ
$V_{PU(ID)}$	pull-up voltage on pin ID		3.0	3.3	3.6	V

Table 50. Static characteristics: regulator

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(REG1V8)}$	output voltage from internal 1.8 V regulator	SUSPENDM = 1b	1.65	1.8	1.95	V
$V_{O(REG3V3)}$	output voltage from internal 3.3 V regulator	SUSPENDM = 1b; not in UART mode	V_{CC} − 0.08	3.3	3.6	V
		SUSPENDM = 1b; in UART mode	2.5	2.77	2.9	V

Table 51. Static characteristics: pin CLKIN

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage		-	-	0.37	V
V_{IH}	HIGH-level input voltage		1.32	-	-	V

14. Dynamic characteristics

Table 52. Dynamic characteristics: reset and power

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{W(POR)}$	internal power-on reset pulse width		0.2	-	-	µs
$t_{w(REG1V8\_H)}$	REG1V8 HIGH pulse width		-	-	2	µs
$t_{w(REG1V8\_L)}$	REG1V8 LOW pulse width		-	-	11	µs
$t_{startup(PLL)}$	PLL start-up time	measured after $t_{d(det)clk(osc)}$	-	-	640	µs
$t_{d(det)clk(osc)}$	oscillator clock detector delay	measured from regulator start-up time	-	-	640	µs
t_{PWRUP}	regulator start-up time	4.7 µF ± 20 % capacitor each on pins REG1V8 and REG3V3	-	-	1	ms
t_{PWRDN}	regulator power-down time	4.7 µF ± 20 % capacitor each on pins REG1V8 and REG3V3	-	-	100	ms

Table 53. Dynamic characteristics: clock applied to pin CLKIN

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{i(CLKIN)}$	input frequency on pin CLKIN	pin CFG1 = HIGH		-	26.000	-	MHz
		pin CFG1 = LOW		-	19.200	-	MHz
$t_{jit(i)(CLKIN)RMS}$	RMS input jitter time on pin CLKIN			-	-	200	ps
$\Delta f_{i(CLKIN)}$	input frequency variation on pin CLKIN			-	-	200	ppm
$\delta_{i(CLKIN)}$	input duty cycle on pin CLKIN	for the first transaction	[1]	-	50	-	%
$t_{r(CLKIN)}$	rise time on pin CLKIN	only for square wave input		-	-	5	ns
$t_{f(CLKIN)}$	fall time on pin CLKIN	only for square wave input		-	-	5	ns

[1] The internal PLL is triggered only on the positive edge of the CLKIN input. Therefore, the duty cycle is not critical.

Table 54. Dynamic characteristics: reset and clock

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	CLOCK pin transitioning between 10 % to 90 % of $V_{CC(I/O)}$ (20 pF load)	-	-	4.0	ns
t_f	fall time	CLOCK pin transitioning between 90 % to 10 % of $V_{CC(I/O)}$ (20 pF load)	-	-	4.4	ns

Table 54. Dynamic characteristics: reset and clock *…continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{o(AV)(CLOCK)}$	average output frequency on pin CLOCK		59.970	60.000	60.030	MHz
$t_{jit(o)(CLOCK)RMS}$	RMS output jitter on pin CLOCK		-	-	500	ps
$\delta_{o(CLOCK)}$	output clock duty cycle on pin CLOCK		40	50	60	%

Table 55. Dynamic characteristics: digital I/O pins

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	output pins transitioning between 10 % to 90 % of $V_{CC(I/O)}$ (20 pF load)	-	-	4.0	ns
t_f	fall time	output pins transitioning between 90 % to 10 % of $V_{CC(I/O)}$ (20 pF load)	-	-	4.4	ns
t_{su}	set-up time	set-up time with respect to the positive edge of CLOCK; input-only pin (STP) and bidirectional pins (DATA[7:0]) as inputs	6.0	-	-	ns
t_h	hold time	hold time with respect to the positive edge of CLOCK; input-only pin (STP) and bidirectional pins (DATA[7:0]) as inputs	0.0	-	-	ns
$t_{d(o)}$	output delay time	output delay with respect to the positive edge of CLOCK; output-only pins (DIR, NXT)	-	-	9.0	ns
		output delay with respect to the positive edge of CLOCK; bidirectional pins as output (DATA[7:0])	-	-	9.0	ns
C_L	load capacitance	DATA[7:0], CLOCK, DIR, NXT, STP [1]	-	-	20	pF

[1] Load capacitance on each ULPI pin.

Table 56. Dynamic characteristics: analog I/O pins (DP, DM) in USB mode

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High-speed driver characteristics						
t_{HSR}	rise time (10 % to 90 %)	drive 45 Ω to GND on pins DP and DM	500	-	-	ps
t_{HSF}	fall time (10 % to 90 %)	drive 45 Ω to GND on pins DP and DM	500	-	-	ps
Full-speed driver characteristics						
t_{FR}	rise time	C_L = 50 pF; 10 % to 90 % of $\lvert V_{OH} - V_{OL} \rvert$	4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 10 % to 90 % of $\lvert V_{OH} - V_{OL} \rvert$	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	t_{FR}/t_{FF}; excluding the first transition from the idle state	90	-	111.1	%

Table 56. Dynamic characteristics: analog I/O pins (DP, DM) in USB mode *…continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Low-speed driver characteristics						
t_{LR}	transition time: rise time	C_L = 200 pF to 600 pF; 1.5 kΩ pull-up on pin DM enabled; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LF}	transition time: fall time	C_L = 200 pF to 600 pF; 1.5 kΩ pull-up on pin DM enabled; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LRFM}	rise and fall time matching	t_{LR}/t_{LF}; excluding the first transition from the idle state	80	-	125	%

Table 57. Dynamic characteristics: analog I/O pins (DP, DM) in transparent UART mode

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Full-speed driver characteristics (DM only)						
$t_{r(UART)}$	rise time for UART TXD	C_L = 185 pF; 0.37 V to 2.16 V	25	-	75	ns
$t_{f(UART)}$	fall time for UART TXD	C_L = 185 pF; 2.16 V to 0.37 V	25	-	75	ns
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	C_L = 185 pF; DATA0 to DM	-	-	39	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	C_L = 185 pF; DATA0 to DM	-	-	34	ns
Low-speed driver characteristics (DM only)						
$t_{r(UART)}$	rise time for UART TXD	C_L = 185 pF; 0.37 V to 2.16 V	100	-	400	ns
$t_{f(UART)}$	fall time for UART TXD	C_L = 185 pF; 2.16 V to 0.37 V	100	-	400	ns
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	C_L = 185 pF; DATA0 to DM	-	-	614	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	C_L = 185 pF; DATA0 to DM	-	-	614	ns
Full-speed receiver characteristics (DP only)						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP to DATA1	-	-	7	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP to DATA1	-	-	7	ns
Low-speed receiver characteristics (DP only)						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP to DATA1	-	-	7	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP to DATA1	-	-	7	ns

Table 58. Dynamic characteristics: analog I/O pins (DP, DM) in serial mode

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver timing (valid only for serial mode)						
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	TX_DAT, TX_SE0 to DP, DM; see Figure 12	-	-	20	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	TX_DAT, TX_SE0 to DP, DM; see Figure 12	-	-	20	ns
t_{PHZ}	driver disable delay from HIGH level	TX_ENABLE to DP, DM; see Figure 13	-	-	12	ns
t_{PLZ}	driver disable delay from LOW level	TX_ENABLE to DP, DM; see Figure 13	-	-	12	ns
t_{PZH}	driver enable delay to HIGH level	TX_ENABLE to DP, DM; see Figure 13	-	-	20	ns
t_{PZL}	driver enable delay to LOW level	TX_ENABLE to DP, DM; see Figure 13	-	-	20	ns
Receiver timing (valid only for serial mode)						
Differential receiver						

Table 58. Dynamic characteristics: analog I/O pins (DP, DM) in serial mode *…continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 14	-	-	20	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 14	-	-	20	ns
Single-ended receiver						
$t_{PLH(se)}$	single-ended propagation delay (LOW to HIGH)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 14	-	-	20	ns
$t_{PHL(se)}$	single-ended propagation delay (HIGH to LOW)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 14	-	-	20	ns

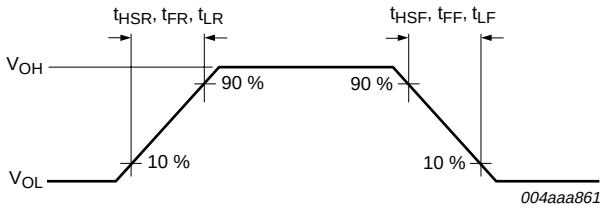


Fig 11. Rise time and fall time

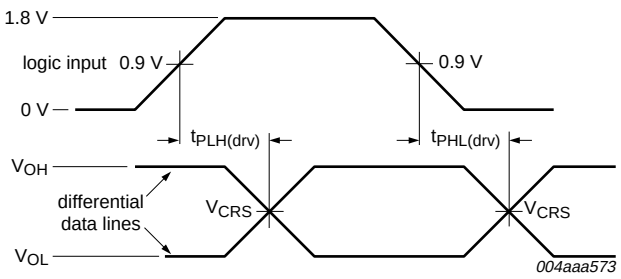


Fig 12. Timing of TX_DAT and TX_SE0 to DP and DM

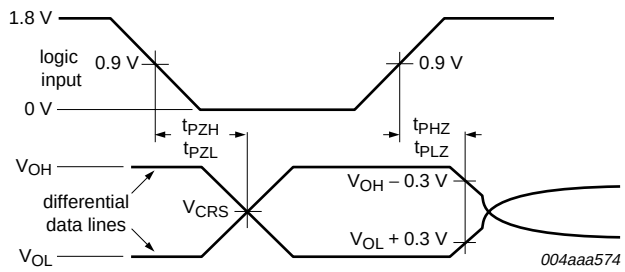


Fig 13. Timing of TX_ENABLE to DP and DM

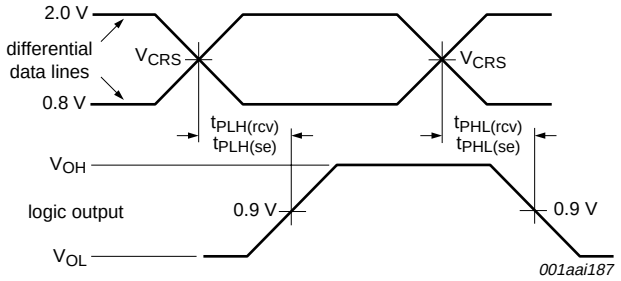


Fig 14. Timing of DP and DM to RX_RCV, RX_DP and RX_DM

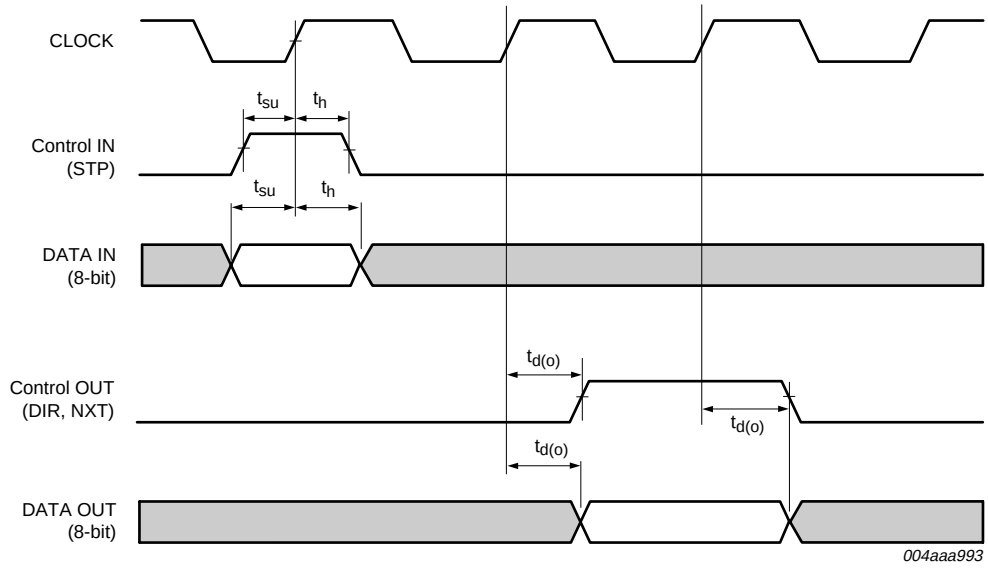


Fig 15. ULPI timing interface

Table 59. Dynamic characteristics: USB charger detection

V_{CC} = 2.4 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values refer to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{th(r)(VBUS)}$	rising threshold voltage on pin V_{BUS}	activates charger detection		4.4	-	4.7	V
$V_{th(f)(VBUS)}$	falling threshold voltage on pin V_{BUS}			0.8	-	2.0	V
$V_{th(trig)r(VBUS)}$	rising trigger threshold voltage on pin V_{BUS}		[1]	0.8	-	4	V
$R_{o(CHGR\_DET)}$	output resistance on pin CHGR_DET	resistance between V_{CC} and pin CHGR_DET		1	-	-	MΩ
$V_{OH(CHGR\_DET)}$	HIGH-level output voltage on pin CHGR_DET			0.7V_{CC}	-	-	V
$I_{OH(CHGR\_DET)}$	HIGH-level output current on pin CHGR_DET			-	-	2	mA
V_{DAT_SRC}	data source voltage	at I_{DAT_SRC}		0.5	-	0.7	V
V_{DAT_REF}	data detect voltage			0.25	-	0.4	V
I_{DAT_SRC}	data source current			0	-	200	µA
I_{DAT_SINK}	data sink current	$V_{DM} = V_{DAT\_SRC}$		50	-	150	µA
$t_{deb(VBUS)}$	debounce time on pin V_{BUS}			6.25	-	16	ms
$t_{DP\_SRC\_ON}$	DP source on time		[2]	125	-	320	ms
$t_{CHGR\_DET\_DBNC}$	charger detect debounce			25	-	64	ms
t_{DPSRC_HICRNT}	DP source off to high current			50	-	128	ms
$f_{clk(int)lp}$	low-power mode internal clock frequency			57.5	115	172.5	kHz
$V_{th(se)}$	single-ended receiver threshold voltage			0.8	-	2.0	V

[1] $V_{th(trig)r(VBUS)}$ has a wide triggering voltage range. Depending on V_{CC}, triggering can occur anywhere between 0.8 V to 4.0 V. When $V_{BUS} > V_{th(trig)r(VBUS)}$, regulator turns on (voltage on pin REG3V3 = $V_{O(REG3V3)}$ and pin REG1V8 = $V_{O(REG1V8)}$).

[2] This pin can be controlled either automatically or manually. When manual control is performed, ensure that DPVSRC_EN is enabled for at least 100 ms.

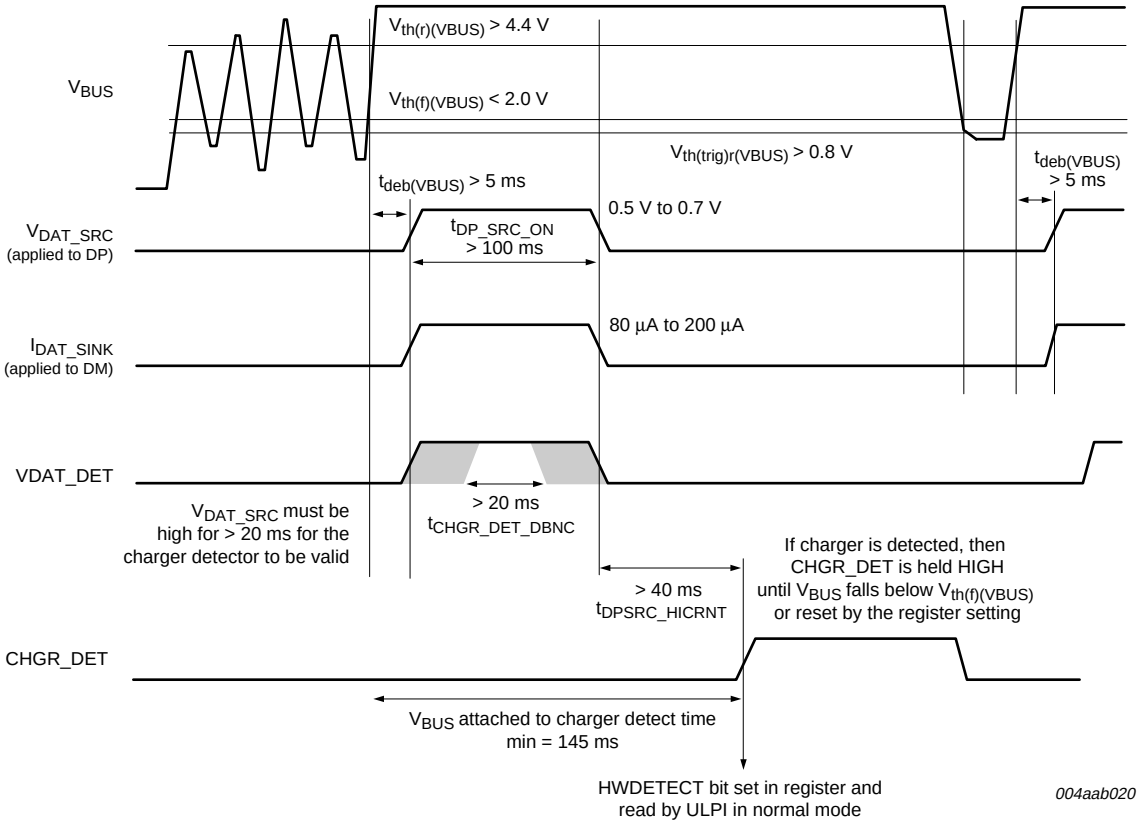
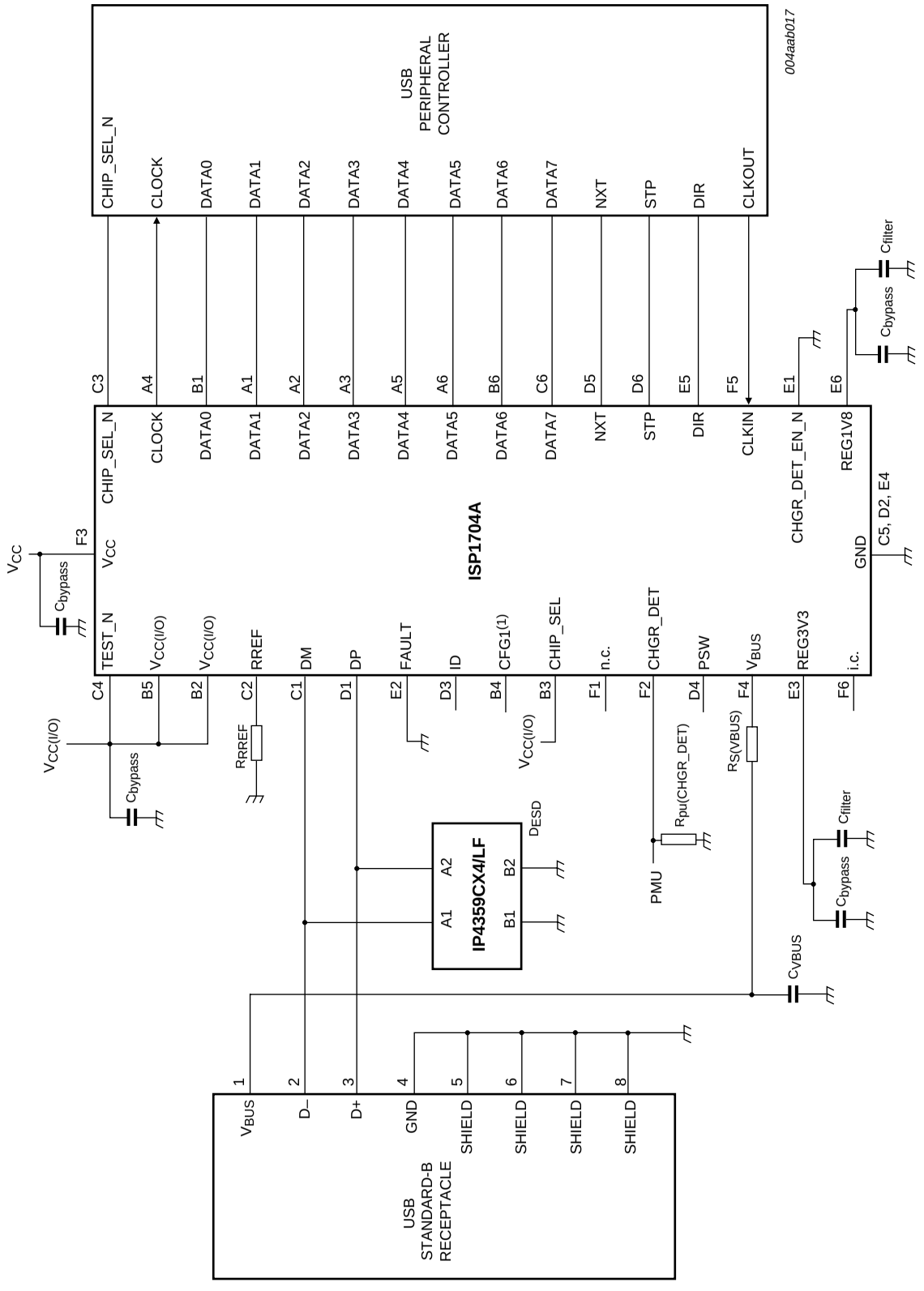


Fig 16. Charger detection

15. Application information

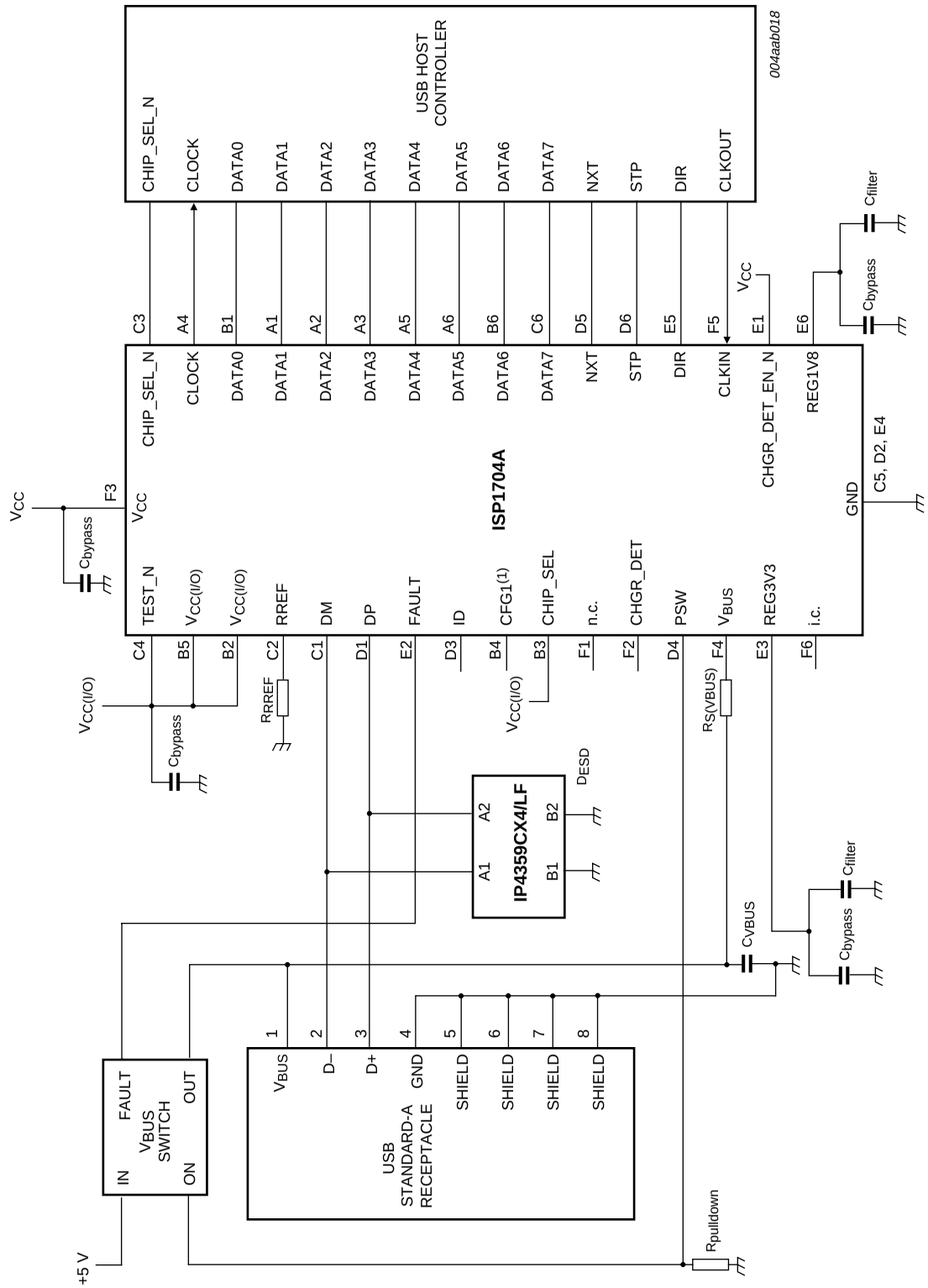
Table 60. Recommended bill of materials

Designator	Application	Part type	Remark
R_{RREF}	mandatory in all applications	12 kΩ ± 1 %	-
$R_{S(VBUS)}$	optional; for peripheral or external 5 V applications	1 kΩ ± 5 %	-
$R_{pulldown}$	recommended; for applications with an external V_{BUS} supply controlled by PSW	100 kΩ (recommended)	maximum value is determined by the voltage drop on PSW caused by leakage into PSW and the external supply control pin
$R_{pu(CHGR\_DET)}$	mandatory when USB battery charging is required	100 kΩ	-
C_{VBUS}	mandatory for peripherals	1 µF to 10 µF	-
	mandatory for host	96 µF (min)	-
	mandatory for OTG	1 µF to 6.5 µF	-
C_{bypass}	highly recommended for all applications	0.1 µF ± 20 %	-
C_{filter}	highly recommended for all applications	4.7 µF ± 20 %	use a low ESR capacitor (0.2 Ω to 2 Ω) for best performance
D_{ESD}	recommended	-	ISP1704A standalone: ESD IEC 61000-4-2 level 4; 8.8kV contact; 17.6kV air discharge compliant protection ISP1704A and IP4359CX4/LF (WLCSP) together: ESD IEC 61000-4-2 level 4; 20kV contact; 40kV air discharge compliant protection



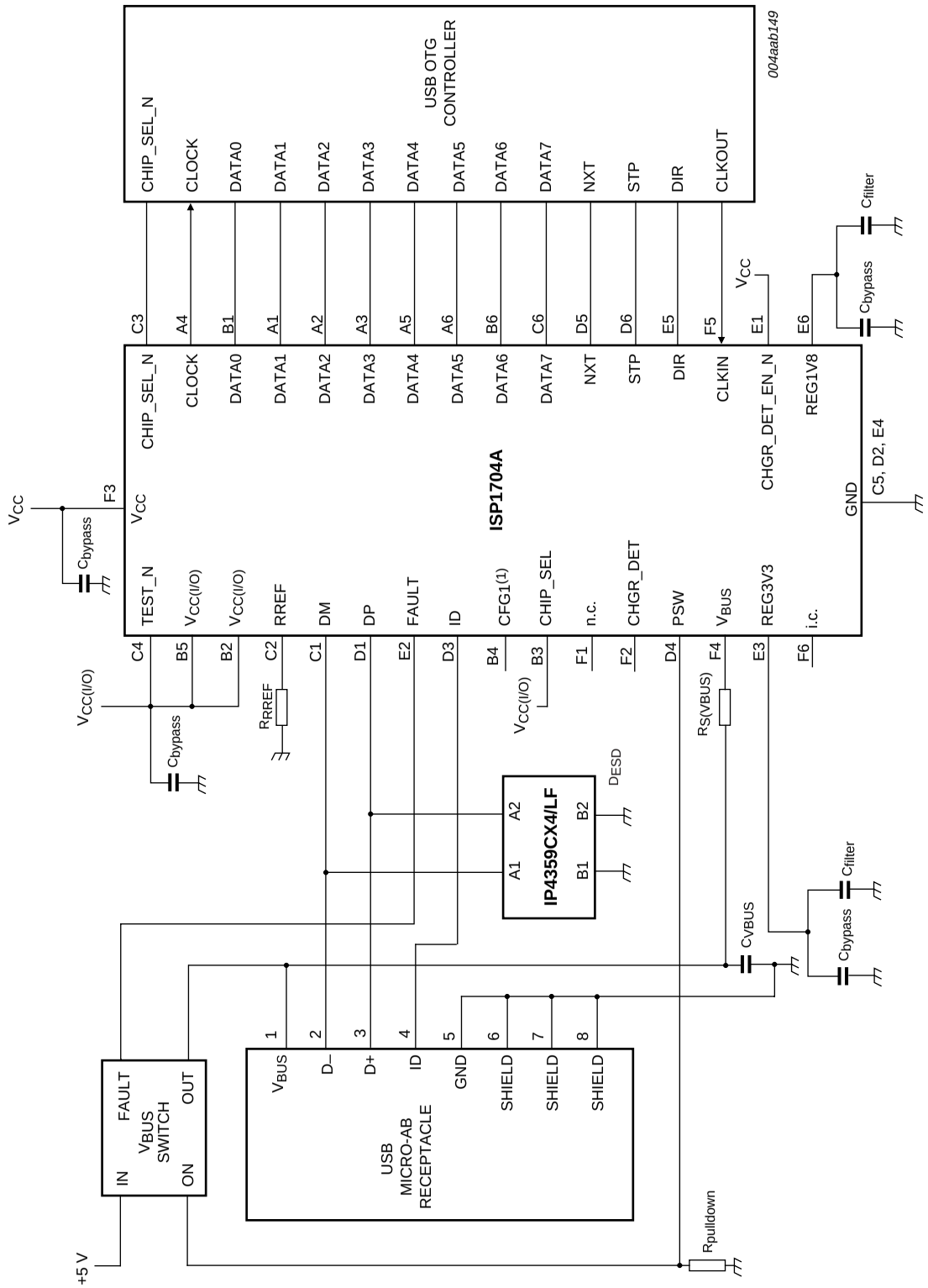
(1) Connect to either GND or $V_{CC(I/O)}$, depending on the clock frequency used. See Table 7.

Fig 17. Using the ISP1704A with a standard USB peripheral controller



(1) Connect to either GND or $V_{CC(I/O)}$, depending on the clock frequency used. See Table 7.

Fig 18. Using the ISP1704A with a standard USB host controller

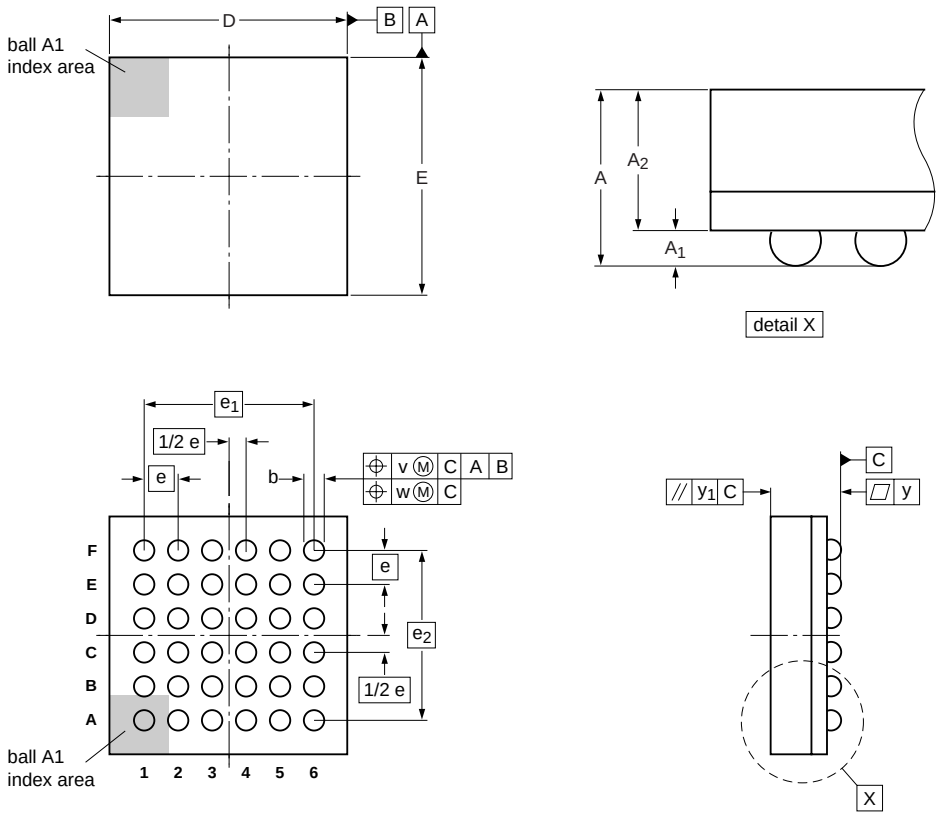


(1) Connect to either GND or $V_{CC(I/O)}$, depending on the clock frequency used. See Table 7.

Fig 19. Using the ISP1704A with a USB OTG controller

16. Package outline

TFBGA36: plastic thin fine-pitch ball grid array package; 36 balls; body 3.5 x 3.5 x 0.8 mm **SOT912-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.15	0.25 0.15	0.90 0.75	0.35 0.25	3.6 3.4	3.6 3.4	0.5	2.5	2.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT912-1	- - -	- - -	- - -			~~05-08-09~~ 05-09-01

Fig 20. Package outline SOT912-1 (TFBGA36)

17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 21) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 61 and 62

Table 61. SnPb eutectic process (from J-STD-020C)

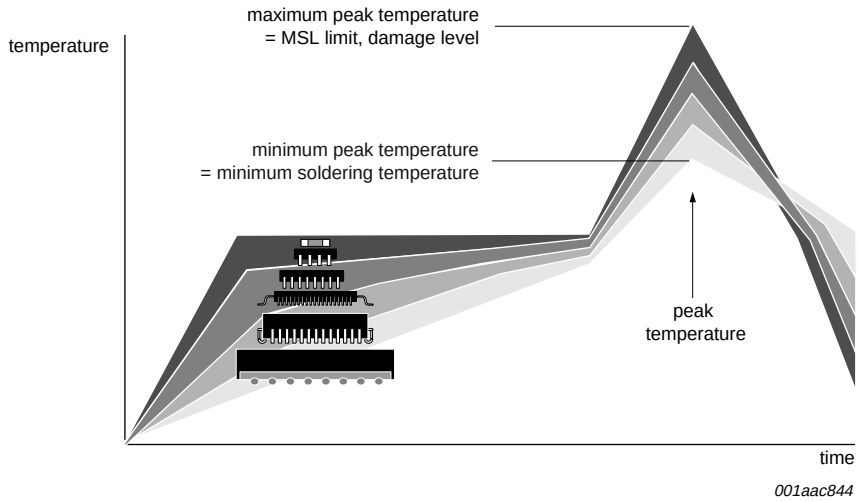
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 62. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 21.



MSL: Moisture Sensitivity Level

Fig 21. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18. Abbreviations

Table 63. Abbreviations

Acronym	Description
ASIC	Application-Specific Integrated Circuit
ATX	Analog USB Transceiver
CDM	Charge Device Model
EMI	ElectroMagnetic Interference
EOP	End-Of-Packet
ESD	ElectroStatic Discharge
ESR	Effective Series Resistance
FPGA	Field Programmable Gate-Array
HBM	Human Body Model
HNP	Host Negotiation Protocol
IEC	International Electrotechnical Commission
MM	Machine Model
NRZI	Non-Return to Zero Inverted
OTG	On-The-Go
PDA	Personal Digital Assistant
PHY	Physical
PID	Packet Identifier
PLL	Phase-Locked Loop
POR	Power-On Reset

Table 63. Abbreviations *...continued*

Acronym	Description
RoHS	Restriction of Hazardous Substances
RXCMD	Receive Command
RXD	Receive Data
SDR	Single Data Rate
SE0	Single-Ended Zero
SOC	System-On-Chip
SRP	Session Request Protocol
SYNC	Synchronous
TTL	Transistor-Transistor Logic
TXCMD	Transmit Command
TXD	Transmit Data
UART	Universal Asynchronous Receiver-Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB-IF	USB Implementers Forum
UTMI	USB Transceiver Macrocell Interface
UTMI+	USB Transceiver Macrocell Interface Plus
WLCSP	Wafer-Level Chip-Scale Package

19. Glossary

A-device — An OTG device with an attached micro-A plug.

B-device — An OTG device with an attached micro-B plug.

Link — ASIC, SOC or FPGA that contains the USB host or peripheral core.

PHY — Physical layer containing USB transceiver.

20. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3

[3] UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1

[4] Battery Charging Specification Rev. 1.0

[5] UTMI+ Specification Rev. 1.0

[6] USB 2.0 Transceiver Macrocell Interface (UTMI) Specification Ver. 1.05

[7] Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) (JESD22-A114D)

[8] Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM) (JESD22-A115-A)

[9] Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components (JESD22-C101-C)

[10] Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test (IEC 61000-4-2)

21. Revision history

Table 64. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ISP1704A_1	20080728	Product data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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24. Tables

25. Figures

26. Contents

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