SC183C

2.5MHz, 2A Synchronous Step-Down Regulator

Features

- V_{IN} Range: 2.9 – 5.5V
- V_{OUT} Options: 0.8 - 3.3V
- Up to 2A Output Current
- Ultra-Small Footprint, <1mm Height Solution
- 2.5MHz Switching Frequency
- Efficiency Up to 93%
- Low Output Noise Across Load Range
- Excellent Transient Response
- Start Up into Pre-Bias Output
- 100% Duty-Cycle Low Dropout Operation
- <1µA Shutdown Current
- Internal Soft Start
- Input Under-Voltage Lockout
- Output Over-Voltage, Current Limit Protection
- Over-Temperature Protection
- Adjustable Output Voltage
- 3mm x 3mm x 0.6mm thermally enhanced MLPQ-UT16 package
- -40 to +85°C Temperature Range
- Fully WEEE and RoHS Compliant

Applications

- Desktop Computing
- Set-Top Box
- LCD TV
- Network Cards
- Printer

Description

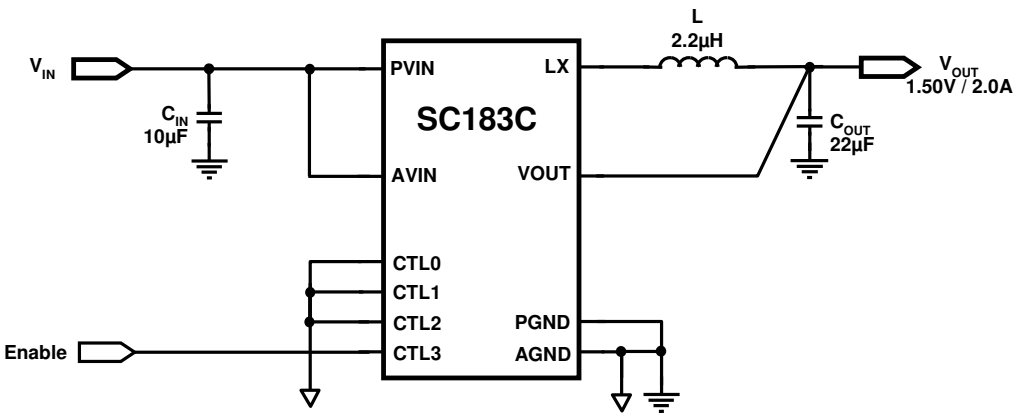
The SC183C is a 2A synchronous step-down regulator designed to operate with an input voltage range of 2.9 to 5.5 Volts. The device offers fifteen pre-determined outputs voltages via four control pins programmable from 0.8 to 3.3 Volts. The control pins allow for on-the-fly voltage changes, enabling system designers to implement dynamic power savings. The SC183C is also capable of adjusting output voltage via an external resistor divider.

The device operates with a fixed 2.5MHz oscillator frequency, allowing use of small surface mount external components.

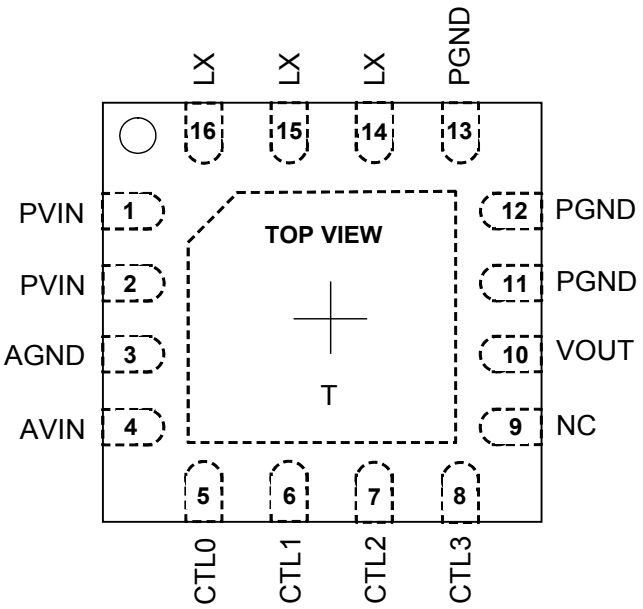
Connecting CTL0 — CTL3 to logic low forces the device into shutdown mode reducing the current to less than 1µA. Connecting any of the control pins to logic high, enables the converter and sets the output voltage according to Table 1. Other features include under-voltage lockout, soft-start to limit in-rush current, and over-temperature protection.

The SC183C is available in a thermally-enhanced, 3mm x 3mm x 0.6mm MLPQ-UT16 package and has a rated temperature range of -40 to +85°C.

Typical Application Circuit



Pin Configuration



3mm x 3mm x 0.6mm MLPQ-UT16

θ_{JA} = 40°C/W (1)

Ordering Information

Device	Package
SC183CULTRT(2)(3)	3mm x 3mm x 0.6mm MLPQ-UT16
SC183CEVB(4)	Evaluation Board

Notes:

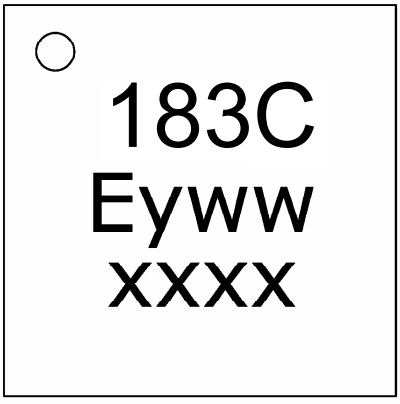
(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

(2) Available in tape and reel only. A reel contains 3,000 devices.

(3) Lead-free package only. Device is WEEE and RoHS compliant.

(4) Please specify the VOUT when ordering.

Marking Information



Marking for 3mm x 3mm MLPQ-UT 16 Lead Package:
Eyww = Datecode (Example: E852)
xxxx = Semtech Lot number (Example: E901)

Table 1 – Output Voltage Settings

CTL3	CTL2	CTL1	CTL0	Output Voltage
0	0	0	0	Shutdown
0	0	0	1	0.80
0	0	1	0	1.00
0	0	1	1	1.025
0	1	0	0	1.05
0	1	0	1	1.20
0	1	1	0	1.25
0	1	1	1	1.30
1	0	0	0	1.50
1	0	0	1	1.80
1	0	1	0	2.20
1	0	1	1	2.50
1	1	0	0	2.60
1	1	0	1	2.80
1	1	1	0	3.00
1	1	1	1	3.30

SEMTECH

Absolute Maximum Ratings

PVIN and AVIN Supply Voltages ..... -0.3 to 6.0V
LX Voltage ..... -1 to PVIN+1V, -3V (20ns Max), 6V Max
VOUT Voltage ..... -0.3 to AVIN+0.3V
CTLx pins Voltages ..... -0.3 to AVIN+0.3V
Peak IR Reflow Temperature ..... 260°C
ESD Protection Level(2) 3kV

Recommended Operating Conditions

Supply Voltage PVIN and AVIN ..... 2.9 to 5.5V
Maximum Output Current 2.0A
Temperature Range ..... -40 to +85°C
Input Capacitor 10uF
Output Capacitor 22uF
Output Inductor 2.2uH

Thermal Information

Thermal Resistance, Junction to Ambient(1) ..... 40 °C/W
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65 to +150 °C

Exceeding the absolute maximum ratings may result in permanent damage to the device and/or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.
(2) Tested according to JEDEC standard JESD22-A114-B.

Electrical Characteristics

Unless specified: PVIN= AVIN= 5.0V, VOUT= 1.50V, C_{IN}= 10µF, C_{OUT}= 22µF; L= 2.2µH; -40°C≤ $T_{J≤}$≤ +125 °C; Unless otherwise noted typical values are T_A= +25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Under-Voltage Lockout	UVLO	Rising AVIN, PVIN=AVIN	2.70	2.80	2.90	V
		Hysteresis	240(2)	300		mV
Output Voltage Tolerance(1)	ΔV_{OUT}	PVIN= AVIN= 2.9 – 5.5V; I_{OUT}=0A	-2.0		+2.0	%
Current Limit	I_{LIMIT}	Peak LX current	2.5	3.0	3.75(2)	A
Supply Current	I_Q	No load		10		mA
Shutdown Current	I_{SHDN}	CTL_{0-3}= AGND		1	10	µA
High Side Switch Resistance(2)	R_{DSON_P}	I_{LX}= 100mA, T_J= 25 °C		0.10	0.125	Ω
		I_{LX}= 100mA, T_J= 125 °C		0.14	0.18	
Low Side Switch Resistance(2,3)	R_{DSON_N}	I_{LX}= -100mA, T_J= 25 °C		0.09	0.115	
		I_{LX}= -100mA, T_J= 125 °C		0.125	0.160	
L_X Leakage Current(3)	$I_{LK(LX)}$	PVIN= AVIN= 5.5V; LX= 0V; CTL_{0-3}= AGND		1	10	µA
		PVIN= AVIN= 5.5V; LX= 5.0V; CTL_{0-3}= AGND	-10	-1		
Load Regulation(2)	$\Delta V_{LOAD-REG}$	PVIN= AVIN= 5.0V; I_{OUT}=1mA – 2A		±0.5	±1.0	%
Oscillator Frequency	F_{OSC}		2.125	2.500	2.875	MHz
Soft-Start Time(2)	T_{SS}	I_{OUT}= 0 - 2A	50	850	980	µs
CTLx Input High Current(3)	I_{EN_HI}	CTL_{0-3}=AVIN	-2.0		2.0	µA
CTLx Input Low Current(3)	I_{EN_LO}	CTL_{0-3}=AGND	-2.0		2.0	µA

Electrical Characteristics (continued)

Unless specified: PVIN= AVIN= 5.0V, VOUT= 1.50V, C_{IN}= 10µF, C_{OUT}= 22µF; L= 2.2µH; -40°C≤ T_J≤ +125 °C; Unless otherwise noted typical values are T_A= +25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CTLx Input High Threshold	V_{EN_HI}		1.2			V
CTLx Input Low Threshold	V_{EN_LO}				0.4	V
V_{OUT} Over Voltage Protection	V_{OVP}		110	115	120	%
Thermal Shutdown Temperature	T_{SD}			160		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}			10		°C

Notes:

(1) The "Output Voltage Tolerance" includes output voltage accuracy, voltage drift over temperature and the line regulation.

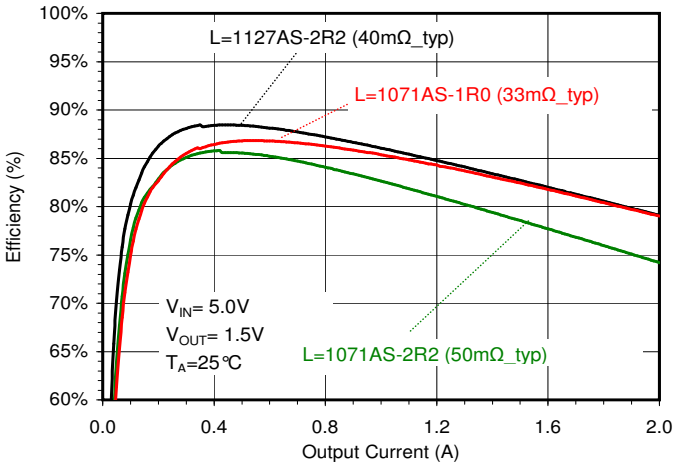
(2) Guaranteed by design.

(3) The negative current means the current flows through into the pin and the positive current means the current flows through out from the pin.

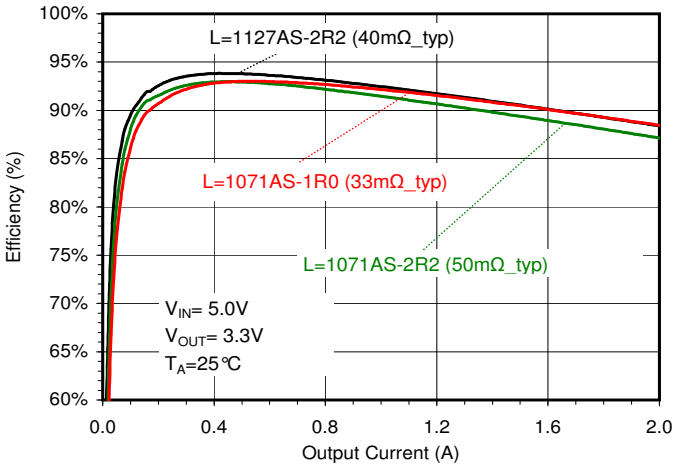
Typical Characteristics

Circuit Conditions: C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V, Unless otherwise noted, L= 2.2uH (TOKO: 1127AS-2R2M).

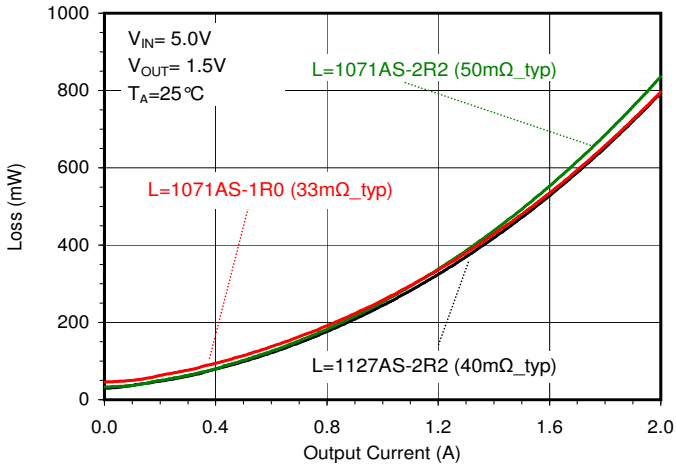
Efficiency vs. Load Current (V_{OUT}=1.5V)



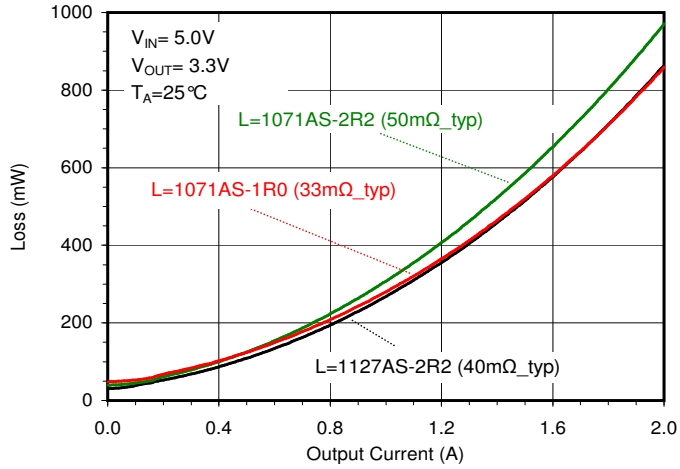
Efficiency vs. Load Current (V_{OUT}=3.3V)



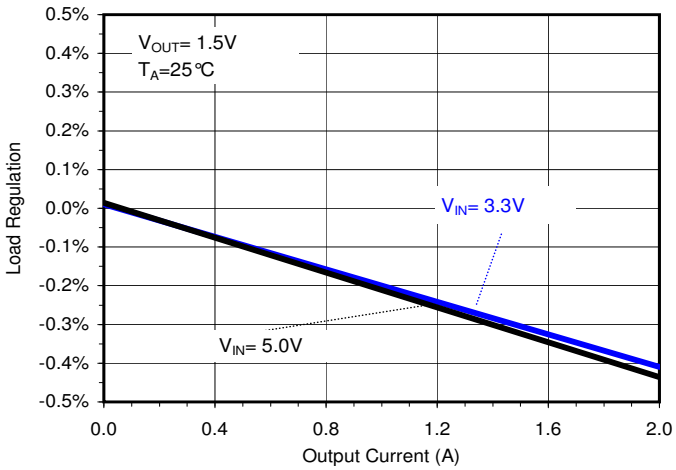
Total Loss vs. Load Current (V_{OUT}=1.5V)



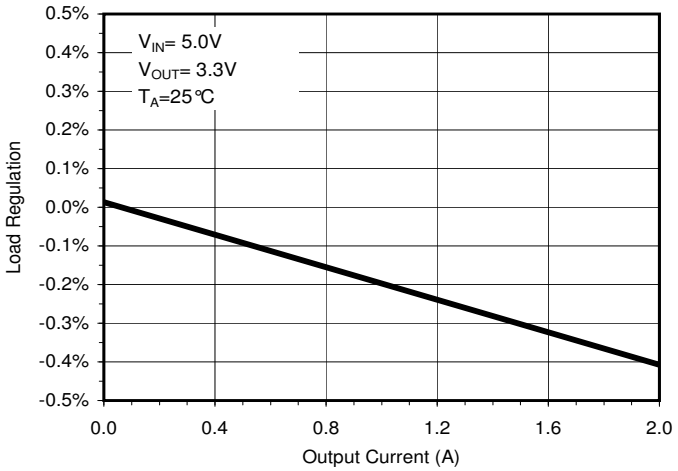
Total Loss vs. Load Current (V_{OUT}=3.3V)



Load Regulation (V_{OUT}=1.5V)



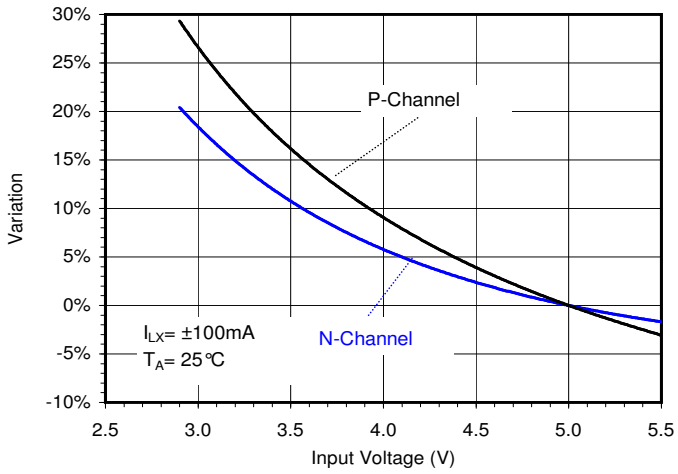
Load Regulation (V_{OUT}=3.3V)



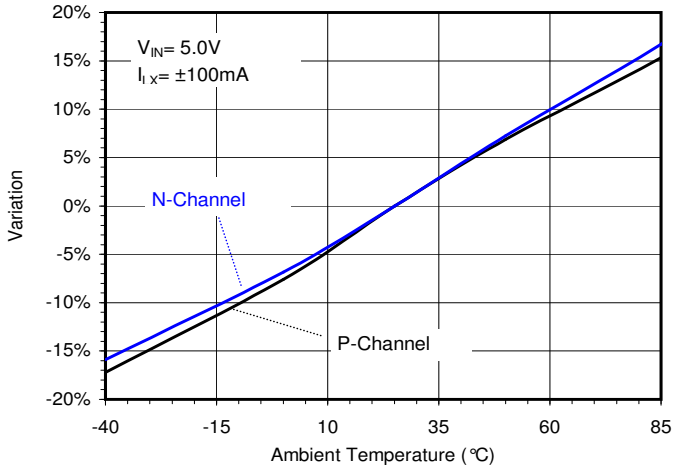
Typical Characteristics

Circuit Conditions: C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V, Unless otherwise noted, L= 2.2uH (TOKO: 1127AS-2R2M).

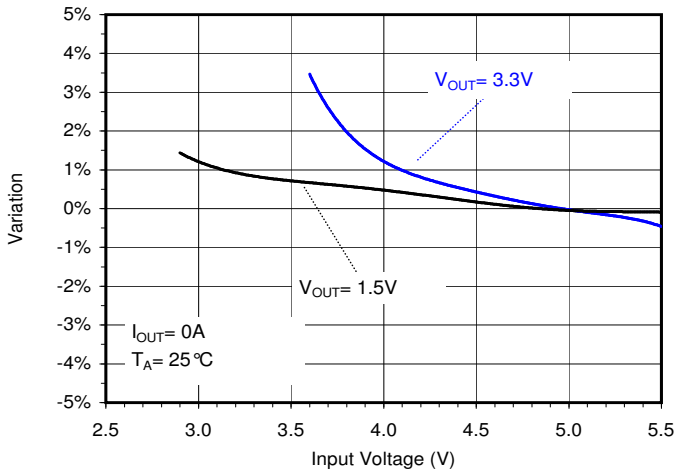
$R_{DS(ON)}$ Variation vs. Input Voltage



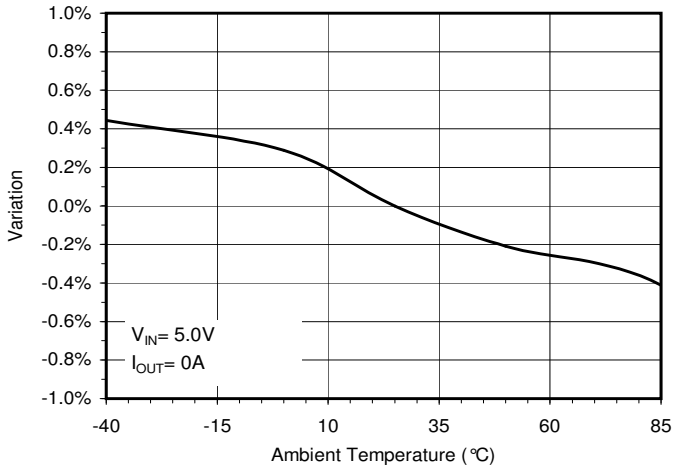
$R_{DS(ON)}$ Variation vs. Temperature



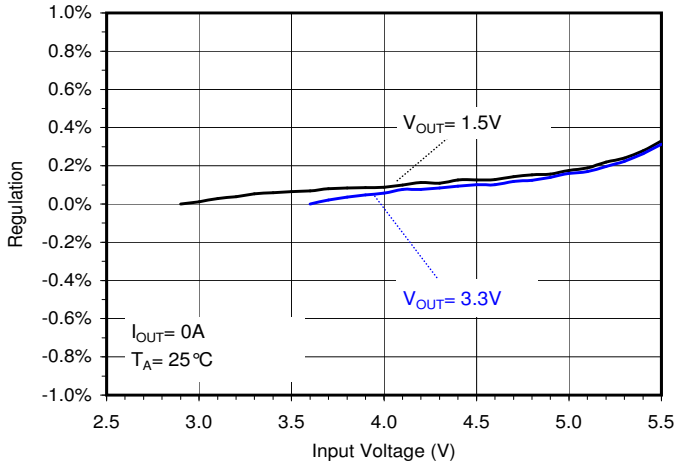
Switching Frequency vs. Input Voltage



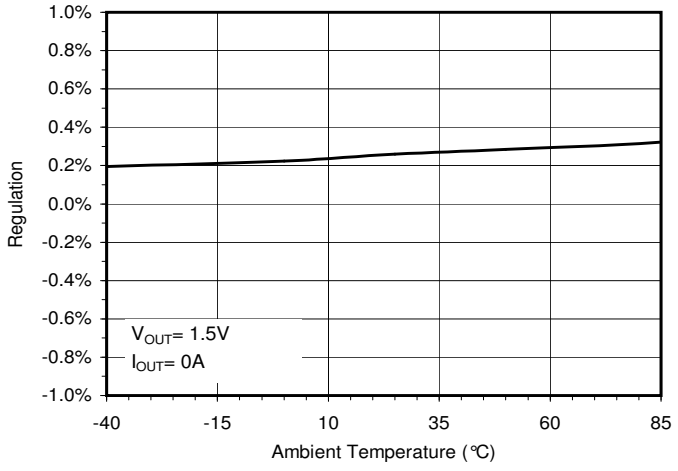
Switching Frequency vs. Temperature



Line Regulation



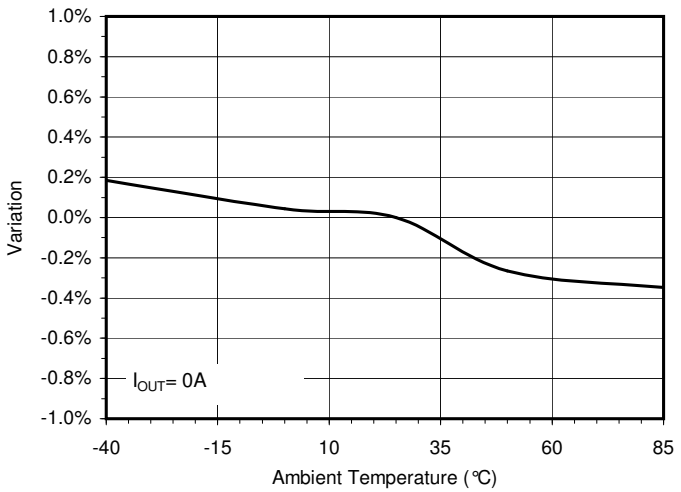
Line Regulation vs. Temperature



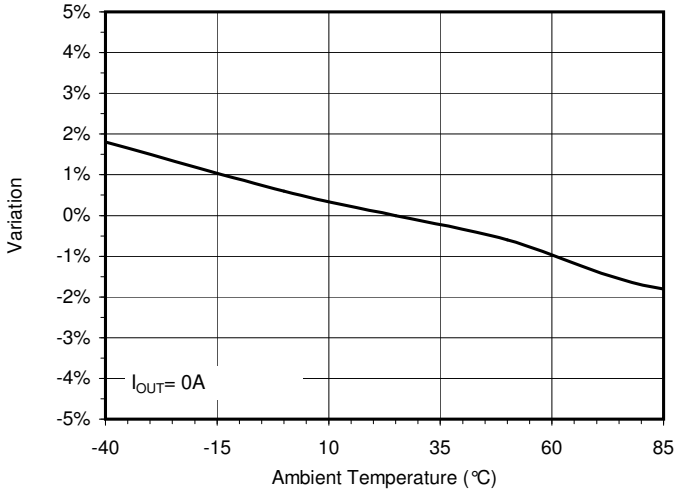
Typical Characteristics

Circuit Conditions: C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V, Unless otherwise noted, L= 2.2uH (TOKO: 1127AS-2R2M).

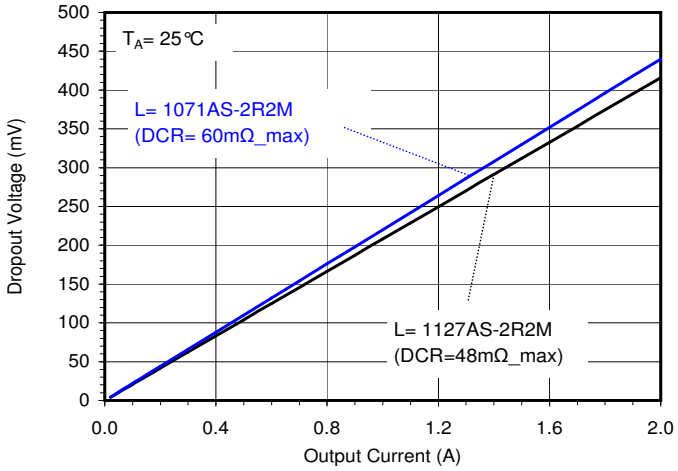
UVLO Rising Threshold Variation



UVLO Hysteresis Variation



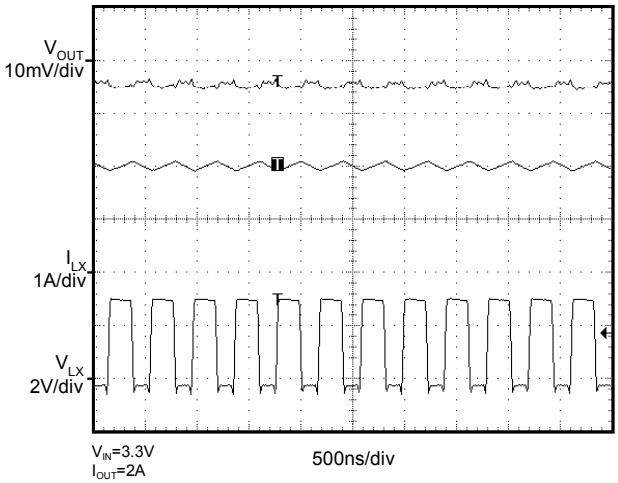
Dropout Voltage in 100% Duty Cycle Operation



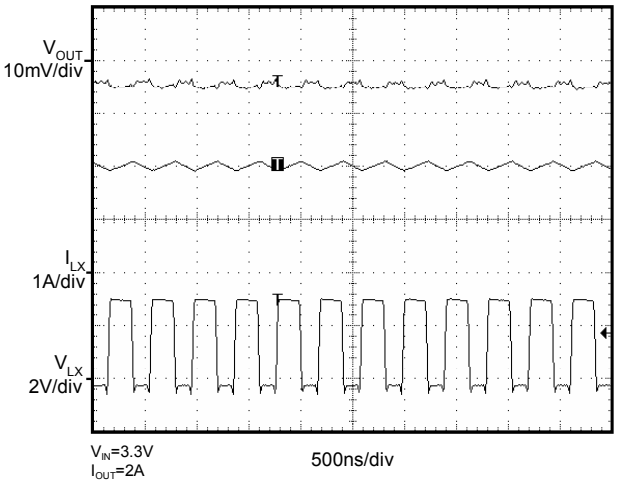
Typical Waveforms

Circuit Conditions: C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V, L= 2.2uH (TOKO: 1127AS-2R2M).

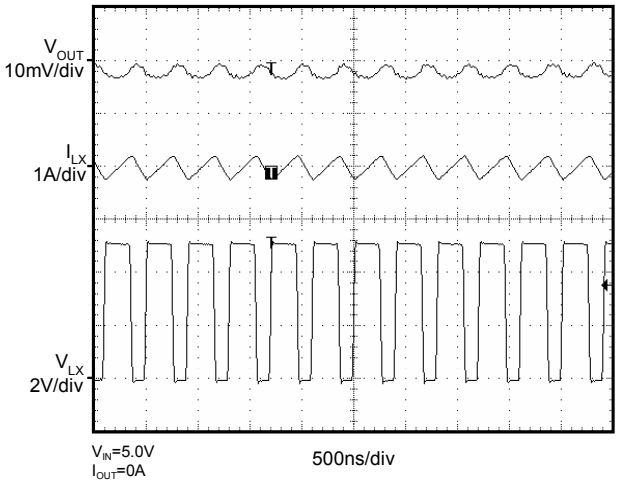
Output Voltage Ripple (V_{OUT}=1.5V)



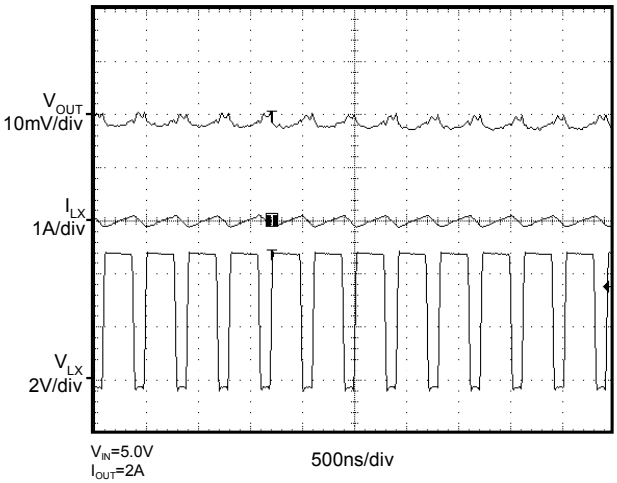
Output Voltage Ripple (V_{OUT}=1.5V)



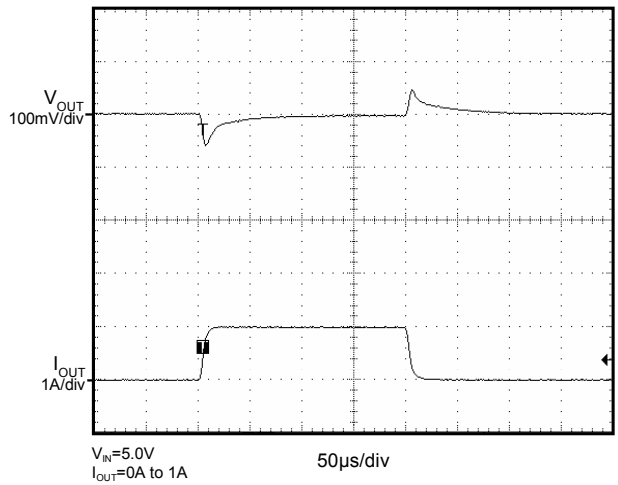
Output Voltage Ripple (V_{OUT}=3.3V)



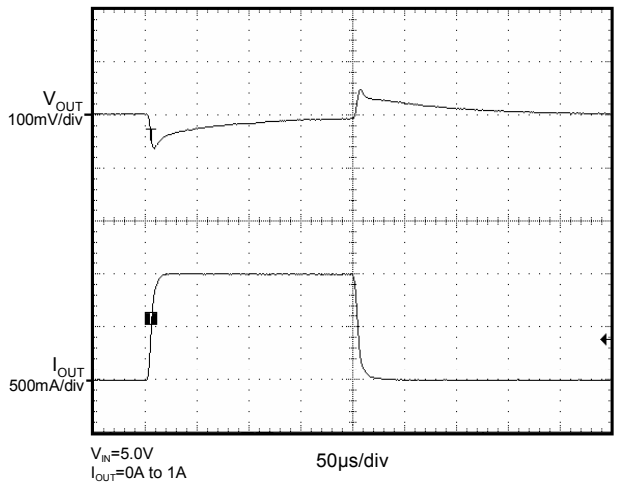
Output Voltage Ripple (V_{OUT}=3.3V)



Transient Response (V_{OUT}=1.5V; 0A to 1A)



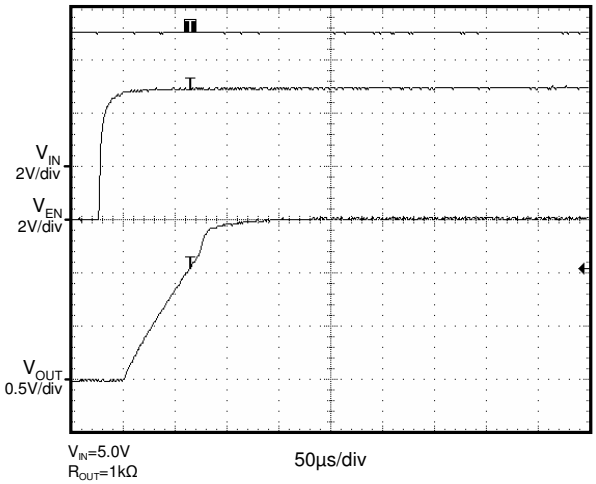
Transient Response (V_{OUT}=3.3V; 0A to 1A)



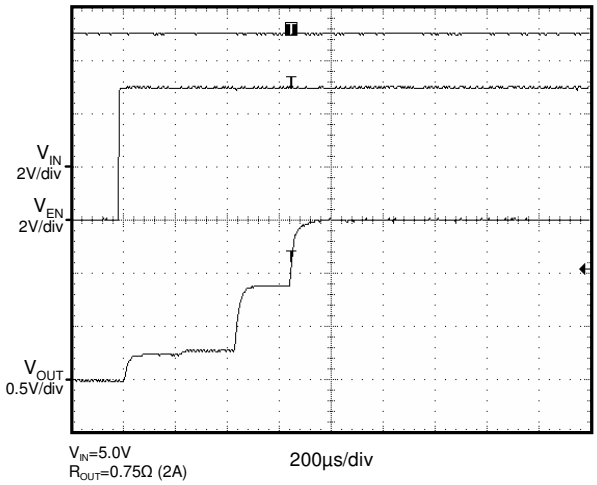
Typical Waveforms

Circuit Conditions: C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V, L= 2.2uH (TOKO: 1127AS-2R2M).

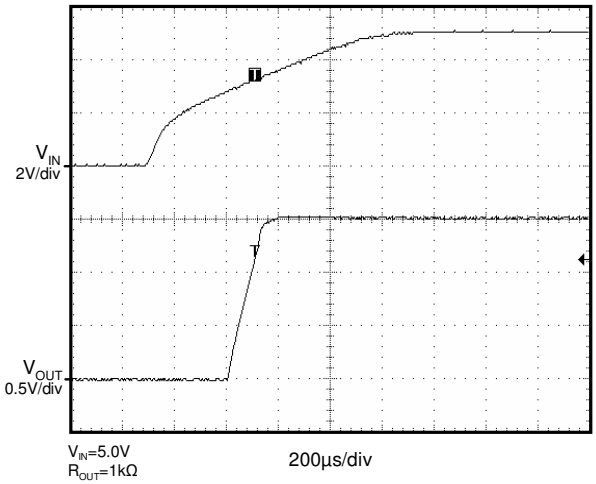
Start Up (Enable)(V_{OUT}=1.5V)



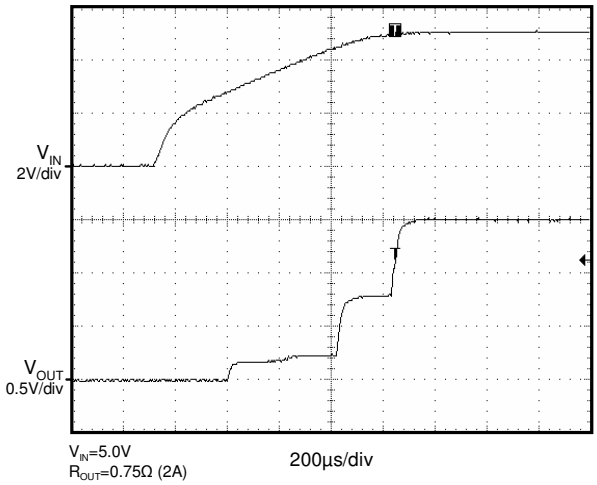
Start Up (Enable)(V_{OUT}=1.5V)



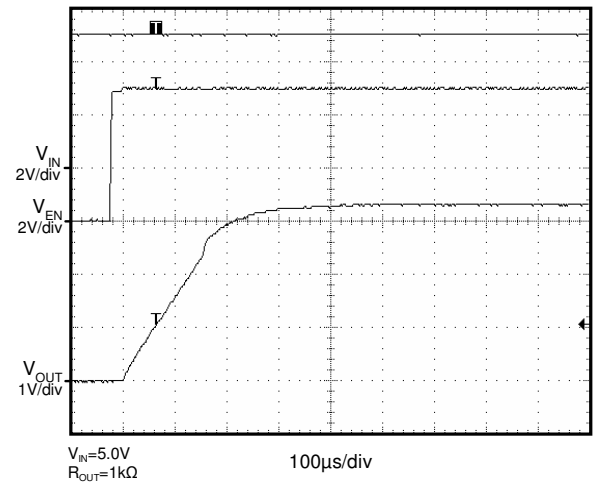
Start Up (Power up V_{IN}) (V_{OUT}=1.5V)



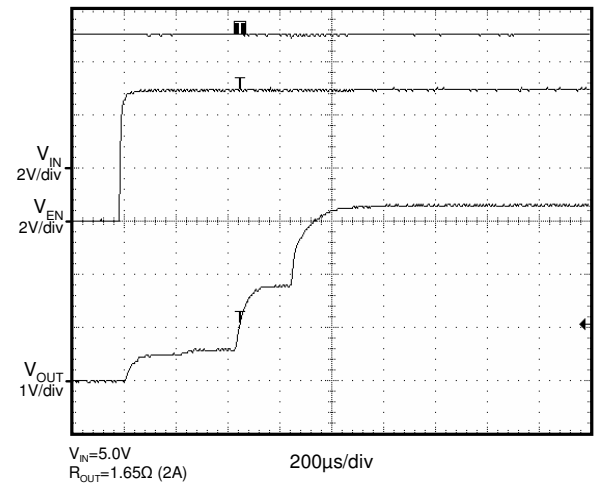
Start Up (Power up V_{IN}) (V_{OUT}=1.5V)



Start Up (Enable)(V_{OUT}=3.3V)



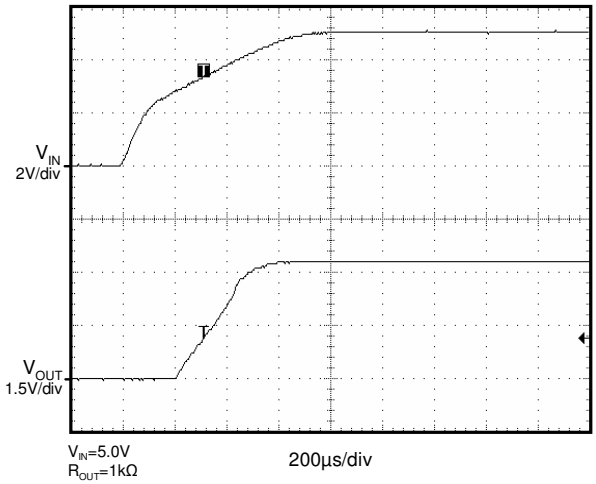
Start Up (Enable)(V_{OUT}=3.3V)



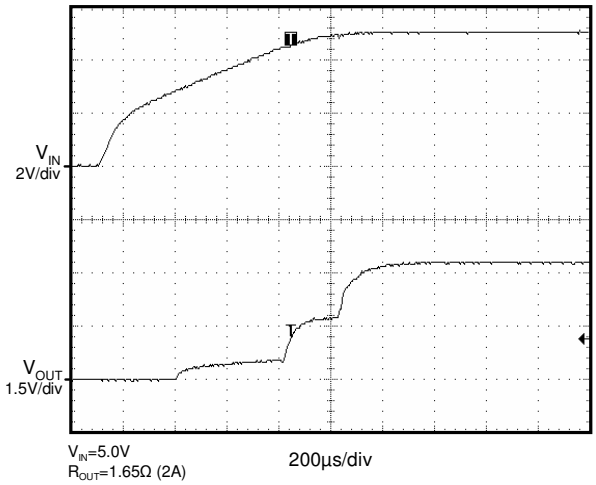
Typical Waveforms

Circuit Conditions: C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V, L= 2.2uH (TOKO: 1127AS-2R2M).

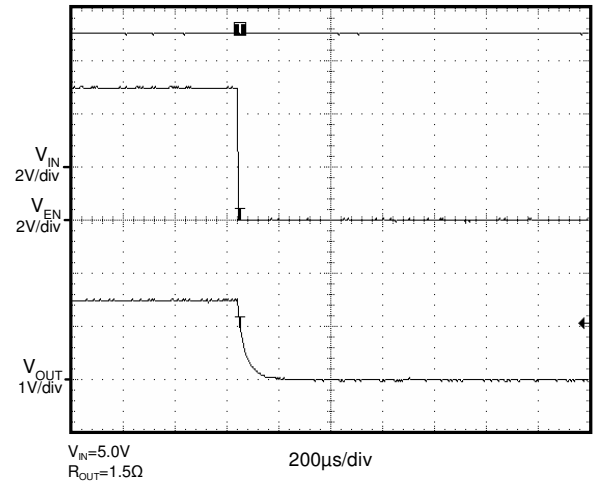
Start Up (Power up V_{IN}) (V_{OUT}=3.3V)



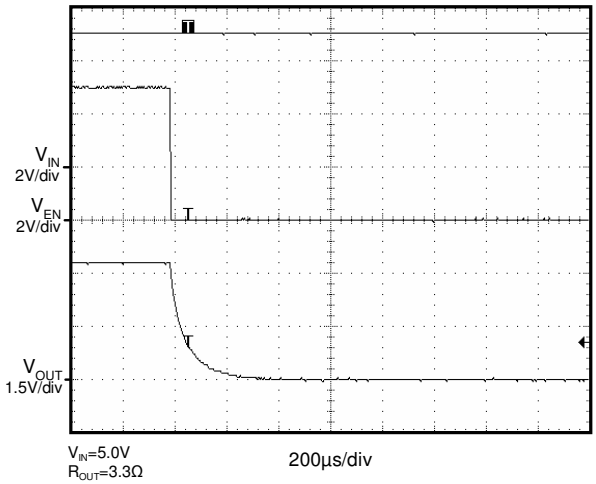
Start Up (Power up V_{IN}) (V_{OUT}=3.3V)



Shutdown (Disable)(V_{OUT}=1.5V)



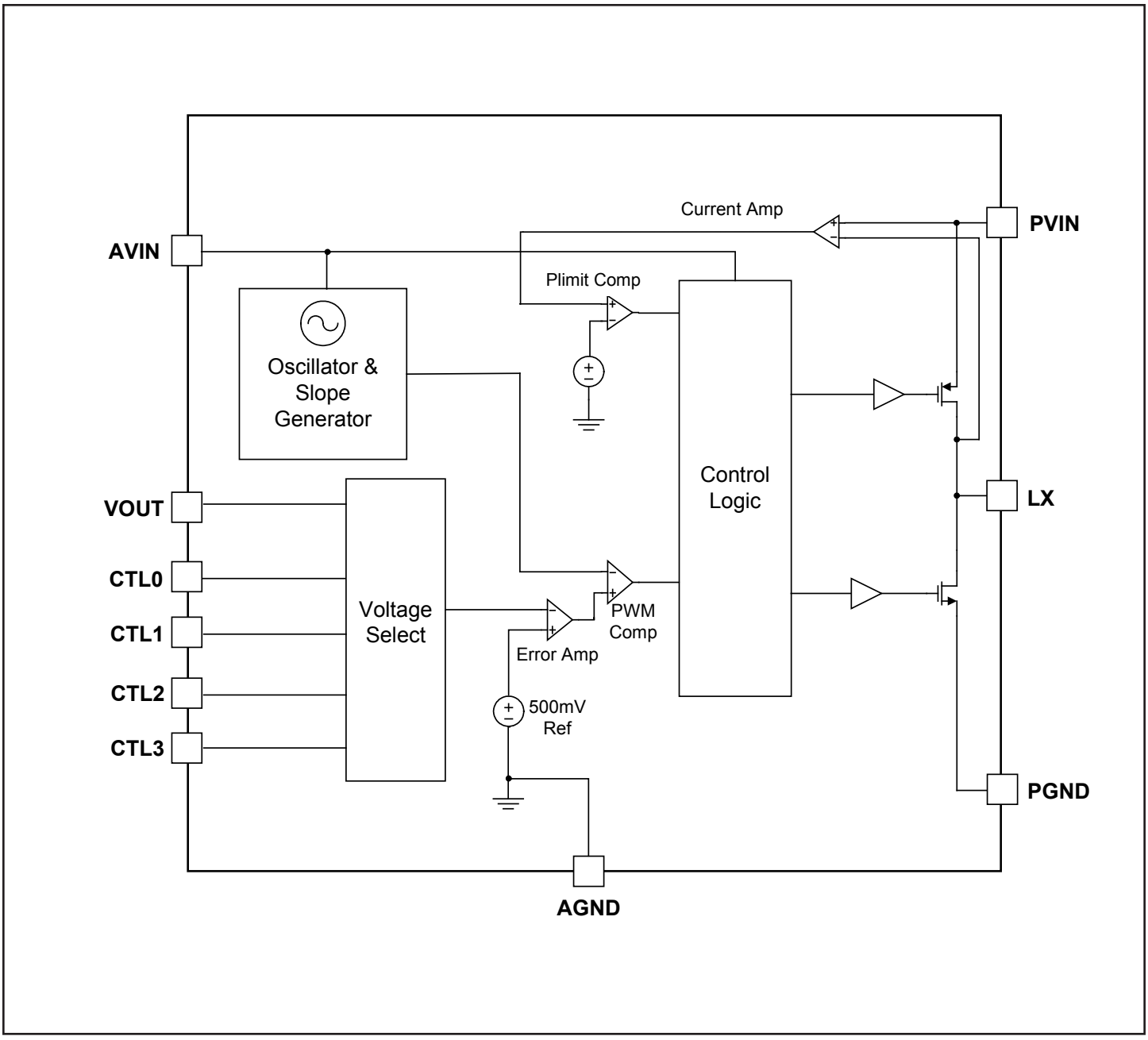
Shutdown (Disable)(V_{OUT}=3.3V)



Pin Descriptions

Pin #	Pin Name	Pin Function
1,2	PVIN	Input supply voltage for the converter power stage.
3	AGND	Ground connection for the internal circuitry. The AGND needs to be connected to PGND directly.
4	AVIN	Power supply for the internal circuitry. The AVIN needs to be connected to PVIN directly.
5	CTL0	Control bit 0 - see Table 1 for decoding. This pin has a 1 MΩ internal pulldown resistor. This resistor is switched in circuit whenever the EN pin is below the enable input high threshold, or when the part is in undervoltage lockout.
6	CTL1	Control bit 1 - see Table 1 for decoding. This pin has a 1 MΩ internal pulldown resistor. This resistor is switched in circuit whenever the EN pin is below the enable input high threshold, or when the part is in undervoltage lockout.
7	CTL2	Control bit 2 - see Table 1 for decoding. This pin has a 1 MΩ internal pulldown resistor. This resistor is switched in circuit whenever the EN pin is below the enable input high threshold, or when the part is in undervoltage lockout.
8	CTL3	Control bit 3 - see Table 1 for decoding. This pin has a 1 MΩ internal pulldown resistor. This resistor is switched in circuit whenever the EN pin is below the enable input high threshold, or when the part is in undervoltage lockout.
9	NC	No connection.
10	VOUT	Output voltage sense pin.
11,12,13	PGND	Ground connection for converter power stage.
14,15,16	LX	Switching node - connect an inductor between this pin and the output capacitor.
T	Thermal Pad	Thermal pad for heatsinking purposes. Recommend to connect it to PGND. It is not connected internally.

Block Diagram



Applications Information

Detailed Description

The SC183C is a synchronous step-down Pulse Width Modulated (PWM), DC-DC converter utilizing a 2.5MHz fixed-frequency voltage mode architecture. The device is designed to operate in fixed-frequency PWM mode. The switching frequency is chosen to minimize the size of the external inductor and capacitors while maintaining high efficiency.

Operation

During normal operation, the PMOS MOSFET is activated on each rising edge of the internal oscillator. The voltage feedback loop uses an internal feedback resistor divider. The period is set by the internal oscillator. The device has an internal synchronous NMOS rectifier and does not require a Schottky diode on the LX pin. The device operates as a buck converter in PWM mode with a fixed frequency of 2.5MHz.

Programmable Output Voltage

The SC183C has fifteen pre-determined output voltage values which can be individually selected by programming the CTL input pins (see Table 1 — Output Voltage Settings). Each CTL pin has an active 1 MΩ internal pull-down resistor. The 1MΩ resistor is switched in circuit whenever the CTL input voltage is below the input threshold, or when the part is in undervoltage lockout. It is recommended to tie all "Hi" CTL pins together and use an external pull-up resistor to AVIN if there is no enable signal or if the enable input is an open drain/collector signal. The CTL pins may be driven by a microprocessor to allow dynamic voltage adjustment for systems that reduce the supply voltage when entering sleep states. Avoid all zeros being present on the CTL pins when changing programmable output voltages as this would disable the device.

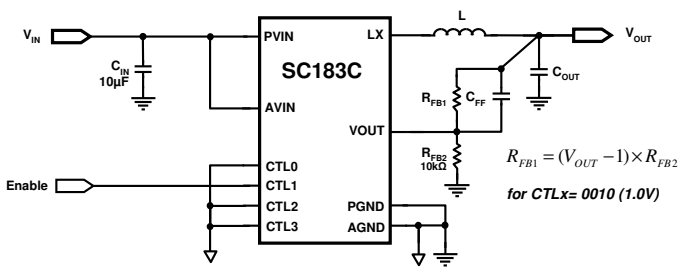


Figure 1 — Typical Schematic for Adjustable Output Voltage Option from The Standard 1.0V (CTL=[0010])

SC183C is also capable of regulating the different output voltage, which is not shown in the Table 1, via an external resistor divider. There will be a typical 2uA current flowing into the VOUT pin. The typical schematic of adjustable output voltage option from the standard 1.0V of CTLx=[0010], is shown in Figure 1. The C_{FF} is needed for maintain the performance of the transient response. The proper value of C_{FF} can be calculated by the equation 1.

$$C_{FF}[nF] = 2.5 \times \frac{(V_{OUT} - 0.5)^2}{R_{FB1}[k\Omega] \cdot (V_{OUT} - V_{OSTD})} \times \left(\frac{V_{OSTD}}{V_{OSTD} - 0.5}\right) \quad \cdots (1)$$

,where V_{OSTD} is the pre-determined output voltage via the CTL pins.

To simplify the design, it is recommended to program the desired output voltage from standard 1.0V as shown in Figure 1 with a proper C_{FF} calculated from equation 1. For programming the output voltage from other standard voltage, the R_{FB1}, R_{FB2} and C_{FF} need to be adjusted to meet the equation 1.

Protection Features

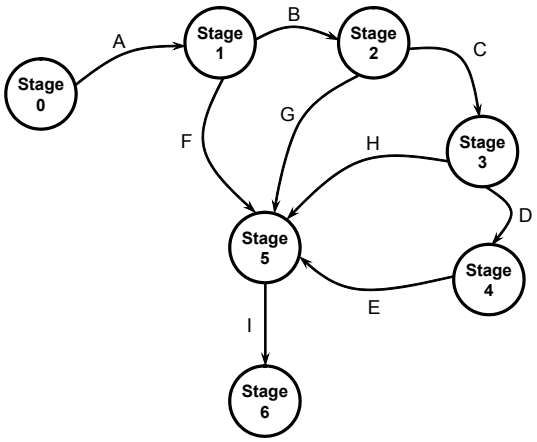
The SC183C provides the following protection features:

- Current Limit
- Over-Voltage Protection
- Soft-Start Operation
- Thermal Shutdown

Current Limit

The internal PMOS power device in the switching stage is protected by current limit feature. If the inductor current is above the PMOS current limit for 16 consecutive cycles, the part enters foldback current limit mode and the output current is limited to the current limit holding current (I_{CL_HOLD}) of a few hundred milliampere. Under this condition, the output voltage will be the product of I_{CL_HOLD} and the load resistance. The current limit holding current (I_{CL_HOLD}) will be decreased when output voltage is increased. The load presented must fall below the current limit holding current for the part to exit foldback current limit mode. Figure 4 shows the typical current limit holding current decreasing rate over different

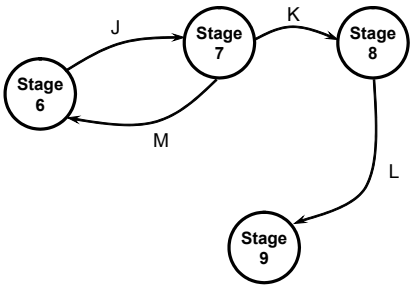
Applications Information (continued)



Stages	Operation description
0	Chip is OFF.
1	Peak current limit at 20% level PWM "ON" when inductor current of 0A PWM "OFF" when inductor current hits peak current limit Stage duration of 200us
2	Peak current limit at 25% level PWM "ON" when inductor current of 0A PWM "OFF" when inductor current hits peak current limit Stage duration of 200us
3	Peak current limit at 40% level PWM "ON" when inductor current of 500mA PWM "OFF" when inductor current hits peak current limit Stage duration of 200us
4	Peak current limit at 100% level PWM "ON" when inductor current of 500mA PWM "OFF" when inductor current hits peak current limit Stage duration of 200us
5	Peak current limit at 100% level Switch to close-loop PWM operation.
6	Soft Start ends. Normal PWM operation Overload protection is enabled

Conditions	Operation description
A	AVIN=PVIN > UVLO Threshold .and. One or more CTL pin is high. .and. Internal reference is ready.
B	End of stage 1 .and. Vout<86% target
C	End of stage 2 .and. Vout<86% target
D	End of stage 3 .and. Vout<86% target
E	End of stage 4 .and. Vout<86% target
F	Vout>86% target
G	Vout>86% target
H	Vout>86% target
I	End of soft start time of 800us

Figure 2 — Typical Diagram of Soft Start Operation



Stages	Operation description
6	Soft Start ends. Normal PWM operation Overload protection is enabled
7	Cycle by cycle peak current limit
8	OCP protection is actived foldback peak current limit to around 600mA PWM "ON" when inductor current of 0A PWM "OFF" when inductor current hits peak current limit of 600mA
9	Normal PWM operation Switch peak current limit to 100% level

Conditions	Operation description
J	Inductor current hits peak current limit
K	Peak current limit for 16 consecutive cycles
L	Vout ≥ 100% target
M	Inductor current doesn't hit peak current limit

Figure 3 — Typical Diagram of Current Limit Protection

Applications Information (continued)

output voltage. The SC183C is capable of sustaining an indefinite short circuit without damage and will resume normal operation when the fault is removed. The foldback current limit mode will be disabled during the soft-start. The typical operation of current limit protection is shown in figure 3.

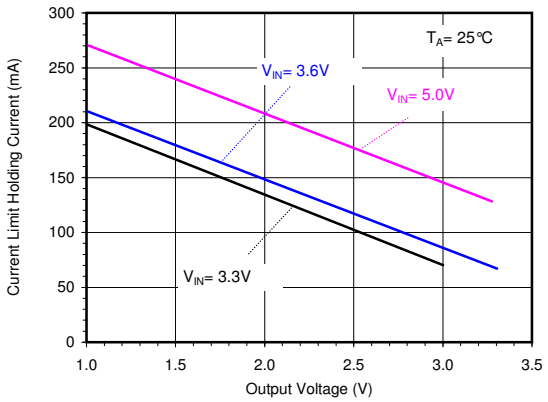


Figure 4 — Typical Current Limit Holding Current Decreasing Rate vs. Output Voltage

Over-Voltage Protection

In the event of a 15% over-voltage on the output, the PWM drive is disabled with LX pin floating.

Sof-Start

The soft-start mode is activated after AVIN reaches its UVLO and one or more CTL pins are set high to enable the part. The thermal shutdown event will also activate the soft start sequence. Soft-start mode controls the maximum current during startup thus limiting in-rush current. The PMOS current limit is stepped through four soft start levels of approximately 20%, 25%, 40%, & 100%. Each step is maintained for 200µs following internal reference start up of 50µs giving the total nominal startup period of 850µs. During startup, the chip operates in controlling the inductor current swings between 0A and current limit. If V_{OUT} reaches 86% of the target or at the end of soft-start period, the SC183C will switch to PWM mode operation. Figure 2 shows the typical diagram of soft start operation.

The SC183C is capable of starting up into a pre-biased output. When the output is precharged by another supply rail, the SC183C will not discharge the output during the soft start interval.

Shut Down

When all CTL pins are low, the SC183C will run in shut-down mode, drawing less than 1µA from the input power supply. The internal switches and bandgap voltage will be immediately turned off.

Thermal Shutdown

The device has a thermal shutdown feature to protect the SC183C if the junction temperature exceeds 160°C. During thermal shutdown, the on-chip power devices are disabled, tri-stating the LX output. When the temperature drops by 10°C, it will initial the soft start cycle to resume normal operation.

Inductor Selection

The SC183C converter has internal loop compensation. The compensation is designed to work with a output filter corner frequency of less than 40kHz for V_{IN} of 5V and 50KHz for V_{IN} of 3.3V over any operating condition. The corner frequency of output filter can be defined by the equation 2.

$$f_C = \frac{1}{2\pi\sqrt{L \cdot C_{OUT}}} \quad \text{(2)}$$

Values outside this range may lead to instability, malfunction, or out-of-specification performance.

In general, the inductance is chosen by making the inductor ripple current to be less than 30% of maximum load current. When choosing an inductor, it is important to consider the change in inductance with DC bias current. The inductor saturation current is specified as the current at which the inductance drops a specific percentage from the nominal value. This is approximately 30%. Except for short-circuit or other fault conditions, the peak current must always be less than the saturation current specified by the manufacturer. The peak current is the maximum load current plus one half of the inductor ripple current at the maximum input voltage. Load and/or line transients can cause the peak current to exceed this level for

Applications Information (continued)

short durations. Maintaining the peak current below the inductor saturation specification keeps the inductor ripple current and the output voltage ripple at acceptable levels. Manufacturers often provide graphs of actual inductance and saturation characteristics versus applied inductor current. The saturation characteristics of the inductor can vary significantly with core temperature. Core and ambient temperatures should be considered when examining the core saturation characteristics.

When the inductance has been determined, the DC resistance (DCR) must be examined. The efficiency that can be achieved is dependent on the DCR of the inductor. The lower values give higher efficiency. The RMS DC current rating of the inductor is associated with losses in the copper windings and the resulting temperature rise of the inductor. This is usually specified as the current which produces a 40˚C temperature rise. Most copper windings are rated to accommodate this temperature rise above maximum ambient.

Magnetic fields associated with the output inductor can interfere with nearby circuitry. This can be minimized by the use of low noise shielded inductors which use the minimum gap possible to limit the distance that magnetic fields can radiate from the inductor. However shielded inductors typically have a higher DCR and are thus less efficient than a similar sized non-shielded inductor.

Final inductor selection depends on various design considerations such as efficiency, EMI, size, and cost. Table 2 lists the manufacturers of recommended inductor options. The saturation characteristics and DC current ratings are also shown.

Manufacturer Part Number	L (µH)	DCR Max (Ω)	Rated Current (A)	L at Rated Current (µH)	Dimensions LxWxH (mm)
TOKO 1071AS-2R2M	2.20±20%	0.060	1.80	1.54	2.8x3.0x1.5
TOKO 1071AS-1R0N	1.00±30%	0.040	2.70	0.70	2.8x3.0x1.5
TOKO 1127AS-2R2M	2.20±20%	0.048	2.50	1.54	3.5x3.7x1.8
Panasonic ELLVGG1R0N	1.00±23%	0.062	2.20	0.70	3.2x3.2x1.5

Table 2 – Recommended Inductors

C_{OUT} Selection

The internal voltage loop compensation in the SC183C limits the minimum output capacitor value to 22µF if using the inductor of 2.2µH or 44uF if using the inductor of 1µH. This is due to its influence on the the loop crossover frequency, phase margin, and gain margin. Increasing the output capacitor above this minimum value will reduce the crossover frequency and provide greater phase margin. A total output capacintance should not exceed 50uF to avoid any start-up problems. For most typical applications it is recommended to use output capacitance of 22uF to 44uF. When choosing output capacitor's capacitance, verify the voltage derating effect from the capacitor vendors data sheet.

Capacitors with X7R or X5R ceramic dielectric are recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

The output voltage droop due to a load transient is determined by the capacitance of the ceramic output capacitor. The ceramic capacitor supplies the load current initially until the loop responds. Within a few switching cycles the loop will respond and the inductor current will increase to match the required load. The output voltage droop during the period prior to the loop responding can be related to the choice of output capacitor by the relationship from equation 3.

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot f_{OSC}} \quad \text{(3)}$$

The output capacitor RMS current ripple may be calculated from the equation 4.

$$I_{COUT(RMS)} = \frac{1}{2\sqrt{3}} \left(\frac{V_{OUT} \cdot \left(V_{IN(MAX)} - V_{OUT}\right)}{L \cdot f_{OSC} \cdot V_{IN}} \right) \quad \text{(4)}$$

Table 3 lists the manufacturers of recommended output capacitor options.

C_{IN} Selection

The SC183C source input current is a DC supply current with a triangular ripple imposed on it. To prevent large

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Applications Information (continued)

input voltage ripple, a low ESR ceramic capacitor is required. A minimum value of 4.7µF should be used. It is important to consider the DC voltage coefficient characteristics when determining the actual required value. It should be noted a 10uF, 6.3V, X5R ceramic capacitor with 5V DC applied may exhibit a capacitance as low as 4.5uF. To estimate the required input capacitor, determine the acceptable input ripple voltage and calculate the minimum value required for C_{IN} from the equation 5.

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{\left(\frac{\Delta V}{I_{OUT}} - ESR\right)\cdot f_{OSC}} \quad \text{(5)}$$

The input capacitor RMS ripple current varies with the input and output voltage. The maximum input capacitor RMS current is found from the equation 6.

$$I_{CIN(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN}}\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad \text{(6)}$$

The input voltage ripple and RMS current ripple are at maximum when the input voltage is twice the output voltage or 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the PMOS switch. Low ESR/ESL X5R ceramic capacitors are recommended for this function. To minimise stray inductance ,the capacitor should be placed as closely as possible to the PVIN and PGND pins of the SC183C.

Manufacturer Part Nunber	Value (µF)	Type	Rated Voltage (VDC)	Value at 3.3V (µF)	Dimensions LxWxH (mm)
Murata GRM21BR60J106K	10±10%	X5R	6.3	4.74	2.0x1.25x1.25 (EIA:0805)
Murata GRM219R60J106K	10±10%	X5R	6.3	4.05	2.0x1.25x0.85 (EIA:0805)
Murata GRM21BR60J226M	22±20%	X5R	6.3	6.57	2.0x1.25x1.25 (EIA:0805)
Murata GRM31CR60J476M	47±20%	X5R	6.3	20.3	3.2x1.6x1.6 (EIA:1206)

Table 3 – Recommended Capacitors

Applications Information (continued)

PCB Layout Considerations

The layout diagram in Figure 5 shows a recommended top-layer PCB for the SC183C and supporting components. Figure 6 shows the bottom layer for this PCB. Fundamental layout rules must be followed since the layout is critical for achieving the performance specified in the Electrical Characteristics table. Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can result.

The following guidelines are recommended when developing a PCB layout:

1. The input capacitor, C_{IN} should be placed as close to the PVIN and PGND pins as possible. This capacitor provides a low impedance loop for the pulsed currents present at the buck converter's input. Use short wide traces to connect as closely to the IC as possible. This will minimize EMI and input voltage ripple by localizing the high frequency current pulses.
2. Keep the LX pin traces as short as possible to minimize pickup of high frequency switching edges to other parts of the circuit. C_{OUT} and L should be connected as close as possible between the LX and GND pins, with a direct return to the GND pin from C_{OUT}.
3. Route the output voltage feedback/sense path away from inductor and LX node to minimize noise and magnetic interference.
4. Use a ground plane referenced to the SC183C PGND pin. Use several vias to connect to the component side ground to further reduce noise and interference on sensitive circuit nodes.
5. If possible, minimize the resistance from the VOUT and AGND pins to the load. This will reduce the voltage drop on the ground plane and improve the load regulation. And it will also improve the overall efficiency by reducing the copper losses on the output and ground planes.

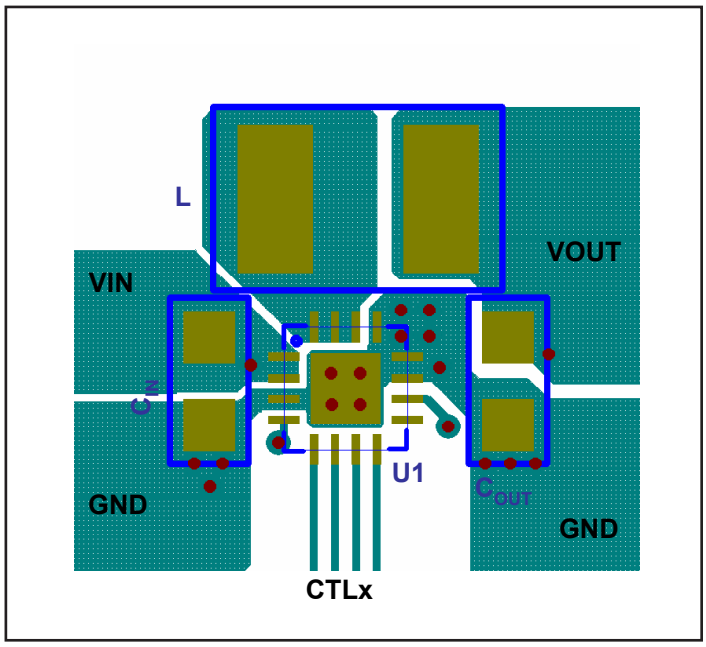


Figure 5 — Recommended PCB Layout

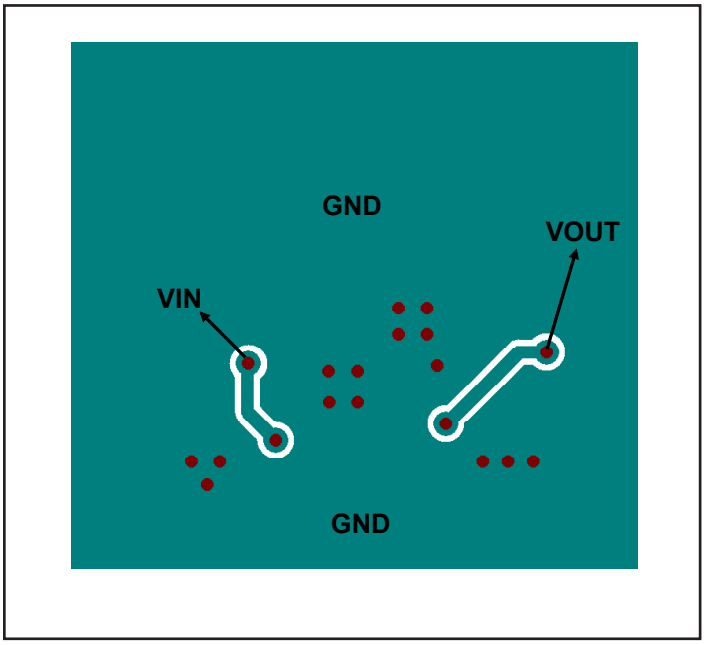
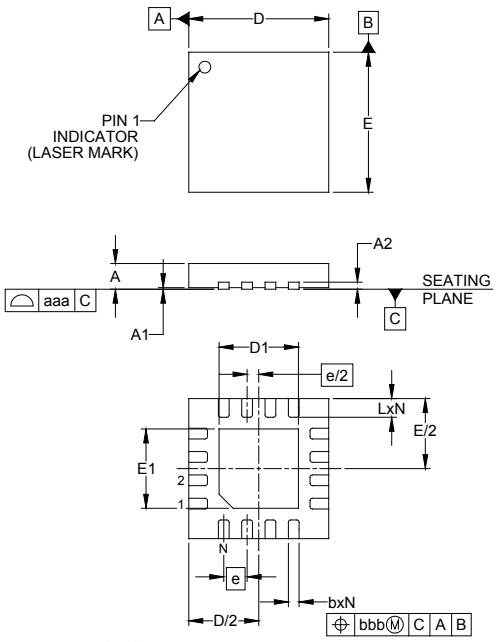


Figure 6 — Bottom Layer Detail

Outline Drawing – 3x3 MLPQ-UT16

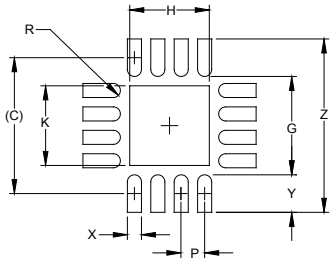


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.152)	
b	.007	.009	.012	0.18	0.23	0.30
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e		.020 BSC			0.50 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		16			16	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

Land Pattern – 3x3 MLPQ-UT16



DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.020	0.50
R	.006	0.15
X	.012	0.30
Y	.031	0.80
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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