

Features

- Host Interface
 - USB (Compliant with USB 1.1 and 2.0, CCID Supported)
 - Transmission Speed: USB: 12 MBit/sec
 - Customer Specific USB-descriptors
 - Serial
- Smart Card Interface
 - Smart Card Interface Compliant with ISO 7816 and EMV 2000
 - Support of T=0, T=1, TWI (S=8), 2-wire: SLE 4432/42 (S=10), 3-wire: SLE4418/28 (S=9), others on request
 - High Performance Smart Card Interface
 - Supports 5V, 3V and 1.8V Smart Cards
 - Supply Current 60 mA to Power the Smart Card
 - Smart Card Movement Detection with Auto Power-off
 - Automatic Detection of Smart Card Type
 - Short Circuit and Thermal Protection
 - 8-pin Handling (C4/C8 Supported)
- Compliance
 - WHQL (Microsoft) Certified
 - EMV 2000 (Europay, Mastercard, Visa) Certified
 - USB 1.1 and 2.0
 - USB CCID
 - ISO 7816
 - HBCI
- Other Features
 - Fast and Easy Certification Process
 - Supports LED Status Indicator (Green: ready; Red: busy)
 - Secure Pin Entry (SPE)
- PC/SC Driver support
 - Windows 98/ME®
 - Windows 2000®
 - Windows XP®
 - Windows CE 3.0®/CE.NET (Depending on Hardware)
 - Windows NT® 4.0 (On Request)
 - Linux®
 - MacOS X®
- Operating Voltage
 - 3.0V - 5.5V
- Temperature
 - -40°C to +85°C
- Packages
 - 32-pin VQFP or 32-pin QFN



CardMan®
Smart@Link

AT83C23OK

Summary

4307CS-SCR-03/07



This is a summary Document. A complete document can be found on the Omnikey Web site.<http://omnikey.aaitg.com>

Description

Smart Cards are increasingly being used for Payments, Home-Banking, Access Control, Internet Security, PKItokens, Health Care, Loyalty, etc.

The CardMan Smart@Link chip set is a ready to use precertified smart card reader interface, that can be implemented into USB hosts. It facilitates hardware integrators by reducing time-to-market and offers a unique opportunity to quickly and easily include smart card reader functionality in systems like PCs, Notebooks, Keyboards, Smart Card based Dongles, Monitors, Mice, PDAs, Thin Clients, Biometric devices etc. The already existing certifications and compliances guarantee a fast and easy certification process.

With its high performance Smart Card Interface CardMan Smart@Link supports smart-card technology of the future.

The integration in any USB system can be easily done without any firmware or software (driver) development, simply by embedding the CardMan Smart@Link design and chipset into the target system. The USB CCID support makes this process the easiest ever by connecting host and Smart Card Reader systems without the need of additional drivers.

CardMan Smart@Link combines Atmel's AT83C5123 microcontroller and Omnikey firmware.

For detailed information on the Omnikey firmware, please refer to the Omnikey web site: <http://omnikey.aaitg.com>.

In addition to the summary information contained in this document, please refer to the AT83C5123 datasheet for complete product information. This document is available on the Atmel web site www.atmel.com.

Pin Configurations

Figure 1. VQFP32 Package Pinout

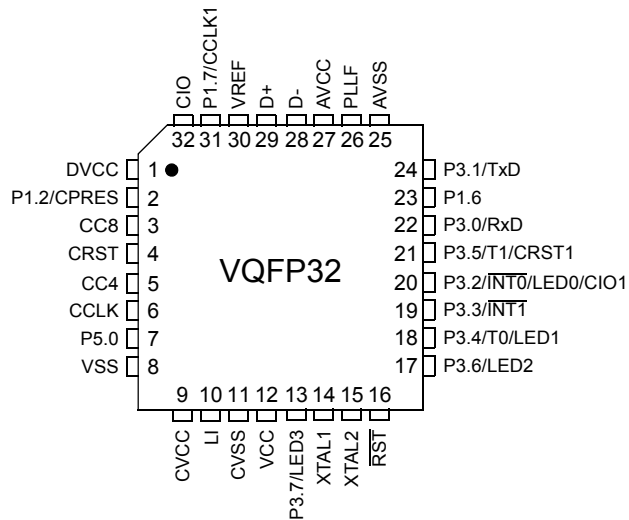
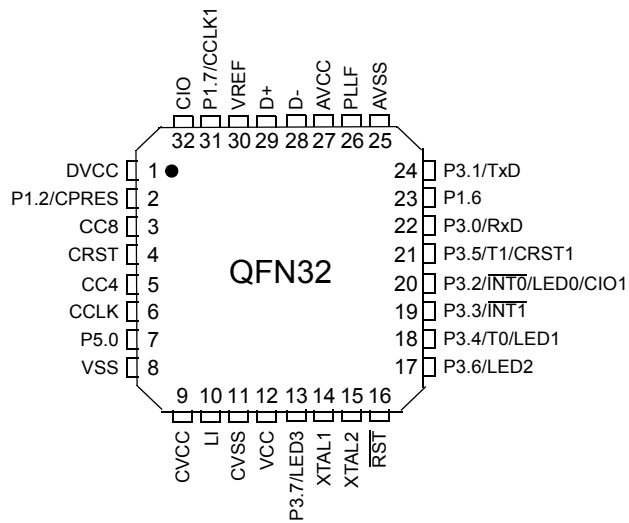


Figure 2. QFN32 Package Pinout



Pin Description

Table 1. Pin Description

Port	VQFP32	QFN32	Internal Power Supply	ESD	I/O	Reset Level	Alt
CIO	32	32	CVCC	6KV	I/O	0	Card interface-I/O pin CVcc inactive at reset . ESD tested with 10μF on CVcc. An external pull-up of 4.7KΩ is recommended to support ICC's with too high internal pull-ups.
CC8	3	3	CVCC	6KV	I/O	0	Card interface-C8 pin CVcc inactive at reset. ESD tested with 10μF on CVcc.
CPRES	2	2	VCC	2KV	I/O	1	Card Presence signal If P3.4 pin is connected to GND, the card inserted information generates a high level on CPRES pin. Else, a low level on this pin indicates that a card is inserted.
CC4	5	5	CVCC	6KV	I/O	0	Card interface-C4 pin CVcc inactive at reset. ESD tested with 10μF on CVcc.
CCLK	6	6	CVCC	6KV	O	0	Card interface-CLK pin CVcc inactive at reset. ESD tested with 10μF on CVcc.
CRST	4	4	CVCC	6KV	O	0	Card interface-RST pin CVcc inactive at reset. ESD tested with 10μF on CVcc.
P1.6	23	23	VCC	2KV	I/O	1	<i>For Serial reader:</i> Connect this to GND. <i>For USB reader:</i> Leave this pin unconnected.
P1.7	31	31	VCC	2KV	I/O	1	Leave this pin unconnected
P3.0	22	22	VCC	2KV	I/O	1	<i>For Serial reader: RxD:</i> Connect this pin to the host TxD signal. <i>For USB reader:</i> Connect this pin to GND.
P3.1	24	24	VCC	2KV	I/O	1	<i>For Serial reader: TxD:</i> Connect this pin to the host RxT signal. <i>For USB reader:</i> Leave this pin unconnected.
P3.2	20	20	VCC	2KV	I/O	1	<i>For Serial reader: INT0:</i> Connect this pin to host RTS signal. <i>For USB reader:</i> Connect this pin to GND.
P3.3	19	19	VCC	2KV	I/O	1	<i>For Serial reader:</i> Leave this pin unconnected. <i>For USB reader:</i> Connect this pin to GND.
P3.4	18	18	VCC	2KV	I/O	1	Eject Signal To support the eject of the smart card under control of the application. Please refer to Design-In Manual for additional information. This pin indicates also the polarity of Card Insertion Signal.
P3.5	21	21	VCC	2KV	I/O	1	<i>For Serial reader:</i> Connect this to GND. <i>For USB reader:</i> Leave this pin unconnected.
SCL	17	17	VCC	2KV	I/O	1	TWI Expansion (I²C compliant) May be used for memory extension, parallel port expanders and more. Please refer to the Design-IN Manual.
SDA	13	13	VCC	2KV	I/O	1	

Table 1. Pin Description (Continued)

Port	VQFP32	QFN32	Internal Power Supply	ESD	I/O	Reset Level	Alt
$\overline{\text{RST}}$	16	16	VCC		I/O		Reset Input The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal 10K pull-up resistor which allows the device to be reset by connecting a capacitor between this pin and VSS. Asserting $\overline{\text{RST}}$ when the chip is in Idle mode or Power-Down mode returns the chip to normal operation. The output is active for at least 12 oscillator periods when an internal reset occurs.
D+	29	29	DVCC		I/O		<i>For Serial reader:</i> Connect this pin to GND. <i>For USB reader:</i> USB Positive Data Upstream Port This pin requires an external serial resistor of 27 Ω (AT8xC122) or 33 Ω (AT83C5123) and a 1.5 K Ω pull-up to V_{REF} for full speed configuration.
D-	28	28	DVCC		I/O		<i>For Serial reader:</i> Connect this pin to GND. <i>For USB reader:</i> USB Negative Data Upstream Port This pin requires an external serial resistor of 27 Ω (AT8xC122) or 33 Ω (AT83C5123)
V_{REF}	30	30	AVCC		O		<i>For Serial reader:</i> Leave this pin unconnected. <i>For USB reader:</i> USB Voltage Reference: $3.0 < V_{REF} < 3.6 \text{ V}$ V_{REF} can be connected to D+ through a 1.5 K Ω resistor. The V_{REF} voltage is controlled by software.
XTAL1	14	14	VCC		I		Input to the on-chip inverting oscillator amplifier To use the internal oscillator, a crystal or an external oscillator must be connected to this pin.
XTAL2	15	15	VCC		O		Output of the on-chip inverting oscillator amplifier To use the internal oscillator, a crystal circuit must be connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.
PLL F	26	26	AVCC		O		PLL Low Pass Filter input Receives the RC network of the PLL low pass filter.
AVCC	27	27			PWR		Analog Supply Voltage AVCC is used to supply the internal 3.3V analog regulator which supplies the internal USB driver
VCC	12	12			PWR		Supply Voltage VCC is used to supply the internal 3.3V digital regulator which supplies the PLL, CPU core and internal I/O's
LI	10	10			PWR		DC/DC Input LI supplies the current for the charge pump of the DC/DC converter. - LI tied directly to VCC : the DC/DC converter must be configured in regulator mode. - LI tied to VCC through an external 10 μH coil : the DC/DC converter can be configured either in regulator or in pump mode.
CVCC	9	9			PWR		Card Supply Voltage CVCC is the output of internal DC/DC converter which supplies the Smart Card Interface. It must be connected to an external decoupling capacitor of 10 μF with the lowest ESR as this parameter influences on the CVCC noise

Table 1. Pin Description (Continued)

Port	VQFP32	QFN32	Internal Power Supply	ESD	I/O	Reset Level	Alt
DVCC	1	1			PWR		Digital Supply Voltage DVCC is the output of the internal analog 3.3V regulator which supplies the USB driver. This pin must be connected to an external 680nF decoupling capacitor if the USB interface is used. This output can be used by the application with a maximum of 10 mA.
CVSS	11	11			GND		DC/DC Ground CVSS is used to sink high shunt currents from the external coil
VSS	8	8			GND		Digital Ground VSS is used to supply the PLL, buffer ring and the digital core
AVSS	25	25			GND		Analog Ground AVSS is used to supply the USB driver.

Electrical Characteristics

Absolute Maximum Ratings

Ambiant Temperature Under Bias	-25°C to 85°C
Storage Temperature	-65°C to + 150°C
Voltage on V_{CC} to V_{SS}	-0.5 V to + 6.0V
Voltage on Any Pin to V_{SS}	-0.5 V to V_{CC} + 0.5 V
Power Dissipation	1 W

Note: Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Power Dissipation value is based on the maximum allowable die temperature and the thermal resistance of the package.

DC Parameters

$T_A = -40$ to $+85^\circ\text{C}$; $V_{SS} = 0$ V, $F_{CK_CPU} = 0$ to 24 MHz, $V_{CC} = 3.0$ V to 5.5V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		$0.2 V_{CC} - 0.1$	V	
V_{IH}	Input High Voltage except XTAL1, \overline{RST}	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage, XTAL1, \overline{RST}	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage: P0, ALE, PSEN			0.45	V	$I_{OL} = 1.6$ mA
V_{OH}	Output High Voltage: P0, ALE, PSEN	$0.9 V_{CC}$			V	$I_{OH} = 10$ μ A
V_{OL1}	Output Low Voltage: P3, P1.2, P1.6, P1.7			0.45	V	$I_{OL} = 0.8$ mA
V_{OH1}	Output High Voltage: P3, P1.2, P1.6, P1.7	$0.9 V_{CC}$			V	$I_{OH} = -10$ μ A
I_{IL}	Logical 0 Input Current ports 2 to 5 and P1.2, P1.6, P1.7, if Weak pull-up enabled			-50	μ A	$V_{in} = 0.45$ V
I_{LI}	Input Leakage Current			± 10	μ A	0.45 V $< V_{IN} < V_{CC}$
I_{TL}	Logical 1 to 0 transition Current, Port 51 configuration			-650	μ A	$V_{IN} = 2$ V
R_{MEDIUM}	Medium Pullup Resistor		10		k Ω	
R_{WEAK}	Weak Pullup Resistor		100		k Ω	
CIO	Capacitance of I/O Buffer			10	pF	$F_C = 1$ MHz $T_A = 25^\circ\text{C}$
DV _{CC}	Digital Supply Voltage	3	3.4	3.6	V	$C_L = 470$ nF
DI _{CC}	Digital Supply Output Current (DV _{CC} pin)			10	mA	$C_L = 100$ nF $F_{CK_CPU} = 24$ MHz
V_{PFDP}	Power Fail High Level Threshold		2.8	3	V	
V_{PFDM}	Power Fail Low Level Threshold	2,5	2.6		V	
t_{rise}, t_{fall}	V_{DD} rise and fall time	1 μ s		600	second	
R_{RST}	Internal reset pull-up resistor	5	10	30	k Ω	

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{PD}	Power down consumption		60 μ A 40 μ A	200 μ A 200 μ A		V _{CC} = 5.5V V _{CC} = 3.6V
I_{CCIDLE}	Power Supply current in IDLE mode			0.4*F+2	mA	V _{CC} = 5.5V (F in MHz)
I_{CCOP}	Power Supply current in Active mode with DC/DC ON			1.6*F+2	mA	V _{CC} = 5.5V (F in MHz)
I_{CCOP}	Power Supply current in Active mode with DC/DC OFF			0.8*F+2	mA	V _{CC} = 5.5V (F in MHz)

I_{CC} Current Test Conditions

Figure 3. Power Down Mode

All other pins are disconnected.

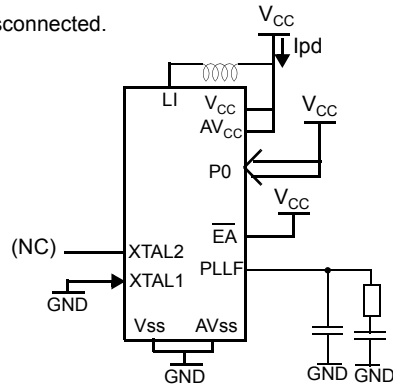
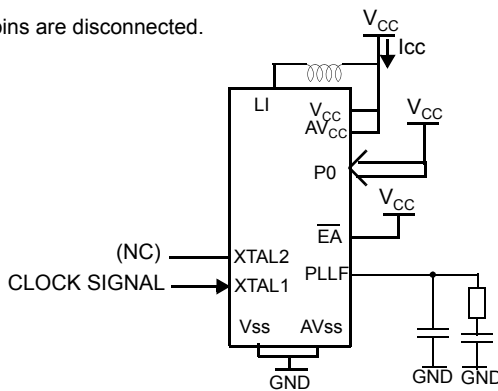


Figure 4. Active and Idle Mode

All other pins are disconnected.



LED's

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I _{OL}	Output Low Current, P3.0 and P3.7 LED modes	1	3	5	mA	2 mA configuration
		2	6	8	mA	4 mA configuration
		5	10	20	mA	10 mA configuration

Note: 1. (T_A = -20°C to +50°C, V_{CC} - V_{OL} = 2 V)

Smart Card Interface

Card VCC 5V (for IEC7816-3 Class A cards)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{CC}	Power Supply	3.0		5.5	V	
Cl _{CC_ovf}	Card Supply Current overflow		100		mA	
CV _{CC}	Card Supply Voltage	4.6		5.4	V	V _{cc} Min = 4.0V, Cl _{CC} = 60 mA V _{cc} Min = 3.0V, Cl _{CC} = 30 mA
	Ripple on Card Voltage			200	mV	0 < Cl _{cc} < 60 mA
CV _{CC}	Card Supply Voltage during spike on I _{cc}	4.5		5.5		Max. charge 20 nA.s Max. duration 400 ns Max. variation Cl _{CC} 100 mA
T _{OFF}	CV _{cc} to 0			750	μs	Cload=10μF, Lload=10μH Vcard = CV _{cc} to 0.4V
T _{ON}	0 to CV _{cc}			750	μs	Cload=10μF, Lload=10μH Vcard = 0V to CV _{cc} With Boost at 60%

Card VCC 3V Power Supply (for IEC7816-3 Class B cards)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{CC}	Power Supply	3.0		5.5	V	
Cl _{CC_ovf}	Card Supply Current overflow		100		mA	
CV _{CC}	Card Supply Voltage	2.76		3.24	V	V _{cc} Min = 3.6V, Cl _{CC} = 55mA V _{cc} Min = 3.0V, Cl _{CC} = 30 mA
	Ripple on Vcard			200	mV	0 < Cl _{CC} < 55mA
CV _{CC}	Card Supply Voltage during spike on I _{cc}	2.7		3.3	V	Maxi. charge 10nA.s Max. duration 400 ns Max. variation Cl _{CC} 50mA
T _{OFF}	CV _{cc} to 0			750	μs	Cload=10μF, Lload=10μH Vcard = CV _{cc} to 0.4V
T _{ON}	0 to CV _{cc}			750	μs	Cload=10μF, Lload=10μH Vcard = 0V to CV _{cc} With Boost at 60%

Card VCC 1.8V Power Supply (for IEC7816-3 Class C cards)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{CC}	Power Supply	3.0		5.5	V	
Cl _{CC_ovf}	Card Supply Current overflow		100		mA	
CV _{CC}	Card Supply Voltage	1.68		1.92	V	Cl _{CC} = 35 mA
T _{OFF}	CV _{CC} to 0			750	μs	Cl _{load} =10μF, L _{load} =10μH V _{card} = CV _{CC} to 0.4V
T _{ON}	0 to CV _{CC}			750	μs	Cl _{load} =10μF, L _{load} =10μH V _{card} = 0V to CV _{CC} With Boost at 60%

- Notes: 1. Test conditions, Capacitor 10 μF, Inductance 10 μH.
2. Ceramic X7R, SMD type capacitor with minimum ESR or 250 mΩ is mandatory

Smart Card CCLK, DC parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{OL}	Output Low Voltage	0 ⁽¹⁾		0.4 0.15 CV _{CC} 0.15 CV _{CC}	V	I _{OH} = 50 μA (5V until 2009) I _{OH} = 100 μA (5V from 2009) I _{OH} = 100 μA (3V & 1.8V)
I _{OL}	Output Low Current			15	mA	
V _{OH}	Output High Voltage	CV _{CC} -0.5 0.8 CV _{CC} 0.8 CV _{CC}		CV _{CC}	V	I _{OH} = 50μA (+5V until 2009) I _{OH} = 100 μA (+5V from 2009) I _{OH} = 100 μA (+3V & 1.8V)
I _{OH}	Output High Current			15	mA	
t _R t _F	Rise and Fall delays			14.5 15.5 32	ns	C _{IN} =30pF (5V) C _{IN} =30pF (3V) C _{IN} =30pF (1.8V)
	Voltage Stability	-0.25 CV _{CC} -0.5		0.4 CV _{CC} CV _{CC} + 0.25	V	Low level High level
	Frequency variation (Jitter)			1%		
	Cycle ratio	45%		55%		

- Notes: 1. The voltage on CLK should remain between -0.3V and V_{CC}+0.3V during dynamic operation.

Smart Card CIO, DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Input Low Voltage	0 ⁽¹⁾		0.2 CV _{CC}	V	
I _{IL}	Input Low Current			500	μA	
V _{IH}	Input High Voltage	0.6 CV _{CC}		CV _{CC}	V	
I _{IH}	Input High Current			-20 / +20	μA	
V _{OL}	Output Low Voltage	0 ⁽¹⁾		0.15 CV _{CC}	V	I _{OL} = 1mA (5V & 3V)) I _{OL} = 0.5 mA (1.8V) External 10K pull-up tied to CV _{CC}

Smart Card CIO, DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL}	Output Low Current			15	mA	
V_{OH}	Output High Voltage	$0.8 CV_{CC}$		$CV_{CC} (1)$	V	$I_{OH} = 20 \mu A$ External 10K pull-up resistor tied to CV_{CC}
I_{OH}	Output High Current			15	mA	
	Voltage Stability	-0.25 $0.8 CV_{CC}$		0.4 $CV_{CC} + 0.25$	V	Low level High level
$t_R t_F$	Rise and Fall delays			0.8	μs	$C_{IN}=30pF$.

Note: 1. The voltage on RST should remain between -0.3V and $V_{CC}+0.3V$ during dynamic operation.

Smart Card RST, CC4, CC8, DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low Voltage	$0^{(1)}$		0.4 $0.12 CV_{CC}$ $0.12 CV_{CC}$	V	$I_{OL} = 50 \mu A$ (5V until 2009) $I_{OL} = 200 \mu A$ (5V from 2009) $I_{OL} = 200 \mu A$ (3V & 1.8V)
I_{OL}	Output Low Current			15	mA	
V_{OH}	Output High Voltage	$CV_{CC}-0.5$ $0.8 CV_{CC}$ $0.8 CV_{CC}$		$CV_{CC}^{(1)}$	V	$I_{OH} = 50 \mu A$ (+5V until 2009) $I_{OH} = 150 \mu A$ (+5V from 2009) $I_{OH} = 150 \mu A$ (+3V & 1.8V)
I_{OH}	Output High Current			15	mA	
$t_R t_F$	Rise and Fall delays			0.8	μs	$C_{IN}=30 pF$
	Voltage Stability	-0.25 $CV_{CC}-0.5$		0.4 CV_{CC} $CV_{CC} + 0.25$		Low level High level

Note: 1. The voltage on RST should remain between -0.3V and $V_{CC}+0.3V$ during dynamic operation.

Card Presence (P1.2) DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL1}	CPRES weak pull-up output current	3	10	25	μA	P1.2=1, short to VSS Pull-up enabled

USB Interface

Figure 5. USB Interface

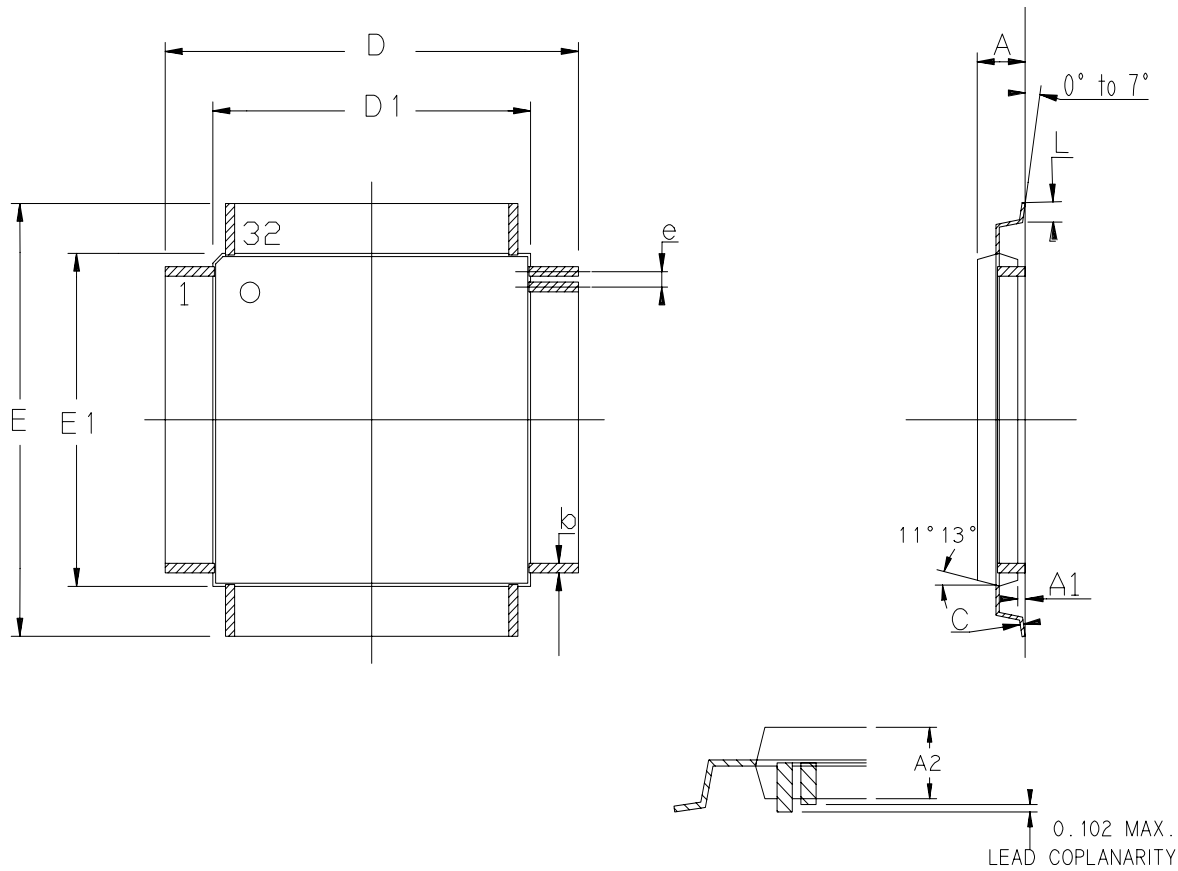
Symbol	Parameter	Min	Typ ⁽⁵⁾	Max	Unit
V_{REF}	USB Reference Voltage	3.0		3.6	V
V_{IH}	Input High Voltage for D+ and D- (driven)	2.0		4.0	V
V_{IHZ}	Input High Voltage for D+ and D- (floating)	2.7		3.6	V
V_{IL}	Input Low Voltage for D+ and D-			0.8	V
V_{OH}	Output High Voltage for D+ and D-	2.8		3.6	V
V_{OL}	Output Low Voltage for D+ and D-	0.0		0.3	V

Ordering information

Part Number	Voltage Range (V)	Temperature Range	Package	Packing
AT83C23OK203-SISIM	3.0 - 5.5	Industrial	PLCC28	Stick
AT83C23OK203-SIRIM	3.0 - 5.5	Industrial	PLCC28	Tape & Reel
AT83C23OK203-RATIM	3.0 - 5.5	Industrial	VQFP32	Tray
AT83C23OK203-RARIM	3.0 - 5.5	Industrial	VQFP32	Tape & Reel
AT83C23OK203-RATUM	3.0 - 5.5	Industrial & Green	VQFP32	Tray
AT83C23OK203-RARUM	3.0 - 5.5	Industrial & Green	VQFP32	Tape & Reel
AT83C23OK203-PUTUM	3.0 - 5.5	Industrial & Green	QFN32	Tray
AT83C23OK203-PURUM	3.0 - 5.5	Industrial & Green	QFN32	Tape & Reel

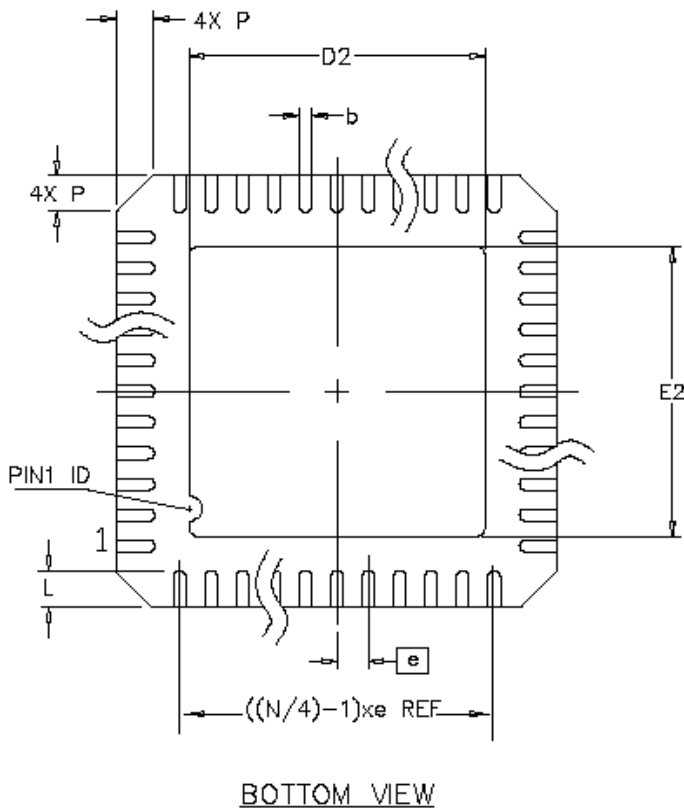
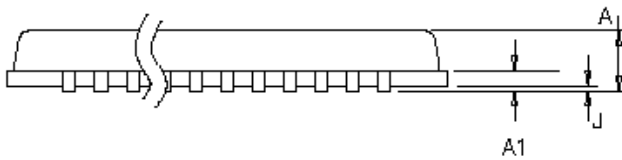
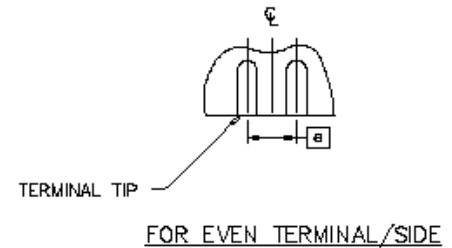
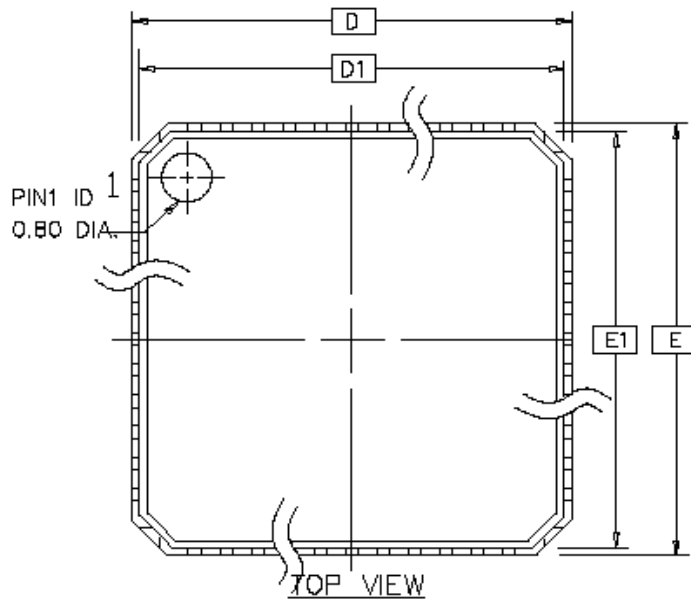
Mechanical Description

VQFP32 Package



	MM		INCH	
	Min	Max	Min	Max
A	-	1.60	-	.063
A1	0.05	0.15	.002	.006
A2	1.35	1.45	.053	.057
C	0.09	0.20	.004	.008
D	9.00 BSC		.354 BSC	
D1	7.00 BSC		.276 BSC	
E	9.00 BSC		.354 BSC	
E1	7.00 BSC		.276 BSC	
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
b	0.30	0.45	.012	.018

QFN32 Package



	MM			INCH		
	MIN	NDM	MAX	MIN	NDM	MAX
A	-	0.85	0.90	-	.033	.035
J	0.00	0.01	0.05	.000	.000	.002
A1	0.20 ref			.008 ref		
D/E	7.00 BSC			.276 BSC		
D1/E1	6.75 BSC			.266 BSC		
D2/E2	4.95	5.10	5.25	.195	.201	.207
N	32					
P	0.24	0.42	0.60	.009	.016	.024
e	0.65 BSC			.026 BSC		
L	0.50	0.60	0.75	.020	.024	.030
b	0.23	0.28	0.35	.009	.011	.014



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