

Document Title

**32Kx8 Bit High Speed Static RAM(5V Operating), Evolutionary Pin out.
Operated at Commercial Temperature Range.**

Revision History

| <u>Rev No.</u> | <u>History</u> | <u>Draft Data</u> | <u>Remark</u> | | | | | | | | | | | | | | | | | | |
|----------------|--|------------------------------------|-------------------------------------|------------------------------------|-----|------------|-------------|-----|-------------|-------------|-----|-----------|---------|------|--------------|--------------|-----|--------------|--------------|--|--|
| Rev. 0.0 | Initial release with Preliminary. | Apr. 1st, 1994 | Preliminary | | | | | | | | | | | | | | | | | | |
| Rev. 1.0 | Release to final Data Sheet. 1. Delete Preliminary | May 14th, 1994 | Final | | | | | | | | | | | | | | | | | | |
| Rev. 2.0 | Update A.C parameters 2.1. Updated A.C parameters | Oct. 4th, 1994 | Final | | | | | | | | | | | | | | | | | | |
| | <table border="1"> <thead> <tr> <th>Items</th> <th>Previous spec. (12/15/20ns part)</th> <th>Updated spec. (12/15/20ns part)</th> </tr> </thead> <tbody> <tr> <td>tOE</td> <td>- / 8/10ns</td> <td>- / 7 /9 ns</td> </tr> <tr> <td>tCW</td> <td>- /12/ - ns</td> <td>- /11/ - ns</td> </tr> <tr> <td>tHZ</td> <td>8/10/10ns</td> <td>6/7/8ns</td> </tr> <tr> <td>tOHZ</td> <td>- / 8 / - ns</td> <td>- / 7 / - ns</td> </tr> <tr> <td>tDW</td> <td>- / 9 / - ns</td> <td>- / 8 / - ns</td> </tr> </tbody> </table> | Items | Previous spec. (12/15/20ns part) | Updated spec. (12/15/20ns part) | tOE | - / 8/10ns | - / 7 /9 ns | tCW | - /12/ - ns | - /11/ - ns | tHZ | 8/10/10ns | 6/7/8ns | tOHZ | - / 8 / - ns | - / 7 / - ns | tDW | - / 9 / - ns | - / 8 / - ns | | |
| Items | Previous spec. (12/15/20ns part) | Updated spec. (12/15/20ns part) | | | | | | | | | | | | | | | | | | | |
| tOE | - / 8/10ns | - / 7 /9 ns | | | | | | | | | | | | | | | | | | | |
| tCW | - /12/ - ns | - /11/ - ns | | | | | | | | | | | | | | | | | | | |
| tHZ | 8/10/10ns | 6/7/8ns | | | | | | | | | | | | | | | | | | | |
| tOHZ | - / 8 / - ns | - / 7 / - ns | | | | | | | | | | | | | | | | | | | |
| tDW | - / 9 / - ns | - / 8 / - ns | | | | | | | | | | | | | | | | | | | |
| | 2.2. Add Voh1=3.95V with the test condition as Vcc=5V±5% at 25°C | | | | | | | | | | | | | | | | | | | | |
| Rev. 3.0 | 3.1. Add 28-TSOP1 Package. 3.2. Add L-version. 3.3. Add Data Rentention Characteristics. | Feb. 22th, 1996 | Final | | | | | | | | | | | | | | | | | | |

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

32K x 8 Bit High-Speed CMOS Static RAM

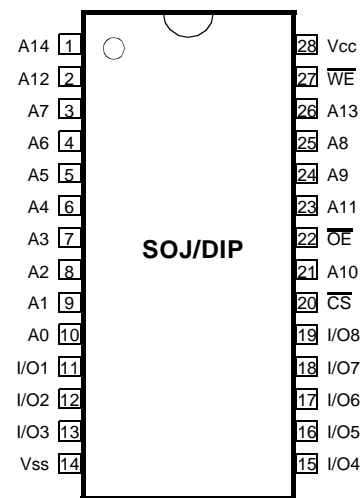
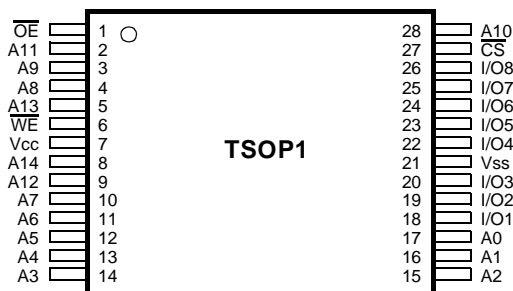
FEATURES

- Fast Access Time 12, 15, 20ns (Max.)
- Low Power Dissipation
 - Standby (TTL) : 40µA (Max.)
 - (CMOS) : 2µA (Max.)
 - 0.1µA (Max.)- L-ver. only
- Operating KM68257C/CL - 12 : 165µA (Max.)
- KM68257C/CL - 15 : 150µA (Max.)
- KM68257C/CL - 20 : 140µA (Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage : 2V(Min.)- L-ver. only
- Standard Pin Configuration
 - KM68257C/CLP : 28-DIP-300
 - KM68257C/CLJ : 28-SOJ-300
 - KM68257C/CLTG : 28-TSOP1-0813, 4F

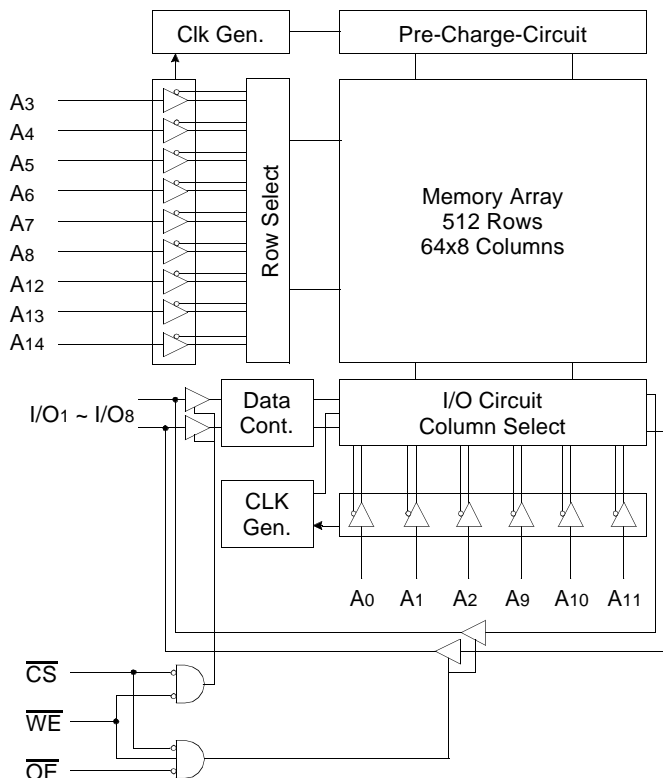
GENERAL DESCRIPTION

The KM68257C is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits. The KM68257C uses 8 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68257C is packaged in a 300 mil 28-pin plastic DIP, SOJ or TSOP1 forward.

PIN CONFIGURATION (Top View)



FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION

| Pin Name | Pin Function |
|-----------------|---------------------|
| A0 - A14 | Address Inputs |
| \overline{WE} | Write Enable |
| \overline{CS} | Chip Select |
| \overline{OE} | Output Enable |
| I/O1 ~ I/O8 | Data Inputs/Outputs |
| Vcc | Power(+5.0V) |
| Vss | Ground |

ABSOLUTE MAXIMUM RATINGS*

| Parameter | Symbol | Rating | Unit |
|---------------------------------------|------------------------------------|-------------|------|
| Voltage on Any Pin Relative to Vss | V _{IN} , V _{OUT} | -0.5 to 7.0 | V |
| Voltage on Vcc Supply Relative to Vss | V _{CC} | -0.5 to 7.0 | V |
| Power Dissipation | P _D | 1.0 | W |
| Storage Temperature | T _{STG} | -65 to 150 | °C |
| Operating Temperature | T _A | 0 to 70 | °C |

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A=0 to 70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|-------------------|-----------------|-------|-----|------------------------|------|
| Supply Voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V |
| Ground | V _{SS} | 0 | 0 | 0 | V |
| Input Low Voltage | V _{IH} | 2.2 | - | V _{CC} +0.5** | V |
| Input Low Voltage | V _{IL} | -0.5* | - | 0.8 | V |

* V_{IL}(Min) = -2.0(Pulse Width ≤ 10ns) for I_L ≤ 20mA

** V_{IH}(Max) = V_{CC}+2.0V(Pulse Width ≤ 10ns) for I_L ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A=0 to 70°C, V_{CC}=5.0V±10% unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Max | Unit | |
|---------------------------|--------------------|---|--------|------|------|-----|
| Input Leakage Current | I _{LI} | V _{IN} = V _{SS} to V _{CC} | -2 | 2 | μA | |
| Output Leakage Current | I _{LO} | $\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} = V _{SS} to V _{CC} | -2 | 2 | μA | |
| Operating Current | I _{CC} | Min. Cycle, 100% Duty $\overline{CS}=V_{IL}$, V _{IN} = V _{IH} or V _{IL} , I _{OUT} =0mA | 12ns | - | 165 | mA |
| | | | 15ns | - | 150 | |
| | | | 20ns | - | 140 | |
| Standby Current | ISB | Min. Cycle, $\overline{CS}=V_{IH}$ | - | 40 | mA | |
| | ISB1 | f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V | Normal | - | | 2 |
| | | | L-ver | - | | 0.1 |
| Output Low Voltage Level | V _{OL} | I _{OL} =8mA | - | 0.4 | V | |
| Output High Voltage Level | V _{OH} | I _{OH} =-4mA | 2.4 | - | V | |
| | V _{OH1} * | I _{OH1} =0.1mA | - | 3.95 | V | |

* V_{CC}=5.0V±5% Temp.=25°C

CAPACITANCE*(T_A =25°C, f=1.0MHz)

| Item | Symbol | Test Conditions | MIN | Max | Unit |
|--------------------------|------------------|----------------------|-----|-----|------|
| Input/Output Capacitance | C _{I/O} | V _{I/O} =0V | - | 8 | pF |
| Input Capacitance | C _{IN} | V _{IN} =0V | - | 7 | pF |

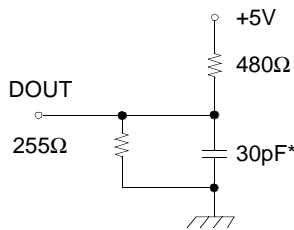
* NOTE : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS($T_A=0$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

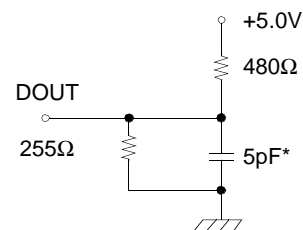
| Parameter | Value |
|--|--------------|
| Input Pulse Levels | 0V to 3V |
| Input Rise and Fall Times | 3ns |
| Input and Output timing Reference Levels | 1.5V |
| Output Loads | See below |

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

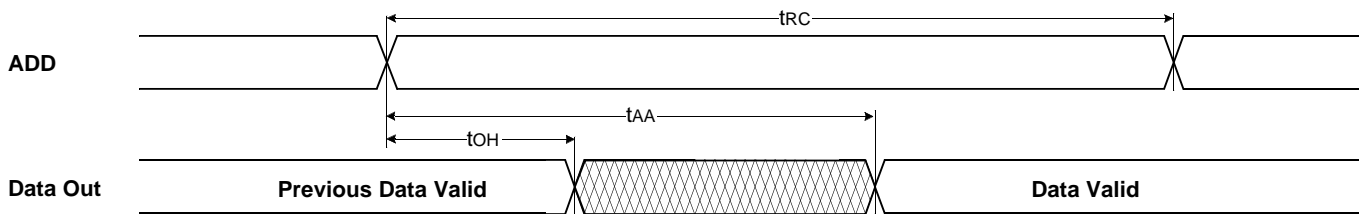
| Parameter | Symbol | KM68257C/CL-12 | | KM68257C/CL-15 | | KM68257C/CL-20 | | Unit |
|------------------------------------|--------|----------------|-----|----------------|-----|----------------|-----|-------------|
| | | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | tRC | 12 | - | 15 | - | 20 | - | ns |
| Address Access Time | tAA | - | 12 | - | 15 | - | 20 | ns |
| Chip Select to Output | tCO | - | 12 | - | 15 | - | 20 | ns |
| Output Enable to Valid Output | tOE | - | 6 | - | 7 | - | 9 | ns |
| Chip Enable to Low-Z Output Access | tLZ | 3 | - | 3 | - | 3 | - | ns |
| Output Enable to Low-Z Output | tOLZ | 0 | - | 0 | - | 0 | - | ns |
| Chip Disable to High-Z Output | tHZ | 0 | 6 | 0 | 7 | 0 | 10 | ns |
| Output Disable to High-Z Output | tOHZ | 0 | 6 | 0 | 7 | 0 | 10 | ns |
| Output Hold from Address Change | tOH | 3 | - | 3 | - | 3 | - | ns |
| Chip Selection to Power Up Time | tPU | 0 | - | 0 | - | 0 | - | ns |
| Chip Selection to Power DownTime | tPD | - | 12 | - | 15 | - | 20 | ns |

WRITE CYCLE

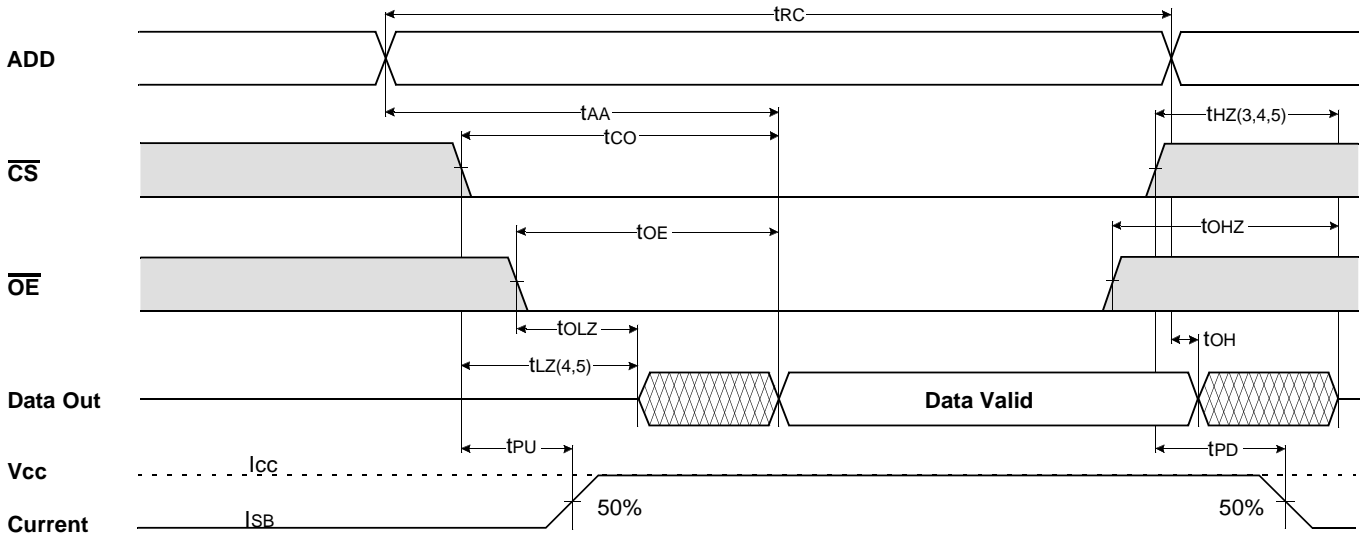
| Parameter | Symbol | KM68257C/CL-12 | | KM68257C/CL-15 | | KM68257C/CL-20 | | Unit |
|--|--------|----------------|-----|----------------|-----|----------------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | tWC | 12 | - | 15 | - | 20 | - | ns |
| Chip Select to End of Write | tCW | 9 | - | 11 | - | 13 | - | ns |
| Address Setup Time | tAS | 0 | - | 0 | - | 0 | - | ns |
| Address Valid to End of Write | tAW | 9 | - | 12 | - | 13 | - | ns |
| Write Pulse Width(\overline{OE} High) | tWP | 9 | - | 12 | - | 13 | - | ns |
| Write Pulse Width(\overline{OE} Low) | tWP1 | 12 | - | 15 | - | 20 | - | ns |
| Write Recovery Time | tWR | 0 | - | 0 | - | 0 | - | ns |
| Write to Output High-Z | tWHZ | 0 | 6 | 0 | 8 | 0 | 8 | ns |
| Data to Write Time Overlap | tDW | 7 | - | 8 | - | 10 | - | ns |
| Data Hold from Write Time | tdH | 0 | - | 0 | - | 0 | - | ns |
| End Write to Output Low-Z | tOW | 0 | - | 0 | - | 0 | - | ns |

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



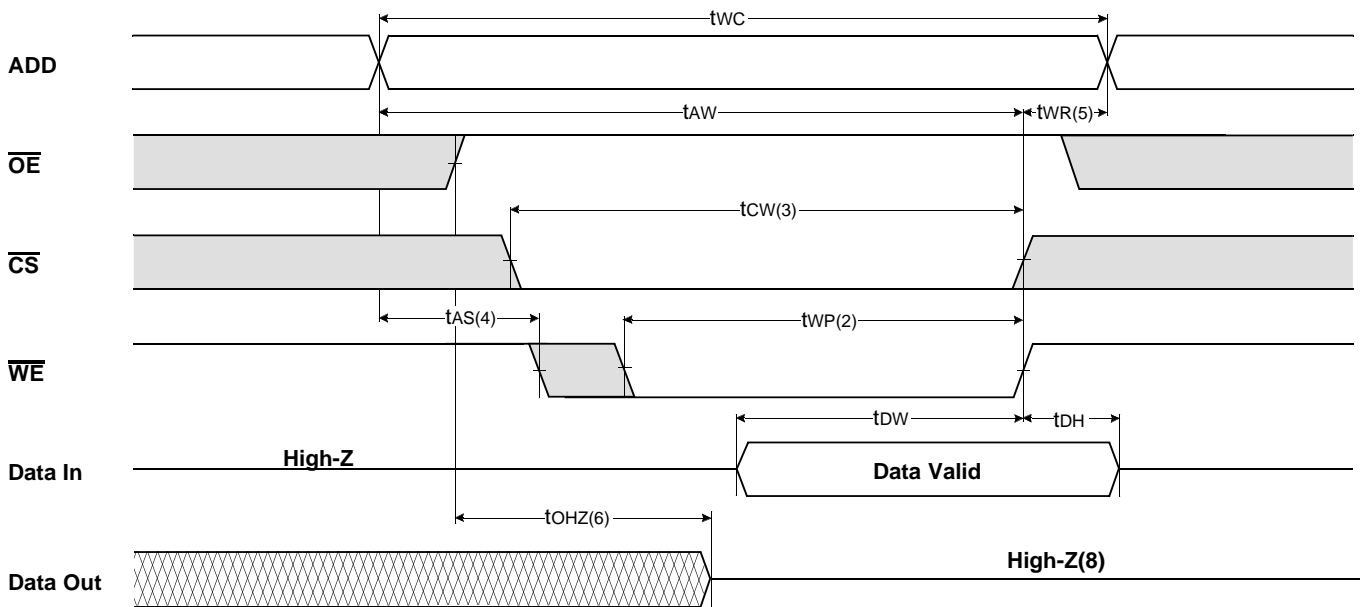
TIMING WAVE FORM OF READ CYCLE(2) $\overline{WE}=V_{IH}$



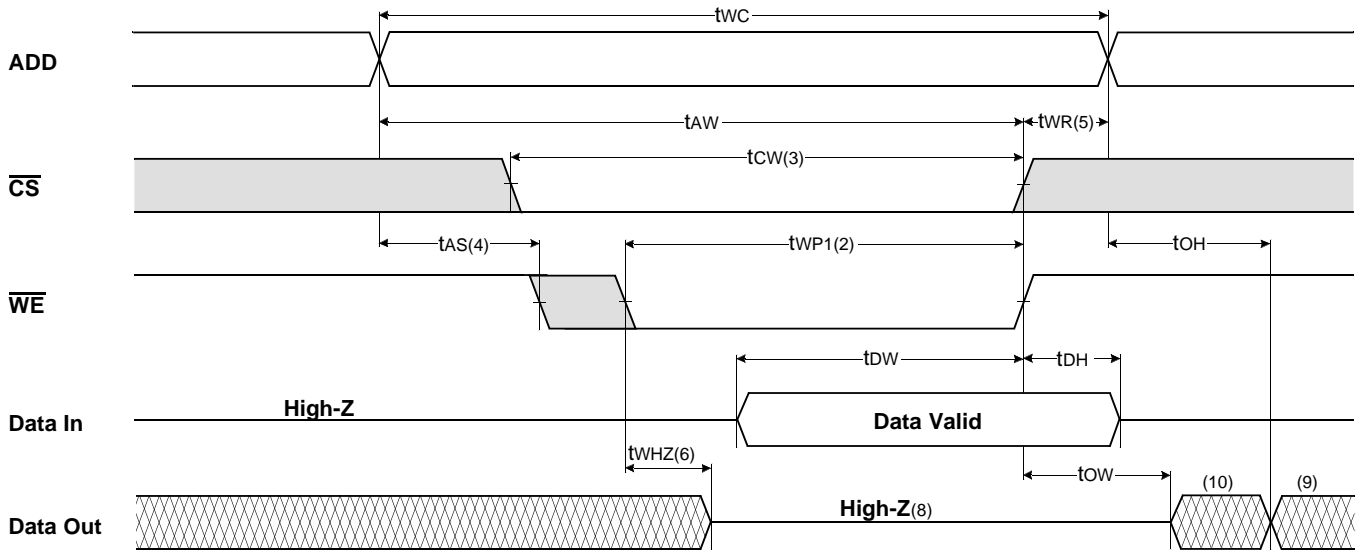
NOTES(READ CYCLE)

1. \overline{WE} is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OH} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} Levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\% E$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with \overline{CS} transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

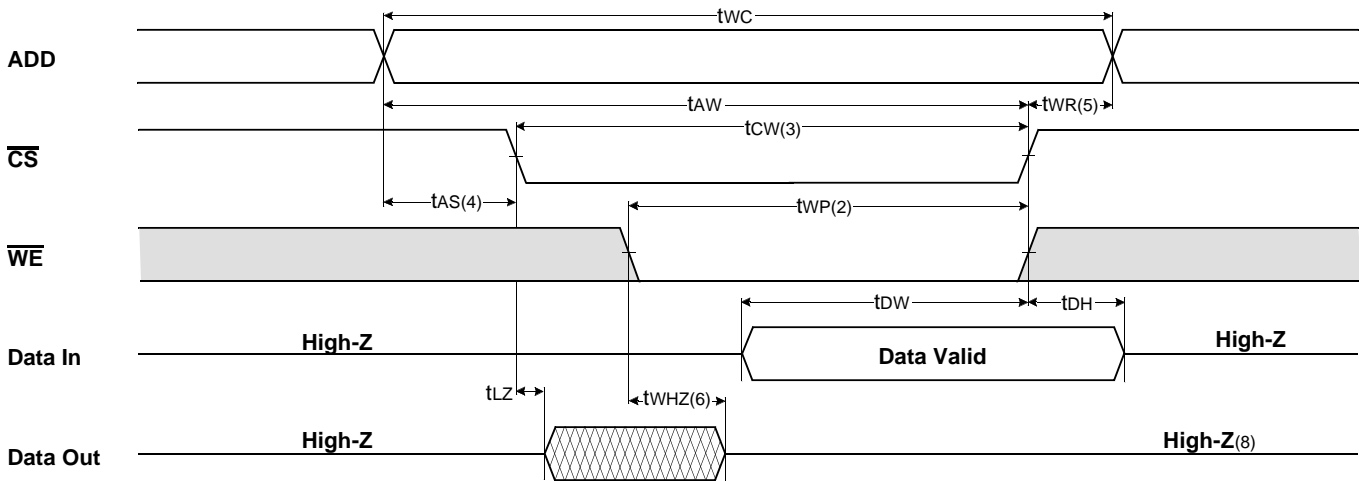
TIMING WAVE FORM OF WRITE CYCLE(1) $\overline{OE}=\text{Clock}$



TIMING WAVE FORM OF WRITE CYCLE(2) \overline{OE} =Low Fixed



TIMING WAVE FORM OF WRITE CYCLE(3) \overline{CS} =Controlled



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low ; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of \overline{CS} going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.
6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
8. If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When \overline{CS} is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

| \overline{CS} | \overline{WE} | \overline{OE} | Mode | I/O Pin | Supply Current |
|-----------------|-----------------|-----------------|----------------|---------|-------------------|
| H | X | X* | Not Select | High-Z | I_{SB}, I_{SB1} |
| L | H | H | Output Disable | High-Z | I_{CC} |
| L | H | L | Read | DOUT | I_{CC} |
| L | L | X | Write | DIN | I_{CC} |

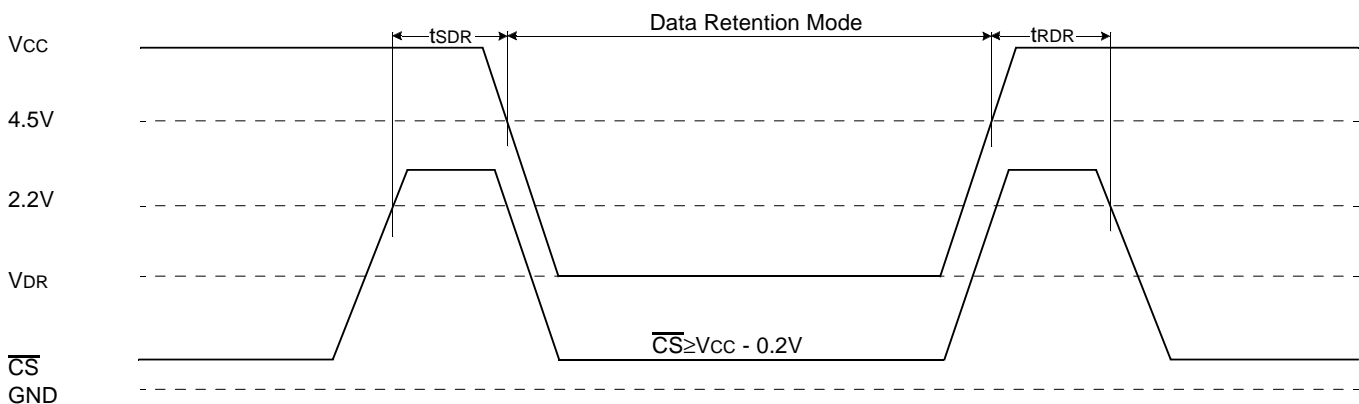
* NOTE : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA = 0 to 70°C)

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|----------------------------|--------|--|------|------|------|---------|
| VCC for Data Retention | VDR | $\overline{CS} \geq V_{CC} - 0.2V$ | 2.0 | - | 5.5 | V |
| Data Retention Current | IDR | $V_{CC} = 3.0V, \overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | - | - | 0.07 | μA |
| Data Retention Set-Up Time | tSDR | See Data Retention Wave form(below) | 0 | - | - | ns |
| Recovery Time | tRDR | | 5 | - | - | ms |

* L-Ver only.

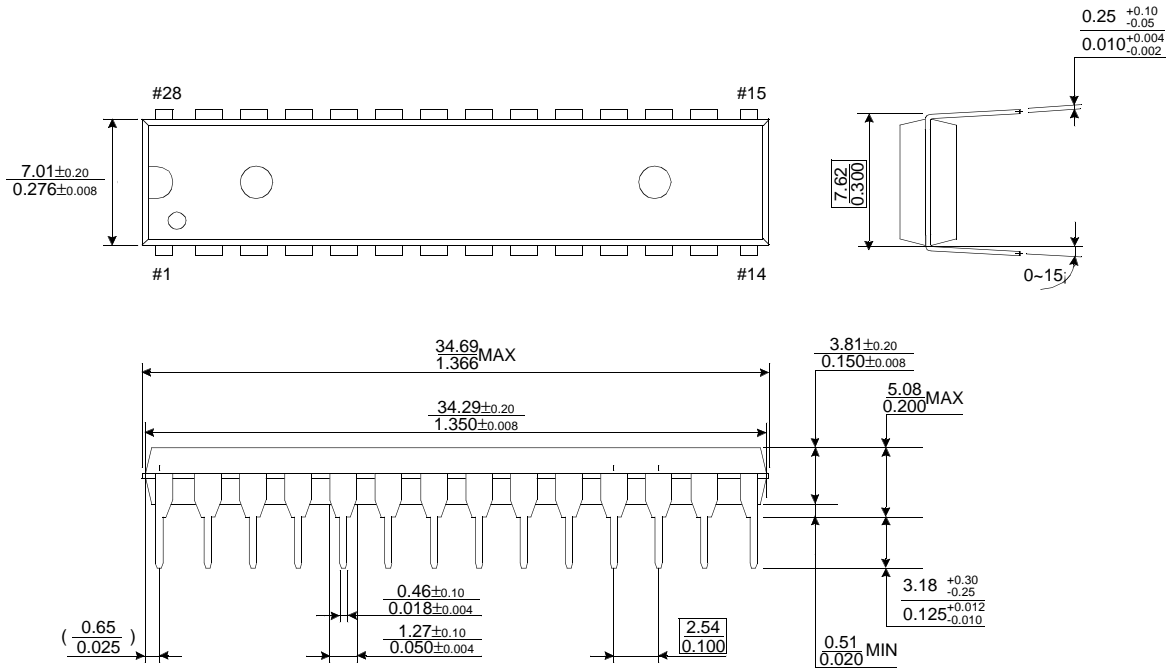
DATA RETENTION WAVE FORM(\overline{CS} Controlled)



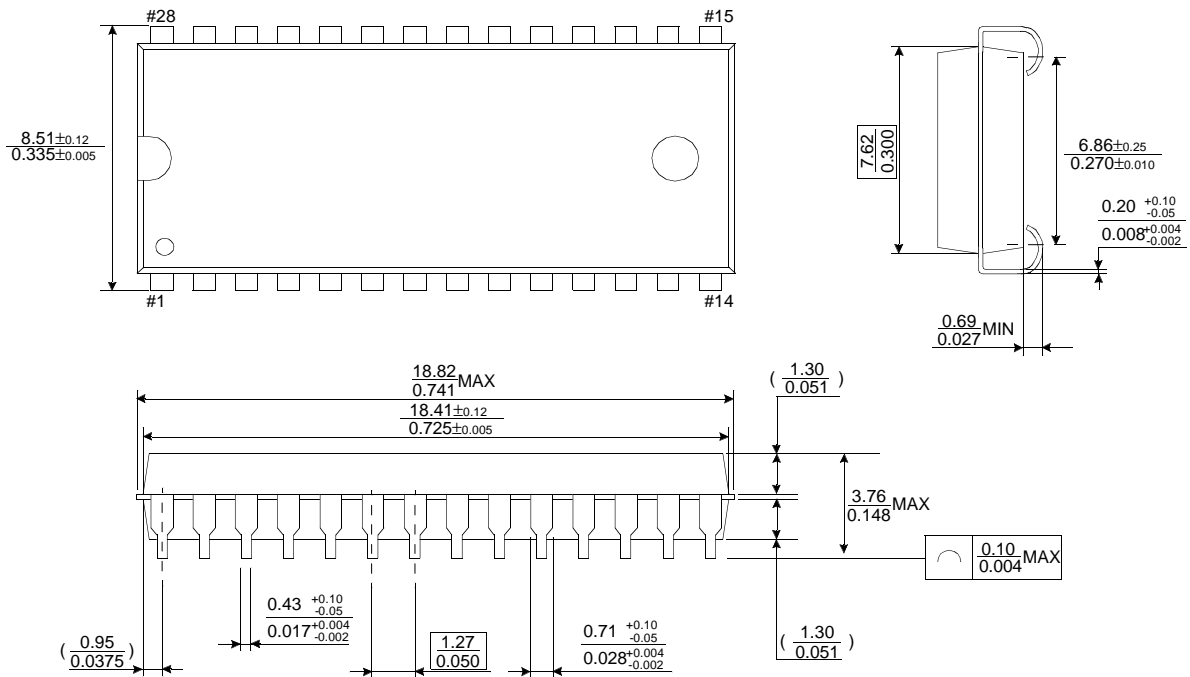
PACKAGE DIMENSIONS

28-DIP-300

Units : Inches (millimeters)



28-SOJ-300



PACKAGE DIMENSIONS

28-TSOP1-0813.4F

Units : Inches (millimeters)

