Document Title

128Kx8 High Speed Static RAM(5V Operating), Revolutionary Pin out.
Operated at Commercial and Industrial Temperature Range.

Revision History

Rev. No.	History	Draft Data	Remark
Rev. 0.0	Initial release with Preliminary.	Apr. 22th, 1995	Preliminary
Rev. 1.0	Release to final Data Sheet. 1.1. Delete Preliminary	Feb. 29th, 1996	Final
Rev. 2.0	Update D.C parameters. 2.1. Update D.C parameters	Jul. 16th, 1996	Final

Items	Previous spec. (12/15/17/20ns part)	Updated spec. (12/15/17/20ns part)
Icc	200/190/180/170mA	170/165/165/160mA
Isb	30mA	25mA
Isb_1	10mA	8mA

Rev. No.	History	Draft Data	Remark

Rev. 3.0	Add Industrial Temperature Range parts and 300mil-SOJ PKG.
	3.1. Add 32-Pin 300mil-SOJ Package.
	3.2. Add Industrial Temperature Range parts with the same parameters as Commercial Temperature Range parts.
	  3.2.1. Add KM68002AI parts for Industrial Temperature Range.
	  3.2.2. Add ordering information.
	  3.2.3. Add the condition for operating at Industrial Temp. Range.
	3.3. Add the test condition for Voh1 with Vcc=5V±5% at 25°C
	3.4. Add timing diagram to define t_{WP} as ″(**Timing Wave Form of Write Cycle($\overline{CS}$=Controlled)**″
		Jun. 2nd, 1997	Final

Rev. 4.0	4.1. Delete 17ns Part	Feb. 25th, 1998	Final

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128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12, 15, 20ns(Max.)
- Low Power Dissipation
  Standby (TTL)   : 25mA(Max.)
              (CMOS) :   8mA(Max.)
  Operating KM681002A - 12 : 170mA(Max.)
              KM681002A - 15 : 165mA(Max.)
              KM681002A - 20 : 160mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
              KM681002AJ : 32-SOJ-400
   KM681002AT: 32-TSOP2-400F

GENERAL DESCRIPTION

The KM681002A is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681002A uses 8 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681002A is packaged in a 400mil 32-pin plastic SOJ or TSOP2 forward.

ORDERING INFORMATION

KM681002A -12/15/20	Commercial Temp.
KM681002AI -12/15/20	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM
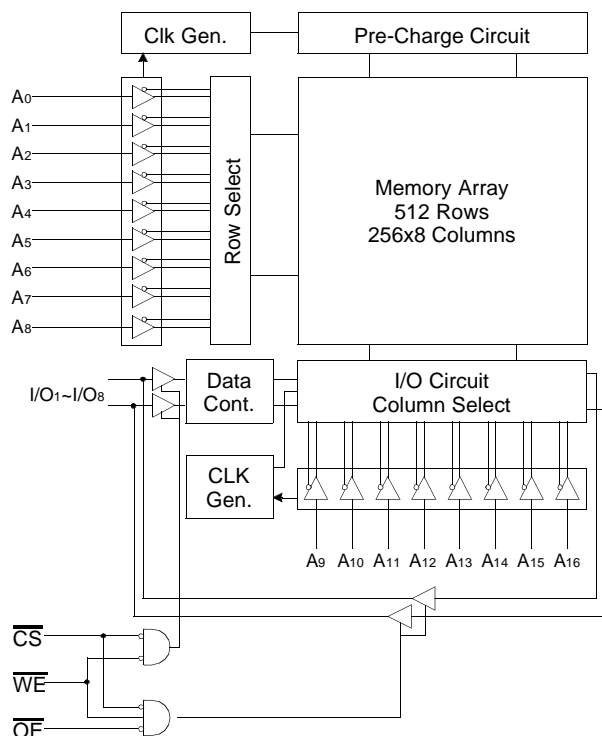
PIN CONFIGURATION (Top View)
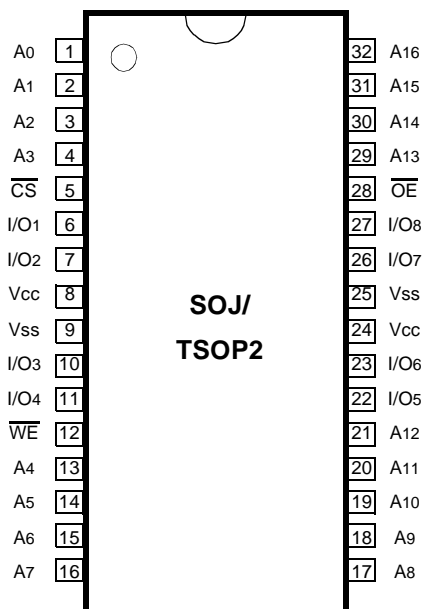
PIN FUNCTION

Pin Name	Pin Function
A_0 - A_{16}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1 ~ I/O_8	Data Inputs/Outputs
V_{CC}	Power(+5.0V)
V_{SS}	Ground

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ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		Vcc	-0.5 to 7.0	V
Power Dissipation		PD	1.0	W
Storage Temperature		TSTG	-65 to 150	°C
Operating Temperature	Commercial	TA	0 to 70	°C
	Industrial	TA	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and
  functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.
  Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

NOTE: The above parameters are also guaranteed at industrial temperature range.
      * VIL(Min) = -2.0V a.c(Pulse Width≤10ns) for I≤20mA
      ** VIH(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I≤20mA

DC AND OPERATING CHARACTERISTICS(TA=0 to 70°C, Vcc=5.0V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	VIN=Vss to Vcc		-2	2	μA
Output Leakage Current	ILO	$\overline{CS}$=VIH or $\overline{OE}$=VIH or $\overline{WE}$=VIL VOUT=Vss to Vcc		-2	2	μA
Operating Current	ICC	Min. Cycle, 100% Duty $\overline{CS}$=VIL, VIN=VIH or VIL, IOUT=0mA	12ns	-	170	mA
			15ns	-	165	
			20ns	-	160	
Standby Current	ISB	Min. Cycle, $\overline{CS}$=VIH		-	25	mA
	ISB1	f=0MHz, $\overline{CS}$ ≥Vcc-0.2V, VIN≥Vcc-0.2V or VIN≤0.2V		-	8	mA
Output Low Voltage Level	VOL	IOL=8mA		-	0.4	V
Output High Voltage Level	VOH	IOH=-4mA		2.4	-	V
	VOH1*	IOH1=-0.1mA		-	3.95	V

NOTE: The above parameters are also guaranteed at industrial temperature range.
      * Vcc=5.0V, Temp.=25°C

CAPACITANCE*(TA=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/O=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	6	pF

* NOTE : Capacitance is sampled and not 100% tested.

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AC CHARACTERISTICS (T$_A$=0 to 70°C, V$_{CC}$=5.0V±10%, unless otherwise noted.)

TEST CONDITIONS

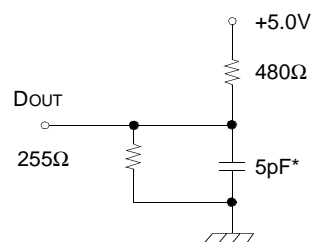| Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE : The above test conditions are also applied at industrial temperature range.

Output Loads(A)

D$_{OUT}$
+5.0V
480Ω
255Ω
30pF*
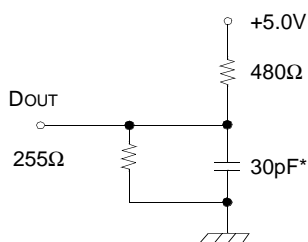
Output Loads(B)
for t$_{HZ}$, t$_{LZ}$, t$_{WHZ}$, t$_{OW}$, t$_{OLZ}$ & t$_{OHZ}$

D$_{OUT}$
+5.0V
480Ω
255Ω
5pF*

* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681002A-12		KM681002A-15		KM681002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t$_{RC}$	12	-	15	-	20	-	ns
Address Access Time	t$_{AA}$	-	12	-	15	-	20	ns
Chip Select to Output	t$_{CO}$	-	12	-	15	-	20	ns
Output Enable to Valid Output	t$_{OE}$	-	6	-	7	-	9	ns
Chip Enable to Low-Z Output	t$_{LZ}$	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t$_{OLZ}$	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t$_{HZ}$	0	6	0	7	0	9	ns
Output Disable to High-Z Output	t$_{OHZ}$	0	6	0	7	0	9	ns
Output Hold from Address Change	t$_{OH}$	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t$_{PU}$	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	t$_{PD}$	-	12	-	15	-	20	ns

NOTE : The above parameters are also guaranteed at industrial temperature range.

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WRITE CYCLE

| Parameter	Symbol	KM681002A-12		KM681002A-15		KM681002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t$_{WC}$	12	-	15	-	20	-	ns
Chip Select to End of Write	t$_{CW}$	8	-	10	-	12	-	ns
Address Set-up Time	t$_{AS}$	0	-	0	-	0	-	ns
Address Valid to End of Write	t$_{AW}$	8	-	10	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	t$_{WP}$	8	-	10	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	t$_{WP1}$	12	-	15	-	20	-	ns
Write Recovery Time	t$_{WR}$	0	-	0	-	0	-	ns
Write to Output High-Z	t$_{WHZ}$	0	6	0	7	0	9	ns
Data to Write Time Overlap	t$_{DW}$	6	-	7	-	9	-	ns
Data Hold from Write Time	t$_{DH}$	0	-	0	-	0	-	ns
End Write to Output Low-Z	t$_{OW}$	3	-	3	-	3	-	ns

NOTE : The above parameters are also guaranteed at industrial temperature range.

TIMMING DIAGRAMS

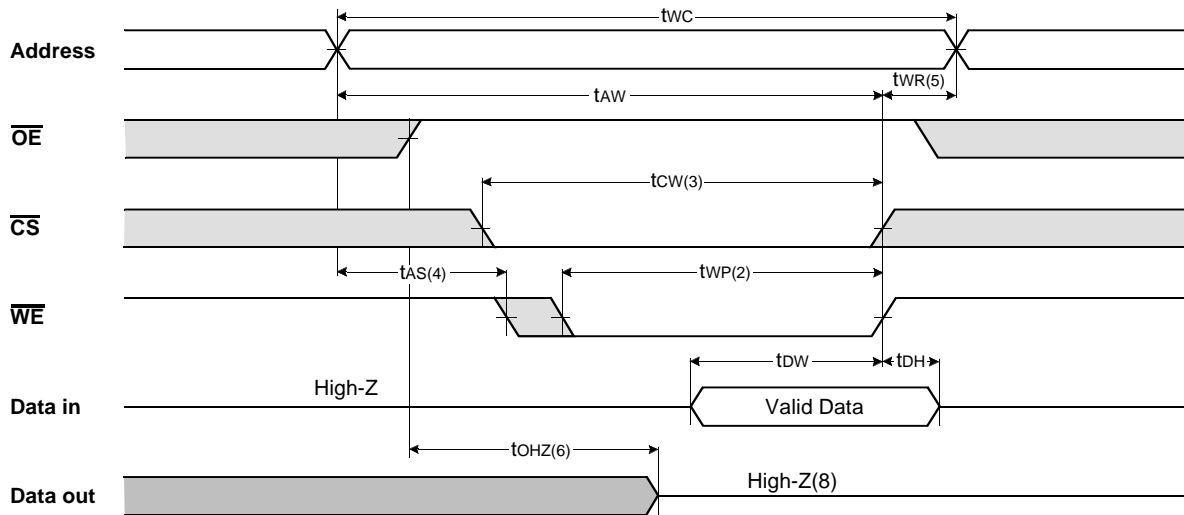### TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V$_{IL}$, $\overline{WE}$=V$_{IH}$)
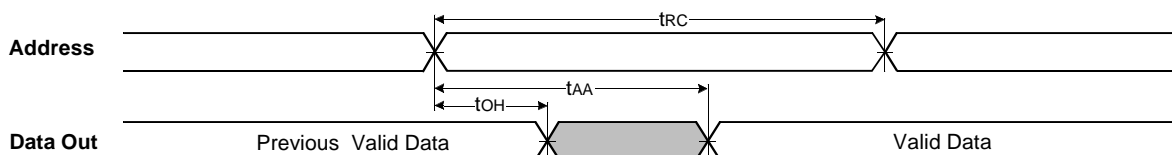
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V$_{IH}$)

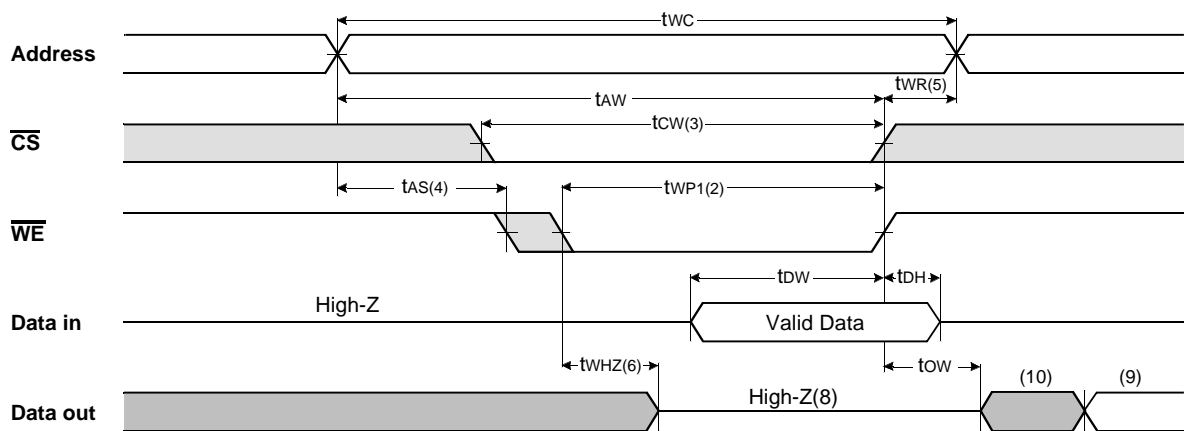**SAMSUNG ELECTRONICS**

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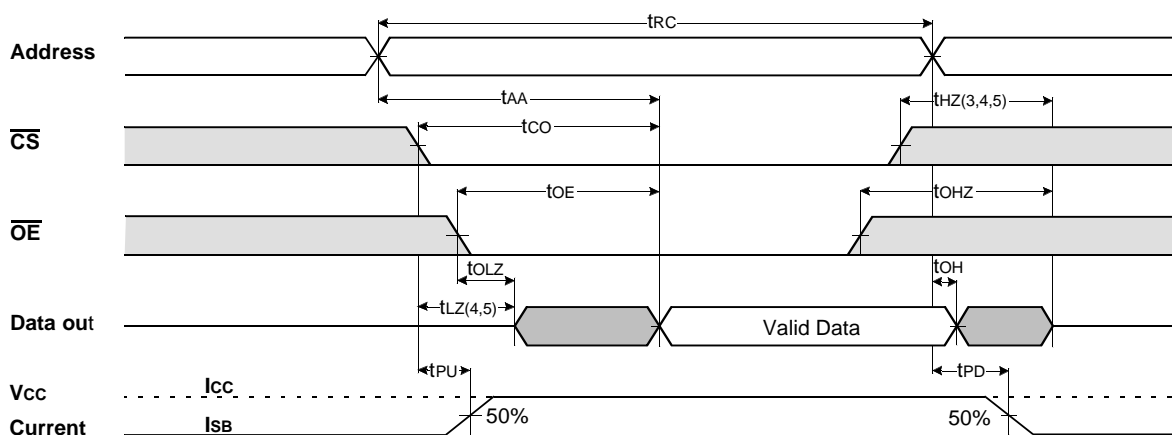
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
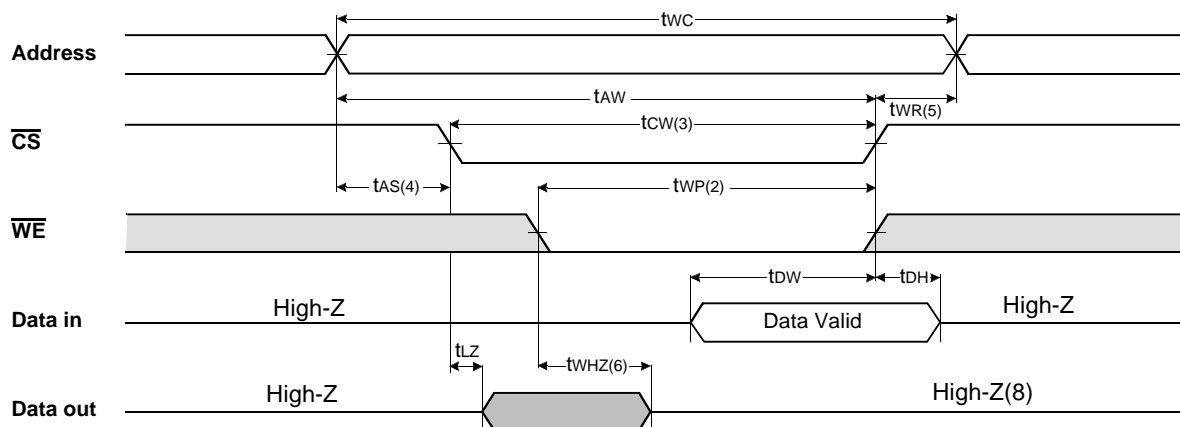
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$= Clock)

Address, $\overline{OE}$, $\overline{CS}$, $\overline{WE}$, Data in, Data out

t_{WC}, t_{AW}, $t_{WR(5)}$, $t_{CW(3)}$, $t_{AS(4)}$, $t_{WP(2)}$, t_{DW}, t_{DH}, $t_{OHZ(6)}$

High-Z, Valid Data, High-Z(8)

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)

Address, $\overline{CS}$, $\overline{WE}$, Data in, Data out

t_{WC}, t_{AW}, $t_{WR(5)}$, $t_{CW(3)}$, $t_{AS(4)}$, $t_{WP1(2)}$, t_{DW}, t_{DH}, $t_{WHZ(6)}$, t_{OW}, (10), (9)

High-Z, Valid Data, High-Z(8)

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TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS}$ = Controlled)

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low. A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.
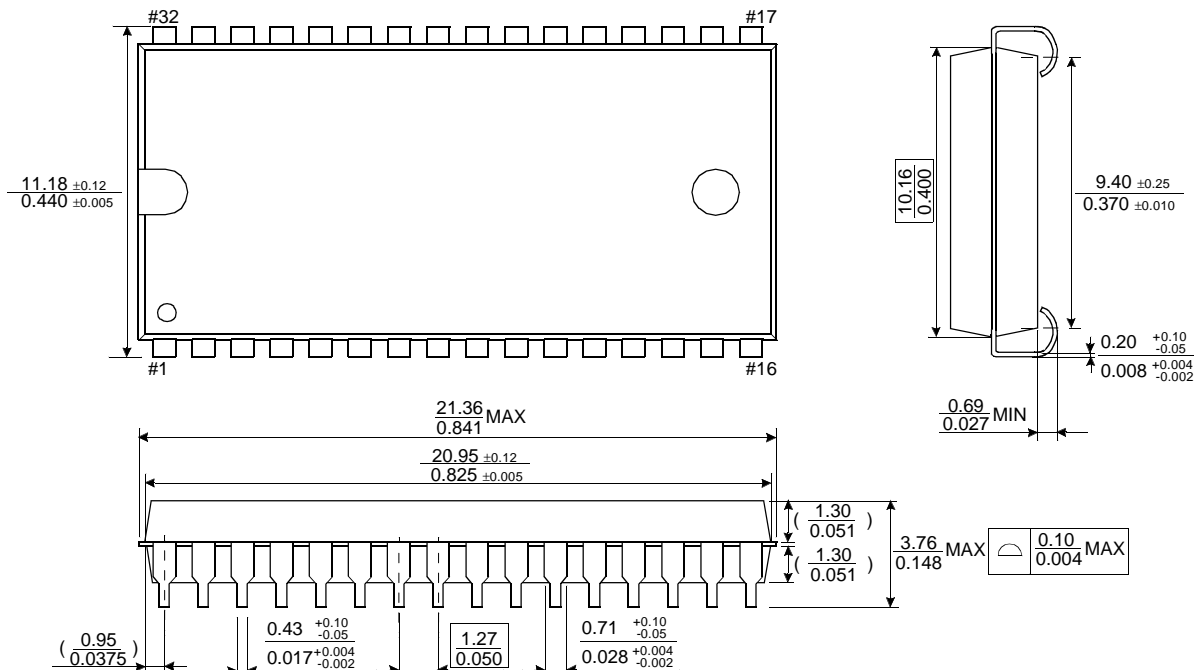
FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* NOTE : X means Don't Care.

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PACKAGE DIMENSIONS

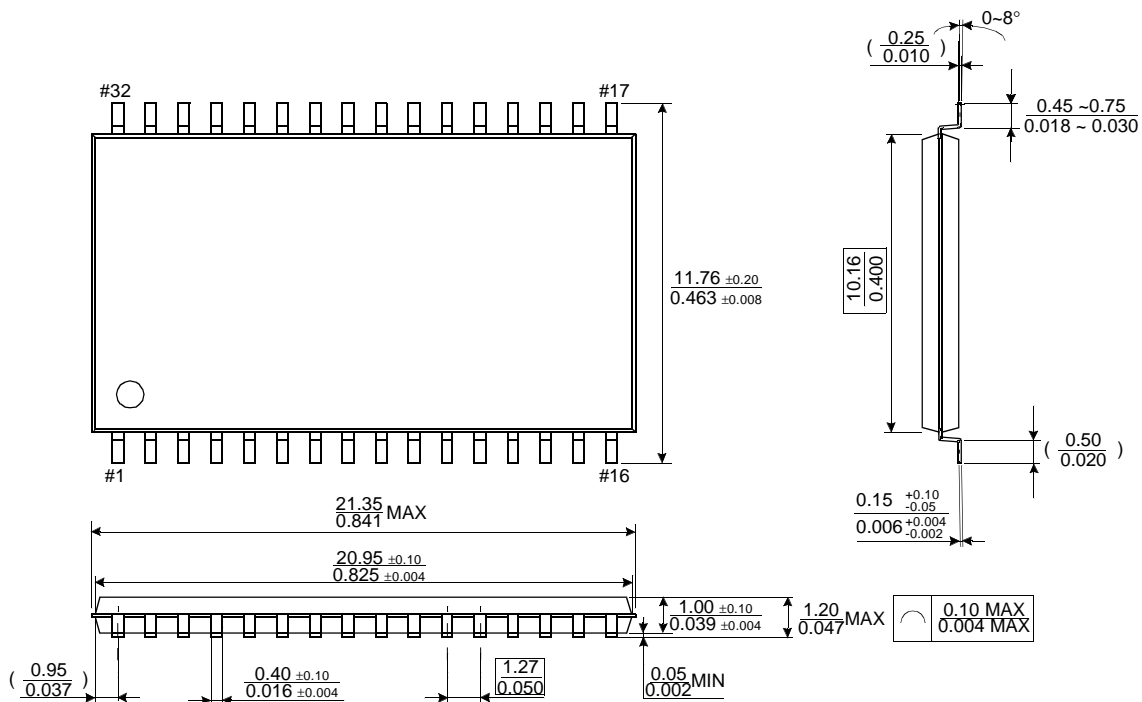**32-SOJ-400**   Units:millimeters/Inches

32-TSOP2-400F   Units:millimeters/Inches

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PACKAGE DIMENSIONS

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