*Product Preview*

# Low Voltage PLL Clock Driver

**MPC2510**

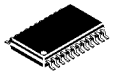
**LOW VOLTAGE**
**PLL ZERO DELAY BUFFER**

The MPC2510 is a 3.3V compatible, PLL based zero delay buffer targeted for high performance clock tree designs. With 11 outputs at frequencies of up to 125MHz and output skews of 200ps the MPC2510 is ideal for the most demanding clock tree designs. The device employs a fully differential PLL design to minimize cycle–to–cycle and phase jitter. The device is compliant to the 1.2 revision of the PC100 design document.

- Fully Integrated PLL
- Output Frequency up to 125MHz in PLL Mode
- Outputs Disable to a Logic Low
- TQFP Packaging
- 50ps Cycle–to–Cycle Jitter
- On Board Series Damping Resistors

The analog $V_{CC}$ pin of the device also serves as a PLL bypass select pin. When driven low the $AV_{CC}$ pin will route the REF_CLK input around the PLL directly to the outputs. The OE input is a logic enable for all of the outputs except QFB. A low on the OE pin forces Q0–Q9 to a logic low state.

The MPC2510 is fully 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the ability to drive terminated 50Ω transmission lines. The output impedance of the MPC2510 is ≈ 40Ω with IV curves that are PC100 Rev 1.2 compliant. The device is packaged in a 24–lead TSSOP package to provide the optimum combination of board density and performance.



**DT SUFFIX**
24–LEAD TSSOP PACKAGE
CASE 948H–01

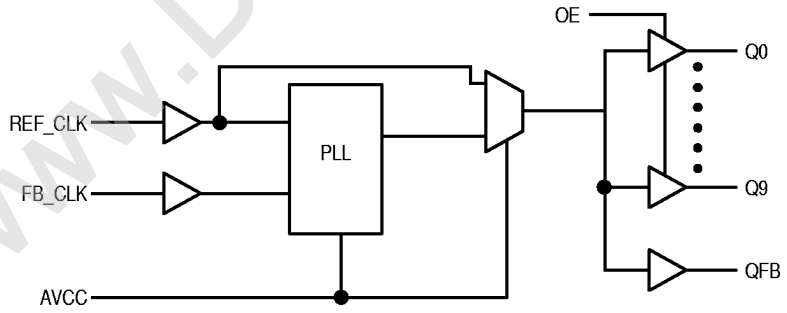



**Figure 1. Block Diagram**

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.







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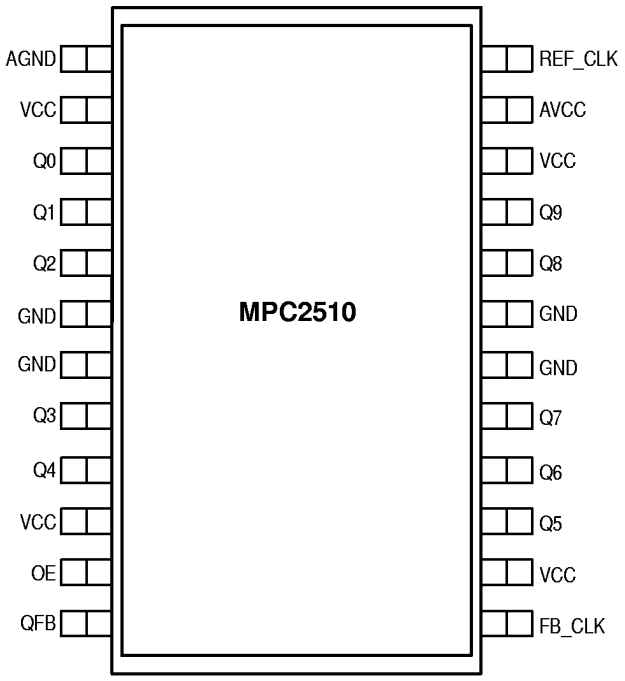



**Figure 2. 24–Lead Pinout** (Top View)

**FUNCTION TABLES**

| $AV_{CC}$ | Function |
|---|---|
| 1 | PLL Enabled |
| 0 | PLL Bypass |

| OE | Function |
|---|---|
| 1 | Q0 – Q9 Enabled |
| 0 | Q0 – Q9 Low |

**ABSOLUTE MAXIMUM RATINGS***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

**DC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage LVCMOS Inputs | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage LVCMOS Inputs | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –6mA, Note 1. |
| $V_{OL}$ | Output LOW Voltage | | | 0.55 | V | $I_{OL}$ = 6mA, Note 1. |
| $I_{IN}$ | Input Current | | | ±120 | µA | |
| $C_{IN}$ | Input Capacitance | | | 4 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | | | pF | Per Output |
| $I_{CC}$ | Maximum Quiescent Supply Current | | 40 | | mA | All VCC Pins |
| $I_{CCPLL}$ | Maximum PLL Supply Current | | 15 | | mA | VCCA Pin Only |

1. The MPC953 outputs can drive series terminated 50Ω transmission lines on the incident edge.

**PLL INPUT REFERENCE CHARACTERISTICS** ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $f_{ref}$ | Reference Input Frequency | 66.66 | 125 | MHz | |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

**AC CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.10 | | 1.0 | ns | 0.8 to 2.0V |
| $t_{pw}$ | Output Duty Cycle | 45 | 50 | 55 | % | |
| $t_{sk(O)}$ | Output–to–Output Skews | | | 200 | ps | |
| $f_{max}$ | Maximum Output Frequency PLL Mode | 66.66 | | 125 | MHz | |
| $t_{pd(lock)}$ | Input to Ext_FB Delay (with PLL Locked) (Including Jitter) | X–150 | X | X+150 | ps | $f_{ref}$ = 100MHz |
| $t_{PLZ,HZ}$ | Output Disable Time | | 7 | | ns | |
| $t_{PZL}$ | Output Enable Time | | 7 | | ns | |
| $t_{jitter}$ | Cycle–to–Cycle Jitter (Peak–to–Peak) | | 50 | | ps | |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

**Power Supply Filtering**

The MPC2510 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC2510 provides separate power supplies for the output buffers (VCCO) and the phase–locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC2510.

Figure 3 illustrates a typical power supply filter scheme. The MPC2510 is most susceptible to noise with spectral content in the 1KHz to 10MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the VCCA pin of the MPC2510. From the data sheet the $I_{VCCA}$ current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 3 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10Ω resistor to avoid potential $V_{CC}$ drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

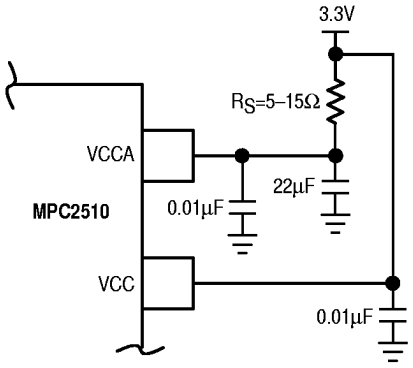
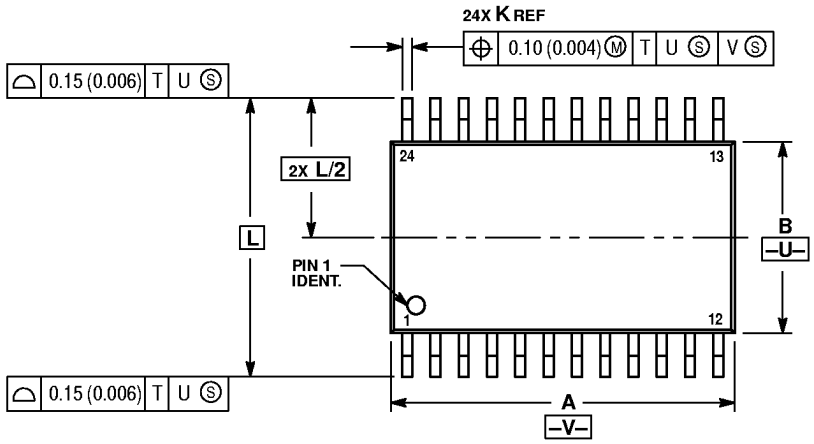


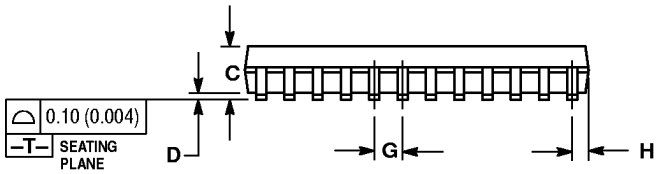

**Figure 3. Power Supply Filter**

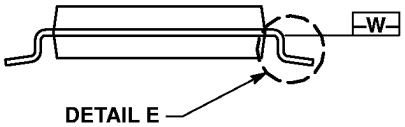
Although the MPC2510 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

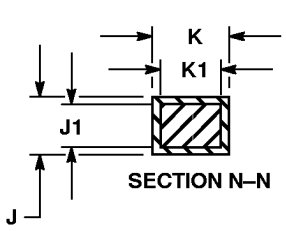
## OUTLINE DIMENSIONS

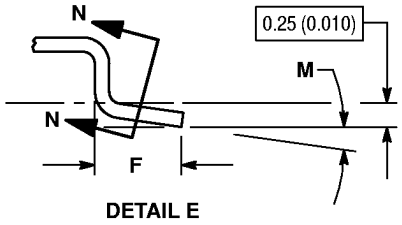
**DT SUFFIX**
TSSOP PACKAGE
CASE 948H–01
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 7.70 | 7.90 | 0.303 | 0.311 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | — | 1.20 | — | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |