National Semiconductor

February 1991

DP83241 CDD™ Device (FDDI Clock Distribution Device)

General Description

The CDD device is a clock generation and distribution device intended for use in FDDI (Fiber Distributed Data Interface) networks. The device provides the complete set of clocks required to convert byte wide data to serial format for fiber medium transmission and to move byte wide data between the PLAYER™ and BMAC™ devices in various station configurations. 12.5 MHz and 125 MHz differential ECL clocks are generated for the conversion of data to serial format and 12.5 MHz and 25 MHz TTL clocks are generated for the byte wide data transfers.

Features

- Provides 12.5 MHz and 25 MHz TTL clocks
- 12.5 MHz and 125 MHz ECL clocks
- 5 phase TTL local byte clocks eliminate clock skew problems in concentrators
- Internal VCO requires no varactors, coils or adjustments
- Option for use of High Q external VCO
- 125 MHz clock generated from a 12.5 MHz crystal
- External PLL synchronizing reference for concentrator configurations
- 28-pin PLCC package
- BiCMOS processing

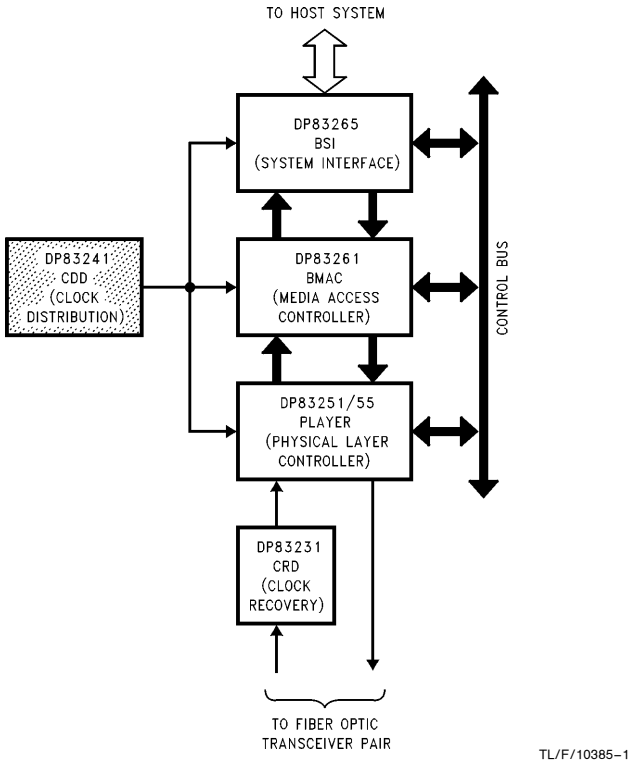

FIGURE 1-1. FDDI Chip Set Block Diagram

RRD-B30M105/Printed in U. S. A.

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1.0 FDDI Chip Set Overview

National Semiconductor's FDDI chip set consists of five components as shown in *Figure 1-1.* For more information about the other devices in the chip set, consult the appropriate data sheets and application notes.

DP83231 CRD™ Device Clock Recovery Device

The Clock Recovery Device extracts a 125 MHz clock from the incoming bit stream.

Features

- PHY Layer loopback test
- Crystal controlled
- Clock locks in less than 85 μs

DP83241 CDD™ Device Clock Distribution Device

From a 12.5 MHz reference, the Clock Distribution Device synthesizes the 125 MHz, 25 MHz and 12.5 MHz clocks required by the BSI, BMAC, and PLAYER devices.

DP83251/55 PLAYER™ Device Physical Layer Controller

The PLAYER device implements the Physical Layer (PHY) protocol as defined by the ANSI FDDI PHY X3T9.5 Standard.

Features

- 4B/5B encoders and decoders
- Framing logic
- Elasticity Buffer, Repeat Filter, and Smoother
- Line state detector/generator
- Link error detector
- Configuration switch
- Full duplex operation
- Separate management port that is used to configure and control operation.

In addition, the DP83255 contains an additional PHY__Data.request and PHY__Data.indicate port required for concentration and dual attach stations.

DP83261 BMAC™ Device Media Access Controller

The BMAC device implements the Timed Token Media Access Control protocol defined by the ANSI FDDI X3T9.5 MAC Standard.

Features

- All of the standard defined ring service options
- Full duplex operation with through parity
- Supports all FDDI Ring Scheduling Classes (Synchronous, Asynchronous, etc.)
- Supports Individual, Group, Short, Long, and External Addressing
- Generates Beacon, Claim, and Void frames internally
- Extensive ring and station statistics gathering
- Extensions for MAC level bridging
- Separate management port that is used to configure and control operation
- Multi-frame streaming interface

DP83265 BSI™ Device System Interface

The BSI Device implements an interface between the National FDDI BMAC device and a host system.

Features

- 32-bit wide Address/Data path with byte parity
- Programmable transfer burst sizes of 4 or 8 32-bit words
- Interfaces to low-cost DRAMs or directly to system bus
- Provides 2 Output and 3 Input Channels
- Supports Header/Info splitting
- Efficient data structures
- Programmable Big or Little Endian alignment
- Full Duplex data path allows transmission to self
- Comfirmation status batching services
- Receive frame filtering services
- Operates from 12.5 MHz to 25 MHz synchronously with host system

2.0 Functional Description

The CDD device clocks are all generated from and phase aligned to either a 12.5 MHz crystal oscillator or a TTL input reference source using digital phase locked loop techniques. The architecture of the Clock Distribution Device ensures that the output clocks which are generated have frequency tolerances identical to the 50 PPM crystal reference. When the reference input signal is a backplane signal, the matching of the phase comparator input path delays guarantees phase alignment within 3 ns.

The phase locked loop generates the desired clocks as shown in the device Block Diagram. One of the Local Byte Clock (LBC) phases is connected to the FEEDBK IN input of the phase comparator where its phase and frequency are compared against that of the selected input reference signal. Any phase error between these signals results in a correction of the voltage into the Voltage Controlled Oscillator (VCO) which is proportional to the amount of phase error. The correction voltage tends to drive the frequency of the VCO in the direction which, when divided down, minimizes the LBC to reference signal phase difference. When the phase transition of the LBC occurs before that of the reference input the VCO frequency is sensed as being too fast and produces a negative going correction to the VCO input. This in turn slows down the VCO's frequency and delays the subsequent LBC phase transitions.

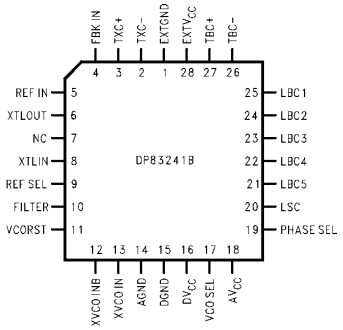
The device's differential 125 MHz ECL transmit clock and differential 12.5 MHz ECL load strobe are used by the PLAYER device to convert data from byte wide NRZ format to serial NRZI format for fiber medium transmission. A 12.5 MHz TTL local byte clock is provided for use by the PLAYER and the BMAC devices. Five phases of the local byte clock are provided for use in large multi-board concentrator configurations to aid in cancelling out backplane delays. A 25 MHz Local Symbol Clock (LSC) is provided which is in phase with the local byte clocks and has a 40% HIGH and 60% LOW duty cycle.

The device provides three user-selectable features. The REF SEL input provides the option to lock the device's outputs to a crystal oscillator or to an external TTL signal (REF IN). The REF IN signal is particularly useful in concentrators where multiple boards need to be phase locked to a common reference signal. The VCO SEL input provides the option to use the internally provided VCO or an external LC voltage controlled oscillator. Although the stability of the internal VCO should be adequate for most applications the external VCO option provides the means of obtaining the maximum possible oscillator Q. The PHASE SEL input pin provides the option of selecting whether the five phase LBC outputs are phase offset 36 degrees or 72 degrees (8 ns or 16 ns).

The phase locked loop (PLL) elements, with the exception of the loop filter which consist of two capacitors and a resistor, are fully contained within the device. The internal VCO associated with the PLL has been implemented totally within the device and requires no external LC oscillator tank coils, capacitors, or varactors. The external VCO option does provide a means of using these conventional LC oscillator techniques if desired.

Connection Diagram

28-Pin PLCC Package



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Order Number DP83241BV
See NS Package Number V28A

FIGURE 2-1. DP83241 Pinout

Block Diagram

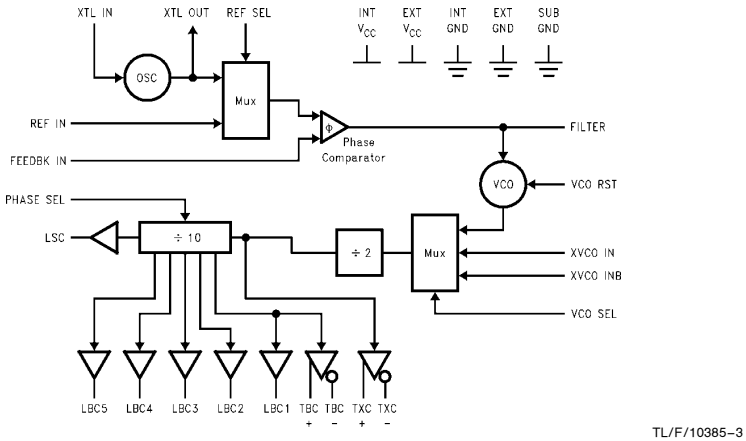

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FIGURE 2-2. DP83241 Block Diagram

3.0 Pin Descriptions

Symbol	Pin No.	I/O	Description
DV_{CC}	16		**Digital V_{CC}:** Positive power supply for all the internal circuitry intended for operation at 5V ±5% relative to GND. A bypass capacitor should be placed as close as possible across the DV_{CC} and DGND pins.
$EXTV_{CC}$	28		**External V_{CC}:** Positive power supply for all the output buffers intended for operation at 5V ±5% relative to GND. A bypass capacitor should be placed as close as possible across the $EXTV_{CC}$ and EXTGND pins.
DGND	15		**Digital Ground:** Internal circuit power supply return.
EXTGND	1		**External Ground:** Output buffer power supply return.
AGND	14		**Analog Ground:** Substrate ground used to ensure proper device biasing and isolation.
AV_{CC}	18		**Analog V_{CC}:** Positive power supply for the critical analog circuitry, intended for +5V operation ±5% relative to Ground. A bypass cap should be placed as close as possible between AV_{CC} and AGND.
XTL IN	8	I	**External Crystal Oscillator Input:** XTL IN can also be used as a CMOS compatible reference frequency input for the PLL. This input is selected when REF SEL is at a logical LOW level. The component connections required for oscillator operation are shown in the application diagrams.
XTL OUT	6		**External Crystal Oscillator Output:** XTL OUT is not intended for use as a logic drive output pin.
REF IN	5	I	**Reference Input:** TTL compatible input for use as the PLL's phase comparator reference frequency input when the REF SEL is at a logic HI level. This input is for use in concentrator configurations where there are multiple CDD devices at a given site requiring synchronization.
FEEDBK IN	4	I	**Feedback Input:** TTL compatible input for use as the PLL's phase comparator feedback input to close the loop. This input is intended to be driven from one of the LBCs (Local Byte Clocks). This input is designed to provide the same frequency and within 2 ns of the same phase as REF IN when REF IN is in active operation.
REF SEL	9	I	**Reference Select:** TTL compatible input which selects either the crystal oscillator inputs XTL IN and XTL OUT or the REF IN inputs as the reference frequency inputs for the PLL. The crystal oscillator inputs are selected when REF SEL is at a logic LOW level and the REF IN input is selected as the reference frequency when REF SEL is at a logic HI level.
FILTER	10	O	**Filter:** Low pass PLL loop filter pin. A three element filter, consisting of one capacitor in parallel with a resistor and another capacitor, should be connected between this pin and ground.
VCO SEL	17	I	**VCO Select:** TTL compatible input used to select either the internal VCO or an external VCO through the XVCO IN and XVCO INB pins. The internal VCO is selected when the VCO SEL pin is at a logic HIGH level and the external VCO is selected when at a logic LOW level.
XVCO IN, XVCO INB	13, 12	I	**External VCO Inputs:** Differential inputs for use with an external VCO. These inputs are D.C. biased to approximately one half V_{CC}, and can be connected to either a full differential VCO, or a single-ended VCO. To use a single-ended VCO, couple the signal into one of the inputs through a series low value capacitor and bypass the other input to GND through a 0.01 μF capacitor. When not in use, ground one input, and let the other float.

3.0 Pin Descriptions (Continued)

Symbol	Pin No.	I/O	Description
VCO RST	11	I	**VCO Reset:** TTL compatible input used to reset the internal VCO on system power up. This input stops the VCO from oscillating when at a logic HI level thereby reinitializing each of the gates in the ring oscillator.
TXC+, TXC−	3, 2	O	**Transmit Clock:** 100K ECL compatible differential outputs for use at 125 MHz as the fiber medium Transmit Clock (TXC) source for the PLAYER device.
TBC+, TBC−	27, 26	O	**Transmit Byte Clock:** 100K ECL compatible differential outputs for use at 12.5 MHz as a load strobe or transmit byte clock by the PLAYER device to convert byte wide data to serial format for fiber medium transmission. These outputs are positioned to transition on the falling edge of the TXC + clock output to provide the maximum setup and hold margin. They are also phase coherent with the TTL LBC1 output, but the phase transition occurs approximately 10 ns earlier.
LBC1 thru 5	25, 24, 23, 22, 21	O	**Local Byte Clocks:** TTL compatible local byte clock outputs which are phase locked to crystal oscillator reference signals. These outputs have a 50% duty cycle waveform at 12.5 MHz. The PHASE SEL input determines whether the five phase outputs are phase offset by 8 ns or 16 ns.
LSC	20	O	**Local Symbol Clock:** TTL compatible 25 MHz output for driving the BMAC device. This output's negative phase transition is aligned with the LBC1 output transitions and has a 40% HI and 60% LOW duty cycle.
PHASE SEL	19	I	**Phase Select:** TTL compatible input used to select either a 8 ns or 16 ns phase offset between the 5 local byte clocks. The LBC's are phase offset 8 ns apart when PHASE SEL is at a logic LOW level and 16 ns apart when at a logic HI level.

4.0 Electrical Characteristics

4.1 ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
TTL Signals	
Inputs	−0.5V to +5.5V
Outputs	−0.5V to +5.5V
ECL Signals	
Output Current	−50 mA
Supplies	
$EXTV_{CC}$ to EXTGND	−0.5V to +7V
DV_{CC} to DGND	−0.5V to +7V
AV_{CC} to AGND	−0.5V to +7V
ESD Protection	1500V

4.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Units
V_{CC} to GND	Power Supply		4.75	5.0	5.25	V
V_{IH}	High Level Input Voltage	TTL	2.0			V
		ECL	V_{CC} − 1.165		V_{CC} − 0.880	
V_{IL}	Low Level Input Voltage	TTL			0.8	V
		ECL	V_{CC} − 1.810		V_{CC} − 1.475	
I_{OH}	High Level Output Current	TTL Outputs (Note 1)			−0.4	mA
I_{OL}	Low Level Output Current	TTL Outputs (Note 1)			8.0	mA
F_{VCO}	VCO Frequency (INT or EXT)			250		MHz
F_{REF}	Reference Input Frequency			12.5		MHz
T_A	Operating Temperature		0	25	70	°C

Note 1: TTL outputs include LBC1, LBC2, LBC3, LBC4, LBC5 and LSC.

4.3 DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Units
V_{IC}	Input Clamp Voltage	I_{IN} = 18 mA		−1.5	V
V_{OH}	High Level Output Voltage	TTL Outputs: I_{OH} = −400 μA	V_{CC} − 2		V
		ECL Outputs: 50Ω Load to V_{CC} − 2V	V_{CC} − 1025	V_{CC} − 880	mV
V_{OL}	Low Level Output Voltage	TTL Outputs: I_{OL} = 8 mA		0.5	V
		ECL Outputs: 50Ω Load to V_{CC} − 2V	V_{CC} − 1810	V_{CC} − 1620	mV
I_I	Max High Level Input Current	TTL Inputs: V_{IN} = 7V		100	μA
I_{IH}	High Level Input Current	TTL Inputs: V_{IN} = 2.7V	−20	20	μA
I_{IL}	Low Level Input Current	TTL Inputs: V_{IN} = 0.4V	−20	20	μA
I_{Filter}	Charge Pump Current	Source	−0.7	+0.7	mA
		Sink	0.2	0.7	mA
		TRI-STATE®	−250	250	nA
I_{CC}	Supply Current			170*	mA

*Includes 60 mA due to external ECL termination of two differential signals.

For 100k ECL output buffers, output levels are specified as:

V_{OH}_Max = V_{CC} − 0.88V

V_{OL}_Max = V_{CC} − 1.62V

Since the outputs are differential, the average output level is V_{CC} − 1.25V. The test load per output is 50Ω at V_{CC} − 2V. The external load current through this 50Ω resistor is thus:

I_Load = [(V_{CC} − 1.25) − (V_{CC} − 2)]/50 Amps
= 0.015 Amps
= 15 mA

There are 2 pairs of differential ECL signals, so the total ECL current is 60 mA.

4.0 Electrical Characteristics (Continued)

4.4 AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Units
T1	TBC to TXC	(Note 1)	−1.5	1.5	ns
T2	TBC to LBC1		10	20	ns
T_{Phase1}	LBC1 to LBC2	PHASE SEL = Low	3	13	ns
		PHASE SEL = High	43	53	ns
T_{Phase2}	LBC1 to LBC3	PHASE SEL = Low	11	21	ns
		PHASE SEL = High	11	21	ns
T_{Phase3}	LBC1 to LBC4	PHASE SEL = Low	19	29	ns
		PHASE SEL = High	59	69	ns
T_{Phase4}	LBC1 to LBC5	PHASE SEL = Low	27	37	ns
		PHASE SEL = High	27	37	ns
T3	LSC to LBC1		−4	6	ns
T4	LSC Positive Pulse Width		12	19	ns
T5	REF IN to FEEDBK IN	In Lock (Note 1)	−3	3	ns
T6	TXC Positive Pulse Width	(Note 1)	3.5	4.5	ns
T7	LBC Positive Pulse Width		35	45	ns

Note 1: These parameters are not tested, but are assured by correlation with characterization data.

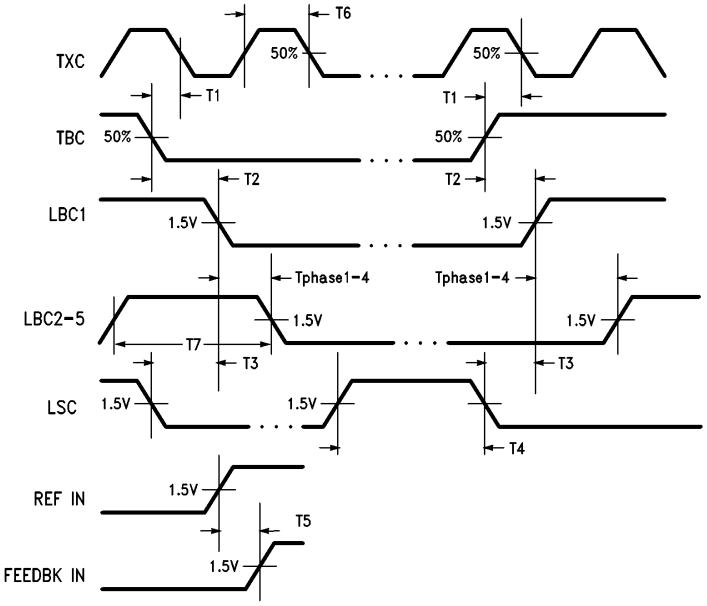

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FIGURE 4-1. AC Timing Waveforms

4.0 Electrical Characteristics (Continued)

4.4 AC ELECTRICAL CHARACTERISTICS (Continued)

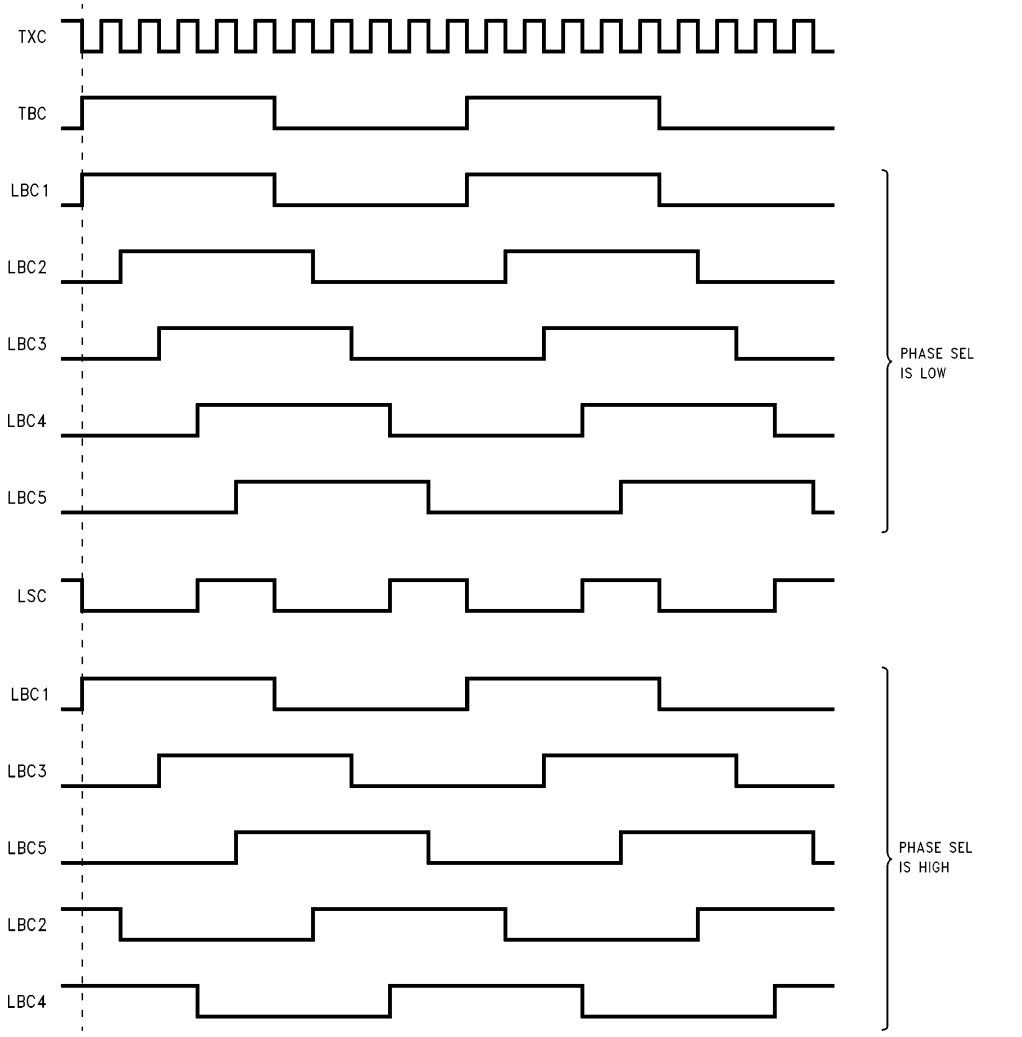


FIGURE 4-2. Typical Clock Relationships

Loop Filter Calculations

Several constants need to be known in order to determine the loop filter components. They are the loop divide ratio, N, the phase detector gain, K_p, the VCO gain, K_o, the loop bandwidth, W_o, and the phase margin, ϕ. The constants K_p and K_o for the DP83241 are fixed at 80 μA/rad and 0.8 Grad/V respectively. N is equal to the VCO frequency divided by the reference frequency. w_o is recommended to be less than 1/20th of the reference frequency (times 2π rads). Having found all these constants, the following equations are used to find the component values:

For $\phi = 57°$ phase margin:

$R_1 = (1.1\ N\ w_o)/(K_p\ K_o)$

$C_1 = (3\ K_p\ K_o)/(N\ w_o^2)$

$C_2 = (0.3\ K_p\ K_o(/(N\ w_o^2)$

For a phase margin other than 57°:

$R_1 = (\text{Cosec}\ \phi + 1)\ ((N\ w_o/2\ K_p\ K_o))$

$C_1 = (\text{Tan}\ \phi)\ ((2\ K_p\ K_o)/(N\ w_o^2))$

$C_2 = (\text{Sec}\ \phi - \text{Tan}\ \phi)\ ((K_p\ K_o/(N\ w_o^2))$

The component equations above are not meant to provide optimal solutions for all implementations.

Let us now design an example system with the following characteristics:

- 12.5 MHz Crystal reference.
- 250 MHz VCO.

Since the VCO is twenty times the frequency of the reference frequency, we get N = 20. We will set w_o to be 1/30th of the reference frequency or 2.62 x 10^6 Rad.

From these values we get:

$C_1 = 1400$ pF, $C_2 = 140$ pF, and $R_1 = 900\Omega$

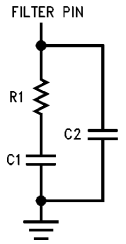
Let us now design an example system with the following characteristics:

- 12.5 MHz Crystal reference.
- 250 MHz External VCO with a gain of 40 MRad/V.

We will set w_o to be 1/78th of the reference frequency or 1.0 x 10^6 Rad.

From these values we get:

$C_1 = 470$ pF, $C_2 = 47$ pF, and $R_1 = 6.8\ k\Omega$.



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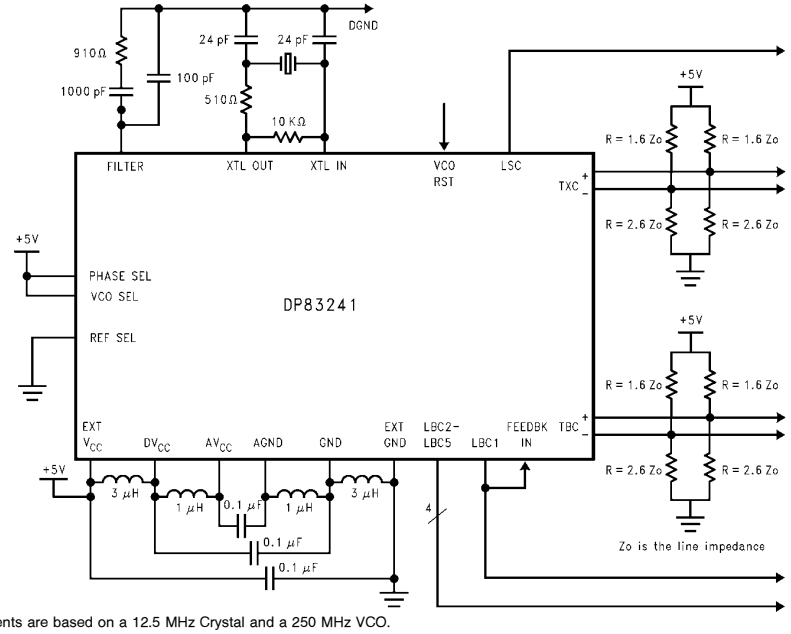
5.0 Detailed Information

5.1 EXTERNAL COMPONENTS



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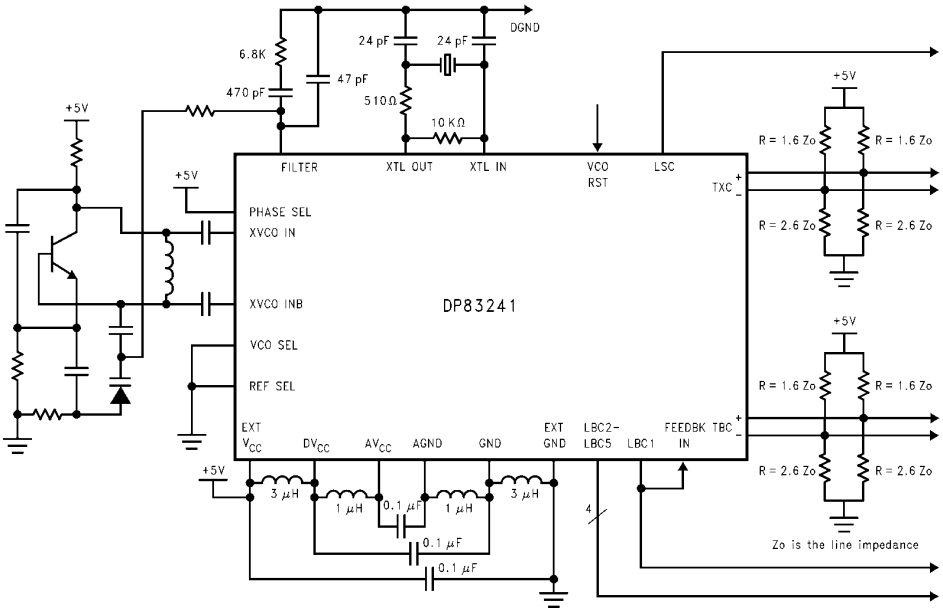
The Filter components are based on a 12.5 MHz Crystal and a 250 MHz VCO.
All component values ±10%.

FIGURE 5-1. General Wiring Diagram



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The Filter components are based on a 12.5 MHz Crystal and an external 250 MHz VCO with a gain of 40 MRad/V.
All component values ±10%.

FIGURE 5-2. General Wiring Diagram with an External VCO

5.0 Detailed Information (Continued)

TABLE 5-1. Special External Components

Crystal Resonator:	Part #: Manufacturer: Key Specifications:	C5410N NEL 12.5000 MHz Center Frequency, 20 PPM Accuracy, 0°C to +70°C 15 pF Load Capacitance
Varactor Diode:	Part#: Manufacturer: Key Specifications:	MV2105 Motorola Cap Tolerance ±10%
VHF NPN Transistor:	Part#: Manufacturer: Key Specifications:	PN3563 National Semiconductor
Inductor:	Part#: Manufacturer: Key Specifications:	 1½ Turns

5.2 CONCENTRATOR AND DUAL ATTACH STATION CONFIGURATIONS

5.2.1 Concentrator Applications

An application where many of the features of the CDD device are used is a FDDI concentrator. A concentrator is used to connect several workstations and peripherals to a single node in the network. A concentrator provides the ability to easily bypass or insert multiple stations into the network. The CDD device in each station is driven from a common oscillator instead of each CDD device being driven by its own crystal. In a small concentrator, the same LBC phase can be used in each station since the data flight time from one board to another is small compared to the LBC period and the skew between the CDD devices on the two boards is minimal. In a larger concentrator configuration where this skew becomes too large, the data setup time of the downstream station will be directly impacted. One way to avoid this problem is to latch data into the next station. The strobe for the latch will be supplied by one of the LBC outputs from the upstream station's CDD device. An LBC output phase is chosen that occurs after the physical layer data is stable. Assuming that the data and LBC flight times are equal, the LBC output will latch data for the next station. The LBC output phase should be selected to give the optimum setup and hold time for the receiving station's physical layer function.

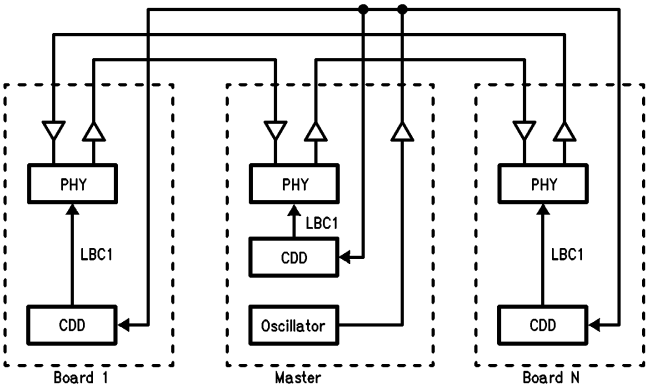

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FIGURE 5-3. Small Concentrator Application

5.0 Detailed Information (Continued)

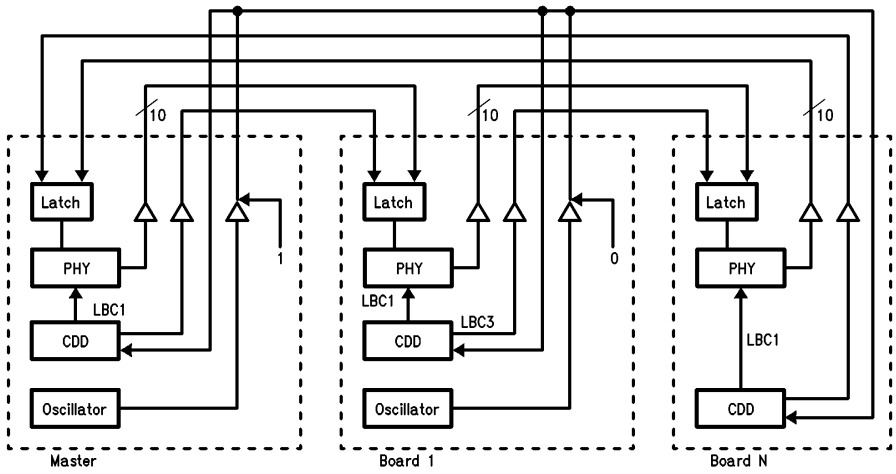

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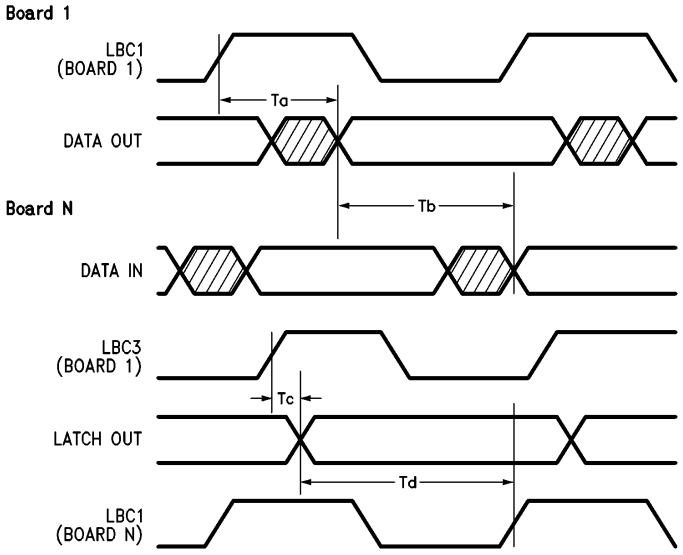
FIGURE 5-4. Large Concentrator Application



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T_a = Time to latch data out of the Physical Layer (Board 1)
T_b = Data flight time
T_c = Latch delay
T_d = Ideal setup time for incoming data
= $T_{d1} + T_{d2} + T_{d3}$
T_{d1} = Reference error between CDD devices
T_{d2} = Minimum phase resolution of CDD device = 8 ns
T_{d3} = Setup time

FIGURE 5-5. Large Concentrator Timing

5.0 Detailed Information (Continued)

5.2.2 CDD Device Driving Multiple PLAYER Devices

In a FDDI concentrator or dual attach station, it may be necessary for a single DP83241 Clock Distribution Device (CDD device) to drive multiple DP83251/55 PLAYER devices. Since these PLAYER devices will be running synchronously to each other they must have the same clocks. The easiest way to accomplish this is to have one CDD device drive multiple PLAYER devices.

We are only concerned with the ECL outputs being able to drive multiple loads. The conventional way of directly wiring the one output to many inputs will not work. If the ECL signals are split into multiple traces then reflections will result which may ruin the signal's integrity. An appropriate method, where individual traces with a series resistor connected to each load, is used instead. The series resistor should match the line impedance and be placed as close to the CDD device as possible. The resistor will act as a voltage divider and cut the voltage level of the signal in half. When this modified signal reaches the input of the unterminated gate, reflections will cause the signal to double and the receiving input will see the full voltage swing. The reflection will then travel back towards the CDD device, but the series resistance will stop this action. An emitter pulldown resistor is needed at the CDD device for this method of routing the ECL signals. The value of this resistor can be calculated from the following equation:

$$R_e\ (\text{Max}) = \frac{10\ Z_o - R_S}{n}$$

Where:

R_e (Max) — Largest emitter pulldown resistor that can be used

n — Number of parallel lines being driven

Z_o — Trace impedance

R_S — Series damping resistor

Another method for sending the ECL signal to multiple players is to route the ECL signal as a bus line and have each load connected to the bus. The ECL bus line must be terminated only at the very end with a matching impedance (e.g.: a 50Ω line will be terminated with a 50Ω load to $V_{CC} - 2V$). It is preferred that the input pin be directly connected to the bus and not have a signal tap connected to the bus. However, if a tap off the bus is necessary, the shortest possible tap is recommended.

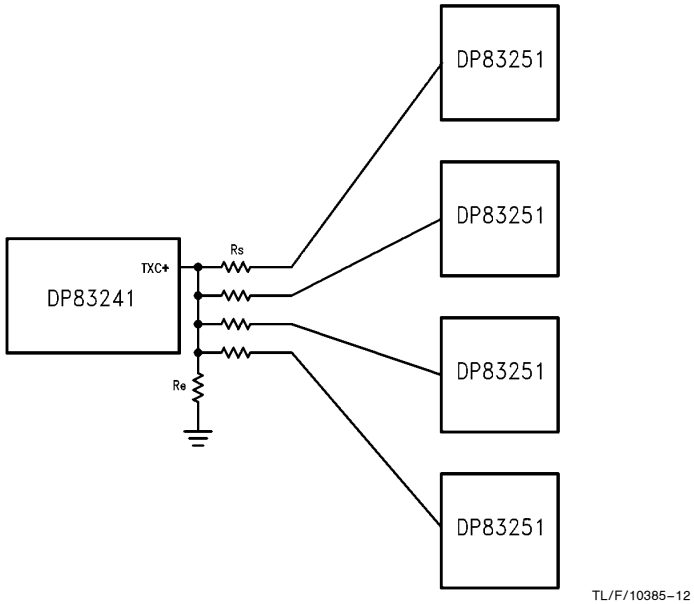

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FIGURE 5-7. CDD Device Driving Four PLAYER Devices in Parallel

5.0 Detailed Information (Continued)

The most conservative method for routing the ECL signals to multiple loads is to use the F100115 Quad Low Skew Driver. This device takes a differential ECL signal and outputs four of the same differential signals with a skew between them of less than 75 ps. Two of these devices will allow the CDD device to drive four PLAYER devices. This setup allows the ECL signals to be routed in a point to point configuration to each PLAYER device.

As with any high speed signal, the routing of the signal must be carefully done. Sharp corners and other changes in trace impedance should be avoided to reduce reflections in high speed signal traces. Traces longer then one inch should have a series or parallel termination scheme. Further system considerations can be found in National's F100K Design Guide. If these methods are followed the DP83241 signals will be able to drive multiple DP83251/55 PLAYER devices without any problems.

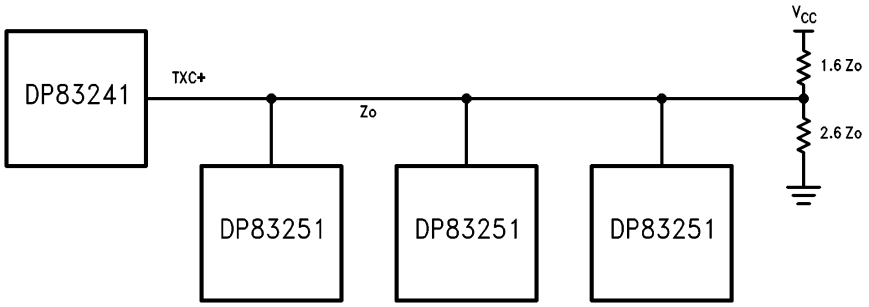

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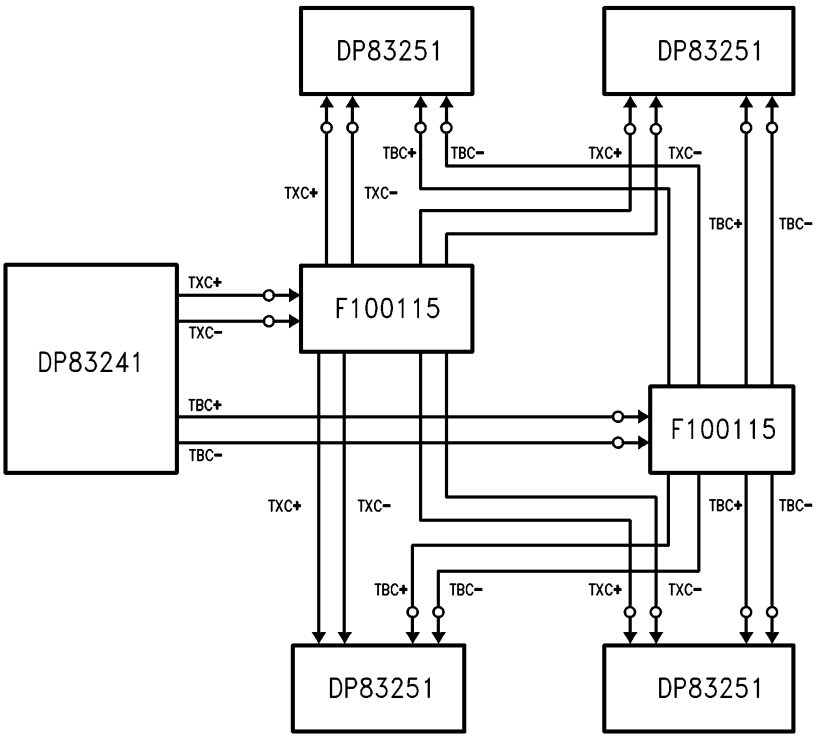
FIGURE 5-8. Proper Bus Line Termination and Connections



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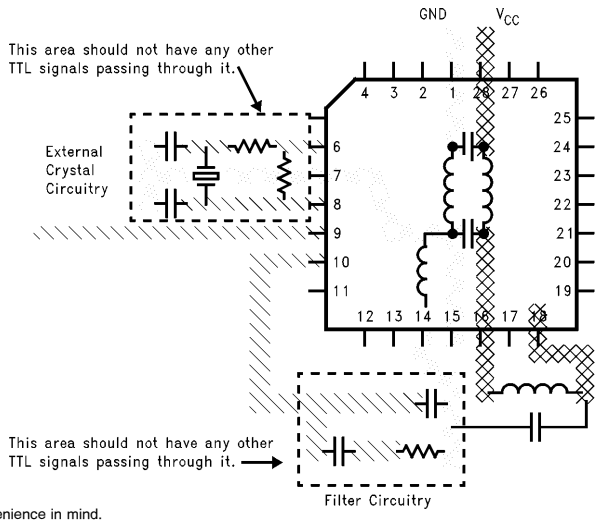
° Parallel Termination

FIGURE 5-9. CDD Device Driving Four PLAYER Devices Using Two F100115 Quad Low Skew Drivers

5.0 Detailed Information (Continued)

5.3 LAYOUT RECOMMENDATIONS

- The part should be bypassed between the $EXTV_{CC}$ and EXTGND as close to the chip as possible (preferably under the chip using chip caps). The part should also be bypassed between the DV_{CC} and DGND as close to the chip as possible.
- The part should be bypassed between AV_{CC} and AGND as close to the chip as possible.
- No TTL logic lines should pass through the external crystal or filter circuitry areas to avoid the possibility of noise due to crosstalk.
- The filter circuitry should be connected to Ground on an isolated branch off of the AGND pin.
- The DV_{CC} pin should be connected to V_{CC} on an isolated branch off of the $EXTV_{CC}$ pin, preferably being connected through a ferrite bead or small inductor.
- The AV_{CC} pin should be connected to V_{CC} on an isolated branch off of the DV_{CC} pin, preferably being connected through a ferrite bead or small inductor.
- The external crystal circuitry should be connected to Ground on an isolated branch off of the DGND pin.
- The DGND pin should be connected to Ground off of an isolated branch of the EXTGND pin, connected through a ferrite bead or small inductor.
- The AGND pin should be connected to Ground off of an isolated branch of the DGND pin, connected through a ferrite bead or small inductor.
- If the part is being driven by an external reference, the XTL IN pin should be tied to either GND or V_{CC}.
- If using a multilayered board with dedicated V_{CC} and Ground planes, ensure that the external crystal circuitry has its own small isolated ground island that is connected to the AGND, DGND and EXTGND pins as described above.
- See *Figure 5.1* for component values.
- For best performance tie the VCORST pin to AGND.



This drawing was done with convenience in mind. TL/F/10385–15

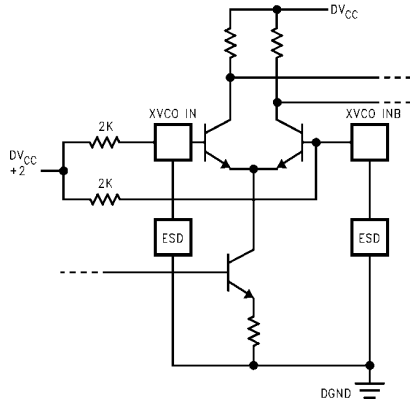
Note: Pin 7 need not be hooked up.

FIGURE 5-10. Recommended Layout

5.0 Detailed Information (Continued)

5.4 INPUT AND OUTPUT SCHEMATICS

XVCO IN, XVCO INB



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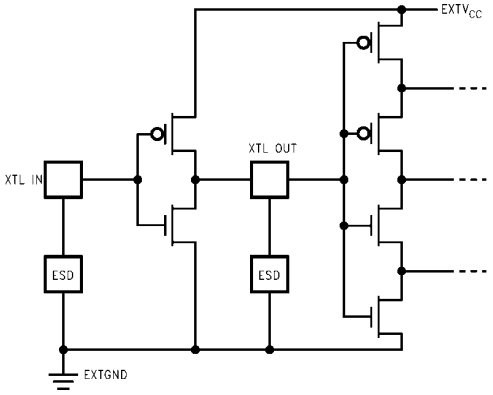
XTL IN, XTL OUT



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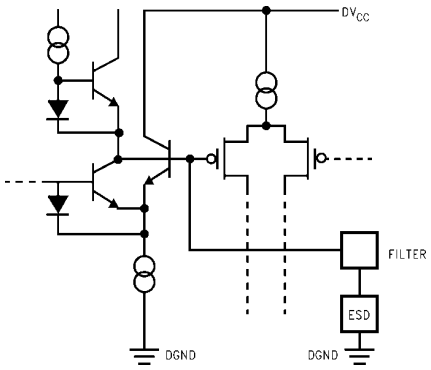
Filter



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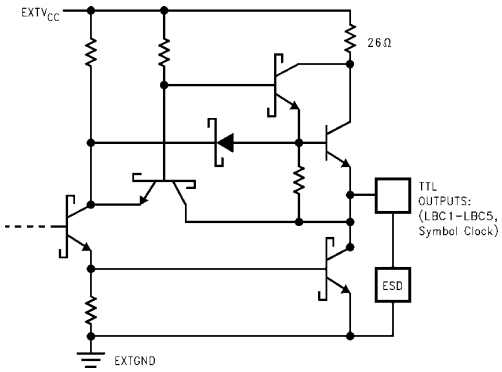
TTL Outputs: LBC1–LBC5, Symbol Clock



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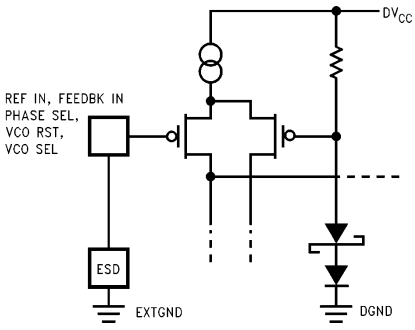
CMOS Inputs: REF IN, FEEDBK IN, PHASE SEL, VCO RST, VCO SEL



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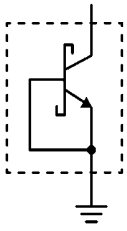
Typical ESD Structure



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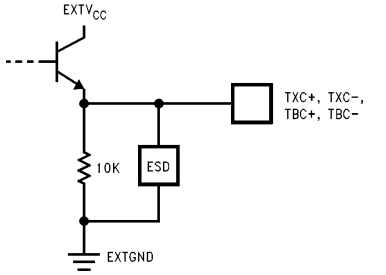
TXC+, TXC−, TBC+, TBC−



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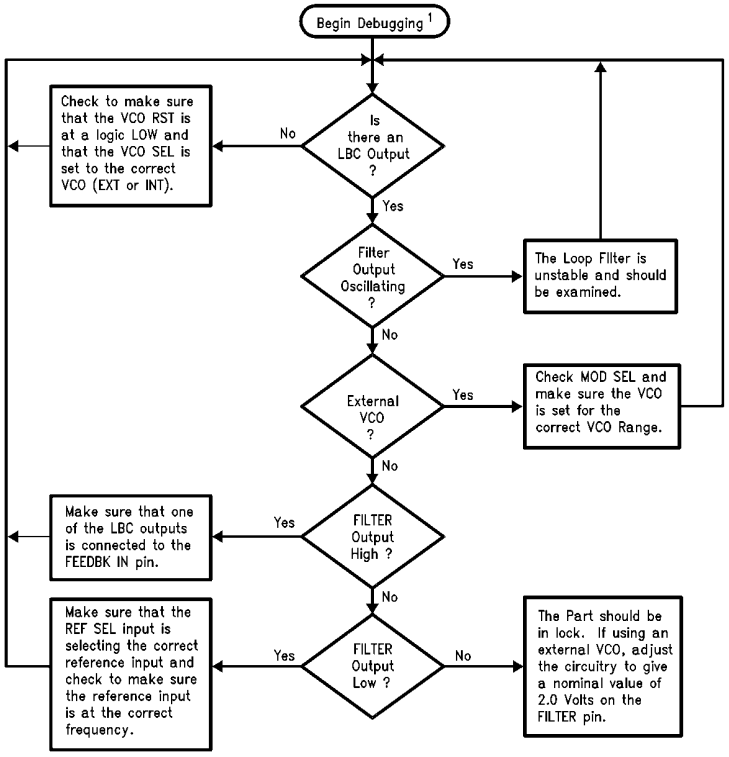
5.0 Detailed Information (Continued)

5.5 SYSTEM DEBUGGING FLOWCHART



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Note 1: If the crystal oscillator is chosen as the input reference source then the XTL OUT pin should be checked for the correct frequency of oscillation. If the oscillator fails to oscillate then the DC voltage on these pins should be checked and be equal to approximately $V_{CC} \div 2$ (with or without the crystal oscillator present).

5.6 AC TEST CIRCUITS

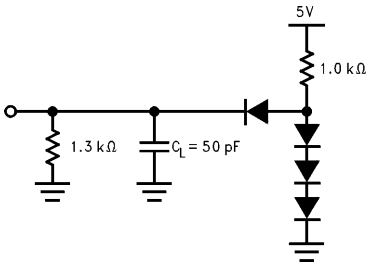

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FIGURE 5-11. Switching Test Circuit for All TTL Output Signals

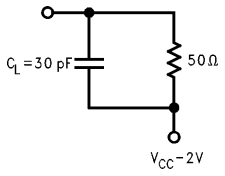

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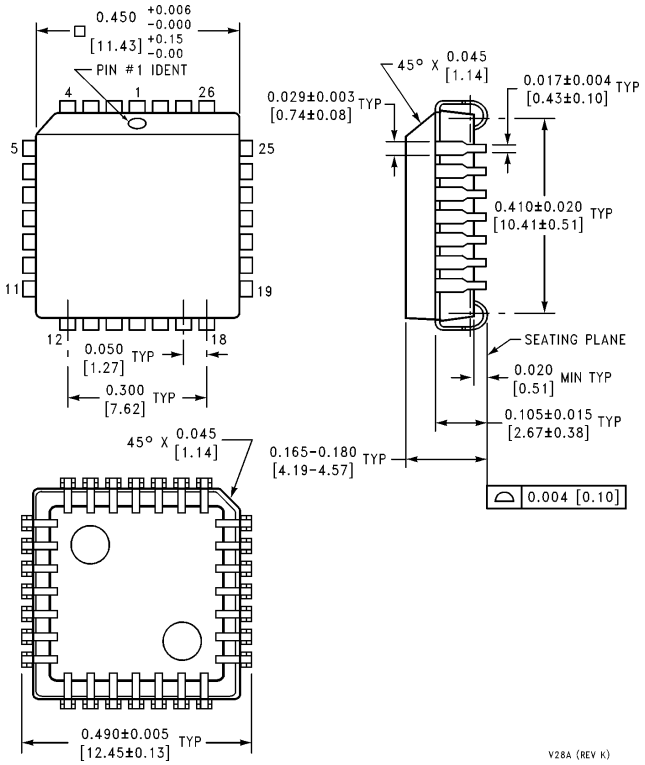
FIGURE 5-12. Switching Test Circuit for All ECL Output Signals

Physical Dimensions inches (millimeters)



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