National Semiconductor

PRELIMINARY
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DP83856B 100 Mb/s Repeater Information Base

General Description

The DP83856B 100 Mb/s Repeater Information Base is designed specifically to meet the management demands of today's high speed Ethernet networking systems.

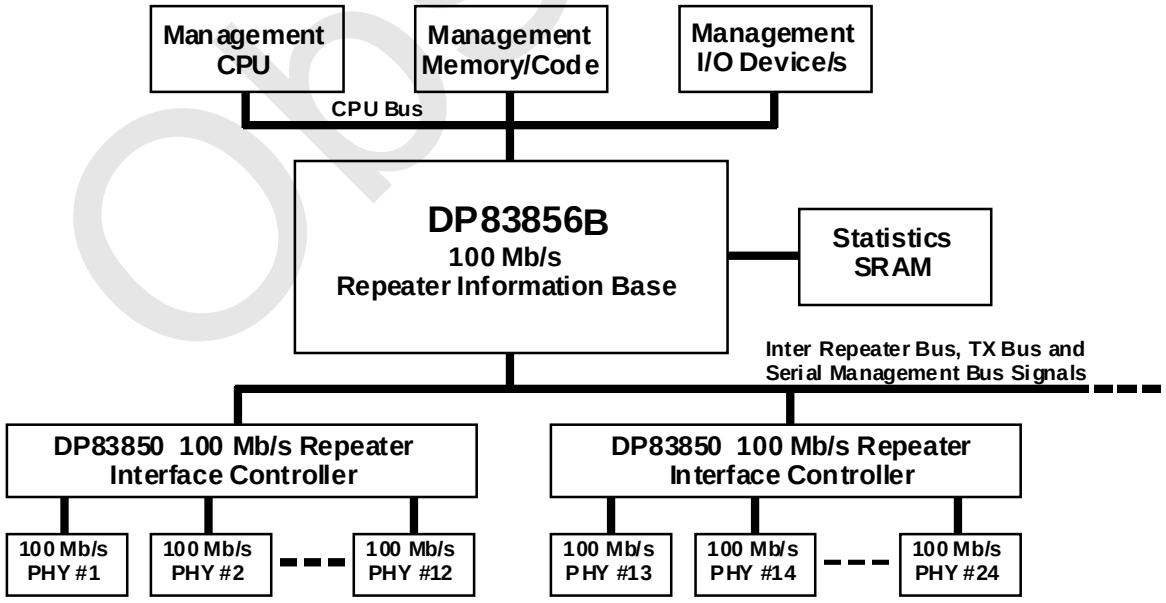
The DP83856B simplifies design of managed multiport repeaters. Used in conjunction with up to 16 DP83850s it enables a repeater system to become a single managed entity that is fully compatible with the IEEE 802.3u clause 30 management requirements.

The DP83856B device incorporates all the necessary functions and counters for collecting network statistics. Information is gathered on a per-packet, per-port basis: the port which is receiving the packet is the active port for statistics collection.

Features

- Supports up to 16 DP83850 Repeater Interface Controllers (192, 100Mb ports on one segment)
- Fully IEEE 802.3u clause 30 compatible
- Network management statistics processed on a per activity (per packet) basis
- Programmed I/O interface for statistics reporting
- Uses external SRAM to maintain per port network management statistics counters
- Single interrupt acknowledgment provides report on all per port SRAM based and P83856B based statistics
- Parallel register interface to CPU (16-bit)
- Allows indirect access to the DP83850 Repeater Interface Controller and DP83840 Physical Layer Device serial registers through a parallel register interface
- 132 pin PQFP

System Diagram



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Block Diagram

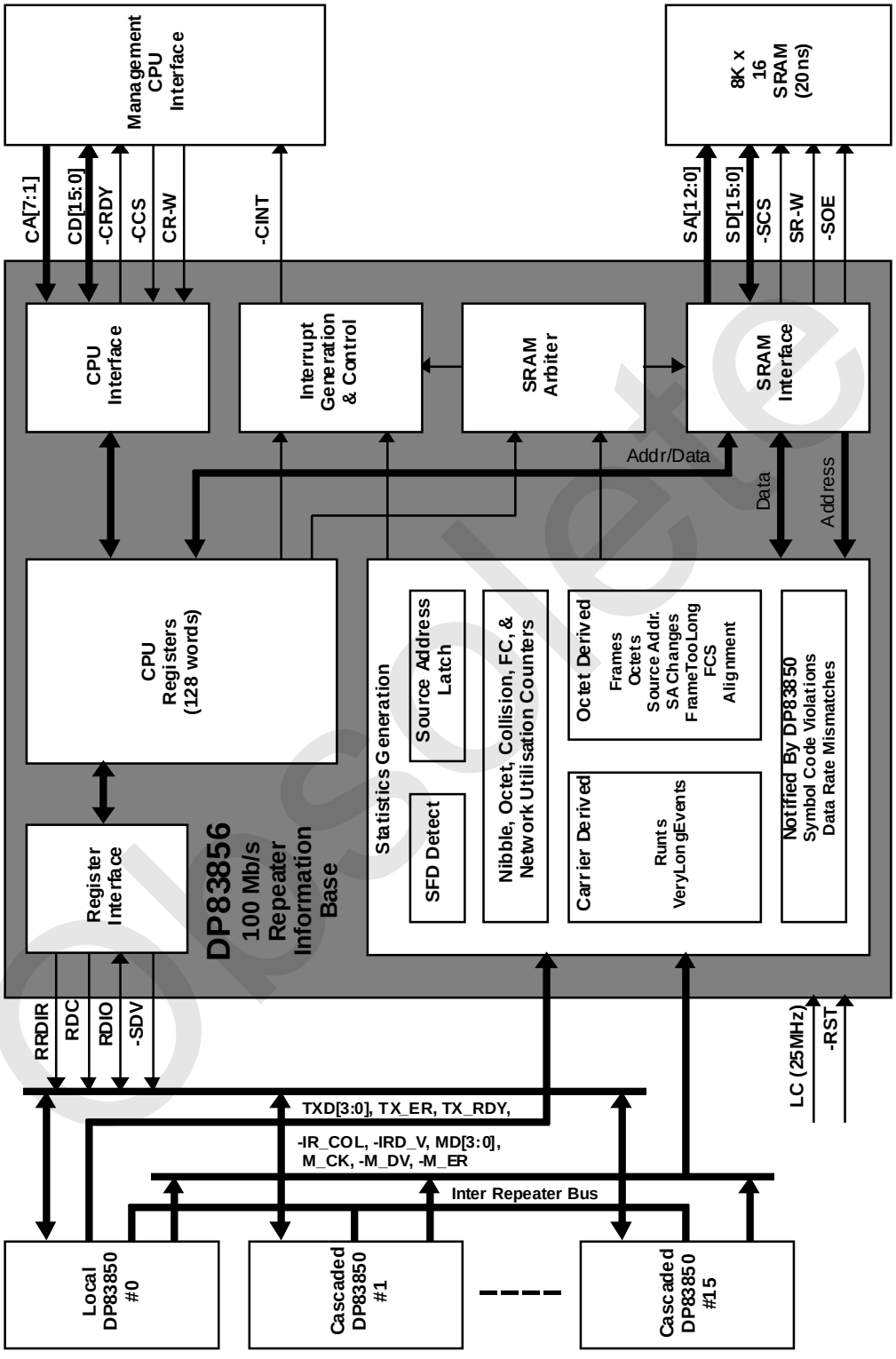

Table of Contents

1.0 Pin Connection Diagram

DP83856B

100 Mb/s Repeater Information Base

132 pin PQFP
(top view)

Order Number DP83856BVF
NS Package Number VF132A

2.0 Pin Descriptions

2.1 CPU Interface

The CPU interface pins are a set of generic interface signals designed to accommodate many different CPU types with minimal external logic. The data interface is 16-bits wide and does not provide any steering capabilities. Furthermore, all accesses must be aligned on 16-bit boundaries, as indicated in the CPU Register map section 4.0.

Signal Name	Type	Active	Description
-CINT	O/Z, L	Low	CPU Interrupt: Indicates that the DP83856B has at least one interrupt pending. The -CINT signal will remain active until the CPU reads the Interrupt Register. It is software's responsibility to keep track of multiple interrupts pending, and service all of the interrupts.
-CRDY	O/Z, L	Low	CPU Ready: Indicates that the DP83856B is ready to terminate the current cycle. The DP83856B asserts -CRDY on writes once it has strobed the data into its write data holding register. The DP83856B asserts -CRDY on reads once it has strobed data into its read data output register.
-CCS	I	Low	CPU Chip Select: Chip select for internal DP83856B registers. Generated by external logic as an address decode of the DP83856B register space. -CCS must remain valid for the entire cycle.
CR-W	I	-	CPU Read-Write: Read/Write strobe for DP83856B internal registers. Read = 1, Write = 0.
CA[7:1]	I	-	CPU Address [7:1]: Address bus for DP83856B register accesses. The DP83856B latches the address for internal use within 45ns of -CCS being asserted.
CD[15:0]	I/O/Z, M	-	CPU Data [15:0]: 16-bit data bus for DP83856B register accesses. CD[15:0] correspond to the low 16-bits of data on the CPU. The DP83856B implements Big Endian convention for data storage. All CPU register accesses should be 16-bit accesses aligned on 16-bit boundaries.

2.2 SRAM Interface

The SRAM interface pins are used to connect the DP83856B to a fast (20ns) external SRAM. The DP83856B supports up to an 8K x 16 bit SRAM configuration.

Signal Name	Type	Active	Description
SA[12:0]	O/Z, L	-	SRAM Address [12:0]: The SRAM address bus should be directly connected to the fast external SRAM's address inputs.
SD[15:0]	I/O/Z/P, L	-	SRAM Data [15:0]: The SRAM data bus should be directly connected to the fast external SRAM's data pins.
SR-W	O/Z,L	-	SRAM Read-Write: Should be directly connected to the fast external SRAM's write enable pin. Read = 1, Write = 0.
-SCS	O/Z, L	Low	SRAM Chip Select: Should be directly connected to the fast external SRAM's chip select pin.
-SOE	O/Z, L	Low	SRAM Output Enable: Should be directly connected to the fast external SRAM's (active low) output enable pin.

2.3 Transmit Bus and Management Bus

Signal Name	Type	Active	Description
TXD[3:0]	I	-	Transmit Data [3:0]: Transfers data from a local DP83850 to the DP83856B. TXD[3:0] is synchronous to the local clock signal LC, and is framed by the transmit ready signal TX_RDY.
TX_RDY	I	High	Transmit Data Ready: Asserted by a local DP83850 when non-idle symbols are repeated on any of the DP83850's output ports. The DP83856B uses this signal as a framing signal for transmit data, transmit error, management data, management error, collision, data valid, and as an enable for carrier and network utilization timing.
TX_ER	I	High	Transmit Data Error: Asserted by a local DP83850 when a transmit error occurs. The DP83856B monitors this signal to determine if the current reception was a Symbol Code violation error. TX_ER is synchronous to the local clock signal LC.
- IR_COL	I	Low	Inter Repeater Collision: Asserted by any (all) DP83850s in the system which are currently experiencing a collision. The DP83856B monitors this signal during TX_RDY valid, and uses the information in statistics processing and collision counting.
- IRD_V	I	Low	Inter Repeater Data Valid: Asserted by any DP83850 in the system which has won the Inter Repeater Bus arbitration and is transmitting valid data symbols. The DP83856B monitors this line at the beginning of the frame to establish whether the frame is a false carrier event. If TX_RDY is valid and -IR_DV is invalid when the DP83856B samples the -IR_DV line, then a false carrier event is counted.
MD[3:0]	I	-	Management Data [3:0]: Data which is sourced by any DP83850 in the system which has won the Inter Repeater Bus arbitration. This data is synchronous to the management clock M_CK, and is framed by the transmit ready signal TX_RDY. The DP83856B uses this data to determine the source of the current data stream (DP83850 number and Port number).
- M_DV	I	Low	Management Data Valid: Asserted by any DP83850 in the system which has won the Inter Repeater Bus arbitration when it places valid data on MD[3:0]. The DP83856B monitors this line when TX_RDY is valid to determine when to latch the RIC and port number for the current reception. -M_DV is synchronous to M_CK.
M_CK	I	-	Management Clock: All data transfers on the management bus are synchronized to the rising edge of this clock. M_CK is the reference 25MHz clock for determining the active DP83850, port, and elasticity buffer errors for the current packet reception. M_CK is sourced by any DP83850 in the system which has won the Inter Repeater Bus arbitration.
- M_ER	I	Low	Management Error: Asserted by any DP83850 in the system which has won the Inter repeater Bus arbitration when a data rate mismatch error occurs (elasticity buffer over/underrun). The DP83856B monitors this line during TX_RDY valid to determine if the current frame contains a data rate management error. -M_ER is synchronous to M_CK.

2.4 MII Interface

Signal Name	Type	Active	Description
RDC	O/Z, L	-	Register Data Clock: A 2.5MHz clock which is continuously output from the DP83856B. Used to synchronize data transfers on the serial MII register bus.
RDIO	I/O/Z, L	-	Register Data I/O: Serial MII register data signal. Used to transfer data to and from the DP83856B on MII register accesses. This signal should be buffered onto the backplane, using the RRDIR signal as a direction control for the buffer. The buffer does not require a tri-state enable.
RRDIR	O/Z, L	High	RIB Register Direction: Serial MII Register Direction pin to drive an external buffer. The buffer should default to READ, and toggle to WRITE only when the DP83856B is initiating an MII register access. 0 = MII Slave (DP83850 or PHY) drives RDIO 1 = DP83856B drives RDIO
- SDV	O/Z, L	Low	Serial Data Valid: Indicates that a valid MII access is in progress. It is asserted one half clock prior to the start of the cycle and remains valid for one half clock after the cycle is complete.

2.5 Test Interface

Signal Name	Type	Active	Description
- TSTATE	I/P	Low	Tri-State: Pulling this pin low puts the DP83856B into a test mode that tristates all outputs except -NAND_E and -NAND_O. This allows an external tester to drive all the outputs of the DP83856B.
- TEST_EN	I/P	Low	Test mode Enable High/Low output test: Forces the DP83856B's outputs to the High or Low state as defined by the -TEST_H_L pin. This enables testers to check for outputs stuck at High or Low.
- TEST_H_L	I/P	Low	Test mode output High/Low: When -TEST_EN is taken Low, the DP83856B's output pins (in two groups) are forced into the High or Low state as defined below: -TEST_H_L Group 1 Outputs Group 2 Outputs 0 1 0 1 0 1 Group 1 output pin numbers are: 21, 23, 27, 31, 35, 37, 39, 43, 61, 64, 68, 70, 72, 74, 78, 80, 82, 87, 89, 90, 92, 96, 98, 100, 104, 108, 113, 115. Group 2 output pin numbers are: 20, 22, 24, 30, 34, 36, 38, 42, 44, 65, 69, 71, 73, 75, 79, 81, 83, 88, 91, 93, 97, 99, 103, 105, 114, 116.
- NAND_E	O, L	Low	NAND tree Even inputs output: The logical NAND of all of the even numbered inputs (except the test input -TEST_EN) and -RST. If all of the inputs are High, the output will go Low. If any of the inputs are Low, the output will remain High.
- NAND_O	O, L	Low	NAND tree Odd inputs output: The logical NAND of all of the odd numbered inputs (except the test inputs -TSTATE, -TEST_H_L and LC). If all of the inputs are High, the output will go Low. If any of the inputs are Low, the output will remain High.

2.6 Miscellaneous Pins

Signal Name	Type	Active	Description
LC	I	-	Local Clock: Primary clock for DP83856B device. All DP83856B internal state machines run off LC. This clock must be the same local clock used to drive the local DP83850 because the TX signals (to which the DP83856B must be synchronized) are all synchronous to the local clock. Must be a 25.000MHz, 40/60 duty cycle, 50ppm.
- RST	I	Low	Reset: The DP83856B is reset when this signal is asserted low. Asserting this signal will cause all DP83856B state machines and registers to enter their reset state.
RES1	O	-	Reserved Output 1: Leave unconnected.
RES2	O	-	Reserved Output 2: Leave unconnected.

2.7 Pin Type Designation

Type	Description
I	Input buffer.
I/P	Input buffer with internal pull-up resistor.
O, L	Output buffer, low drive(4mA).
O/Z, L	Output buffer with high impedance capability, low drive (4mA).
I/O/Z, L	Bi-directional buffer with high impedance capability, low drive (4mA).
I/O/Z, M	Bi-directional buffer with high impedance capability, medium drive (12mA).
I/O/Z/P, L	Bi-directional buffer with high impedance capability and pull-up resistor, low drive (4mA).

3.0 Functional Description

The following sections describe the different functional blocks of the DP83856B 100 Mb/s Repeater Information Base. Referring to the block diagram on page 2 of this datasheet, the DP83856B is used in conjunction with a number of DP83850s, a management CPU and a fast (20ns) 8k x 16 bit SRAM. The DP83856B collects and maintains network management statistics from the connected DP83850s and makes them available to the management CPU.

3.1 Statistics Generation

Inputs to the DP83856B Statistic Generation block include the Inter Repeater Bus signals, Management Bus signals and TX BUS signals. These signals provide the data streams necessary to create all the statistics collected by the DP83856B. The DP83856B uses the fast external SRAM to hold statistics for the current packet reception. Statistics for the current receive packet are collected in one of four ways:

3.1.1 Octet Derived

The majority of the statistics are a function of the octet count. Statistics based on octet counts imply that a valid SFD has been detected and an accurate count of the number of data bytes in the packet are available.

The DP83856B Statistic Generation module has an SFD detect block, which indicates that a valid SFD has been detected so that the octet counter can be enabled. The Source Address latch is used to store the source address of the current packet, so that a comparison to the previous source address can be made at the end of the packet reception. Octet derived statistics include:

Frames
Octets
FCS Errors
Alignment Errors
Frames Too Long
Source Address
Source Address Changes

3.1.2 Carrier Derived

Other statistics are a function of carrier. Carrier derived statistics have a high probability of occurring on activity bursts which do not include a valid SFD. To ensure accurate statistic gathering a carrier based detection scheme is implemented. A nibble counter is used to calculate the length of the carrier, which is used to create the carrier derived statistics.

The DP83856B employs 32-bit counters for network utilization, false carrier events, and collisions. All of these counters monitor events for all ports, i.e. they are an aggregate of the total repeater events.

Carrier derived statistics gathered by the DP83856B include:

Runts
Very Long Events (jabber)
Network Utilization
Repeater False Carrier Events
Repeater Collisions (per port collision map obtained from DP83850s)

3.1.3 DP83850 Notified

For a few of the required statistics the DP83856B has no way of determining the occurrence of that event. These statistics are obtained by notification from the connected DP83850s. DP83850 notified statistics include:

Data Rate Mismatches
Symbol Code Violations

3.1.4 Collision Counter

The 100 RIB has a 32 bit counter which is incremented any time the repeater experiences a collision. This counter is used to keep track of total number of collisions happening on the repeater.

3.2 SRAM Interface

The SRAM interface provides the logic required to communicate with the fast external SRAM.

The interface between the DP83856B and the fast external SRAM is very straightforward. The fast external SRAM is a dedicated block of memory directly accessed only by the DP83856B. The DP83856B provides the address capability for 8Kx16 bits of SRAM.

Figure 1 shows a memory map for the 8Kx16 configuration. For each port there are 11 statistics defined which are stored in SRAM. Ten of these statistics are 32 bit values, and one is a 48 bit value (Last Source Address).

Last Source Address is stored in little endian mode as two 32 bit values for simplicity of hardware implementation. All other statistics are stored in big endian mode.

The DP83856B can be directly connected to the SRAM; there is no need for buffering between the DP83856B and the SRAM. The DP83856B requires fast SRAM with a maximum access time of 20ns.

The SRAM interface block contains the address and data multiplexers to select between CPU and Statistic Update accesses. Data is multiplexed under control of the SRAM arbiter

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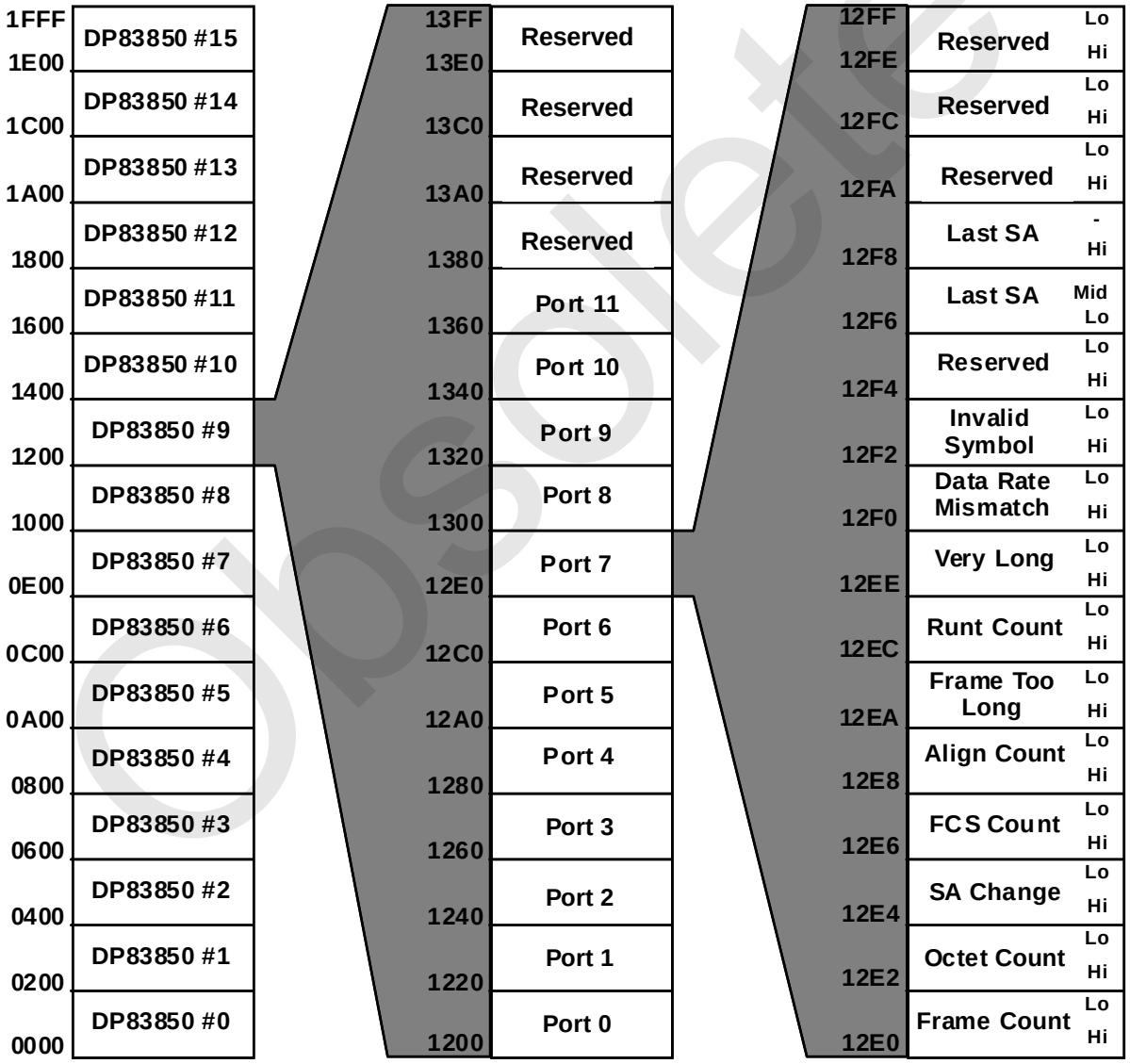


Figure 1. Memory Map for the DP83856 Statistics SRAM

3.3 SRAM Arbiter

The SRAM arbiter controls the SRAM data multiplexers depending on what type of access is being performed and creates all of the control signals for the SRAM, ensuring the timing is correct. There are three events that result in SRAM arbitration:

- End of packet request- Runt (Statistic Update State Machine)
- End of packet request- Legal Length or greater (Statistic Update State Machine)
- CPU request (read or write)

The arbiter assigns highest priority to EOP-runts and lowest priority to CPU requests. For single statistic reads, the arbiter produces two 16-bit locked read cycles on the SRAM to form the 32-bit value. For block reads the SRAM arbiter re-arbitrates after each 32-bit SRAM read (two 16-bit locked reads) to allow any higher priority event access to the SRAM. Writes to the SRAM must always be word (16-bit) accesses: byte writes are not supported.

3.4 Interrupt Generation and Control

There are four events that can generate an interrupt:

- SRAM access complete
- MII Register access complete
- Invalid MII register read
- DP83856B error

The DP83856B provides one interrupt line that is shared for all interrupts. The interrupt is an active low, level sensitive signal. Interrupts are generated based on a valid event occurring with the appropriate mask bit set. Interrupts are cleared by reading the interrupt register.

The "Invalid MII register read" interrupt is generated based on the DP83856B detecting an error while performing a read access. The DP83856B looks for a leading 0 on reads; if it does not see it, it flags the read as invalid and generates the interrupt.

3.5 MII Register Interface

The MII register interface block is a state machine that performs accesses to DP83850 and Physical Layer Device registers (read & write) based on requests from the CPU.
This interface uses the IEEE 802.3u clause 22 MII compliant serial interface protocol.

The MII Register Interface eliminates the need for the CPU to talk directly to the DP83850 and Physical Layer Device registers. The amount of spare management CPU processing bandwidth is therefore increased.

The CPU provides the opcode, type of access (read or write), register address, and device ID to the MII Interface Register, and then asserts a start command by writing a 1 to bit 0 (MII_ACC) of the Configuration Register.

MII Protocol for performing reads and writes are as follows:

READ
<01><10><AAAAA><RRRRR><z0><xxxx xxxx xxxx xxxx>
where <01> is a start bit sequence, <10> is a read opcode, <AAAAA> is the device address (up to 32 devices), and <RRRRR> is the register address (up to 32 registers). <z0> is a 2-bit turn-around time used to avoid contention on RDIO. During the first bit time no device actively drives RDIO (all devices are in a high-impedance state). During the second bit time, the slave device will drive a 0 onto RDIO. Finally, <xx ... xx> is 16 bits of data.

WRITE
<01><01><AAAAA><RRRRR><10><xxxx xxxx xxxx xxxx>
where <01> is a start bit sequence, <01> is a write opcode, <AAAAA> is the device address (up to 32 devices), and <RRRRR> is the register address (up to 32 registers). <10> is a 2-bit turn-around. For this turn-around, the DP83856B will drive a 1 for the first bit time and a zero for the second bit time. Finally, <xx ... xx> is 16 bits of data.

Refer to the IEEE 802.3u standard for more details on the MII interface, its function and timing.

3.6 CPU Register Block

The CPU register block provides the system management CPU access to all of the data in the DP83856B, SRAM and connected DP83850s and Physical Layer Devices

4.0 Registers

All the DP83856B registers are directly addressable by the system management CPU. Although some bits in the Configuration Register have been allocated to a register paging scheme, these are not currently used (they're there for future expansion) and should always be set to zero.

All register accesses are word (16-bit) wide: byte access is not supported. The addresses given in the tables below assume that the user has connected the DP83856B to a management CPU in the normal 16-bit manner with address bits A1 through A7 from the CPU connected to bits CA1 to CA7 on the DP83856B. The addresses are thus the offset from the base address at which the DP83856B is located in the system.

4.1 Register Memory Map

Address	Register	Access
00h	Configuration Register	R/W
02h	Interrupt	R/W
04h	Reserved	-
06h	SRAM Interface	R/W
08h	MII Management Interface	R/W
0Ah	SRAM Write Data	R/W
0Ch	MII Write Data	R/W
0Eh	Device ID	R only
10h	Frame Count Hi Read	R/W
12h	Frame Count Lo Read	R/W
14h	Octet Count Hi Read	R/W
16h	Octet Count Lo Read	R/W
18h	Source Address Change Count Hi Read	R/W
1Ah	Source Address Change Count Lo Read	R/W
1Ch	FCS Error Count Hi Read	R/W
1Eh	FCS Error Count Lo Read	R/W
20h	Alignment Error Count Hi Read	R/W
22h	Alignment Error Count Lo Read	R/W
24h	Frame Too Long Count Hi Read	R/W
26h	Frame Too Long Count Lo Read	R/W
28h	Runt Count Hi Read	R/W
2Ah	Runt Count Lo Read	R/W
2Ch	Very Long Event Count Hi Read	R/W
2Eh	Very Long Event Count Lo Read	R/W
30h	Data Rate Mismatch Count Hi Read	R/W
32h	Data Rate Mismatch Count Lo Read	R/W
34h	Invalid Symbol Count Hi Read	R/W
36h	Invalid Symbol Count Lo Read	R/W
38h	Reserved	-
3Ah	Reserved	-
3Ch	Source Address Hi Read	R/W
3Eh	Source Address Mid Read	R/W
40h	Source Address Lo Read	R/W
42h	Reserved	-
44h - 7Eh	Reserved	-
80h	Carrier Count Register	R/W
82h	Oct_Nib Count Register	R/W
84h - 8Eh	Reserved	-

Register Memory Map Continued

Address	Register	Access
90h	Repeater Collisions Hi Read	R/W
92h	Repeater Collisions Lo Read	R/W
94h	Network Utilization Hi Read	R/W
96h	Network Utilization Lo Read	R/W
98h	False Carrier Hi Read	R/W
9Ah	False Carrier Lo Read	R/W
9Ch - 9Eh	Reserved	-
A0h	MII Read Data / Port 0-11 Short Event Hi Block Read Data	R only
A2h	DP83850 Port 0-11 Short Event Lo Block Read Data	R only
A4h	DP83850 Port 0-11 Late Event Hi Block Read Data	R only
A6h	DP83850 Port 0-11 Late Event Lo Block Read Data	R only
A8h	DP83850 Port 0-11 Collision Hi Block Read Data	R only
AAh	DP83850 Port 0-11 Collision Lo Block Read Data	R only
ACh	DP83850 Port 0-11 Auto-Partitions Block Read Data	R only
AEh	Reserved	-
B0h - 1FEh	Reserved	-

4.2 Configuration Register

Address: 00h
Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D0	MII_ACC	R/W	0: DP83856B writes 0 after register access completes. 1: CPU initiates register access by writing 1 This bit indicates when the current DP83850 or Physical Layer device register access is complete.
D1	SR_ACC	R/W	0: DP83856B writes 0 after SRAM access completes. 1: CPU initiates SRAM access by writing 1. This bit indicates when the current SRAM access is complete.
D2	SR_ACC_TYPE	R/W	0: Perform Single Access 1: Perform Block Access (Reads Only) All SRAM based statistics will be loaded into SRAM (CPU Addr. 10h - 40h) Note: If you set this bit to a 1, the STAT # field and the R/W bit in the SRAM I/F Register will be ignored (Addr 06h, bits 4:0 and 7 respectively).
D3	MEN	R/W	0: Statistics gathering disabled 1: Statistics gathering enabled This bit enables management statistics gathering.
D(4:7)	PAGE_SEL	R/W	These bits define which page of the register map the CPU is pointing to. Allows for 16 pages x 256 word registers. Always write 0 for compatibility with later versions of DP83856B. **Note:** The Page bits are not implemented in current version.
D(8:15)	Reserved	R/W	Write: 0 Read: Undefined.

4.3 Interrupt Register

Address: 02h
Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D0	MII_INT_STS	R	1: MII access complete Interrupt asserted. Cleared by read of register. Writes ignored.
D1	SR_ACC_STS	R	1: SRAM access complete Interrupt asserted. Cleared by read of register. Writes ignored.
D2	RIBERR_STS	R	1: DP83856B error Interrupt asserted. Cleared by read of register. Writes ignored.
D3	MII_RD_ERR_STS	R	1: MII (MII) register read error Interrupt asserted. Cleared by read of register. Writes ignored.
D4	MII_INT_MSK	R/W	0: Mask MII access complete Interrupt. 1: Enable MII access complete Interrupt.
D5	SR_ACC_MSK	R/W	0: Mask SRAM access complete Interrupt. 1: Enable SRAM access complete Interrupt.
D6	RIBERR_MSK	R/W	0: Mask DP83856B error Interrupt. 1: Enable DP83856B error Interrupt.
D7	MII_RD_ERR_MSK	R/W	0: Mask MII Register Error Interrupt. 1: Enable MII Register Error Interrupt. This bit indicates the occurrence of an MII register read error.
D8	INT_EN	R/W	0: Disable -CINT signal. 1: Enable -CINT signal. This bit is a global enable for the -CINT signal. It has NO effect on the status bits.
D(9:15)	Reserved	R/W	Write: 0 Read: Undefined.

4.4 SRAM Interface Register

Address: 06h
Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:4)	STAT_ACC#	R/W	These bits set which STATISTIC the SRAM access is destined for. Values are: **00h:** Frame Count **02h:** Octet Count **04h**: SA Change Count **06h:** FCS Error Count **08h:** Alignment Error Count **0Ah:** Frame Too Long Count **0Ch:** Runt Count **0Eh:** Very Long Event Count **10h**: Data Rate Mismatch Count **12h:** Invalid Symbol Count **14h:** Reserved **16h:** Source Address Hi **18h:** Source Address Lo **1Ah-1Eh:** Reserved
D(5:6)	Reserved	R/W	Always Write 0
D7	R/W_SRAM	R/W	0: SRAM Write 1: SRAM Read This bit defines whether the current CPU SRAM access is a read or a write. Ignored for block accesses.
D(8:11)	PORT_ACC#	R/W	These bits set which PORT the access is destined for: Valid values are 0h - Bh (12 ports)
D(12:15)	RIC_ACC#	R/W	These bits set which DP83850 the access is destined for. Valid values are 0h - Fh (16 DP83850s)

Note: This register should NOT be accessed while an SRAM access is in progress (If bit D1 of Configuration Register is 1, then do not access this register).

4.5 MII Management Interface Register

Address: 08h
Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:4)	REG_ADDR	R/W	These bits set which register the access is destined for.
D(5:9)	DEV_ID	R/W	These bits set which DEVICE_ID the access is destined for.
D(10:11)	OPCODE	R/W	Opcode value: Corresponds to the opcodes defined in the MII specification. 01: Extended Addressed Mode Write, 16-bit payload. 10: Extended Addressed Mode Read, 16-bit payload.
D12	MII_ACC_TYP	R/W	MII Access Type: Sets the access type to single or block read:. 0: Perform Single Access (All Physical Layer device accesses and all DP83850 accesses except DP83850 counters). 1: Perform Block Read (DP83850 reads only). All DP83850 based counters will be loaded into registers (Address A0h-ACh). The OPCODE field should be set to 10 for block reads. REG_ADDR is set to register address corresponding to the Port_ShortEvent Counter for the desired port.
D(13:15)	Reserved	R/W	Write: 0 Read: Undefined.

4.6 SRAM Write Data Register

Address: 0Ah
Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:15)	WR_DATA	R/W	This register contains the data to be written on an SRAM write access. SRAM writes should only be performed during DP83856B initialization.

4.7 MII Write Data Register

Address: 0Ch
Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:15)	WR_DATA	R/W	This register contains the data to be written on an MII register write access.

4.8 Device ID Register

Address: 0Eh
Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:3)	REV_LEVEL	R	These bits are the Revision level of the device and are embedded into the DP83856B silicon. Reads 0h for initial revisions.
D(4:7)	DEVICE ID	R	These bits are a vendor specific code embedded in the DP83856B. Reads 0 for initial revision.
D(8:15)	Reserved	R/W	Write: 0 Read: Undefined.

4.9 SRAM Read Data Registers

Addresses: 10h - 40h
Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:15)	SRAM Read Data	R	Contains data corresponding to the SRAM location selected.

4.10 Carrier Count Register

Address: 80h
Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:13)	Carrier Count	R/W	Contains data which is used to preset the carrier counter FOR TEST PURPOSES only. This register can only be written when the MEN bit in the CONFIG register is 0.
D(14:15)	Unused	R/W	Write: 0 Read: Undefined.

4.11 Oct_Nib Count Register

Address: 82h
Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:11)	Oct_Nib Count	R/W	Contains data which is used to preset the Octet-Nibble counter FOR TEST PURPOSES only. This register can only be written when the MEN bit in the CONFIG register is 0.
D(12:15)	Unused	R/W	Write: 0 Read: Undefined.

4.12 Network Counters

Addresses: 90h - 9Ah
Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:15)	Counter Data	R/W	Contains data corresponding to the selected counter. Disable the Management function by writing 0 to the MEN, bit D3 in the Configuration Register prior to writing to these counters.

4.13 MII Read Data Registers

Addresses: A0h - ACh
Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(15:0)	MII Data	R	Contains read data corresponding to the MII register selected.

For single Physical Layer Management register read accesses and single statistic read accesses to connected DP83850s, the read data appears in data register address A0h. When the DP83856B is instructed to do a block statistics read from a connected DP83850, the block of 7 read values is placed in the registers A0h to ACh. The register's designations are given in the memory map in section 4.1 above.

5.0 A.C. and D.C. Specifications

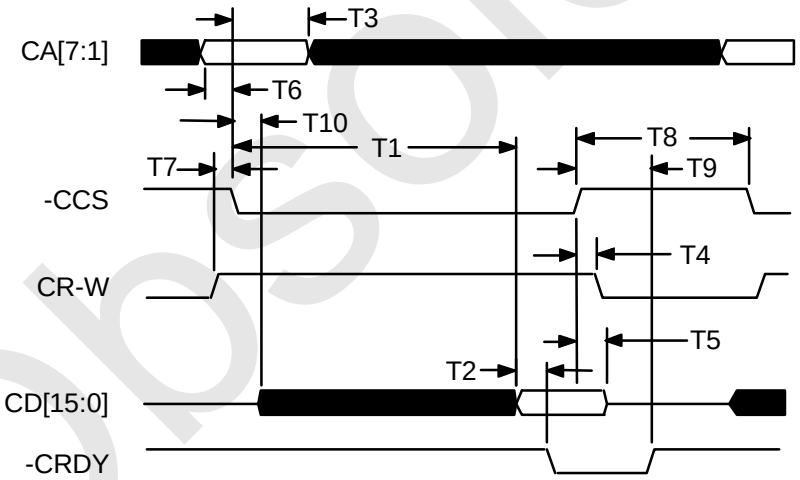
5.1 D.C. Specifications

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Minimum High Level Output Voltage		3.7		V
V_{OL}	Maximum Low Level Output Voltage			0.4	V
V_{IH}	Minimum High Level Input Voltage		2.0		V
V_{IL}	Maximum Low Level Input Voltage			0.8	V
I_{IN}	Input Current			±150	µA
I_{OZ}	Minimum TRI-STATE Output Leakage Current			±160	µA
I_{CC}	Supply Current (Calculated)			150	mA

5.2 A.C. Specifications

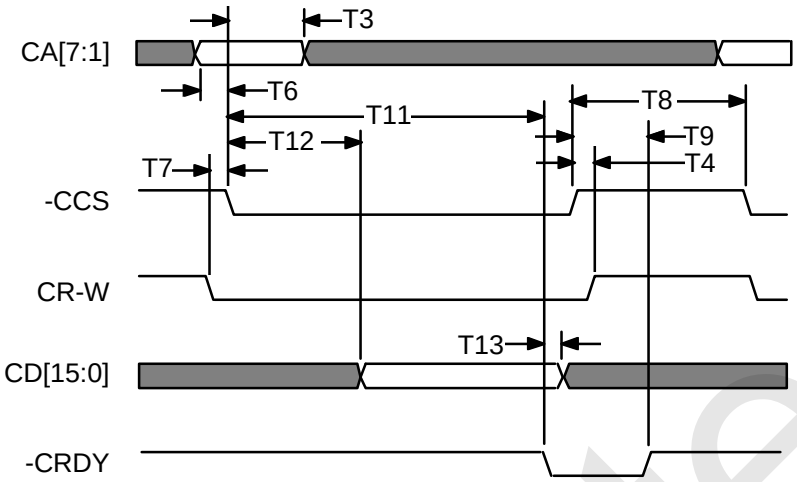
Some timing parameters are shown more than once (both on the same timing diagram, and in different sections) for clarity.

5.2.1 CPU Read Timing



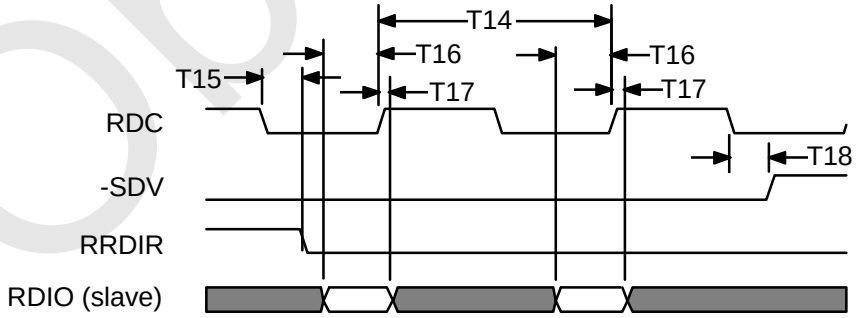
	Description	Min (ns)	Max (ns)
T1	-CCS low to CPU Data valid	-	180
T2	CPU Data valid to -CRDY low	10	-
T3	CPU Address hold from -CCS low	60	-
T4	CR-W hold from -CCS high	0	-
T5	CPU Data hold from -CCS high	0	-
T6	CPU Address setup to -CCS low	0	-
T7	CR-W setup to -CCS low	0	-
T8	-CCS high between cycles	100	-
T9	-CCS high to -CRDY high	-	60
T10	-CCS low to CPU Data driven	0	20

5.2.2 CPU Write Timing



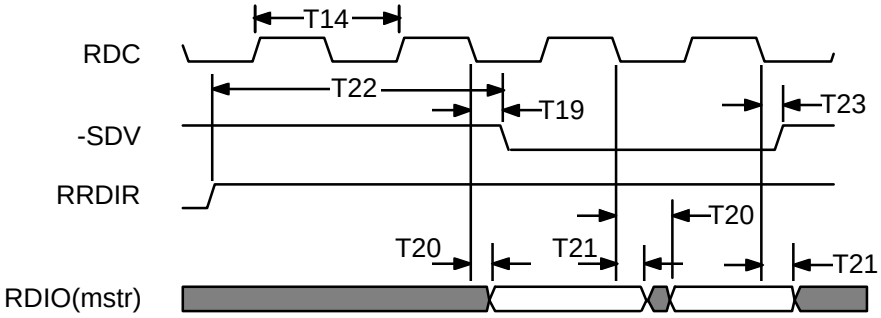
	Description	Min (ns)	Max (ns)
T3	CPU Address hold from -CCS low	60	-
T4	CR-W hold from -CCS high	0	-
T6	CPU Address setup to -CCS low	0	-
T7	CR-W setup to -CCS low	0	-
T8	-CCS high between cycles	100	-
T9	-CCS high to -CRDY high	-	60
T11	-CCS low to -CRDY low	-	180
T12	-CCS low to CPU Data valid	-	70
T13	CPU Data hold from -CRDY low	0	-

5.2.3 MII Slave Timing (DP83856B receiving data on RDIO)



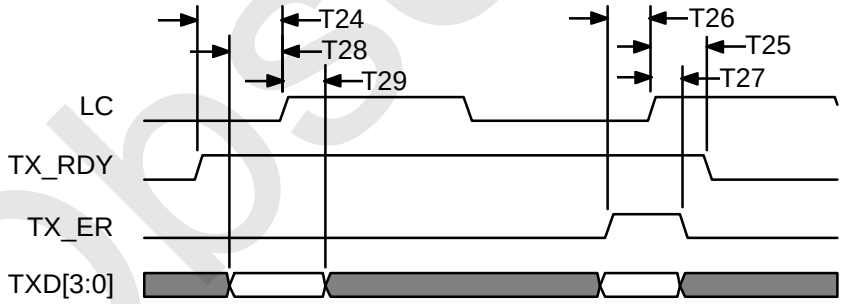
	Description	Min (ns)	Typ (ns)	Max (ns)
T14	RDC pulse width		400	
T15	RDC falling edge to RRDIR	-		60
T16	RDIO setup to RDC rising edge	100		-
T17	RDIO hold from RDC rising edge	0		-
T18	RDC falling edge to -SDV high	-		60

5.2.4 MII Master Timing (DP83856B sending data on RDIO)



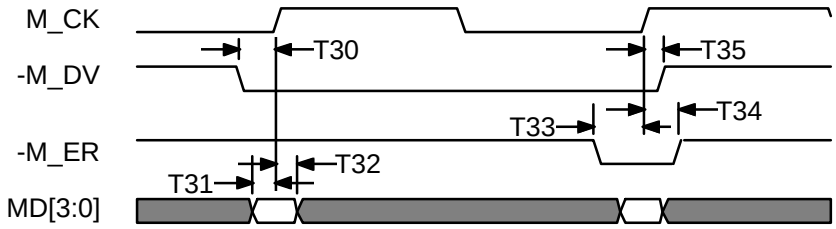
	Description	Min (ns)	Typ (ns)	Max (ns)
T14	RDC pulse width		400	
T19	RDC falling edge to -SDV falling edge	-		60
T20	RDC falling edge to RDIO valid	-		60
T21	RDC falling edge to RDIO invalid	0		-
T22	RRDIR rising edge to -SDV falling edge	600		-
T23	RDC falling edge to -SDV rising edge	-		60

5.2.5 TX Bus Timing



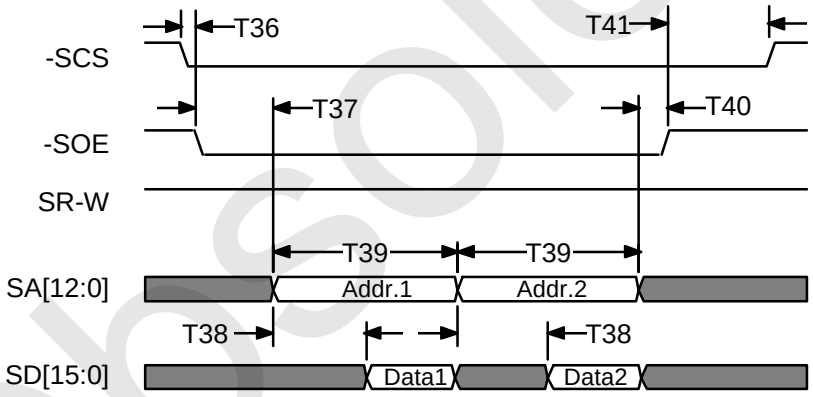
	Description	Min (ns)	Typ (ns)	Max (ns)
T24	TX_RDY setup to LC rising edge	9		-
T25	TX_RDY hold from LC rising edge	3		-
T26	TX_ER setup to LC rising edge	5		-
T27	TX_ER hold from LC rising edge	2		-
T28	TXD[3:0] setup to LC rising edge	6		-
T29	TXD[3:0] hold from LC rising edge	2		-

5.2.6 Management Bus Timing



	Description	Min (ns)	Typ (ns)	Max (ns)
T30	-M_DV setup to M_CK rising edge	3		-
T31	MD[3:0] setup to M_CK rising edge	1		-
T32	MD[3:0] hold from M_CK rising edge	1		-
T33	-M_ER setup to M_CK rising edge	3		-
T34	-M_ER hold from M_CK rising edge	1		-
T35	-M_DV hold from M_CK rising edge	1		-

5.2.7 SRAM Read Timing

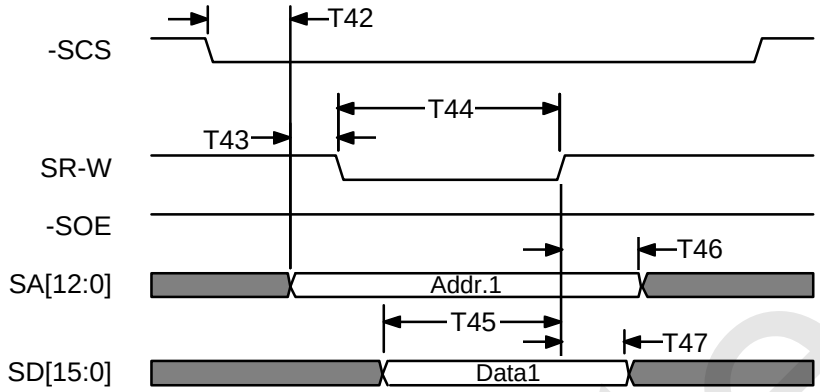


	Description	Min (ns)	Typ (ns)	Max (ns)
T36	-SCS low to -SOE low	0		-
T37 [1]	-SOE low to SA[12:0] valid	-	20	30
T38 [2]	SA[12:0] valid to SD[15:0] valid (SRAM t_{su})	-		25
T39 [3]	SA[12:0] width	50		-
T40 [4]	SA[12:0] invalid to -SOE high	0		-
T41	-SOE high to -SCS high	35		-

Notes:

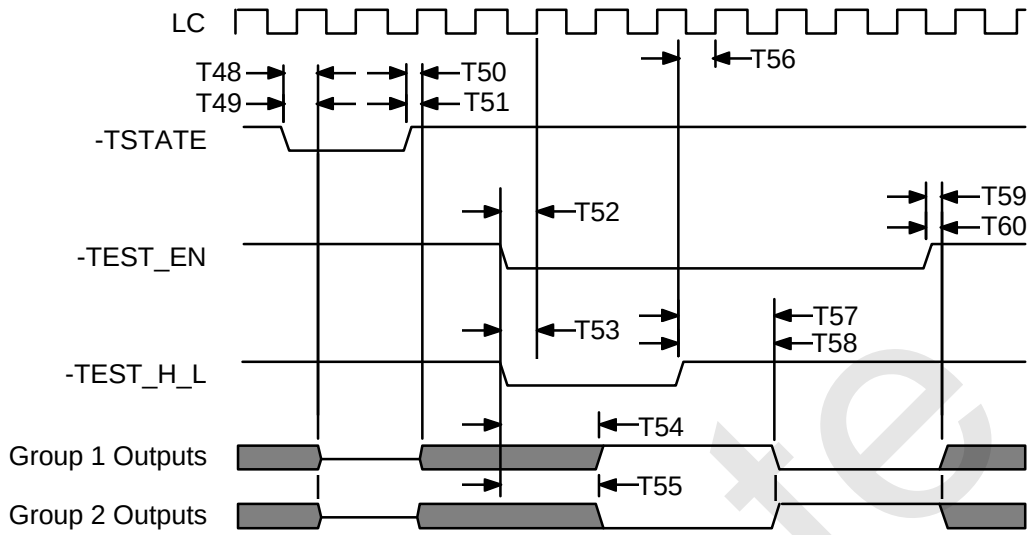
1. All SRAM read cycles are Address controlled.
2. SRAM must have a read access time of 20ns or faster.
3. The DP83856B latches data prior to changing the SA[12:0] value.
4. The DP83856B latches data prior to terminating -SOE.

5.2.8 SRAM Write Timing



	Description	Min (ns)	Typ (ns)	Max (ns)
T42	-SCS low to SA[12:0] valid	30		-
T43	SA[12:0] valid to SR-W low	10		-
T44	SR-W width	35		-
T45	SD[15:0] valid to SR-W high	25		-
T46	SR-W high to SA[12:0] invalid	15		-
T47	SR-W high to SD[15:0] invalid	15		-

5.2.9 Test Mode Timing



	Description	Min (ns)	Typ (ns)	Max (ns)
T48	-TSTATE low to Group 1 Outputs Hi-Z	-		25
T49	-TSTATE low to Group 2 Outputs Hi-Z	-		25
T50	-TSTATE high to Group 1 Outputs driven	-		25
T51	-TSTATE high to Group 2 Outputs driven	-		25
T52	-TEST_EN low setup to LC rising edge	20		-
T53	-TEST_H_L low setup to LC rising edge	20		-
T54	-TEST_EN, -TEST_H_L low to Group 1 Outputs high	-		2 * LC + 0ns
T55	-TEST_EN, -TEST_H_L low to Group 2 Outputs low	-		2 * LC + 0ns
T56	-TEST_H_L high setup to LC rising edge	20		-
T57	-TEST_EN low, -TEST_H_L high to Group 1 Outputs low	-		2 * LC + 0ns
T58	-TEST_EN low, -TEST_H_L high to Group 2 Outputs high	-		2 * LC + 0ns
T59	-TEST_EN high to Group 1 Outputs undefined	-		2 * LC + 0ns
T60	-TEST_EN high to Group 2 Outputs undefined	-		2 * LC + 0ns

Group 1 output pin numbers are:
21, 23, 27, 31, 35, 37, 39, 43, 61, 64, 68, 70, 72, 74, 78, 80, 82, 87, 89, 90, 92, 96, 98, 100, 104, 108, 113, 115.

Group 2 output pin numbers are:
20, 22, 24, 30, 34, 36, 38, 42, 44, 65, 69, 71, 73, 75, 79, 81, 83, 88, 91, 93, 97, 99, 103, 105, 114, 116.

6.0 System Considerations

The following section provides descriptions of issues that should be considered during the design of a DP83856B based system. Please contact your National Semiconductor representative for any questions or concerns regarding these issues.

6.1 Lost MII Read Error Status Events

If users have configured the DP83856B Interrupt Register (02h) to enable MII_RD_ERR_STS, and are polling the Interrupt Register after starting an MII register access for this bit to go valid, then it is possible for the event to come in and be cleared prior to the CPU seeing the event. In other words, the clear function can beat the set function, with the result being a lost event.

Users often want to check this status bit when an MII register access has completed to ensure the addressed device has responded and the data returned is valid.

The solution to this issue is simple, and adds MINIMAL overhead and complexity to the software implementation. Instead of polling the MII_RD_ERR_STS bit in the Interrupt register (02h), poll the MII_ACC bit (bit D0) in the Configuration Register (00h) for MII access completion. MII_ACC will be a 0 when the MII access is complete. Once the MII access is complete, then the Interrupt Register can be read to obtain the status of the MII_RD_ERR_STS bit.

The only overhead involved is performing one extra read to the Interrupt Register after the polling cycle is complete. MII accesses take on the order of 12.8 us per access, and this workaround only adds one more ~300 ns read to complete the operation: not a large overhead.

6.2 Sixty-Three Byte Packet Counting

Any packet received on a repeater port that is managed by the DP83856B, which has a frame length of 142 or 143 nibbles (63 bytes + 8 bytes of preamble/sfd) will not be logged as a Runt packet.

IEEE 802.3 clause 30 states: "Increment counter by one for each CarrierEvent that meets one of the following two conditions. Only one test need be made. (1) The Activity Duration is greater than ShortEventMaxTime and less than ValidPacketMinTime and the CollisionEvent signal is deasserted (10 Mb operation) or the Collision Count Increment state of the partition state diagram (figure 27-8) has not been entered (100 Mb operation). (2) The OctetCount is less than 64, the ActivityDuration is greater than ShortEventMaxTime and the CollisionEvent signal is deasserted (10 Mb operation) or the Collision Count Increment state of the partition state diagram (figure 27-8) has not been entered (100 Mb operation). ValidPacketMinTime is greater than or equal to 552 bit times and less than 565 bit times. ..."

The DP83856B uses definition (1) by setting the upper limit on runts to 564 bits or 141 nibbles. Therefore if the packet activity is greater than 141 nibbles, the DP83856B does not log the activity as a runt. This opens a window for events which are not logged either as a runt or a good/fcs frame. Including 8 octets of preamble/sfd, a minimum size good packet is 72 bytes (8 + 64), or 144 nibbles. Thus, if the frame length is 142 or 143 nibbles (63 bytes + 8 bytes of preamble/SFD), the packet will not be logged.

6.3 Initial Packet Logging

When activity occurs while the DP83856B is not in management mode, certain counters and flags are activated. When the device is placed into management mode they are not reset. This potentially causes the first packet received to be flagged as a collision or other sort of error condition even though it may have been a valid packet.

The anomaly occurs most frequently at power up. At power up, the device has not yet been placed in management mode and activity (noise) is present on the network. This causes the counters and/or flags to be set.

The anomaly can also occur if the device is run through the following sequence of events:

1. The device is removed from management mode,

2. A collision packet is received,

3. The device is placed back into management mode

4. Finally, a valid packet is received. The counters will log all subsequent packets correctly but not this initial valid packet.

There is no workaround for the case of power up. While this anomaly may cause the count of valid packets received to by off by 1, most networks have orders of magnitude more packet activity such that this is of no consequence.

For other cases, ensure that there is no network activity while the device is not in management mode. This is generally of little consequence as well, because most systems are expected to keep the device either in or out of management mode for extended network activity periods and not toggle modes frequently with respect to packet activity.

6.4 Random Activity On Management Interface

When a twisted-pair cable is removed from a port, the DP83850 (100RIC) may assert -M_DV without TX_RDY and send activity on M_CK. Under these conditions, when the next packet is received, even if it is a valid packet, an inappropriate device ID may be latched from Management Data (MD[3:0]). Depending on the actual device ID latched, the DP83856B may either not log the packet in the correct location or may not log the packet at all.

To avoid the possibility of not counting a packet after random invalid management bus activity, use external logic to ensure that -M_DV is asserted only when TX_RDY is also asserted.

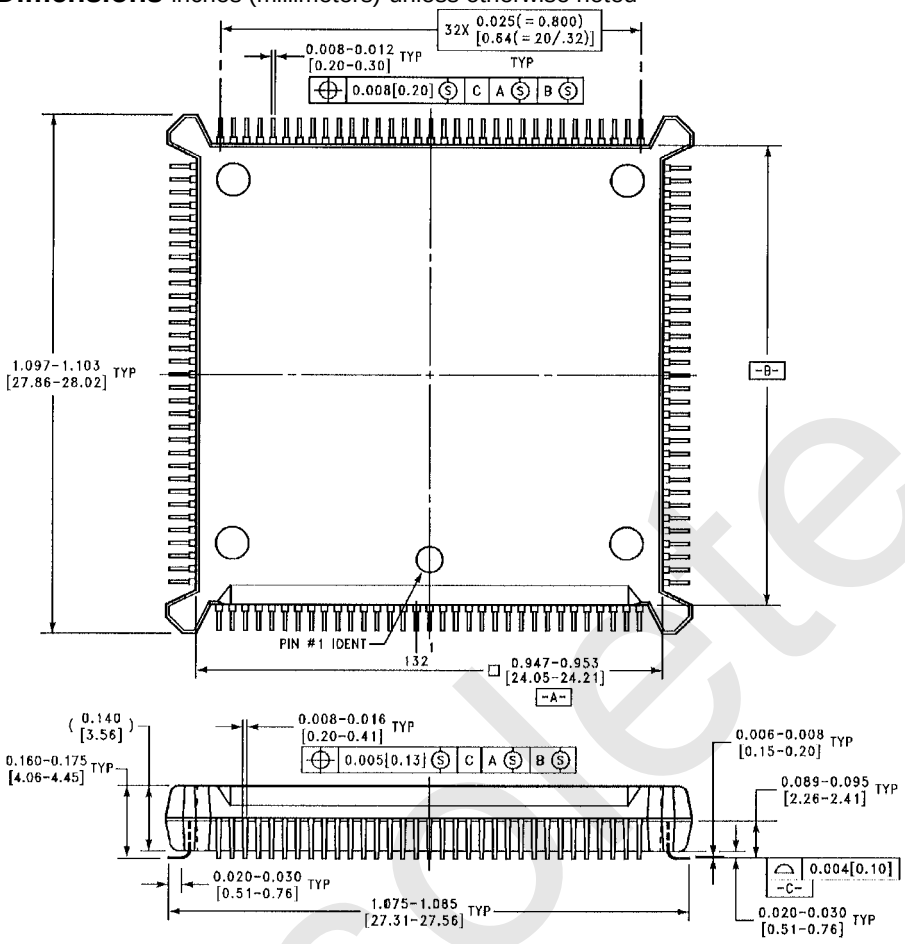
6.5 Symbol Error During Packet Count

IEEE 802.3u Clause 30.4.3.1.17 defines SymbolErrorDuringPacket as “a count of the number of times when a valid length packet was received at the port and there was at least one occurrence of an invalid data symbol...”.

The DP83856B’s Invalid Symbol Count increments for valid size and oversize packets which contain at least one occurrence of an invalid data symbol.

There is no workaround required. The DP83856B’s implementation is actually more robust because it will flag symbol errors contained in FrameTooLong packets and Jabber packets as well as valid length packets.

7.0 Physical Dimensions inches (millimeters) unless otherwise noted



132-Lead Molded Plastic Quad Flat Package, JEDEC
Order Number DP83856BVF
NS Package Number VF132A

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