MiDAS Family

BM-MiDAS1.0-V2.1

BM

Brief Manual of MiDAS1.0 Family

EPROM / ROM / ROMless based
8-bit Turbo Microcontrollers

V2.1

May 2007

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Contents

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1. Product Overview

- CORERIVER's MiDAS1.0 Family is a group of fast 80C52 compatible microcontrollers.
- The instruction execution of MiDAS1.0 Family is max. 3 times faster than that of traditional 80C52.
  - ✓ 1 machine cycle = 4 clocks vs. 12 clocks
- Additional peripherals of MiDAS1.0 Family:
  - ✓ 9bit ADC / 8bit PWM / WDT / LVD / POR.
- Power saving modes
- Noise tolerant scheme
- Provides User-Friendly MDS environment
- Provides Easy-to-Use training-kit system

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1. Product Overview (Cont'd)

A. MiDAS1.0 Family - GC80C520G Series (General MCU)

Product	Mask-ROM (byte)	EPROM (byte)	RAM (Byte)	Volt (V)	Freq. (MHz)	T/C (16bits)	Serial I/O	WDT	ADC (bit x ch)	PWM (bit x ch)	I/O Pins	Package	Others	Available Time
GC87C520G0-PL44I GC87C520G0-LQ44I GC87C520G0-P40I GC87C520G0-SP28I GC87C520G0-SO28I	-	8K	256	2.7~5.5	40 (20)	3	1 UART	YES	-	-	36 36 32 22 22	44-PLCC 44-MQFP 40-PDIP 28-SPDIP 28-SOIC	LVD POR	**Now** **Now** **Now** **Now** **Now**
GC81C520G0-PL44I GC81C520G0-LQ44I GC81C520G0-P40I GC81C520G0-SP28I GC81C520G0-SO28I	8K	-	256	2.7~5.5	40 (20)	3	1 UART	YES	-	-	36 36 32 22 22	44-PLCC 44-MQFP 40-PDIP 28-SPDIP 28-SOIC	LVD POR	**Now** **Now** **Now** **Now** **Now**
GC80C320G0-PL44I GC80C320G0-LQ44I GC80C320G0-P40I	ROMless		256	2.7~5.5	40 (20)	3	1 UART	YES	-	-	36 36 32	44-PLCC 44-MQFP 40-PDIP	LVD POR	**Now** **Now** **Now**

* Operating frequency of MiDAS family is 40 MHz at 5.0 voltage.

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1. Product Overview (Cont'd)

B. MiDAS1.0 Family - GC80C520A Series (ADC Application MCU)

Product	Mask-ROM (byte)	EPROM (byte)	RAM (Byte)	Volt (V)	Freq. (MHz)	T/C (16bits)	Serial I/O	WDT	ADC (bit x ch)	PWM (bit x ch)	I/O Pins	Package	Others	Available Time
GC87C520A0-PL44I GC87C520A0-LQ44I GC87C520A0-P40I GC87C520A0-SP28I GC87C520A0-SO28I	-	8K	256	2.7~5.5	40 (20)	3	1 UART	YES	9x4	8x2	36 36 32 22 22	44-PLCC 44-MQFP 40-PDIP 28-SPDIP 28-SOIC	LVD POR	**Now** **Now** **Now** **Now** **Now**
GC81C520A0-PL44I GC81C520A0-LQ44I GC81C520A0-P40I GC81C520A0-SP28I GC81C520A0-SO28I	8K	-	256	2.7~5.5	40 (20)	3	1 UART	YES	9x4	8x2	36 36 32 22 22	44-PLCC 44-MQFP 40-PDIP 28-SPDIP 28-SOIC	LVD POR	**Now** **Now** **Now** **Now** **Now**
GC80C320A0-PL44I GC80C320A0-LQ44I GC80C320A0-P40I	ROMless		256	2.7~5.5	40 (20)	3	1 UART	YES	9x4	8x2	36 36 32	44-PLCC 44-MQFP 40-PDIP	LVD POR	**Now** **Now** **Now**

* Operating frequency of MiDAS1.0 family is 40 MHz at 5.0 voltage.

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2. Features

- CPU
  - ✓ 8-bit turbo 80C52 architecture
  - ✓ 4 cycles/1 machine cycle
  - ✓ Pin/instruction level compatible with Intel 80C52
- 0/8Kbytes of on-chip ROM
- 256bytes of on-chip RAM
- Supply voltage: 2.7V ~ 5.5V
- Operating Frequency
  - ✓ Max. 40MHz @4.5V ~ 5.5V
  - ✓ Max. 20MHz @2.7V ~ 3.3V
- Temperature Range: -20 °C to 85 °C
- Max. Programmable 36 IO pins
  - ✓ Intel 8052 compatible as default
  - ✓ Optional Input/Output control
  - ✓ TTL input level and CMOS compatible logic levels
- EMI reduction mode : Inhibit ALE
- Low Voltage Detector
- 27-bit Programmable Watchdog Timer
- Three 16-bit Timer/Counters
- Full-Duplex Programmable UART
  - ✓ Automatic address recognition
- 2-channel 8-bit high speed PWM
- 4-channel 9-bit ADC
  - ✓ Max 100K sample per second (@8 MHz)
  - ✓ Programmable input clock frequency
- 13 interrupt sources (with 6 external sources)
  - ✓ Timer0/1/2, UART, ADC, WDT, LVD, and 6 External
  - ✓ Four-level interrupt priority & NMI
- Reset scheme
  - ✓ On-chip Power-On-Reset(POR)
  - ✓ External reset
  - ✓ Low voltage detector reset
  - ✓ Watchdog timer reset
- Power consumption
  - ✓ Active current : Max 20mA @5V, 40MHz
  - ✓ Stop current : Max 1uA
- ESD protection up to 2,000V
- Latch-up protection up to ±200mA
- Package :
  - ✓ 44-PLCC, 44-MQFP,40-PDIP, and 28-SPDIP/SOIC

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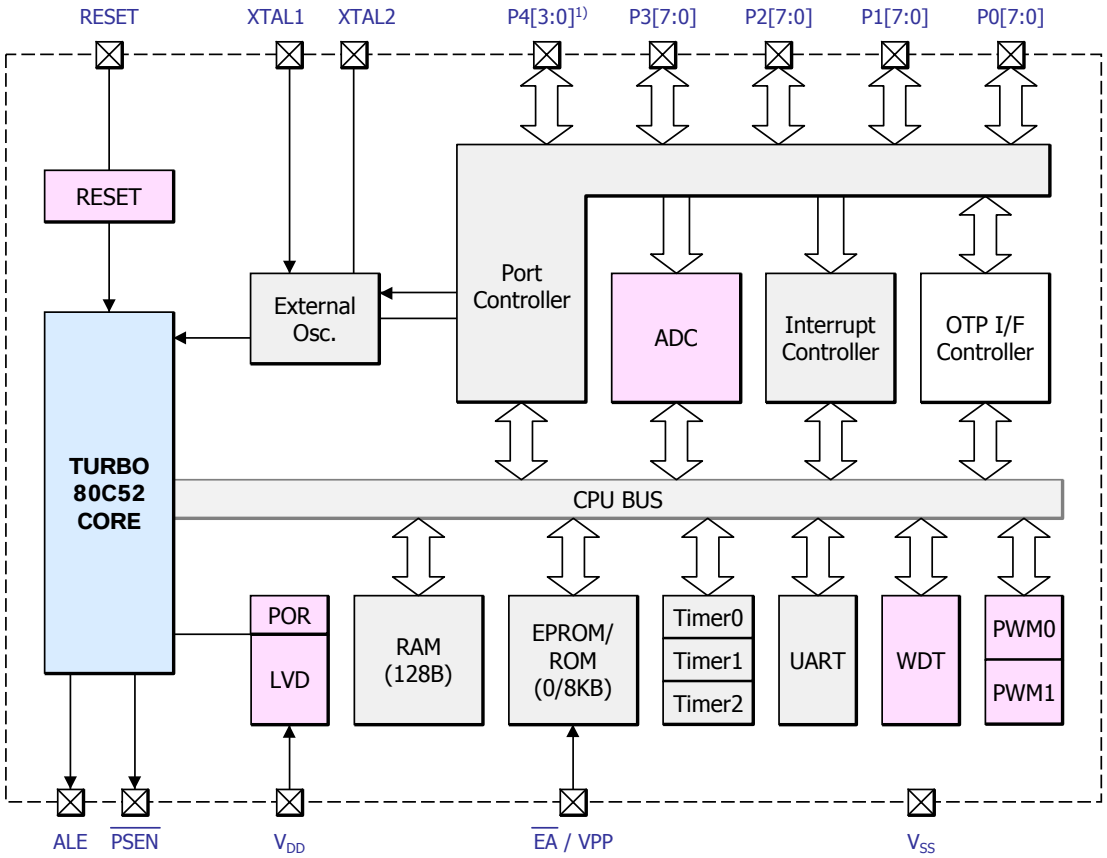
3. Block Diagram



1) P4[3:0] are only available for 44-PLCC and 44-LQFP type Package.

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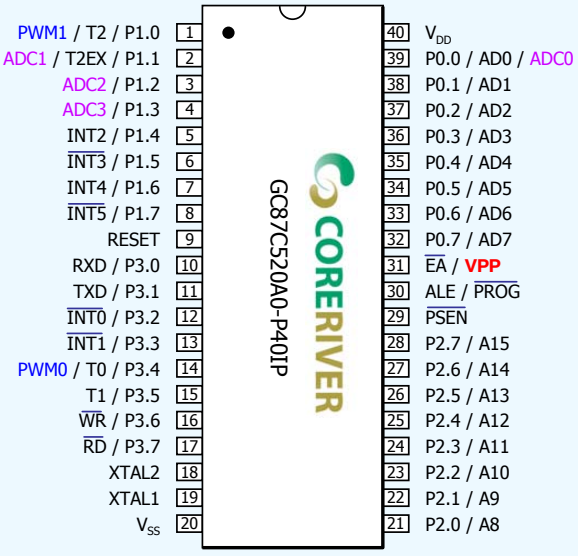
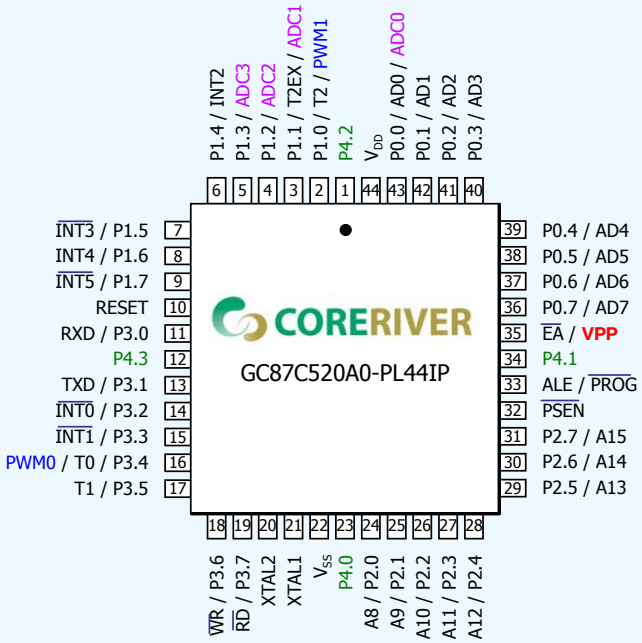
4. Pin Configurations



[40-PDIP]



[44-PLCC]

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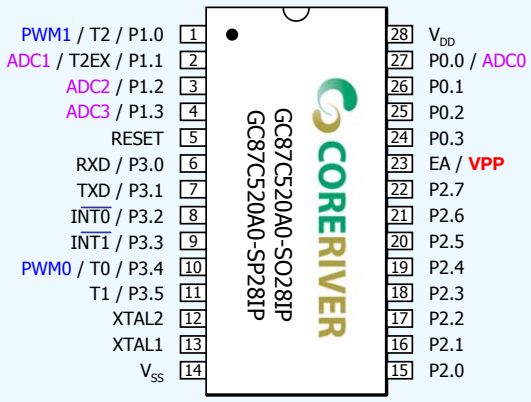
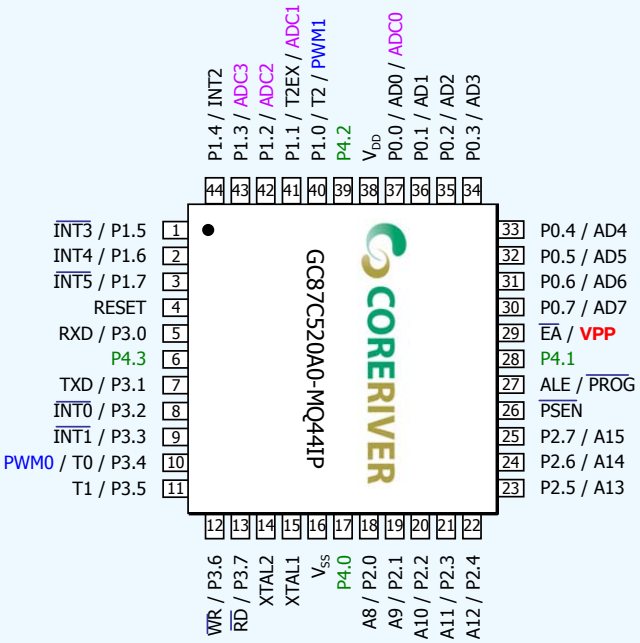
4. Pin Configurations (Cont'd)



[28-SPDIP/SOIC]



[44-MQFP]

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5. Pin Descriptions

Symbol	Direction	Description	Share Pins
V_{DD}	Input	Power Supply	-
V_{SS}	Input	Ground	-
RESET	Input	External Reset	-
XTAL1	Input	Input to the inverting oscillator amplifier	-
XTAL2	Output	Output from the inverting oscillator amplifier	-
$\overline{EA}$	Input	External Access Enable (0 → fetched from external ROM, 1 → from internal ROM) This pin must not be floating.	VPP
$\overline{ALE}$	Input/Output	Address Latch Enable	$\overline{PROG}$
PSEN	Input/Output	Program Store Enable (Enables external program memory to the bus)	-
P0[7:0]	Input/Output	Programmable I/O Port: Schmitt Trigger Input or Push-pull/Open-Drain Output. Pull-up Resistor can be switched on/off by Software.	P0.0 / AD0 / ADC0 P0.1~P0.7 / AD1~7
P1[7:0]	Input/Output	Programmable I/O Port: Schmitt Trigger Input or Push-pull Output. Pull-up Resistor can be switched on/off by Software.	P1.0 / T2 / PWM1 P1.1 / T2EX / ADC1 P1.2~P1.3 / ADC2~ADC3 P1.4~P1.7 / INT2~INT5
P2[0:7]	Input/Output	Programmable I/O Port: Schmitt Trigger Input or Push-pull Output Pull-up Resistor can be switched on/off by Software.	P2.0~P2.7 / A8~A15
P3[7:0]	Input/Output	Programmable I/O Port: Schmitt Trigger Input or Push-pull Output. Pull-up Resistor can be switched on/off by Software.	P3.0 / RXD P3.1 / TXD P3.2~P3.3 / INT0~INT1 P3.4 / T0 / PWM0 P3.5 / T1 P3.6 / WR P3.7 / RD
P4[3:0]	Input/Output	Programmable I/O Port: Schmitt Trigger Input or Push-pull Output. Pull-up Resistor can be switched on/off by Software.	-

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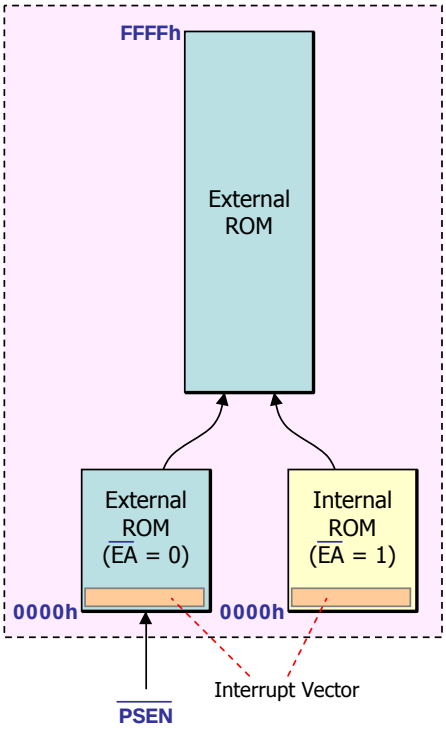
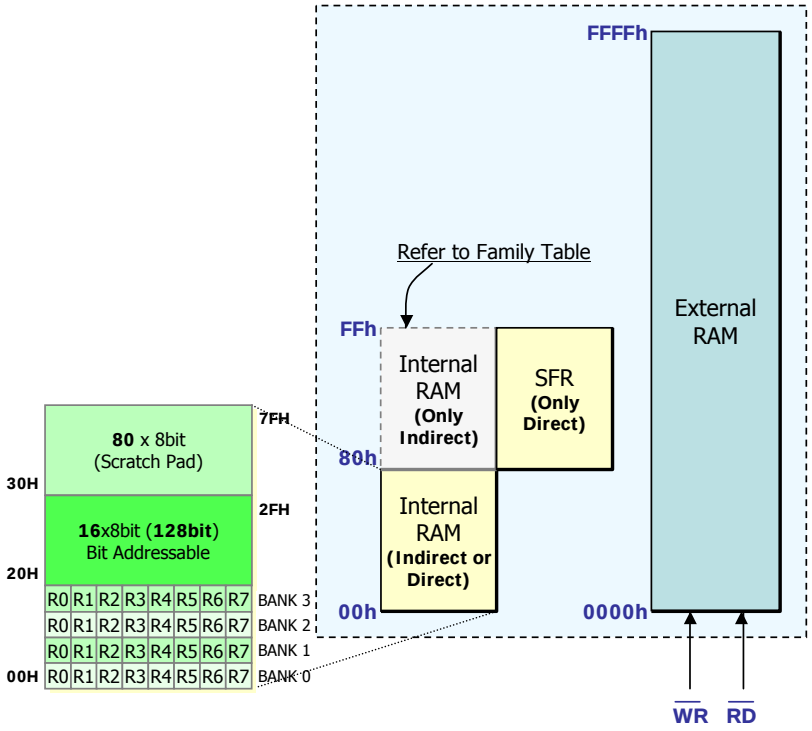
6.1. Memory Organization



[Program Memory]
(Read Only)



[Data Memory]
(Read and Write)

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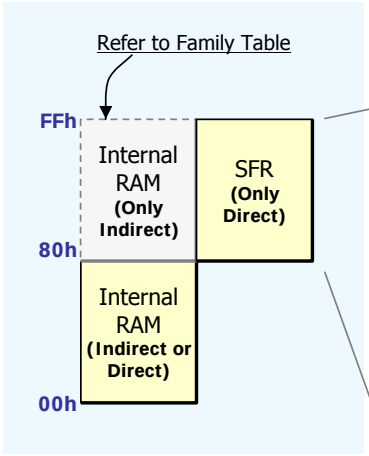
6.2. SFR (Special Function Register) Map



: Newly added SFR at MiDAS1.0 Family

: Reserved for future use.

Bit addressable

F8h	**EIP**								FFh
F0h	B								F7h
E8h	**EIE**						**ADCR**	**ADCON**	EFh
E0h	ACC		**ADCSEL**	**ALTSEL**	**P0SEL**	**P1SEL**	**P2SEL**	**P3SEL**	E7h
D8h	**WDCON**				**PWM0CON**	**PWM1CON**	**PWM0D**	**PWM1D**	DFh
D0h	PSW								D7h
C8h	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			CFh
C0h					**PMR**	**STATUS**			C7h
B8h	IP	SADEN							BFh
B0h	P3							IPH	B7h
A8h	IE	SADDR							AFh
A0h	P2					**P4**	**P4SEL**		A7h
98h	SCON	SBUF							9Fh
90h	P1	**EXIF**							97h
88h	TCON	TMOD	TL0	TL1	TH0	TH1	**CKCON**		8Fh
80h	P0	SP	DPL	DPH				PCON	87h

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6.2. SFR Brief Description

- 80C52 SFR Registers

Register	Name	Reset Value
ACC	Accumulator	00000000
B	B Register	00000000
PSW	Program Status Word	00000000
SP	Stack Pointer	00000111
DPTR	Data Pointer (2 bytes)	
DPL	Low byte	00000000
DPH	High byte	00000000
P0	Port 0	11111111
P1	Port 1	11111111
P2	Port 2	11111111
P3	Port 3	11111111
IP	Interrupt Priority Low	10000000
IPH	Interrupt Priority High	10000000
IE	Interrupt Enable Control	00000000
TCON	T/C 0/1 Control	00000000
TMOD	T/C 0/1 Mode Control	00000000
T2CON	T/C 2 Control	00000000
T2MOD	T/C 2 Mode Selection	******00
TH0	T/C 0 High byte	00000000
TL0	T/C 0 Low byte	00000000
TH1	T/C 1 High byte	00000000
TL1	T/C 1 Low byte	00000000
TH2	T/C 2 High byte	00000000
TL2	T/C 2 Low byte	00000000
RCAP2H	T/C 2 Capture Reg. High byte	00000000
RCAP2L	T/C 2 Capture Reg. Low byte	00000000
SCON	Serial Control	00000000
SBUF	Serial Buffer	00000000
SADEN	Slave Address Mask Enable	00000000
SADDR	Slave Address	00000000
PCON	Power Control	00*10000

- Newly added SFR Registers in MiDAS1.0 Family

Register	Name	Reset Value
P0SEL	Port 0 Pull-up Control	11111111
P1SEL	Port 1 Pull-up Control	00000000
P2SEL	Port 2 Pull-up Control	00000000
P3SEL	Port 3 Pull-up Control	00000000
P4SEL	Port 4 Pull-up Control	****0000
P4	Port 4. Only Available for 44PLCC	****1111
ALTSEL	Alternative Function Selection only for 8/10/20 DIP/SOP Package Type Don't use in 40DIP/44PLCC Package Type.	**000000
PWM0CON	PWM 0 Control	00000000
PWM1CON	PWM 1 Control	00000000
PWM0D	PWM 0 Duty Data	00000000
PWM1D	PWM 1 Duty Data	00000000
ADCON	ADC Control & ADC Result LSB	001000*0
ADCR	ADC Result Value Including MSB bit	00000000
ADCSEL	ADC Channel Selection and ADC Input Clock Divide Control	000*0000
WDCON	Power Flag and Watchdog Timer Control	*1010000
CKCON	Watchdog Timer and 4-cycle Switching Control	00000***
PMR	Power Management Control	*****0**
EXIF	Added External Interrupt and LVD Control	00001**1
EIP	Extended Interrupt Priority	*0000000
EIE	Extended Interrupt Enable	*0000000
STATUS	Crystal Status	***0****

CAUTION : Don't touch bit *. Updating these bits will cause the malfunctions.

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6.3. Instruction Set Summary

- Refer to Appendix A (Instruction Set) for more details.

Type	Instruction	Description
Arithmetic	**ADD**	Addition
	ADDC	Addition with Carry
	SUBB	Subtraction with Borrow
	INC	Increment
	DEC	Decrement
	MUL	Multiply
	DIV	Divide
	DA	Decimal Adjust
Logical	**ANL**	AND
	ORL	OR
	XRL	Exclusive OR
	CLR	Clear
	CPL	Complement
	RL	Rotate Left
	RLC	Rotate Left with Carry
	RR	Rotate Right
	RRC	Rotate Right with Carry
	SWAP	Swap Nibbles
Data Transfer	**MOV**	Move Data
	MOVC	Move Code
	MOVX	Move Data to Ext. RAM
	PUSH	PUSH
	POP	POP
	XCH	Exchange
	XCHD	Exchange Low-digit

Type	Instruction	Description
Boolean	**CLR**	Clear bit
	SETB	Set bit
	CPL	Complement bit
	ANL	AND bit
	ORL	OR bit
	MOV	Move bit
	JC	Jump if Carry is set
	JNC	Jump if Carry is not set
	JB	Jump if bit is set
	JNB	Jump if bit is not set
	JBC	Jump if bit is set & clear
Branch	**ACALL**	Absolute Call
	LCALL	Long Call
	RET	Return from Subroutine
	RETI	Return from Interrupt
	AJMP	Absolute Jump
	LJMP	Long Jump
	SJMP	Short Jump
	JMP	Jump with DPTR
	JZ	Jump if ACC is zero
	JNZ	Jump if ACC is not zero
	CJNE	Compare and Jump if not equal
	DJNZ	Decrement and Jump if not zero
	NOP	No Operation

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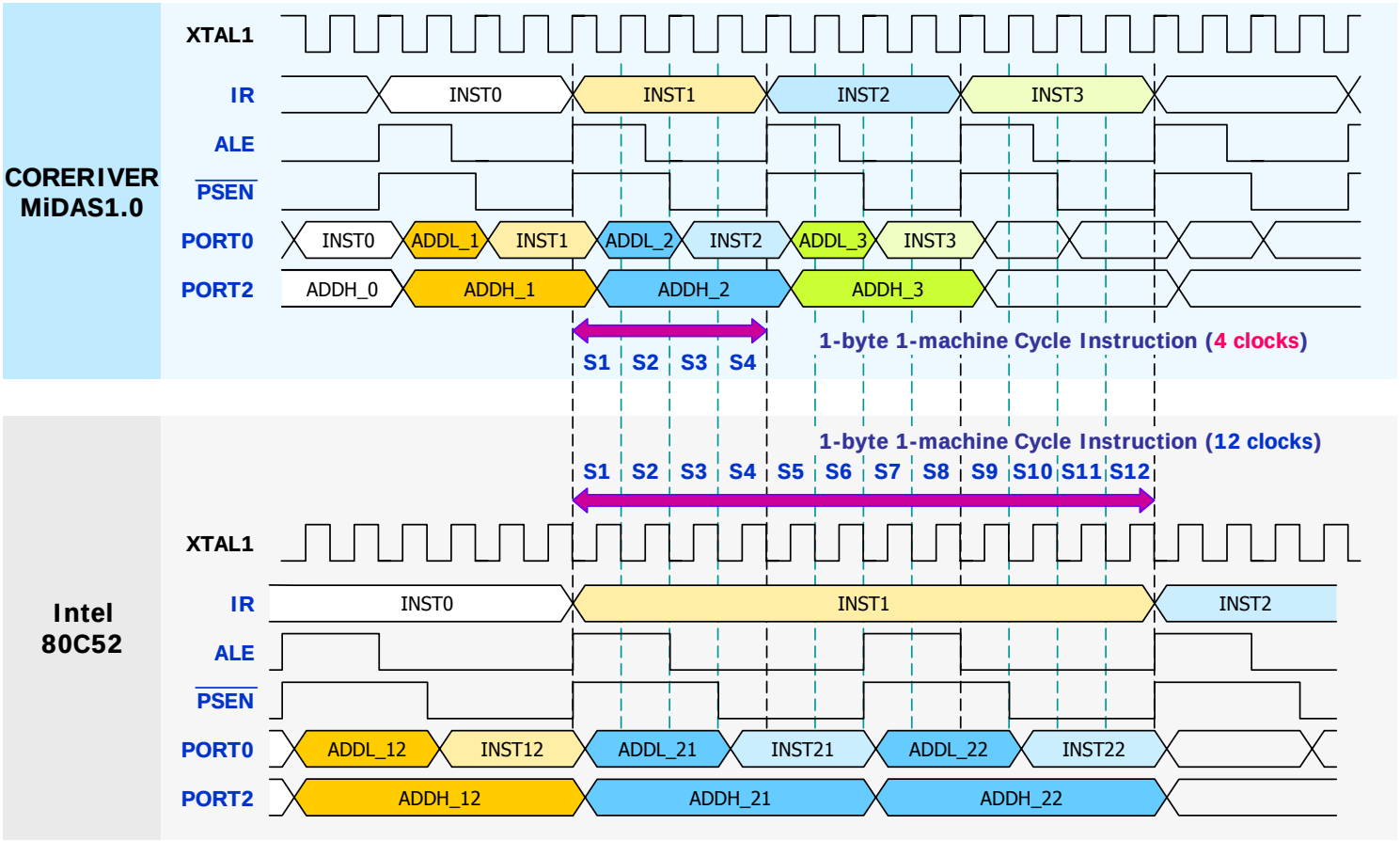
6.4. CPU Timing

- Instruction timing comparison of the MiDAS1.0 family and Intel 80C52



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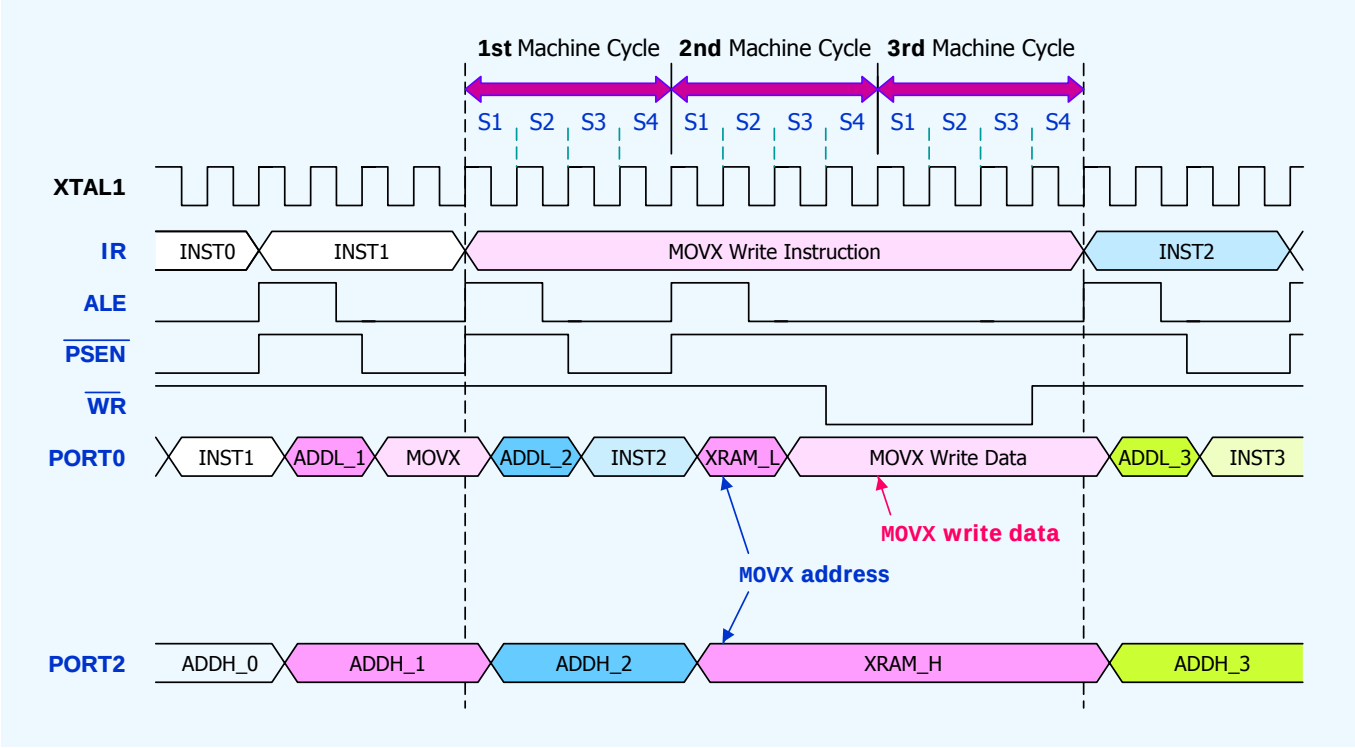
6.4. CPU Timing : MOVX Write



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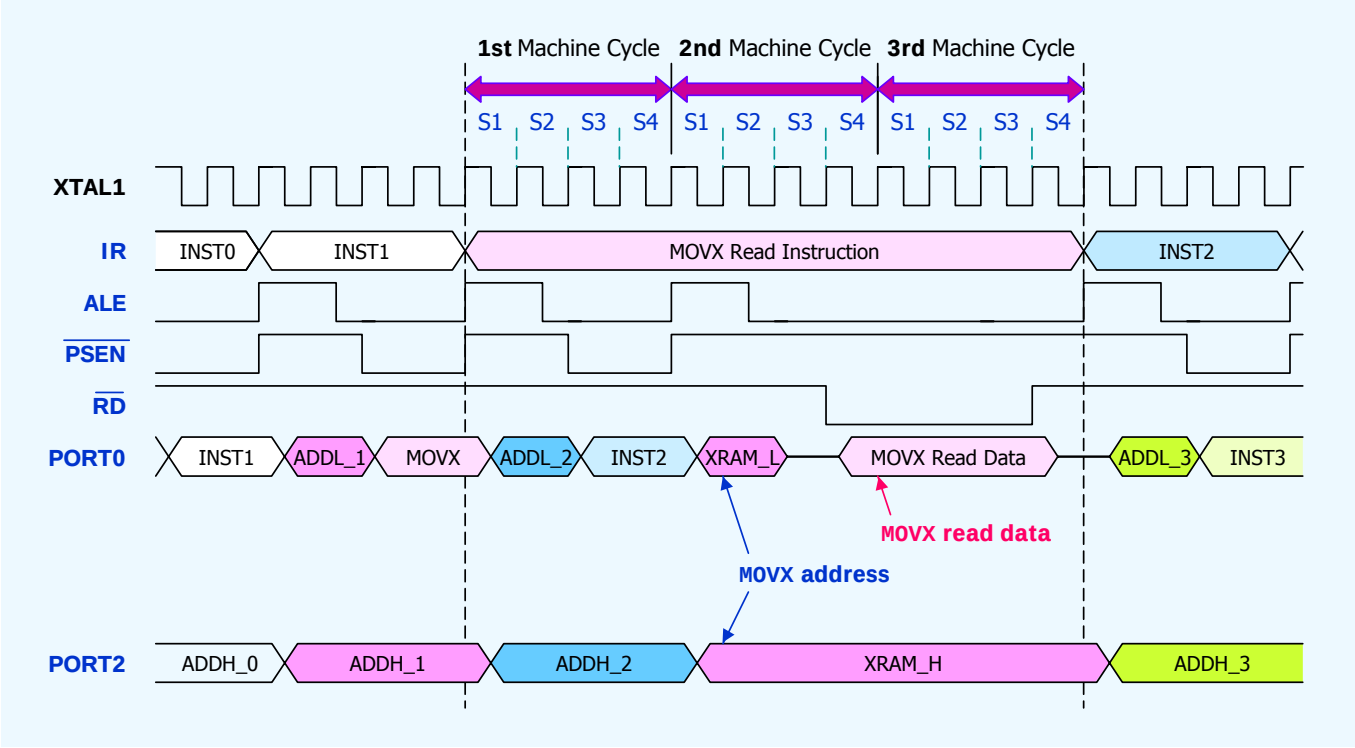
6.4. CPU Timing : MOVX Reading



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6.4. CPU Timing : Comparison Table

- The Fastest CPU timing in the world

Instruction	**MiDAS1.0 (CORERIVER)**	W77C32 (Winbond)	DS80C320 (Maxim)	87C52 (Intel)
`MUL AB` `DIV AB`	**12 clocks**	20 clocks	20 clocks	48 clocks
`MOVC A, @A+PC` `MOVC A, @A+DPTR`	**8 clocks**	8 clocks	12 clocks	24 clocks
`JMP @A+DPTR`	**8 clocks**	8 clocks	12 clocks	24 clocks
`RET` `RETI`	**8 clocks**	8 clocks	16 clocks	24 clocks
`INC DPTR` `DEC DPTR`	**4 clocks** **4 clocks**	8 clocks 8 clocks	12 clocks Not exist	24 clocks Not exist
`Others`	**Same**	Same	Same	-

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6.5. I/O Ports : PORT0[7:0]

- Open-Drain output at default condition (Intel 8052 compatible).
- Only the P0.0 pin is available for analog input (ADC input channel 0).
- During accesses to external memory, the P0 SFR will be automatically set to "FFh".
- Internal pull-up resistors are switched on/off by changing the value of the P0SEL SFR.
  If the Port is used as ADC Function, ADC_EN Bit must be Set. Then Internal pull-up become off.
- Read-Modify-Write instructions do not read port pin but the port SFR.
  - ✓ ANL / ORL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y

- PORT0 Description

✓ **ADCSEL** (E2h) : ADC Input Select Register

ADIV2	ADIV1	ADIV0	-	ADC3	ADC2	ADC1	ADC0
R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ADC0 : 1 = ADC0 input enable & digital input disable at P0.0.

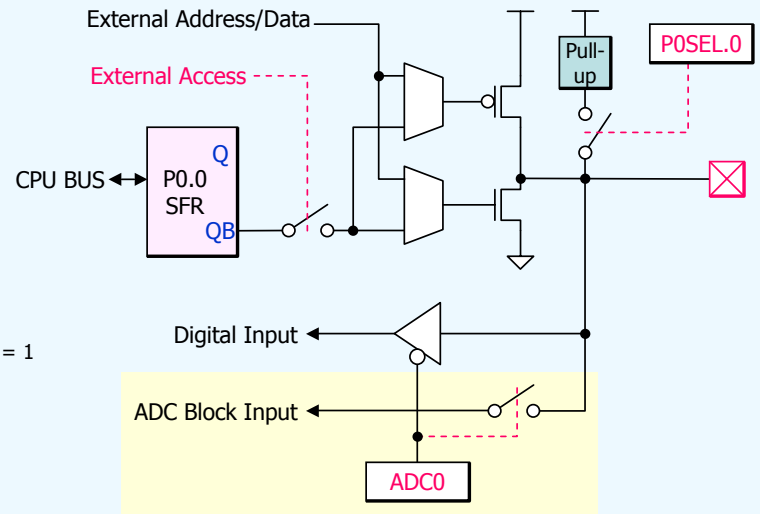
✓ **P0SEL** (E4h) : P0 Pull-up Control Register

P0SEL.7	P0SEL.6	P0SEL.5	P0SEL.4	P0SEL.3	P0SEL.2	P0SEL.1	P0SEL.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- P0SEL[7:0] : Pull-up resistor enable
  0 = Pull-up resistor ON
  1 = Pull-up resistor Off when ADC_EN(ADNCON[7]) = 1
  PORT0 Pull-up resistor is **OFF** after reset.

✓ **P0** (80h) : PORT0 Register

P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



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6.5. I/O Ports : PORT1[7:0]

- Quasi bi-directional port (Intel 8052 Compatible).
- The P1.1 / P1.2 / P1.3 pins are available for analog input (ADC input channel 1/2/3).
- Pull-up resistors are switched on/off by changing the value of the P1SEL SFR.
  If the Port is used as ADC Function, ADC_EN Bit must be Set. Then Internal pull-up become off.
- The alternative functions are available only when the corresponding SFR bit is "1".
  - ✓ P1.0 = T2, PWM1 / P1.1 = T2EX, ADC1 / P1.2 = ADC2 / P1.3 = ADC3 / P1.4 = INT2 / P1.5 = $\overline{\text{INT3}}$ / P1.6 = INT4 / P1.7 = $\overline{\text{INT5}}$
- Read-Modify-Write instructions do not read port pin but the port SFR.
  - ✓ ANL / ORL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y
- PORT1 Description

✓ **ADCSEL** (E2h) : ADC Input Select Register

ADIV2	ADIV1	ADIV0	-	ADC3	ADC2	ADC1	ADC0
R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ADC1 : 1 = ADC1 input enable & digital input disable at P1.1.
- ADC2 : 1 = ADC2 input enable & digital input disable at P1.2.
- ADC3 : 1 = ADC3 input enable & digital input disable at P1.3.

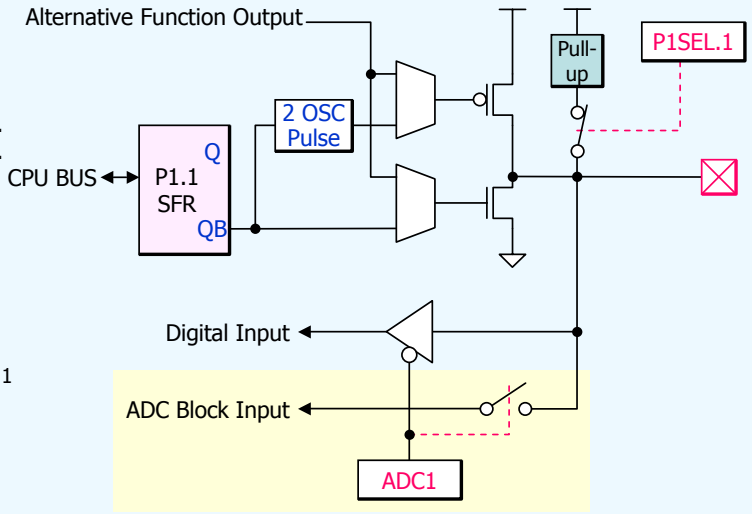
✓ **P1SEL** (E5h) : P1 Pull-up Control Register

P1SEL.7	P1SEL.6	P1SEL.5	P1SEL.4	P1SEL.3	P1SEL.2	P1SEL.1	P1SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- P1SEL[7:0] : Pull-up resistor Enable
  0 = Pull-up resistor ON
  1 = Pull-up resistor Off when ADC_EN(ADCON[7]) = 1
  PORT1 Pull-up resistor is **ON** after reset.

✓ **P1** (90h) : PORT1 Register

P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



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6.5. I/O Ports : PORT2[7:0]

- Quasi bi-directional port (Intel 8052 Compatible).
- Pull-up resistors are switched on/off by changing the value of the P2SEL SFR.
- Read-Modify-Write instructions do not read port pin but the port SFR.
  - ✓ ANL / ORL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y

- PORT2 Description

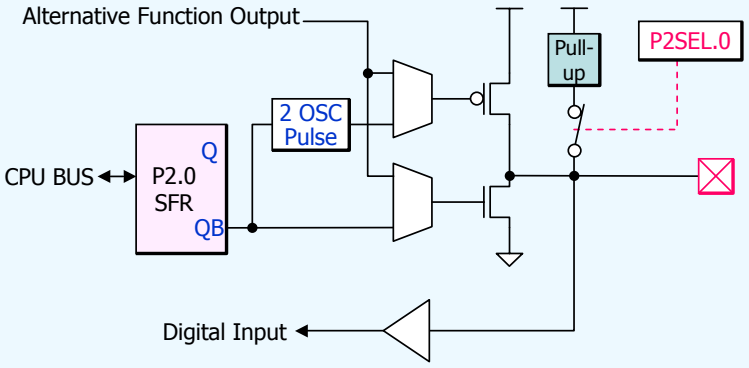
✓ **P2SEL** (E6h) : P2 Pull-up Control Register

P2SEL.7	P2SEL.6	P2SEL.5	P2SEL.4	P2SEL.3	P2SEL.2	P2SEL.1	P2SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- P2SEL[7:0] : Pull-up resistor Enable
  0 = Pull-up resistor ON / 1 = Pull-up resistor Off
  PORT2 Pull-up resistor is **ON** after reset.

✓ **P2** (A0h) : PORT2 Register

P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



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6.5. I/O Ports : PORT3[7:0]

- Quasi bi-directional port (Intel 8052 Compatible).
- Pull-up resistors are switched on/off by changing the value of the P3SEL SFR.
- The alternative functions are available only when the corresponding SFR bit is "1"
  - ✓ P3.0 = RXD / P3.1 = TXD / P3.2 = $\overline{INT0}$ / P3.3 = $\overline{INT1}$ / P3.4 = T0, PWM0 / P3.5 = T1 / P3.6 = $\overline{WR}$ / P3.7 = $\overline{RD}$
- Read-Modify-Write instructions do not read port pin but the port SFR.
  - ✓ ANL / ORL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y

- PORT3 Description

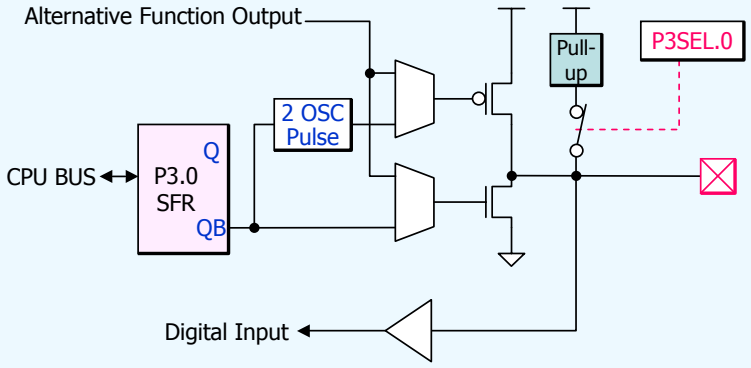
✓ **P3SEL** (E7h) : P3 Pull-up Control Register

P3SEL.7	P3SEL.6	P3SEL.5	P3SEL.4	P3SEL.3	P3SEL.2	P3SEL.1	P3SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- P3SEL[7:0] : Pull-up resistor Enable
  0 = Pull-up resistor ON / 1 = Pull-up resistor Off
  PORT3 Pull-up resistor is **ON** after reset.

✓ **P3** (B0h) : PORT3 Register

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



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6.5. I/O Ports : PORT4[3:0]

- Quasi bi-directional port.
- Pull-up resistors are switched on/off by changing the value of the P4SEF SFR.
- Available only for 44-pin PLCC package
- Read-Modify-Write instructions do not read port pin but the port SFR.
  - ✓ ANL / ORL / XRL / JBC / CPL / INC / DEC / DJNZ

- PORT4 Description

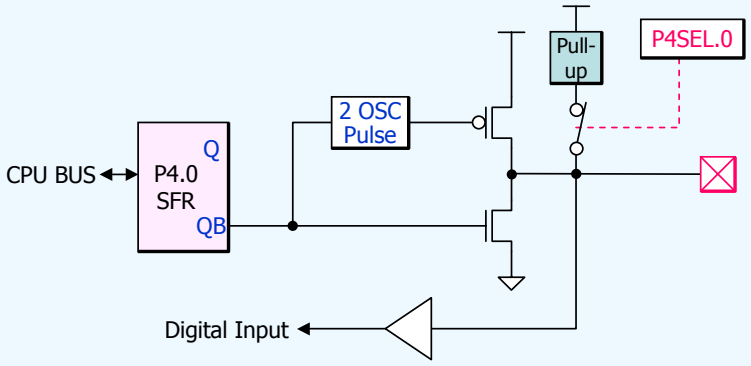
✓ **P4SEL** (A6h) : P4 Pull-up Control Register

-	-	-	-	P4SEL.3	P4SEL.2	P4SEL.1	P4SEL.0
				R/W(0)	R/W(0)	R/W(0)	R/W(0)

- P4SEL[3:0] : Pull-up resistor Enable
  0 = Pull-up resistor ON / 1 = Pull-up resistor Off
  PORT4 Pull-up resistor is **ON** after reset.

✓ **P4** (A5h) : PORT4 Register

-	-	-	-	P4.3	P4.2	P4.1	P4.0
				R/W(1)	R/W(1)	R/W(1)	R/W(1)



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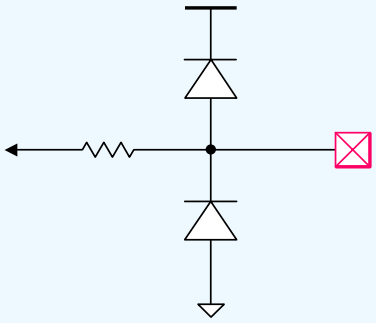
6.6. The ESD Structure of Pads

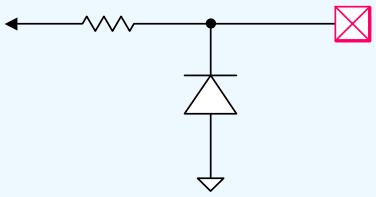
- Two ESD diodes and one ESD resister are contained in all pads except $\overline{EA}$/VPP.
- One ESD diode and one ESD resister are contained in $\overline{EA}$/VPP.

[All pads except $\overline{EA}$ / VPP]



- Two ESD Diodes (V_{DD} side, GND side)
- One ESD Resister

[$\overline{EA}$ / VPP]



- One ESD Diode (GND side)
- One ESD Resister

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6.7. LVD (Low Voltage Detector)

- On-chip power-on reset : 2.5V
- On-chip power-fail reset : 2.5V
- Optional power-fail interrupt : 4.0V

- Flag Transition

	POF	POR	PFI
A	X → 1	X → 1	X
B	1	1	X → 1
C	X	X	X → 1
D	X → 1	X → 1	1

- POF is a mirror of POR.

✓ **EXIF** (91h) : External Interrupt Flag Register

IE5	IE4	IE3	IE2	XT	-	-	BGS
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R(1)			R/W(1)

- BGS : Band-gap Select
  0 = LVD Block Off / 1 = LVD Block ON

✓ **PCON** (87h) : Power Control Register

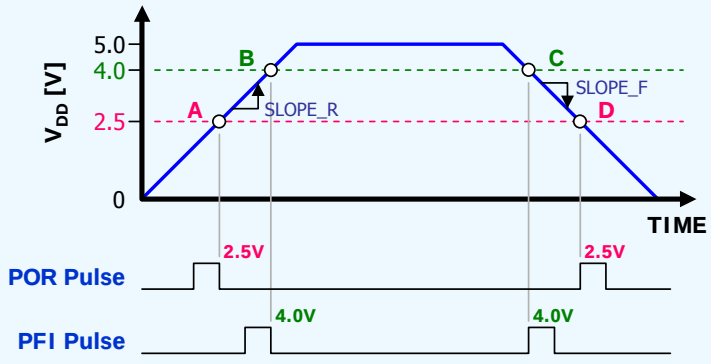
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R/W(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

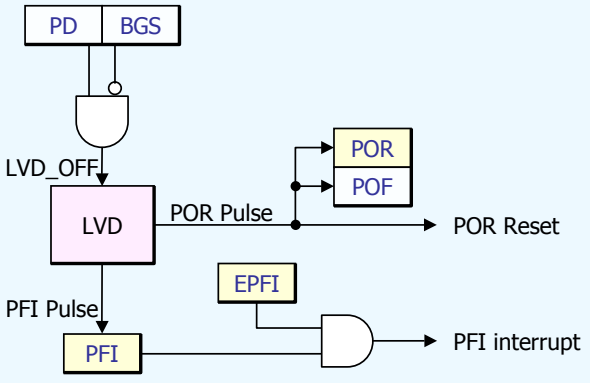
- POF : Power-off Flag
- PD : Power-down mode bit

✓ **WDCON** (D8h) : Watchdog & Power Status Register

-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- POR : Power-on Reset Flag
- EPFI : Enable Power-fail Interrupt
- PFI : Power-Fail interrupt Flag (always 1 @ 3V operation)





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6.8. WDT (Watchdog Timer)

- Detects software upset due to external noise or other causes
- Allows an automatic recovery using WDT interrupt

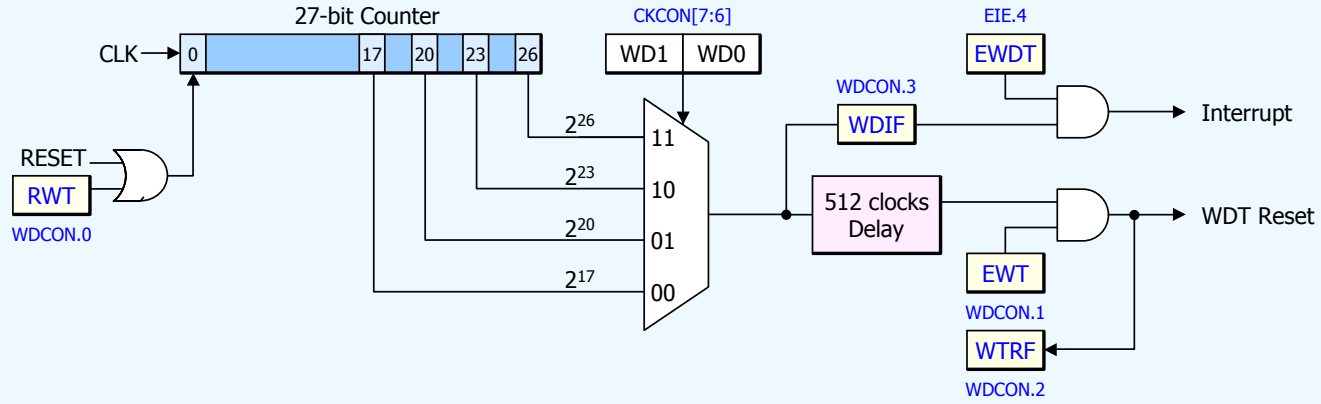
- Watchdog Time-out Values
  - ✓ Default : WD[1:0] = [0,0]

WD1	WD0	Interrupt Time-out (@25MHz)		Reset Time-out (@25MHz)	
0	0	2^{17} clocks	5.24 ms	2^{17} + 512 clocks	5.26 ms
0	1	2^{20} clocks	41.94 ms	2^{20} + 512 clocks	41.96 ms
1	0	2^{23} clocks	335.54 ms	2^{23} + 512 clocks	335.56 ms
1	1	2^{26} clocks	2,684.35 ms	2^{26} + 512 clocks	2,684.38 ms

✓ **WDCON** (D8h) : Watchdog & Power Status Register

-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- POR : Power-on Reset Flag
- EPFI : Power-fail Interrupt Enable
- PFI : Power-Fail interrupt Flag
- WDIF : Watchdog Timer Interrupt Flag
- WTRF : Watchdog Timer Reset Flag. Only cleared by S/W.
- EWT : Watchdog Timer Reset Enable
- RWT : Restart Watchdog Timer



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6.9. Timer/Counter : Timer 0/1

- Compatible with traditional 80C52 Timer/Counter
- Time base is selectable by S/W : 4 clocks or 12 clocks

Mode / Timer	Mode 0 (M1,M0=00)	Mode 1 (M1,M0=01)	Mode 2 (M1,M0=10)	Mode 3 (M1,M0=11)
Timer0	13-bit T/C	16-bit T/C	8-bit T/C with automatic reload (TL0 ← TH0)	8-bit T/C (TL0) ➔ Timer0 interrupt 8-bit T/C (TH0) ➔ Timer1 interrupt
Timer1	13-bit T/C	16-bit T/C	8-bit T/C with automatic reload (TL1 ← TH1)	Halt

✓ **TMOD** (89h) : Timer/Counter 0/1 Mode Control Register

GATE	C/T	M1	M0	GATE	C/T	M1	M0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Timer[1]: GATE[7], C/T[6], M1:M0[5:4]
- Timer[0]: GATE[3], C/T[2], M1:M0[1:0]
- GATE : When TRx (in TCON) is set and GATE=1, Timer x will run only while INTx pin is high (hardware control). When GATE=0, Timer x will run only while TRx=1 (software control).
- C/T : Counter or Timer Selector. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin).
- M1, M0 : Mode Selector bits
  - [0 0] Mode 0. 13-bit T/C.
  - [0 1] Mode 1. 16-bit T/C.
  - [1 0] Mode 2. 8-bit Auto-Reload T/C.
  - [1 1] Mode 3.
    (Timer 1) stopped,
    (Timer 0) TL0: 8-bit T/C controlled by the Timer 0 control bits.
    TH0: 8-bit T/C controlled by the Timer 1 control bits.

✓ **CKCON** (8Eh) : Clock Control Register

WD1	WD0	T2M	T1M	T0M	-	-	-
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)			

- T1M : Timer 1 Clock Time-base Selection
  T1M=1, Time-base is 4 clocks not 12clocks.
- T0M : Timer 0 Clock Time-base Selection
  T0M=1, Time-base is 4 clocks not 12clocks.

✓ **TCON** (88h) : Timer/Counter 0/1 Control Register

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- TF1 : Timer 1 Overflow Flag
- TR1 : Timer 1 Run Control
- TF0 : Timer 0 Overflow Flag
- TR0 : Timer 0 Run Control
- IE1 : External Interrupt 1 Flag
- IT1 : External Interrupt 1 Type Select
  Edge Detect (IT1=1). Level Detect (IT1=0)
- IE0 : External Interrupt 0 Flag
- IT0 : External Interrupt 0 Type Select
  Edge Detect (IT0=1). Level Detect (IT0=0)

✓ **TL0** (8Ah) : Timer/Counter 0 Low Byte Register

TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

✓ **TH0** (8Ch) : Timer/Counter 0 High Byte Register

TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

✓ **TL1** (8Bh) : Timer/Counter 1 Low Byte Register

TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

✓ **TH1** (8Dh) : Timer/Counter 1 High Byte Register

TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

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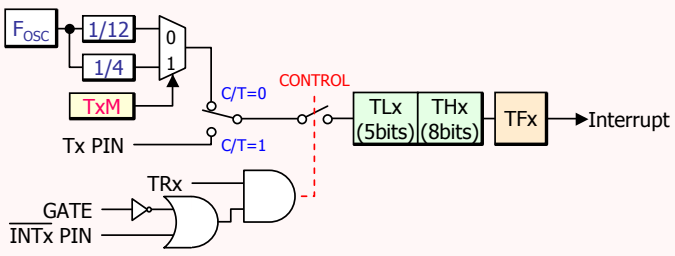
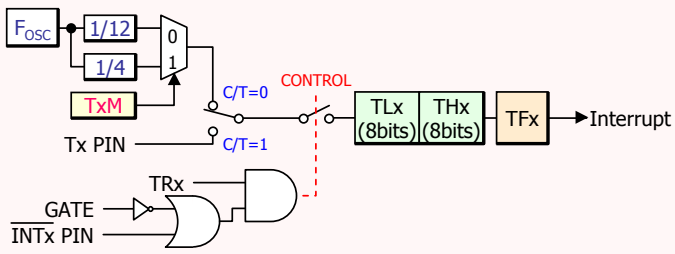
6.9. Timer/Counter : Timer 0/1 Mode Description

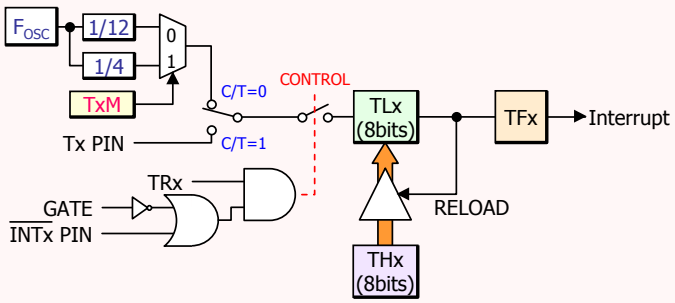
* Default : $F_{OSC}/12$ (T0M and T1m is each 0.)



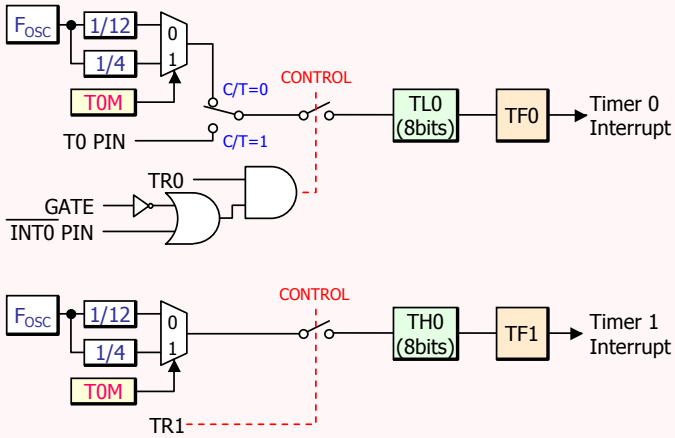
[Mode 0]



[Mode 1]



[Mode 2]



[Mode 3(Timer 0 only)]

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6.9. Timer/Counter : Timer 2

- Compatible with traditional 80C52 Timer/Counter 2 function
- Up or down counting selectable by a software
- Time base is selectable by S/W : 4 clocks or 12 clocks

1. 16-bit Auto-reload [RCLK+TCLK=0, CP/RL2=0, T2OE=0]	16-bit Timer/Counter With Automatic Reload (TH2, TL2 ← RCAP2H, RCAP2L)
2. 16-bit Capture [RCLK+TCLK=0, CP/RL2=1, T2OE=0]	16-bit Timer/Counter with Capture (RCAP2H, RCAP2L ← TH2, TL2)
3. Baudrate Generator [RCLK+TCLK=1, CP/RL2=X, T2OE=X]	Baudrate Generation * Timer 2 Interrupt Disable
4. Programmable Clock Out [RCLK+TCLK=X, CP/RL2=0, T2OE=1]	Clock-out on P1.0

✓ **T2CON** (C8h) : Timer 2 Control Register

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- TF2 : Timer 2 Overflow Flag
- EXF2 : Timer 2 External Flag
- RCLK : Receive Clock Flag
- TCLK : Transmit Clock Flag
- EXEN2 : Timer 2 External Enable Flag
- TR2 : Timer 2 Run Control
- C/T2 : Timer or Counter Selection. If C/T2=0, Timer Operation.
- CP/RL2 : Capture/Reload Flag.
  CP/RL2=0, Reload. (TH2,TL2) ← (RCAP2H, RCAP2L)
  CP/RL2=1, Capture. (RCAP2H, RCAP2L) ← (TH2,TL2)

✓ **CKCON** (8Eh) : Clock Control Register

WD1	WD0	T2M	T1M	T0M	-	-	-
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)			

- T2M : Timer 2 Clock Time-base Selection
  T2M=1, Time-base is 4 clocks not 12clocks.

✓ **T2MOD** (C9h) : Timer 2 Mode Register

-	-	-	-	-	-	T2OE	DCEN
						R/W(0)	R/W(0)

- T2OE : Timer 2 Clock Output to P1.0
- DCEN : Timer 2 Down Count Enable

✓ **TL2** (CCh) : Timer 2 Low Byte Register

TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

✓ **TH2** (CDh) : Timer 2 High Byte Register

TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

✓ **RCAP2L** (CAh) : Timer 2 Capture/Reload Low Byte Register

RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

✓ **RCAP2H** (CBh) : Timer 2 Capture/Reload High Byte Register

RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

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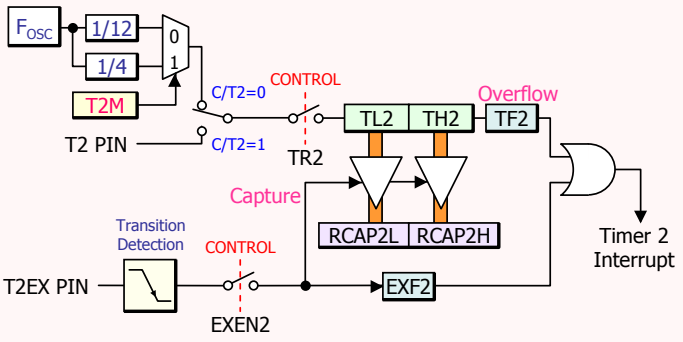
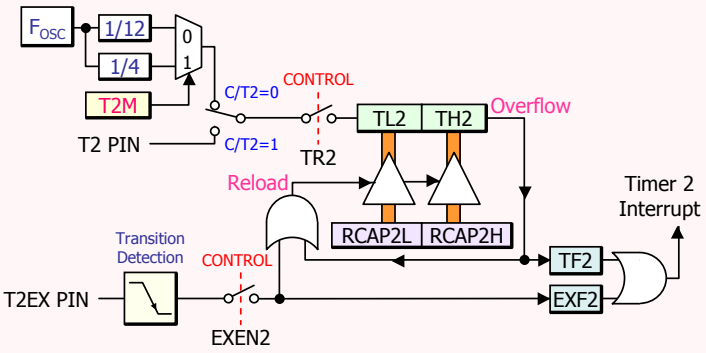
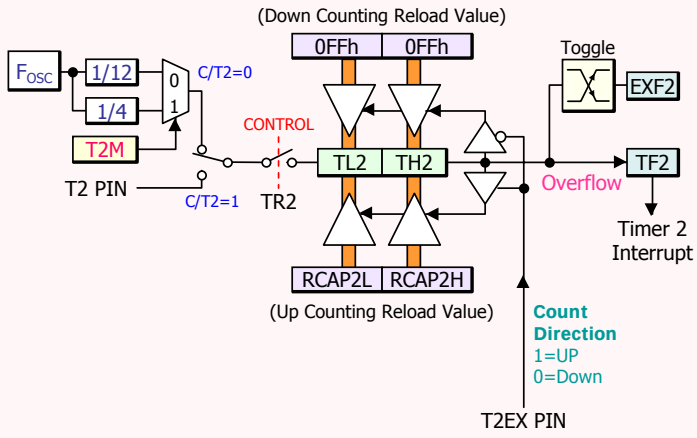
6.9. Timer/Counter : Timer 2 Mode Description



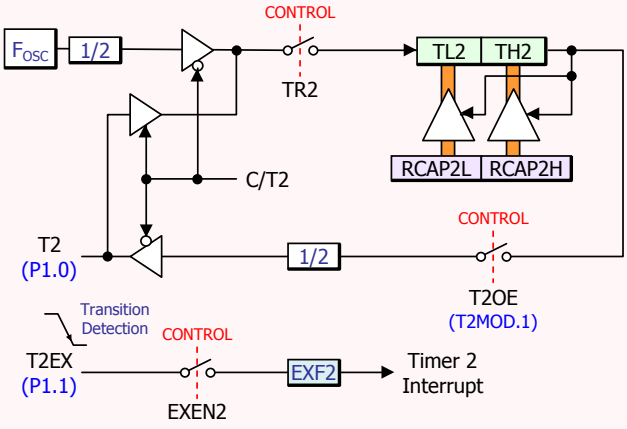
[Capture Mode]



[Auto Reload Mode (DCEN=0)]



[Auto Reload Mode (DCEN=1)]



[Clock-Out Mode]

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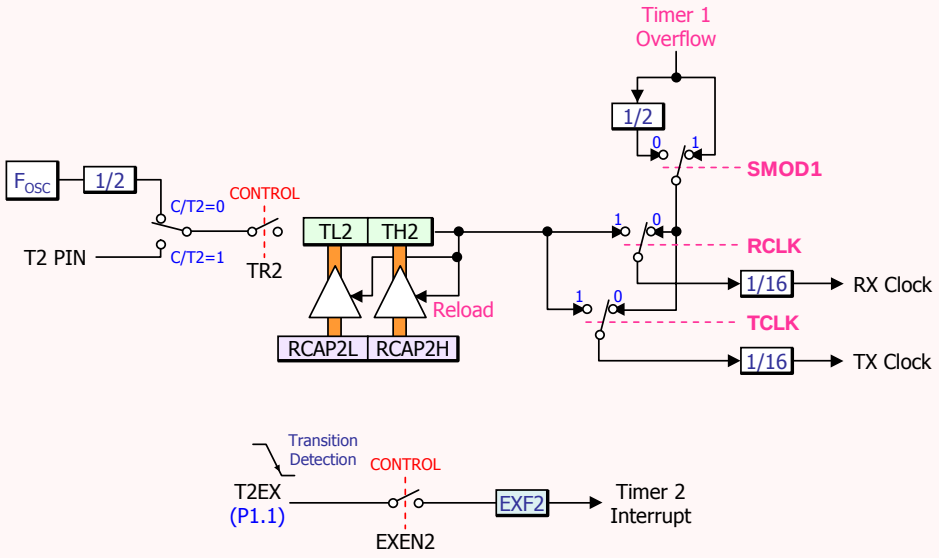
6.9. Timer/Counter : Timer 2 Mode Description



[Baudrate Generator Mode]

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6.10. UART

- Function-level compatible with traditional 80C52 UART.
- Automatic address recognition : Multiprocessor communication.

	Data Size		Baudrate
Mode 0	8 bits	8 data bits	1/4 x Oscillator Clock
Mode 1	10 bits	Start bit(0) 8 data bit Stop bit(1)	1/32 x Timer 1 Overflow (SMOD1=0) 1/16 x Timer 1 Overflow (SMOD1=1) 1/16 x Timer 2 Overflow Rate
Mode 2	11 bits	Start bit(0) 8 data bit Programmable bit Stop bit(1)	1/32 x Oscillator Clock (SMOD1=0) 1/16 x Oscillator Clock (SMOD1=1)
Mode 3	11 bits	Start bit(0) 8 data bit Programmable bit Stop bit(1)	1/32 x Timer 1 Overflow (SMOD1=0) 1/16 x Timer 1 Overflow (SMOD1=1) 1/16 x Timer 2 Overflow Rate

✓ **The Timer 1 Overflow varies with CKCON register.**
➔ 12 clocks time-base or 4 clocks time-base.

✓ **PCON** (87h) : Power Control Register

SMOD1	SDMO0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- SMOD1 : Timer 1 baudrate double in UART mode 1, 2, and 3
- SMOD0 : Enable SM0 access. Don't modify this bit.

✓ **SCON** (98h) : Serial Port Control Register

SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- SM0, SM1 : Serial Port Operating Mode Selection
  [0,0] : Mode 0. 8-bit Shift Register (OSC/4)
  [0,1] : Mode 1. 8-bit UART (Variable)
  [1,0] : Mode 2. 9-bit UART (OSC/32 or OSC/16)
  [1,1] : Mode 3. 9-bit UART (Variable)
- SM2 : Enable the Automatic Address Recognition in Mode 2 and 3.
  Cleared after receiving the address.
  In Mode 1, the validity of a Stop Bit is checked if SM2=1.
  In Mode 0, SM2 should be 0.
- REN : Enable/Disable Reception.
- TB8 : 9th data bit that will be transmitted in Mode 2 and 3.
- RB8 : 9th data bit that was received in Mode 2 and 3.
  In Mode 1, RB8 is equal to Stop Bit if SM2=0.
  In Mode 0, RB8 is not used.
- TI : Transmission Interrupt Flag. Must be cleared by S/W.
- RI : Reception Interrupt Flag. Must be cleared by S/W.

✓ **SBUF** (99h) : Serial Data Buffer Register

SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- The transmission buffer and the reception buffer are separated.
- The transmission/reception buffers have the same address.

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6.10. UART : Baudrate Example

- Serial Port Operating Mode 0

$$\text{Baudrate} = \frac{\text{Oscillator Frequency}}{4}$$

- Serial Port Operating Mode 2

$$\text{Baudrate} = \frac{2^{SMOD1}}{32} \times \text{Oscillator Frequency}$$

(PCON.7)

- Serial Port Operating Mode 1, 3
  - ✓ Using Timer 1 Overflow

$$\text{Baudrate} = \frac{2^{SMOD1}}{32} \times \text{Timer 1 overflow}$$

  - ✓ Using Timer 2 Overflow

$$\text{Baudrate} = \frac{\text{Timer 2 overflow}}{16}$$

EX) Using Timer 1 to Generate Baudrates

$$\text{Mode 1 \& 3 Baudrate} = \frac{2^{SMOD1}}{32} \times F_{OSC} \times \frac{3^{T1M}}{12} \times \frac{1}{[\,256 - (TH1)\,]}$$

- If SMOD1(PCON.7) = 1 ➔ Double Buadrate
- If T1M(CKCON.4) = 0 ➔ F_{OSC} / 12
- If T1M(CKCON.4) = 1 ➔ F_{OSC} / 4

EX) Using Timer 2 to Generate Baudrates

$$\text{Mode 1 \& 3 Baudrate} = \frac{1}{32} \times F_{OSC} \times \frac{1}{[65536 - (RCAPH,RCAPL)\,]}$$

Baudrate		UART Mode	F_{OSC}	SMOD1	Timer 1		
T1M=0	T1M=1				C/T	Mode	Reload Value (TH1)
Max : 3 MHz	Max : 3 MHz	Mode 0	12 MHz	X	X	X	X
Max : 750 KHz	Max : 750 KHz	Mode 2	12 MHz	1	X	X	X
62.5 KHz	187.5 KHz	Mode 1 & 3	12 MHz	1	0	2	FFh
19.2 KHz	57.6 KHz		11.0592 MHz	1	0	2	FDh
9.6 KHz	28.8 KHz		11.0592 MHz	0	0	2	FDh
4.8 KHz	14.4 KHz		11.0592 MHz	0	0	2	FAh
2.4 KHz	7.2 KHz		11.0592 MHz	0	0	2	F4h
1.2 KHz	3.6 KHz		11.0592 MHz	0	0	2	E8h
137.5 Hz	412.5 Hz		11.0592 MHz	0	0	2	1Dh
110 Hz	330 Hz		6 MHz	0	0	2	72h
110 Hz	330 Hz		12 MHz	0	0	1	FEEBh

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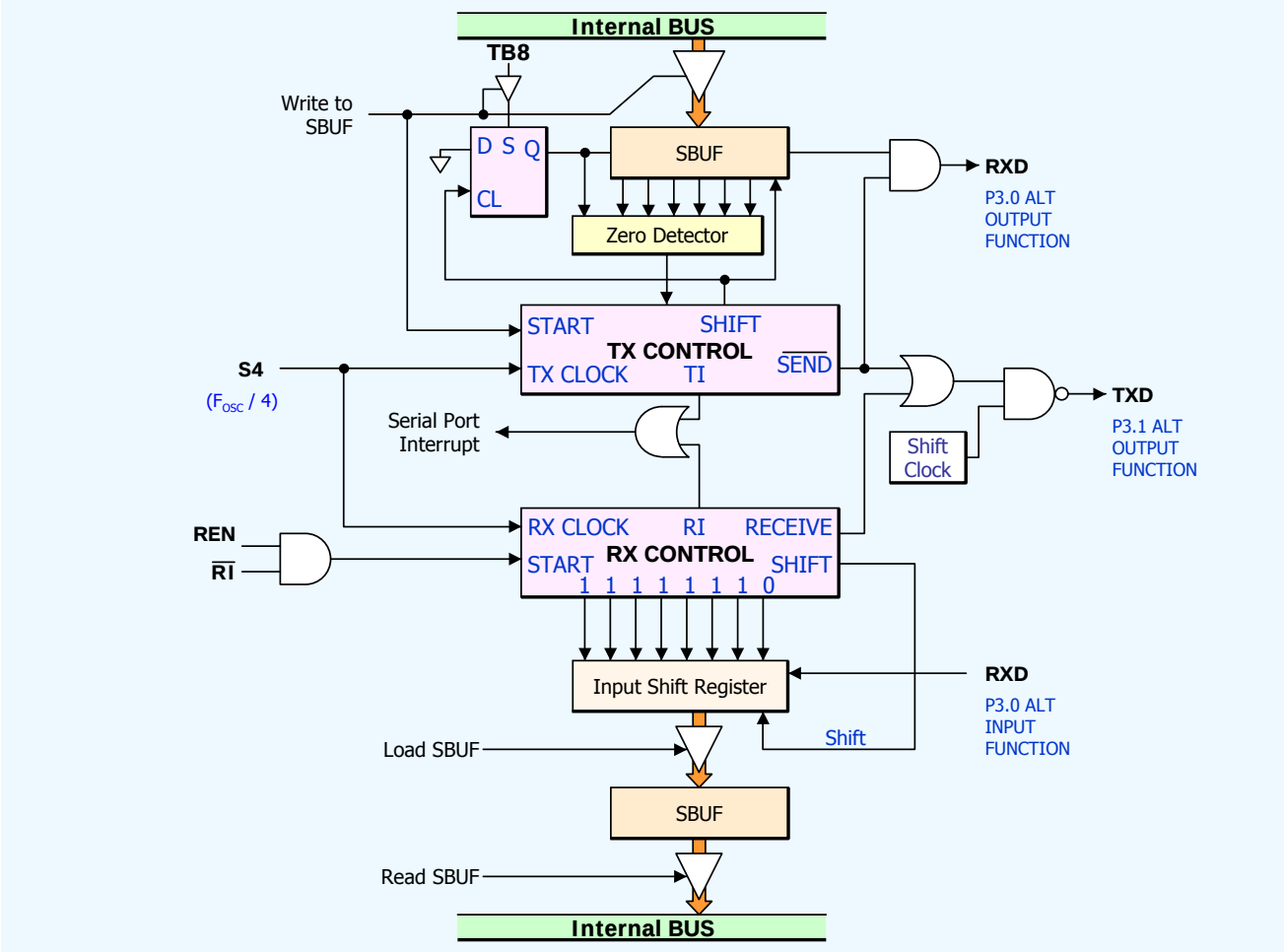
6.10. UART : Mode 0, Functional Diagram



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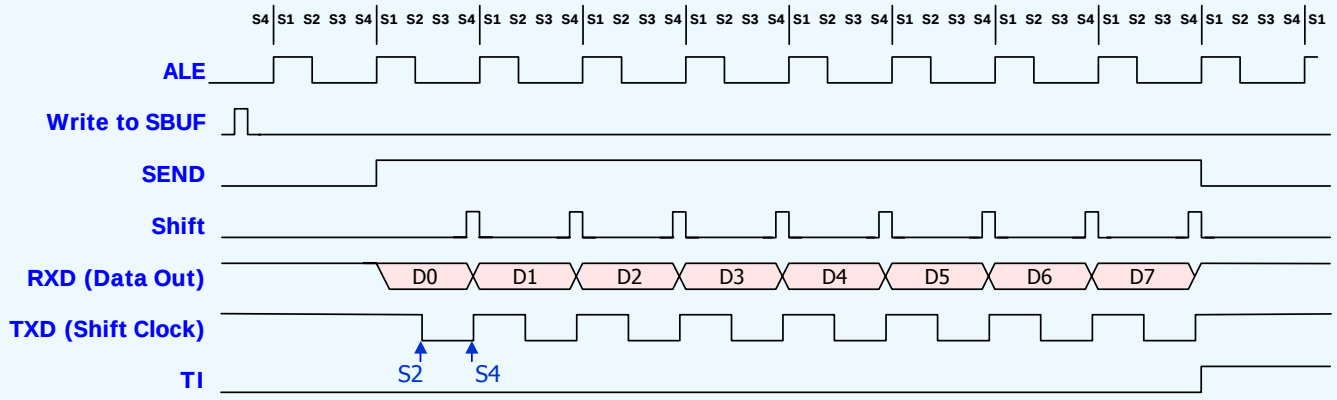
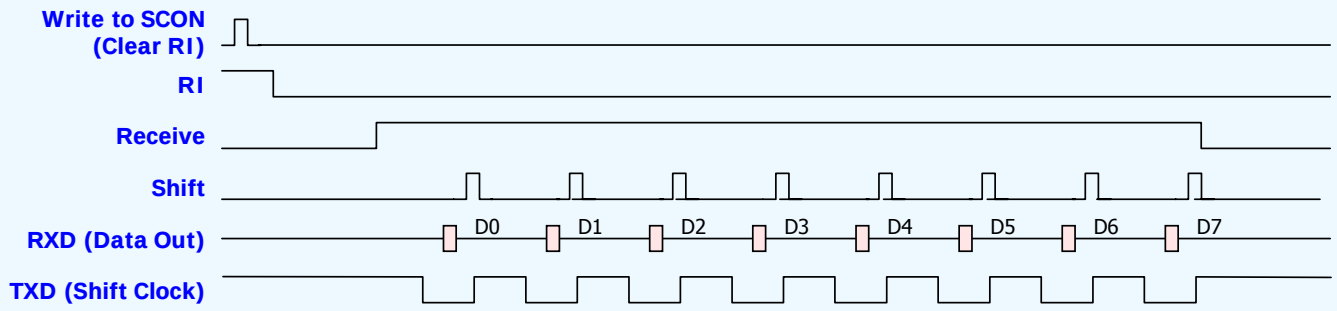
6.10. UART : Mode 0, Timing Diagram

[Transmit]



[Receive]



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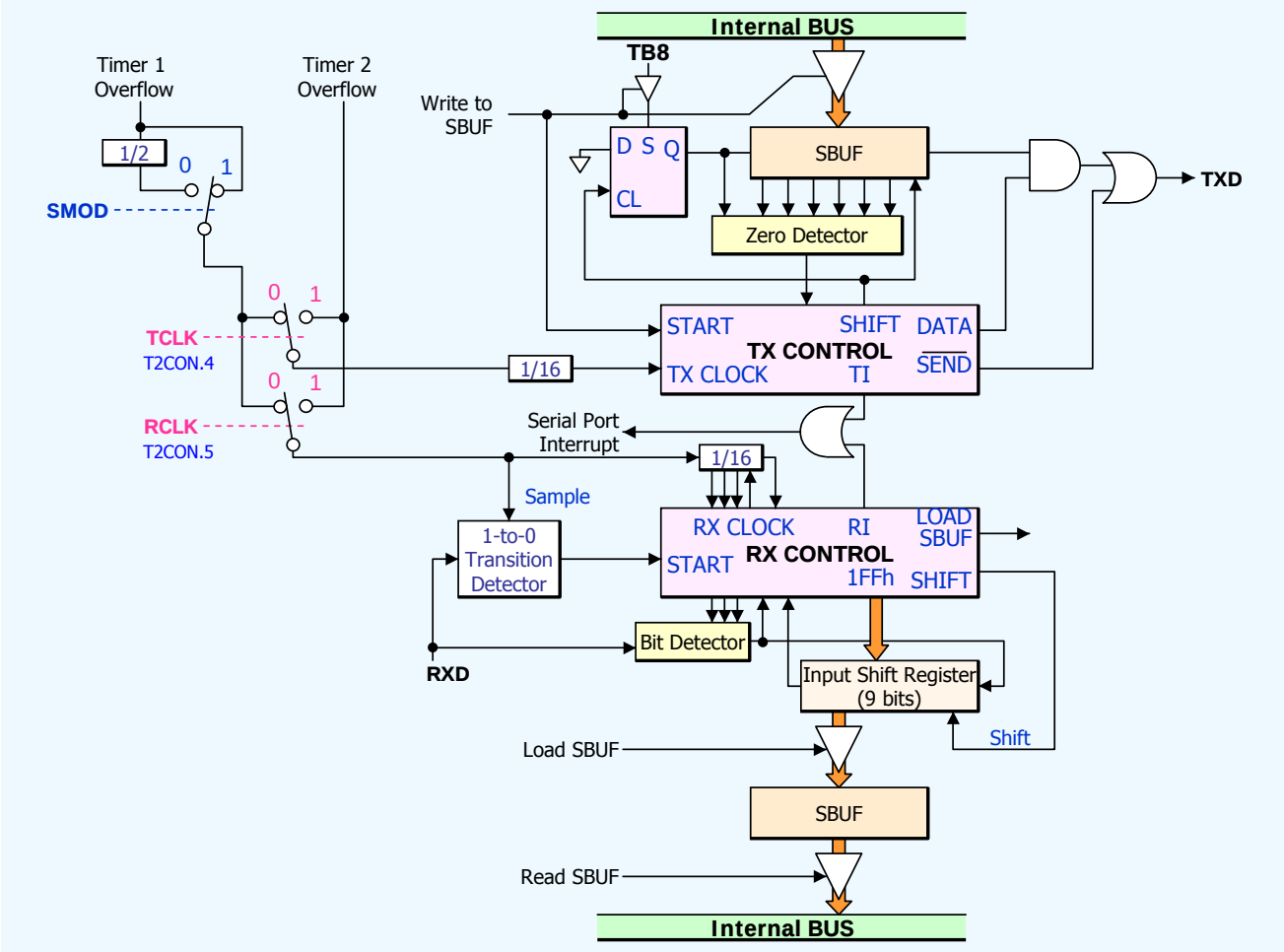
6.10. UART : Mode 1, Functional Diagram



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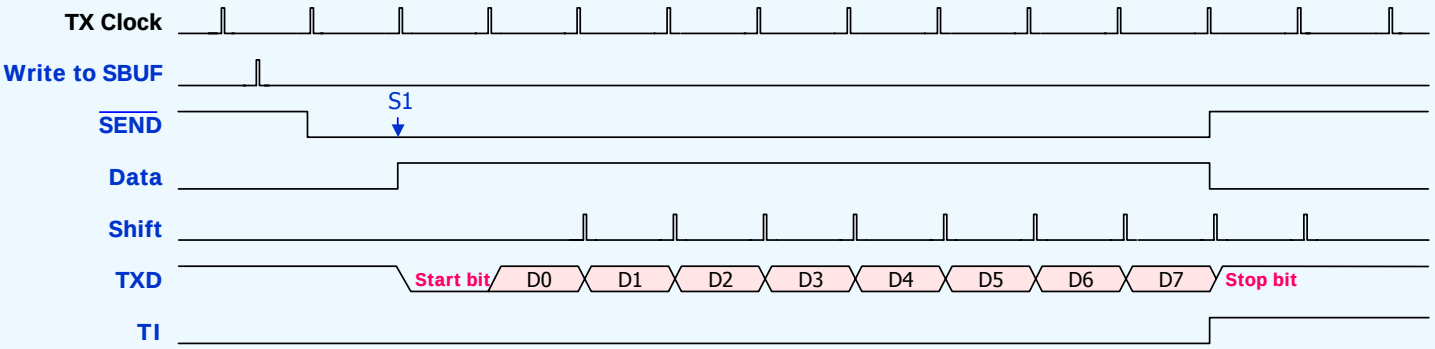
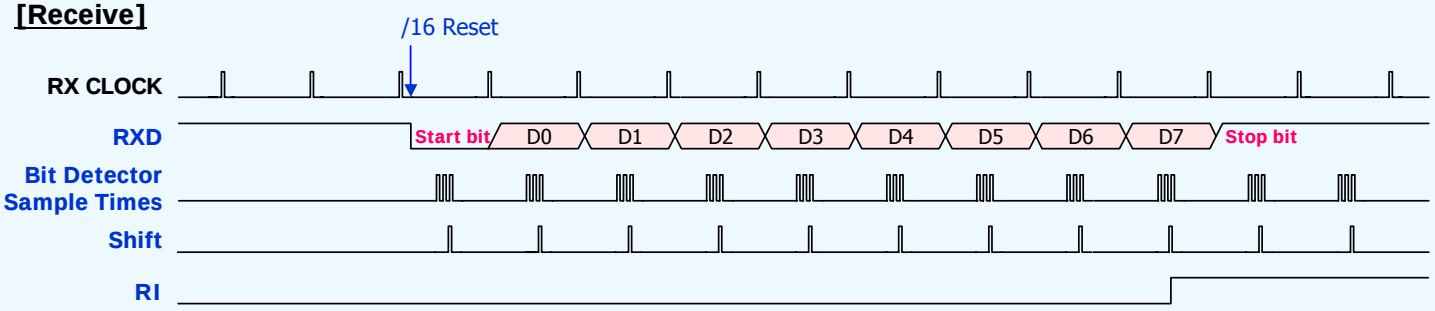
6.10. UART : Mode 1, Timing Diagram

[Transmit]



[Receive]



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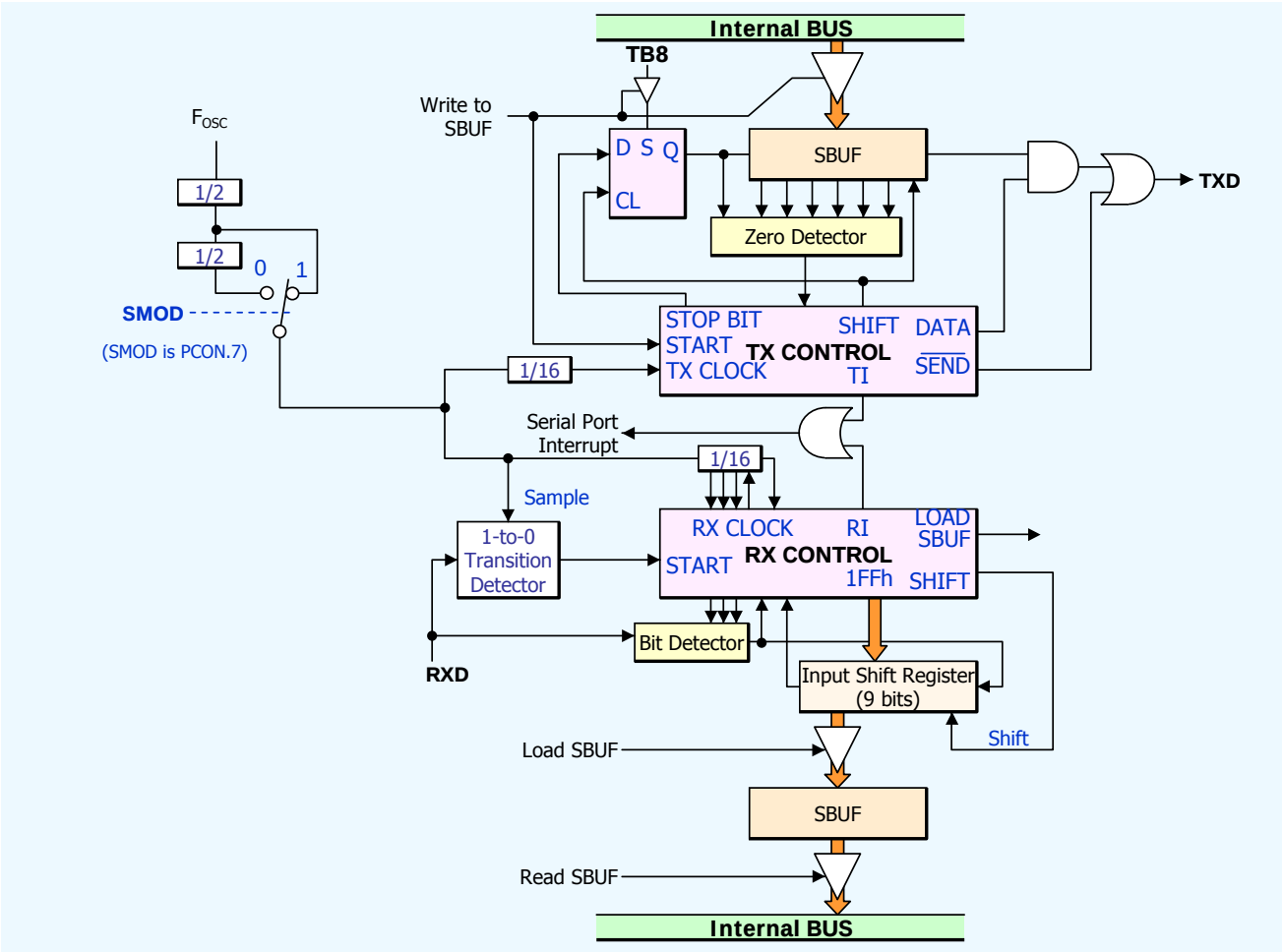
6.10. UART : Mode 2, Functional Diagram



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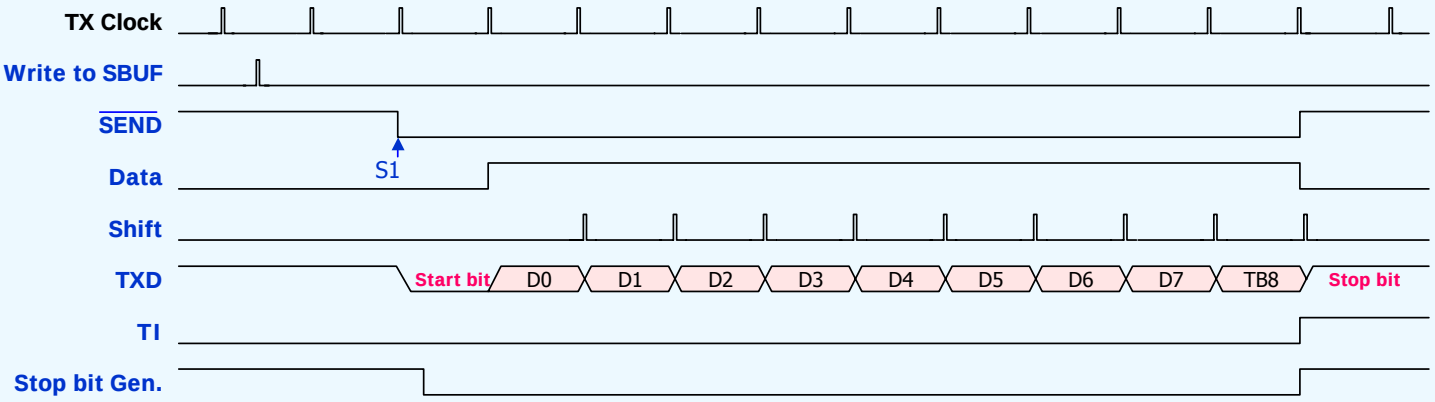
6.10. UART : Mode 2, Timing Diagram

[Transmit]



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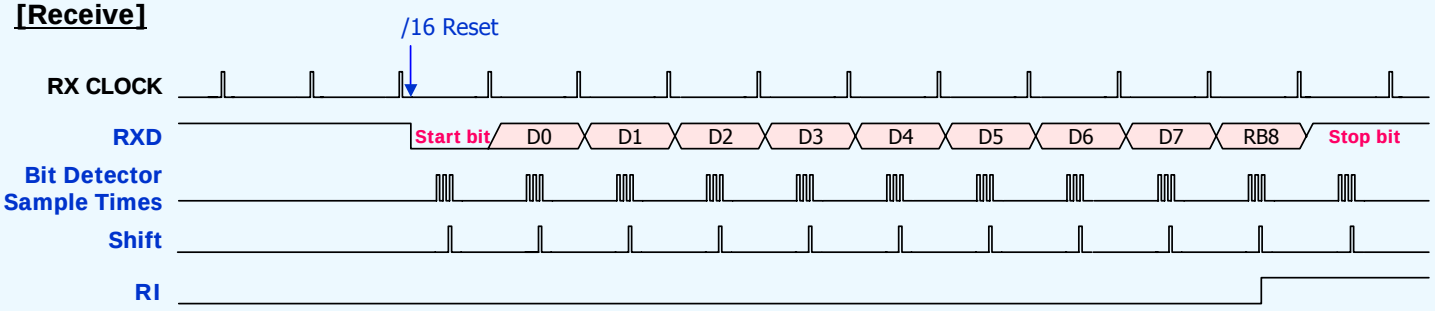

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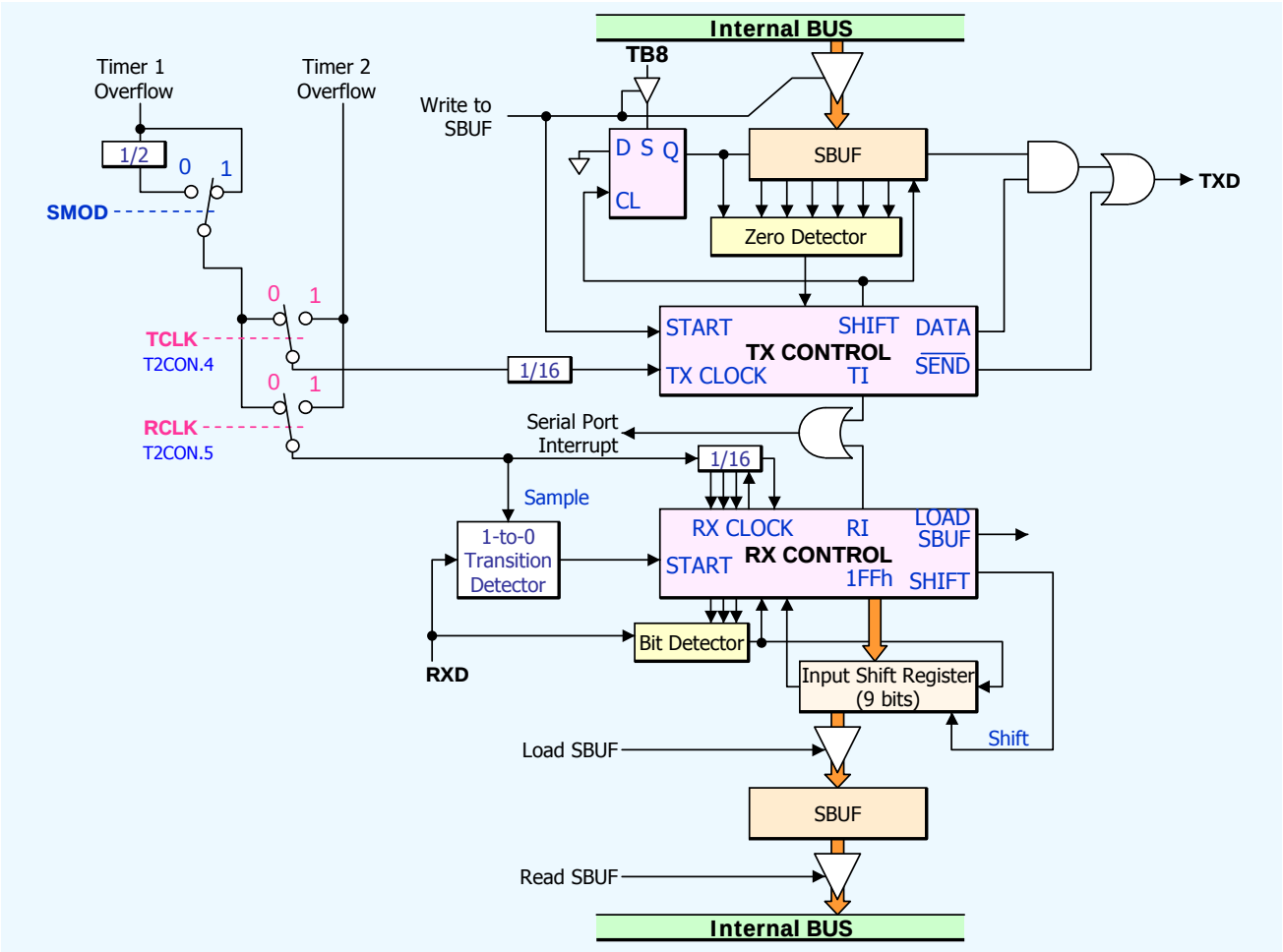
6.10. UART : Mode 3, Functional Diagram



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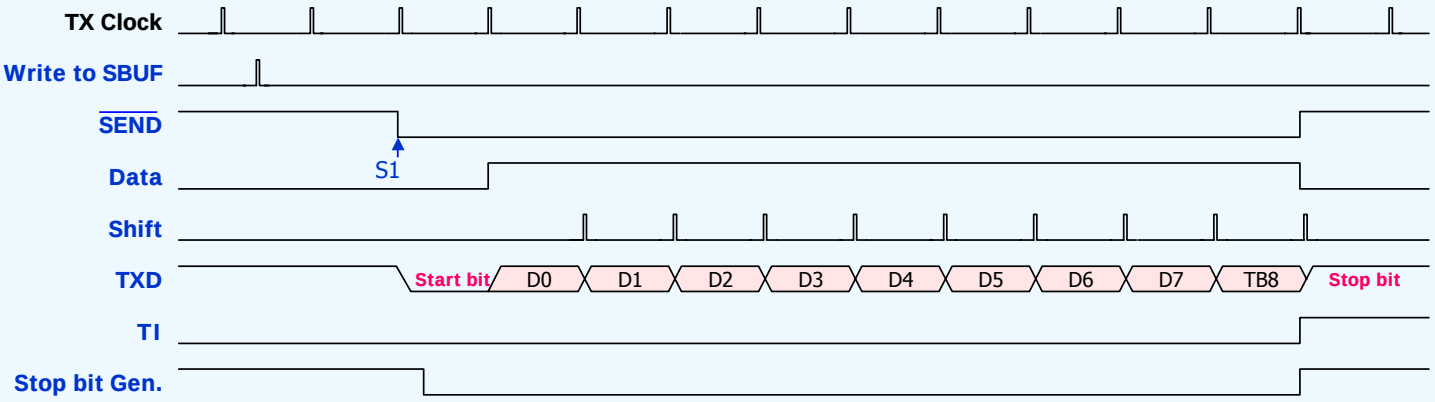
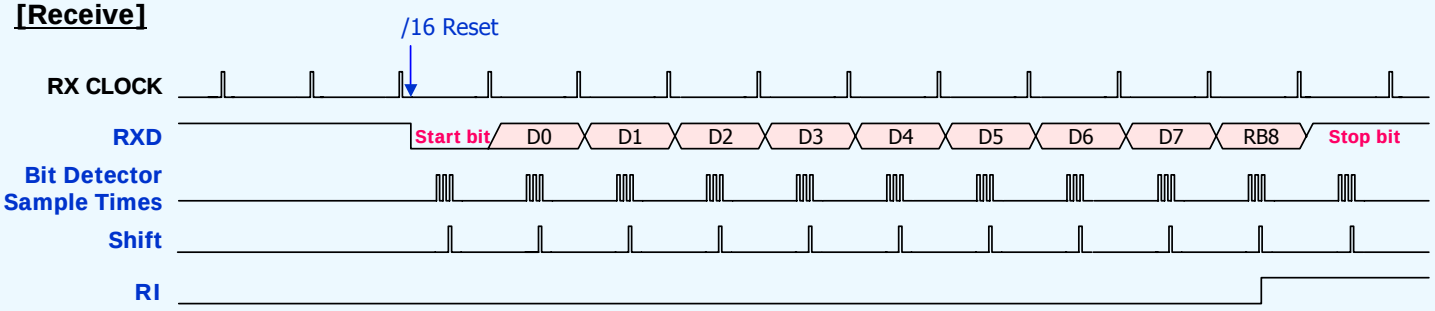
6.10. UART : Mode 3, Timing Diagram

[Transmit]



[Receive]



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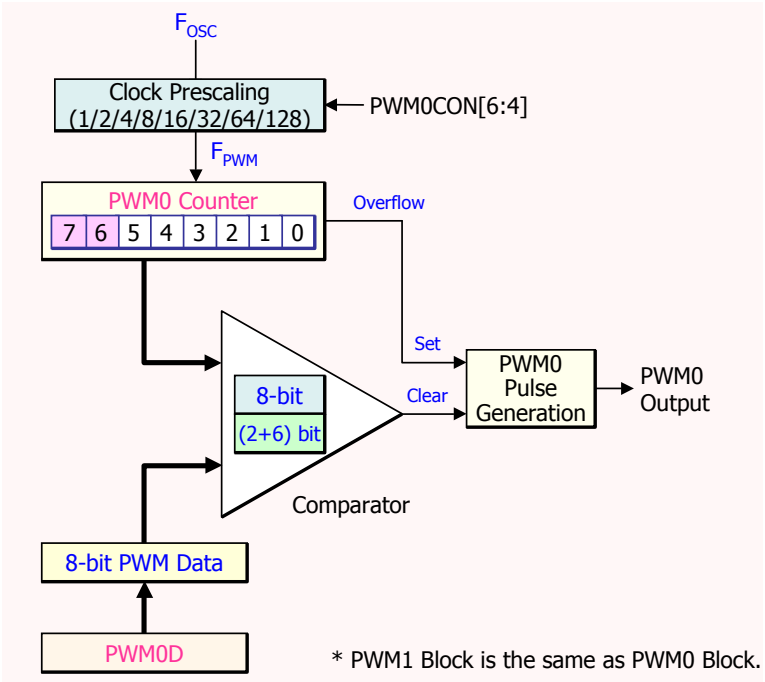
6.11. PWM (Pulse Width Modulator)

- Intelligent 2-channel 8-bit PWM
- PWM Data buffer Update (8-bit / 6-bit Counter Overflow Update)
- PWM Counter can be cleared by S/W.
- PWM is stopped or started (resumed) by S/W.

Mode	Description
8-bit Mode	8-bit Compare
(2+6)-bit Mode	2-bit Extension Compare & 6-bit Compare



* PWM1 Block is the same as PWM0 Block.

✓ **PWM0CON** (DCh) : PWM0 Control Register

P0SEL	PS2_P0	PS1_P0	PS0_P0	MODE_P0	RL_P0	CLR_P0	RUN_P0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- P0SEL : PWM0 Waveform Output to Port 3.4.
- PS2_P0, PS1_P0, and PS0_P0 : Clock prescale ratio Selection. F_{OSC}/1, /2, /4, /8, /16, /32, /64, /128.
- MODE_P0 : 8-bit / (2+6)-bit Counter Mode Selector. MODE_P0=0, (2+6)-bit Mode MODE_P0=1, 8-bit Mode
- RL_P0 : PWM data update mode selector. RL_P0=0, update at 6-bit Counter Overflow. RL_P0=1, update at 8-bit Counter Overflow.
- CLR_P0 : Counter Reset Enable. Clear by H/W.
- RUN_P0 : Counter Start Enable.

✓ **PWM1CON** (DDh) : PWM1 Control Register

P1SEL	PS2_P1	PS1_P1	PS0_P1	MODE_P1	RL_P1	CLR_P1	RUN_P1
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

✓ **PWM0D** (DEh) : PWM0 Duty Data Register

PWM0D.7	PWM0D.6	PWM0D.5	PWM0D.4	PWM0D.3	PWM0D.2	PWM0D.1	PWM0D.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

✓ **PWM1D** (DFh) : PWM1 Duty Data Register

PWM1D.7	PWM1D.6	PWM1D.5	PWM1D.4	PWM1D.3	PWM1D.2	PWM1D.1	PWM1D.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

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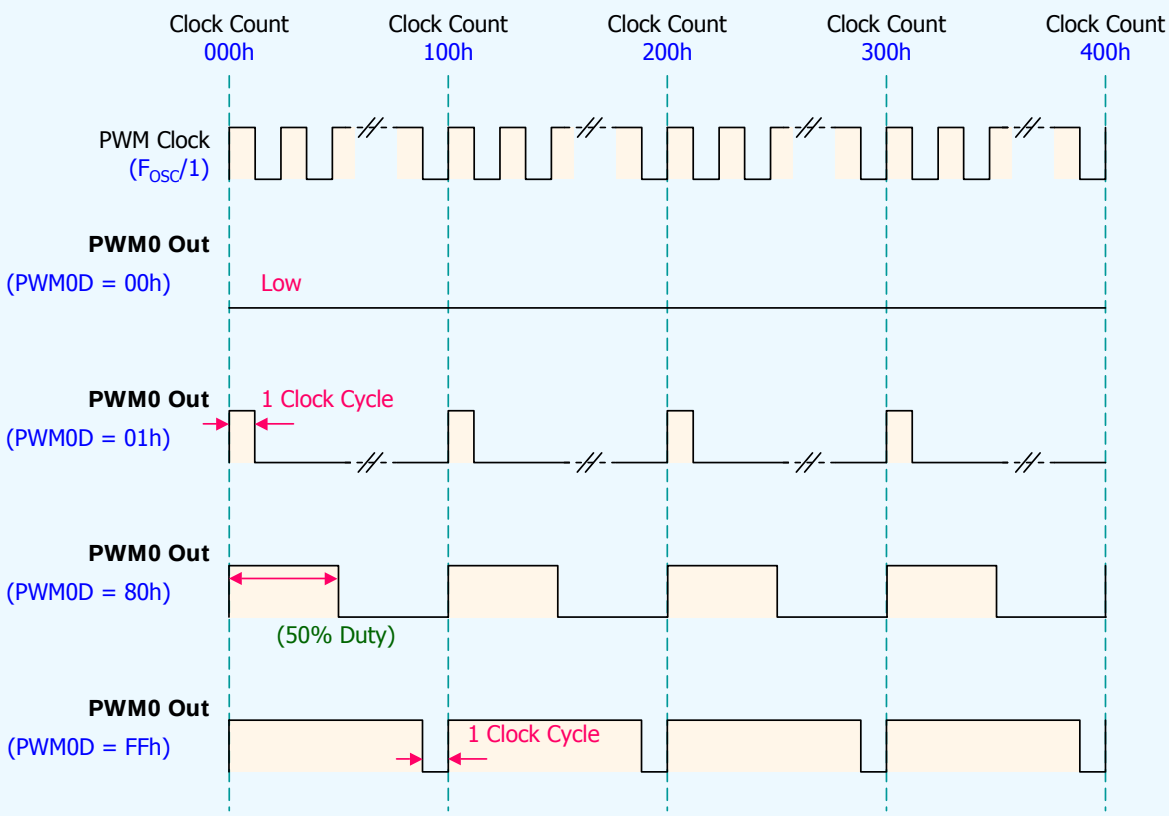
6.11. PWM : 8-bit Mode Pulse Generation



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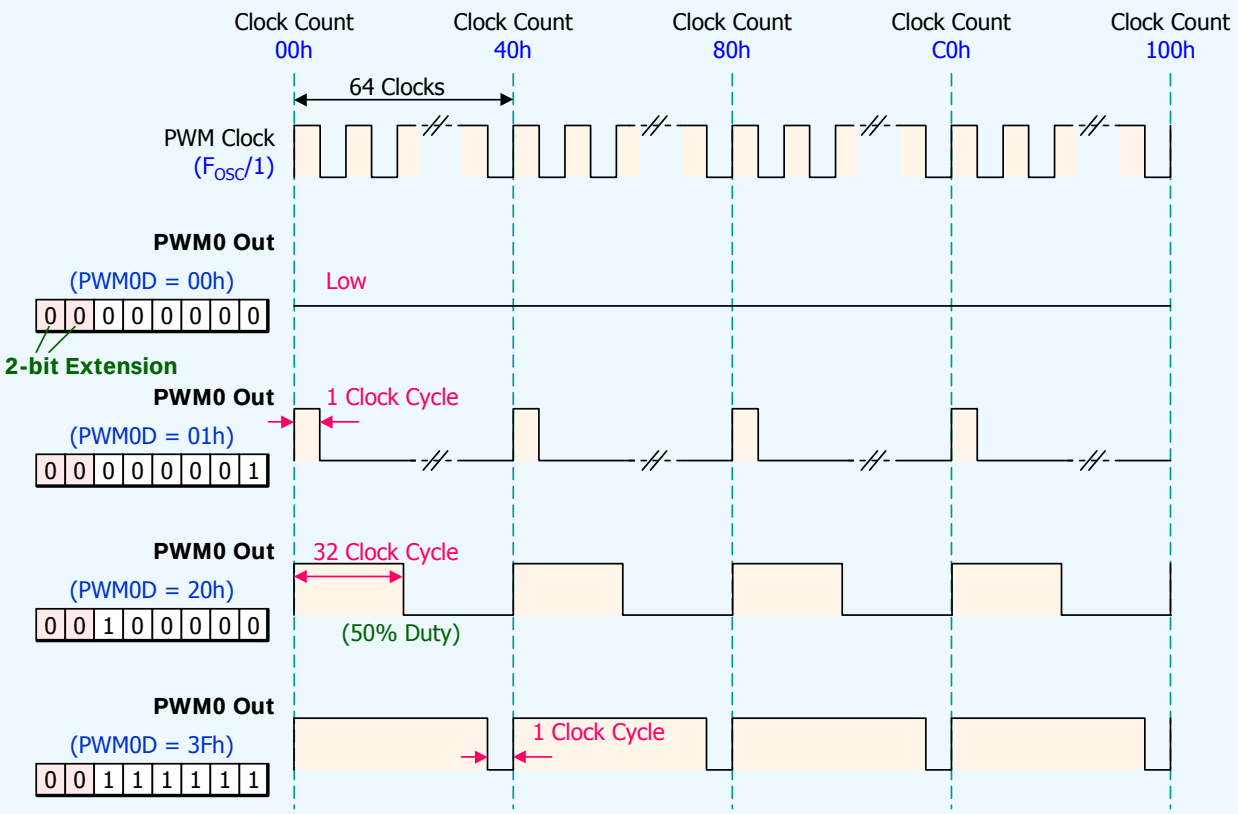
6.11. PWM : The (2+6)-bit Mode



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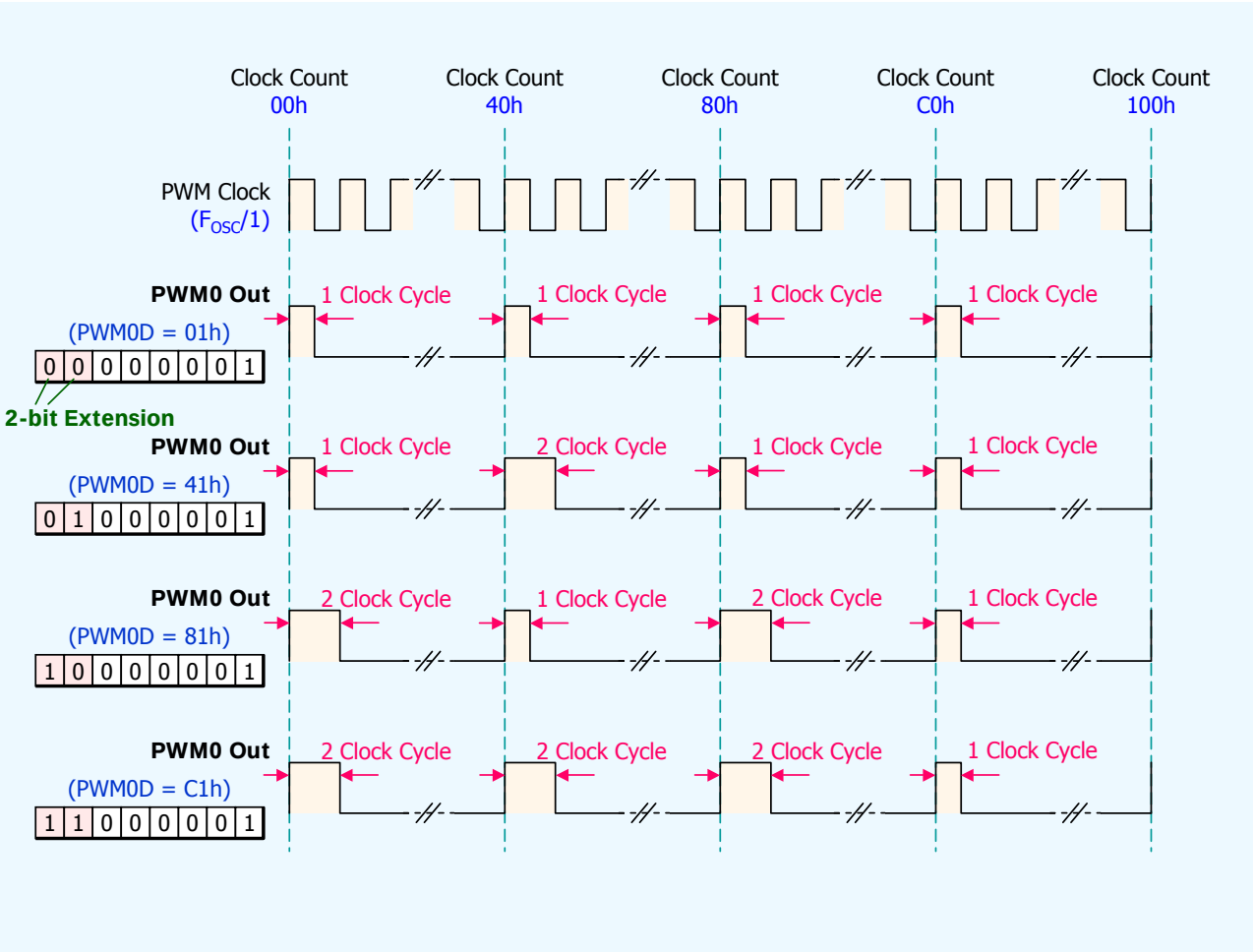
6.11. PWM : The (2+6)-bit Mode (Cont'd)



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6.12. ADC (Analog-to-Digital Converter)

- 4-channel 9-bit ADC (SAR Type)
- Max. 114ksps(samples per sec.) @ F_{ADC} = 10MHz & 5V
- Max. 57ksps @ F_{ADC} = 5MHz & 3V.

✓**ADCON** (EFh) : ADC Control & ADC Result Value[0] Register

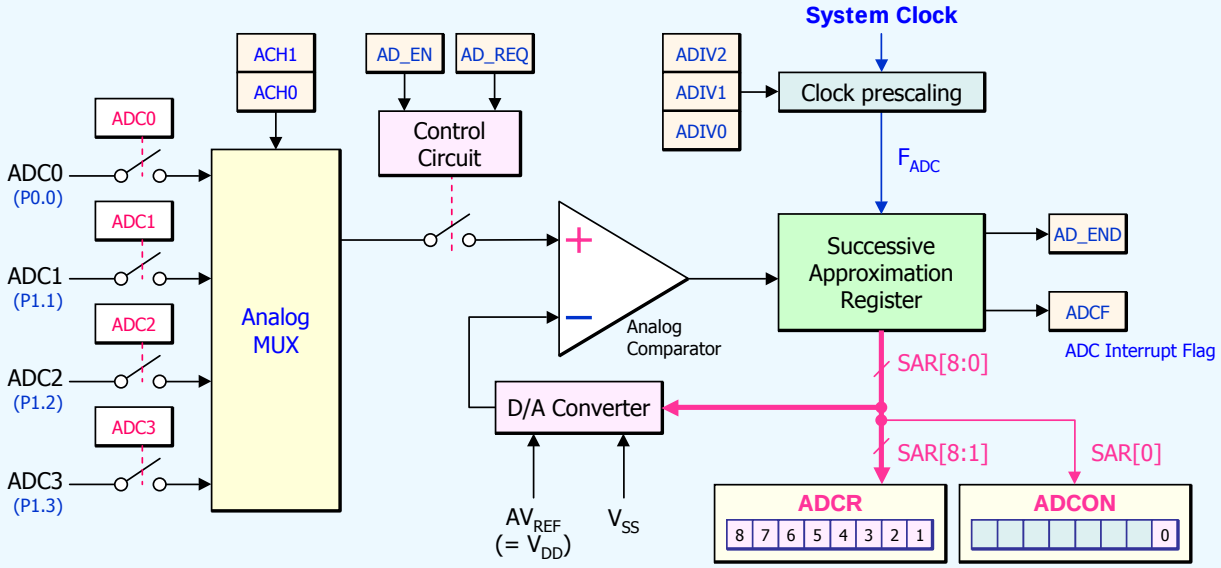
AD_EN	AD_REQ	AD_END	ADCF	ACH1	ACH0	-	SAR0
R/W(0)	R/W(0)	R(1)	R/W(0)	R/W(0)	R/W(0)		R/W(0)

✓**ADCSEL** (E2h) : ADC Clock and Port Control Register

ADIV2	ADIV1	ADIV0	-	ADC3	ADC2	ADC1	ADC0
R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)	R/W(0)	R/W(0)

✓ **ADCR** (EEh) : ADC Result Value[8:1] Register

SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	SAR1
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)



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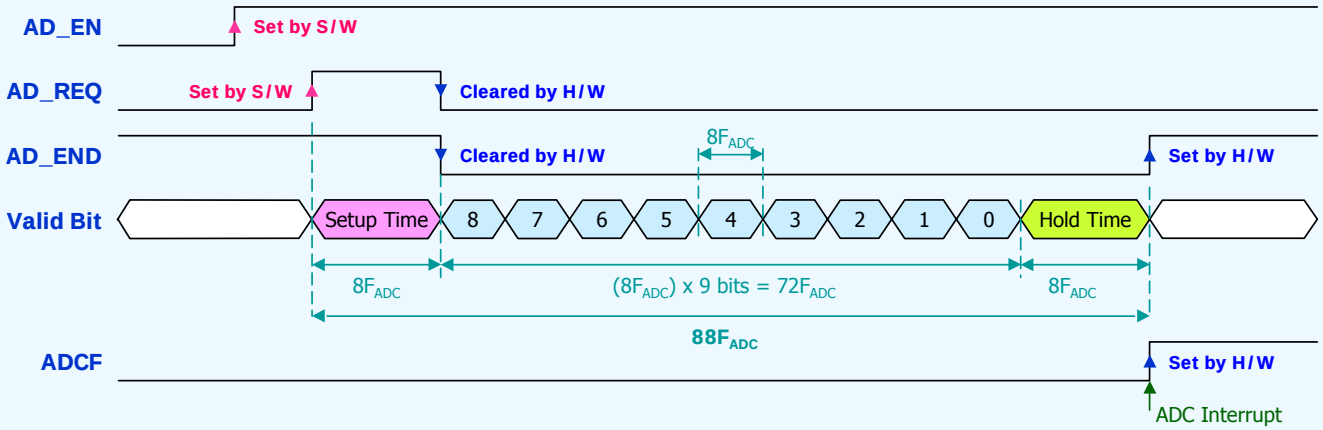
6.12. ADC : Conversion Timing



- ✓ **AD_EN** : AD conversion Enable.
  Set or Cleared by S/W.
- ✓ **AD_REQ** : AD conversion Request.
  Set by S/W and Cleared by H/W.
  This bit must be set again
  for AD conversion of each sample.
- ✓ **AD_END** : This bit is set and cleared by H/W.
  Cleared when AD conversion starts.
  Set when the AD conversion ends.
- ✓ **ADCF** : AD conversion Interrupt Flag.
  Set by H/W and Cleared by S/W.
  It should be cleared by ADC interrupt routine.

[An Example of ADC Conversion Table]

OSC	Divide (ADCSEL[7:5])	F_{ADC}	T ($1/F_{ADC}$)	1 Sample Conversion Time
20MHz @5V	000 (OSC/2)	10MHz	100ns	8.8us
	001 (OSC/4)	5MHz	200ns	17.6us
	010 (OSC/8)	2.5MHz	400ns	35.2us
	011 (OSC/16)	1.25MHz	800ns	70.4us
	100 (OSC/32)	0.625MHz	1.6us	140.8us
10MHz @3V/5V	000 (OSC/2)	5MHz	200ns	17.6us
	001 (OSC/4)	2.5MHz	400ns	35.2us
	010 (OSC/8)	1.25MHz	800ns	70.4us
	011 (OSC/16)	0.625MHz	1.6us	140.8us
	100 (OSC/32)	0.312MHz	3.2us	281.6us

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6.13. Interrupt : 13 Sources / 4-level Priority

- Interrupt Sources : Timer 0/1/2, UART, ADC, WDT, LVD, 6 External.
- 4-level Interrupt Priority

[Interrupt Vector Address]

HIGH

PRIORITY

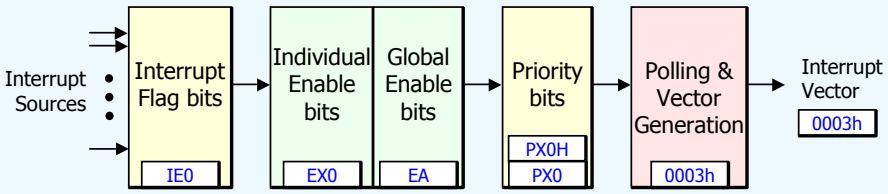
LOW

Interrupt Sources	Address	Priority Level	
LVD	0033h	-	NMI
$\overline{INT0}$	0003h	4 Levels	8052
TF0	000Bh	4 Levels	
$\overline{INT1}$	0013h	4 Levels	
TF1	001Bh	4 Levels	
RI+TI	0023h	4 Levels	
TF2	002Bh	4 Levels	
ADC	003Bh	4 Levels	
INT2	0043h	2 Levels	
$\overline{INT3}$	004Bh	2 Levels	
INT4	0053h	2 Levels	
$\overline{INT5}$	005Bh	2 Levels	
WDT	0063h	2 Levels	

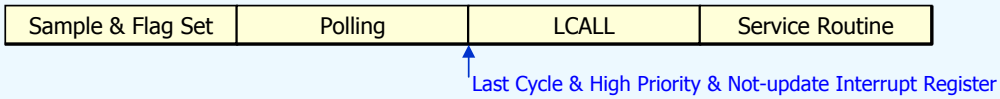
*** Interrupt related to SFR (refer to Appendix B : SFR Description)**

✓ **TCON** (88h)	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
✓ **EXIF** (91h)	IE5	IE4	IE3	IE2	XT	-	-	BGS
✓ **IE** (A8h)	EA	EADC	ET2	ES	ET1	EX1	ET0	EX0
✓ **EIE** (E8h)	-			EWDT	EX5	EX4	EX3	EX2
✓ **IP** (B8h)	-	PADC	PT2	PS	PT1	PX1	PT0	PX0
✓ **IPH** (B7h)	-	PADCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
✓ **EIP** (F8h)	-			PWDT	PX5	PX4	PX3	PX2
✓ **WDCON** (D8h)	-	POR	EPFI	PRI	WDIF	WTRF	EWT	RWT

[Interrupt Vector Generation Flow]



[Response Sequence]



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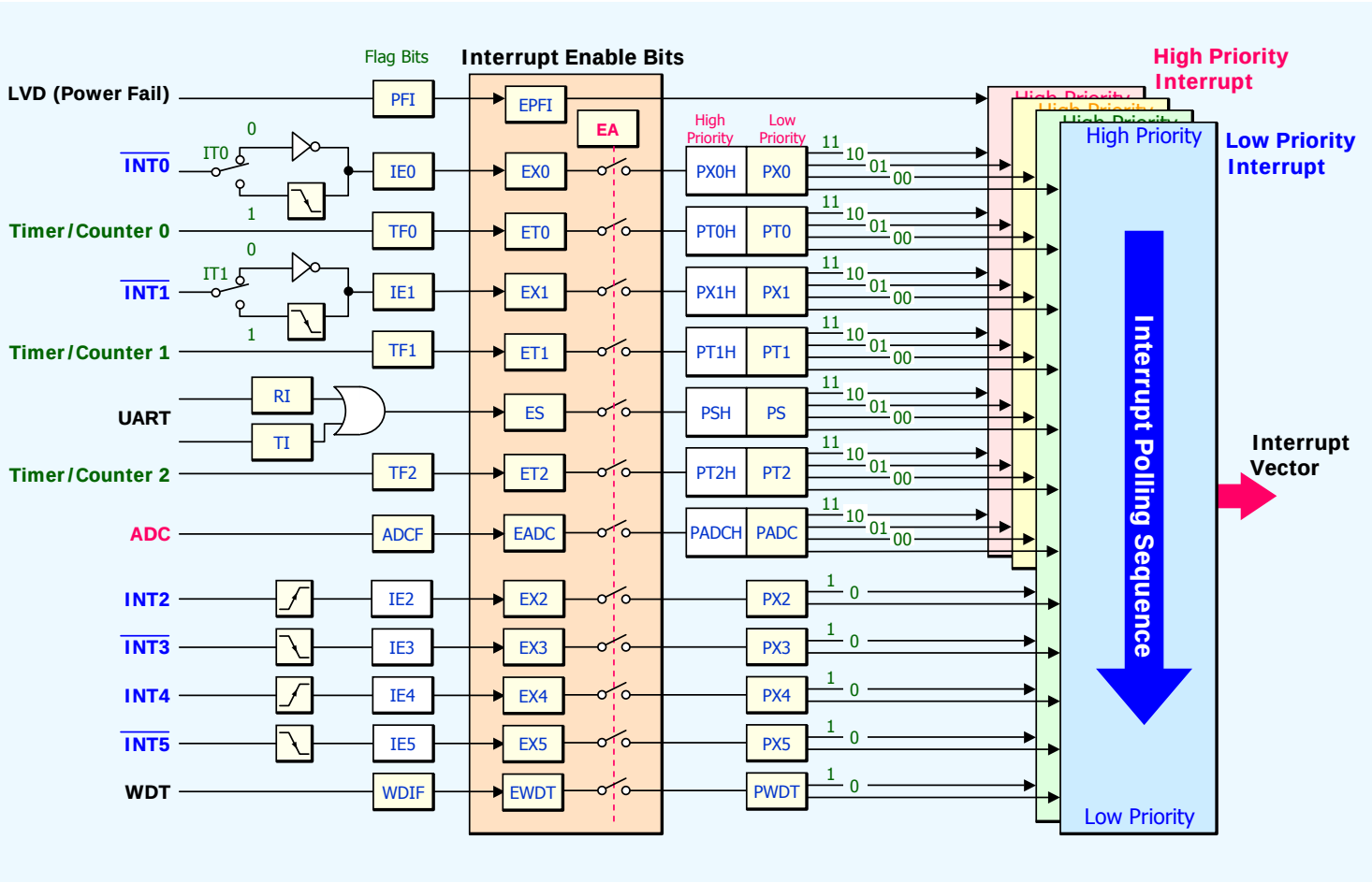
6.13. Interrupt Functional Description



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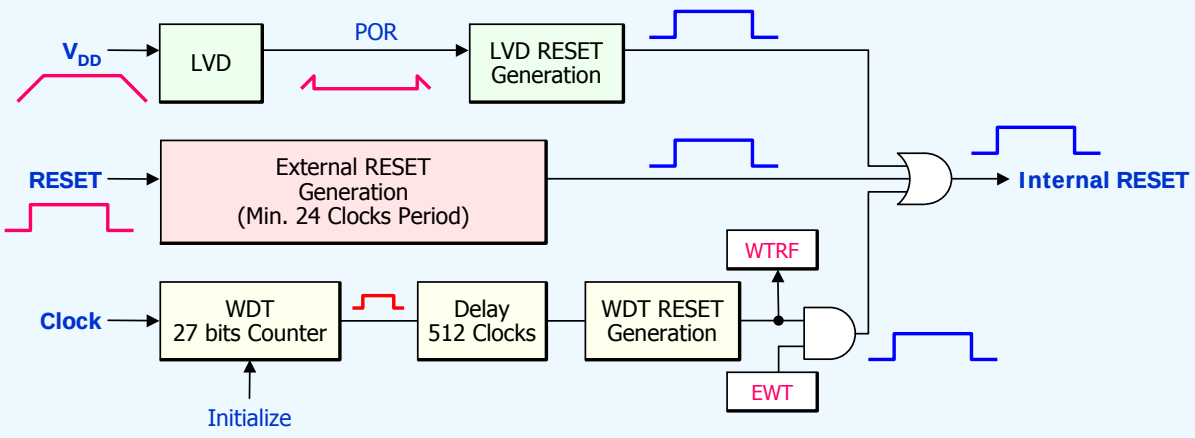
6.14. Reset Circuit : 3 Reset Sources

- LVD(POR) Reset
  - ✓ Power-on Reset when power is turned on.
  - ✓ Power-fail Reset when the supply voltage is below the threshold voltage (V_{RST}).
- External RESET Pin
  - ✓ RESET Pin must be held "High" for at least 24 clock cycles.
- WDT Reset : Enable or Disable by S/W

✓ **WDCON** (D8h) : Watchdog & Power Status Register

-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- WTRF : Watchdog Timer Reset Flag. Only cleared by S/W.
- EWT : Watchdog Timer Reset Enable.



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6.15. Clock Circuit

- System Clock Sources
  - ✓ Crystal OSC
  - ✓ Oscillator

✓ **EXIF** (91h) : External Interrupt Flag Register

IE5	IE4	IE3	IE2	XT	-	-	BGS
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R(1)			R/W(1)

✓ **STATUS** (C5h) : Crystal Status Register

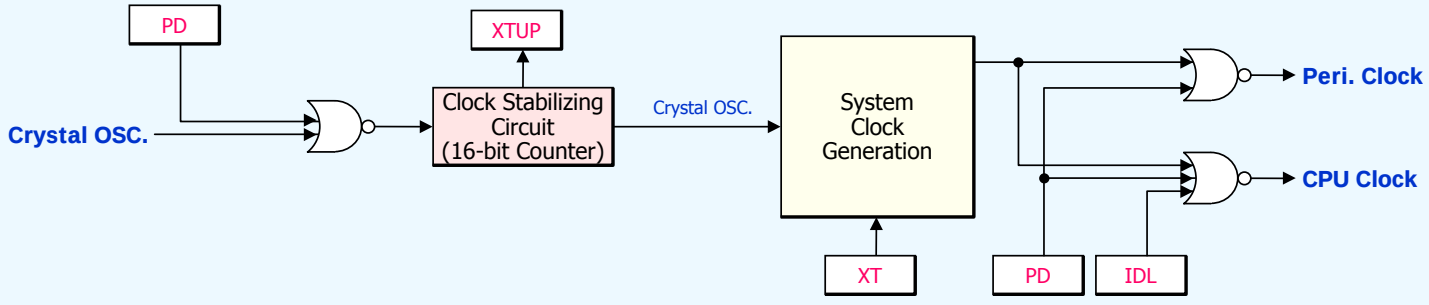
-	-	-	XTUP	-	-	-	-
			R(0)				

✓ **PMR** (C4h) : Power Management Control Register

-	-	-	-	-	ALEOFF	-	-
					R/W(0)		

✓ **PCON** (87h) : Power Control Register

SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R/W(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)



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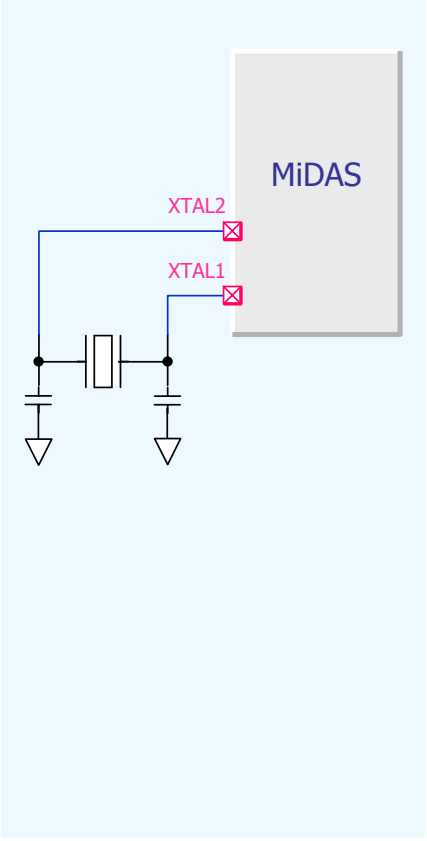
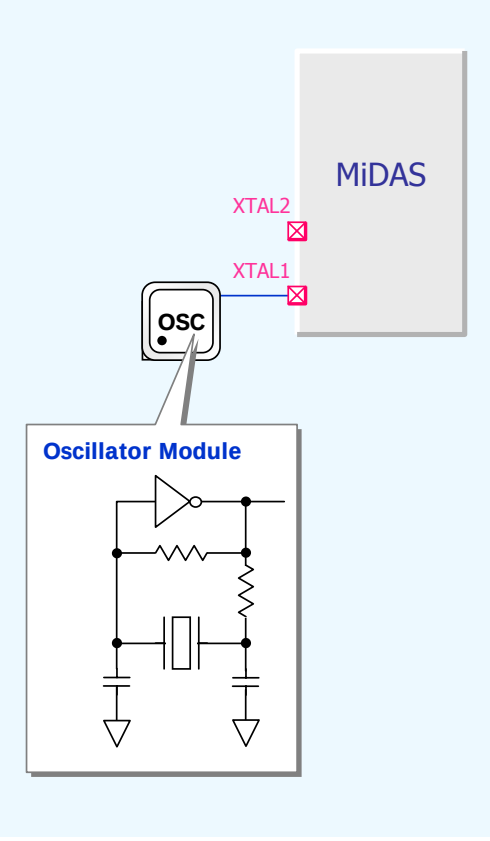
6.15. Clock Circuit : Guideline for Configuration

◆ **Crystal Oscillator**



◆ **Oscillator Module**



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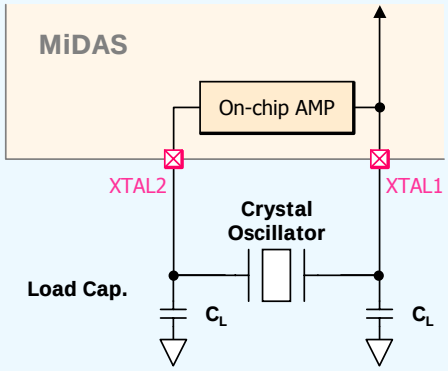
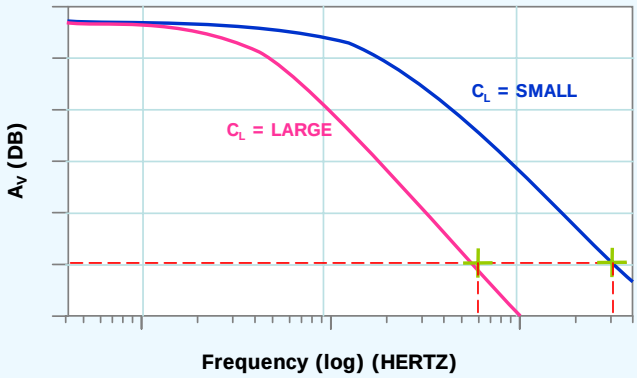
6.15. Clock Circuit: Guideline for Using a Crystal

◆ Crystal Oscillator & Load Capacitors



◆ Graph for Load Capacitor & Frequency



◆ Recommended C_L (Load Capacitor)

V_{DD} = 5 V

	Crystal Oscillator [MHz]		
	~ 11.0592	22.1184	30.0000
Load Cap. C_L	47pF	20pF	10pF

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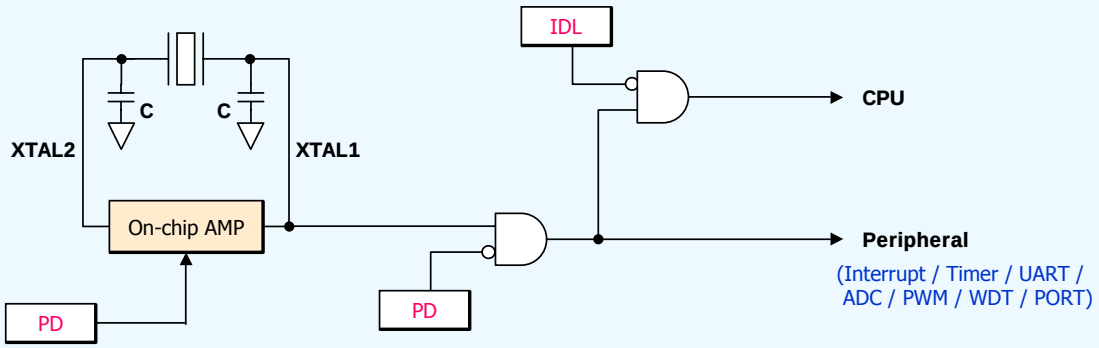
6.16. Power Management : 3 Modes

- **Active Mode** : The CPU and The Peripherals operate.
- **Idle Mode** : The CPU is gated off from the clock signal.
  Only the Peripherals operate.
  - ✓ Exited by activating any interrupt. The CPU resumes.
  - ✓ Exited by activating any reset. The CPU restarts.
- **Stop Mode** : All clocks are stopped.
  All activity is completely stopped.
  - ✓ Exited by activating external interrupt 0 or 1 (level detect) The CPU resumes.
    External pins must hold '0' during at least crystal stabilization time.
  - ✓ Exited by activating any reset. The CPU restarts.

✓ **PCON** (87h) : Power Control Register

SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R/W(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- PD : Stop Mode (Power-down) bit.
- IDL : IDLE Mode bit.



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6.17. EPROM

- Programming & verify timing is very similar to that of Intel 87C52.
- Write Voltage : 11.5V ± 0.5V
- Write Pulse Width : Min. 100us ~ Max. 500us
- Erase Time : 20 minutes in UV-light (15mW/cm^2)
- 44-pin PLCC requires an additional adaptor.

[EPROM Cell Configuration In Physical Layout]

Main Cell (4K / 8Kbytes)
Encryption Cell (64 bytes)
Lock Bit Cell (3 bits)
Signature Cell (3 bytes)

ROM Writer Interface										Functional Description
Mode		RESET	$\overline{\text{PSEN}}$	ALE	VPP	P2.6	P2.7	P3.3	P3.6	P3.7	
Program Code Data		H	L	⎍	11.5V	L	H	H	H	H	VPP = 11.5V and ALE Low Pulse
Verify Code Data		H	L	H	5V	L	L	L	H	H	Code = (Main byte) XNOR (Encryption byte)
Program Encryption Array		H	L	⎍	11.5V	L	H	H	L	H	VPP = 11.5V and ALE Low Pulse
Program Lock Bits	Bit 1	H	L	⎍	11.5V	H	H	H	H	H	LOCK1 = 1 : MOVC Instruction Disable. Further Programming Disable.
	Bit 2	H	L	⎍	11.5V	H	H	H	L	L	LOCK2 = 1 : Same as LOCK1 and Verify Disable.
	Bit 3	H	L	⎍	11.5V	H	L	H	H	L	LOCK3 = 1 : Same as LOCK1 and LOCK2. External Code Execution Disable.
Read Signature		H	L	H	5V	L	L	L	L	L	30h = C0h (CORERIVER) 31h = 87h (Product) 60h = 52h (EPROM Size)

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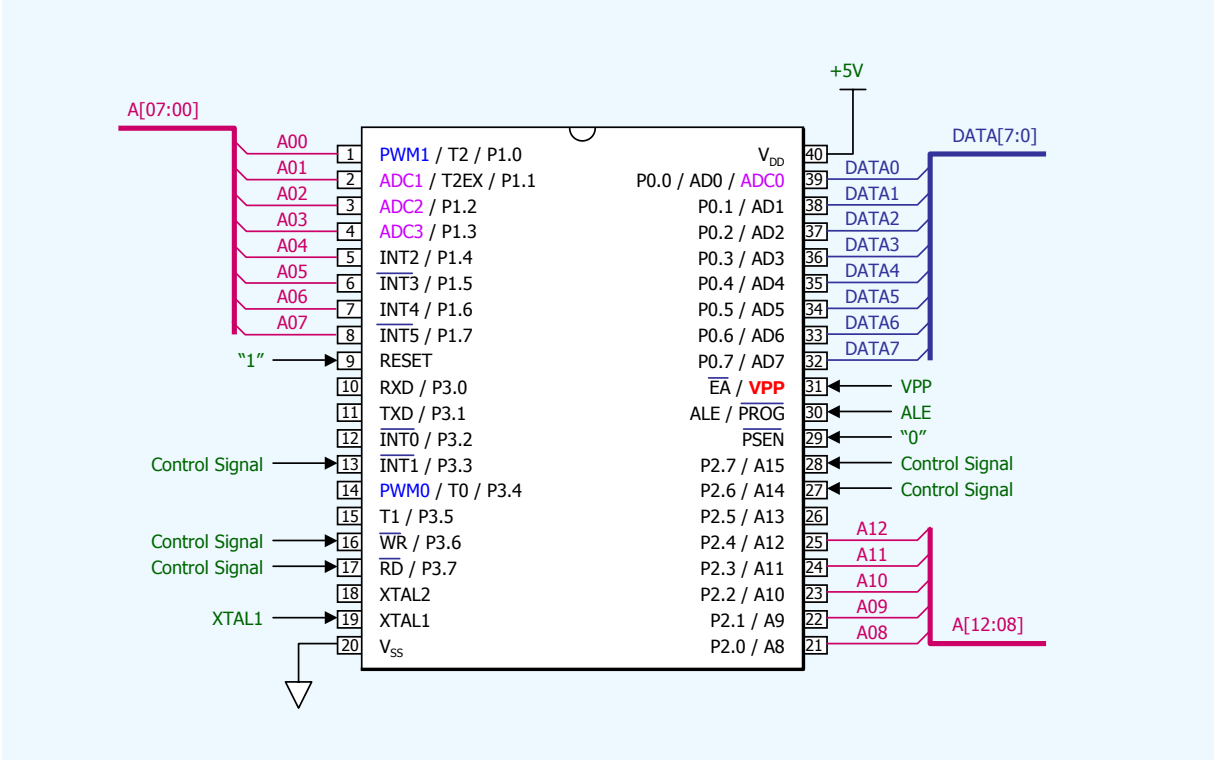
6.17. EPROM : Pin configuration



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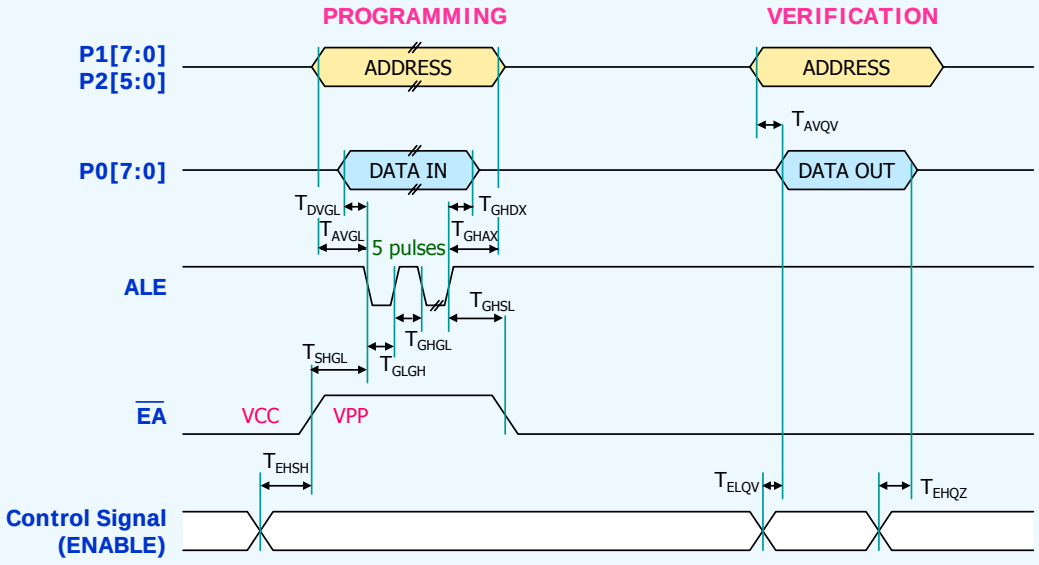
6.17. EPROM : Program & Verify Timing

*** Oscillator Frequency : Frequency = 4 ~ 6 MHz (T_{CLCL} = 1/Frequency)**

Parameter	Symbol	min.	Max.	Unit
Programming Supply Voltage	VPP	11.0	12.0	V
Programming Supply Current	IPP		75	mA
Address Setup to ALE Low	T_{AVGL}	48 T_{CLCL}		
Address hold after ALE High	T_{GHAX}	48 T_{CLCL}		
Data Setup to ALE Low	T_{DVGL}	48 T_{CLCL}		
Data Hold after ALE High	T_{GHDX}	48 T_{CLCL}		
ENABLE High to VPP	T_{EHSH}	48 T_{CLCL}		

Parameter	Symbol	min.	Max.	Unit
VPP Setup to ALE Low	T_{SHGL}	10		µs
VPP Hold after ALE High	T_{GHSL}	10		µs
ALE Low Width	T_{GLGH}	90	110	µs
Address to Data Valid	T_{AVQV}		48 T_{CLCL}	
ENABLE Low to Data Valid	T_{ELQV}		48 T_{CLCL}	
Data Float after ENABLE	T_{EHQZ}	0	48 T_{CLCL}	
ALE High to ALE Low	T_{GHGL}	10		µs



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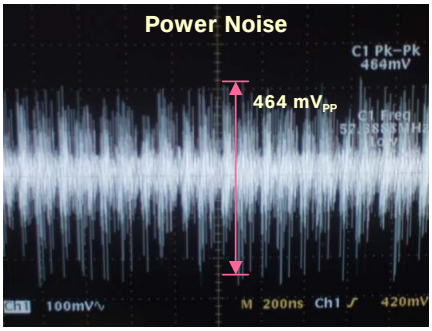
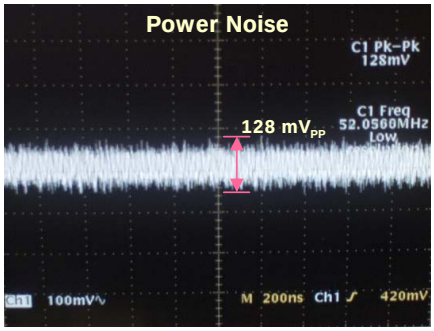
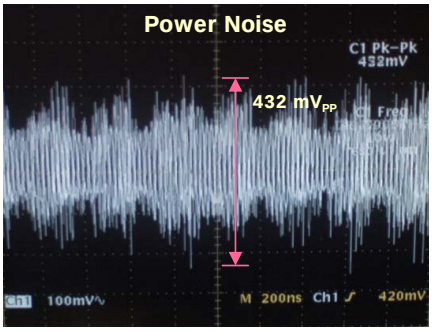
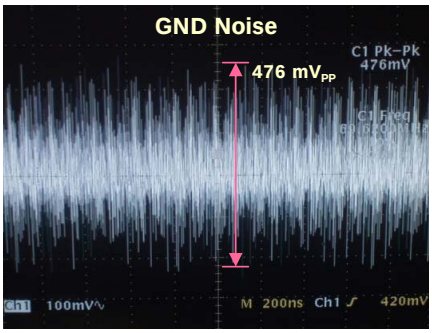
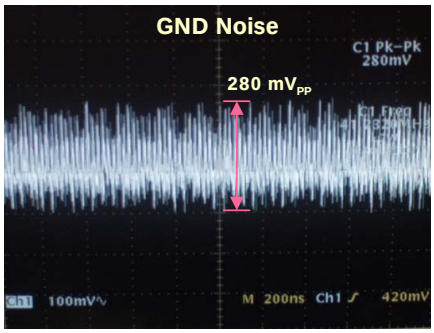
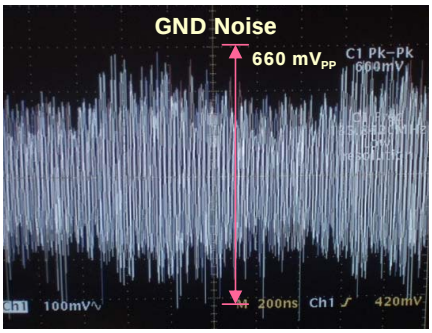
7. Strong Point I : Noise Reduction

Clock : 22.1184 MHz

MiDAS1.0 : ALE "ON"	MiDAS1.0 : ALE "OFF"	Company A's 80C52
		
		

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7. Strong Point I : Noise Reduction (Cont'd)

System Clock [MHz]	Noise	MiDAS1.0		Company A's 80C52
		ALE "ON"	ALE "OFF"	ALE always "ON"
11.0592	Power	410 mV_{PP}	**170 mV_{PP}**	360 mV_{PP}
	Ground	550 mV_{PP}	**330 mV_{PP}**	500 mV_{PP}
22.1184	Power	464 mV_{PP}	**128 mV_{PP}**	432 mV_{PP}
	Ground	476 mV_{PP}	**280 mV_{PP}**	640 mV_{PP}
6	Power	360 mV_{PP}	**170 mV_{PP}**	380 mV_{PP}
	Ground	500 mV_{PP}	**330 mV_{PP}**	480 mV_{PP}

- MiDAS1.0 can reduce EMI by removing the needless swing of ALE signal.
- You can enable/disable ALE signal by changing the value of ALEOFF bit (SFR PMR.2).
- Or can reduce system cost by removing needless decoupling capacitors while maintaining the EMI.

* This experimental results can vary according to design style of an application system.

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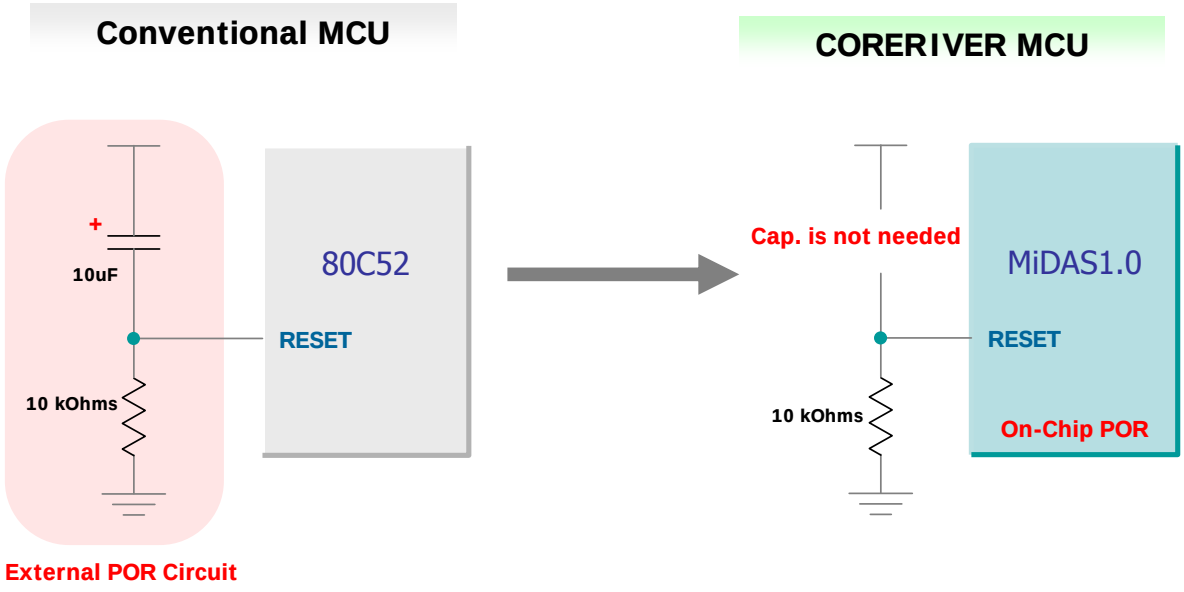
7. Strong Point II : On-Chip POR



- On-Chip POR (Power On Reset) can reduce system cost by removing a needless capacitor.
- The states of all ports will not be determined until the POR procedure ends.

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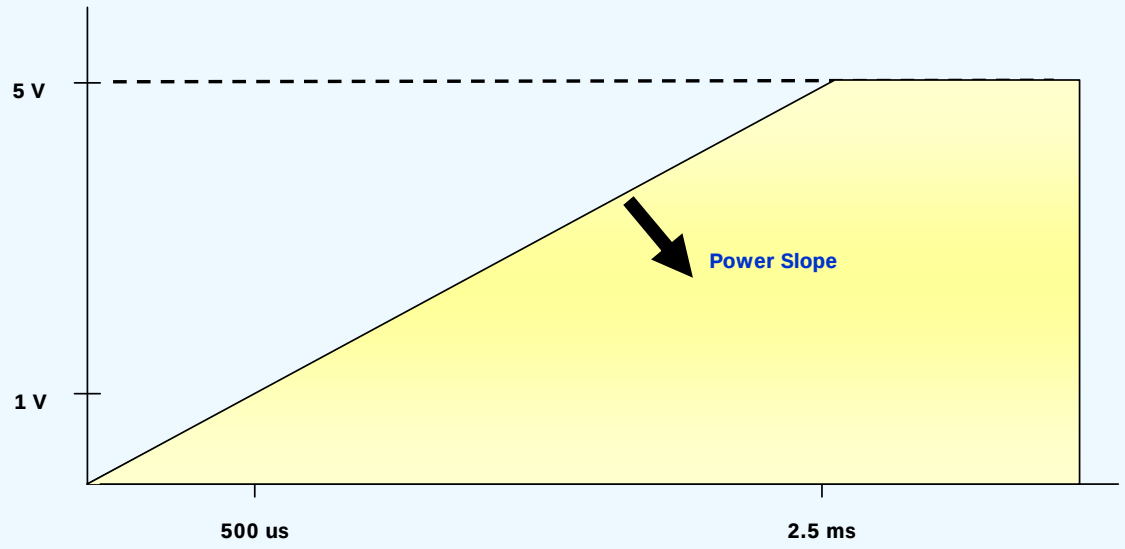
8. Recommended Power Slope

- The supply voltage slope must be in the range from 0.0V/us to 1.0V/500us. (5V/2.5ms)
  (That is, the supply voltage should be increasing monotonically until it reaches to the normal range.)



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9. Absolute Maximum Ratings

Items	Ranges
Voltage on any pin relative to Ground	-0.3V to (V_{DD}+0.5V)
Voltage in V_{DD} relative to Ground	-0.3V to 6.0V
Output Voltage	-0.3V to (V_{DD}+0.3V)
Operating Temperature	-20 ºC to 85 ºC
Storage Temperature	-55 ºC to +125 ºC
Soldering Temperature	160 ºC for 10 seconds

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10. DC Characteristics

*** TA = -20 ºC ~ +85 ºC, V_{DD} = 2.7V ~ 5.5V unless otherwise specified.**

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Input Low Voltage	V_{IL}	Except EA	V_{DD} = 2.7V~5.5V	-0.5	-	$0.2V_{DD}$-0.1	V
	V_{IL1}	EA		-0.5	-	$0.2V_{DD}$-0.3	
Input high Voltage	V_{IH}	ALE, PSEN, P0, P1, P2, P3, P4	V_{DD} = 2.7V~5.5V	2.0	-	V_{DD}+0.5	V
	V_{IH1}	EA, RESET, XTAL1		$0.7V_{DD}$	-	V_{DD}+0.5	
Output Low Voltage	V_{OL}	P1, P2, P3, P4	V_{DD} = 2.7V~5.5V(I_{OL} = 1.6mA)	-	-	0.45	V
	V_{OL1}	P0, ALE, PSEN	V_{DD} = 2.7V~5.5V(I_{OL} = 3.2mA)	-	-	0.45	
Output High Voltage	V_{OH}	P1, P2, P3, P4	V_{DD} = 2.7V~5.5V (I_{OH}=-60uA)	$0.75V_{DD}$	-	-	V
			V_{DD} = 2.7V~5.5V (I_{OH}=-25uA)	$0.76V_{DD}$	-	-	
			V_{DD} = 2.7V~5.5V (I_{OH}=-10uA)	$0.78V_{DD}$	-	-	
	V_{OH1}	ALE, PSEN, P0 (External Access)	V_{DD} = 2.7V~5.5V(I_{OH}=-800uA)	$0.75V_{DD}$	-	-	V
			V_{DD} = 2.7V~5.5V(I_{OH}=-300uA)	$0.78V_{DD}$	-	-	
			V_{DD} = 2.7V~5.5V(I_{OH}=-80uA)	$0.8V_{DD}$	-	-	
Logical 0 Input Current	I_{IL}	P0, P1, P2, P3, P4	V_{DD} = 5.5V(V_{IN}=0.45V)	-	-	-1	μA
Logical 1 to 0 Transition Current	I_{TL}	P0, P1, P2, P3, P4	V_{DD} = 5V±10% (V_{IN}=2V)	-	-	-650	μA
Input Leakage Current	I_{IL}	All pin except XTAL1,XTAL2	V_{IN} = V_{IH} or V_{IL}	-	-	±1	μA
Reset Pull-down Resistor	R_{RST}	RESET	-	25	-	100	kΩ
Pin Capacitance	C_{IO}	All	V_{DD} = 5V	-	10	-	pF

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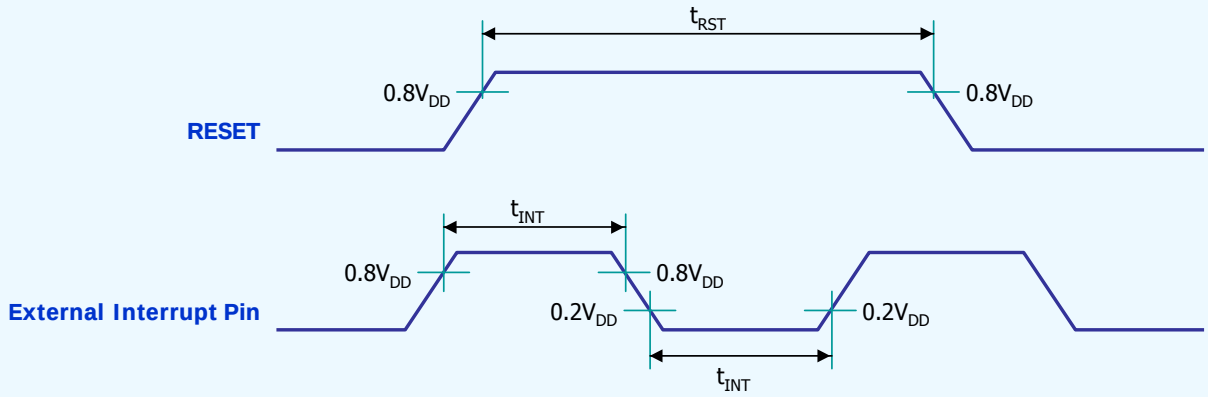
11. AC Characteristics

*** TA = -20 ºC ~ +85 ºC unless otherwise specified.**

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Operating Frequency	F_{OSC}	XTAL1, XTAL2	V_{DD} = 5V ± 10%	1	-	40	MHz
			V_{DD} = 3V ± 10%	1	-	20	
RESET Input Width	t_{RST}	RESET	V_{DD} = 5V ± 10%	24	-	-	F_{OSC}
			V_{DD} = 3V ± 10%	24	-	-	
External Interrupt Input Width	t_{INT}	External Interrupt	V_{DD} = 5V ± 10%	4	-	-	F_{OSC}
			V_{DD} = 3V ± 10%	4	-	-	



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12. ADC Specifications

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Supply Voltage		V_{DDADC}	-	2.7	-	5.5	V
Input Voltage		V_{INADC}	-	V_{SS}	-	V_{DD}	V
Resolution		RES_{ADC}	-	-	9	-	bit
Operating Frequency		F_{ADC}	V_{DD} = 4.5V ~ 5.5V V_{DD} = 2.7V ~ 3.3V	-	-	10 5	MHz
Conversion Time		t_{ADC}	-	-	88 / F_{ADC}	-	s
Overall Accuracy		OA_{ADC}	V_{DD} =5V, F_{ADC}=10MHz V_{DD} =3V, F_{ADC}=5MHz	-	±2	±4	LSB
Integral Nonlinearity		INL_{ADC}	V_{DD} =5V, F_{ADC}=10MHz V_{DD} =3V, F_{ADC}=5MHz	-	±2	±4	LSB
Differential Nonlinearity		DNL_{ADC}	V_{DD} =5V, F_{ADC}=10MHz V_{DD} =3V, F_{ADC}=5MHz	-	±0.5	±1	LSB
Zero Input Error		ZIE_{ADC}	V_{DD} =5V, F_{ADC}=10MHz V_{DD} =3V, F_{ADC}=5MHz	-	±2	±4	LSB
Full Scale Error		FSE_{ADC}	V_{DD} =5V, F_{ADC}=10MHz V_{DD} =3V, F_{ADC}=5MHz	-	±2	±4	LSB
Analog Input Capacitance		C_{INADC}	-	-	10	15	pF
ADC Current	Active	I_{ADC}	V_{DD} = 5V, F_{ADC}=10MHz	-	1	2	mA
			V_{DD} = 3V, F_{ADC}=5MHz	-	0.3	0.6	
	Power-down		V_{DD} = 5V	-		500	nA

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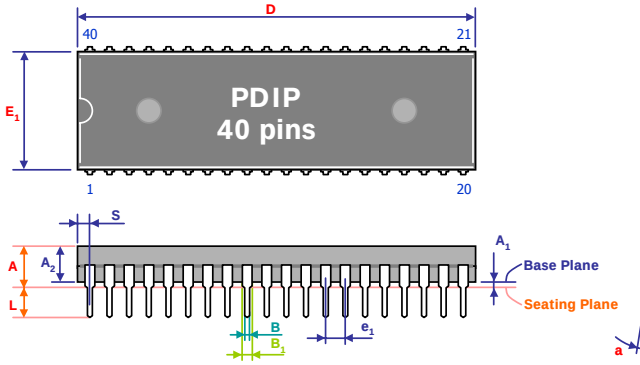
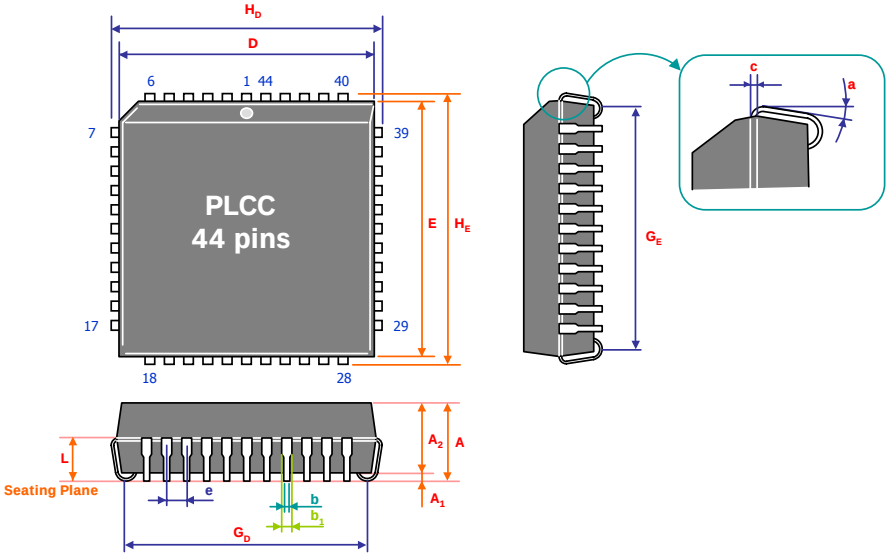
13. Package Dimensions : 40-PDIP & 44-PLCC



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.200	-	-	5.080
A_1	0.015	-	-	0.381	-	-
A_2	0.150	0.155	0.160	3.810	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.045	0.055	0.065	1.143	1.397	1.651
c	0.008	0.010	0.012	0.203	0.254	0.356
D	2.045	2.055	2.075	51.943	52.197	52.705
E	0.590	0.600	0.610	14.986	15.240	15.494
E_1	0.530	0.545	0.550	13.720	13.840	13.970
e_1	0.090	0.100	0.110	2.286	2.540	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0°	-	15°	0°	-	15°
e_A	0.630	0.650	0.670	16.000	16.510	17.010
S	-	-	0.090	-	-	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar Burns.
2. Dimension E_1 dose not include interlead flash.
3. Dimension D & E_1 include mold mismatch and are determined at the mold parting line.
4. Dimension B_1 does not include dambar protrusion/intrusion.
5. General appearance spec. should be based on final visual inspection spec.



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.165	-	0.180	4.191	-	4.572
A_1	0.020	-	-	0.508	-	-
A_2	0.145	0.150	0.155	3.683	3.810	3.937
b_1	0.026	0.028	0.032	0.660	0.711	0.813
b	0.013	0.017	0.021	0.330	0.432	0.533
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.650	0.658	16.460	16.510	16.710
E	0.648	0.650	0.658	16.460	16.510	16.710
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.986	15.494	16.002
G_E	0.590	0.610	0.630	14.986	15.494	16.002
H_D	0.680	0.690	0.700	17.272	17.526	17.780
H_E	0.680	0.690	0.700	17.272	17.526	17.780
L	0.090	0.100	0.120	2.296	2.540	3.048

Notes:
1. Dimension D * E do not include interlead flash.
2. Dimension b_1 dose not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

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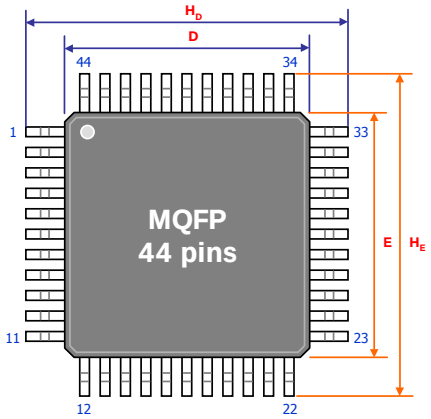
13. Package Dimensions : 44-MQFP

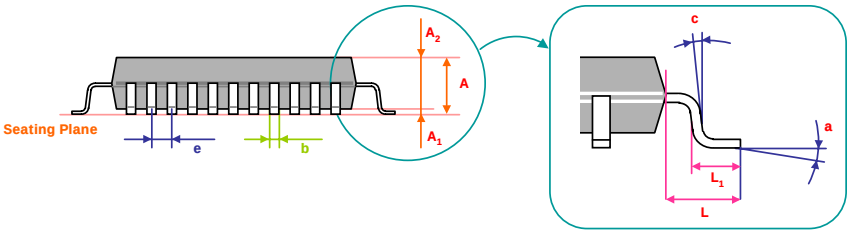


[44-MQFP]

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.091	-	-	2.30
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.077	0.081	0.085	1.95	2.05	2.15
b	0.012	0.015	0.018	0.30	0.37	0.45
D	0.394 BSC			10.00 BSC		
E	0.394 BSC			10.00 BSC		
e	0.031 BSC			0.80 BSC		
H_D	0.520 BSC			13.20 BSC		
H_E	0.520 BSC			13.20 BSC		
L	-	0.063	-	-	1.60	-
L_1	0.024	0.031	0.039	0.60	0.80	1.00
a	0°	-	8°	0°	-	8°
c	0°	-	-	0°	-	-

Notes:

1. Dimension D * E do not include interlead flash.
2. Controlling dimension: Inches
3. General appearance spec. should be based on final visual inspection spec.



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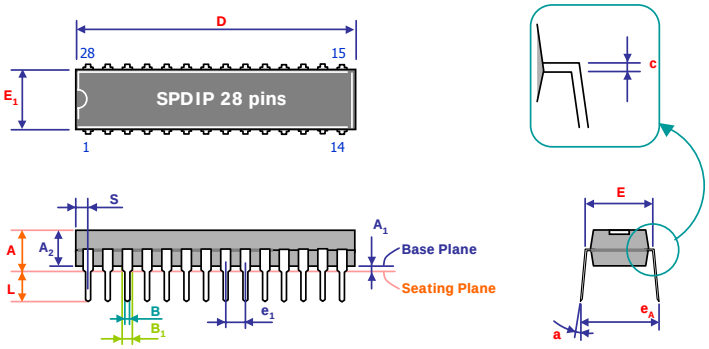
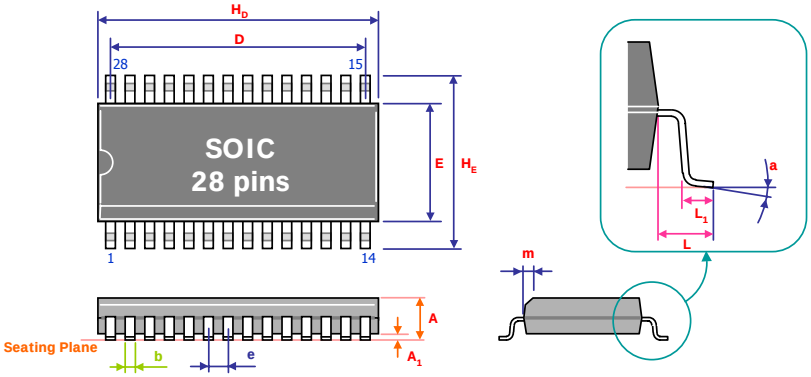
13. Package Dimensions : 28-SPDIP/SOIC



[28-SPDIP]

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.200	-	-	5.080
A_1	0.015	-	-	0.381	-	-
A_2	0.150	0.155	0.160	3.810	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.045	0.055	0.065	1.143	1.397	1.651
c	0.008	0.010	0.012	0.203	0.254	0.356
D	1.445	1.455	1.475	36.703	36.907	37.465
E	0.290	0.300	0.310	7.366	7.62	7.874
E_1	0.530	0.545	0.550	13.720	13.840	13.970
e_1	0.090	0.100	0.110	2.286	2.540	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0°	-	15°	0°	-	15°
e_A	0.330	0.350	0.370	8.382	8.89	9.398
S	-	-	0.090	-	-	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar Burns.
2. Dimension E_1 dose not include interlead flash.
3. Dimension D & E_1 include mold mismatch and are determined at the mold parting line.
4. Dimension B_1 does not include dambar protrusion/intrusion.
5. General appearance spec. should be based on final visual inspection spec.



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.093	0.099	0.104	2.35	2.45	2.65
A_1	0.004	0.008	0.012	0.10	0.20	0.30
b	0.014	0.016	0.019	0.35	0.42	0.49
D	-	0.65	-	-	16.51	-
E	0.291	0.295	0.299	7.40	7.50	7.60
H_D	0.697	0.705	0.713	17.70	17.90	18.10
H_E	0.404	0.411	0.419	10.26	10.45	10.65
L	0.057	0.058	0.060	1.43	1.48	1.53
L_1	0.034	0.038	0.042	0.86	0.96	1.07
a	0°	-	8°	0°	-	8°
e	0.050 BSC			1.27 BSC		
m	0.020	0.025	0.030	0.50	0.62	0.75

Notes:
1. Dimension D Max. & S include mold flash or tie bar Burns.
2. Dimension E_1 dose not include interlead flash.
3. Dimension D & E_1 include mold mismatch and are determined at the mold parting line.
4. Dimension B_1 does not include dambar protrusion/intrusion.
5. General appearance spec. should be based on final visual inspection spec.

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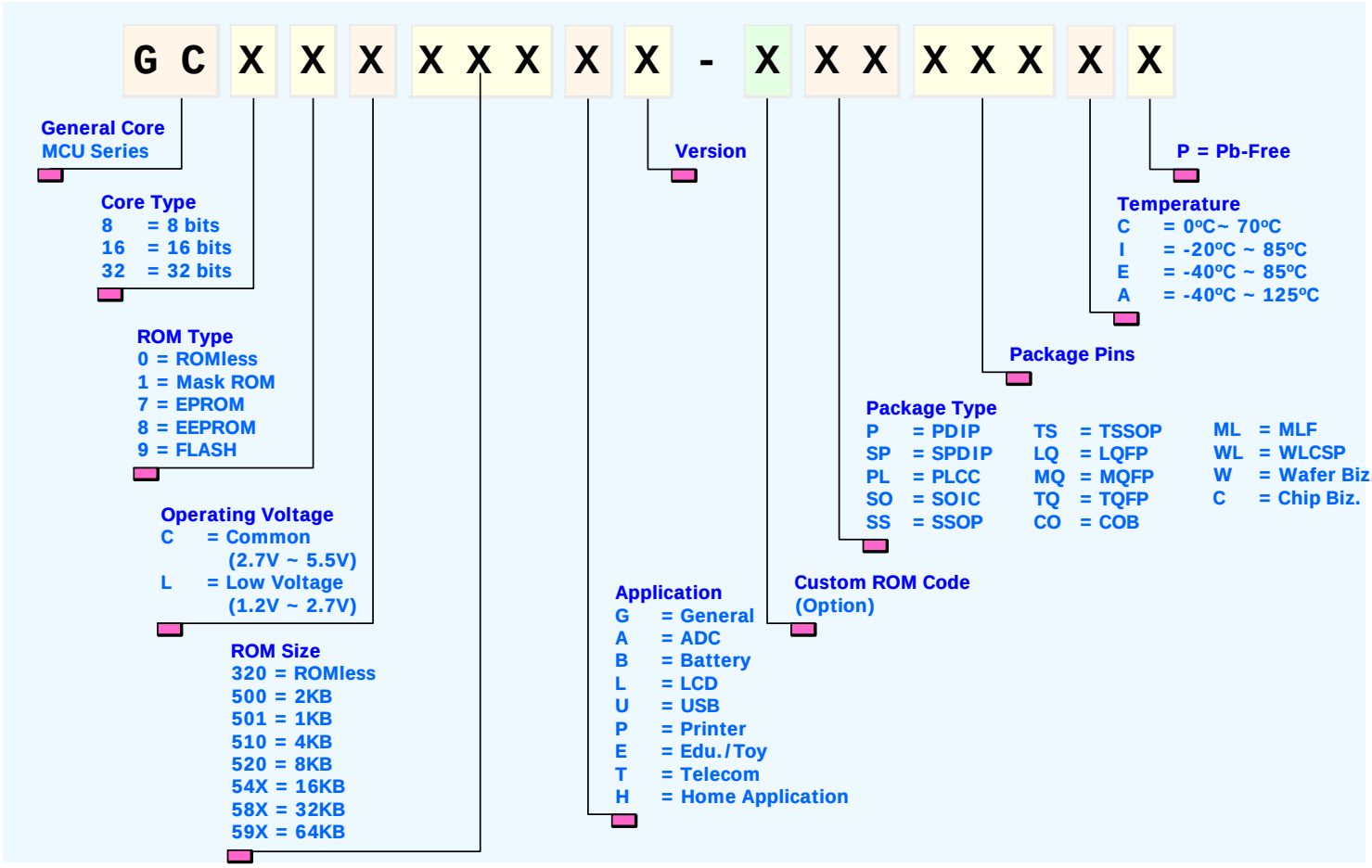
14. Product Numbering System



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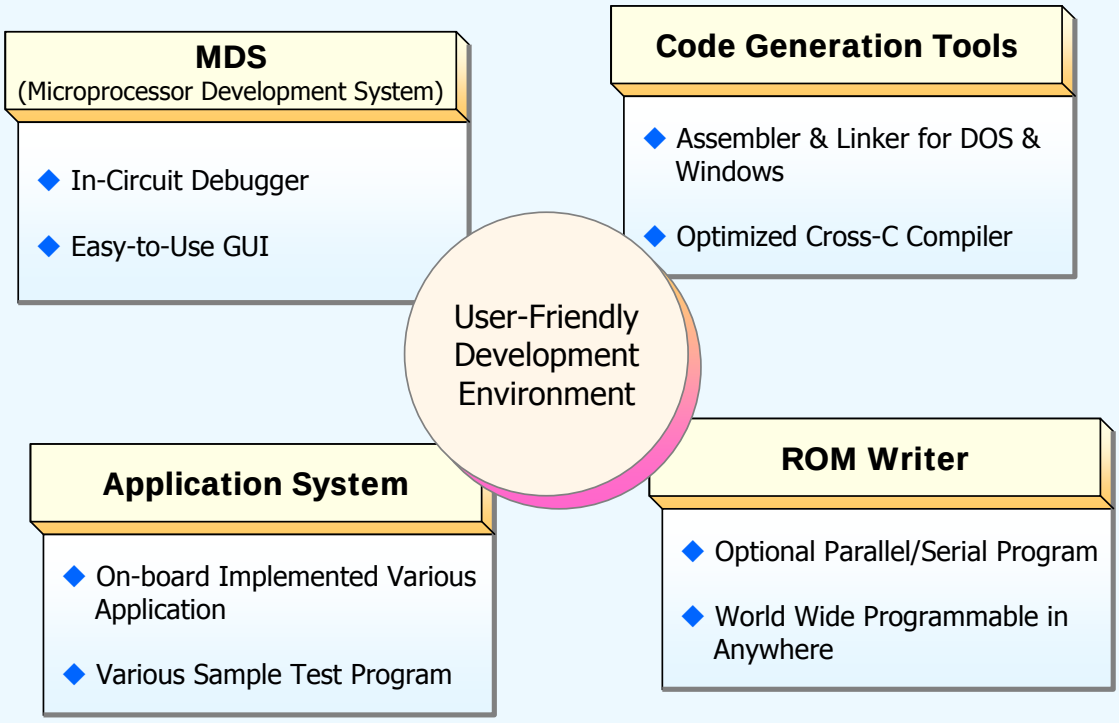
15. Supporting tools



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Appendix A : instruction set (1/18)

ADD A, <src-byte>

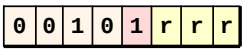
1 cycle = 4 clocks

Add

ADD A, Rn

Operation : (A) ← (A) + (Rn)

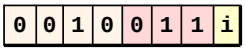
Encoding : HEX: 28h, #bytes: 1, Cycles: 1



ADD A, @Ri

Operation : (A) ← (A) + ((Ri))

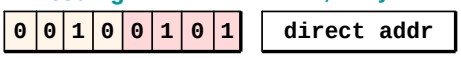
Encoding : HEX: 26h, #bytes: 1, Cycles: 1



ADD A, direct

Operation : (A) ← (A) + (direct)

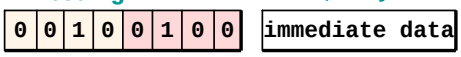
Encoding : HEX: 25h, #bytes: 2, Cycles: 2



ADD A, #date

Operation : (A) ← (A) + data

Encoding : HEX: 24h, #bytes: 2, Cycles: 2



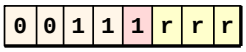
ADDC A, <src-byte>

Add with Carry

ADDC A, Rn

Operation : (A) ← (A) + (C) + (Rn)

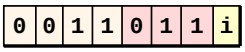
Encoding : HEX: 38h, #bytes: 1, Cycles: 1



ADDC A, @Ri

Operation : (A) ← (A) + (C) + ((Ri))

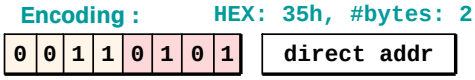
Encoding : HEX: 36h, #bytes: 1, Cycles: 1



ADDC A, direct

Operation : (A) ← (A) + (C) + (direct)

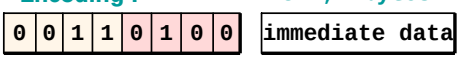
Encoding : HEX: 35h, #bytes: 2, Cycles: 2



ADDC A, #date

Operation : (A) ← (A) + (C) + data

Encoding : HEX: 34h, #bytes: 2, Cycles: 2



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Appendix A : instruction set (2/18)

SUBB A, <src-byte>

Subtract with Borrow

SUBB A, Rn

Operation : (A) ← (A) - (C) - (Rn)

Encoding : HEX: 98h, #bytes: 1, Cycles: 1

1	0	0	1	1	r	r	r

SUBB A, @Ri

Operation : (A) ← (A) - (C) - ((Ri))

Encoding : HEX: 96h, #bytes: 1, Cycles: 1

1	0	0	1	0	1	1	i

SUBB A, direct

Operation : (A) ← (A) - (C) - (direct)

Encoding : HEX: 95h, #bytes: 2, Cycles: 2

1	0	0	1	0	1	0	1	direct addr

SUBB A, #date

Operation : (A) ← (A) - (C) - data

Encoding : HEX: 94h, #bytes: 2, Cycles: 2

1	0	0	1	0	1	0	0	immediate data

INC <byte>

Increment

INC A

Operation : (A) ← (A) + 1

Encoding : HEX: 04h, #bytes: 1, Cycles: 1

0	0	0	0	0	1	0	0

INC Rn

Operation : (Rn) ← (Rn) + 1

Encoding : HEX: 08h, #bytes: 1, Cycles: 1

0	0	0	0	1	r	r	r

INC @Ri

Operation : ((Ri)) ← ((Ri)) + 1

Encoding : HEX: 06h, #bytes: 1, Cycles: 1

0	0	0	0	0	1	1	i

INC direct

Operation : (direct) ← (direct) + 1

Encoding : HEX: 05h, #bytes: 2, Cycles: 2

0	0	0	0	0	1	0	1	direct addr

INC DPTR

Operation : (DPTR) ← (DPTR) + 1

Encoding : HEX: A3h, #bytes: 1, Cycles: 1

1	0	1	0	0	0	1	1

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Appendix A : instruction set (3/18)

DEC <byte>

Decrement

DEC A

Operation : (A) ← (A) - 1

Encoding : HEX: 14h, #bytes: 1, Cycles: 1

0	0	0	1	0	1	0	0

DEC Rn

Operation : (Rn) ← (Rn) - 1

Encoding : HEX: 18h, #bytes: 1, Cycles: 1

0	0	0	1	1	r	r	r

DEC @Ri

Operation : ((Ri)) ← ((Ri)) - 1

Encoding : HEX: 16h, #bytes: 1, Cycles: 1

0	0	0	1	0	1	1	i

DEC direct

Operation : (direct) ← (direct) - 1

Encoding : HEX: 15h, #bytes: 1, Cycles: 1

0	0	0	1	0	1	0	1

direct addr

DEC DPTR

Operation : (DPTR) ← (DPTR) - 1

Encoding : HEX: A5h, #bytes: 1, Cycles: 1

1	0	1	0	0	1	0	1

MUL AB

Multiply

Operation : $(A)_{7-0}$ $(B)_{15-8}$ ← (A) x (B)

Encoding : HEX: A4h, #bytes: 1, Cycles: 3

1	0	1	0	0	1	0	0

DIV AB

Divide

Operation : $(A)_{15-8}$ $(B)_{7-0}$ ← (A) / (B)

Encoding : HEX: 84h, #bytes: 1, Cycles: 3

1	0	0	0	0	1	0	0

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Appendix A : instruction set (4/18)

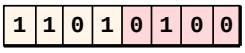
DA A

Decimal-adjust Accumulator for Addition

Operation :

IF [[(A_{3-0})>9] ∨ [(AC)=1]]
THEN (A_{3-0}) ← (A_{3-0})+6
IF [[(A_{7-4})>9] ∨ [(C)=1]]
THEN (A_{7-4}) ← (A_{7-4})+6

Encoding : HEX: D4h, #bytes: 1, Cycles: 1



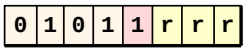
ANL <dest-byte>, <src-byte>

Logical AND for byte variables

ANL A, Rn

Operation : (A) ← (A) ^ (Rn)

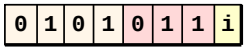
Encoding : HEX: 58h, #bytes: 1, Cycles: 1



ANL A, @Ri

Operation : (A) ← (A) ^ ((Ri))

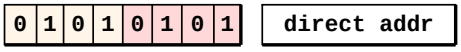
Encoding : HEX: 56h, #bytes: 1, Cycles: 1



ANL A, direct

Operation : (A) ← (A) ^ (direct)

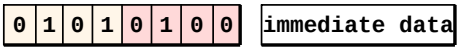
Encoding : HEX: 55h, #bytes: 2, Cycles: 2



ANL A, #date

Operation : (A) ← (A) ^ data

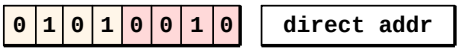
Encoding : HEX: 54h, #bytes: 2, Cycles: 2



ANL direct, A

Operation : (direct) ← (direct) ^ (A)

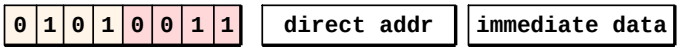
Encoding : HEX: 52h, #bytes: 2, Cycles: 2



ANL direct, #data

Operation : (direct) ← (direct) ^ data

Encoding : HEX: 53h, #bytes: 3, Cycles: 3



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Appendix A : instruction set (5/18)

ANL C, <src-bit>

Logical AND for bit variables

ANL C, bit

Operation : (C) ← (C) ^ (bit)

Encoding : HEX: 82h, #bytes: 2, Cycles: 2

1	0	0	0	0	0	1	0	bit addr

ANL C, /bit

Operation : (C) ← (C) ^ ~(bit)

Encoding : HEX: B0h, #bytes: 2, Cycles: 2

1	0	1	1	0	0	0	0	bit addr

ORL <dest-byte>, <src-byte>

Logical OR for byte variables

ORL A, Rn

Operation : (A) ← (A) ∨ (Rn)

Encoding : HEX: 48h, #bytes: 1, Cycles: 1

0	1	0	0	1	r	r	r

ORL A, @Ri

Operation : (A) ← (A) ∨ ((Ri))

Encoding : HEX: 46h, #bytes: 1, Cycles: 1

0	1	0	0	0	1	1	i

ORL A, direct

Operation : (A) ← (A) ∨ (direct)

Encoding : HEX: 45h, #bytes: 2, Cycles: 2

0	1	0	0	0	1	0	1	direct addr

ORL A, #date

Operation : (A) ← (A) ∨ data

Encoding : HEX: 44h, #bytes: 2, Cycles: 2

0	1	0	0	0	1	0	0	immediate data

ORL direct, A

Operation : (direct) ← (direct) ∨ (A)

Encoding : HEX: 42h, #bytes: 2, Cycles: 2

0	1	0	0	0	0	1	0	direct addr

ORL direct, #data

Operation : (direct) ← (direct) ∨ data

Encoding : HEX: 43h, #bytes: 3, Cycles: 3

0	1	0	0	0	0	1	1	direct addr	immediate data

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Appendix A : instruction set (6/18)

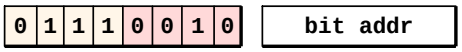
ORL C, <src-byte>

Logical OR for byte variables

ORL C, bit

Operation : (C) ← (C) ∨ (bit)

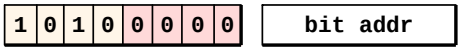
Encoding : HEX: 72h, #bytes: 2, Cycles: 2



ORL C, /bit

Operation : (C) ← (C) ∨ ~(bit)

Encoding : HEX: A0h, #bytes: 2, Cycles: 2



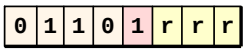
XRL <dest-byte>, <src-byte>

Logical Exclusive-OR for byte variables

XRL A, Rn

Operation : (A) ← (A) ⊕ (Rn)

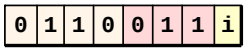
Encoding : HEX: 68h, #bytes: 1, Cycles: 1



XRL A, @Ri

Operation : (A) ← (A) ⊕ ((Ri))

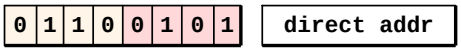
Encoding : HEX: 66h, #bytes: 1, Cycles: 1



XRL A, direct

Operation : (A) ← (A) ⊕ (direct)

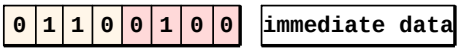
Encoding : HEX: 65h, #bytes: 2, Cycles: 2



XRL A, #date

Operation : (A) ← (A) ⊕ data

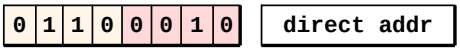
Encoding : HEX: 64h, #bytes: 2, Cycles: 2



XRL direct, A

Operation : (direct) ← (direct) ⊕ (A)

Encoding : HEX: 62h, #bytes: 2, Cycles: 2



XRL direct, #data

Operation : (direct) ← (direct) ⊕ data

Encoding : HEX: 63h, #bytes: 3, Cycles: 3

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Appendix A : instruction set (7/18)

CLR A

Clear Accumulator

Operation : (A) ← 0

Encoding : HEX: E4h, #bytes: 1, Cycles: 1

1	1	1	0	0	1	0	0

CLR <bit>

Clear bit

CLR C

Operation : (C) ← 0

Encoding : HEX: C3h, #bytes: 1, Cycles: 1

1	1	0	0	0	0	1	1

CLR bit

Operation : (bit) ← 0

Encoding : HEX: C2h, #bytes: 2, Cycles: 2

1	1	0	0	0	0	1	0	bit addr

CPL A

Complement Accumulator

Operation : (A) ← ~(A)

Encoding : HEX: F4h, #bytes: 1, Cycles: 1

1	1	1	1	0	1	0	0

CPL <bit>

Complement bit

CPL C

Operation : (C) ← ~(C)

Encoding : HEX: B3h, #bytes: 1, Cycles: 1

1	0	1	1	0	0	1	1

CPL bit

Operation : (bit) ← ~(bit)

Encoding : HEX: B2h, #bytes: 2, Cycles: 2

1	0	1	1	0	0	1	0	bit addr

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Appendix A : instruction set (8/18)

RL A

Rotate Accumulator Left

Operation :
$(A_{n+1}) \leftarrow (A_n)$ n=0~6
$(A_0) \leftarrow (A_7)$

Encoding : HEX: 23h, #bytes: 1, Cycles: 1

0	0	1	0	0	0	1	1

RLC A

Rotate Accumulator Left through the Carry flag

Operation :
$(A_{n+1}) \leftarrow (A_n)$ n=0~6
$(A_0) \leftarrow (C)$
$(C) \leftarrow (A_7)$

Encoding : HEX: 33h, #bytes: 1, Cycles: 1

0	0	1	1	0	0	1	1

RR A

Rotate Accumulator Right

Operation :
$(A_n) \leftarrow (A_{n+1})$ n=0~6
$(A_7) \leftarrow (A_0)$

Encoding : HEX: 03h, #bytes: 1, Cycles: 1

0	0	0	0	0	0	1	1

RRC A

Rotate Accumulator Right through the Carry flag

Operation :
$(A_n) \leftarrow (A_{n+1})$ n=0~6
$(A_7) \leftarrow (C)$
$(C) \leftarrow (A_0)$

Encoding : HEX: 13h, #bytes: 1, Cycles: 1

0	0	0	1	0	0	1	1

SWAP A

Swap nibbles within the Accumulator

Operation : $(A_{3-0}) \leftrightarrow (A_{7-4})$

Encoding : HEX: C4h, #bytes: 1, Cycles: 1

1	1	0	0	0	1	0	0

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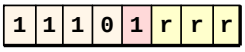
Appendix A : instruction set (9/18)

MOV <dest-byte>, <src-byte>

Move byte variable

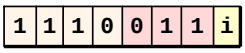
MOV A, Rn
Operation : (A) ← (Rn)

Encoding : HEX: E8h, #bytes: 1, Cycles: 1



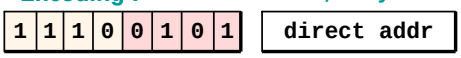
MOV A, @Ri
Operation : (A) ← ((Ri))

Encoding : HEX: E6h, #bytes: 1, Cycles: 1



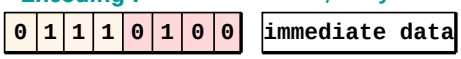
MOV A, direct
Operation : (A) ← (direct)

Encoding : HEX: E5h, #bytes: 2, Cycles: 2



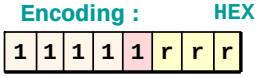
MOV A, #date
Operation : (A) ← data

Encoding : HEX: 74h, #bytes: 2, Cycles: 2



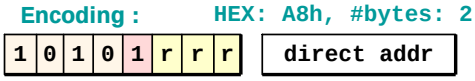
MOV Rn, A
Operation : (Rn) ← (A)

Encoding : HEX: F8h, #bytes: 1, Cycles: 1



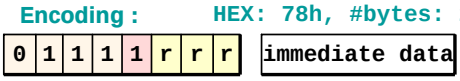
MOV Rn, direct
Operation : (Rn) ← (direct)

Encoding : HEX: A8h, #bytes: 2, Cycles: 2



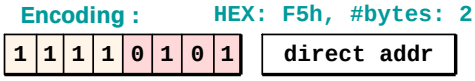
MOV Rn, #date
Operation : (Rn) ← data

Encoding : HEX: 78h, #bytes: 2, Cycles: 2



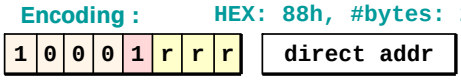
MOV direct, A
Operation : (direct) ← (A)

Encoding : HEX: F5h, #bytes: 2, Cycles: 2



MOV direct, Rn
Operation : (direct) ← (Rn)

Encoding : HEX: 88h, #bytes: 2, Cycles: 2



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Appendix A : instruction set (10 / 18)

MOV direct, @Ri

Operation : (direct) ← ((Ri))

Encoding : HEX: 86h, #bytes: 2, Cycles: 2

1	0	0	0	0	1	1	i	direct addr

MOV direct, direct

Operation : (direct) ← (direct)

Encoding : HEX: 85h, #bytes: 3, Cycles: 3

1	0	0	0	0	1	0	1	direct addr(src)	direct addr(dest)

MOV direct, #data

Operation : (direct) ← data

Encoding : HEX: 75h, #bytes: 3, Cycles: 3

0	1	1	1	0	1	0	1	direct addr	immediate data

MOV @Ri, A

Operation : ((Ri)) ← (A)

Encoding : HEX: F6h, #bytes: 1, Cycles: 1

1	1	1	1	0	1	1	i

MOV @Ri, direct

Operation : ((Ri)) ← (direct)

Encoding : HEX: A6h, #bytes: 2, Cycles: 2

1	0	1	0	0	1	1	i	direct addr

MOV @Ri, #data

Operation : ((Ri)) ← data

Encoding : HEX: 76h, #bytes: 2, Cycles: 2

0	1	1	1	0	1	1	i	immediate Data

MOV <dest-bit>, <src-bit>

Move bit data

MOV C, bit

Operation : (C) ← (bit)

Encoding : HEX: A2h, #bytes: 2, Cycles: 2

1	0	1	0	0	0	1	0	bit addr

MOV bit, C

Operation : (bit) ← (C)

Encoding : HEX: 92h, #bytes: 2, Cycles: 2

1	0	0	1	0	0	1	0	bit addr

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Appendix A : instruction set (11/18)

MOV DPTR, #data16

Load Data Pointer with a 16-bit constant

Operation :
(DPTR) ← $data_{15-0}$
(DPH,DPL) ← ($data_{15-8}$,$data_{7-0}$)

Encoding : HEX: 90h, #bytes: 3, Cycles: 3

1	0	0	1	0	0	0	0	immed. data 15-8	immed. data 7-0

MOVC A, @A + <base-reg>

Move Code byte

MOVC A, @A + DPTR

Operation : (A) ← ((A) + (DPTR))

Encoding : HEX: 93h, #bytes: 1, Cycles: 2

1	0	0	1	0	0	1	1

MOVC A, @A + PC

Operation :
(PC) ← (PC) + 1
(A) ← ((A) + (PC))

Encoding : HEX: 83h, #bytes: 1, Cycles: 2

1	0	0	0	0	0	1	1

MOVX <dest-byte>, <src-byte>

Move External

MOVX A, @Ri

Operation : (A) ← ((Ri))

Encoding : HEX: E2h, #bytes: 1, Cycles: 3

1	1	1	0	0	0	1	i

MOVX A, @DPTR

Operation : (A) ← ((DPTR))

Encoding : HEX: E0h, #bytes: 1, Cycles: 3

1	1	1	0	0	0	0	0

MOVX @Ri, A

Operation : ((Ri)) ← (A)

Encoding : HEX: F2h, #bytes: 1, Cycles: 3

1	1	1	1	0	0	1	i

MOVX @DPTR, A

Operation : ((DPTR)) ← (A)

Encoding : HEX: F0h, #bytes: 1, Cycles: 3

1	1	1	1	0	0	0	0

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Appendix A : instruction set (12/18)

XCH A, <src-byte>

Exchange Accumulator with byte variable

XCH A, Rn

Operation : (A) ↔ (Rn)

Encoding : HEX: C8h, #bytes: 1, Cycles: 1

1	1	0	0	1	r	r	r

XCH A, @Ri

Operation : (A) ↔ ((Ri))

Encoding : HEX: C6h, #bytes: 1, Cycles: 1

1	1	0	0	0	1	1	i

XCH A, direct

Operation : (A) ↔ (direct)

Encoding : HEX: C5h, #bytes: 2, Cycles: 2

1	1	0	0	0	1	0	1	direct addr

XCHD A, @Ri

Exchange Digit

Operation : $(A_{3\text{-}0}) \leftrightarrow ((Ri))_{3\text{-}0}$

Encoding : HEX: D6h, #bytes: 1, Cycles: 1

1	1	0	1	0	1	1	i

PUSH direct

Push onto stack

Operation :
(SP) ← (SP) + 1
((SP)) ← (direct)

Encoding : HEX: C0h, #bytes: 2, Cycles: 2

1	1	0	0	0	0	0	0	direct addr

POP direct

Pop onto stack

Operation :
(direct) ← ((SP))
(SP) ← (SP) – 1

Encoding : HEX: D0h, #bytes: 2, Cycles: 2

1	1	0	1	0	0	0	0	direct addr

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Appendix A : instruction set (13/18)

SETB <bit>

Set bit

SETB C

Operation : (C) ← 1

Encoding : HEX: D3h, #bytes: 1, Cycles: 1

1	1	0	1	0	0	1	1

SETB bit

Operation : (bit) ← 1

Encoding : HEX: D2h, #bytes: 2, Cycles: 2

1	1	0	1	0	0	1	0	bit addr

JC rel

Jump if Carry is set

Operation :
(PC) ← (PC) + 2
If (C) = 1, then (PC) ← (PC) + rel

Encoding : HEX: 40h, #bytes: 2, Cycles: 3

0	1	0	0	0	0	0	0	relative addr

JNC rel

Jump if Carry is not set

Operation :
(PC) ← (PC) + 2
If (C) = 0, then (PC) ← (PC) + rel

Encoding : HEX: 50h, #bytes: 2, Cycles: 3

0	1	0	1	0	0	0	0	relative addr

JB bit, rel

Jump if Bit is set

Operation :
(PC) ← (PC) + 3
If (bit) = 1, then (PC) ← (PC)+rel

Encoding : HEX: 20h, #bytes: 3, Cycles: 4

0	0	1	0	0	0	0	0	bit addr	relative addr

JNB bit, rel

Jump if Bit is not set

Operation :
(PC) ← (PC) + 3
If (bit) = 0, then (PC) ← (PC)+rel

Encoding : HEX: 30h, #bytes: 3, Cycles: 4

0	0	1	1	0	0	0	0	bit addr	relative addr

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Appendix A : instruction set (14/18)

JBC bit, rel

Jump if Bit is set and Clear bit

Operation :

```
(PC)   ← (PC) + 3
If (bit) = 1,
then (bit) ← 0, (PC) ← (PC) + rel
```

Encoding : HEX: 10h, #bytes: 3, Cycles: 4

0	0	0	1	0	0	0	0	bit addr	relative addr

ACALL addr11

Absolute Subroutine Call

Operation :

```
(PC)    ← (PC) + 2
(SP)    ← (SP) + 1
((SP))  ← (PC7-0)
(SP)    ← (SP) + 1
((SP))  ← (PC15-8)
(PC10-0)← page address
```

Encoding : HEX: 11h, #bytes: 2, Cycles: 3

a_{10}	a_9	a_8	1	0	0	0	1	a_{7-0}

LCALL addr16

Long Subroutine Call

Operation :

```
(PC)    ← (PC) + 3
(SP)    ← (SP) + 1
((SP))  ← (PC7-0)
(SP)    ← (SP) + 1
((SP))  ← (PC15-8)
(PC)    ← addr15-0
```

Encoding : HEX: 12h, #bytes: 3, Cycles: 4

0	0	0	1	0	0	1	0	a_{15-8}	a_{7-0}

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Appendix A : instruction set (15/18)

RET

Return from Subroutine

Operation :

$(PC_{15-8}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$
$(PC_{7-0}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$

Encoding : HEX: 22h, #bytes: 1, Cycles: 2

0	0	1	0	0	0	1	0

RETI

Return from Interrupt

Operation :

$(PC_{15-8}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$
$(PC_{7-0}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$

Encoding : HEX: 32h, #bytes: 1, Cycles: 2

0	0	1	1	0	0	1	0

AJMP addr11

Absolute Jump

Operation :

$(PC) \leftarrow (PC) + 2$
$(PC_{10-0}) \leftarrow$ page address

Encoding : HEX: 01h, #bytes: 2, Cycles: 3

a_{10}	a_9	a_8	0	0	0	0	1	a_{7-0}

SJMP rel

Short Jump (Relative address)

Operation :

$(PC) \leftarrow (PC) + 2$
$(PC_{10-0}) \leftarrow (PC) + rel$

Encoding : HEX: 80h, #bytes: 2, Cycles: 3

1	0	0	0	0	0	0	0	relative addr

LJMP addr16

Long Jump

Operation : $(PC) \leftarrow addr_{15-0}$

Encoding : HEX: 02h, #bytes: 3, Cycles: 4

0	0	0	0	0	0	1	0	a_{15-8}	a_{7-0}

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Appendix A : instruction set (16/18)

JMP @A + DPTR

Jump Indirect Relative to the DPTR

Operation : (PC) ← (A) + (DPTR)

Encoding : HEX: 73h, #bytes: 1, Cycles: 2

0	1	1	1	0	0	1	1

JZ rel

Jump if Accumulator is Zero

Operation : (PC) ← (PC) + 2
If (A)=0, then (PC) ← (PC) + rel

Encoding : HEX: 60h, #bytes: 2, Cycles: 3

0	1	1	0	0	0	0	0	relative addr

JNZ rel

Jump if Accumulator is Not Zero

Operation : (PC) ← (PC) + 2
If (A)≠0, then (PC) ← (PC) + rel

Encoding : HEX: 70h, #bytes: 2, Cycles: 3

0	1	1	1	0	0	0	0	relative addr

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Appendix A : instruction set (17 / 18)

CJNE <dest-byte>, <src-byte>, rel

Compare and Jump if Not Equal

CJNE A, direct, rel

Operation :

```
(PC)  ← (PC) + 3
If (A) ≠ (direct),
      then (PC) ← (PC) + rel
If (A) < (direct), then (C) ← 1
Else                  (C) ← 0
```

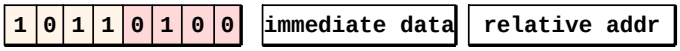
Encoding : HEX: B5h, #bytes: 3, Cycles: 4

CJNE A, #data, rel

Operation :

```
(PC)  ← (PC) + 3
If (A) ≠ data,
      then (PC) ← (PC) + rel
If (A) < data, then (C) ← 1
Else                (C) ← 0
```

Encoding : HEX: B4h, #bytes: 3, Cycles: 4

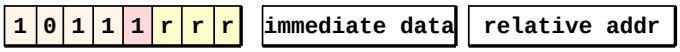


CJNE Rn, #data, rel

Operation :

```
(PC)  ← (PC) + 3
If (Rn) ≠ data,
      then (PC) ← (PC) + rel
If (Rn) < data, then (C) ← 1
Else                (C) ← 0
```

Encoding : HEX: B8h, #bytes: 3, Cycles: 4

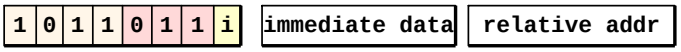


CJNE @Ri, #data, rel

Operation :

```
(PC)  ← (PC) + 3
If ((Ri)) ≠ data,
      then (PC) ← (PC) + rel
If ((Ri)) < data, then (C) ← 1
Else                  (C) ← 0
```

Encoding : HEX: B6h, #bytes: 3, Cycles: 4



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Appendix A : instruction set (18/18)

DJNZ <byte>, rel

Decrement and Jump if Not Zero

DJNZ Rn, rel

Operation :

```
(PC)  ← (PC) + 2
(Rn)  ← (Rn) - 1
If (Rn)≠0, then (PC) ← (PC) + rel
```

Encoding : HEX: D8h, #bytes: 2, Cycles: 3

1	1	0	1	1	r	r	r	relative addr

DJNZ direct, rel

Operation :

```
(PC)     ← (PC) + 3
(direct)← (direct) - 1
If (direct)≠0,
       then (PC) ← (PC) + rel
```

Encoding : HEX: D5h, #bytes: 3, Cycles: 4

1	1	0	1	0	1	0	1	direct addr	relative addr

NOP

No Operation

Operation : (PC) ← (PC) + 1

Encoding : HEX: 00h, #bytes: 1, Cycles: 1

0	0	0	0	0	0	0	0

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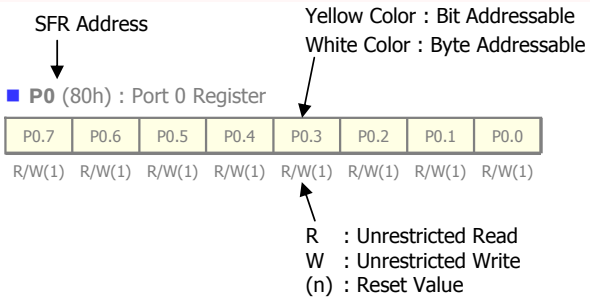
Appendix B : SFR Description [80h ~ 87h] (1/9)

[How to Read a SFR Descriptions]



■ **P0** (80h) : Port 0 Register

P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- Open-drain bi-directional port.
- Multiplexed low order address/data bus during external memory access.

■ **SP** (81h) : Stack Pointer Register

SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(1)	R/W(1)	R/W(1)

- Indicate where stack will start.
- Increment by PUSH and decrement by POP.

■ **DPL** (82h) : Data Pointer Low Register

DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **DPH** (83h) : Data Pointer High Register

DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **PCON** (87h) : Power Control Register

SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R/W(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- SMOD1 : Timer 1 baudrate double in UART mode 1, 2, 3.
- SMOD0 : Enable SM0 access. Don't modify this bit.
- POF : Power off flag.
  When power-on, this bit will be set by H/W.
- GF1, GF0 : General purpose flag.
- PD : Power-down (Stop) mode bit.
- IDL : IDL mode bit.

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Appendix B : SFR Description [88h ~ 8Dh] (2/9)

■ **TCON** (88h) : Timer/Counter 0/1 Control Register

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ TF1 : Timer 1 overflow flag.
- ◆ TR1 : Timer 1 run control.
- ◆ TF0 : Timer 0 overflow flag.
- ◆ TR0 : Timer 0 run control.
- ◆ IE1 : External interrupt 1 flag.
  If IT1 = 0, cleared by S/W (software).
  If IT1 = 1, cleared by H/W when the interrupt is serviced.
- ◆ IT1 : External interrupt 1 level/edge trigger control.
  Edge detect (IT1=1) / Level detect (IT1=0; Default)
- ◆ IE0 : External interrupt 0 flag.
  If IT0 = 0, cleared by S/W (software).
  If IT0 = 1, cleared by H/W when the interrupt is serviced.
- ◆ IT0 : External interrupt 0 level/edge trigger control.
  Edge detect (IT0=1) / Level detect (IT0=0; Default)

■ **TMOD** (89h) : Timer/Counter 0 Mode Control Register

GATE	C/T	M1	M0	GATE	C/T	M1	M0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ Timer[1]: GATE[7], C/T[6], M1:M0[5:4]
- ◆ Timer[0]: GATE[3], C/T[2], M1:M0[1:0]
- ◆ GATE : When TRx (in TCON) is set and GATE=1, Timer x will run only while INTx pin is high (hardware control). When GATE=0, Timer x will run only while TRx=1 (software control).
- ◆ C/T : Counter or Timer Selector. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin).

- ◆ M1, M0 : Mode Selector bits
  [0 0] Mode 0. 13-bit T/C.
  [0 1] Mode 1. 16-bit T/C.
  [1 0] Mode 2. 8-bit Auto-Reload T/C.
  [1 1] Mode 3.
  (Timer 1) stopped, (Timer 0)
  TL0: 8-bit T/C controlled by the Timer 0 control bits.
  TH0: 8-bit T/C controlled by the Timer 1 control bits.

■ **TL0** (8Ah) : Timer/Counter 0 Low Byte Register

TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **TL1** (8Bh) : Timer/Counter 1 Low Byte Register

TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **TH0** (8Ch) : Timer/Counter 0 High Byte Register

TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **TH1** (8Dh) : Timer/Counter 1 High Byte Register

TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

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Appendix B : SFR Description [8Eh ~ 99h] (3/9)

■ CKCON (8Eh) : Clock Control Register

WD1	WD0	T2M	T1M	T0M	-	-	-
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)			

- ◆ WD1, WD0 : Watchdog timer mode select
  - [0,0] : 2^{17} clocks (interrupt), 2^{17} + 512 clocks (reset)
  - [0,1] : 2^{20} clocks (interrupt), 2^{20} + 512 clocks (reset)
  - [1,0] : 2^{23} clocks (interrupt), 2^{23} + 512 clocks (reset)
  - [1,1] : 2^{26} clocks (interrupt), 2^{26} + 512 clocks (reset)
- ◆ T2M, T1M, T0M : Timer 2/1/0 time base selection
  - 0: time base is 4 clocks.
  - 1: time base is 12 clocks.

■ P1 (90h) : Port 1 Register

P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- ◆ Quasi bi-directional port with internal pull-up resistors.
- ◆ For using an alternative function, P1.X must be "1".

■ EXIF (91h) : External Interrupt Flag Register

IE5	IE4	IE3	IE2	XT	-	-	BGS
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R(1)			R/W(1)

- ◆ IE5, IE4, IE3, IE2 : External interrupt 5, 4, 3, 2 flag. Cleared by S/W.
- ◆ IE2 : External interrupt 2 flag. Cleared by S/W.
- ◆ XT : Crystal Select. (Read only)
  When Set, The crystal is selected as the system clock.
- ◆ BGS : Band-gap select. When set, LVD will run in power-down mode.

■ SCON (98h) : Serial Port Control Register of UART0

SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ SM0, SM1 : Serial Port mode selector.
  - [0,0] : Mode0, 8-bit shift register (F_{OSC}/4)
  - [0,1] : Mode1, 8-bit UART (Variable)
  - [1,0] : Mode2, 9-bit UART (F_{OSC}/32 or F_{OSC}/16)
  - [1,1] : Mode3, 9-bit UART (Variable)
- ◆ SM2 : Enables the Automatic Address Recognition in Mode2 and 3.
  In Mode1, the validity of a Stop Bit is checked if SM2=1
  In Mode0, SM2 should be "0".
- ◆ REN : Enable/Disable reception.
- ◆ TB8 : 9th data bit that will be transmitted in Mode2 and 3.
- ◆ RB8 : 9th data bit that was received in Mode 2 and 3.
  In Mode1, RB8 is equal to stop bit if SM2 is "0".
  In Mode0, RB8 is not used.
- ◆ TI : Transmission interrupt flag. Must be cleared by S/W.
- ◆ RI : Reception interrupt flag. Must be cleared by S/W.

■ SBUF (99h) : Serial Data Buffer Register

SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ The transmission buffer and the reception buffer are separated.
- ◆ The transmission/reception buffers have the same address.

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Appendix B : SFR Description [A0h ~ B7h] (4/9)

■ **P2** (A0h) : Port 2 Register

P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- Quasi bi-directional port with internal pull-up resistors.
- General I/O and address output during access to external memory.

■ **P4** (A5h) : Port 4 Register

-	-	-	-	P4.3	P4.2	P4.1	P4.0
				R/W(1)	R/W(1)	R/W(1)	R/W(1)

- Quasi bi-directional port with internal pull-up resistors.

■ **P4SEL** (A6h) : Port 4 Pull-up Control Register

-	-	-	-	P4SEL.3	P4SEL.2	P4SEL.1	P4SEL.0
				R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Internal Pull-up resistor is ON (Default) / 1= OFF

■ **IE** (A8h) : Interrupt Enable Register

EA	EADC	ET2	ES	ET1	EX1	ET0	EX0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- EA : Enable/Disable all interrupts.
- EADC : ADC interrupt enable.
- ET2 : Timer 2 interrupt enable.
- ES : Serial port interrupt enable.
- ET1 : Timer 1 interrupt enable.
- EX1 : External interrupt 1 enable.
- ET0 : Timer0 interrupt enable.
- EX0 : External interrupt 0 enable.

■ **SADDR** (A9h) : Slave Address Register

SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Programmed with the given or broadcast address assigned to serial port

■ **P3** (B0h) : Port 3 Register

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- Quasi bi-directional port with internal pull-up resistors.
- When alternative function enabled, P3.X must be "1".

■ **IPH** (B7h) : Interrupt Priority High Register

-	PADCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
R(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- PADCH : ADC interrupt priority high.
- PT2H : Timer 2 interrupt priority high.
- PSH : Serial Port (UART) interrupt priority high.
- PT1H : Timer 1 interrupt priority high.
- PX1CH : External interrupt 1 priority high.
- PT0H : Timer 0 interrupt priority high.
- PX0H : External interrupt 0 priority high.

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Appendix B : SFR Description [B8h ~ CBh] (5/9)

IP (B8h) : Interrupt Priority Register

-	PADC	PT2	PS	PT1	PX	PT0	PX0
R(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- PADC : ADC interrupt priority low.
- PT2 : Timer 2 interrupt priority low.
- PS : Serial port (UART) interrupt priority low.
- PT1 : Timer 1 interrupt priority low.
- PX1 : External interrupt 1 priority low.
- PT0 : Timer 0 interrupt priority low.
- PX0 : External interrupt 0 priority low.

SADEN (B9h) : Slave Address Mask Enable Register

SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

PMR (C4h) : Power Management Control Register

-	-	-	-	-	ALEOFF	-	-
					R/W(0)		

- ALEOFF : 1 = ALE toggling disable.
  0 = ALE toggling enable (Default).

STATUS (C5h) : Crystal Status Register

-	-	-	XTUP	-	-	-	-
			R(0)				

- XTUP : Crystal oscillator warm-up status.
  This bit is cleared by H/W during executing Power-on reset or during exiting from the power-down mode.
  It is set by H/W after XTAL stabilization.

T2CON (C8h) : Timer/Counter 2 Control Register

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- TF2 : Timer 2 overflow flag.
- EXF2 : Timer 2 external flag.
- RCLK : Receive clock flag.
- TCLK : Transmit clock flag.
- EXEN2 : Timer 2 external enable flag.
- TR2 : Timer 2 run flag.
- C/T2 : Timer 2 Timer/Counter select. When set, counter by T2.
- CP/RL2 : Capture/Reload flag.
  CP/RL2 = 0, Reload. (TH2,TL2) ← (RCAP2H,RCAP2L)
  CP/RL2 = 1, Capture. (RCAP2H,RCAP2L) ← (TH2,TL2)

T2MOD (C9h) : Timer/Counter 2 Mode Control Register

-	-	-	-	-	-	T2OE	DCEN
						R/W(0)	R/W(0)

- T2OE : Timer 2 clock output enable. When set, clock output to P1.0.
- DCEN : Timer 2 down count enable. When set, count down.

RCAP2L (CAh) : Timer/Counter 2 Capture/Reload Low Byte Register

RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

RCAP2H (CBh) : Timer/Counter 2 Capture/Reload High Byte Register

RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

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Appendix B : SFR Description [CCh ~ DCh] (6/9)

■ **TL2** (CCh) : Timer/Counter 2 Low Byte Register

TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **TH2** (CDh) : Timer/Counter 2 High Byte Register

TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **PSW** (D0h) : Program Status Word Register

CY	AC	F0	RS1	RS0	OV	F1	P
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R(0)

- CY : Carry Flag.
- AC : Auxiliary carry flag.
- F0 : User flag 0.
- RS1, RS0 : Register bank select
  [0,0] : Bank 0
  [0,1] : Bank 1
  [1,0] : Bank 2
  [1,1] : Bank 3
- OV : Overflow flag.
- F1 : User flag 1.
- P : Parity bit. Set/clear by H/W according to ACC odd parity.

■ **WDCON** (D8h) : Watchdog Timer & Power Status Register

-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- POR : Power-on reset flag.
- EPFI : Enable power-fail interrupt.
- PFI : Power-fail interrupt flag.
- WDIF : Watchdog timer interrupt flag.
- WTRF : Watchdog timer reset flag.
- EWT : Watchdog timer reset enable.
- RWT : Restart watchdog timer.

■ **PWM0CON** (DCh) : PWM Control Register

P0SEL	PS2_P0	PS1_P0	PS0_P0	MODE_P0	RL_P0	CLR_P0	RUN_P0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- P0SEL : PWM waveform output enable to P3.4.
- PS2_P0, PS1_P0, PS0_P0 : Pre-scaled Clock Selection.
  [0,0,0] = FOSC/1, [0,0,1] = FOSC/2, [0,1,0] = FOSC/4,
  [0,1,1] = FOSC/8, [1,0,0] = FOSC/16, [1,0,1] = FOSC/32,
  [1,1,0] = FOSC/64, [1,1,1] = FOSC/128
- MODE_P0 : 8 bits / (2+6) bits counter mode selector.
  0 = (2+6) bits mode (Default)
  1 = 8 bits mode
- RL_P0 : PWM data update mode selector
  0 = 6-bit counter overflow update (Default)
  1 = 8-bit counter overflow update
- CLR_P0 : Counter reset enable. Cleared by H/W.
- RUN_P0 : Counter start enable.

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Appendix B : SFR Description [DDh ~ E3h] (7/9)

■ PWM1CON (DDh) : PWM Control Register

P1SEL	PS2_P1	PS1_P1	PS0_P1	MODE_P1	RL_P1	CLR_P1	RUN_P1
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- P1SEL : PWM waveform output enable to P1.0.
- PS2_P1, PS1_P1, PS0_P1 : Pre-scaled Clock Selection.
  [0,0,0] = FOSC/1, [0,0,1] = FOSC/2, [0,1,0] = FOSC/4,
  [0,1,1] = FOSC/8, [1,0,0] = FOSC/16, [1,0,1] = FOSC/32,
  [1,1,0] = FOSC/64, [1,1,1] = FOSC/128
- MODE_P1 : 8 bits / (2+6) bits counter mode selector.
  0 = (2+6) bits mode (Default)
  1 = 8 bits mode
- RL_P1 : PWM data update mode selector
  0 = 6-bit counter overflow update (Default)
  1 = 8-bit counter overflow update
- CLR_P1 : Counter reset enable. Cleared by H/W.
- RUN_P1 : Counter start enable.

■ PWM0D (DEh) : PWM 0 Duty Data Register

PWM0D.7	PWM0D.6	PWM0D.5	PWM0D.4	PWM0D.3	PWM0D.2	PWM0D.1	PWM0D.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ PWM1D (DFh) : PWM 1 Duty Data Register

PWM1D.7	PWM1D.6	PWM1D.5	PWM1D.4	PWM1D.3	PWM1D.2	PWM1D.1	PWM1D.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ ACC/A (E0h) : Accumulator

ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ ADCSEL (E2h) : ADC Clock and Port Control Register

ADIV2	ADIV1	ADIV0	-	ADC3	ADCS2	ADCS1	ADCS0
R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ADIV2, ADIV1, ADIV0 : ADC input clock divide.
  [0,0,0] : 1-divide (F_{OSC})
  [0,0,1] : 2-divide ($F_{OSC}/2$)
  [0,1,0] : 4-divide ($F_{OSC}/4$)
  [0,1,1] : 8-divide ($F_{OSC}/8$)
  [1,0,0] : 16-divide ($F_{OSC}/16$)
- ADC3 : 1 = ADC3 input enable & digital input disable at P1.3.
- ADC2 : 1 = ADC2 input enable & digital input disable at P1.2.
- ADC1 : 1 = ADC1 input enable & digital input disable at P1.1.
- ADC0 : 1 = ADC0 input enable & digital input disable at P0.0.

■ ALTSEL (E3h) : Alternative Function Selection Register

-	-	EAINT0	P0INT1	P0INT0	TX	RX	PWM1
		R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Only Available I 8/10/20-pin SPDIP/SOIC Package.
  Don't used in 40-PDIP, 44-PLCC/LQFP, 28-SPDP/SOIC Package.
- EAINT0 : 1 = EA Pin is used for INT0 input.
- P0INT1 : 1 = P0.2 pin is used for INT1 input.
- P0INT0 : 1 = P0.1 pin is used for INT0 input
- TX : 1 = P0.1 pin is used for TX input/output.
- RX : 1 = P0.0 pin is used for RX output.
- PWM1 : 1 = P0.1 pin is used for PWM1 output.

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Appendix B : SFR Description [E4h ~ EFh] (8/9)

■ **P0SEL** (E4h) : Port 0 Pull-up Control Register

P0SEL.7	P0SEL.6	P0SEL.5	P0SEL.4	P0SEL.3	P0SEL.2	P0SEL.1	P0SEL.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Internal Pull-up resistor is ON
- 1 = Internal Pull-up resistor is OFF (Default) when ADC_EN = 1

■ **P1SEL** (E5h) : Port 1 Pull-up Control Register

P1SEL.7	P1SEL.6	P1SEL.5	P1SEL.4	P1SEL.3	P1SEL.2	P1SEL.1	P1SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Internal Pull-up resistor is ON (Default)
- 1 = Internal Pull-up resistor is OFF when ADC_EN = 1

■ **P2SEL** (E6h) : Port 2 Pull-up Control Register

P2SEL.7	P2SEL.6	P2SEL.5	P2SEL.4	P2SEL.3	P2SEL.2	P2SEL.1	P2SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Internal Pull-up resistor is ON (Default) / 1= OFF

■ **P3SEL** (E6h) : Port 3 Pull-up Control Register

P3SEL.7	P3SEL.6	P3SEL.5	P3SEL.4	P3SEL.3	P3SEL.2	P3SEL.1	P3SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Internal Pull-up resistor is ON (Default) / 1= OFF

■ **EIE** (E8h) : Extended Interrupt Enable Register

-	-	-	EWDT	EX5	EX4	EX3	EX2
			R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- EWDT : Watchdog timer interrupt enable
- EX5 : External interrupt 5 enable.
- EX4 : External interrupt 4 enable.
- EX3 : External interrupt 3 enable.
- EX2 : External interrupt 2 enable.

■ **ADCR** (EEh) : ADC Result High Register : Value[8:1]

SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	SAR1
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **ADCON** (EFh) : ADC Control & ADC Result LSB Register : Value[0]

AD_EN	AD_REQ	AD_END	ADCF	ACH1	ACH0	-	SAR0
R/W(0)	R/W(0)	R(1)	R/W(0)	R/W(0)	R/W(0)		R/W(0)

- AD_EN : AD conversion enable.
- AD_REQ : Request AD conversion at current channel.
  Cleared by H/W when AD_END goes to 1 from 0.
- AD_END : Current ADC status.
  0 = ADC is running now.
- ADCF : ADC interrupt flag. Must be cleared by S/W.
- ACH1, ACH0 : ADC channel selection
  [0,0] = ADC0 input selection (P0.0)
  [0,1] = ADC1 input selection (P1.1)
  [1,0] = ADC2 input selection (P1.2)
  [1,1] = ADC3 input selection (P1.3)
- SAR0 : LSB of ADC result value.

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Appendix B : SFR Description [F0h ~ F8h] (9/9)

■ **B** (F0h) : B Register

B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **EIP** (F8h) : Extended Interrupt Priority Register

-	-	-	PWDT	RX5	PX4	PX3	PX2
			R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ PWDT : Watchdog timer interrupt priority bit.
- ◆ PX5 : External interrupt 5 priority bit.
- ◆ PX4 : External interrupt 4 priority bit.
- ◆ PX3 : External interrupt 3 priority bit.
- ◆ PX2 : External interrupt 2 priority bit.

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Appendix C : Update History

- V1.8
  - ✓ 44-LQFP → 44-MQFP
- V1.9
  - ✓ EA : This pin must not be floating.
  - ✓ Describe the constraint of power slope
- V2.0
  - ✓ Add on the ESD Structure of Pads slide
  - ✓ Update the 'On-Chip POR' slide.
  - ✓ Update the Product Numbering System
- V2.1
  - ✓ Add on the Power Slope slide
  - ✓ Feedback Pull-up Issue : Update PnSEL Control
  - ✓ Update the Block Diagram slide
  - ✓ Update the 'On-Chip POR' Slide

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