MiDAS Family

BM-MiDAS2.0-V1.8

BM

Brief Manual of MiDAS2.0 Family

FLASH / ISP / IAP
8-bit Turbo Microcontrollers

V1.8

Oct. 2007

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Contents

1. Product Overviews

- CORERIVER's MiDAS2.0 Family is a group of fast 80C52 compatible microcontrollers
- The instruction execution of MiDAS2.0 is max. 3 times faster than that of traditional 80C52.
  - ✓ 1 Machine cycle = 4 clocks vs. 12 clocks
- Additional peripherals of MiDAS2.0 Family:
  - ✓ 10 bit ADC / 12 PWM outputs in two 6-module PCA's / Extra UART / WDT / LVD / POR.
- Power saving modes
- Noise tolerant scheme
- Supports ISP / IAP of FLASH memory
- Provides User-Friendly MDS environment with on-chip HW debugging engine
- Provides Easy-to-Use training-kit system

1. Product Overview

A. MiDAS2.0 Family - GC80C590AE Series (ISP Flash MCU)

Product	EEPROM (byte)	Mask-ROM (byte)	Flash (byte)	RAM (Byte)	Volt (V)	Freq. (MHz)	T/C (16bits)	Serial I/O	WDT	ADC (bit x ch)	PWM (bit x ch)	I/O Pins	Package	Others	Available Time
GC89C591A0-TQ100I	2K	-	62K	2K	3.0~3.6	40	3	2 UART	Yes	10X8	8x12	80	100-TQFP	ISP	**Now**
GC89C591A0-P64I												48	64-PDIP	IAP	**Now**
GC89C591A0-LQ64I												48	64-LQFP	EJTAG	**Now**
GC89C591A0-TQ64I												48	64-TQFP	LVD	**Now**
GC89C591A0-PL44I												32	44-PLCC	POR	**Now**
GC89C591A0-MQ44I												32	44-MQFP	Ring OSC.	**Now**
GC81C591A0-TQ100I	2K	62K	-	2K	3.0~3.6	40	3	2 UART	Yes	10X8	8x12	80	100-TQFP	ISP	**Now**
GC81C591A0-P64I												48	64-PDIP	IAP	**Now**
GC81C591A0-LQ64I												48	64-LQFP	EJTAG	**Now**
GC81C591A0-TQ64I												48	64-TQFP	LVD	**Now**
GC81C591A0-PL44I												32	44-PLCC	POR	**Now**
GC81C591A0-MQ44I												32	44-MQFP	Ring OSC.	**Now**
GC89C541A0-TQ100I	2K	-	14K	2K	3.0~3.6	40	3	2 UART	Yes	10X8	8x12	80	100-TQFP	ISP	**Now**
GC89C541A0-P64I												48	64-PDIP	IAP	**Now**
GC89C541A0-LQ64I												48	64-LQFP	EJTAG	**Now**
GC89C541A0-TQ64I												48	64-TQFP	LVD	**Now**
GC89C541A0-PL44I												32	44-PLCC	POR	**Now**
GC89C541A0-MQ44I												32	44-MQFP	Ring OSC.	**Now**
GC81C541A0-TQ100I	2K	14K	-	2K	3.0~3.6	40	3	2 UART	Yes	10X8	8x12	80	100-TQFP	ISP	**Now**
GC81C541A0-P64I												48	64-PDIP	IAP	**Now**
GC81C541A0-LQ64I												48	64-LQFP	EJTAG	**Now**
GC81C541A0-TQ64I												48	64-TQFP	LVD	**Now**
GC81C541A0-PL44I												32	44-PLCC	POR	**Now**
GC81C541A0-MQ44I												32	44-MQFP	Ring OSC.	**Now**

1. Product Overview (Cont'd)

A. MiDAS2.0 Family - GC80C590AE Series (ISP Flash MCU)

Product	EEPROM (byte)	Mask-ROM (byte)	Flash (byte)	RAM (Byte)	Volt (V)	Freq. (MHz)	T/C (16bits)	Serial I/O	WDT	ADC (bit x ch)	PWM (bit x ch)	I/O Pins	Package	Others	Available Time
GC89C581A0-TQ100I	2K	-	30K	2K	3.0~3.6	40	3	2 UART	Yes	10X8	8x12	80	100-TQFP	ISP	**Now**
GC89C581A0-P64I												48	64-PDIP	IAP	**Now**
GC89C581A0-LQ64I												48	64-LQFP	EJTAG	**Now**
GC89C581A0-TQ64I												48	64-TQFP	LVD	**Now**
GC89C581A0-PL44I												32	44-PLCC	POR	**Now**
GC89C581A0-MQ44I												32	44-MQFP	Ring OSC.	**Now**
GC81C581A0-TQ100I	2K	30K	-	2K	3.0~3.6	40	3	2 UART	Yes	10X8	8x12	80	100-TQFP	ISP	**Now**
GC81C581A0-P64I												48	64-PDIP	IAP	**Now**
GC81C581A0-LQ64I												48	64-LQFP	EJTAG	**Now**
GC81C581A0-TQ64I												48	64-TQFP	LVD	**Now**
GC81C581A0-PL44I												32	44-PLCC	POR	**Now**
GC81C581A0-MQ44I												32	44-MQFP	Ring OSC.	**Now**

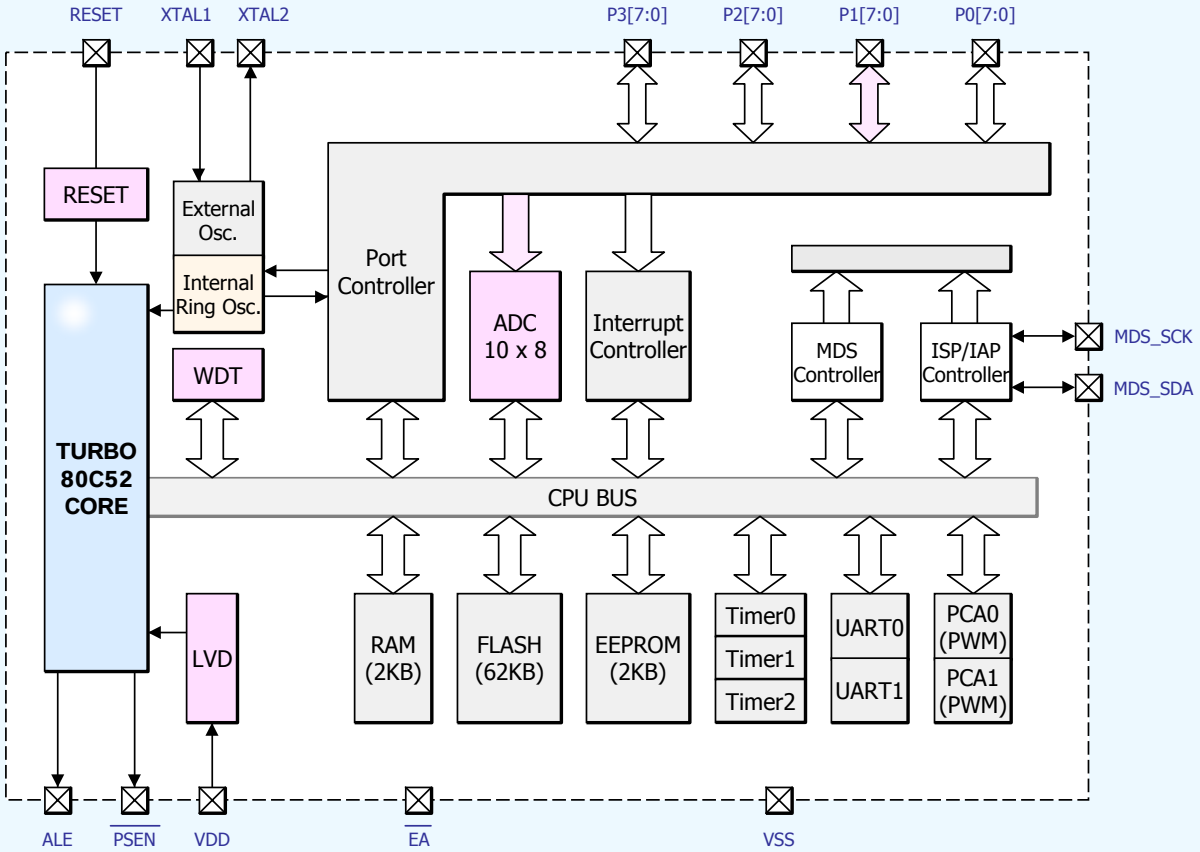
2. Features

- CPU
  - ✓ 8-bit turbo 80C52 architecture
  - ✓ 4 cycles/1 machine cycle
  - ✓ Pin/instruction level compatible with Intel 80C52
- 16/32/62 KBytes on-chip FLASH ROM
  - ✓ ISP by serial interface
  - ✓ IAP and virtual EEPROM for data (2KByte)
- On-chip H/W debugging engine for ICE.
- 2 KBytes on-chip RAM
  - ✓ 256 bytes IRAM
  - ✓ 1,792 bytes AUXRAM (Accessed with `MOVX`)
- Max. programmable 80 I/O pins (for 100-TQFP)
  - ✓ Quasi-bidirectional Intel type ports : P0 ~ P4
  - ✓ Input/Output and pull-up control : P5 ~ P9
  - ✓ TTL & CMOS compatible logic levels : P0 ~ P3
  - ✓ CMOS levels : P4 ~ P9
  - ✓ All ports are initialized during asynchronous power-on reset.
- EMI reduction mode : Inhibit ALE
- Low Voltage Detector
- 27-bit Programmable Watchdog Timer
- Three 16-bit Timer/Counters
- Two Full-Duplex UART
  - ✓ Automatic address recognition
- 12 PWM outputs provided by two 6-module Programmable Counter Arrays
  - ✓ 8-bit dynamic PWM (12 channels).
  - ✓ 16-bit Compare/Capture counter (12 channels).
  - ✓ High Speed Output (12 channels).
- 8-channel 10-bit ADC
  - ✓ Max. 400K samples per second (@40 MHz)
  - ✓ Programmable clock frequency prescaler
- 16 interrupt sources (with 6 external sources)
  - ✓ Timer0/1/2, UART0/1, PCA0/1, ADC, WDT, LVD, and 6 External
  - ✓ Four/Two-level interrupt priority

2. Features (Cont'd)

- Wake-up from power-down mode
  - ✓ External reset
  - ✓ External interrupt 0/1
  - ✓ WDT interrupt or reset
- Reset scheme
  - ✓ On-chip power-on-reset
  - ✓ External reset
  - ✓ Low voltage detector reset
  - ✓ Watchdog timer reset if enabled
- Internal power stabilization counter
  - ✓ Extends power on reset up to 50ms.
- Supply voltage : 3.0V ~ 3.6V
- Operating temperature : -20 °C ~ 85 °C
- On-chip oscillator circuitry using external crystal
  - ✓ Max. 40 MHz internal operating frequency
- Internal Ring oscillator running at 2.8 MHz
- Power consumption
  - ✓ Active current : Max. 30mA @ 3.3V, 40MHz
  - ✓ Stop current : Typ. 2 uA (Max. 10 uA)
- E.S.D. protection up to 2,000V
- Latch-up protection up to ±200mA
- Package
  - ✓ 44-PLCC/MQFP
  - ✓ 64-PDIP/LQFP/TQFP
  - ✓ 100-TQFP

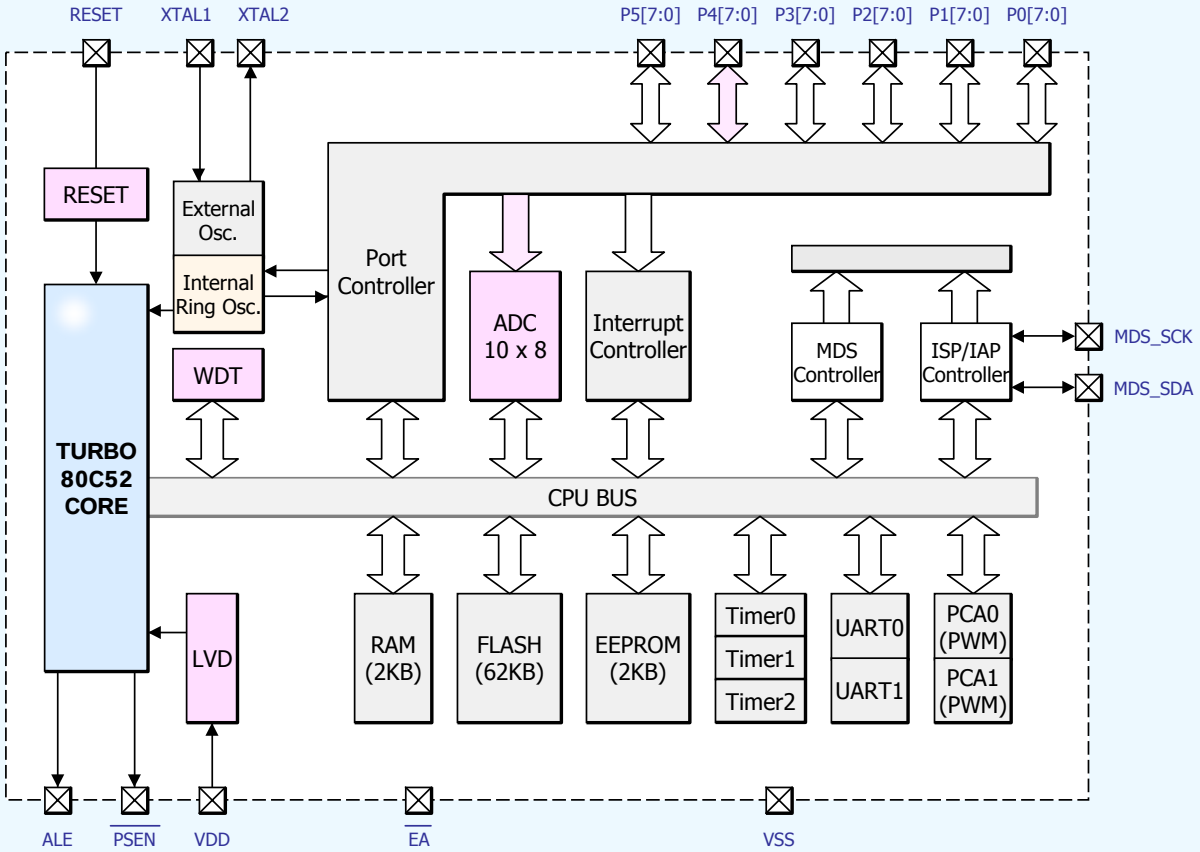
3. Block Diagram



[44-PLCC / MQFP]

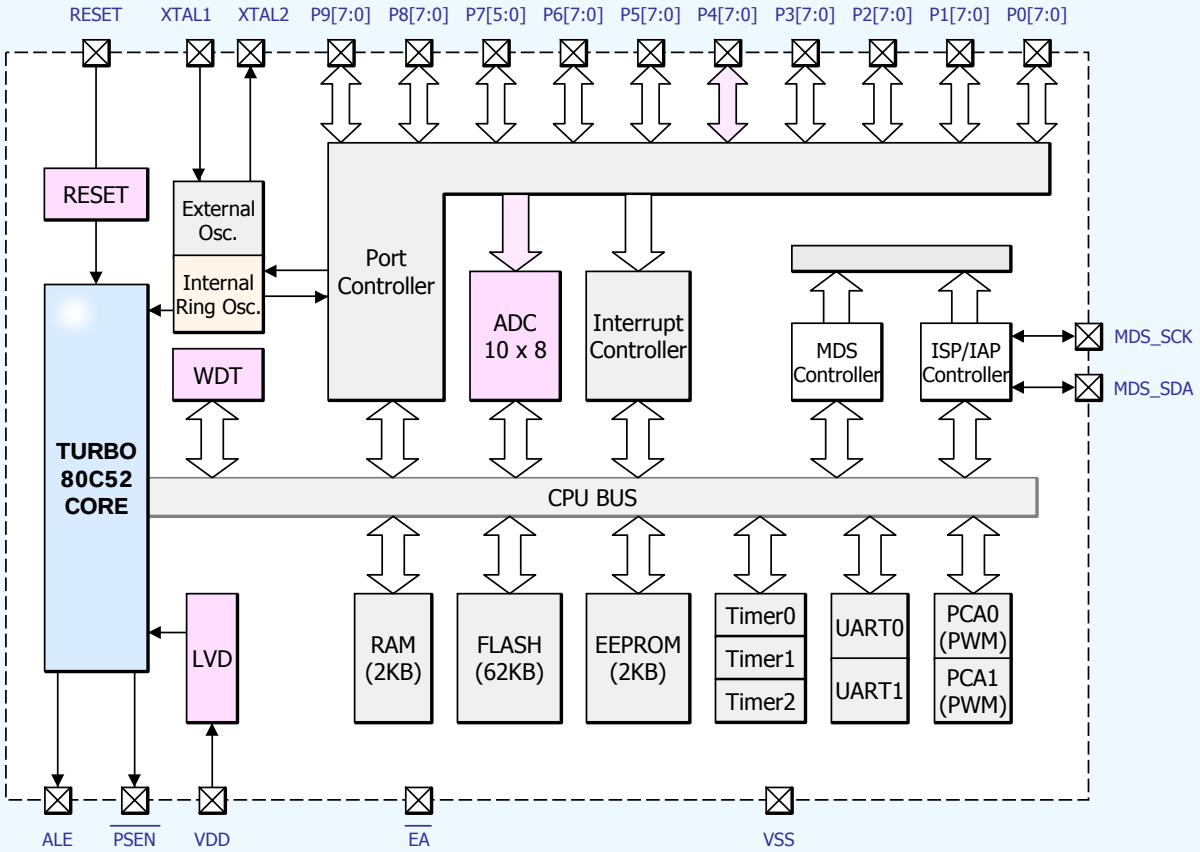
* PKGOPT (IOCFG.0) flag bit must be set to "1".

3. Block Diagram (Cont'd)



[64-PDIP/LQFP/TQFP]

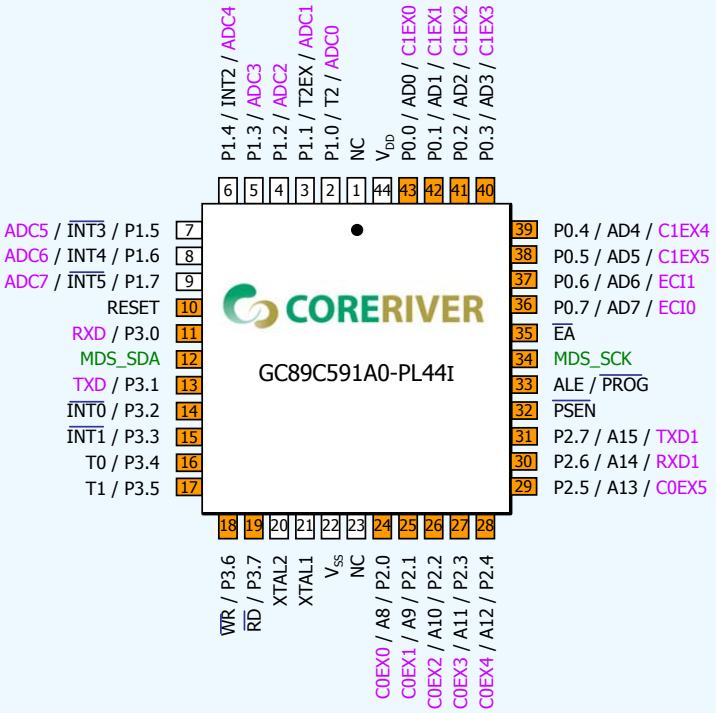
3. Block Diagram (Cont'd)



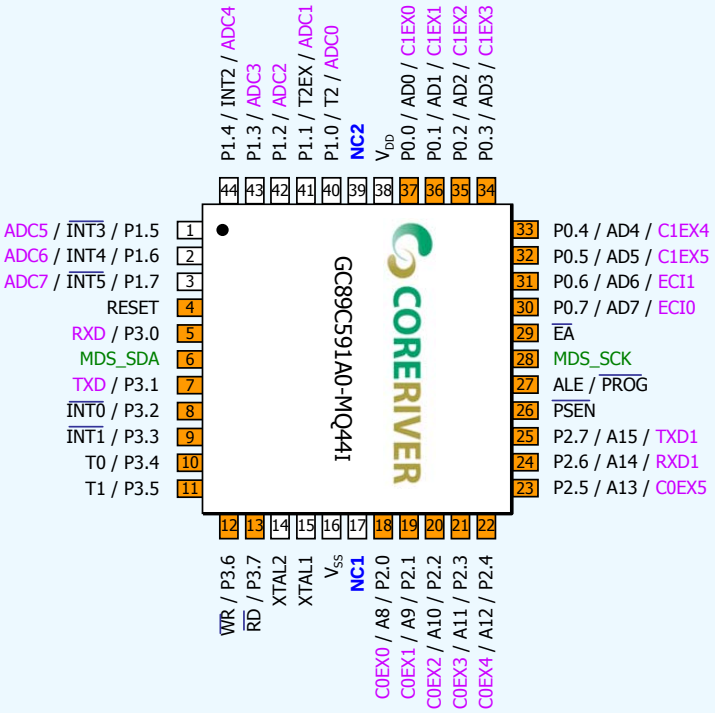
[100-TQFP]

4. Pin Configurations

: 5V Tolerant Input (3.3V Output)
: 3.3V Tolerant Input (3.3V Output)



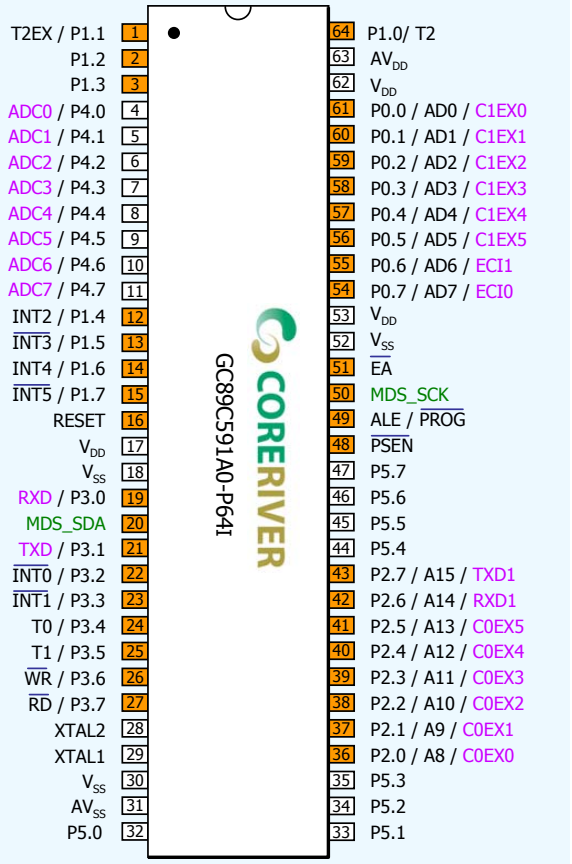
[44-PLCC]



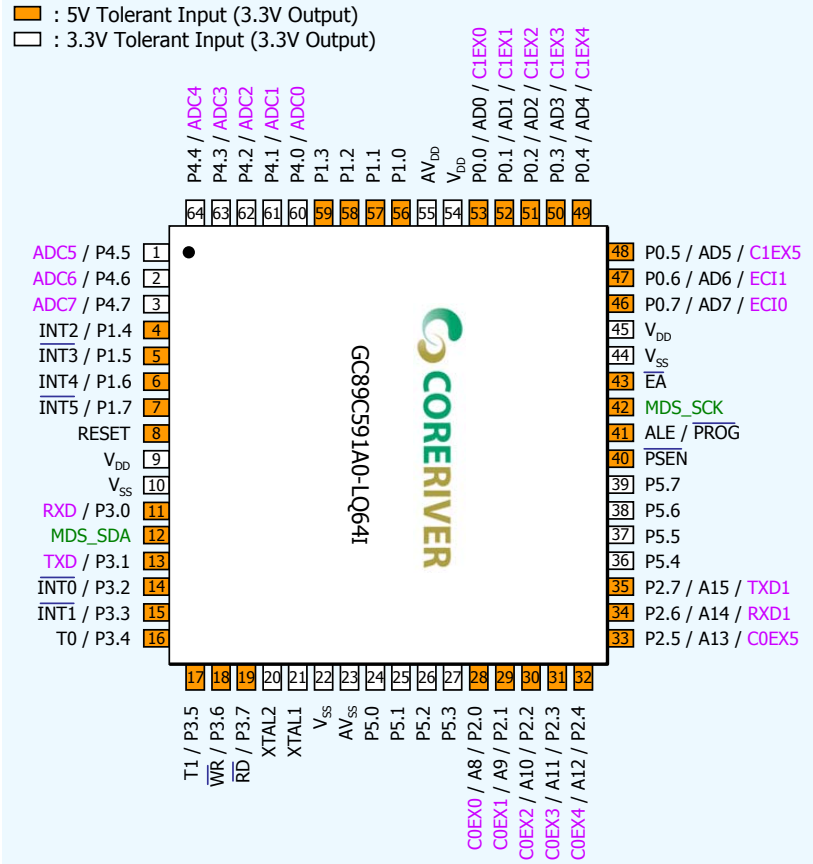
[44-MQFP]

NOTE : Do not connect NC1 and NC2 pins on PCB.
If necessary, connect NC1 to VDD and NC2 to Ground.

4. Pin Configurations (Cont'd)

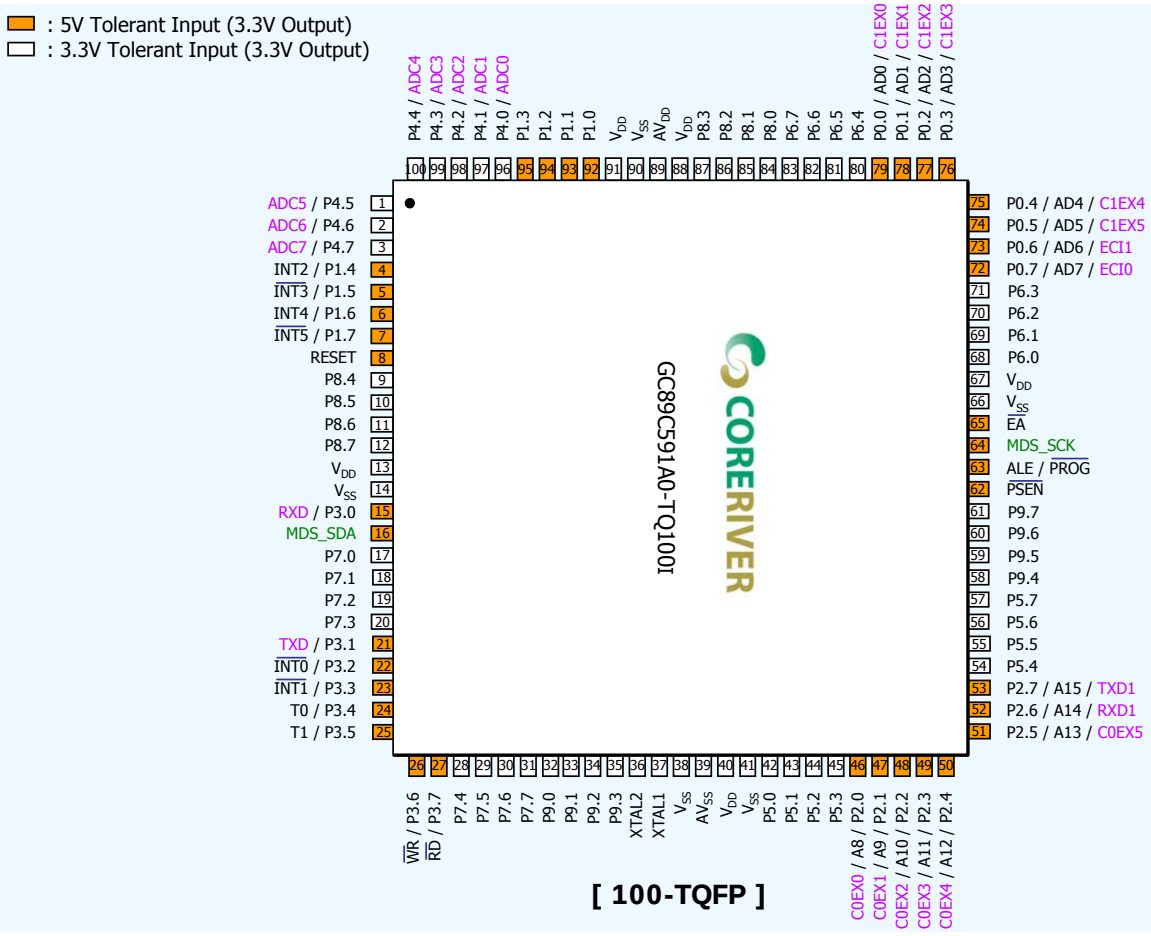


[64-PDIP]



[64-LQFP/TQFP]

4. Pin Configurations (Cont'd)



5. Pin Descriptions

Symbol	Direction	Description	Share Pins
V_{DD}	Input	Power Supply	-
AV_{DD}	Input	Reference Voltage for ADC	-
V_{SS}	Input	Ground	-
AV_{SS}	Input	Reference Ground for ADC	-
RESET	Input	External Reset	-
XTAL1	Input	Input to the inverting oscillator amplifier	-
XTAL2	Output	Output from the inverting oscillator amplifier	-
$\overline{EA}$	Input	External ROM Access Enable (MiDAS2.0 family dose not use this pin.)	-
ALE	Input/Output	Address Latch Enable (If ALEOFF is set, active only for external RAM access) This pin is also used for the parallel programming of FLASH memory.	$\overline{PROG}$
$\overline{PSEN}$	Input/Output	Program Strobe Enable. Pull-up. Used for Special Input only. (MiDAS2.0 does not support the code fetch from external ROM.)	-
MDS_SDA, MDS_SCK	Input/Output	I/O for MDS/ISP. The pull-up resistor is always switched on. This port is quasi-bidirectional.	-
P0[7:0]	Input/Output	◆ An 8-bit quasi-bidirectional open-drain I/O port. 5V Tolerant Input. ◆ Note that the output is fully driven (push-pull) when P0 drives address/data to access external RAM or PCA1 drives output signals (C1EXn). • P0.0 ~ P0.7 → AD0 ~ AD7 : Low address or data input/output • P0.0 ~ P0.5 → C1EX0 ~ C1EX5 for PCA1 • P0.6 → ECI1 for PCA1 • P0.7 → ECI0 for PCA0	P0.0 / AD0 / C1EX0 P0.1 / AD1 / C1EX1 P0.2 / AD2 / C1EX2 P0.3 / AD3 / C1EX3 P0.4 / AD4 / C1EX4 P0.5 / AD5 / C1EX5 P0.6 / AD6 / ECI1 P0.7 / AD7 / ECI0

5. Pin Descriptions (Cont'd)

Symbol	Direction	Description	Share Pins
P1[7:0]	Input/Output	◆ An 8-bit Quasi-bidirectional I/O port. 5V Tolerant Input. ◆ **64/80/100 pins Package** : General I/O. • P1.0 → T2 : External Input for Timer/Counter 2 • P1.1 → T2EX : Timer/Counter 2 Capture/Reload Trigger • P1.4 → INT2 : External Interrupt 2 (Positive Edge) • P1.5 → $\overline{\text{INT3}}$: External Interrupt 3 (Negative Edge) • P1.6 → INT4 : External Interrupt 4 (Positive Edge) • P1.7 → $\overline{\text{INT5}}$: External Interrupt 5 (Negative Edge)	P1.0 / T2 P1.1 / T2EX P1.4 / INT2 P1.5 / $\overline{\text{INT3}}$ P1.6 / INT4 P1.7 / $\overline{\text{INT5}}$
		◆ An 8-bit Quasi-bidirectional I/O port. 3.3V Tolerant Input. ◆ **44 pins Package** : Port for Digital I/O or ADC Input (3.3V). • P1.0 → T2 : External Input for Timer/Counter 2 • P1.1 → T2EX : Timer/Counter 2 Capture/Reload Trigger • P1.4 → INT2 : External Interrupt 2 (Positive Edge) • P1.5 → $\overline{\text{INT3}}$: External Interrupt 3 (Negative Edge) • P1.6 → INT4 : External Interrupt 4 (Positive Edge) • P1.7 → $\overline{\text{INT5}}$: External Interrupt 5 (Negative Edge) • P1.0 → ADC0 : A/D converter Input 0 • P1.1 → ADC1 : A/D converter Input 1 • P1.2 → ADC2 : A/D converter Input 2 • P1.3 → ADC3 : A/D converter Input 3 • P1.4 → ADC4 : A/D converter Input 4 • P1.5 → ADC5 : A/D converter Input 5 • P1.6 → ADC6 : A/D converter Input 6 • P1.7 → ADC7 : A/D converter Input 7	P1.0 / T2 / ADC0 P1.1 / T2EX / ADC1 P1.2 / ADC2 P1.3 / ADC3 P1.4 / INT2 / ADC4 P1.5 / $\overline{\text{INT3}}$ / ADC5 P1.6 / INT4 / ADC6 P1.7 / $\overline{\text{INT5}}$ / ADC7

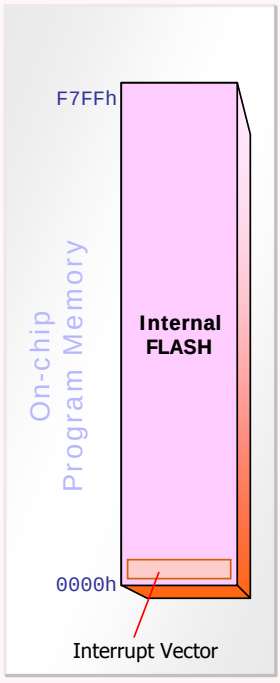
5. Pin Descriptions (Cont'd)

Symbol	Direction	Description	Share Pins
P2[7:0]	Input/Output	◆ An 8-bit Quasi-bidirectional I/O port. 5V Tolerant Input. ◆ Note that the output is fully driven (push-pull) when P2 drives the high byte of address to access external RAM or PCA0 drives output signals (C0EXn). • P2.0~P2.7 → AD8 ~ AD15 : High address output • P2.0~P2.5 → C0EX0 ~ C0EX5 for PCA0 • P2.6 → RXD1 : Serial Port 1 Output • P2.7 → TXD1 : Serial Port 1 Input	P2.0 / AD8 / C0EX0 P2.1 / AD9 / C0EX1 P2.2 / AD10 / C0EX2 P2.3 / AD11 / C0EX3 P2.4 / AD12 / C0EX4 P2.5 / AD13 / C0EX5 P2.6 / AD14 / RXD1 P2.7 / AD15 / TXD1
P3[7:0]	Input/Output	◆ An 8-bit Quasi-bidirectional I/O port. 5V Tolerant Input. • P3.0 → RXD : Serial Port 0 Input • P3.1 → TXD : Serial Port 0 Output • P3.2 → $\overline{INT0}$: External Interrupt Input 0 • P3.3 → $\overline{INT1}$: External Interrupt Input 1 • P3.4 → T0 : Timer 0 External Input • P3.5 → T1 : Timer 1 External Input • P3.6 → $\overline{WR}$: External Data Memory Writer Strobe • P3.7 → $\overline{RD}$: External Data Memory Read Strobe	P3.0 / RXD P3.1 / $\overline{TXD}$ P3.2 / $\overline{INT0}$ P3.3 / $\overline{INT1}$ P3.4 / T0 P3.5 / T1 P3.6 / $\overline{WR}$ P3.7 / $\overline{RD}$
P4[7:0]	Input/Output	◆ An 8-bit Quasi-bidirectional 3.3V Operation I/O port. ◆ Port for digital I/O or ADC Input (3.3V). • P4.0 → ADC0 : A/D converter Input 0 • P4.1 → ADC1 : A/D converter Input 1 • P4.2 → ADC2 : A/D converter Input 2 • P4.3 → ADC3 : A/D converter Input 3 • P4.4 → ADC4 : A/D converter Input 4 • P4.5 → ADC5 : A/D converter Input 5 • P4.6 → ADC6 : A/D converter Input 6 • P4.7 → ADC7 : A/D converter Input 7	P4.0 / ADC0 P4.1 / ADC1 P4.2 / ADC2 P4.3 / ADC3 P4.4 / ADC4 P4.5 / ADC5 P4.6 / ADC6 P4.7 / ADC7

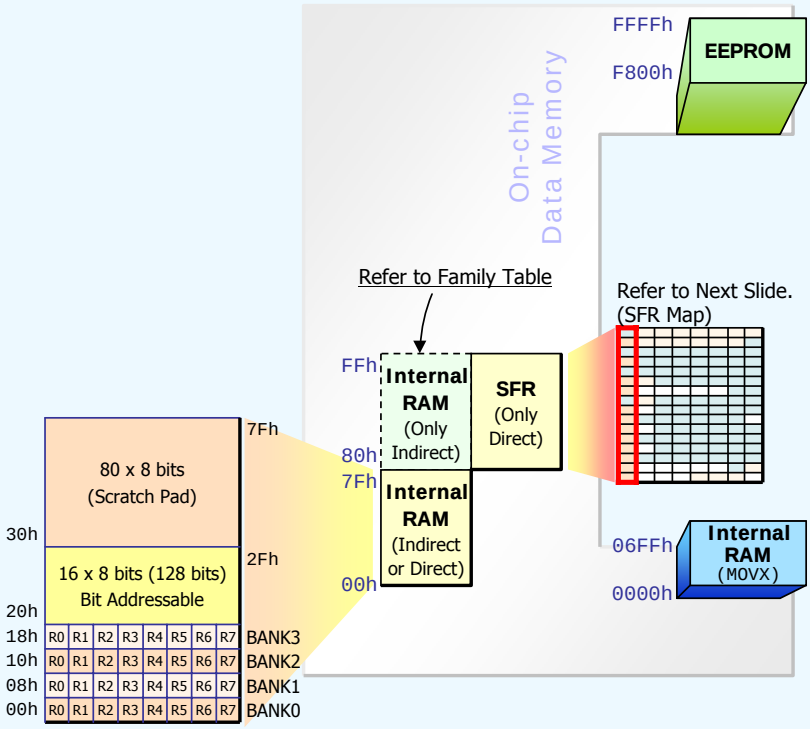
5. Pin Descriptions (Cont'd)

Symbol	Direction	Description	Share Pins
P5[7:0]	Input/Output	◆ 3.3V Operation ◆ Programmable I/O Port used as Schmitt Trigger Input or Push-pull Output. An Internal Pull-up Resistor is switched on/off by S/W. ◆ After Reset, this port will be configured as Input and the Pull-up Resistor will be switched on.	-
P6[7:0]	Input/Output	◆ 3.3V Operation ◆ Programmable I/O Port used as Schmitt Trigger Input or Push-pull Output. An Internal Pull-up Resistor is switched on/off by S/W. ◆ After Reset, this port will be configured as Input and the Pull-up Resistor will be switched on.	-
P7[7:0]	Input/Output	◆ 3.3V Operation ◆ Programmable I/O Port used as Schmitt Trigger Input or Push-pull Output. An Internal Pull-up Resistor is switched on/off by S/W. ◆ After Reset, this port will be configured as Input and the Pull-up Resistor will be switched on.	-
P8[7:0]	Input/Output	◆ 3.3V Operation ◆ Programmable I/O Port used as Schmitt Trigger Input or Push-pull Output. An Internal Pull-up Resistor is switched on/off by S/W. ◆ After Reset, this port will be configured as Input and the Pull-up Resistor will be switched on.	-
P9[7:0]	Input/Output	◆ 3.3V Operation ◆ Programmable I/O Port used as Schmitt Trigger Input or Push-pull Output. An Internal Pull-up Resistor is switched on/off by S/W. ◆ After Reset, this port will be configured as Input and the Pull-up Resistor will be switched on.	-

6.1. Memory Organization



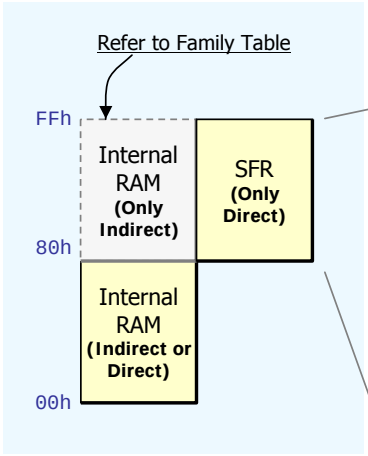
[On-chip Program Memory]
(Read/Write with IAP)



[On-chip Data Memory]
(Read and Write)

[Off-chip Data Memory]
(Read and Write)

6.2. SFR (Special Function Register) Map



: Newly added SFR at MiDAS2.0 Family

: Reserved for future use.

Bit addressable

F8h	EIP								FFh
F0h	B							FAEN	F7h
E8h	EIE	P9PUP	C1L	C1H	ADCHEN	ADCSEL	ADCR	ADCON	EFh
E0h	ACC	P8PUP	C1CAPM0	C1CAPM1	C1CAPM2	C1CAPM3	C1CAPM4	C1CAPM5	E7h
D8h	WDCON	P7PUP	C1CAP0H	C1CAP1H	C1CAP2H	C1CAP3H	C1CAP4H	C1CAP5H	DFh
D0h	PSW		C1CAP0L	C1CAP1L	C1CAP2L	C1CAP3L	C1CAP4L	C1CAP5L	D7h
C8h	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	C1CON	C1MOD	CFh
C0h	P4		P5PUP	P6PUP	PMR	STATUS	OSCICN	IOCFG	C7h
B8h	IP	SADEN	P5DIR	P6DIR	P7DIR	P8DIR	P9DIR	AUXAD	BFh
B0h	P3	SCON1	P5	P6	P7	P8	P9	IPH	B7h
A8h	IE	SADDR	SADDR1	SADEN1	C0CON	C0MOD	C0L	C0H	AFh
A0h	P2	SBUF1	C0CAPM0	C0CAPM1	C0CAPM2	C0CAPM3	C0CAPM4	C0CAPM5	A7h
98h	SCON	SBUF	C0CAP0H	C0CAP1H	C0CAP2H	C0CAP3H	C0CAP4H	C0CAP5H	9Fh
90h	P1	EXIF	C0CAP0L	C0CAP1L	C0CAP2L	C0CAP3L	C0CAP4L	C0CAP5L	97h
88h	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON		8Fh
80h	P0	SP	DPL	DPH				PCON	87h

(for 100-TQFP)

6.2. SFR Brief Description

- 80C52 SFR Registers

Register	Name	Reset Value
ACC	Accumulator	00000000
B	B Register	00000000
PSW	Program Status Word	00000000
SP	Stack Pointer	00000111
DPTR	Data Pointer (2 bytes)	
DPL	Low byte	00000000
DPH	High byte	00000000
P0	Port 0	11111111
P1	Port 1	11111111
P2	Port 2	11111111
P3	Port 3	11111111
IP	Interrupt Priority Low	10000000
IPH	Interrupt Priority High	10000000
IE	Interrupt Enable Control	00000000
TCON	T/C 0/1 Control	00000000
TMOD	T/C 0/1 Mode Control	00000000
T2CON	T/C 2 Control	00000000
T2MOD	T/C 2 Mode Selection	******00
TH0	T/C 0 High byte	00000000
TL0	T/C 0 Low byte	00000000
TH1	T/C 1 High byte	00000000
TL1	T/C 1 Low byte	00000000
TH2	T/C 2 High byte	00000000
TL2	T/C 2 Low byte	00000000
RCAP2H	T/C 2 Capture Reg. High byte	00000000
RCAP2L	T/C 2 Capture Reg. Low byte	00000000
SCON	Serial Port Control of UART0	00000000
SBUF	Serial Data Buffer of UART0	00000000
SADEN	Slave Address Mask Enable of UART0	00000000
SADDR	Slave Address of UART0	00000000
PCON	Power Control	00*10000

- Newly added SFR Registers in MiDAS2.0 Family

Register	Name	Reset Value
P5PUP	Port 5 Pull-up Control	11111111
P6PUP	Port 6 Pull-up Control	11111111
P7PUP	Port 7 Pull-up Control	11111111
P8PUP	Port 8 Pull-up Control	11111111
P9PUP	Port 9 Pull-up Control	11111111
P5DIR	Port 5 Input/Output Control	11111111
P6DIR	Port 6 Input/Output Control	11111111
P7DIR	Port 7 Input/Output Control	11111111
P8DIR	Port 8 Input/Output Control	11111111
P9DIR	Port 9 Input/Output Control	11111111
P4	Port 4	11111111
P5	Port 5	11111111
P6	Port 6	11111111
P7	Port 7	11111111
P8	Port 8	11111111
P9	Port 9	11111111
SCON1	Serial Port Control of UART1	00000000
SBUF1	Serial Data Buffer of UART1	00000000
SADDR1	Slave Address of UART1	00000000
SADEN1	Slave Address Mask Enable of UART1	00000000
ADCON	ADC Control & ADC Result Low	0010**00
ADCR	ADC Result High	00000000
ADCSEL	ADC Clock & MUX Selection	000**000
ADCHEN	ADC Input Channel Enable	00000000
EIP	Extended Interrupt Priority	00000000
EIE	Extended Interrupt Enable	00000000
AUXAD	High Address for MOVX with Ri	00000000
WDCON	Watchdog Timer & Power Status	*1010000
FAEN	IAP Routine Access Enable	*******0

*** : Don't touch bit.**

6.2. SFR Brief Description (Cont'd)

- Newly added SFR Registers in MiDAS2.0 Family (Cont'd)

Register	Name	Reset Value
PMR	Power Management	****00**
EXIF	External Interrupt Flag	00001001
CKCON	Clock Control	11000*00
STATUS	Crystal Status	***1****
OSCICN	Internal RING Oscillator Control	*****100
IOCFG	I/O Configuration	****0**0
C0L	Low Byte of PCA0 Counter	00000000
C0H	High Byte of PCA0 Counter	00000000
C0CON	PCA0 Counter Control	00000000
C0MOD	PCA0 Counter Mode	00*00000
C0CAPM0	Mode Control of PCA0 MODULE0	01000000
C0CAPM1	Mode Control of PCA0 MODULE1	01000000
C0CAPM2	Mode Control of PCA0 MODULE2	01000000
C0CAPM3	Mode Control of PCA0 MODULE3	01000000
C0CAPM4	Mode Control of PCA0 MODULE4	01000000
C0CAPM5	Mode Control of PCA0 MODULE5	01000000
C0CAP0L	Low Capture/Compare of PCA0 MODULE0	00000000
C0CAP1L	Low Capture/Compare of PCA0 MODULE1	00000000
C0CAP2L	Low Capture/Compare of PCA0 MODULE2	00000000
C0CAP3L	Low Capture/Compare of PCA0 MODULE3	00000000
C0CAP4L	Low Capture/Compare of PCA0 MODULE4	00000000
C0CAP5L	Low Capture/Compare of PCA0 MODULE5	00000000
C0CAP0H	High Capture/Compare of PCA0 MODULE0	00000000
C0CAP1H	High Capture/Compare of PCA0 MODULE1	00000000
C0CAP2H	High Capture/Compare of PCA0 MODULE2	00000000
C0CAP3H	High Capture/Compare of PCA0 MODULE3	00000000
C0CAP4H	High Capture/Compare of PCA0 MODULE4	00000000
C0CAP5H	High Capture/Compare of PCA0 MODULE5	00000000

Register	Name	Reset Value
C1L	Low Byte of PCA1 Counter	00000000
C1H	High Byte of PCA1 Counter	00000000
C1CON	PCA1 Counter Control	00000000
C1MOD	PCA1 Counter Mode	00*00000
C1CAPM0	Mode Control of PCA1 MODULE0	01000000
C1CAPM1	Mode Control of PCA1 MODULE1	01000000
C1CAPM2	Mode Control of PCA1 MODULE2	01000000
C1CAPM3	Mode Control of PCA1 MODULE3	01000000
C1CAPM4	Mode Control of PCA1 MODULE4	01000000
C1CAPM5	Mode Control of PCA1 MODULE5	01000000
C1CAP0L	Low Capture/Compare of PCA1 MODULE0	00000000
C1CAP1L	Low Capture/Compare of PCA1 MODULE1	00000000
C1CAP2L	Low Capture/Compare of PCA1 MODULE2	00000000
C1CAP3L	Low Capture/Compare of PCA1 MODULE3	00000000
C1CAP4L	Low Capture/Compare of PCA1 MODULE4	00000000
C1CAP5L	Low Capture/Compare of PCA1 MODULE5	00000000
C1CAP0H	High Capture/Compare of PCA1 MODULE0	00000000
C1CAP1H	High Capture/Compare of PCA1 MODULE1	00000000
C1CAP2H	High Capture/Compare of PCA1 MODULE2	00000000
C1CAP3H	High Capture/Compare of PCA1 MODULE3	00000000
C1CAP4H	High Capture/Compare of PCA1 MODULE4	00000000
C1CAP5H	High Capture/Compare of PCA1 MODULE5	00000000

*** : Don't touch bit.**

6.3. Instruction Set Summary

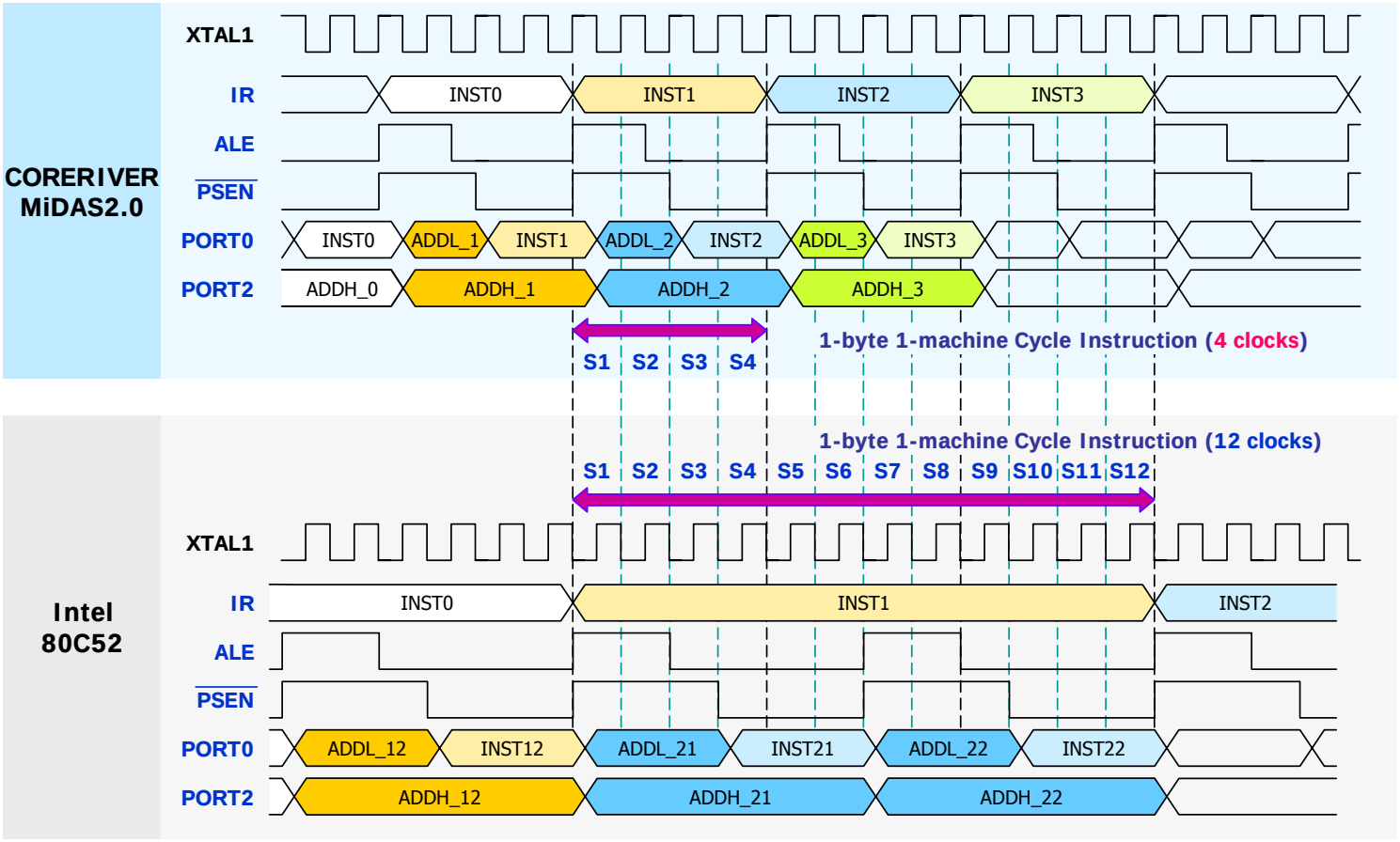
- Refer to Appendix A (Instruction Set) for more details.

Type	Instruction	Description
Arithmetic	**ADD**	Addition
	ADDC	Addition with Carry
	SUBB	Subtraction with Borrow
	INC	Increment
	DEC	Decrement
	MUL	Multiply
	DIV	Divide
	DA	Decimal Adjust
Logical	**ANL**	AND
	ORL	OR
	XRL	Exclusive OR
	CLR	Clear
	CPL	Complement
	RL	Rotate Left
	RLC	Rotate Left with Carry
	RR	Rotate Right
	RRC	Rotate Right with Carry
	SWAP	Swap Nibbles
Data Transfer	**MOV**	Move Data
	MOVC	Move Code
	MOVX	Move Data to Ext. RAM
	PUSH	PUSH
	POP	POP
	XCH	Exchange
	XCHD	Exchange Low-digit

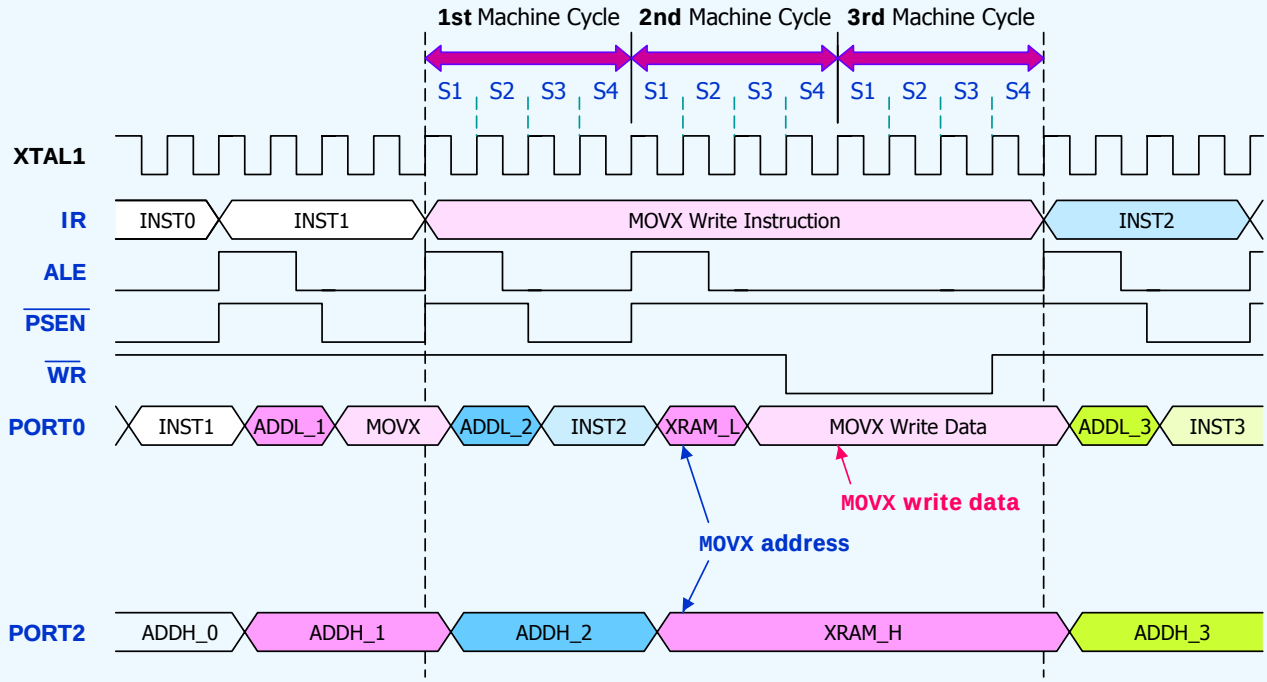
Type	Instruction	Description
Boolean	**CLR**	Clear bit
	SETB	Set bit
	CPL	Complement bit
	ANL	AND bit
	ORL	OR bit
	MOV	Move bit
	JC	Jump if Carry is set
	JNC	Jump if Carry is not set
	JB	Jump if bit is set
	JNB	Jump if bit is not set
	JBC	Jump if bit is set & clear
Branch	**ACALL**	Absolute Call
	LCALL	Long Call
	RET	Return from Subroutine
	RETI	Return from Interrupt
	AJMP	Absolute Jump
	LJMP	Long Jump
	SJMP	Short Jump
	JMP	Jump with DPTR
	JZ	Jump if ACC is zero
	JNZ	Jump if ACC is not zero
	CJNE	Compare and Jump if not equal
	DJNZ	Decrement and Jump if not zero
	NOP	No Operation

6.4. CPU Timing

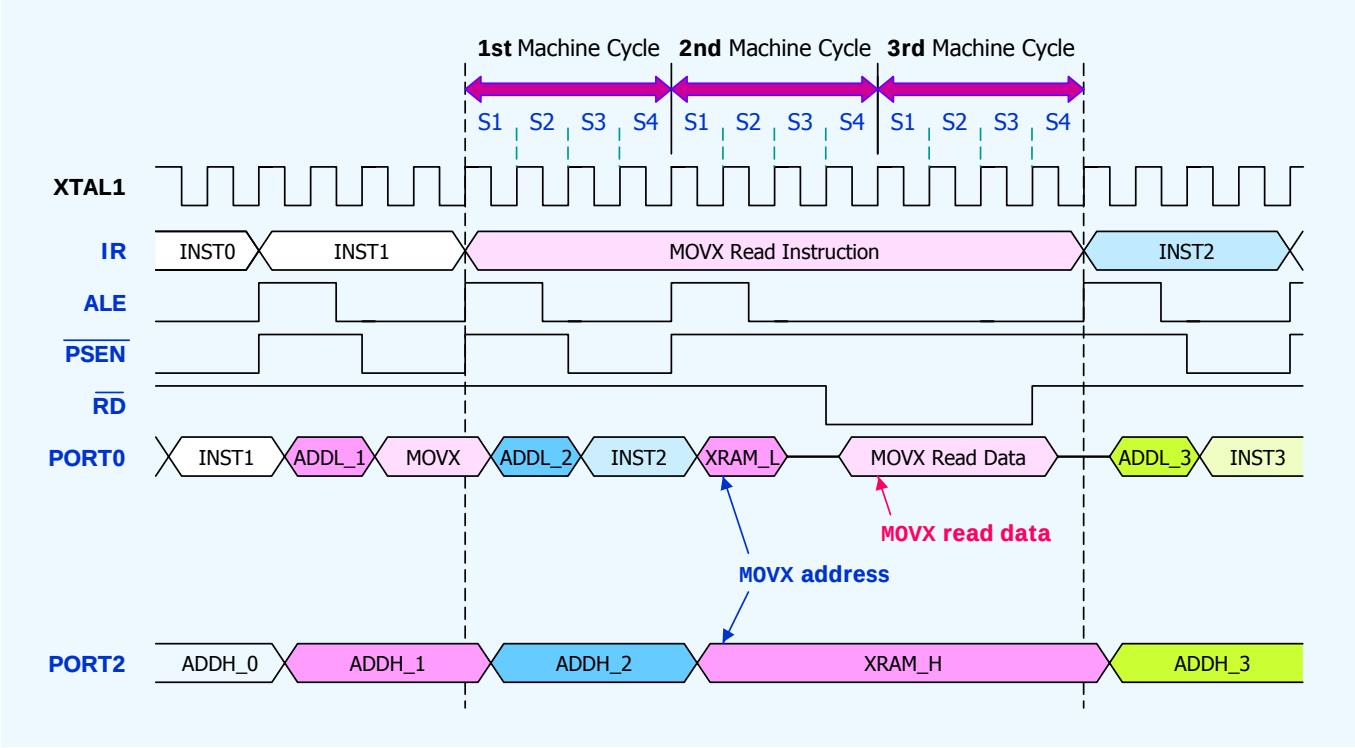
- Comparative timing of the MiDAS2.0 family and Intel 80C52



6.4. CPU Timing : MOVX Write Timing



6.4. CPU Timing : MOVX Read Timing



6.4. CPU Timing : Instruction Execution Time

- The Fastest instruction execution in the world

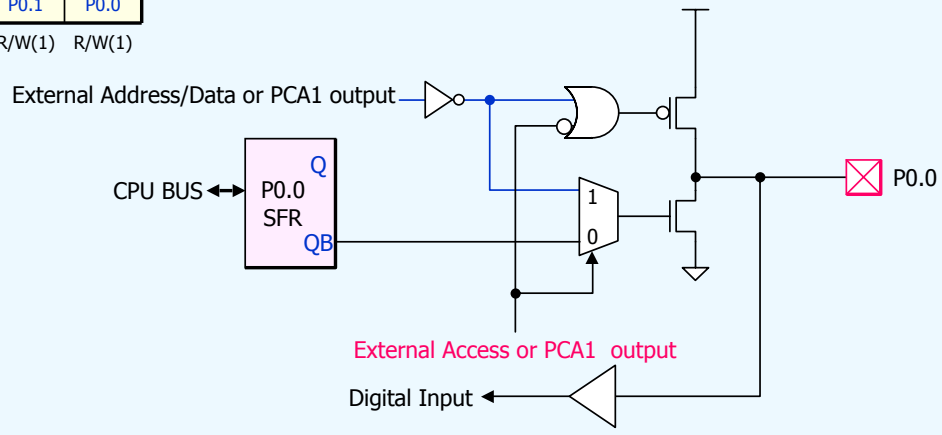
Instruction	**MiDAS2.0 (CORERIVER)**	W77C32 (Winbond)	DS80C320 (Maxim)	87C52 (Intel)
`MUL AB` `DIV AB`	**12 clocks**	20 clocks	20 clocks	48 clocks
`MOVC A, @A+PC` `MOVC A, @A+DPTR`	**8 clocks**	8 clocks	12 clocks	24 clocks
`JMP @A+DPTR`	**8 clocks**	8 clocks	12 clocks	24 clocks
`RET` `RETI`	**8 clocks**	8 clocks	16 clocks	24 clocks
`INC DPTR` `DEC DPTR`	**4 clocks** **4 clocks**	8 clocks 8 clocks	12 clocks Not exist	24 clocks Not exist
`Others`	**Same**	Same	Same	-

6.5. I/O Ports : PORT0[7:0]

- 5V tolerant input and open-drain output in default condition (Intel 8052 compatible).
- The output is fully driven (push-pull) when P0 drives address/data to access external RAM or PCA1 drives output signals (C1EXn).
- During access to external memory, P0 register will automatically be set to "FFh".
- Read-Modify-Write instructions do not read port pin but read SFR register.
  - ✓`ANL / OPL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y`
- An available alternative input functions when the corresponding SFR bit is "1" (PCA0 and PCA1 input pins).
  - ✓ C1EX0(P0.0), C1EX1(P0.1), C1EX2(P0.2), C1EX3(P0.3), C1EX4(P0.4), C1EX5(P0.5), ECI1(P0.6), ECI0(P0.7)
- PORT 0 Description

✓ **P0** (80h) : PORT 0 Register

P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



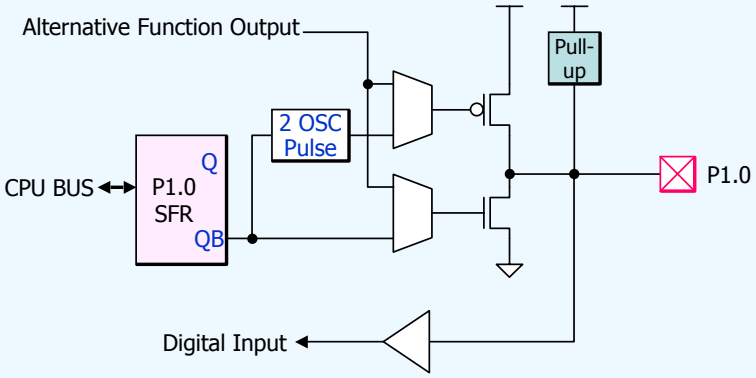
6.5. I/O Ports : PORT1[7:0] (Except 44-pin)

- An 8-bit 5V tolerant input quasi-bidirectional port (Intel 8052 compatible).
- Read-Modify-Write instructions do not read port pin but read SFR register.
  - ✓`ANL / OPL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y`
- An available alternative input functions when the corresponding SFR bit is "1".
  - ✓ P1.0 = T2 / P1.1 = T2EX / P1.4 = INT2 / P1.5 = $\overline{\text{INT3}}$ / P1.6 = INT4 / P1.7 = $\overline{\text{INT5}}$

- PORT 1 Description

✓ **P1** (90h) : PORT 1 Register

P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



6.5. I/O Ports : PORT1[7:0] (44-pin)

- 3.3V operation
- A port used as quasi-bidirectional I/O (Intel 8052 compatible) or ADC input.
- Read-Modify-Write instructions do not read port pin but read SFR register.
  - ✓`ANL / OPL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y`
- Available alternative input functions when the corresponding SFR bit is "1".
  - ✓ P1.0 = T2 / P1.1 = T2EX / P1.4 = INT2 / P1.5 = $\overline{\text{INT3}}$ / P1.6 = INT4 / P1.7 = $\overline{\text{INT5}}$
  - ✓ ADC0(P1.0), ADC1(P1.1), ADC2(P1.2), ADC3(P1.3), ADC4(P1.4), ADC5(P1.5), ADC6(P1.6), ADC7(P1.7)
- To use the digital I/O and an alternative function of the Port 1, an user must set PKGOPT bit (IOCFG.0) to 1.
- PORT 1 Description of 44-pin

✓ **ADCHEN** (ECh) : ADC Input Channel Enable Register

ADCHEN.7	ADCHEN.6	ADCHEN.5	ADCHEN.4	ADCHEN.3	ADCHEN.2	ADCHEN.1	ADCHEN.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ADCHEN.X : ADC Input Channel Enable
  0 = ADC input disable / Pull-up Resistor ON (Default)
  1 = ADC input enable / Pull-up Resistor OFF

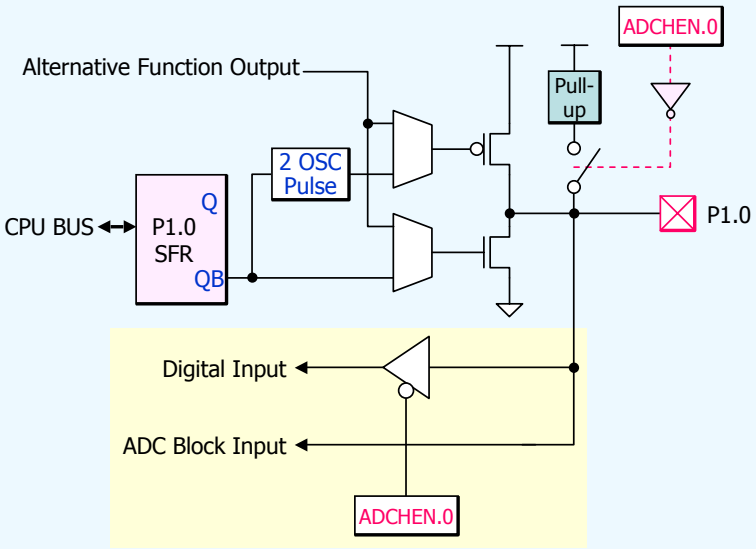
✓ **P1** (90h) : PORT 1 Register

P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

✓ **IOCFG** (C7h) : I/O Configuration Register

-	-	-	-	ENAUX	-	-	PKGOPT
				R/W(0)			R/W(0)

- PKGOPT : must be "1" for 44-pin package.

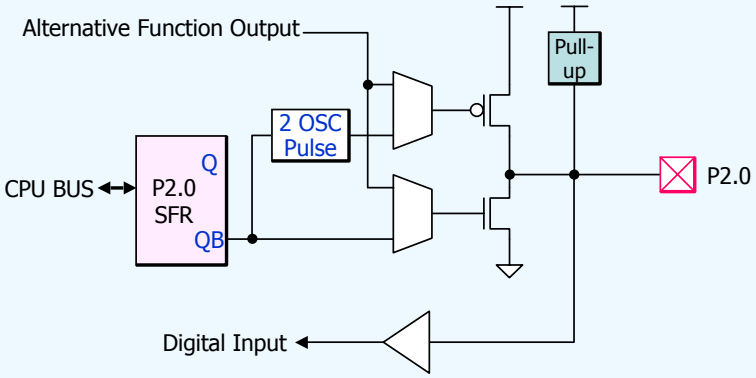


6.5. I/O Ports : PORT2[7:0]

- An 8-bit 5V tolerant input quasi-bidirectional port (Intel 8052 compatible).
- The output is fully driven (push-pull) when P2 drives the high byte of address to access external RAM or PCA0 drives output signals (C0EXn).
- Read-Modify-Write instructions do not read port pin but read SFR register.
  - ✓`ANL / OPL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y`
- An available alternative input function when the corresponding SFR bit is "1".
  - ✓ PCA0 inputs : C0EX0(P2.0), C0EX1(P2.1), C0EX2(P2.2), C0EX3(P2.3), C0EX4(P2.4), C0EX5(P2.5)
  - ✓ UART1 : RXD1(P2.6), TXD1(P2.7)
- PORT 2 Description

✓ **P2** (A0h) : PORT 2 Register

P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



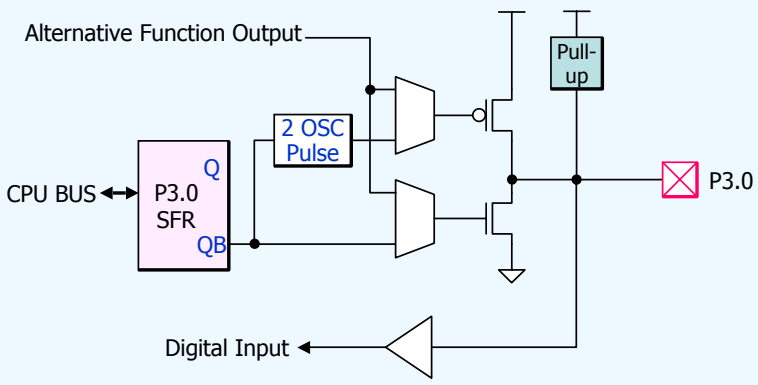
6.5. I/O Ports : PORT3[7:0]

- An 8-bit 5V tolerant input quasi-bidirectional port (Intel 8052 compatible).
- Read-Modify-Write instructions do not read port pin but read SFR register.
  - ✓`ANL / OPL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y`
- The available alternative input function when the corresponding SFR bit is "1".
  - ✓ P3.0 = RXD / P3.1 = TXD / P3.2 = $\overline{\text{INT0}}$ / P3.3 = $\overline{\text{INT1}}$ / P3.4 = T0 / P3.5 = T1 / P3.6 = $\overline{\text{WR}}$ / P3.7 = $\overline{\text{RD}}$

- PORT 3 Description

✓ **P3** (B0h) : PORT 3 Register

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



6.5. I/O Ports : PORT4[7:0]

- An 8-bit 3.3V operation quasi-bidirectional port (Intel 8052 compatible).
- Used as ADC input channel or Digital Input/Output.
- Read-Modify-Write instructions do not read port pin but read SFR register.
  - ✓`ANL / OPL / XRL / JBC / CPL / INC / DEC / DJNZ / MOV PX.Y, C / CLR PX.Y / SETB PX.Y`
- Available alternative input functions when the corresponding SFR bit is "1" (ADC input pins).
  - ✓ ADC0(P4.0), ADC1(P4.1), ADC2(P4.2), ADC3(P4.3), ADC4(P4.4), ADC5(P4.5), ADC6(P4.6), ADC7(P4.7)
  - ✓ For each ADC input channel, the corresponding channel enable bit (ADCHEN.n) must be set to "1".
- PORT 4 Description

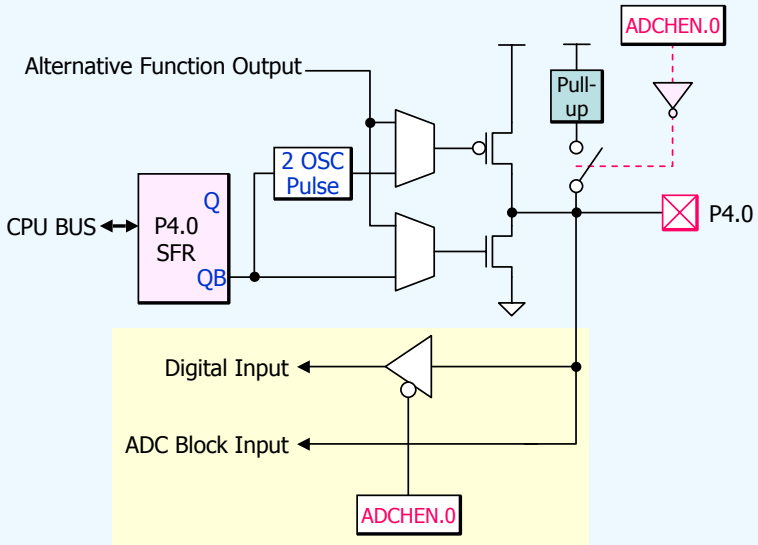
✓ **ADCHEN** (ECh) : ADC Input Channel Enable

ADCHEN.7	ADCHEN.6	ADCHEN.5	ADCHEN.4	ADCHEN.3	ADCHEN.2	ADCHEN.1	ADCHEN.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ADCHEN.X : ADC Input Channel Enable
  0 = ADC input disable / Pull-up Resistor ON (Default)
  1 = ADC input enable / Pull-up Resistor OFF

✓ **P4** (C0h) : PORT 4 Register

P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



6.5. I/O Ports : PORT5[7:0]

- 3.3V operation and push-pull output.
- A pull-up is switched on/off by changing the value of the P5UP register.
- I/O direction is determined by the value of the P5DIR register.

- PORT 5 Description

✓ **P5DIR** (BAh) : PORT 5 Input/Output Control Register

P5DIR.7	P5DIR.6	P5DIR.5	P5DIR.4	P5DIR.3	P5DIR.2	P5DIR.1	P5DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- P5DIR.X : 1 = Input (Default) / 0 = Output

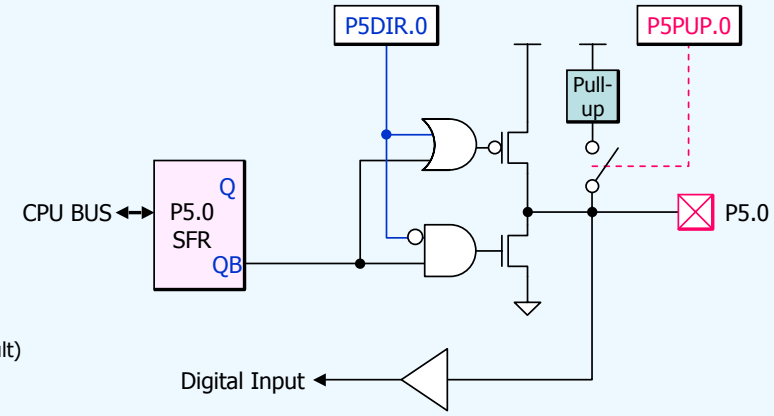
✓ **P5PUP** (C2h) : PORT 5 Pull-up Control Register

P5PUP.7	P5PUP.6	P5PUP.5	P5PUP.4	P5PUP.3	P5PUP.2	P5PUP.1	P5PUP.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- P5PUP.X : 0 = Pull-up resistor OFF, 1 = Pull-up resistor ON (Default)

✓ **P5** (B2h) : PORT 5 Register

P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



6.5. I/O Ports : PORT6[7:0]

- 3.3V operation and push-pull output.
- A pull-up is switched on/off by changing the value of the P6UP register.
- I/O direction is determined by the value of the P6DIR register.

- PORT 6 Description

✓ **P6DIR** (BBh) : PORT 6 Input/Output Control Register

P6DIR.7	P6DIR.6	P6DIR.5	P6DIR.4	P6DIR.3	P6DIR.2	P6DIR.1	P6DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- P6DIR.X : 1 = Input (Default) / 0 = Output

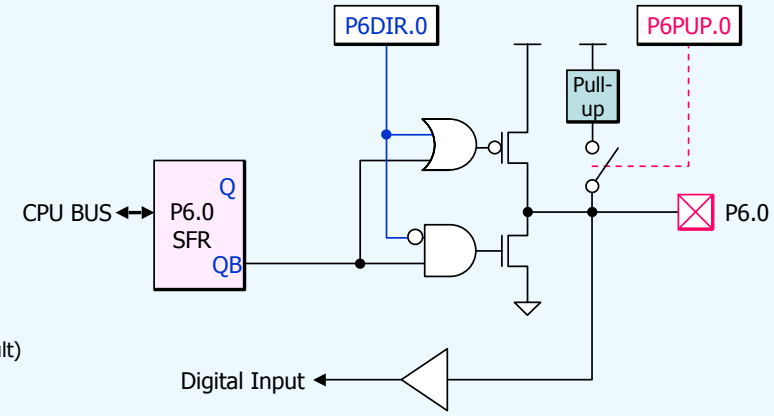
✓ **P6PUP** (C3h) : PORT 6 Pull-up Control Register

P6PUP.7	P6PUP.6	P6PUP.5	P6PUP.4	P6PUP.3	P6PUP.2	P6PUP.1	P6PUP.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- P6PUP.X : 0 = Pull-up resistor OFF, 1 = Pull-up resistor ON (Default)

✓ **P6** (B3h) : PORT 6 Register

P6.7	P6.6	P6.5	P6.4	P6.3	P6.2	P6.1	P6.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



6.5. I/O Ports : PORT7[7:0]

- 3.3V operation and push-pull output.
- A pull-up is switched on/off by changing the value of the P7UP register.
- I/O direction is determined by the value of the P7DIR register.

- PORT 7 Description

✓ **P7DIR** (BCh) : PORT 7 Input/Output Control Register

P7DIR.7	P7DIR.6	P7DIR.5	P7DIR.4	P7DIR.3	P7DIR.2	P7DIR.1	P7DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- P7DIR.X : 1 = Input (Default) / 0 = Output

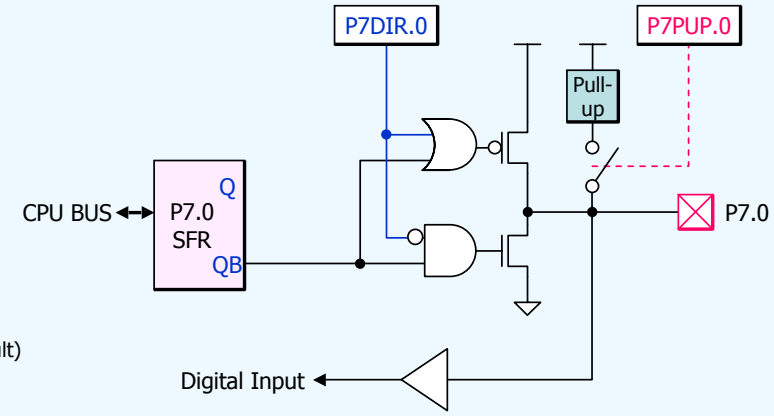
✓ **P7PUP** (D9h) : PORT 7 Pull-up Control Register

P7PUP.7	P7PUP.6	P7PUP.5	P7PUP.4	P7PUP.3	P7PUP.2	P7PUP.1	P7PUP.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- P7PUP.X : 0 = Pull-up resistor OFF, 1 = Pull-up resistor ON (Default)

✓ **P7** (B4h) : PORT 7 Register

P7.7	P7.6	P7.5	P7.4	P7.3	P7.2	P7.1	P7.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



6.5. I/O Ports : PORT8[7:0]

- 3.3V operation and push-pull output.
- A pull-up is switched on/off by changing the value of the P8UP register.
- I/O direction is determined by the value of the P8DIR register.

- PORT 8 Description

✓ **P8DIR** (BDh) : PORT 8 Input/Output Control Register

P8DIR.7	P8DIR.6	P8DIR.5	P8DIR.4	P8DIR.3	P8DIR.2	P8DIR.1	P8DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- P8DIR.X : 1 = Input (Default) / 0 = Output

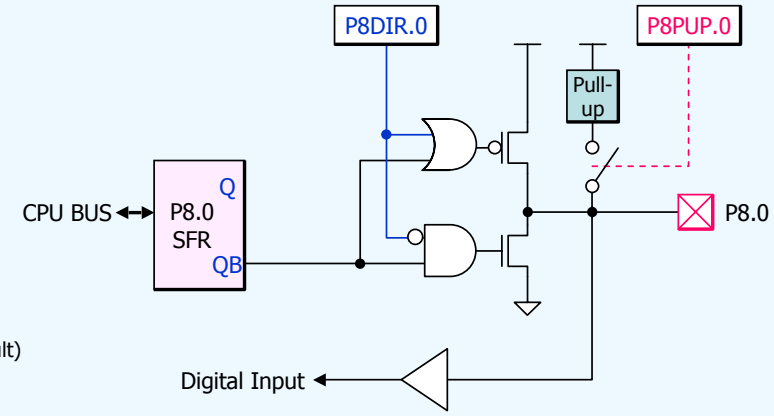
✓ **P8PUP** (E1h) : PORT 8 Pull-up Control Register

P8PUP.7	P8PUP.6	P8PUP.5	P8PUP.4	P8PUP.3	P8PUP.2	P8PUP.1	P8PUP.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- P8PUP.X : 0 = Pull-up resistor OFF, 1 = Pull-up resistor ON (Default)

✓ **P8** (B5h) : PORT 8 Register

P8.7	P8.6	P8.5	P8.4	P8.3	P8.2	P8.1	P8.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



6.5. I/O Ports : PORT9[7:0]

- 3.3V operation and push-pull output.
- A pull-up is switched on/off by changing the value of the P9UP register.
- I/O direction is determined by the value of the P9DIR register.

- PORT 9 Description

✓ **P9DIR** (BEh) : PORT 9 Input/Output Control Register

P9DIR.7	P9DIR.6	P9DIR.5	P9DIR.4	P9DIR.3	P9DIR.2	P9DIR.1	P9DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- P9DIR.X : 1 = Input (Default) / 0 = Output

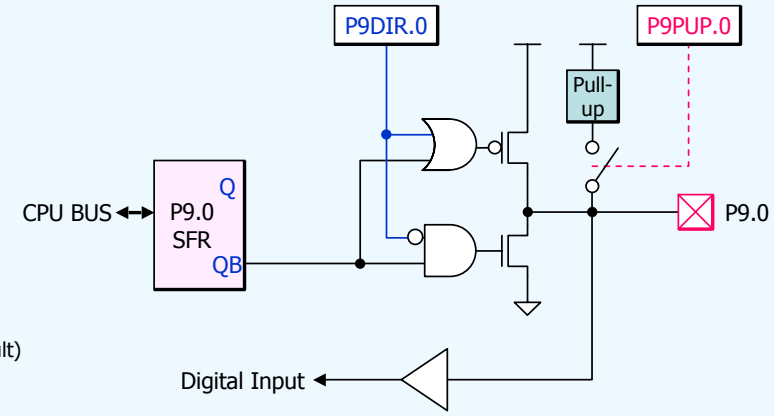
✓ **P9PUP** (E9h) : PORT 9 Pull-up Control Register

P9PUP.7	P9PUP.6	P9PUP.5	P9PUP.4	P9PUP.3	P9PUP.2	P9PUP.1	P9PUP.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- P9PUP.X : 0 = Pull-up resistor OFF, 1 = Pull-up resistor ON (Default)

✓ **P9** (B6h) : PORT 9 Register

P9.7	P9.6	P9.5	P9.4	P9.3	P9.2	P9.1	P9.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)



6.5. I/O Ports : PORT Configuration

- MiDAS2.0 family provides a dedicated address register for `movx` instructions using Ri.
  - ✓ If configured so, the AUXAD register provides the high byte of address for `movx` instruction instead of P2 SFR.
  - ✓ Then, the PORT2 can be used exclusively as general purpose I/O or PCA I/O on the condition that an user accesses only the internal RAM (0000h ~ 06FFh).
  - ✓ To enable this feature, set ENAUX bit (IOCFG.3) to 1.
  - ✓ To use pdata type in KEIL compiler with MiDAS2.0, User must set ENAUX bit.
- PORT1 enable of 44-pin packages.
  - ✓ To use digital I/O or an alternative function of PORT1, an user must set PKGOPT bit (IOCFG.0) to 1.
  - ✓ This configuration is required only for 44-PLCC and 44-MQFP.

✓ **AUXAD** (BFh) : High Address Register for MOVX with Ri

AUXAD.7	AUXAD.6	AUXAD.5	AUXAD.4	AUXAD.3	AUXAD.2	AUXAD.1	AUXAD.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- If ENAUX bit (IOCFG.3) is set, "MOVX A, @Ri" and "MOVX @Ri, A" instructions refer to AUXAD instead of P2 register for high address.

✓ **IOCFG** (C7h) : I/O Configuration Register

-	-	-	-	ENAUX	-	-	PKGOPT
				R/W(0)			R/W(0)

- ENAUX : Select AUXAD for MOVX with Ri.
  1 = AUXAD register serves high address for MOVX with Ri.
  0 = P2 register serves high address for MOVX with Ri.
- PKGOPT : Must be "1" for 44-pin package.

6.6. LVD (Low Voltage Detector)

- On-chip power-on reset : **2.0V**
- On-chip power-fail reset : **2.0V**
- Optional power-fail interrupt : **2.7V**
- After POR pulse is off, the internal power stabilization counter starts to run, which lengthens power-up reset to 50ms.

- Flag Transition

	POF	POR	PFI
A	X → 1	X → 1	X
B	1	1	X → 1
C	X	X	X → 1
D	X → 1	X → 1	1

- POF is a mirror of POR.

✓ **EXIF** (91h) : External Interrupt Flag Register

IE5	IE4	IE3	IE2	XT/RG	RGMD	RGSL	BGS
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(1)	R(0)	R/W(0)	R/W(1)

- BGS : Band-gap Select
  0 = LVD (POR) Block Off / 1 = LVD(POR) Block ON

✓ **PCON** (87h) : Power Control Register

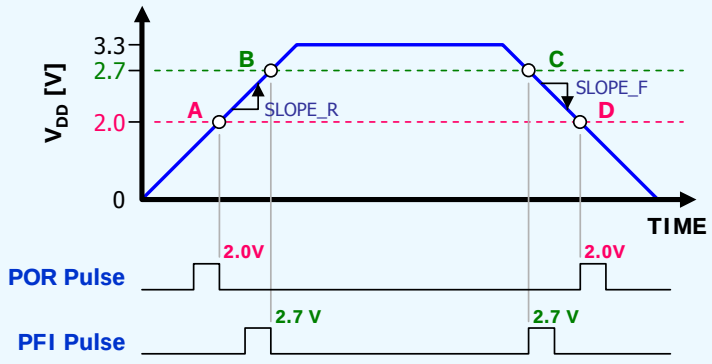
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R/W(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

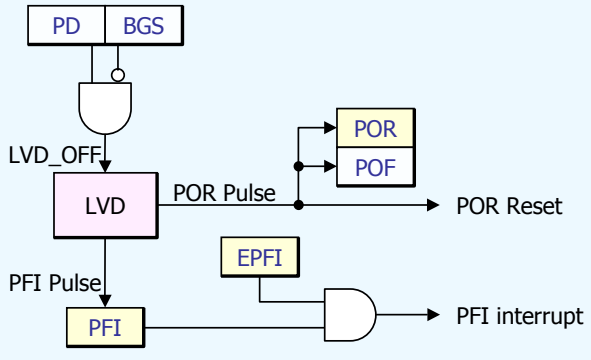
- POF : Power-off Flag
- PD : Power-down mode bit

✓ **WDCON** (D8h) : Watchdog Timer & Power Status Register

-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- POR : Power-on Reset Flag
- EPFI : Enable Power-fail Interrupt
- PFI : Power-Fail interrupt Flag





6.7. WDT (Watch Dog Timer)

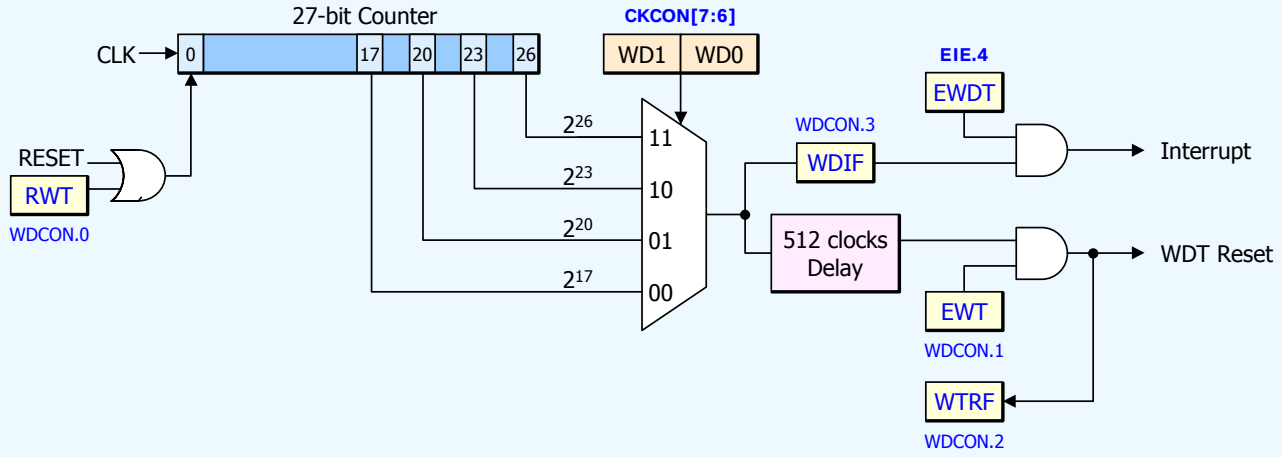
- Detects software upset due to external noise or other causes
- Allows an automatic recovery using WDT interrupt
- If enabled, WDT interrupt or WDT reset makes MCU wake up from stop mode.
- Watchdog Time-out Values (CKCON[7:6])
  - ✓ Default : WD1,WD0 = [1,1]

WD1	WD0	Interrupt Time-out (@25MHz)		Reset Time-out (@25MHz)	
0	0	2^{17} clocks	5.24 ms	2^{17} + 512 clocks	5.26 ms
0	1	2^{20} clocks	41.94 ms	2^{20} + 512 clocks	41.96 ms
1	0	2^{23} clocks	335.53 ms	2^{23} + 512 clocks	335.56 ms
1	1	2^{26} clocks	2,684.35 ms	2^{26} + 512 clocks	2,684.38 ms

✓ **WDCON** (D8h) : Watchdog Timer & Power Status Register

-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- POR : Power-on Reset Flag
- EPFI : Enable Power-fail Interrupt
- PFI : Power-Fail interrupt Flag
- WDIF : Watchdog Timer Interrupt Flag
- WTRF : Watchdog Timer Reset Flag
- EWT : Watchdog Timer Reset Enable
- RWT : Restart Watchdog Timer



6.8. Timer/Counter : Timer 0/1

- Compatible with traditional 80C52 Timer/Counter function
- Time base is selectable by S/W : 4 clocks or 12 clocks

Mode / Timer	Mode 0 (M1,M0=00)	Mode 1 (M1,M0=01)	Mode 2 (M1,M0=10)	Mode 3 (M1,M0=11)
Timer0	13-bit T/C	16-bit T/C	8-bit T/C with automatic reload (TL0 ← TH0)	8-bit T/C (TL0) ➔ Timer0 interrupt 8-bit T/C (TH0) ➔ Timer1 interrupt
Timer1	13-bit T/C	16-bit T/C	8-bit T/C with automatic reload (TL1 ← TH1)	Halt

✓ **TMOD** (89h) : Timer 0/1 Mode Control Register

GATE	C/T	M1	M0	GATE	C/T	M1	M0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Timer[1]: GATE[7], C/T[6], M1:M0[5:4]
- Timer[0]: GATE[3], C/T[2], M1:M0[1:0]
- GATE : When TRx (in TCON) is set and GATE=1, Timer x will run only while INTx pin is high (hardware control). When GATE=0, Timer x will run only while TRx=1 (software control).
- C/T : Counter or Timer Selector. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin).
- M1, M0 : Mode Selector bits
  - [0 0] Mode 0. 13-bit T/C.
  - [0 1] Mode 1. 16-bit T/C.
  - [1 0] Mode 2. 8-bit Auto-Reload T/C.
  - [1 1] Mode 3. (Timer 1) stopped, (Timer 0) TL0: 8-bit T/C controlled by the Timer 0 control bits. TH0: 8-bit T/C controlled by the Timer 1 control bits.

✓ **CKCON** (8Eh) : Clock Control Register

WD1	WD0	T2M	T1M	T0M	-	U1T2DIS	U2T2DIS
R/W(1)	R/W(1)	R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)

- T1M : Timer 1 Clock Time-base Selection T1M=1, Time-base is 4 clocks not 12 clocks.
- T0M : Timer 0 Clock Time-base Selection T0M=1, Time-base is 4 clocks not 12 clocks.

✓ **TCON** (88h) : Timer 0/1 Control Register

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- TF1 : Timer 1 Overflow Flag
- TR1 : Timer 1 Run Enable
- TF0 : Timer 0 Overflow Flag
- TR0 : Timer 0 Run Enable
- IE1 : External Interrupt 1 Flag
- IT1 : External Interrupt 1 Type Select Edge Detect (IT1=1). Level Detect (IT1=0)
- IE0 : External Interrupt 0 Flag
- IT0 : External Interrupt 0 Type Select Edge Detect (IT0=1). Level Detect (IT0=0)

✓ **TL0** (8Ah) : Timer 0 Low Byte Register

TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

✓ **TH0** (8Ch) : Timer 0 High Byte Register

TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

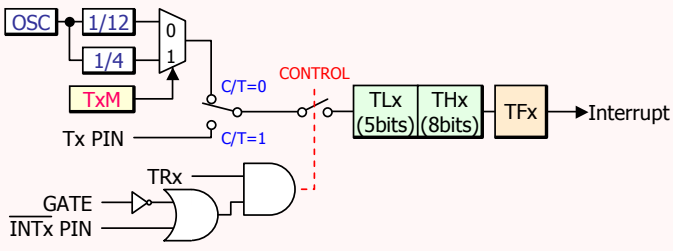
✓ **TL1** (8Bh) : Timer 1 Low Byte Register

TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

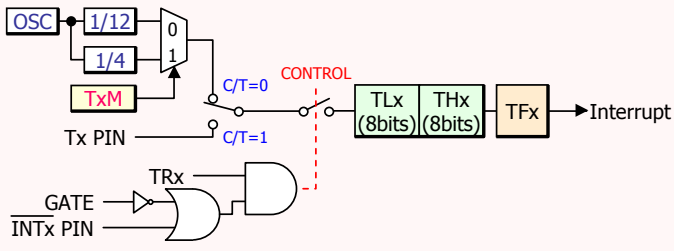
✓ **TH1** (8Dh) : Timer 1 High Byte Register

TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

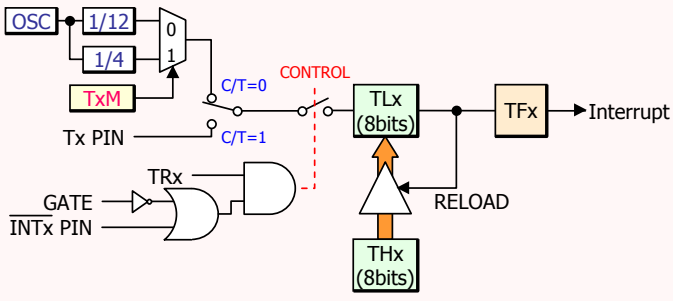
6.8. Timer/Counter : Timer 0/1 Mode Description



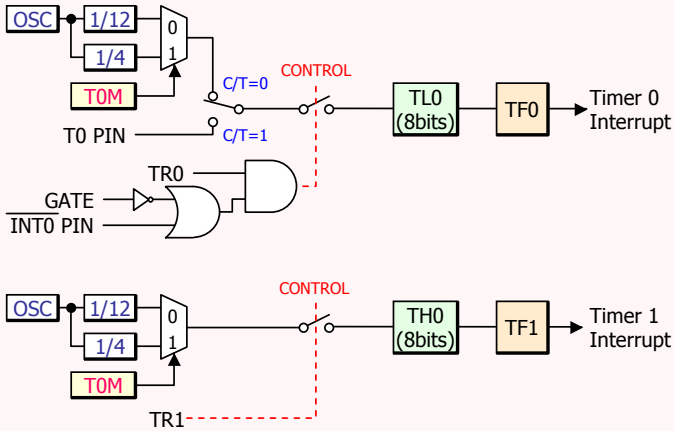
[Mode 0]



[Mode 1]



[Mode 2]



[Mode 3(Timer 0 only)]

6.8. Timer/Counter : Timer 2

- Compatible with traditional 80C52 Timer/Counter 2 function
- Up or down counting selectable by a software
- Time base is selectable by S/W : 4 clocks or 12 clocks

1. 16-bit Auto-reload [RCLK+TCLK=0, CP/RL2=0, T2OE=0]	16-bit Timer/Counter With Automatic Reload (TH2, TL2 ← RCAP2H, RCAP2L)
2. 16-bit Capture [RCLK+TCLK=0, CP/RL2=1, T2OE=0]	16-bit Timer/Counter with Capture (RCAP2H, RCAP2L ← TH2, TL2)
3. Baud Rate Generator [RCLK+TCLK=1, CP/RL2=X, T2OE=X]	Baud Rate Generation * Timer 2 Interrupt Disable
4. Programmable Clock Out [RCLK+TCLK=X, CP/RL2=0, T2OE=1]	Clock-out on P1.0

✓ **T2CON** (C8h) : Timer 2 Control Register

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- TF2 : Timer 2 Overflow Flag
- EXF2 : Timer 2 External Flag
- RCLK : Receive Clock Flag
- TCLK : Transmit Clock Flag
- EXEN2 : Timer 2 External Enable Flag
- TR2 : Timer 2 Run Enable
- C/T2 : Timer or Counter Selection. If C/T2=0, Timer Operation.
- CP/RL2 : Capture/Reload Flag.
  CP/RL2=0, Reload. (TH2,TL2) ← (RCAP2H, RCAP2L)
  CP/RL2=1, Capture. (RCAP2H, RCAP2L) ← (TH2,TL2)

✓ **CKCON** (8Eh) : Clock Control Register

WD1	WD0	T2M	T1M	T0M	-	U1T2DIS	U2T2DIS
R/W(1)	R/W(1)	R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)

- T2M : Timer 2 Clock Time-base Selection
  T2M=1, Time-base is 4 clocks not 12 clocks.

✓ **T2MOD** (C9h) : Timer 2 Mode Register

-	-	-	-	-	-	T2OE	DCEN
						R/W(0)	R/W(0)

- T2OE : Timer 2 Clock Output to P1.0
- DCEN : Timer 2 Down Count Enable

✓ **TL2** (CCh) : Timer 2 Low Byte Register

TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

✓ **TH2** (CDh) : Timer 2 High Byte Register

TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

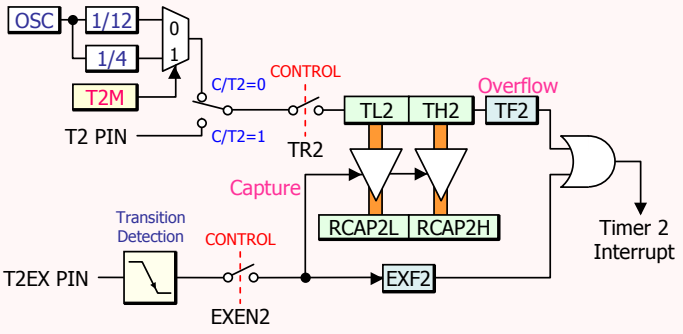
✓ **RCAP2L** (CAh) : Timer 2 Capture/Reload Low Byte Register

RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

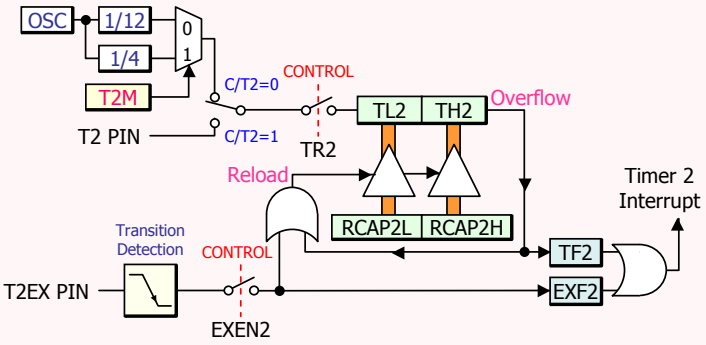
✓ **RCAP2H** (CBh) : Timer 2 Capture/Reload High Byte Register

RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

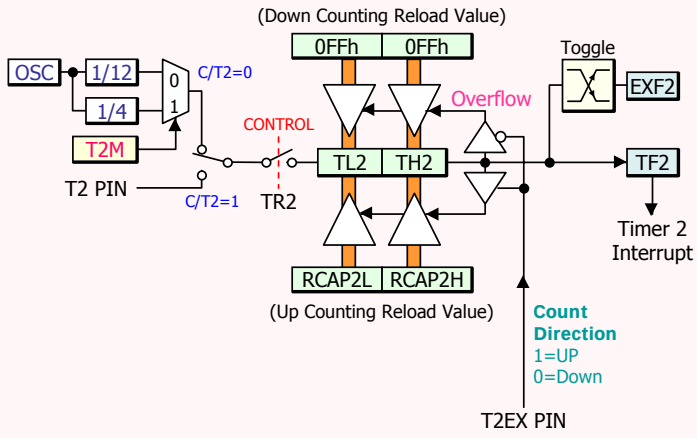
6.8. Timer/Counter : Timer 2 Mode Description



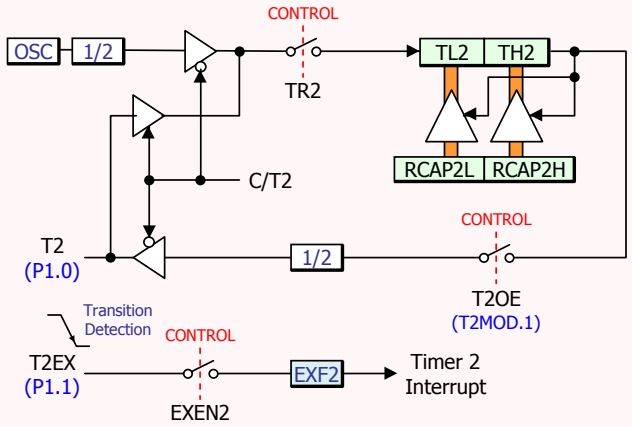
[Capture Mode]



[Auto Reload Mode (DCEN=0)]

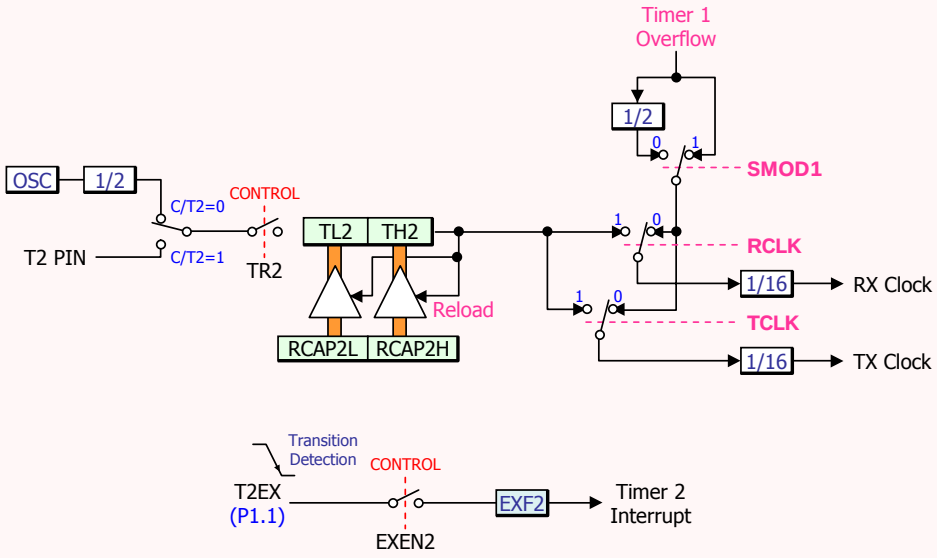


[Auto Reload Mode (DCEN=1)]



[Clock-Out Mode]

6.8. Timer/Counter : Timer 2 Mode Description



[Baud Rate Generator Mode]

6.9. UART (UART0 / UART1)

- Function-level compatible with traditional 80C52 UART.
- Automatic address recognition :
  - ✓ Multi processor communication.
- The SFR name for UART0 is the same as the legacy UART.

	Data Size		Baud Rate
Mode 0	8 bits	8 data bits	1/4 x Oscillator Clock
Mode 1	10 bits	Start bit(0) 8 data bit Stop bit(1)	1/32 x Timer 1 Overflow (SMOD1=0) 1/16 x Timer 1 Overflow (SMOD1=1) 1/16 x Timer 2 Overflow Rate
Mode 2	11 bits	Start bit(0) 8 data bit Programmable bit Stop bit(1)	1/32 x Oscillator Clock (SMOD1=0) 1/16 x Oscillator Clock (SMOD1=1)
Mode 3	11 bits	Start bit(0) 8 data bit Programmable bit Stop bit(1)	1/32 x Timer 1 Overflow (SMOD1=0) 1/16 x Timer 1 Overflow (SMOD1=1) 1/16 x Timer 2 Overflow Rate

✓ **Timer 1 Overflow varies with the CKCON register value**

➔ 12 clocks time-base or 4 clocks time-base.

✓ **PCON** (87h) : Power Control Register

SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- SMOD1 : Timer 1 baud rate double in UART mode 1, 2, and 3
- SMOD0 : Enable SM0 access. Don't modify this bit.

✓ **SCON** (98h) : Serial Port Control Register for UART0

SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- SM0, SM1 : Serial Port Mode Select
  [0,0] : Mode 0. 8-bit Shift Register (OSC/4)
  [0,1] : Mode 1. 8-bit UART (Variable)
  [1,0] : Mode 2. 9-bit UART (OSC/32 or OSC/16)
  [1,1] : Mode 3. 9-bit UART (Variable)
- SM2 : Enable the Automatic Address Recognition in Mode 2 and 3.
  Clear after receiving the address.
  In Mode 1, Valid Stop Bit Check if SM2=1.
  In Mode 0, SM2 should be 0.
- REN : Serial Reception Enable.
- TB8 : 9th data bit that will be transmitted in Mode 2 and 3.
- RB8 : 9th data bit that was received in Mode 2 and 3.
  In Mode 1, RB8 is equal to Stop Bit if SM2=0.
  In Mode 0, RB8 is not used.
- TI : Transmission Interrupt Flag. Must be cleared by S/W.
- RI : Reception Interrupt Flag. Must be cleared by S/W.

✓ **SBUF** (99h) : Serial Data Buffer Register for UART0

SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- The transmission buffer and the reception buffer are separated.
- The transmission/reception buffers have the same address.

6.9. UART : Automatic Address Recognition

◆ Example

Slave 1:

```
SADDR = 11110001
SADEN = 11111010
GIVEN = 11110X0X
```

Slave 2:

```
SADDR = 11110011
SADEN = 11111001
GIVEN = 11110XX1
```

- A master can selectively communicate with groups of slaves by using the Given Address.
- It sends 11110000 to communicate with just Slave 1.
- It sends 11110111 to communicate with just Slave 2.
- It sends 11110001 or 11110101 to communicate with Slave 1 and Slave 2.

✓ **SADDR**(A9h) : Slave Address Register of UART0

SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Programmed with the given or broadcast address assigned to serial port0.

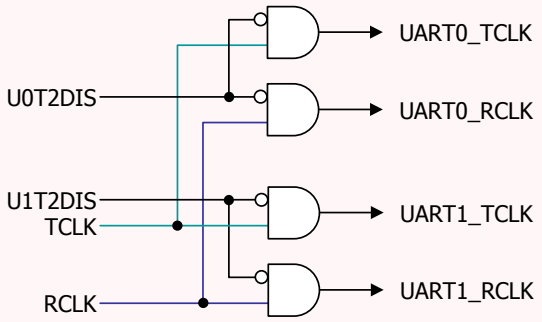
✓ **SADEN**(B9h) : Slave Address Mask Enable Register of UART0

SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ Baud Rate Discrimination between UART0 and UART1

✓ An user can selectively disable TCLK or RCLK to set UART0 and UART1 to different baud rates.

✓ For instance, if U0T2DIS is set, UART0 may use Timer1 for baud rate generation even though TCLK or RCLK bit is set.



✓ **CKCON**(8Eh) : Clock Control Register

WD1	WD0	T2M	T1M	T0M	-	U1T2DIS	U0T2DIS
R/W(1)	R/W(1)	R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)

- U1T2DIS : Used to disable RCLK/TCLK control for UART1 to generate its baud rate with T1 overflow.
- U0T2DIS : Used to disable RCLK/TCLK control for UART0 to generate its baud rate with T1 overflow.

6.9. UART : UART1 SFRs

✓ **SCON1** (B1h) : Serial Port Control Register for UART1

SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- SM0, SM1 : Serial Port Operating Mode Selection
  [0,0] : Mode 0. 8-bit Shift Register (OSC/4)
  [0,1] : Mode 1. 8-bit UART (Variable)
  [1,0] : Mode 2. 9-bit UART (OSC/32 or OSC/16)
  [1,1] : Mode 3. 9-bit UART (Variable)
- SM2 : Enable the Automatic Address Recognition in Mode 2 and 3.
  Clear after receiving the address.
  In Mode 1, the Validity of the Stop Bit is checked if SM2=1.
  In Mode 0, SM2 should be 0.
- REN : Enable/Disable Reception.
- TB8 : 9th data bit that will be transmitted in Mode 2 and 3.
- RB8 : 9th data bit that was received in Mode 2 and 3.
  In Mode 1, RB8 is equal to Stop Bit if SM2=0.
  In Mode 0, RB8 is not used.
- TI : Transmission Interrupt Flag. Must be cleared by S/W.
- RI : Reception Interrupt Flag. Must be cleared by S/W.

✓ **SBUF1** (A1h) : Serial Data Buffer for UART1

SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Transmission buffer and reception buffer are separated.
- Read and Write address are same.

✓ **SADDR1**(AAh) : Slave Address Register of UART1

SADDR1.7	SADDR1.6	SADDR1.5	SADDR1.4	SADDR1.3	SADDR1.2	SADDR1.1	SADDR1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- Programmed with the given
  or broadcast address assigned to serial port1.

✓ **SADEN1**(ABh) : Slave Address Mask Enable Register of UART1

SADEN1.7	SADEN1.6	SADEN1.5	SADEN1.4	SADEN1.3	SADEN1.2	SADEN1.1	SADEN1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

6.9. UART : Baud Rate Example

Serial Port Mode 0

$$\text{Baudrate} = \frac{\text{Oscillator Frequency}}{4}$$

Serial Port Mode 2

$$\text{Baudrate} = \frac{2^{\text{SMOD1}}}{32} \times \text{Oscillator Frequency}$$

PCON.7

Serial Port Mode 1, 3

✓ Using Timer 1 Overflow

$$\text{Baudrate} = \frac{2^{\text{SMOD1}}}{32} \times \text{Timer 1 overflow}$$

✓Using Timer 2 Overflow

$$\text{Baudrate} = \frac{\text{Timer 2 overflow}}{16}$$

EX) Using Timer 1 to Generate Baudrates

$$\text{Mode 1 \& 3 Baudrate} = \frac{2^{\text{SMOD1}}}{32} \times F_{OSC} \times \frac{3^{\text{T1M}}}{12} \times \frac{1}{[\ 256 - (\text{TH1})\ ]}$$

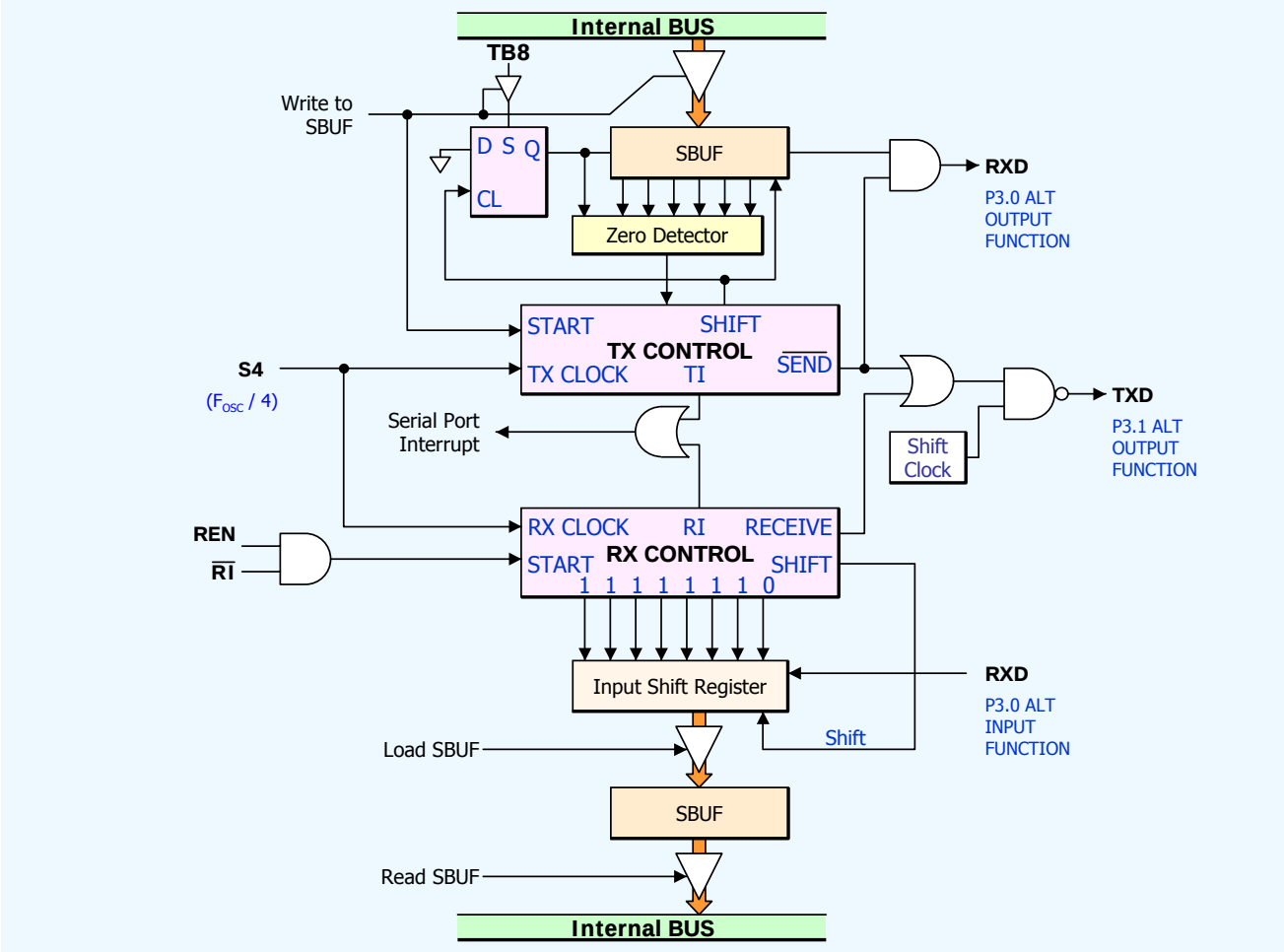
- If SMOD1(PCON.7) = 1 ➔ Double Buadrate
- If T1M(CKCON.4) = 0 ➔ 1/12 x F_{OSC}
- If T1M(CKCON.4) = 1 ➔ 1/4 X F_{OSC}

EX) Using Timer 2 to Generate Baudrates

$$\text{Mode 1 \& 3 Baudrate} = \frac{1}{32} \times F_{OSC} \times \frac{1}{[65536 - (\text{RCAPH,RCAPL})\ ]}$$

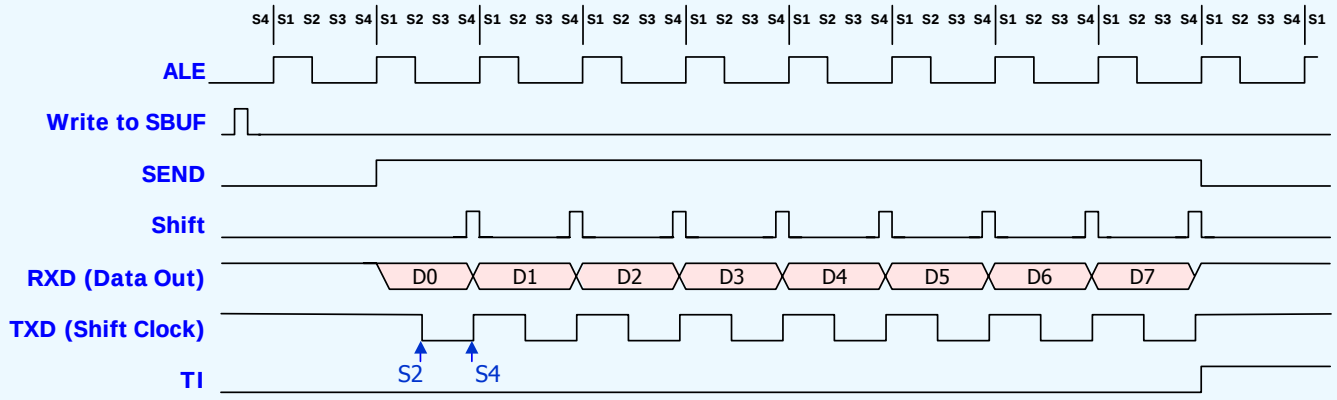
Baudrate		UART Mode	F_{OSC}	SMOD1	Timer 1		
T1M=0	T1M=1				C/T	Mode	Reload Value (TH1)
Max : 3 MHz	Max : 3 MHz	Mode 0	12 MHz	X	X	X	X
Max : 750 KHz	Max : 750 KHz	Mode 2	12 MHz	1	X	X	X
62.5 KHz	187.5 KHz	Mode 1 & 3	12 MHz	1	0	2	FFh
19.2 KHz	57.6 KHz		11.0592 MHz	1	0	2	FDh
9.6 KHz	28.8 KHz		11.0592 MHz	0	0	2	FDh
4.8 KHz	14.4 KHz		11.0592 MHz	0	0	2	FAh
2.4 KHz	7.2 KHz		11.0592 MHz	0	0	2	F4h
1.2 KHz	3.6 KHz		11.0592 MHz	0	0	2	E8h
137.5 Hz	412.5 Hz		11.0592 MHz	0	0	2	1Dh
110 Hz	330 Hz		6 MHz	0	0	2	72h
110 Hz	330 Hz		12 MHz	0	0	1	FEEBh

6.9. UART : Mode 0 Function

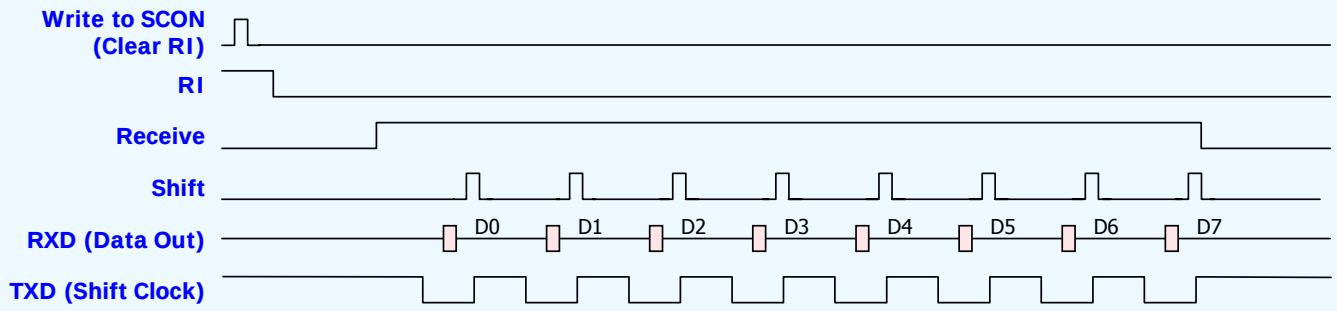


6.9. UART : Mode 0 Timing

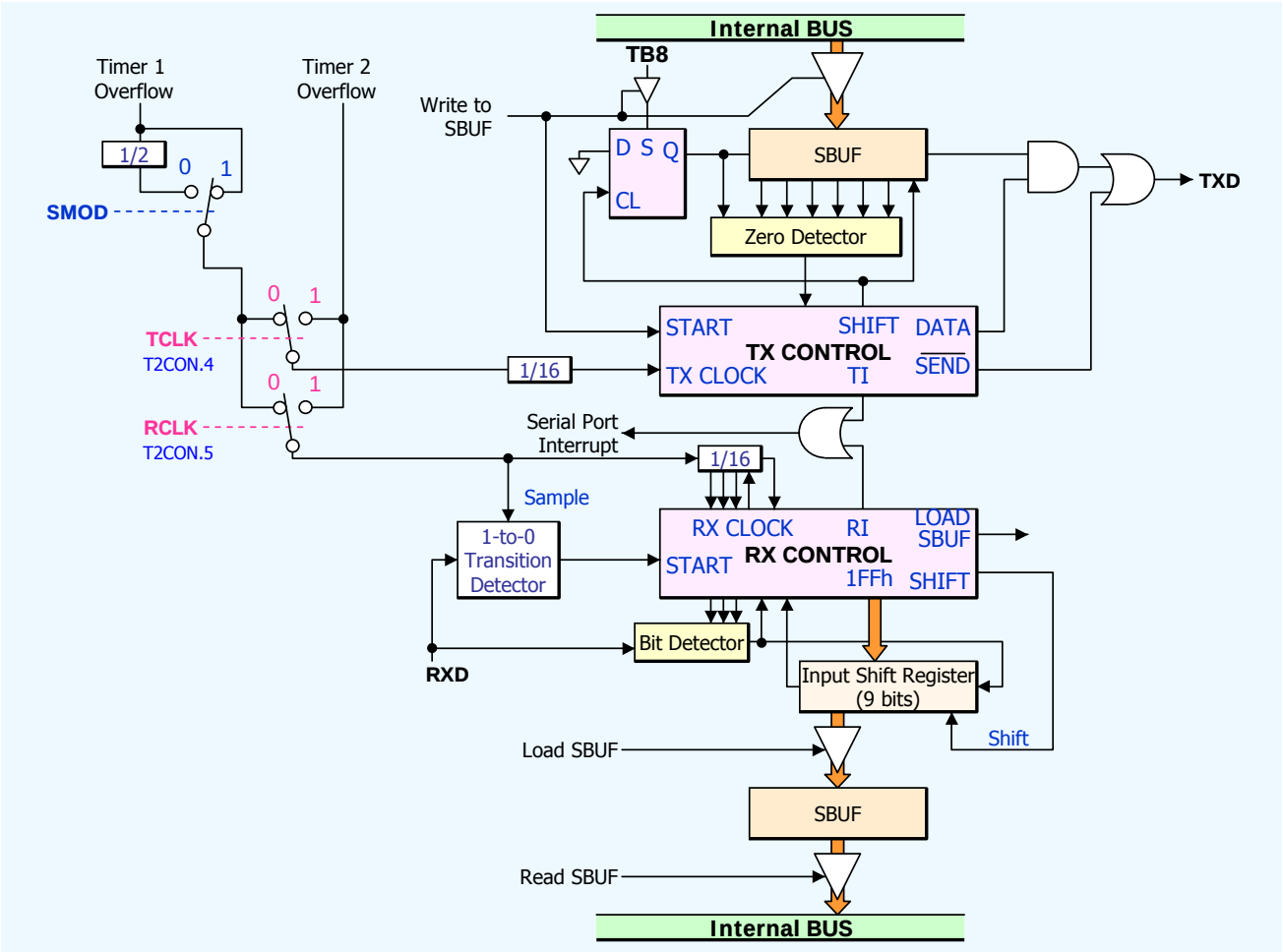
[Transmit]



[Receive]

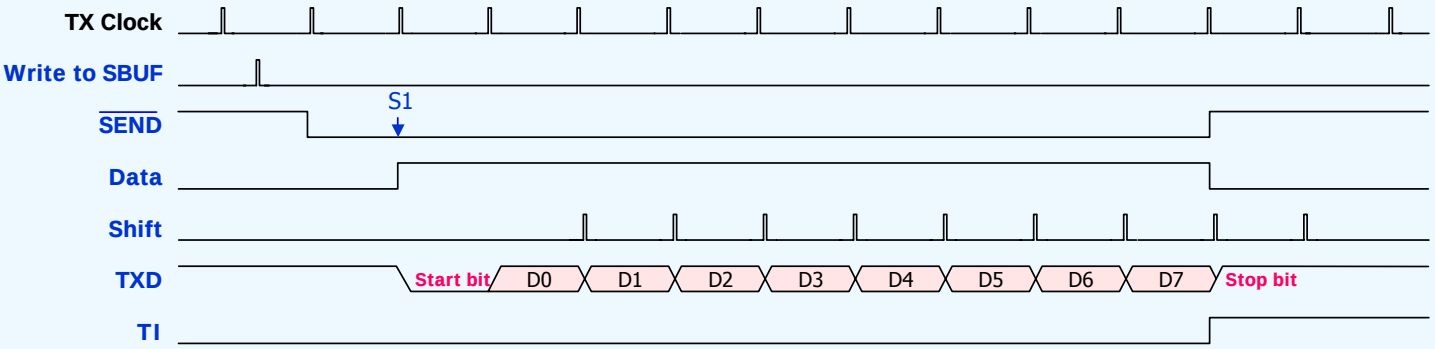


6.9. UART : Mode 1 Function

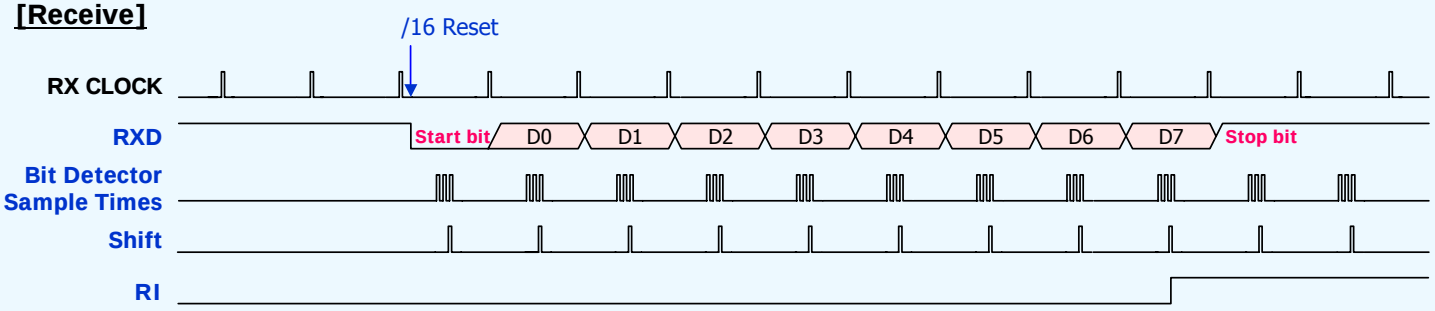


6.9. UART : Mode 1 Timing

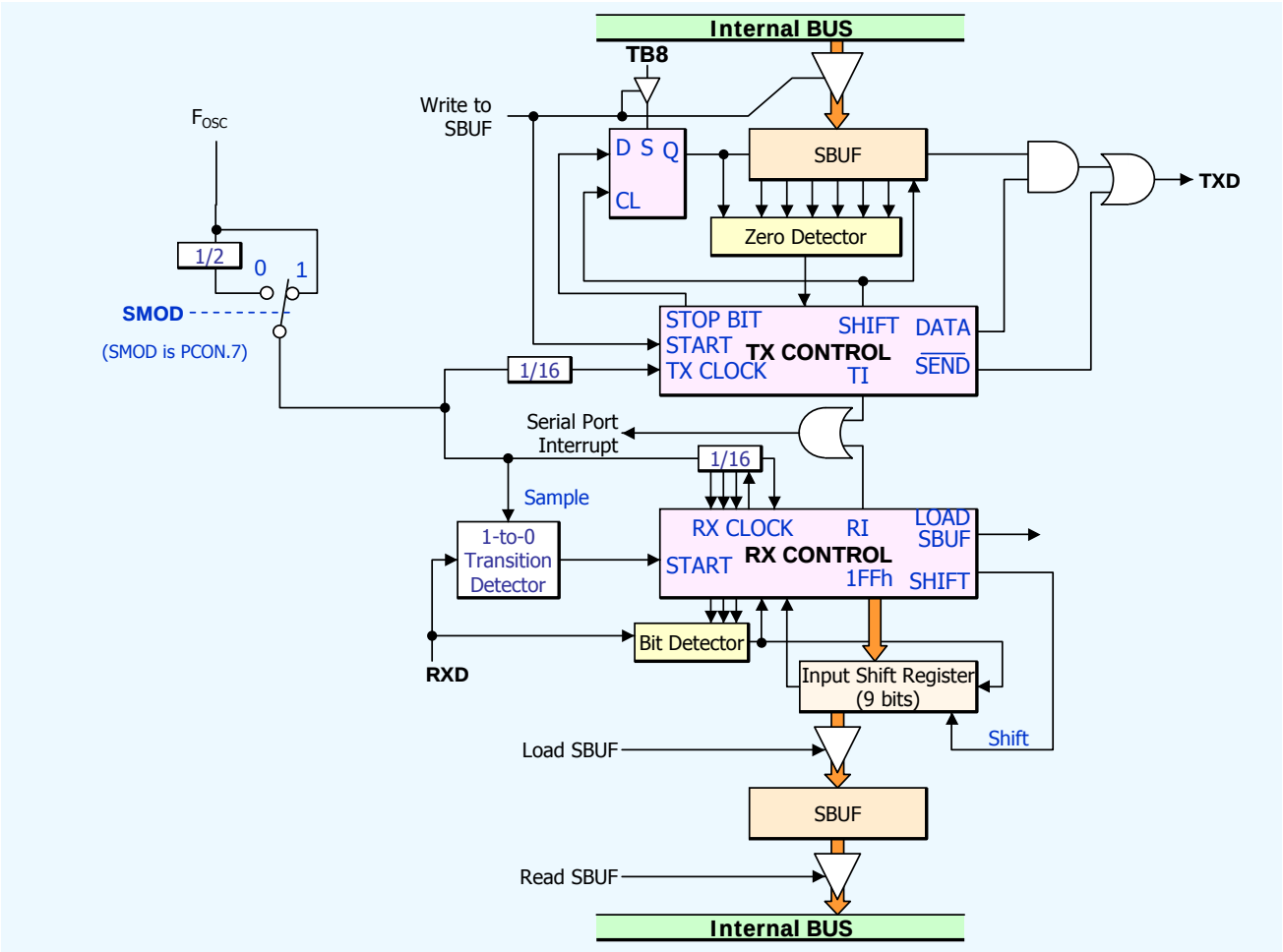
[Transmit]



[Receive]

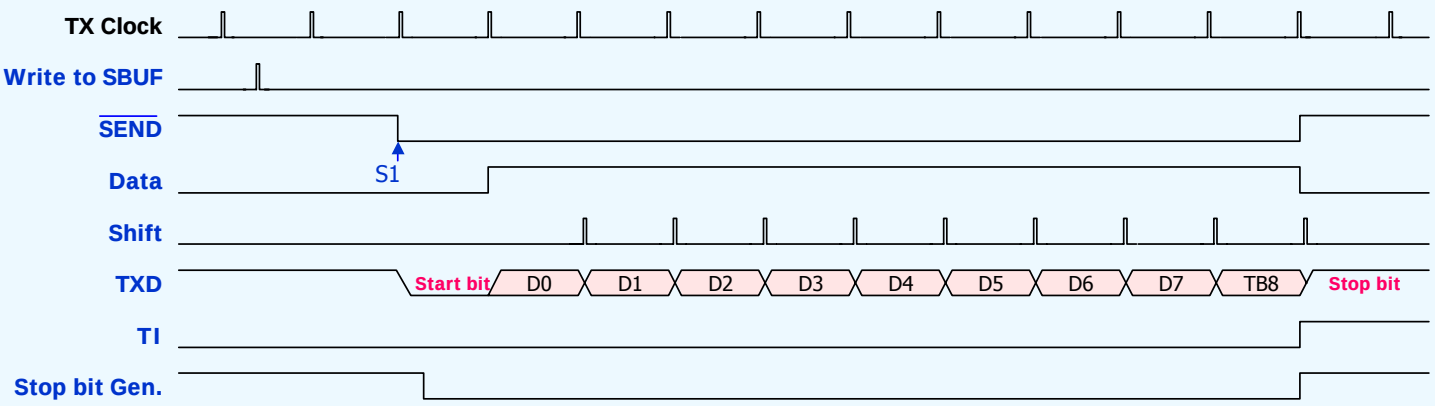


6.9. UART : Mode 2 Function

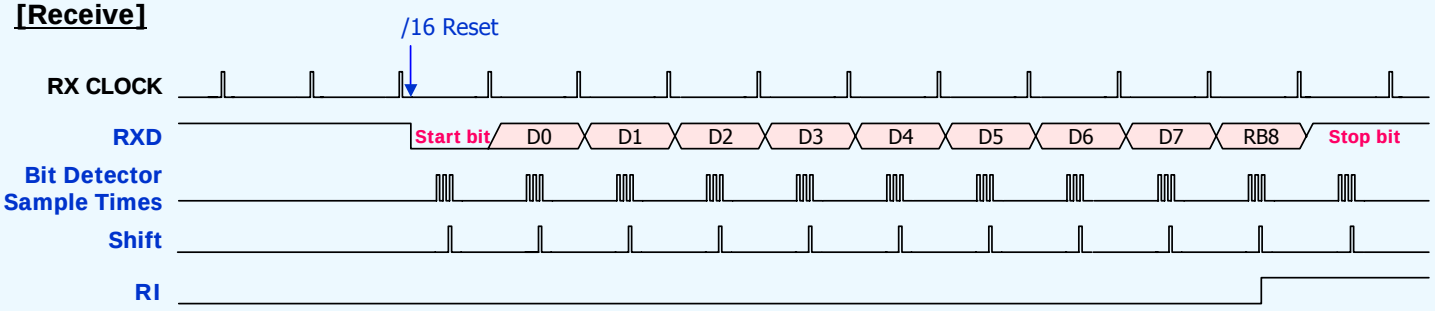


6.9. UART : Mode 2 Timing

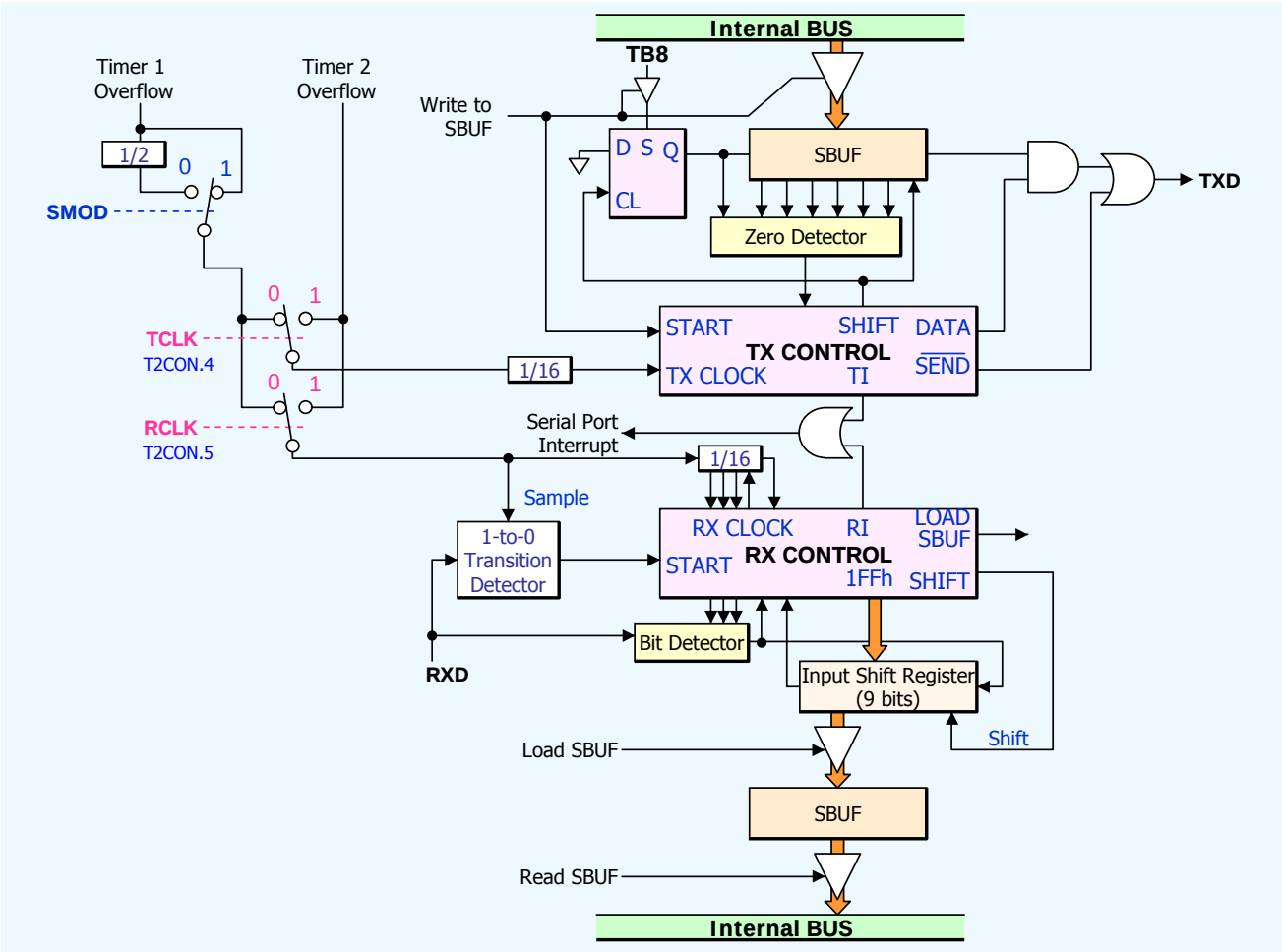
[Transmit]



[Receive]

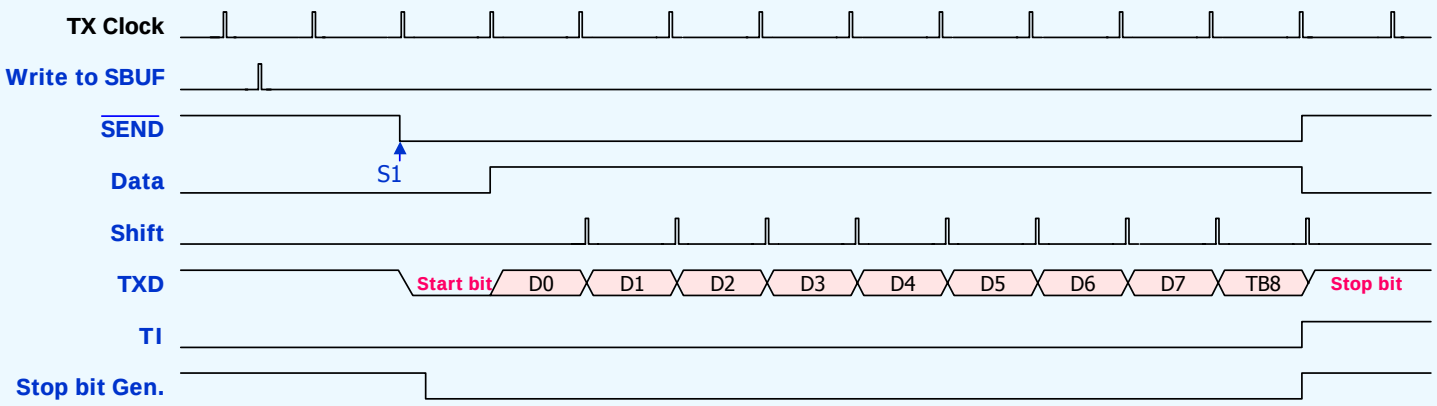


6.9. UART : Mode 3 Function

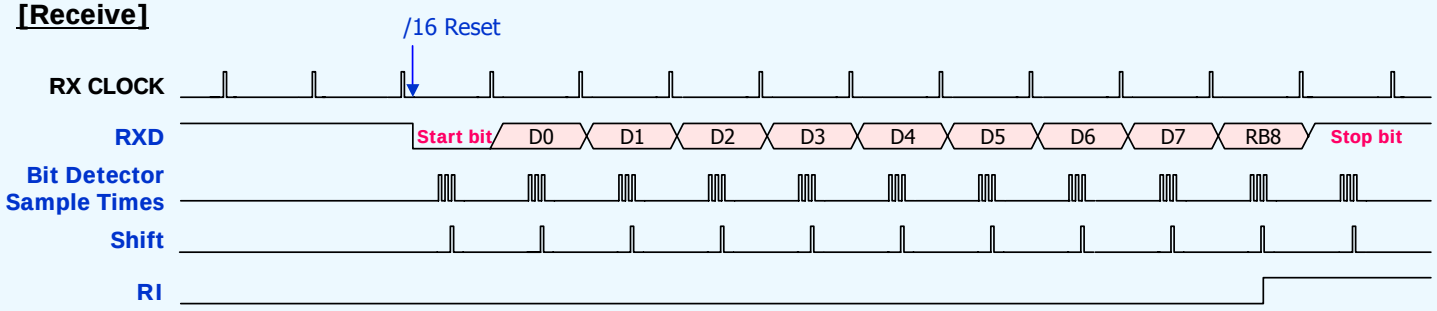


6.9. UART : Mode 3 Timing

[Transmit]



[Receive]

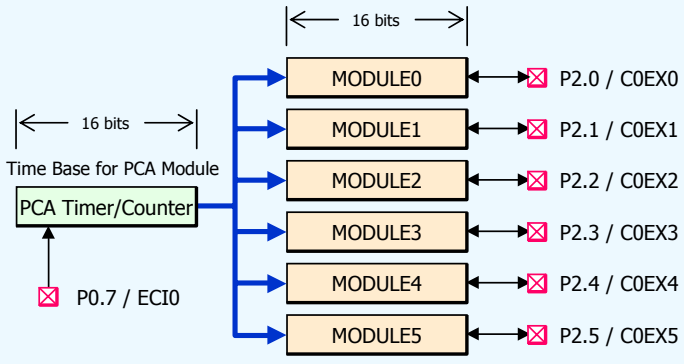


6.10. PCA (Programmable Counter Arrays)

- Basic Feature
  - ✓ Support Intel/Philips compatible functions.

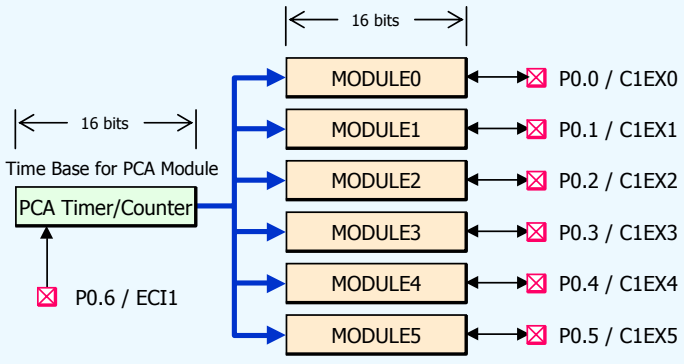
- Unique Features
  - ✓ Each PCA provides 6 modules.
  - ✓ In the auto-reset mode, C0L (or C1L) is reset when a match occurs between C0L (or C1L) and C0H (or C1H).
  - ✓ Support Dynamic PWM (Pulse Width Modulation) by using the auto-reset mode.
  - ✓ An 8-bit prescaler generates the PCA clock.

[PCA0]



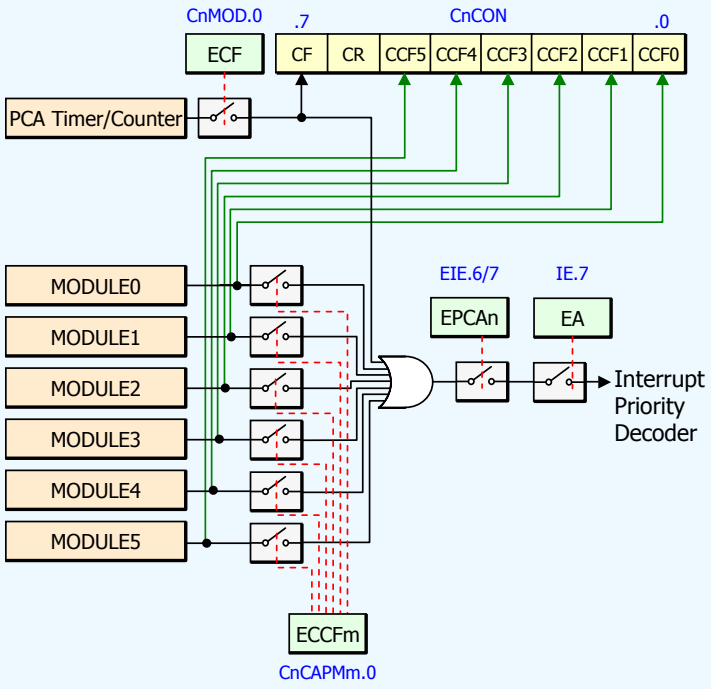
- **Module Functions:**
  - 16-bit Capture
  - 16-bit Timer
  - 16-bit High Speed Output
  - **8-bit Fixed PWM Output**
  - **8-bit Dynamic PWM Output**

[PCA1]



- **Module Functions:**
  - 16-bit Capture
  - 16-bit Timer
  - 16-bit High Speed Output
  - **8-bit Fixed PWM Output**
  - **8-bit Dynamic PWM Output**

6.10. PCA : Interrupt Sources of a PCA



✓ **C0CON** (ACh) : PCA0 Counter Control Register

CF	CR	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

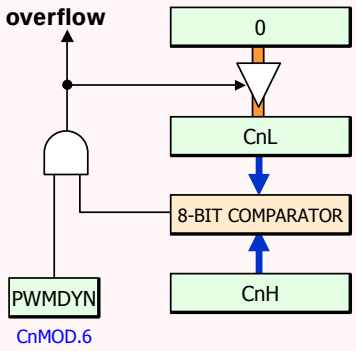
- CF : PCA counter overflow flag.
  Set by hardware when the counter rolls over.
  CF flags an interrupt if bit ECF in COMOD is set.
  CF may be set by either hardware or software but can only be cleared by software
- CR : PCA counter run control bit.
  Set by software to turn the PCA counter on.
  Must be cleared by software to turn the PCA counter off.
- CCF5 : PCA module 5 interrupt flag.
  Set by hardware when a match or capture occurs.
  Must be cleared by software.
- CCF4 : PCA module 4 interrupt flag.
- CCF3 : PCA module 3 interrupt flag.
- CCF2 : PCA module 2 interrupt flag.
- CCF1 : PCA module 1 interrupt flag.
- CCF0 : PCA module 0 interrupt flag.

✓ **C1CON** (CEh) : PCA1 Counter Control Register

CF	CR	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

6.10. PCA : PCAn Counter Control Registers

- To use a PCA Counter as an 8-bit Auto-reset Counter
  - ✓ Turn off the PCAn by clearing CR bit (CnCON.6)
  - ✓ Load target values into CnL and CnH.
  - ✓ Set PWMDYN bit (CnMOD.6) and set CF bit (CnCON.7)
  - ✓ Run PCAn by setting CR bit (CnCON.6)
  - ✓ An interrupt will occur when CnL reaches to CnH.
  - ✓ Insert the procedure for the PCAn counter overflow into the PCA interrupt service routine.



[Counter in Dynamic Mode (PWMDYN=1)]

✓ **C0MOD** (ADh) : PCA0 Counter Mode Register

CIDL	PWMDYN	-	CPS3	CPS2	CPS1	CPS0	ECF
R/W(0)	R/W(0)		R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- CIDL : Counter idle control.
  CIDL = 0 programs the PCA counter to continue functioning during idle mode.
  CIDL = 1 programs it to be stop during idle mode.
- PWMDYN : Dynamic PWM bit.
  If this bit is set, the dynamic PWM is generated.
  C0L is cleared when a match occurs between C0L and C0H.
  The match signal replaces the overflow signal for PWM.
- CPS[3:0] : PCA prescaler rate (F_{PCA}) selection. (Refer to below Table)
- ECF : Enable PCA counter overflow interrupt.
  ECF = 1 enables CF bit in C0CON to generate an interrupt.
  ECF = 0 disables that function.

[Count Rate (F_{PCA}) Selection]

CPS3	CPS2	CPS1	CPS0	Description
0	0	0	0	0 Internal clock, F_{OSC}
0	0	0	1	1 Internal clock, F_{OSC} / 2
0	0	1	0	2 Internal clock, F_{OSC} / 4
0	0	1	1	3 Internal clock, F_{OSC} / 8
0	1	0	0	4 Internal clock, F_{OSC} / 12
0	1	0	1	5 Internal clock, F_{OSC} / 16
0	1	1	0	6 Internal clock, F_{OSC} / 32
0	1	1	1	7 Internal clock, F_{OSC} / 64
1	0	0	0	8 Internal clock, F_{OSC} / 128
1	0	0	1	9 Internal clock, F_{OSC} / 256
1	0	1	0	10 External clock at ECIn pin (max rate = F_{OSC} / 2)
1	0	1	1	11 Timer 0 overflow

✓ **C1MOD** (CFh) : PCA1 Counter Mode Register

6.10. PCA : PCAn Module Control Registers

✓ **C0CAPM0** (A2h) : Mode Control Register of PCA0 MODULE0

IPWM0	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- IPWM0 : Inverted PWM output. If this bit is set, the PWM output is high when C0L ≥ C0CAPmL. The change of this bit will take effect from the next overflow / match time of PWM.
- ECOM0 : Enable comparator. ECOM0 = 1 enables the comparator function.
- CAPP0 : Capture positive. CAPP0 = 1 enables positive edge capture.
- CAPN0 : Capture negative. CAPN0 = 1 enables negative edge capture.
- MAT0 : Match. When MAT0 = 1, a match of the PCA counter with this module's comparator/capture register causes the CCF0 bit int C0CON to be set, flagging an interrupt.
- TOG0 : Toggle. When TOG0 = 1, a match of the PCA counter with this module's comparator/capture register causes the C0EX0 pin to toggle.
- PWM0 : Pulse width modulation mode. PWM0 = 1 enables the C0EX0 pin to be used as a pulse width modulated output.
- ECCF0 : Enable CCF interrupt. Enables compare/capture flag CCF0 in the C0CON register to generate an interrupt.

✓ **C0CAPM1** (A3h) : Mode Control Register of PCA0 MODULE1
✓ **C0CAPM2** (A4h) : Mode Control Register of PCA0 MODULE2
✓ **C0CAPM3** (A5h) : Mode Control Register of PCA0 MODULE3
✓ **C0CAPM4** (A6h) : Mode Control Register of PCA0 MODULE4
✓ **C0CAPM5** (A7h) : Mode Control Register of PCA0 MODULE5

✓ **C1CAPM0** (E2h) : Mode Control Register of PCA1 MODULE0
✓ **C1CAPM1** (E3h) : Mode Control Register of PCA1 MODULE1
✓ **C1CAPM2** (E4h) : Mode Control Register of PCA1 MODULE2
✓ **C1CAPM3** (E5h) : Mode Control Register of PCA1 MODULE3
✓ **C1CAPM4** (E6h) : Mode Control Register of PCA1 MODULE4
✓ **C1CAPM5** (E7h) : Mode Control Register of PCA1 MODULE5

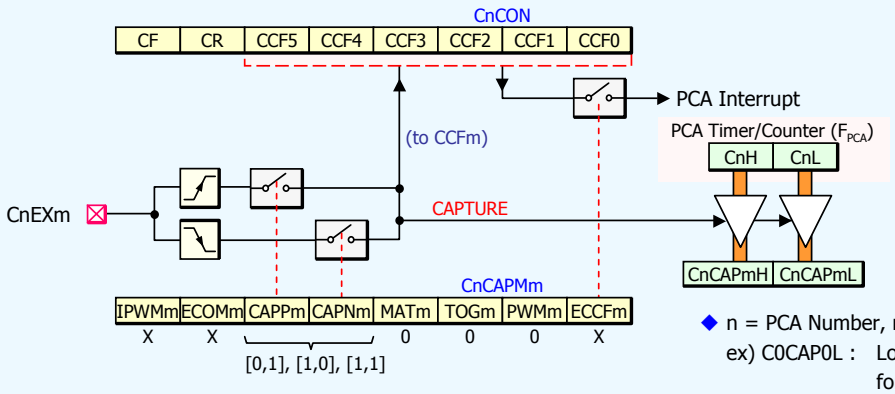
[PCA Module Modes (CnCAPMm Register)]

IPWMm	ECOMm	CAPPm	CAPNm	MATm	TOGm	PWMm	ECCFm	Module Function
X	0	0	0	0	0	0	0	No operation
X	X	1	0	0	0	0	X	1) 16-bit capture by a positive-edge trigger on CnEXm
X	X	0	1	0	0	0	X	1) 16-bit capture by a negative-edge trigger on CnEXm
X	X	1	1	0	0	0	X	1) 16-bit capture by any transition on CnEXm
X	1	0	0	1	0	0	X	2) 16-bit software timer
X	1	0	0	1	1	0	X	3) 16-bit high speed output
0	1	0	0	0	0	1	0	4) 5) 8-bit PWM normal output
1	1	0	0	0	0	1	0	4) 5) 8-bit PWM inverted output

* 1) ~ 5) : Refer to next slides.

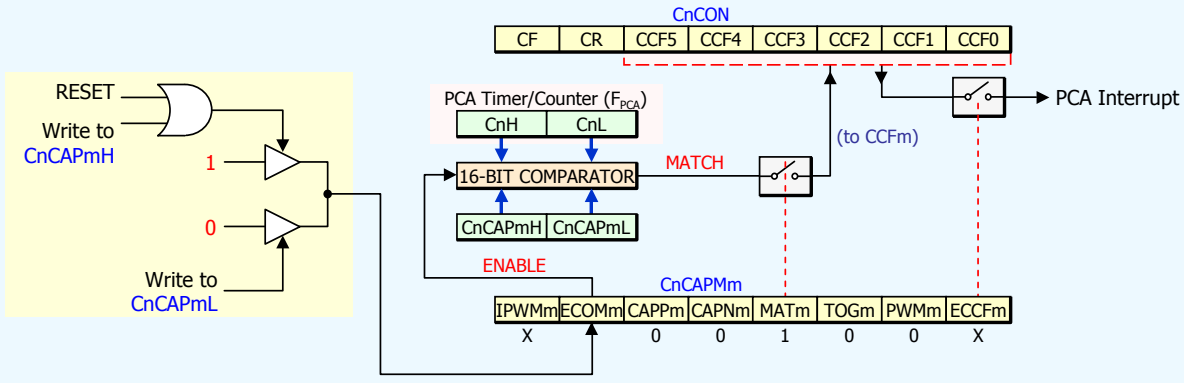
6.10. PCA : PCA Modes

1) Capture Mode



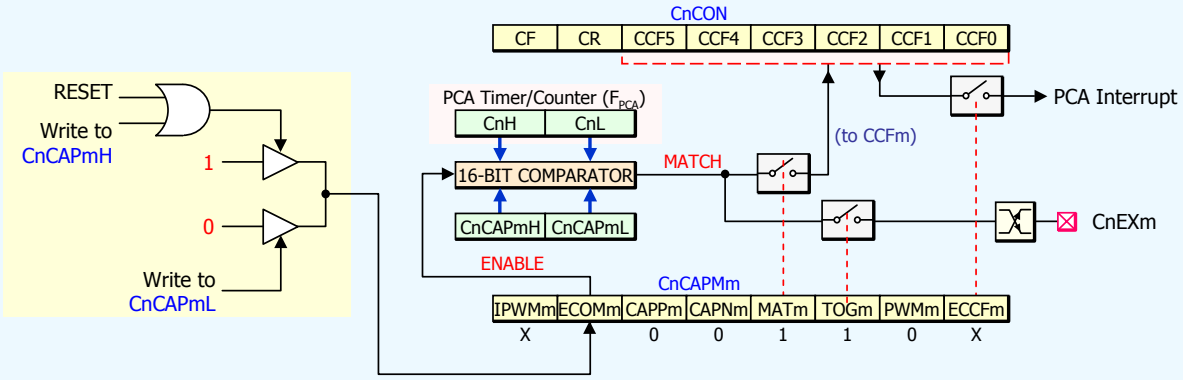
◆ n = PCA Number, m = Module Number
ex) C0CAP0L : Low Capture/Compare Register for Module0 of PCA0

2) Compare/Timer Mode



6.10. PCA : PCA Modes

3) PCA High Speed Output Mode

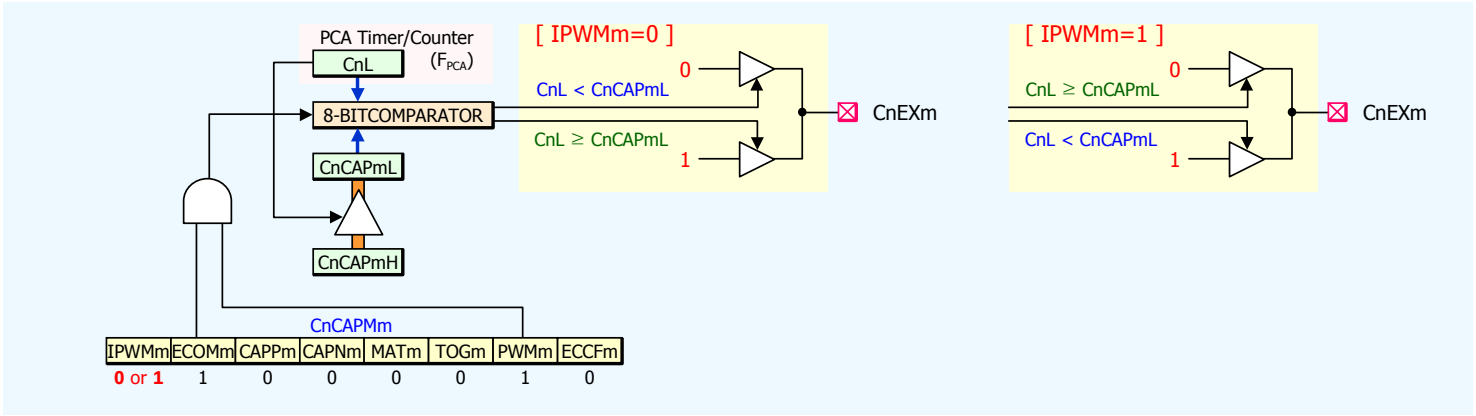


[Update of CnCAPmH & CnCAPmL]

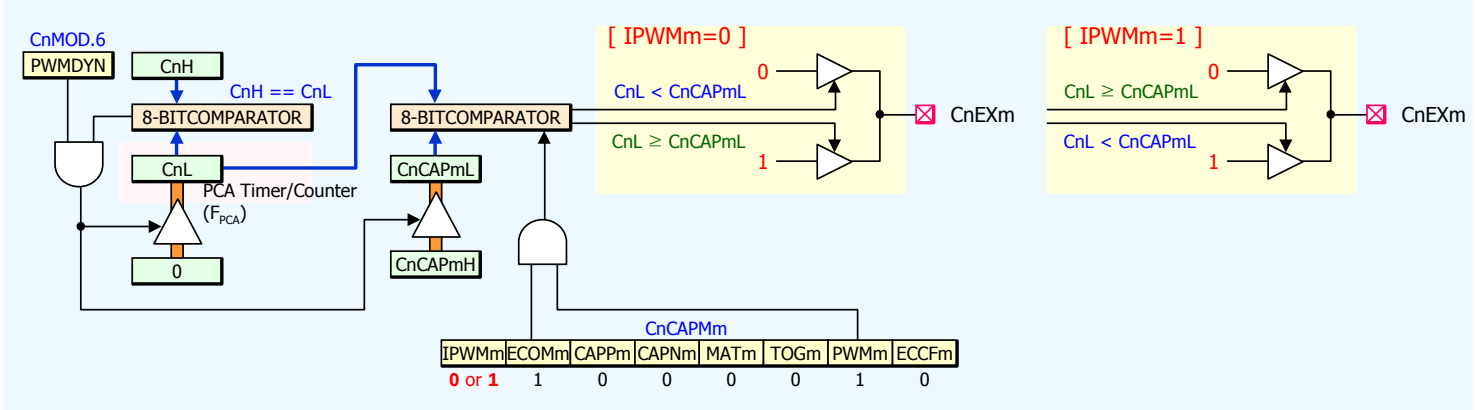
- During the interrupt routine, a new 16-bit compare value can be written to the compare register (CnCAPmH & CnCAPmL)
- Notice, however, that a write to CnCAPmL clears the ECOMm bit, which temporarily disables the comparator function while these registers are being updated so an invalid match does not occur.
- A write to CnCAPmH sets the ECOMm bit and re-enables the comparator.
- For this reason, user software should write to CnCAPmL first, then the CnCAPmH.

6.10. PCA : PCA Modes

4) PWM Mode (Fixed : PWMDYN = 0)

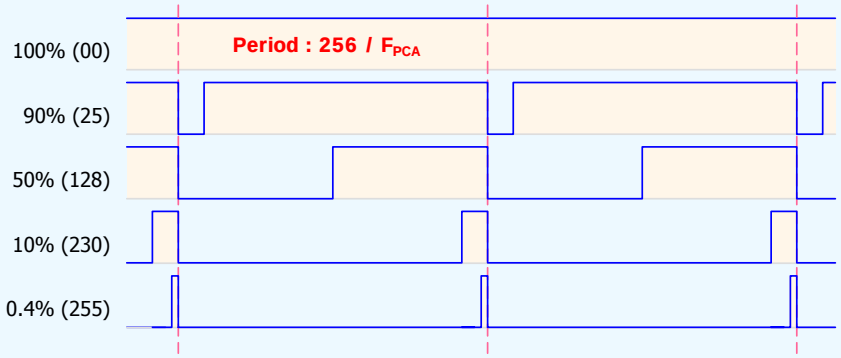


5) PWM Mode (Dynamic : PWMDYN = 1)

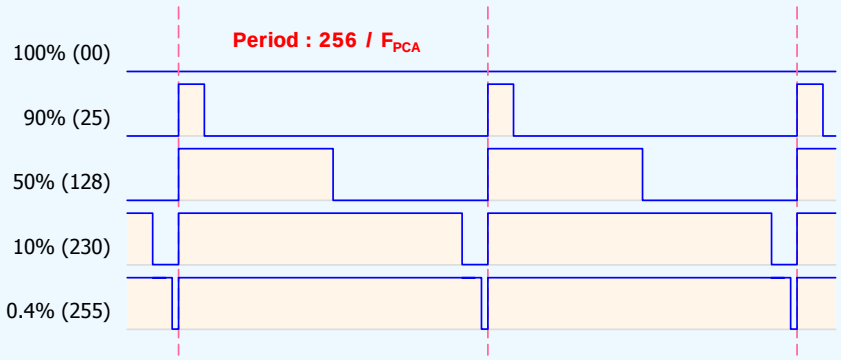


6.10. PCA : Examples of Fixed PWM Output

- Duty Cycle (CnCAPmH) with IPWMm = 0

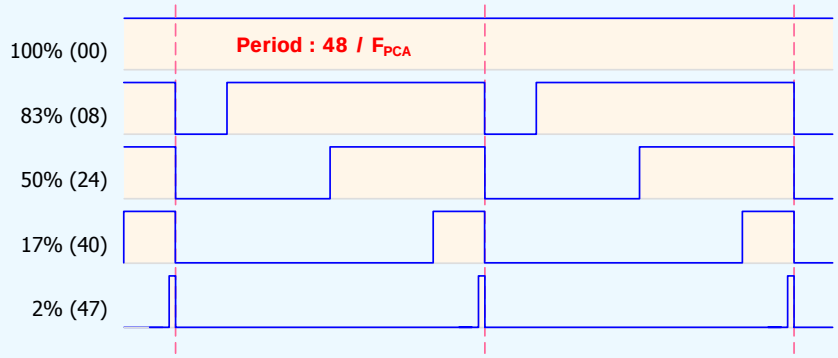


- Duty Cycle (CnCAPmH) with IPWMm = 1 (Inverted PWM Output)

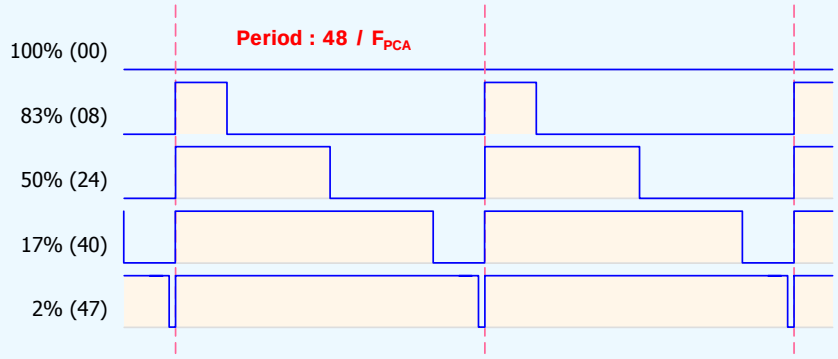


6.10. PCA : Examples of Dynamic PWM Output

- Duty Cycle (CnCAPmH) with IPWMm = 0, PWMDYN = 1, CnH = 47(0x2F).



- Duty Cycle (CnCAPmH) with IPWMm = 1, PWMDYN = 1, CnH = 47(0x2F).



6.11. ADC (Analog-to-Digital Converter)

- 8-channel 10-bit ADC (SAR Type)
- Max. 400ksps(samples per sec.) @ F_{ADC} = 20MHz & 3.3V

✓**ADCSEL** (EDh) : ADC Clock and MUX Selection Register

ADIV2	ADIV1	ADIV0	-	-	ADCS2	ADCS1	ADCS0
R/W(0)	R/W(0)	R/W(0)			R/W(0)	R/W(0)	R/W(0)

✓**ADCHEN** (ECh) : ADC Input Channel Enable Register

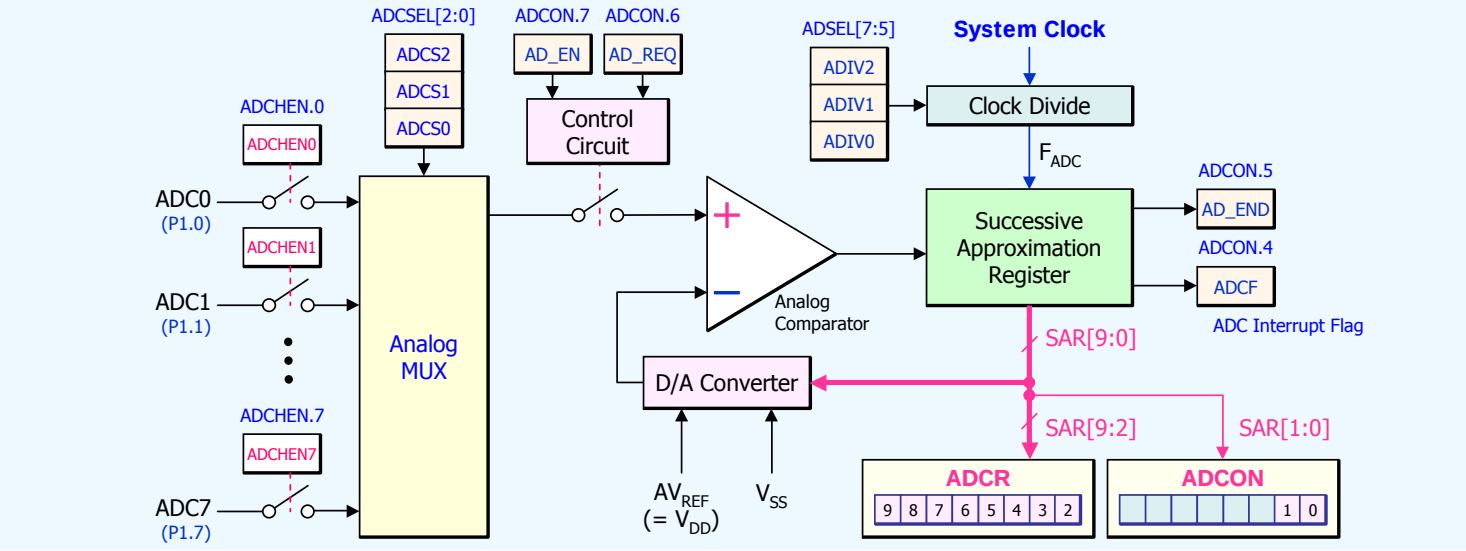
ADCHEN.7	ADCHEN.6	ADCHEN.5	ADCHEN.4	ADCHEN.3	ADCHEN.2	ADCHEN.1	ADCHEN.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

✓**ADCON** (EFh) : ADC Control & ADC Result Low Register

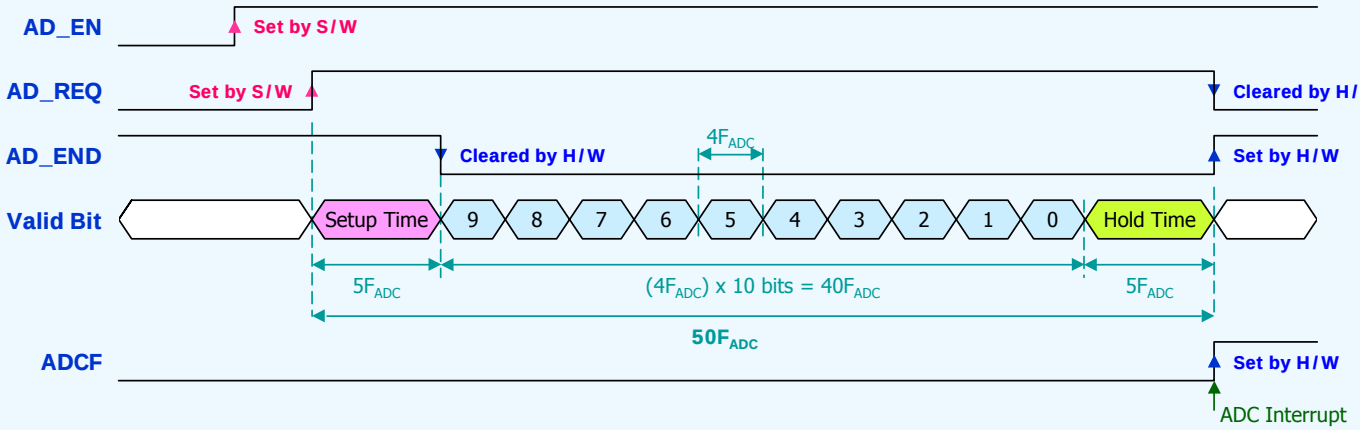
AD_EN	AD_REQ	AD_END	ADCF	-	-	SAR1	SAR0
R/W(0)	R/W(0)	R(1)	R/W(0)			R/W(0)	R/W(0)

✓ **ADCR** (EEh) : ADC Result High Register

SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)



6.11. ADC : Conversion Timing



- ✓ **AD_EN** : AD Conversion Enable Signal.
  Set or Cleared by S/W.
- ✓ **AD_REQ** : AD Conversion Request Bit.
  Set by S/W and Cleared by H/W.
  This bit must be set again for every sample conversion.
- ✓ **AD_END** : Set or Cleared by H/W.
  Cleared when the conversion is started.
  Set when the conversion is finished.
- ✓ **ADCF** : ADC Interrupt Flag.
  Set by H/W and Cleared by S/W.
  You should clear ADCF bit in the ADC interrupt routine.

[An Example of ADC Conversion Table]

OSC	Divide (ADCSEL[7:5])	F_{ADC}	T ($1/F_{ADC}$)	1 Sample Conversion Time
40MHz @3.3V	000 (OSC/2)	20MHz	50ns	2.5us
	001 (OSC/4)	10MHz	100ns	5.0us
	010 (OSC/8)	5MHz	200ns	10.0us
	011 (OSC/16)	2.5MHz	400ns	20.0us
	100 (OSC/32)	1.25MHz	800ns	40.0us

6.12. Interrupt : 16 Sources / 4-level Priority

- Interrupt Sources : Timer 0/1/2, UART0/1, PCA0/1, ADC, WDT, LVD, 6 External.
- 4-level Interrupt Priority

[Interrupt Vector Address]

HIGH

PRIORITY

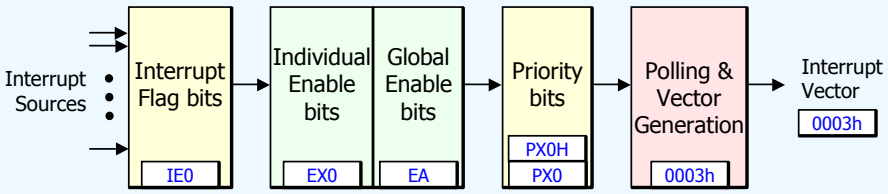
LOW

Interrupt Sources	Address	Priority Level	
LVD	0033h	Highest	NMI
$\overline{INT0}$	0003h	4 Levels	8052
TF0	000Bh	4 Levels	
$\overline{INT1}$	0013h	4 Levels	
TF1	001Bh	4 Levels	
RI+TI	0023h	4 Levels	
TF2	002Bh	4 Levels	
ADC	003Bh	4 Levels	
INT2	0043h	2 Levels	
$\overline{INT3}$	004Bh	2 Levels	
INT4	0053h	2 Levels	
$\overline{INT5}$	005Bh	2 Levels	
WDT	0063h	2 Levels	
RI1+TI1	006Bh	2 Levels	
PCA0	0073h	2 Levels	
PCA1	007Bh	2 Levels	

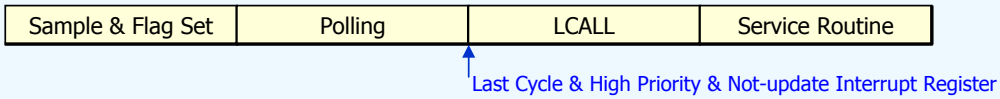
*** Interrupt SFR's (refer to Appendix B : SFR Description)**

✓ **TCON** (88h)	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
✓ **EXIF** (91h)	IE5	IE4	IE3	IE2	XT/RL	RGM0	RGSL	BGS
✓ **IE** (A8h)	EA	EADC	ET2	ES	ET1	EX1	ET0	EX0
✓ **EIE** (E8h)	EPCA1	EPCA0	ES1	EWDT	EX5	EX4	EX3	EX2
✓ **IP** (B8h)	-	PADC	PT2	PS	PT1	PX1	PT0	PX0
✓ **IPH** (B7h)	-	PADCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
✓ **EIP** (F8h)	PPCA1	PPCA0	PS1	PWDT	PX5	PX4	PX3	PX2
✓ **WDCON** (D8h)	-	POR	EPFI	PRI	WDIF	WTRF	EWT	RWT

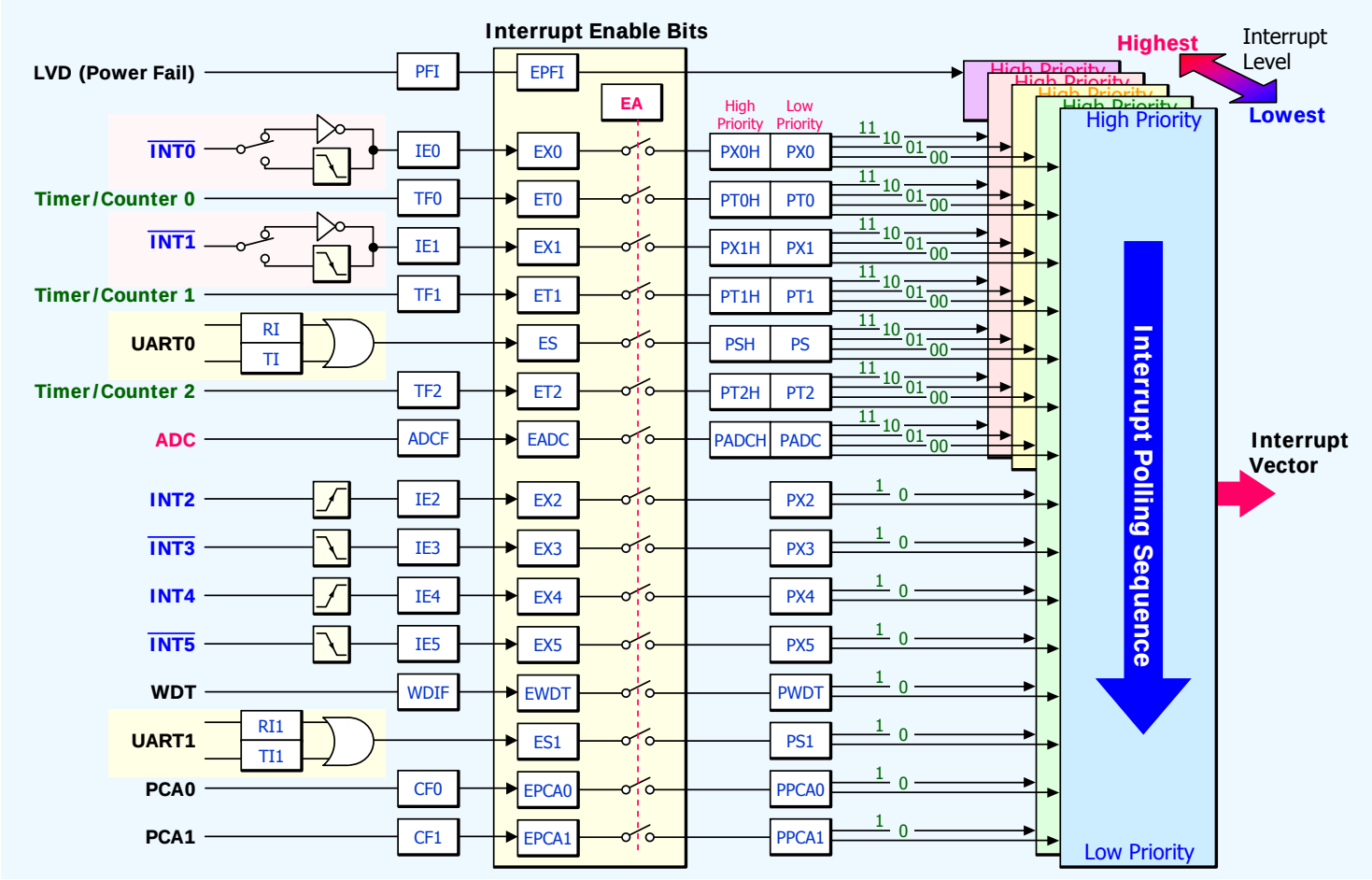
[Interrupt Vector Generation Flow]



[Response Sequence]



6.12. Interrupt Functional Description



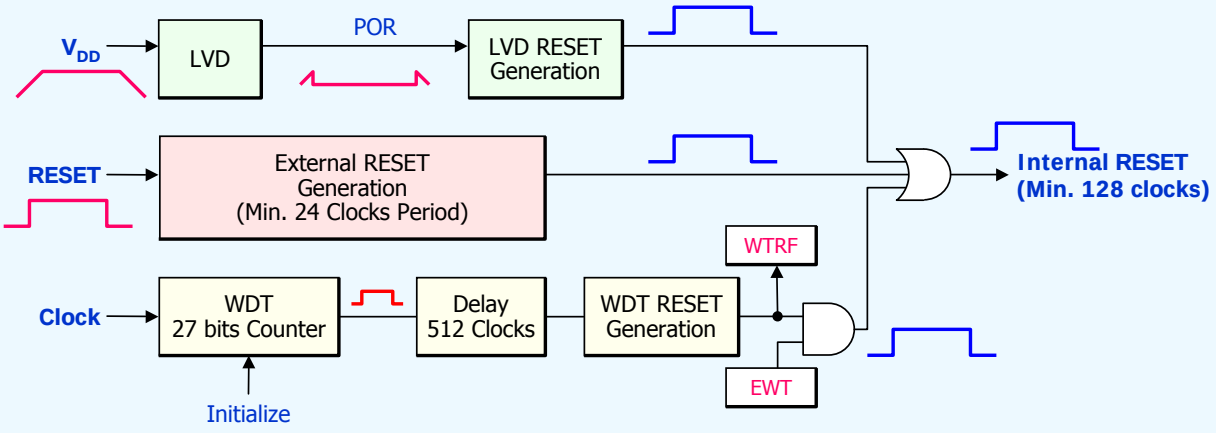
6.13. Reset Circuit : 3 Reset Sources

- LVD(POR) Reset
  - ✓ Power-on Reset when power is turned on.
  - ✓ Power-fail Reset when the supply voltage is below the threshold voltage (V_{RST}).
- External RESET Pin
  - ✓ RESET Pin must be held "H" for min. 24 clocks period.
- WDT Reset : Enable or disable by S/W
- Once triggered by any one of reset sources, the internal reset of MiDAS2.0 remains high for at least 128 clocks.

✓ **WDCON** (D8h) : Watchdog Timer & Power Status Register

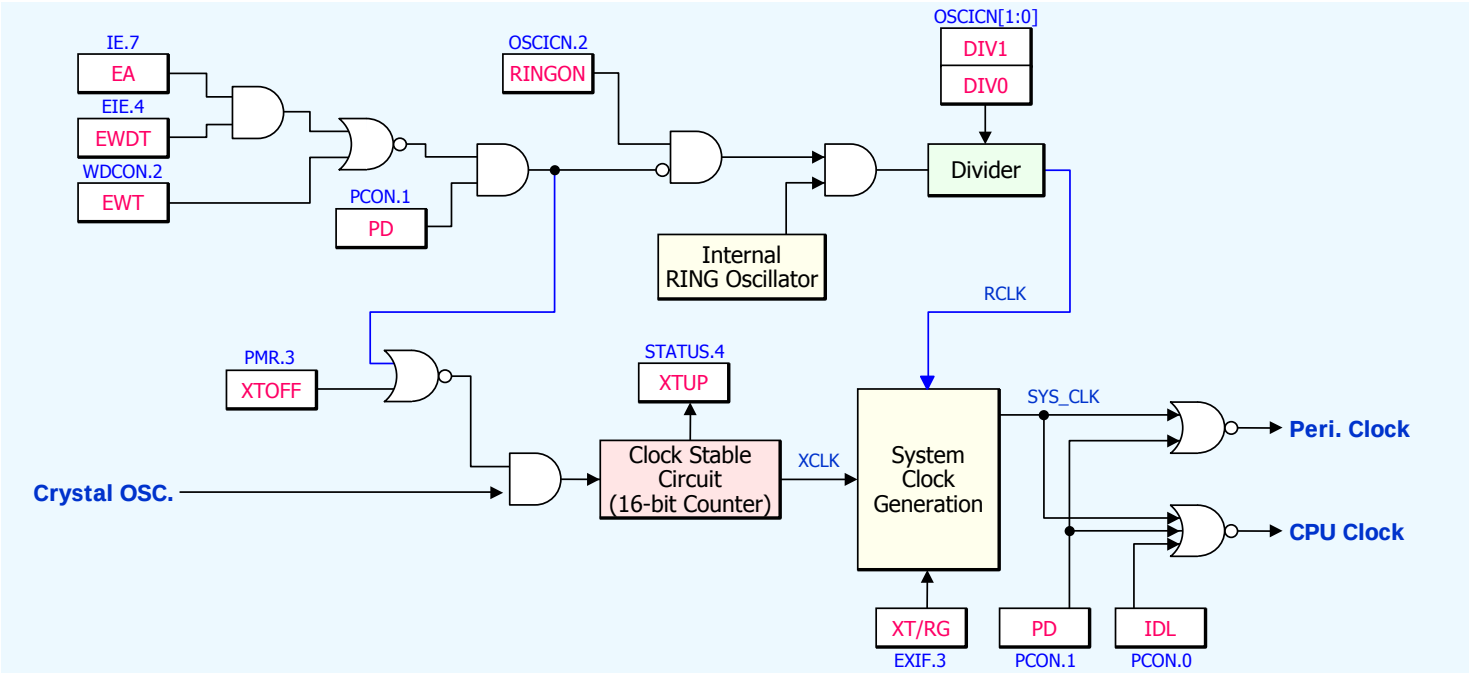
-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- WTRF : Watchdog Timer Reset Flag.
- EWT : Watchdog Timer Reset Enable.



6.14. Clock Circuit

- System Clock Sources
  - ✓ External Oscillator or Crystal
  - ✓ Internal Ring Oscillator
- Disable of External Clock (Crystal or External Oscillator)
  - ✓ If XTOFF is set.
  - ✓ When MCU is in stop mode and WDT is not active.
- Disable of the Internal RING Oscillator
  - ✓ If RINGON is cleared.
  - ✓ When MCU is in stop mode and WDT is not active.
- Wake-up from stop by WDT
  - ✓ WDT is active in stop mode if EWT is set or WDT interrupt is enabled.
  - ✓ In this case, the clock of WDT is alive during stop mode.



6.14. Clock Circuit : SFR

✓ **IE** (A8h) : Interrupt Enable Register

EA	EADC	ET2	ES	ET1	EX1	ET0	EX0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- EA : Global interrupt enable

✓ **EIE** (E8h) : Extended Interrupt Enable Register

-	-	-	EWDT	EX5	EX4	EX3	EX2
			R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- EWDT : Watchdog timer interrupt enable

✓ **PCON** (87h) : Extended Interrupt Enable Register

SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R/W(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- PD : Power-down (Stop) mode enable.
- IDL : IDL mode enable

✓ **EXIF** (91h) : External Interrupt Flag Bit Register

IE5	IE4	IE3	IE2	XT/RG	RGMD	RGSL	BGS
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(1)	R(0)	R/W(0)	R/W(1)

- XT/RG : System clock selection.
  0 = Internal RING oscillator is selected as system clock.
  1 = External clock is selected as system clock.

✓ **PMR** (C4h) : Power Management Control Register

-	-	-	-	XTOFF	ALEOFF	-	-
				R/W(0)	R/W(0)		

- XTOFF : 1 = External crystal oscillator disable.
  0 = External crystal will restart (Default).

✓ **STATUS** (C5h) : Crystal Status Register

-	-	-	XTUP	-	-		-
			R(1)				

- XTUP : Crystal oscillator warm-up status.
  It represents if the crystal clock is stable(1) or not(0).
  Cleared by H/W if XTOFF is set or if PD is set and WDT is not enabled.
  Set by H/W after crystal stabilization time.

✓ **OSCICN** (C6h) : Internal RING Oscillator Control Register

-	-	-	-	-	RINGON	DIV1	DIV0
					R/W(1)	R/W(0)	R/W(0)

- RINGON : Internal RING oscillator operates.
  0 = Internal RING oscillator disable.
  Don't clear RINGON bit when XTRG = 0.
- DIV1, DIV0 : RING oscillator divider.
  [0,0] = F_{RING} / 1 [0,1] = F_{RING} / 2
  [1,0] = F_{RING} / 4 [1,1] = F_{RING} / 8
  F_{RING} = 2.8 MHz (at room temp. 3.3V +/- 15%)

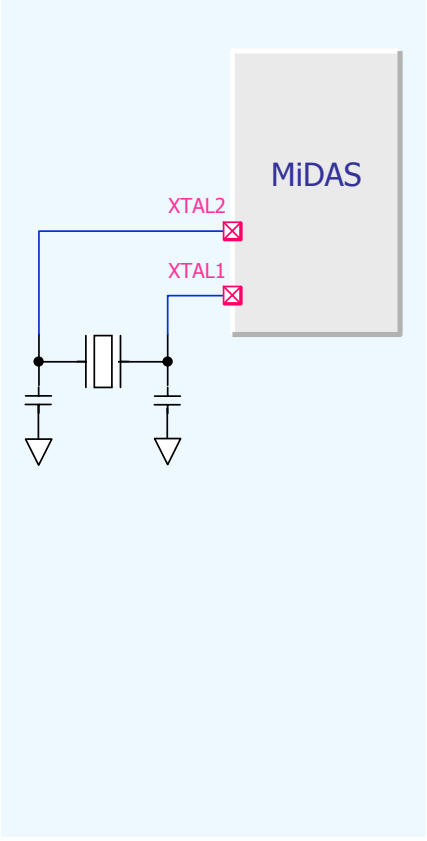
✓ **WDCON** (D8h) : Watchdog Timer & Power Status Register

-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

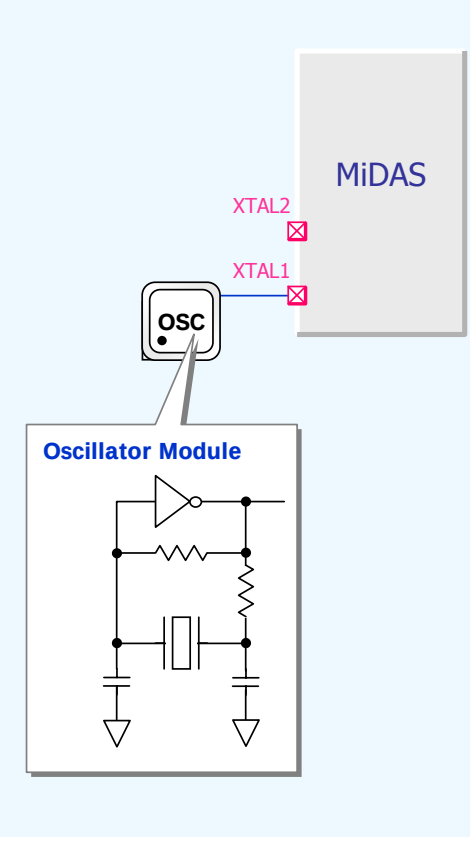
- EWT : Watchdog timer reset enable

6.14. Clock Circuit : Guideline for Configuration

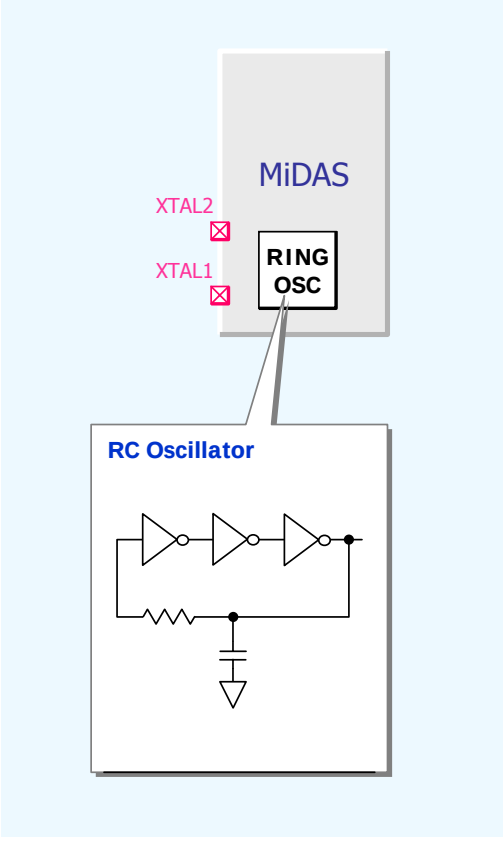
◆ **Crystal Oscillator**



◆ **Oscillator Module**



◆ **Internal Ring Oscillator**



6.15. Power Management : 3 Modes

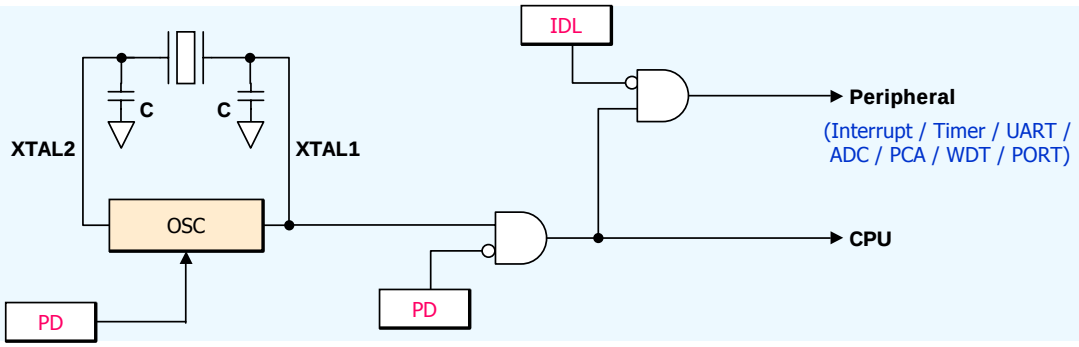
- Active Mode : The CPU and The Peripherals operate.
- Idle Mode : The CPU is gated off from the clock signal. Only the Peripherals operate.
  - ✓ Wake-up by activating any interrupt. The CPU resumes.
  - ✓ Wake-up by activating any reset. The CPU restarts..
- Stop Mode : The CPU and Peripherals are stopped.
  - ✓ Wake-up by activating external interrupt 0 or 1 (level detect) The CPU resumes.
  - ✓ Wake-up by activating all kinds of resets. CPU restarts.
  - ✓ Wake-up by activating WDT interrupt or reset. If WDT remains enabled, either the crystal oscillator or the ring oscillator will operate during the stop mode.
  - ✓ To prevent malfunction of I/O ports during wake-up, it is recommended to execute the NOP instruction twice after the PD bit of PCON is set to 1.

✓ **PCON** (87h) : Power Control Register

SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R/W(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

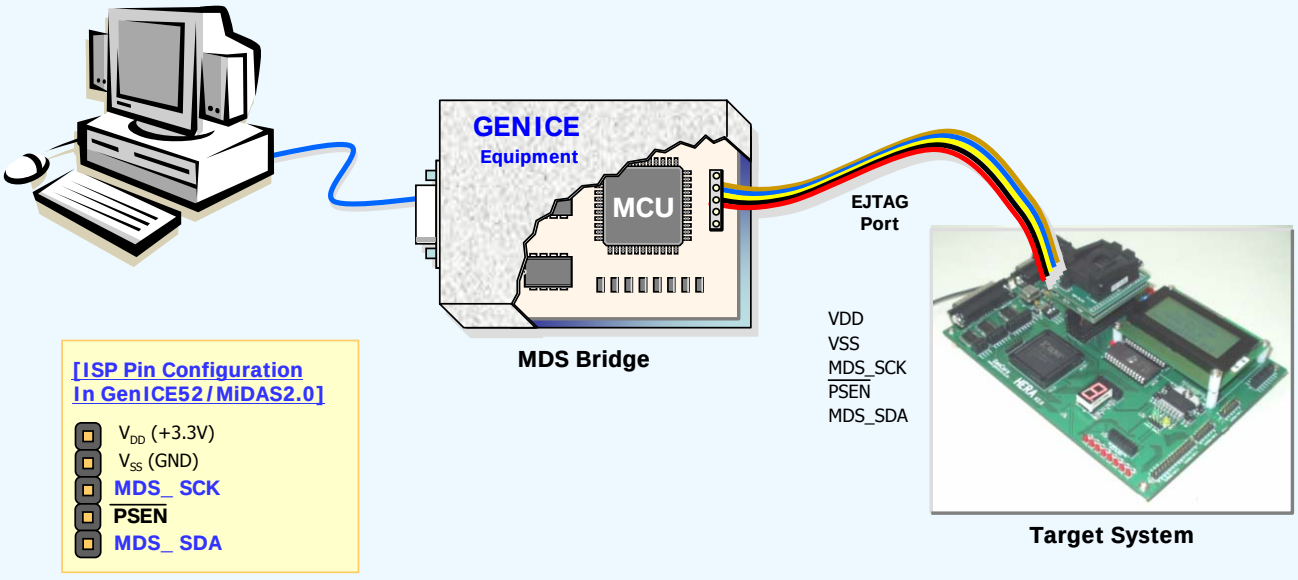
- PD : Stop Mode (Power-down) Enable.
- IDL : IDLE Mode Enable.

- Wake-up from stop mode
  - ✓ The crystal oscillator was used before invoking stop mode and WDT is disabled : External interrupt signals must be held '0' for at least (2^{16} + 8) clock cycles. The internal MCU clocks will be activated after the 16-bit crystal stabilization counter overflows.
  - ✓ An User set RGSL(EXIF.1) bit. It enables the MCU immediately to wake up using the internal ring oscillator. After the stabilization counter overflows, XTAL clock will be available again.
  - ✓ The ring oscillator is available without stabilization. In this case, external interrupt signals should be held '0' is for at least 8 clock cycles, implemented by executing the NOP instruction twice, to enter the interrupt service routine.



6.16. ISP (In-System Programming)

- Code memory (62KBytes) can be programmed using EJTAG in target system.
- EEPROM (2KBytes) can be programmed using EJTAG in target system.
- EJTAG Port
  - ✓ VDD, VSS, MDS_SCK, MDS_SDA, $\overline{\text{PSEN}}$



6.16. ISP : Command Set

Command	Function
Blank	◆ Check the blank status of the device currently connected.
Erase Chip	◆ Erases the device's memory.
	◆ Performs an erase chip, the device's memory, both code and data. • Code : Flash • User data : EEPROM • Information data : Lock bits, RING option, PGM/ERS time (ISP & Parallel)
	◆ The device will be blank and in a programmable state.
Read Code/EEPROM	◆ Reads in the device's memory.
	◆ The results from the read are loaded into the CORERIVER ISP software's buffer and displayed on the screen.
Write Chip/EEPROM	◆ Writes all memory locations in the CORERIVER ISP software's buffer out to the device's memory.
Verify Chip	◆ Compares the CORERIVER ISP software buffer with the device's internal memory.
	◆ If the buffers are found to be exact replicas of the device's memory, a success result is returned.
	◆ If there are any differences, a failure result is returned along with the total number of mismatched bytes.

6.17. IAP (In-Application Programming)

- IAP function is provided for the applications which need to save operation data/status in nonvolatile memory (on-chip EEPROM) or to update application code (on-chip FLASH) by itself.
  - ✓ Code memory(62KB) can be programmed or erased during the operation of MCU.
  - ✓ EEPROM(2KB) can be programmed or erased during the operation of MCU.
- IAP erase byte routine (code/EEPROM) uses on-chip XRAM area(0600h~06FFh).
  - ✓ If user software uses XRAM area(0600h~06FFh), the contents must be backup.
- Program/Erase time
  - ✓ Program : 50us except for IAP code execution time.
  - ✓ Erase : 10ms except for IAP code execution time.
- Program/Erase unit
  - ✓ Program : 1 byte
  - ✓ Erase : 1 byte or 1 sector (256 bytes)
- IAP SFR
  - ✓ FAEN : IAP routine Access Enable (default value = 0x00)

✓ **FAEN** (F7h) : IAP Routine Access Enable Register

-	-	-	-	-	-	-	FALSH_AEN
							R/W(0)

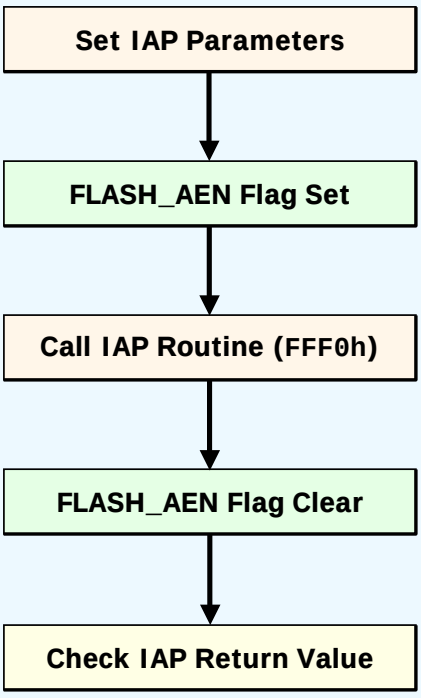
- FLASH_AEN : IAP Routine Access Enable

6.17. IAP : Function Set

- IAP call address
  - ✓ FFF0h
- IAP return value
  - ✓ Success : [ACC] 8Xh
  - ✓ Program Fail : [ACC] FCh
  - ✓ Address fail : [ACC] FDh
  - ✓ Lock fail : [ACC] FEh
  - ✓ Command fail : [ACC] FFh
- Before calling IAP function, FLASH_AEN flag in FAEN SFR must be set.
- After executing IAP function, the value of PSW SFR can be changed.
- During "Byte Erase" IAP functions, the part of External RAM (0600h~06FFh) is used.
  - ✓ If user software uses External RAM area(0600h~06FFh), the contents must be backup.
- Any interrupt service routine will not be executed in time since the CPU is suspended for tens of milliseconds during executing an IAP function (Program/Erase).

Call Address	Command	Function	B	ACC	DPTR	Used XRAM Area	Return Value (ACC)
FFF0h	Program	Program Code Byte	3h	Programmed code	Flash address	No	83h/FCh/FDh/FEh/FFh
		Program EEPROM Byte	6h	Programmed data	EEP Address	No	86h/FCh/FDh/FEh/FFh
	Erase	Erase Code Sector	1h	Don't care	Sector Address	No	81h/FDh/FEh/F로
		Erase Code Byte	2h	Don't care	Flash Address	0600h ~ 06ffh	82h/FDh/FEh/FFh
		Erase EEPROM Sector	4h	Don't care	Sector Address	No	84h/FDh/FEh/FFh
		Erase EEPROM Byte	5h	Don't care	EEP Address	0600h ~ 06FFh	85h/FDh/FEh/FFh

6.17. IAP : Coding Flow

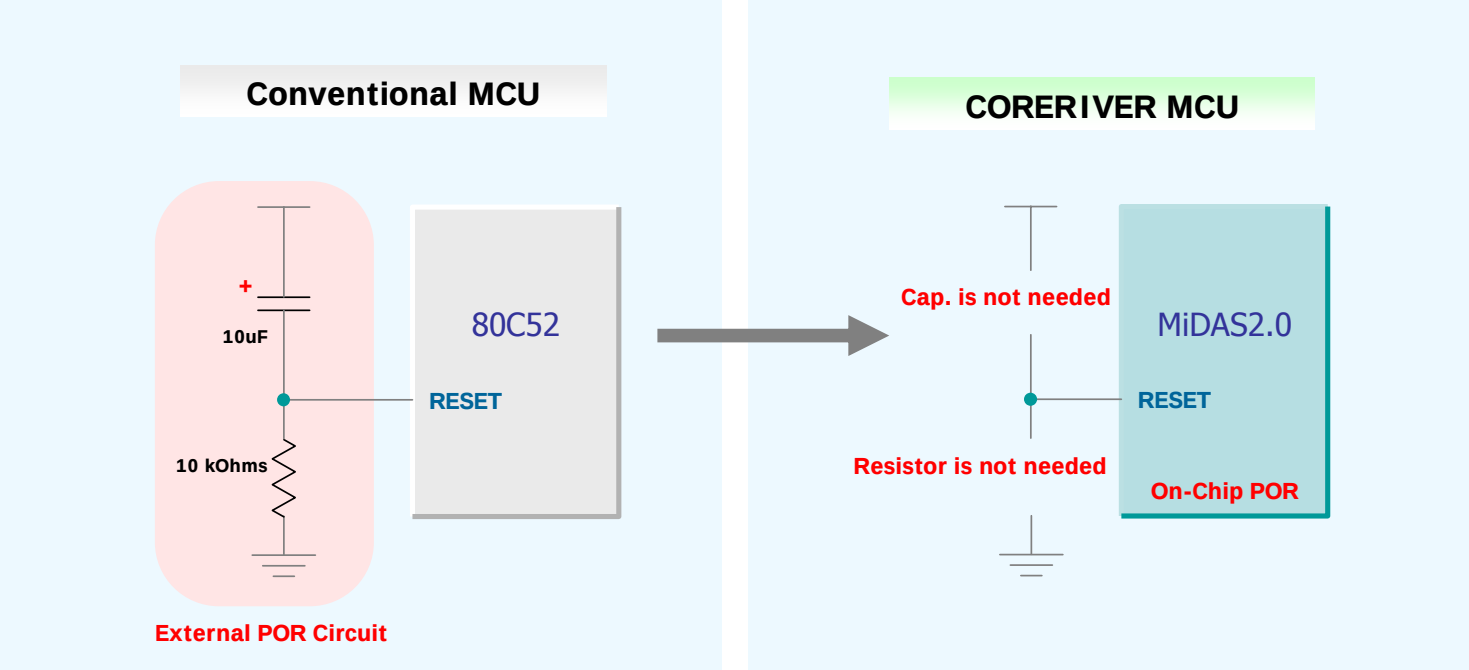


[Example Code : Program FLASH]

```
MOV B, #03h              ;IAP function setting
MOV A, #55h              ;Programmed data
MOV DPTR, #08000h        ;Programmed address

MOV FAEN, #01h           ;IAP routine access enable

CALL 0FFF0h              ;Call IAP routine

MOV FAEN, #00h           ;IAP routine access disable

CJNE A, #83h, IAP_FAIL   ;Check return message
```

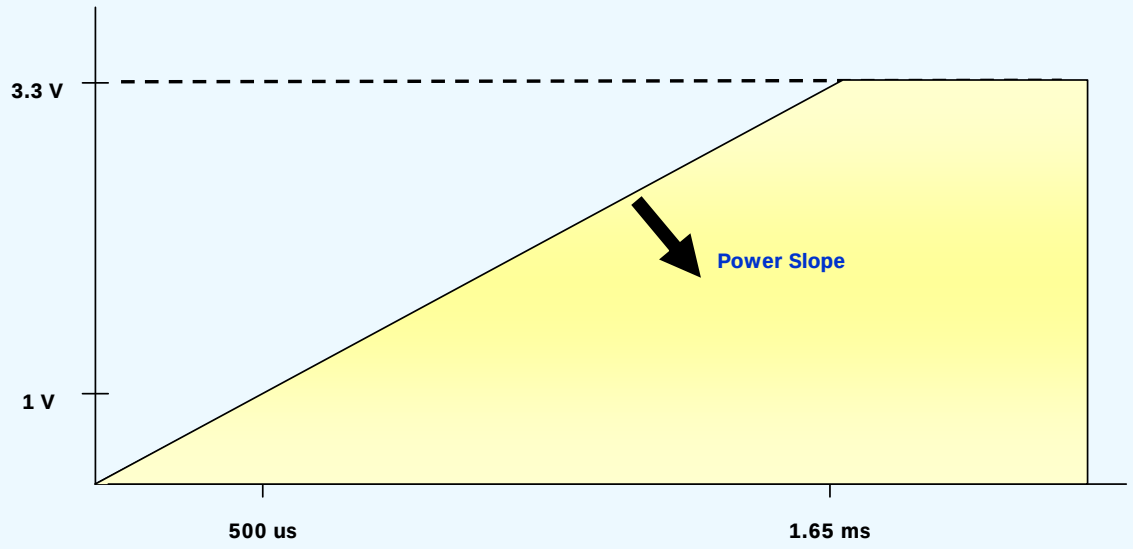
7. Strong Points

- MiDAS 2.0 can reduce EMI by removing the needless swing of ALE signal.
  - ✓ You can enable/disable ALE signal by changing the value of ALEOFF bit (SFR PMR.2).
- User can reduce system cost by removing needless decoupling capacitors while maintaining the EMI.
- On-chip POR (Power On Reset) can reduce system cost by removing needless capacitor or even resistor.



8. Recommended Power Slope

- The supply voltage slope must be in the range from 0.0V/us to 1.0V/500us. (3.3V/1.65ms)
  (That is, the supply voltage should be increasing monotonically until it reaches to the normal range.)



9. Absolute Maximum Ratings

Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit
V_{DD}	DC supply voltage	-0.3 to 3.8		V
V_{IN}	DC input voltage	3.3V I/O	-0.3 to V_{DD}+0.3	V
		5V-tolerant	-0.3 to 5.5	
I_{IN}	DC input current	±10		mA
T_{STG}	Storage temperature	-40 to 125		ºC

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	3.0 to 3.6	V
T_A	Industrial temperature range	-20 to 85	ºC

Notes

- ✓ All electrical characteristics are applied to digital cell blocks without any analog core.

10. DC Characteristics (5V Tolerant I/O)

V_{DD} = 3.3 ± 0.3V, VEXT = 5V ± 0.25V, T_A = -20 to 85 ºC
(In case of P0, P1, P2, P3, RESET, PSEN, ALE, EA, MDS_SCK, MDS_SDA)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage[Note1]					V
	LVCMOS interface[Note1]		2.0			
V_{IL}	Low level input voltage					V
	LVCMOS interface				0.8	
VT	Switching threshold	LVCMOS		1.4		V
VT+	Schmitt trigger, positive-going threshold	LVCMOS			2.0	V
VT-	Schmitt trigger, negative-going threshold	LVCMOS	0.8			V
I_{IH}	High level input current					uA
	Input buffer **(except RESET)**	$V_{IN} = V_{DD}$	-10		10	
	Input buffer with pull-down **(RESET)**		10	30	60	
I_{IL}	Low level input current					uA
	Input buffer **(RESET, ALE, P0)**	$V_{IN} = V_{SS}$	-10		10	
	Input buffer with pull-up **(Remainder)**		-60	-30	-10	
V_{OH}	High level output voltage					V
	Output buffer	**I_{OH} = -6mA**	2.4			
V_{OL}	Low level output voltage					V
	Output buffer	**I_{OL} = 6mA**			0.4	
I_{OZ}	Tri-state output leakage current	$V_{OUT} = V_{SS}$ or V_{DD}	-10		10	uA
I_{OS}	Output short circuit current	V_{DD} = 3.6V, $V_O = V_{DD}$			55	mA
		V_{DD} = 3.6V, $V_O = V_{SS}$	-55			
I_{DD}	Quiescent supply current	$V_{IN} = V_{SS}$ or V_{DD}			100[Note2]	uA
C_{IN}	Input capacitance[Note3]	input & bidirection buf.			4	pF
C_{OUT}	Output capacitance[Note3]	Any output buffer			4	pF

Note 1 : All 5V tolerant inputs have less than 0.2V hysteresis.
Note 2 : This value may vary according to the customer application.
Note 3 : This value exclude package parasitic capacitances.

10. DC Characteristics (Normal I/O)

V_{DD} = 3.3 ± 0.3V, T_A = -20 to 85 °C

(In case of XTAL2, P4, P5, P6, P7, P8, P9)

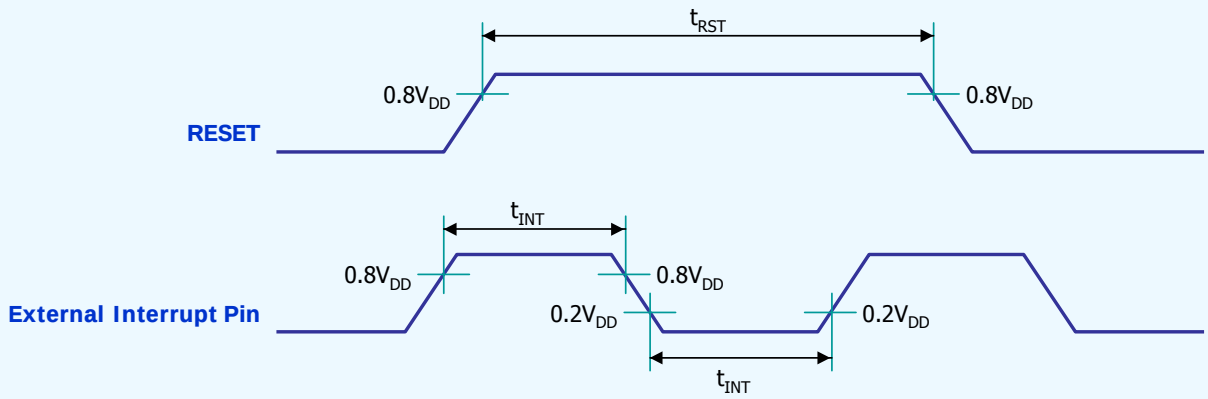
Symbol	Parameter	Rating	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage					V
	LVCMOS interface		2.0			
V_{IL}	Low level input voltage					V
	LVCMOS interface				0.8	
VT	Switching threshold	LVCMOS		1.4		V
VT+	Schmitt trigger, positive-going threshold	LVCMOS			2.0	V
VT-	Schmitt trigger, negative-going threshold	LVCMOS	0.8			V
I_{IH}	High level input current					uA
	Input buffer	$V_{IN} = V_{DD}$	-10		10	
I_{IL}	Low level input current					uA
	Input buffer with pull-up	$V_{IN} = V_{SS}$	-60	-30	-10	
V_{OH}	High level output voltage					V
	Output buffer **(XTAL2)**	**I_{OH} = -5mA**	2.4			
	Output buffer **(P4)**	**I_{OH} = -6mA**				
	Output buffer **(P5, P6, P7, P8, P9)**	**I_{OH} = -20mA**				
V_{OL}	Low level output voltage					V
	Output buffer **(XTAL2)**	**I_{OL} = 5mA**			0.4	
	Output buffer **(P4)**	**I_{OL} = 6mA**				
	Output buffer **(P5, P6, P7, P8, P9)**	**I_{OL} = 20mA**				
I_{OZ}	Tri-state output leakage current	$V_{OUT} = V_{SS}$ or V_{DD}	-10		10	uA
I_{OS}	Output short circuit current	V_{DD} = 3.6V, $V_O = V_{DD}$			55	mA
		V_{DD} = 3.6V, $V_O = V_{SS}$	-55			
I_{DD}	Quiescent supply current	$V_{IN} = V_{SS}$ or V_{DD}			100[Note2]	uA
C_{IN}	Input capacitance[Note3]	input & bidirection buf.			4	pF
C_{OUT}	Output capacitance[Note3]	Any output buffer			4	pF

Note 1 : All 5V tolerant inputs have less than 0.2V hysteresis.
Note 2 : This value may vary according to the customer application.
Note 3 : This value exclude package parasitic capacitances.

11. AC Characteristics

*** T_A = -20 ºC ~ +85 ºC unless otherwise specified.**

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Operating Frequency	F_{OSC}	XTAL1, XTAL2	V_{DD} = 3.3V ± 10%	-	-	40	MHz
RESET Input Width	t_{RST}	RESET	V_{DD} = 3.3V ± 10%	24	-	-	F_{OSC}
External Interrupt Input Width	t_{INT}	External Interrupt	V_{DD} = 3.3V ± 10%	4	-	-	F_{OSC}



12. ADC Characteristics

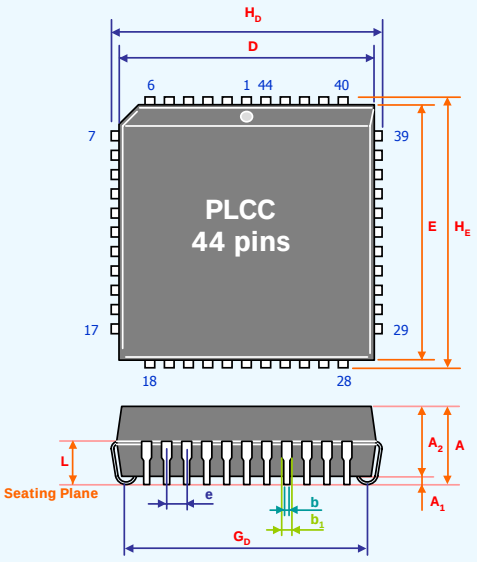
DC Electrical Characteristics

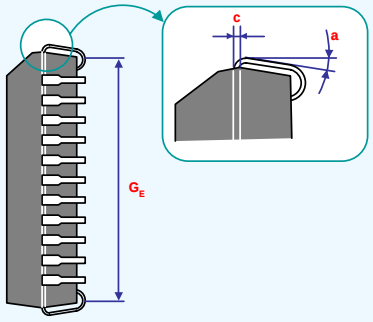
Characteristics	Symbol	Min.	Typ.	Max.	Unit	Conditions
Resolution	-	-	10		Bits	
Differential Linearity Error	DLE	-	±0.5	±1.0	LSB	F_{OSC} = 40MHz (F_{ADC} = 20MHz)
Integral Linearity Error	ILE	-	±1.0	±2.0	LSB	
Offset Voltage Error (top)	EOT	-	±2.0	±4.0	LSB	
Offset Voltage Error (bottom)	EOB	-	±2.0	±4.0	LSB	
Channel to Channel Mismatch	-	-		±1/4	LSB	8-channel
Analog Input Voltage	AIN	0		VDD	V	

AC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Conditions
Conversion Rate	f_{AD}	-	-	400	KSPS	F_{OSC} = 40MHz (F_{ADC} = 20MHz)
Conversion Time	t_{AD}	2.5	-	-	us	
Dynamic Supply Current	Is	-	1	1.5	mA	Is=I(VDDA)+I(VDDD)+I(REFP) Power Load Cap : 10uF//0.1uF Output Load Cap. = 1pF
	Isd	-	0.1	0.5	uA	At Power down
Power Dissipation	Pd	-	3.3	5.4	mW	During A/D operation
	Pdd	-	0.33	1.8	uW	At Power Down

13. Package Dimensions : 44-PLCC



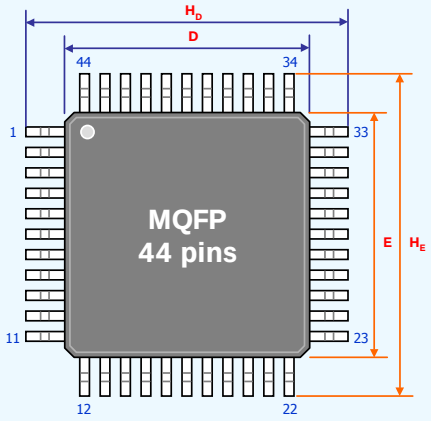


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.165	-	0.180	4.191	-	4.572
A_1	0.020	-	-	0.508	-	-
A_2	0.145	0.150	0.155	3.683	3.810	3.937
b_1	0.026	0.028	0.032	0.660	0.711	0.813
b	0.013	0.017	0.021	0.330	0.432	0.533
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.650	0.658	16.460	16.510	16.710
E	0.648	0.650	0.658	16.460	16.510	16.710
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.986	15.494	16.002
G_E	0.590	0.610	0.630	14.986	15.494	16.002
H_D	0.680	0.690	0.700	17.272	17.526	17.780
H_E	0.680	0.690	0.700	17.272	17.526	17.780
L	0.090	0.100	0.120	2.296	2.540	3.048

Notes:

1. Dimension D * E do not include interlead flash.
2. Dimension b_1 dose not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

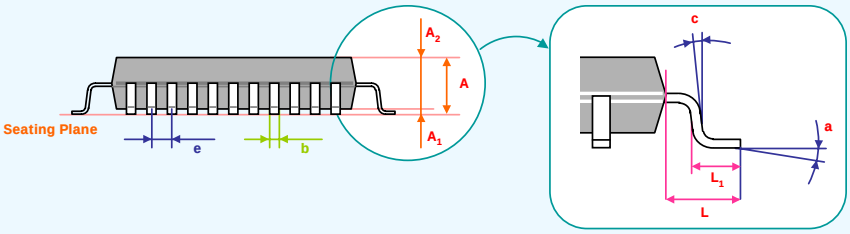
13. Package Dimensions : 44-MQFP



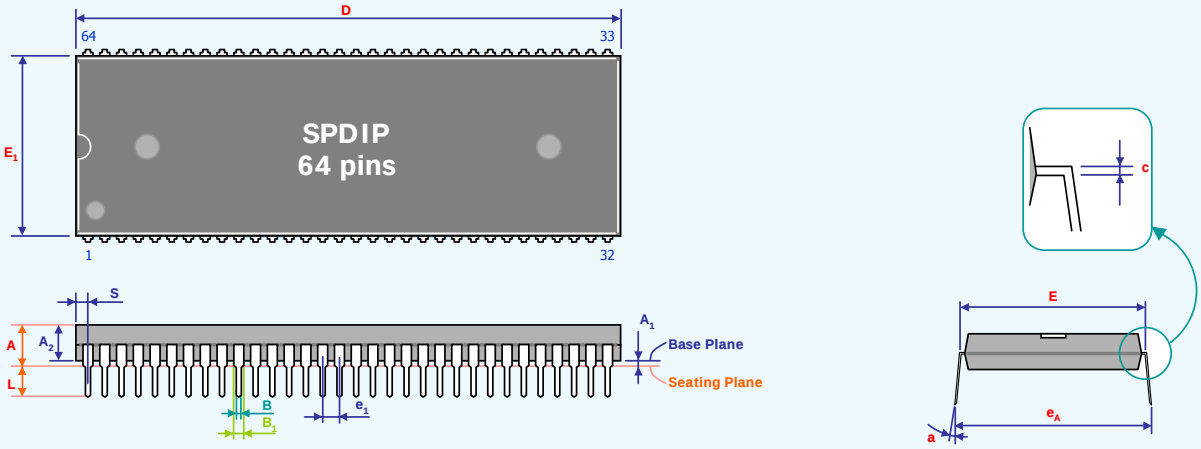
[44-MQFP]

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.091	-	-	2.30
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.077	0.081	0.085	1.95	2.05	2.15
b	0.012	0.015	0.018	0.30	0.37	0.45
D	0.394 BSC			10.00 BSC		
E	0.394 BSC			10.00 BSC		
e	0.031 BSC			0.80 BSC		
H_D	0.520 BSC			13.20 BSC		
H_E	0.520 BSC			13.20 BSC		
L	-	0.063	-	-	1.60	-
L_1	0.024	0.031	0.039	0.60	0.80	1.00
a	0°	-	8°	0°	-	8°
c	0°	-	-	0°	-	-

Notes:
1. Dimension D * E do not include interlead flash.
2. Controlling dimension: Inches
3. General appearance spec. should be based on final visual inspection spec.



13. Package Dimensions : 64-PDIP



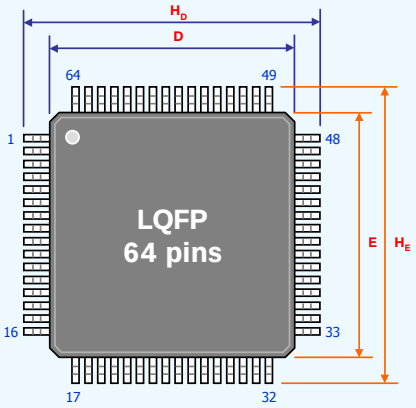
[64-SPDIP]

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.200	-	-	5.080
A_1	0.020	-	-	0.508	-	-
A_2	0.135	0.150	0.165	3.420	3.810	4.190
B	0.015	0.018	0.022	0.381	0.457	0.559
B_1	0.035	0.040	0.045	0.889	1.016	1.143
c	0.009	0.010	0.012	0.229	0.254	0.305
D	2.260	2.273	2.280	57.400	57.730	57.910
E	0.750	-	0.775	19.050	-	19.690
E_1	0.660	0.670	0.680	16.760	17.020	17.270
e_1	0.070 BSC			1.780 BSC		
L	0.120	-	0.135	3.048	-	3.430
a	0°	-	15°	0°	-	15°
e_A	0.630	0.650	0.670	16.000	16.510	17.010
S	0.047	0.052	0.057	1.19	1.32	1.45

Notes:

1. Dimension D Max. & S include mold flash or tie bar Burns.
2. Dimension E_1 dose not include interlead flash.
3. Dimension D & E_1 include mold mismatch and are determined at the mold parting line.
4. Dimension B_1 does not include dambar protrusion/intrusion.
5. General appearance spec. should be based on final visual inspection spec.

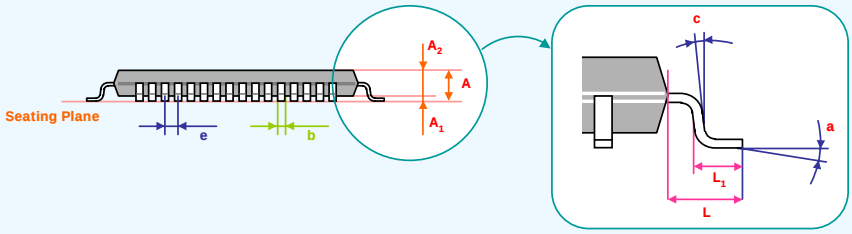
13. Package Dimensions : 64-LQFP



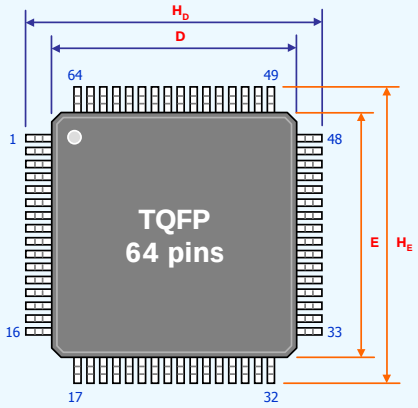
[64-LQFP]

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.60
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
D	0.394 BSC			10.00 BSC		
E	0.394 BSC			10.00 BSC		
e	0.020 BSC			0.50 BSC		
H_D	0.472 BSC			12.00 BSC		
H_E	0.472 BSC			12.00 BSC		
L	-	0.039	-	-	1.00	-
L_1	0.018	0.024	0.029	0.45	0.60	0.75
a	0°	-	7°	0°	-	7°
c	0°	-	-	0°	-	-

Notes:
1. Dimension D * E do not include interlead flash.
2. Controlling dimension: Inches
3. General appearance spec. should be based on final visual inspection spec.



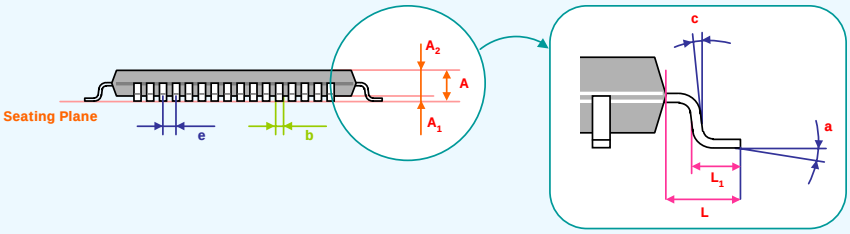
13. Package Dimensions : 64-TQFP



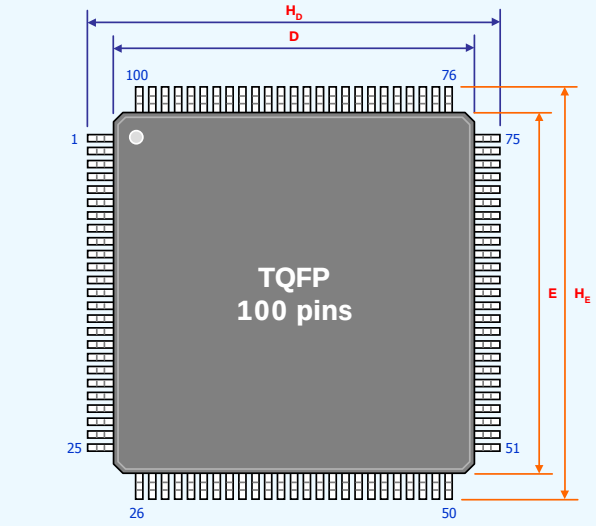
[64-TQFP]

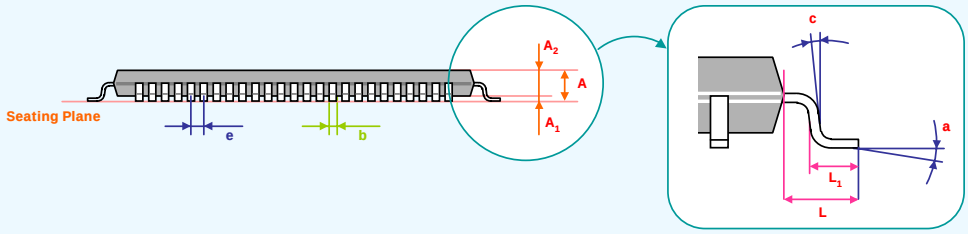
Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
D	0.394 BSC			10.00 BSC		
E	0.394 BSC			10.00 BSC		
e	0.020 BSC			0.50 BSC		
H_D	0.472 BSC			12.00 BSC		
H_E	0.472 BSC			12.00 BSC		
L	-	0.039	-	-	1.00	-
L_1	0.018	0.024	0.029	0.45	0.60	0.75
a	0°	-	7°	0°	-	7°
c	0°	-	-	0°	-	-

Notes:
1. Dimension D * E do not include interlead flash.
2. Controlling dimension: Inches
3. General appearance spec. should be based on final visual inspection spec.



13. Package Dimensions : 100-TQFP





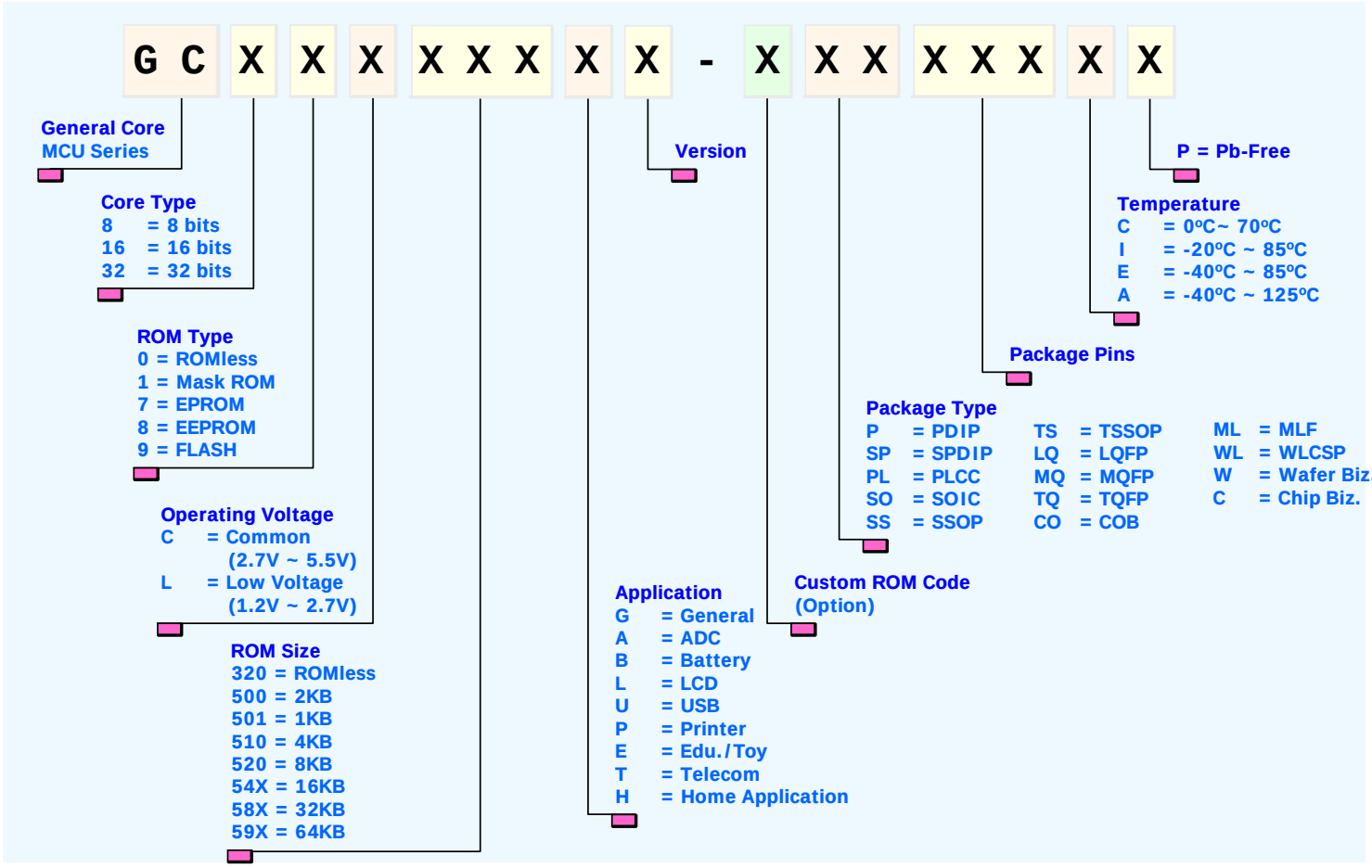
[100-TQFP]

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
D	0.551 BSC			14.00 BSC		
E	0.551 BSC			14.00 BSC		
e	0.020 BSC			0.50 BSC		
H_D	0.630 BSC			16.00 BSC		
H_E	0.630 BSC			16.00 BSC		
L	-	0.039	-	-	1.00	-
L_1	0.018	0.024	0.029	0.45	0.60	0.75
a	0°	-	7°	0°	-	7°
c	0°	-	-	0°	-	-

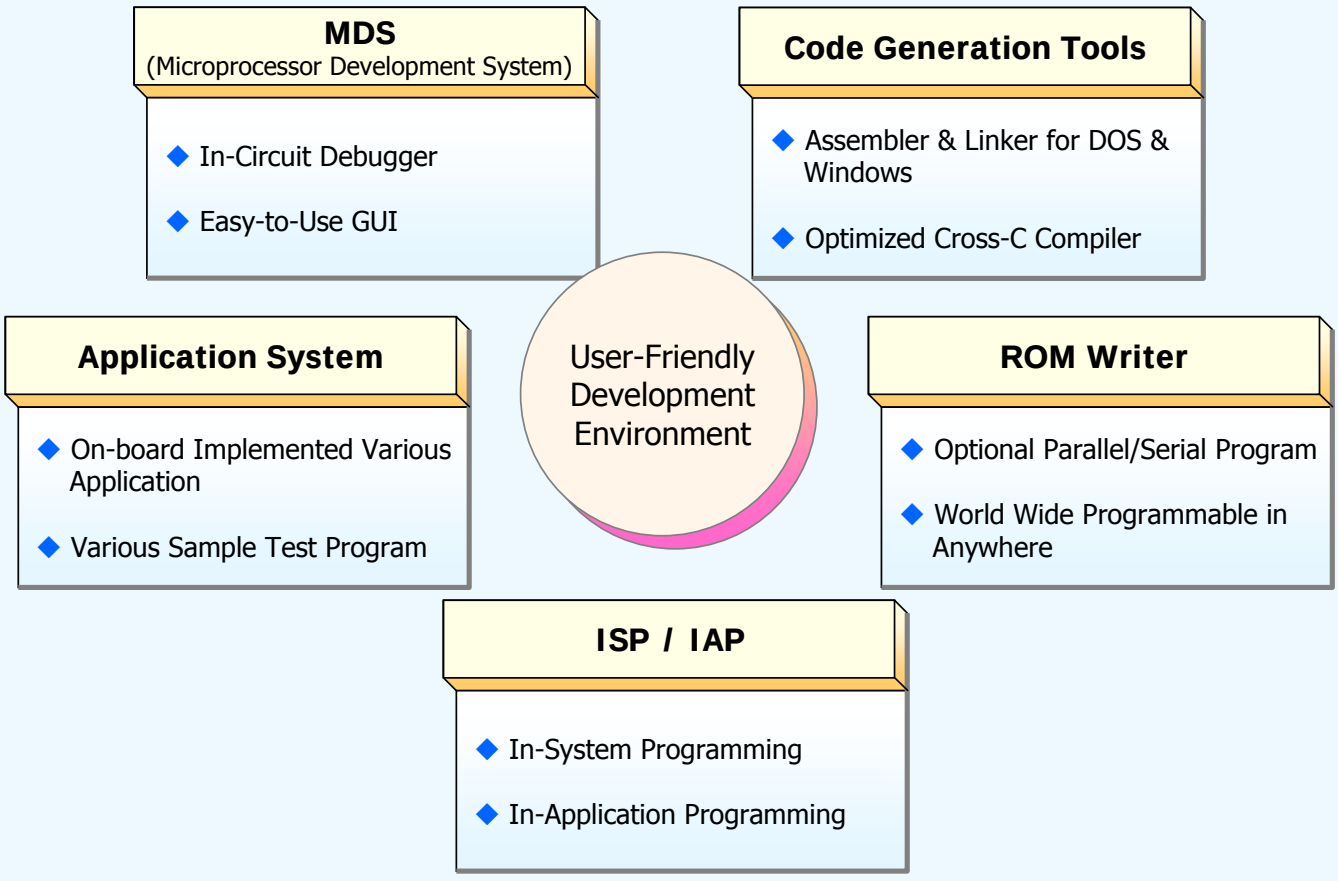
Notes:

1. Dimension D * E do not include interlead flash.
2. Controlling dimension: Inches
3. General appearance spec. should be based on final visual inspection spec.

14. Product Numbering System



15. Supporting tools



Appendix A : Instruction Set (1/19)

- Note on Instruction Set and Addressing Modes

Notation	Descriptions
Rn	Register R0 ~ R7 of the currently selected Register Bank (RB0 ~ RB3).
direct	The address of 8-bit internal data location. This could be an IRAM location (0x00 ~ 0x7F; 128 bytes) or a SFR (0x80 ~ 0xFF).
@Ri	8-bit IRAM location (0x00 ~ 0xFF; 256 bytes) addressed indirectly through register **R0** or **R1**.
#data	8-bit constant included in instruction.
#data16	16-bit constant included in instruction.
addr16	16-bit destination address. Used by **LCALL** & **LJMP**. The branch can be anywhere within the 64kbytes program memory address space. (MiDAS1.1 Family : 4kbytes program memory)
addr11	11-bit destination address. Used by **ACALL** & **AJMP**. The branch will be within the same 2kbytes page of program memory as the first byte of the following instruction.
rel	Signed (2's complement number) 8-bit offset byte. Used by **SJMP** and all conditional jumps. Range is -128 to +127 byte relative to first byte of the following instruction.
bit	Direct addressed bit n IRAM of SFR.

Appendix A : Instruction Set (2/19)

ADD A, <src-byte>

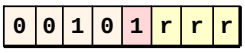
1 cycle = 4 clocks

Add

ADD A, Rn

Operation : (A) ← (A) + (Rn)

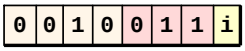
Encoding : HEX: 28h, #bytes: 1, Cycles: 1



ADD A, @Ri

Operation : (A) ← (A) + ((Ri))

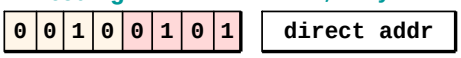
Encoding : HEX: 26h, #bytes: 1, Cycles: 1



ADD A, direct

Operation : (A) ← (A) + (direct)

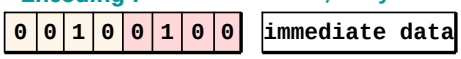
Encoding : HEX: 25h, #bytes: 2, Cycles: 2



ADD A, #data

Operation : (A) ← (A) + data

Encoding : HEX: 24h, #bytes: 2, Cycles: 2



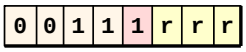
ADDC A, <src-byte>

Add with Carry

ADDC A, Rn

Operation : (A) ← (A) + (C) + (Rn)

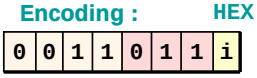
Encoding : HEX: 38h, #bytes: 1, Cycles: 1



ADDC A, @Ri

Operation : (A) ← (A) + (C) + ((Ri))

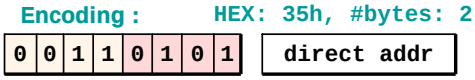
Encoding : HEX: 36h, #bytes: 1, Cycles: 1



ADDC A, direct

Operation : (A) ← (A) + (C) + (direct)

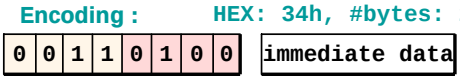
Encoding : HEX: 35h, #bytes: 2, Cycles: 2



ADDC A, #data

Operation : (A) ← (A) + (C) + data

Encoding : HEX: 34h, #bytes: 2, Cycles: 2



Appendix A : Instruction Set (3/19)

SUBB A, <src-byte>

Subtract with Borrow

SUBB A, Rn

Operation : (A) ← (A) - (C) - (Rn)

Encoding : HEX: 98h, #bytes: 1, Cycles: 1

1	0	0	1	1	r	r	r

SUBB A, @Ri

Operation : (A) ← (A) - (C) - ((Ri))

Encoding : HEX: 96h, #bytes: 1, Cycles: 1

1	0	0	1	0	1	1	i

SUBB A, direct

Operation : (A) ← (A) - (C) - (direct)

Encoding : HEX: 95h, #bytes: 2, Cycles: 2

1	0	0	1	0	1	0	1	direct addr

SUBB A, #data

Operation : (A) ← (A) - (C) - data

Encoding : HEX: 94h, #bytes: 2, Cycles: 2

1	0	0	1	0	1	0	0	immediate data

INC <byte>

Increment

INC A

Operation : (A) ← (A) + 1

Encoding : HEX: 04h, #bytes: 1, Cycles: 1

0	0	0	0	0	1	0	0

INC Rn

Operation : (Rn) ← (Rn) + 1

Encoding : HEX: 08h, #bytes: 1, Cycles: 1

0	0	0	0	1	r	r	r

INC @Ri

Operation : ((Ri)) ← ((Ri)) + 1

Encoding : HEX: 06h, #bytes: 1, Cycles: 1

0	0	0	0	0	1	1	i

INC direct

Operation : (direct) ← (direct) + 1

Encoding : HEX: 05h, #bytes: 2, Cycles: 2

0	0	0	0	0	1	0	1	direct addr

INC DPTR

Operation : (DPTR) ← (DPTR) + 1

Encoding : HEX: A3h, #bytes: 1, Cycles: 1

1	0	1	0	0	0	1	1

Appendix A : Instruction Set (4/19)

DEC <byte>

Decrement

DEC A

Operation : (A) ← (A) - 1

Encoding : HEX: 14h, #bytes: 1, Cycles: 1

0	0	0	1	0	1	0	0

DEC Rn

Operation : (Rn) ← (Rn) - 1

Encoding : HEX: 18h, #bytes: 1, Cycles: 1

0	0	0	1	1	r	r	r

DEC @Ri

Operation : ((Ri)) ← ((Ri)) - 1

Encoding : HEX: 16h, #bytes: 1, Cycles: 1

0	0	0	1	0	1	1	i

DEC direct

Operation : (direct) ← (direct) - 1

Encoding : HEX: 15h, #bytes: 1, Cycles: 1

0	0	0	1	0	1	0	1

direct addr

DEC DPTR

Operation : (DPTR) ← (DPTR) - 1

Encoding : HEX: A5h, #bytes: 1, Cycles: 1

1	0	1	0	0	1	0	1

MUL AB

Multiply

Operation : $(A)_{7-0}$ $(B)_{15-8}$ ← (A) x (B)

Encoding : HEX: A4h, #bytes: 1, Cycles: 3

1	0	1	0	0	1	0	0

DIV AB

Divide

Operation : $(A)_{15-8}$ $(B)_{7-0}$ ← (A) / (B)

Encoding : HEX: 84h, #bytes: 1, Cycles: 3

1	0	0	0	0	1	0	0

Appendix A : Instruction Set (5/19)

DA A

Decimal-adjust Accumulator for Addition

Operation :

```
IF [[(A3-0)>9] ∨ [(AC)=1]]
      THEN (A3-0) ← (A3-0)+6
IF [[(A7-4)>9] ∨ [(C)=1]]
      THEN (A7-4) ← (A7-4)+6
```

Encoding : HEX: D4h, #bytes: 1, Cycles: 1

1	1	0	1	0	1	0	0

ANL <dest-byte>, <src-byte>

Logical AND for byte variables

ANL A, Rn

Operation : (A) ← (A) ^ (Rn)

Encoding : HEX: 58h, #bytes: 1, Cycles: 1

0	1	0	1	1	r	r	r

ANL A, @Ri

Operation : (A) ← (A) ^ ((Ri))

Encoding : HEX: 56h, #bytes: 1, Cycles: 1

0	1	0	1	0	1	1	i

ANL A, direct

Operation : (A) ← (A) ^ (direct)

Encoding : HEX: 55h, #bytes: 2, Cycles: 2

0	1	0	1	0	1	0	1	direct addr

ANL A, #data

Operation : (A) ← (A) ^ data

Encoding : HEX: 54h, #bytes: 2, Cycles: 2

0	1	0	1	0	1	0	0	immediate data

ANL direct, A

Operation : (direct) ← (direct) ^ (A)

Encoding : HEX: 52h, #bytes: 2, Cycles: 2

0	1	0	1	0	0	1	0	direct addr

ANL direct, #data

Operation : (direct) ← (direct) ^ data

Encoding : HEX: 53h, #bytes: 3, Cycles: 3

0	1	0	1	0	0	1	1	direct addr	immediate data

Appendix A : Instruction Set (6/19)

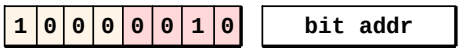
ANL C, <src-bit>

Logical AND for bit variables

ANL C, bit

Operation : (C) ← (C) ^ (bit)

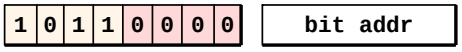
Encoding : HEX: 82h, #bytes: 2, Cycles: 2



ANL C, /bit

Operation : (C) ← (C) ^ ~(bit)

Encoding : HEX: B0h, #bytes: 2, Cycles: 2



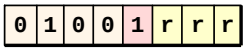
ORL <dest-byte>, <src-byte>

Logical OR for byte variables

ORL A, Rn

Operation : (A) ← (A) ∨ (Rn)

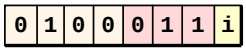
Encoding : HEX: 48h, #bytes: 1, Cycles: 1



ORL A, @Ri

Operation : (A) ← (A) ∨ ((Ri))

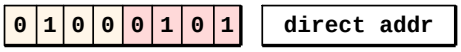
Encoding : HEX: 46h, #bytes: 1, Cycles: 1



ORL A, direct

Operation : (A) ← (A) ∨ (direct)

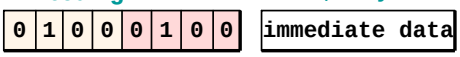
Encoding : HEX: 45h, #bytes: 2, Cycles: 2



ORL A, #data

Operation : (A) ← (A) ∨ data

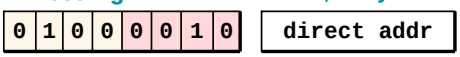
Encoding : HEX: 44h, #bytes: 2, Cycles: 2



ORL direct, A

Operation : (direct) ← (direct) ∨ (A)

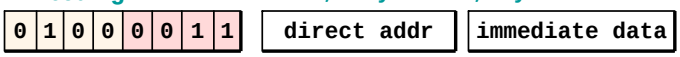
Encoding : HEX: 42h, #bytes: 2, Cycles: 2



ORL direct, #data

Operation : (direct) ← (direct) ∨ data

Encoding : HEX: 43h, #bytes: 3, Cycles: 3



Appendix A : Instruction Set (7/19)

ORL C, <src-byte>

Logical OR for byte variables

ORL C, bit

Operation : (C) ← (C) ∨ (bit)

Encoding : HEX: 72h, #bytes: 2, Cycles: 2

0	1	1	1	0	0	1	0	bit addr

ORL C, /bit

Operation : (C) ← (C) ∨ ~(bit)

Encoding : HEX: A0h, #bytes: 2, Cycles: 2

1	0	1	0	0	0	0	0	bit addr

XRL <dest-byte>, <src-byte>

Logical Exclusive-OR for byte variables

XRL A, Rn

Operation : (A) ← (A) ⊕ (Rn)

Encoding : HEX: 68h, #bytes: 1, Cycles: 1

0	1	1	0	1	r	r	r

XRL A, @Ri

Operation : (A) ← (A) ⊕ ((Ri))

Encoding : HEX: 66h, #bytes: 1, Cycles: 1

0	1	1	0	0	1	1	i

XRL A, direct

Operation : (A) ← (A) ⊕ (direct)

Encoding : HEX: 65h, #bytes: 2, Cycles: 2

0	1	1	0	0	1	0	1	direct addr

XRL A, #data

Operation : (A) ← (A) ⊕ data

Encoding : HEX: 64h, #bytes: 2, Cycles: 2

0	1	1	0	0	1	0	0	immediate data

XRL direct, A

Operation : (direct) ← (direct) ⊕ (A)

Encoding : HEX: 62h, #bytes: 2, Cycles: 2

0	1	1	0	0	0	1	0	direct addr

XRL direct, #data

Operation : (direct) ← (direct) ⊕ data

Encoding : HEX: 63h, #bytes: 3, Cycles: 3

0	1	1	0	0	0	1	1	direct addr	immediate Data

Appendix A : Instruction Set (8/19)

CLR A

Clear Accumulator

Operation : (A) ← 0

Encoding : HEX: E4h, #bytes: 1, Cycles: 1

1	1	1	0	0	1	0	0

CLR <bit>

Clear bit

CLR C

Operation : (C) ← 0

Encoding : HEX: C3h, #bytes: 1, Cycles: 1

1	1	0	0	0	0	1	1

CLR bit

Operation : (bit) ← 0

Encoding : HEX: C2h, #bytes: 2, Cycles: 2

1	1	0	0	0	0	1	0	bit addr

CPL A

Complement Accumulator

Operation : (A) ← ~(A)

Encoding : HEX: F4h, #bytes: 1, Cycles: 1

1	1	1	1	0	1	0	0

CPL <bit>

Complement bit

CPL C

Operation : (C) ← ~(C)

Encoding : HEX: B3h, #bytes: 1, Cycles: 1

1	0	1	1	0	0	1	1

CPL bit

Operation : (bit) ← ~(bit)

Encoding : HEX: B2h, #bytes: 2, Cycles: 2

1	0	1	1	0	0	1	0	bit addr

Appendix A : Instruction Set (9/19)

RL A

Rotate Accumulator Left

Operation :
$(A_{n+1}) \leftarrow (A_n)$ n=0~6
$(A_0) \leftarrow (A_7)$

Encoding : HEX: 23h, #bytes: 1, Cycles: 1

0	0	1	0	0	0	1	1

RLC A

Rotate Accumulator Left through the Carry flag

Operation :
$(A_{n+1}) \leftarrow (A_n)$ n=0~6
$(A_0) \leftarrow (C)$
$(C) \leftarrow (A_7)$

Encoding : HEX: 33h, #bytes: 1, Cycles: 1

0	0	1	1	0	0	1	1

RR A

Rotate Accumulator Right

Operation :
$(A_n) \leftarrow (A_{n+1})$ n=0~6
$(A_7) \leftarrow (A_0)$

Encoding : HEX: 03h, #bytes: 1, Cycles: 1

0	0	0	0	0	0	1	1

RRC A

Rotate Accumulator Right through the Carry flag

Operation :
$(A_n) \leftarrow (A_{n+1})$ n=0~6
$(A_7) \leftarrow (C)$
$(C) \leftarrow (A_0)$

Encoding : HEX: 13h, #bytes: 1, Cycles: 1

0	0	0	1	0	0	1	1

SWAP A

Swap nibbles within the Accumulator

Operation : $(A_{3-0}) \leftrightarrow (A_{7-4})$

Encoding : HEX: C4h, #bytes: 1, Cycles: 1

1	1	0	0	0	1	0	0

Appendix A : Instruction Set (10/19)

MOV <dest-byte>, <src-byte>

Move byte variable

MOV A, Rn

Operation : (A) ← (Rn)

Encoding : HEX: E8h, #bytes: 1, Cycles: 1

1	1	1	0	1	r	r	r

MOV A, @Ri

Operation : (A) ← ((Ri))

Encoding : HEX: E6h, #bytes: 1, Cycles: 1

1	1	1	0	0	1	1	i

MOV A, direct

Operation : (A) ← (direct)

Encoding : HEX: E5h, #bytes: 2, Cycles: 2

1	1	1	0	0	1	0	1	direct addr

MOV A, #data

Operation : (A) ← data

Encoding : HEX: 74h, #bytes: 2, Cycles: 2

0	1	1	1	0	1	0	0	immediate data

MOV Rn, A

Operation : (Rn) ← (A)

Encoding : HEX: F8h, #bytes: 1, Cycles: 1

1	1	1	1	1	r	r	r

MOV Rn, direct

Operation : (Rn) ← (direct)

Encoding : HEX: A8h, #bytes: 2, Cycles: 2

1	0	1	0	1	r	r	r	direct addr

MOV Rn, #data

Operation : (Rn) ← data

Encoding : HEX: 78h, #bytes: 2, Cycles: 2

0	1	1	1	1	r	r	r	immediate data

MOV direct, A

Operation : (direct) ← (A)

Encoding : HEX: F5h, #bytes: 2, Cycles: 2

1	1	1	1	0	1	0	1	direct addr

MOV direct, Rn

Operation : (direct) ← (Rn)

Encoding : HEX: 88h, #bytes: 2, Cycles: 2

1	0	0	0	1	r	r	r	direct addr

Appendix A : Instruction Set (11/19)

MOV direct, @Ri

Operation : (direct) ← ((Ri))

Encoding : HEX: 86h, #bytes: 2, Cycles: 2

1	0	0	0	0	1	1	i	direct addr

MOV direct, direct

Operation : (direct) ← (direct)

Encoding : HEX: 85h, #bytes: 3, Cycles: 3

1	0	0	0	0	1	0	1	direct addr(src)	direct addr(dest)

MOV direct, #data

Operation : (direct) ← data

Encoding : HEX: 75h, #bytes: 3, Cycles: 3

0	1	1	1	0	1	0	1	direct addr	immediate data

MOV @Ri, A

Operation : ((Ri)) ← (A)

Encoding : HEX: F6h, #bytes: 1, Cycles: 1

1	1	1	1	0	1	1	i

MOV @Ri, direct

Operation : ((Ri)) ← (direct)

Encoding : HEX: A6h, #bytes: 2, Cycles: 2

1	0	1	0	0	1	1	i	direct addr

MOV @Ri, #data

Operation : ((Ri)) ← data

Encoding : HEX: 76h, #bytes: 2, Cycles: 2

0	1	1	1	0	1	1	i	immediate Data

MOV <dest-bit>, <src-bit>

Move bit data

MOV C, bit

Operation : (C) ← (bit)

Encoding : HEX: A2h, #bytes: 2, Cycles: 2

1	0	1	0	0	0	1	0	bit addr

MOV bit, C

Operation : (bit) ← (C)

Encoding : HEX: 92h, #bytes: 2, Cycles: 2

1	0	0	1	0	0	1	0	bit addr

Appendix A : Instruction Set (12/19)

MOV DPTR, #data16

Load Data Pointer with a 16-bit constant

Operation :
(DPTR) ← $data_{15-0}$
(DPH,DPL) ← ($data_{15-8}$,$data_{7-0}$)

Encoding : HEX: 90h, #bytes: 3, Cycles: 3

1	0	0	1	0	0	0	0	immed. data 15-8	immed. data 7-0

MOVC A, @A + <base-reg>

Move Code byte

MOVC A, @A + DPTR

Operation : (A) ← ((A) + (DPTR))

Encoding : HEX: 93h, #bytes: 1, Cycles: 2

1	0	0	1	0	0	1	1

MOVC A, @A + PC

Operation :
(PC) ← (PC) + 1
(A) ← ((A) + (PC))

Encoding : HEX: 83h, #bytes: 1, Cycles: 2

1	0	0	0	0	0	1	1

MOVX <dest-byte>, <src-byte>

Move External

MOVX A, @Ri

Operation : (A) ← ((Ri))

Encoding : HEX: E2h, #bytes: 1, Cycles: 3

1	1	1	0	0	0	1	i

MOVX A, @DPTR

Operation : (A) ← ((DPTR))

Encoding : HEX: E0h, #bytes: 1, Cycles: 3

1	1	1	0	0	0	0	0

MOVX @Ri, A

Operation : ((Ri)) ← (A)

Encoding : HEX: F2h, #bytes: 1, Cycles: 3

1	1	1	1	0	0	1	i

MOVX @DPTR, A

Operation : ((DPTR)) ← (A)

Encoding : HEX: F0h, #bytes: 1, Cycles: 3

1	1	1	1	0	0	0	0

Appendix A : Instruction Set (13/19)

XCH A, <src-byte>

Exchange Accumulator with byte variable

XCH A, Rn

Operation : (A) ↔ (Rn)

Encoding : HEX: C8h, #bytes: 1, Cycles: 1

1	1	0	0	1	r	r	r

XCH A, @Ri

Operation : (A) ↔ ((Ri))

Encoding : HEX: C6h, #bytes: 1, Cycles: 1

1	1	0	0	0	1	1	i

XCH A, direct

Operation : (A) ↔ (direct)

Encoding : HEX: C5h, #bytes: 2, Cycles: 2

1	1	0	0	0	1	0	1	direct addr

XCHD A, @Ri

Exchange Digit

Operation : $(A_{3\text{-}0}) \leftrightarrow ((Ri))_{3\text{-}0}$

Encoding : HEX: D6h, #bytes: 1, Cycles: 1

1	1	0	1	0	1	1	i

PUSH direct

Push onto stack

Operation :
(SP) ← (SP) + 1
((SP)) ← (direct)

Encoding : HEX: C0h, #bytes: 2, Cycles: 2

1	1	0	0	0	0	0	0	direct addr

POP direct

Pop onto stack

Operation :
(direct) ← ((SP))
(SP) ← (SP) – 1

Encoding : HEX: D0h, #bytes: 2, Cycles: 2

1	1	0	1	0	0	0	0	direct addr

Appendix A : Instruction Set (14/19)

SETB <bit>

Set bit

SETB C

Operation : (C) ← 1

Encoding : HEX: D3h, #bytes: 1, Cycles: 1

1	1	0	1	0	0	1	1

SETB bit

Operation : (bit) ← 1

Encoding : HEX: D2h, #bytes: 2, Cycles: 2

1	1	0	1	0	0	1	0	bit addr

JC rel

Jump if Carry is set

Operation :
(PC) ← (PC) + 2
If (C) = 1, then (PC) ← (PC) + rel

Encoding : HEX: 40h, #bytes: 2, Cycles: 3

0	1	0	0	0	0	0	0	relative addr

JNC rel

Jump if Carry is not set

Operation :
(PC) ← (PC) + 2
If (C) = 0, then (PC) ← (PC) + rel

Encoding : HEX: 50h, #bytes: 2, Cycles: 3

0	1	0	1	0	0	0	0	relative addr

JB bit, rel

Jump if Bit is set

Operation :
(PC) ← (PC) + 3
If (bit) = 1, then (PC) ← (PC)+rel

Encoding : HEX: 20h, #bytes: 3, Cycles: 4

0	0	1	0	0	0	0	0	bit addr	relative addr

JNB bit, rel

Jump if Bit is not set

Operation :
(PC) ← (PC) + 3
If (bit) = 0, then (PC) ← (PC)+rel

Encoding : HEX: 30h, #bytes: 3, Cycles: 4

0	0	1	1	0	0	0	0	bit addr	relative addr

Appendix A : Instruction Set (15/19)

JBC bit, rel

Jump if Bit is set and Clear bit

Operation :

```
(PC)   ← (PC) + 3
If (bit) = 1,
then (bit) ← 0, (PC) ← (PC) + rel
```

Encoding : HEX: 10h, #bytes: 3, Cycles: 4

0	0	0	1	0	0	0	0	bit addr	relative addr

ACALL addr11

Absolute Subroutine Call

Operation :

```
(PC)    ← (PC) + 2
(SP)    ← (SP) + 1
((SP))  ← (PC7-0)
(SP)    ← (SP) + 1
((SP))  ← (PC15-8)
(PC10-0)← page address
```

Encoding : HEX: 11h, #bytes: 2, Cycles: 3

a_{10}	a_9	a_8	1	0	0	0	1	a_{7-0}

LCALL addr16

Long Subroutine Call

Operation :

```
(PC)    ← (PC) + 3
(SP)    ← (SP) + 1
((SP))  ← (PC7-0)
(SP)    ← (SP) + 1
((SP))  ← (PC15-8)
(PC)    ← addr15-0
```

Encoding : HEX: 12h, #bytes: 3, Cycles: 4

0	0	0	1	0	0	1	0	a_{15-8}	a_{7-0}

Appendix A : Instruction Set (16/19)

RET

Return from Subroutine

Operation :

$(PC_{15-8}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$
$(PC_{7-0}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$

Encoding : HEX: 22h, #bytes: 1, Cycles: 2

0	0	1	0	0	0	1	0

RETI

Return from Interrupt

Operation :

$(PC_{15-8}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$
$(PC_{7-0}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$

Encoding : HEX: 32h, #bytes: 1, Cycles: 2

0	0	1	1	0	0	1	0

AJMP addr11

Absolute Jump

Operation :

$(PC) \leftarrow (PC) + 2$
$(PC_{10-0}) \leftarrow$ page address

Encoding : HEX: 01h, #bytes: 2, Cycles: 3

a_{10}	a_9	a_8	0	0	0	0	1	a_{7-0}

SJMP rel

Short Jump (Relative address)

Operation :

$(PC) \leftarrow (PC) + 2$
$(PC_{10-0}) \leftarrow (PC) + rel$

Encoding : HEX: 80h, #bytes: 2, Cycles: 3

1	0	0	0	0	0	0	0	relative addr

LJMP addr16

Long Jump

Operation : $(PC) \leftarrow addr_{15-0}$

Encoding : HEX: 02h, #bytes: 3, Cycles: 4

0	0	0	0	0	0	1	0	a_{15-8}	a_{7-0}

Appendix A : Instruction Set (17/19)

JMP @A + DPTR

Jump Indirect Relative to the DPTR

Operation : (PC) ← (A) + (DPTR)

Encoding : HEX: 73h, #bytes: 1, Cycles: 2

0	1	1	1	0	0	1	1

JZ rel

Jump if Accumulator is Zero

Operation : (PC) ← (PC) + 2
If (A)=0, then (PC) ← (PC) + rel

Encoding : HEX: 60h, #bytes: 2, Cycles: 3

0	1	1	0	0	0	0	0	relative addr

JNZ rel

Jump if Accumulator is Not Zero

Operation : (PC) ← (PC) + 2
If (A)≠0, then (PC) ← (PC) + rel

Encoding : HEX: 70h, #bytes: 2, Cycles: 3

0	1	1	1	0	0	0	0	relative addr

Appendix A : Instruction Set (18/19)

CJNE <dest-byte>, <src-byte>, rel

Compare and Jump if Not Equal

CJNE A, direct, rel

Operation :

```
(PC)  ← (PC) + 3
If (A) ≠ (direct),
      then (PC) ← (PC) + rel
If (A) < (direct), then (C) ← 1
Else                  (C) ← 0
```

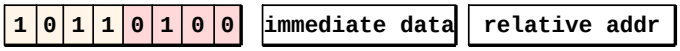
Encoding : HEX: B5h, #bytes: 3, Cycles: 4

CJNE A, #data, rel

Operation :

```
(PC)  ← (PC) + 3
If (A) ≠ data,
      then (PC) ← (PC) + rel
If (A) < data, then (C) ← 1
Else                (C) ← 0
```

Encoding : HEX: B4h, #bytes: 3, Cycles: 4

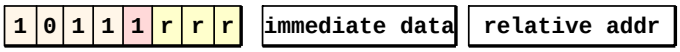


CJNE Rn, #data, rel

Operation :

```
(PC)  ← (PC) + 3
If (Rn) ≠ data,
      then (PC) ← (PC) + rel
If (Rn) < data, then (C) ← 1
Else                (C) ← 0
```

Encoding : HEX: B8h, #bytes: 3, Cycles: 4

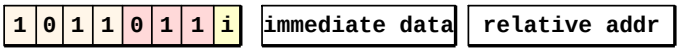


CJNE @Ri, #data, rel

Operation :

```
(PC)  ← (PC) + 3
If ((Ri)) ≠ data,
      then (PC) ← (PC) + rel
If ((Ri)) < data, then (C) ← 1
Else                  (C) ← 0
```

Encoding : HEX: B6h, #bytes: 3, Cycles: 4



Appendix A : Instruction Set (19/19)

DJNZ <byte>, rel

Decrement and Jump if Not Zero

DJNZ Rn, rel

Operation :
```
(PC)  ← (PC) + 2
(Rn)  ← (Rn) - 1
If (Rn)≠0, then (PC) ← (PC) + rel
```

Encoding : HEX: D8h, #bytes: 2, Cycles: 3

DJNZ direct, rel

Operation :
```
(PC)     ← (PC) + 3
(direct)← (direct) - 1
If (direct)≠0,
       then (PC) ← (PC) + rel
```

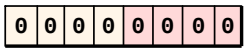
Encoding : HEX: D5h, #bytes: 3, Cycles: 4

NOP

No Operation

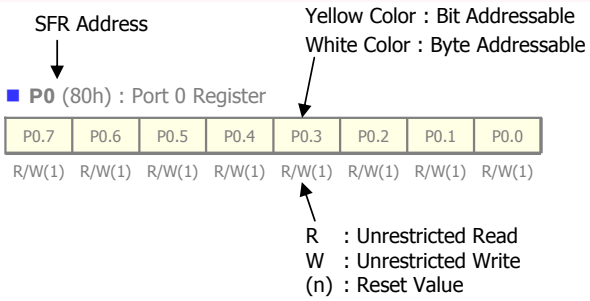
Operation : (PC) ← (PC) + 1

Encoding : HEX: 00h, #bytes: 1, Cycles: 1



Appendix B : SFR Description [80h ~ 87h] (1/17)

[How to Read a SFR Descriptions]



■ **P0** (80h) : Port 0 Register

P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- Open-drain bidirectional port.
- Multiplexing low order address/data bus during external memory access

■ **SP** (81h) : Stack Pointer Register

SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(1)	R/W(1)	R/W(1)

- Indicate where stack will start.
- Increment by PUSH and decrement by POP.

■ **DPL** (82h) : Data Pointer Low Register

DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **DPH** (83h) : Data Pointer High Register

DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **PCON** (87h) : Power Control Register

SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
R/W(0)	R/W(0)		R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- SMOD1 : Timer 1 baud rate double in UART mode 1/2/3
- SMOD0 : Enable SM0 access. Don't modify this bit.
- POF : Power off flag.
  When power-on, this bit will be set by H/W.
- GF1, GF0 : General purpose flag bit.
- PD : Stop Mode (Power-down) Bit.
- IDL : IDLE Mode Bit.

Appendix B : SFR Description [88h ~ 8Dh] (2/17)

■ **TCON** (88h) : Timer/Counter 0/1 Control Register

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ TF1 : Timer 1 overflow flag.
- ◆ TR1 : Timer 1 run enable.
- ◆ TF0 : Timer 0 overflow flag.
- ◆ TR0 : Timer 0 run enable.
- ◆ IE1 : External interrupt 1 flag.
  If IT1 = 0, cleared by S/W (software).
  If IT1 = 1, cleared automatically when go to routine.
- ◆ IT1 : External interrupt 1 type select.
  Edge detect (IT1=1) / Level detect (IT1=0; Default)
- ◆ IE0 : External interrupt 0 flag.
  If IT0 = 0, cleared by S/W (software).
  If IT0 = 1, cleared automatically when go to routine.
- ◆ IT0 : External interrupt 0 type select.
  Edge detect (IT0=1) / Level detect (IT0=0; Default)

■ **TMOD** (89h) : Timer/Counter 0/1 Mode Control Register

GATE	C/T	M1	M0	GATE	C/T	M1	M0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ Timer[1]: GATE[7], C/T[6], M1:M0[5:4]
- ◆ Timer[0]: GATE[3], C/T[2], M1:M0[1:0]
- ◆ GATE : When TRx (in TCON) is set and GATE=1, Timer x will run only while INTx pin is high (hardware control). When GATE=0, Timer x will run only while TRx=1 (software control).
- ◆ C/T : Counter or Timer Selector. Cleared for Timer operation (input from internal system clock). Set for Counter
- ◆ M1, M0 : Mode Selector bits
  [0 0] Mode 0. 13-bit T/C.
  [0 1] Mode 1. 16-bit T/C.
  [1 0] Mode 2. 8-bit Auto-Reload T/C.
  [1 1] Mode 3.
  (Timer 1) stopped, (Timer 0)
  TL0: 8-bit T/C controlled by the Timer 0 control bits.
  TH0: 8-bit T/C controlled by the Timer 1 control bits.

■ **TL0** (8Ah) : Timer/Counter 0 Low Byte Register

TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **TL1** (8Bh) : Timer/Counter 1 Low Byte Register

TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **TH0** (8Ch) : Timer/Counter 0 High Byte Register

TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **TH1** (8Dh) : Timer/Counter 1 High Byte Register

TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **CKCON** (8Eh) : Clock Control Register

WD1	WD0	T2M	T1M	T0M	-	U1T2DIS	U0T2DIS
R/W(1)	R/W(1)	R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)

- WD1, WD0 : Watchdog timer mode select
  [0,0] : 2^{17} clocks (interrupt), 2^{17} + 512 clocks (reset)
  [0,1] : 2^{20} clocks (interrupt), 2^{20} + 512 clocks (reset)
  [1,0] : 2^{23} clocks (interrupt), 2^{23} + 512 clocks (reset)
  [1,1] : 2^{26} clocks (interrupt), 2^{26} + 512 clocks (reset)
- T2M : Timer 2 clock select. When set, base time is 4 clocks.
- T1M : Timer 1 clock select. When set, base time is 4 clocks.
- T0M : Timer 0 clock select. When set, base time is 4 clocks.
- U1T2DIS : Used to disable RCLK/TCLK control for UART1 to generate its baud rate with T1 overflow
- U0T2DIS : Used to disable RCLK/TCLK control for UART0 to generate its baud rate with T1 overflow.

■ **P1** (90h) : Port 1 Register

P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- Quasi-bidirectional port with internal pull-up resistors.
- When alternative function enabled, P1.X must be "1".

■ **EXIF** (91h) : External Interrupt Flag Register

IE5	IE4	IE3	IE2	XT/RG	RGMD	RGSL	BGS
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(1)	R(0)	R/W(0)	R/W(1)

- IE5 : External interrupt 5 flag.
- IE4 : External interrupt 4 flag.
- IE3 : External interrupt 3 flag.
- IE2 : External interrupt 2 flag.
- XT/RG : System clock selection
  0 = Internal Ring oscillator is selected as system clock.
  1 = External clock is selected as system clock.
- RGMD : Ring mode. Now system clock is Ring or XTAL. Generally RGMD is the invert of XT/RG except when the ring oscillator provides clock during wake-up from power-down .
- RGSL : 1 = When wake-up from power-down mode in XTAL clock, use Ring oscillator as system clock during 65,536 XTAL clocks.
- BGS : Band-gap select. When set, LVD will run in power-down mode.

■ **C0CAP0L** (92h) : Low Capture/Compare Register of PCA0 MODULE0

C0CAP0L.7	C0CAP0L.6	C0CAP0L.5	C0CAP0L.4	C0CAP0L.3	C0CAP0L.2	C0CAP0L.1	C0CAP0L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP1L** (93h) : Low Capture/Compare Register of PCA0 MODULE1

C0CAP1L.7	C0CAP1L.6	C0CAP1L.5	C0CAP1L.4	C0CAP1L.3	C0CAP1L.2	C0CAP1L.1	C0CAP1L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP2L** (94h) : Low Capture/Compare Register of PCA0 MODULE2

C0CAP2L.7	C0CAP2L.6	C0CAP2L.5	C0CAP2L.4	C0CAP2L.3	C0CAP2L.2	C0CAP2L.1	C0CAP2L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP3L** (95h) : Low Capture/Compare Register of PCA0 MODULE3

C0CAP3L.7	C0CAP3L.6	C0CAP3L.5	C0CAP3L.4	C0CAP3L.3	C0CAP3L.2	C0CAP3L.1	C0CAP3L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP4L** (96h) : Low Capture/Compare Register of PCA0 MODULE4

C0CAP4L.7	C0CAP4L.6	C0CAP4L.5	C0CAP4L.4	C0CAP4L.3	C0CAP4L.2	C0CAP4L.1	C0CAP4L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP5L** (97h) : Low Capture/Compare Register of PCA0 MODULE5

C0CAP5L.7	C0CAP5L.6	C0CAP5L.5	C0CAP5L.4	C0CAP5L.3	C0CAP5L.2	C0CAP5L.1	C0CAP5L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **SCON** (98h) : Serial Port Control Register of UART0

SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ SM0, SM1 : Serial Port mode select.
  [0,0] : Mode0, 8-bit shift register (OSC/4)
  [0,1] : Mode1, 8-bit UART (Variable)
  [1,0] : Mode2, 9-bit UART (OSC/32 or OSC/16)
  [1,1] : Mode3, 9-bit UART (Variable)
- ◆ SM2 : Enables the Automatic Address Recognition in Mode2 and 3.
  In Mode 1, the Validity of the Stop Bit is checked if SM2=1.
  In Mode0, SM2 should be "0".
- ◆ REN : Enable/Disable Reception.
- ◆ TB8 : 9th data bit that will be transmitted in Mode2 and 3.
- ◆ RB8 : 9th data bit that was received in Mode 2 and 3.
  In Mode1, RB8 is equal to stop bit if SM2 is "0".
  In Mode0, RB8 is not used.
- ◆ TI : Transmission interrupt flag. Must be cleared by S/W.
- ◆ RI : Reception interrupt flag. Must be cleared by S/W.

■ **SBUF** (99h) : Serial Data Buffer Register of UART0

SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ The transmission buffer and the reception buffer are separated.
- ◆ The transmission/reception buffers have the same address.

Appendix B : SFR Description [9Ah ~ A1h] (5/17)

■ **C0CAP0H** (9Ah) : High Capture/Compare Register of PCA0 MODULE0

C0CAP0H.7	C0CAP0H.6	C0CAP0H.5	C0CAP0H.4	C0CAP0H.3	C0CAP0H.2	C0CAP0H.1	C0CAP0H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP1H** (9Bh) : High Capture/Compare Register of PCA0 MODULE1

C0CAP1H.7	C0CAP1H.6	C0CAP1H.5	C0CAP1H.4	C0CAP1H.3	C0CAP1H.2	C0CAP1H.1	C0CAP1H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP2H** (9Ch) : High Capture/Compare Register of PCA0 MODULE2

C0CAP2H.7	C0CAP2H.6	C0CAP2H.5	C0CAP2H.4	C0CAP2H.3	C0CAP2H.2	C0CAP2H.1	C0CAP2H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP3H** (9Dh) : High Capture/Compare Register of PCA0 MODULE3

C0CAP3H.7	C0CAP3H.6	C0CAP3H.5	C0CAP3H.4	C0CAP3H.3	C0CAP3H.2	C0CAP3H.1	C0CAP3H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP4H** (9Eh) : High Capture/Compare Register of PCA0 MODULE4

C0CAP4H.7	C0CAP4H.6	C0CAP4H.5	C0CAP4H.4	C0CAP4H.3	C0CAP4H.2	C0CAP4H.1	C0CAP4H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAP5H** (9Fh) : High Capture/Compare Register of PCA0 MODULE5

C0CAP5H.7	C0CAP5H.6	C0CAP5H.5	C0CAP5H.4	C0CAP5H.3	C0CAP5H.2	C0CAP5H.1	C0CAP5H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **P2** (A0h) : Port 2 Register

P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- ◆ Quasi-bidirectional port with internal pull-up resistors.
- ◆ Address output when external memory access and general I/O.

■ **SBUF1** (A1h) : Serial Data Buffer Register of UART1

SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ The transmission buffer and the reception buffer are separated.
- ◆ The transmission/reception buffers have the same address.

Appendix B : SFR Description [A2h ~ A7h] (6/17)

■ **C0CAPM0** (A2h) : Mode Control Register of PCA0 MODULE0

IPWM0	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ IPWM0 : Inverted PWM output.
  If this bit is set, the PWM output is high when C0L ≥ C0CAPmL.
  The change of this bit will take effect from the next overflow / match time of PWM.
- ◆ ECOM0 : Enable comparator.
  ECOM0 = 1 enables the comparator function.
- ◆ CAPP0 : Capture positive.
  CAPP0 = 1 enables positive edge capture.
- ◆ CAPN0 : Capture negative.
  CAPN0 = 1 enables negative edge capture.
- ◆ MAT0 : Match.
  When MAT0 = 1, a match of the PCA counter with this module's comparator/capture register causes the CCF0 bit in C0CON to be set, flagging an interrupt.
- ◆ TOG0 : Toggle.
  When TOG0 = 1, a match of the PCA counter with this module's compare/capture register causes the C0EX0 pin to toggle.
- ◆ PWM0 : Pulse width modulation mode.
  PWM0 = 1 enables the C0EX0 pin to be used as a pulse width modulated output.
- ◆ ECCF0 : Enable CCF interrupt.
  Enables compare/capture flag CCF0 in the C0CON register to generate an interrupt.

■ **C0CAPM1** (A3h) : Mode Control Register of PCA0 MODULE1

IPWM1	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAPM2** (A4h) : Mode Control Register of PCA0 MODULE2

IPWM2	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAPM3** (A5h) : Mode Control Register of PCA0 MODULE3

IPWM3	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAPM4** (A6h) : Mode Control Register of PCA0 MODULE4

IPWM4	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CAPM5** (A7h) : Mode Control Register of PCA0 MODULE5

IPWM5	ECOM5	CAPP5	CAPN5	MAT5	TOG5	PWM5	ECCF5
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **IE** (A8h) : Interrupt Enable Register

EA	EADC	ET2	ES	ET1	EX1	ET0	EX0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ EA : Global interrupt enable.
- ◆ EADC : ADC interrupt enable.
- ◆ ET2 : Timer 2 interrupt enable.
- ◆ ES : Serial port interrupt enable.
- ◆ ET1 : Timer 1 interrupt enable.
- ◆ EX1 : External interrupt 1 enable.
- ◆ ET0 : Timer0 interrupt enable.
- ◆ EX0 : External interrupt 0 enable.

■ **SADDR** (A9h) : Slave Address Register of UART0

SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ Programmed with the given or broadcast address assigned to serial port 0.

■ **SADDR1** (AAh) : Slave Address Register of UART1

SADDR1.7	SADDR1.6	SADDR1.5	SADDR1.4	SADDR1.3	SADDR1.2	SADDR1.1	SADDR1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ Programmed with the given or broadcast address assigned to serial port 1.

■ **SADEN1** (ABh) : Slave Address Mask Enable Register of UART1

SADEN1.7	SADEN1.6	SADEN1.5	SADEN1.4	SADEN1.3	SADEN1.2	SADEN1.1	SADEN1.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0CON** (ACh) : PCA0 Counter Control Register

CF	CR	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ CF : PCA counter overflow flag.
- ◆ CR : PCA counter run control bit.
  Set by software to turn the PCA counter on.
- ◆ CCF5 : MODULE5 interrupt flag.
  Set by hardware when a match or capture occurs.
  Must be cleared by software.
- ◆ CCF4 : MODULE4 interrupt flag.
- ◆ CCF3 : MODULE3 interrupt flag.
- ◆ CCF2 : MODULE2 interrupt flag.
- ◆ CCF1 : MODULE1 interrupt flag.
- ◆ CCF0 : MODULE0 interrupt flag.

■ **C0MOD** (ADh) : PCA0 Counter Mode Register

CIDL	PWMDYN	-	CPS3	CPS2	CPS1	CPS0	ECF
R/W(0)	R/W(0)		R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ CIDL : Counter Idle Control.
  CIDL = 0 programs the PCA counter to continue functioning during Idle Mode.
  CIDL = 1 programs it to be stop during Idle Mode.
- ◆ PWMDYN: Dynamic PWM bit.
  If this bit is set, the dynamic PWM is generated.
  C0L is cleared when a match occurs between C0L and C0H.
  The match signal replaces the overflow signal for PWM.
- ◆ CPS[3:0] : PCA count rate (F_{PCA}) select.
- ◆ ECF : Enable PCA counter overflow interrupt.
  ECF = 1 enables CF bit int C0CON to generate an interrupt.
  ECF = 0 disables that function.

■ **C0L** (AEh) : Low Byte Register of PCA0 Counter

C0L.7	C0L.6	C0L.5	C0L.4	C0L.3	C0L.2	C0L.1	C0L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C0H** (AFh) : High Byte Register of PCA0 Counter

C0H.7	C0H.6	C0H.5	C0H.4	C0H.3	C0H.2	C0H.1	C0H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **P3** (B0h) : Port 3 Register

P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ Quasi-bidirectional port with internal pull-up resistors.
◆ When alternative function enabled, P3.X must be "1".

■ **SCON1** (B1h) : Serial Port Control Register of UART1

SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ SM0, SM1 : Serial Port mode select.
[0,0] : Mode0, 8-bit shift register (OSC/4)
[0,1] : Mode1, 8-bit UART (Variable)
[1,0] : Mode2, 9-bit UART (OSC/32 or OSC/16)
[1,1] : Mode3, 9-bit UART (Variable)

◆ SM2 : Enables the Automatic Address Recognition in Mode2 and 3.
In Mode 1, the Validity of the Stop Bit is checked if SM2=1.
In Mode0, SM2 should be "0".

◆ REN : Enable/Disable Reception.
◆ TB8 : 9th data bit that will be transmitted in Mode2 and 3.
◆ RB8 : 9th data bit that was received in Mode 2 and 3.
In Mode1, RB8 is equal to stop bit if SM2 is "0".
In Mode0, RB8 is not used.
◆ TI : Transmission interrupt flag. Must be cleared by S/W.
◆ RI : Reception interrupt flag. Must be cleared by S/W.

■ **P5** (B2h) : Port 5 Register

P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ Bidirectional port with direction and pull-up control.

■ **P6** (B3h) : Port 6 Register

P6.7	P6.6	P6.5	P6.4	P6.3	P6.2	P6.1	P6.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ Bidirectional port with direction and pull-up control.

■ **P7** (B4h) : Port 7 Register

P7.7	P7.6	P7.5	P7.4	P7.3	P7.2	P7.1	P7.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ Bidirectional port with direction and pull-up control.

Appendix B : SFR Description [B5h ~ BBh] (9/17)

■ **P8** (B5h) : Port 8 Register

P8.7	P8.6	P8.5	P8.4	P8.3	P8.2	P8.1	P8.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ Bidirectional port with direction and pull-up control.

■ **P9** (B6h) : Port 9 Register

P9.7	P9.6	P9.5	P9.4	P9.3	P9.2	P9.1	P9.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ Bidirectional port with direction and pull-up control.

■ **IPH** (B7h) : Interrupt Priority High Register

-	PADCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
R(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ PADCH : ADC interrupt priority high.
◆ PT2H : Timer 2 interrupt priority high.
◆ PSH : Serial port interrupt priority high.
◆ PT1H : Timer 1 interrupt priority high.
◆ PX1H : External interrupt 1 priority high.
◆ PT0H : Timer 0 interrupt priority high.
◆ PX0H : External interrupt 0 priority high.

■ **IP** (B8h) : Interrupt Priority Low Register

-	PADC	PT2	PS	PT	PX	PT0	PX0
R(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ PADC : ADC interrupt priority low.
◆ PT2 : Timer 2 interrupt priority low.
◆ PS : Serial port interrupt priority low.
◆ PT1 : Timer 1 interrupt priority low.
◆ PX1 : External interrupt 1 priority low.
◆ PT0 : Timer 0 interrupt priority low.
◆ PX0 : External interrupt 0 priority low.

■ **SADEN** (B9h) : Slave Address Mask Enable Register of UART0

SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **P5DIR** (BAh) : Port 5 Input/Output Control Register

P5DIR.7	P5DIR.6	P5DIR.5	P5DIR.4	P5DIR.3	P5DIR.2	P5DIR.1	P5DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 1 = Input (Default) / 0 = Output

■ **P6DIR** (BBh) : Port 6 Input/Output Control Register

P6DIR.7	P6DIR.6	P6DIR.5	P6DIR.4	P6DIR.3	P6DIR.2	P6DIR.1	P6DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 1 = Input (Default) / 0 = Output

Appendix B : SFR Description [BCh ~ C4h] (10/17)

■ **P7DIR** (BCh) : Port 7 Input/Output Control Register

P7DIR.7	P7DIR.6	P7DIR.5	P7DIR.4	P7DIR.3	P7DIR.2	P7DIR.1	P7DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 1 = Input (Default) / 0 = Output

■ **P8DIR** (BDh) : Port 8 Input/Output Control Register

P8DIR.7	P8DIR.6	P8DIR.5	P8DIR.4	P8DIR.3	P8DIR.2	P8DIR.1	P8DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 1 = Input (Default) / 0 = Output

■ **P9DIR** (BEh) : Port 9 Input/Output Control Register

P9DIR.7	P9DIR.6	P9DIR.5	P9DIR.4	P9DIR.3	P9DIR.2	P9DIR.1	P9DIR.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 1 = Input (Default) / 0 = Output

■ **AUXAD** (BFh) : High Address Register for MOVX with Ri

AUXAD.7	AUXAD.6	AUXAD.5	AUXAD.4	AUXAD.3	AUXAD.2	AUXAD.1	AUXAD.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ If ENAUX bit (IOCFG.3) is set, "MOVX A, @Ri" and "MOVX @Ri, A" instructions refer to AUXAD instead of P2 register for high address.

■ **P4** (C0h) : Port 4 Register

P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ Quasi-bidirectional port with internal pull-up resistors.
◆ When alternative function is enabled, P4.X must be "1".
◆ When ADC is used, the pull-up resistors for enabled channel are automatically disabled.

■ **P5PUP** (C2h) : Port 5 Pull-up Control Register

P5PUP.7	P5PUP.6	P5PUP.5	P5PUP.4	P5PUP.3	P5PUP.2	P5PUP.1	P5PUP.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 1 = Pull-up resistor ON (Default) / 0 = Pull-up resistor OFF

■ **P6PUP** (C3h) : Port 6 Pull-up Control Register

P6PUP.7	P6PUP.6	P6PUP.5	P6PUP.4	P6PUP.3	P6PUP.2	P6PUP.1	P6PUP.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 1 = Pull-up resistor ON (Default) / 0 = Pull-up resistor OFF

■ **PMR** (C4h) : Power Management Control Register

-	-	-	-	XTOFF	ALEOFF	-	-
				R/W(0)	R/W(0)		

◆ XTOFF : 1 = External crystal oscillator disable.
0 = External crystal will restart (Default).
◆ ALEOFF : 1 = ALE toggling disable.
0 = ALE toggling enable (Default).

■ STATUS (C5h) : Crystal Status Register

-	-	-	XTUP	-	-	-	-
			R(1)				

◆ XTUP : Crystal oscillator warm-up status.
It represents if the crystal clock is stable(1) or not(0).
Cleared by H/W if XTOFF is set or if PD is set and WDT is not enabled.
Set by H/W after crystal stabilization time.

■ OSCICN (C6h) : Internal Ring Oscillator Control Register

-	-	-	-	-	RINGON	DIV1	DIV0
					R/W(1)	R/W(0)	R/W(0)

◆ RINGON : Internal RING oscillator operates.
0 = Internal RING oscillator disable.
Don't clear RINGON bit when XTRG = 0.

◆ DIV1, DIV0 : Ring oscillator divider.
[0,0] = F_{RING} / 1 [0,1] = F_{RING} / 2
[1,0] = F_{RING} / 4 [1,1] = F_{RING} / 8

F_{RING} = 2.8 MHz (at room temp. 3.3V, +/- 15%)

■ IOCFG (C7h) : I/O Configuration Register

-	-	-	-	ENAUX	-	-	PKGOPT
				R/W(0)			R/W(0)

◆ ENAUX : Select AUXAD for MOVX with Ri.
1 = AUXAD register serves high address for MOVX with Ri.
0 = P2 register serves high address for MOVX with Ri.

◆ PKGOPT : Must be "1" for 44-pin package.

■ T2CON (C8h) : Timer/Counter 2 Control Register

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

◆ TF2 : Timer 2 overflow flag.
◆ EXF2 : Timer 2 external flag.
◆ RCLK : Receive clock flag.
◆ TCLK : Transmit clock flag.
◆ EXEN2 : Timer 2 external enable flag.
◆ TR2 : Timer 2 run flag.
◆ C/T2 : Timer 2 Timer/Counter select. When set, counter by T2.
◆ CP/RL2 : Capture/Reload flag.
CP/RL2 = 0, Reload. (TH2,TL2) ← (RCAP2H,RCAP2L)
CP/RL2 = 1, Capture. (RCAP2H,RCAP2L) ← (TH2,TL2)

■ T2MOD (C9h) : Timer/Counter 2 Mode Control Register

-	-	-	-	-	-	T2OE	DCEN
						R/W(0)	R/W(0)

◆ T2OE : Timer 2 clock output enable. When set, clock output to P1.0.
◆ DCEN : Timer 2 down count enable. When set, count down.

■ RCAP2L (CAh) : Timer/Count 2 Capture/Reload Low Byte Register

RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ RCAP2H (CBh) : Timer/Counter 2 Capture/Reload High Byte Register

RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **TL2** (CCh) : Timer/Counter 2 Low Byte Register

TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **TH2** (CDh) : Timer/Counter 2 High Byte Register

TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CON** (CEh) : PCA1 Counter Control Register

CF	CR	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ CF : PCA counter overflow flag.
- ◆ CR : PCA counter run control bit.
  Set by software to turn the PCA counter on.
- ◆ CCF5 : MODULE5 interrupt flag.
  Set by hardware when a match or capture occurs.
  Must be cleared by software.
- ◆ CCF4 : MODULE4 interrupt flag.
- ◆ CCF3 : MODULE3 interrupt flag.
- ◆ CCF2 : MODULE2 interrupt flag.
- ◆ CCF1 : MODULE1 interrupt flag.
- ◆ CCF0 : MODULE0 interrupt flag.

■ **C1MOD** (CFh) : PCA1 Counter Mode Register

CIDL	PWMDYN	-	CPS3	CPS2	CPS1	CPS0	ECF
R/W(0)	R/W(0)		R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ CIDL : Counter Idle control.
  CIDL = 0 programs the PCA counter to continue functioning during Idle Mode.
  CIDL = 1 programs it to be stop during Idle Mode.
- ◆ PWMDYN: Dynamic PWM bit.
  If this bit is set, the dynamic PWM is generated.
  C1L is cleared when a match occurs between C1L and C1H.
  The match signal replaces the overflow signal for PWM.
- ◆ CPS[3:0] : PCA prescaler rate (F_{PCA}) selection.
- ◆ ECF : Enable PCA counter overflow interrupt.
  ECF = 1 enables CF bit int C1CON to generate an interrupt.
  ECF = 0 disables that function.

■ **PSW** (D0h) : Program Status Word Register

CY	AC	F0	RS1	RS0	OV	F1	P
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R(0)

- ◆ CY : Carry Flag.
- ◆ AC : Auxiliary carry flag.
- ◆ F0 : User flag 0.
- ◆ RS1, RS0: Register bank select
  [0,0] : Bank 0
  [0,1] : Bank 1
  [1,0] : Bank 2
  [1,1] : Bank 3
- ◆ OV : Overflow flag.
- ◆ F1 : User flag 1.
- ◆ P : Parity bit. Set/clear by H/W according to ACC odd parity.

Appendix B : SFR Description [D2h ~ D9h] (13/17)

■ **C1CAP0L** (D2h) : Low Capture/Compare Register of PCA1 MODULE0

C1CAP0L.7	C1CAP0L.6	C1CAP0L.5	C1CAP0L.4	C1CAP0L.3	C1CAP0L.2	C1CAP0L.1	C1CAP0L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP1L** (D3h) : Low Capture/Compare Register of PCA1 MODULE1

C1CAP1L.7	C1CAP1L.6	C1CAP1L.5	C1CAP1L.4	C1CAP1L.3	C1CAP1L.2	C1CAP1L.1	C1CAP1L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP2L** (D4h) : Low Capture/Compare Register of PCA1 MODULE2

C1CAP2L.7	C1CAP2L.6	C1CAP2L.5	C1CAP2L.4	C1CAP2L.3	C1CAP2L.2	C1CAP2L.1	C1CAP2L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP3L** (D5h) : Low Capture/Compare Register of PCA1 MODULE3

C1CAP3L.7	C1CAP3L.6	C1CAP3L.5	C1CAP3L.4	C1CAP3L.3	C1CAP3L.2	C1CAP3L.1	C1CAP3L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP4L** (D6h) : Low Capture/Compare Register of PCA1 MODULE4

C1CAP4L.7	C1CAP4L.6	C1CAP4L.5	C1CAP4L.4	C1CAP4L.3	C1CAP4L.2	C1CAP4L.1	C1CAP4L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP5L** (D7h) : Low Capture/Compare Register of PCA1 MODULE5

C1CAP5L.7	C1CAP5L.6	C1CAP5L.5	C1CAP5L.4	C1CAP5L.3	C1CAP5L.2	C1CAP5L.1	C1CAP5L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **WDCON** (D8h) : Watchdog Timer & Power Status Register

-	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT
	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ POR : Power-on reset flag.
- ◆ EPFI : Enable power-fail interrupt.
- ◆ PFI : Power-fail interrupt flag.
- ◆ WDIF : Watchdog timer interrupt flag.
- ◆ WTRF : Watchdog timer reset flag.
- ◆ EWT : Watchdog timer reset enable.
- ◆ RWT : Restart watchdog tier.

■ **P7PUP** (D9h) : Port 7 Pull-up Control Register

P7PUP.7	P7PUP.6	P7PUP.5	P7PUP.4	P7PUP.3	P7PUP.2	P7PUP.1	P7PUP.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- ◆ 1 = Pull-up resistor ON (Default) / 0 = Pull-up resistor OFF

■ **C1CAP0H** (DAh) : High Capture/Compare Register of PCA1 MODULE0

C1CAP0H.7	C1CAP0H.6	C1CAP0H.5	C1CAP0H.4	C1CAP0H.3	C1CAP0H.2	C1CAP0H.1	C1CAP0H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP1H** (DBh) : High Capture/Compare Register of PCA1 MODULE1

C1CAP1H.7	C1CAP1H.6	C1CAP1H.5	C1CAP1H.4	C1CAP1H.3	C1CAP1H.2	C1CAP1H.1	C1CAP1H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP2H** (DCh) : High Capture/Compare Register of PCA1 MODULE2

C1CAP2H.7	C1CAP2H.6	C1CAP2H.5	C1CAP2H.4	C1CAP2H.3	C1CAP2H.2	C1CAP2H.1	C1CAP2H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP3H** (DDh) : High Capture/Compare Register of PCA1 MODULE3

C1CAP3H.7	C1CAP3H.6	C1CAP3H.5	C1CAP3H.4	C1CAP3H.3	C1CAP3H.2	C1CAP3H.1	C1CAP3H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP4H** (DEh) : High Capture/Compare Register of PCA1 MODULE4

C1CAP4H.7	C1CAP4H.6	C1CAP4H.5	C1CAP4H.4	C1CAP4H.3	C1CAP4H.2	C1CAP4H.1	C1CAP4H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAP5H** (DFh) : High Capture/Compare Register of PCA1 MODULE5

C1CAP5H.7	C1CAP5H.6	C1CAP5H.5	C1CAP5H.4	C1CAP5H.3	C1CAP5H.2	C1CAP5H.1	C1CAP5H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **ACC** (E0h) : Accumulator

ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **P8PUP** (E1h) : Port 8 Pull-up Control Register

P8PUP.7	P8PUP.6	P8PUP.5	P8PUP.4	P8PUP.3	P8PUP.2	P8PUP.1	P8PUP.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

◆ 1 = Pull-up resistor ON (Default) / 0 = Pull-up resistor OFF

■ **C1CAPM0** (E2h) : Mode Control Register of PCA1 MODULE0

IPWM0	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ IPWM0 : Inverted PWM output.
  If this bit is set, the PWM output is high when C1L ≥ C1CAPmL.
  The change of this bit will take effect from the next overflow / match time of PWM.
- ◆ ECOM0 : Enable comparator.
  ECOM0 = 1 enables the comparator function.
- ◆ CAPP0 : Capture positive.
  CAPP0 = 1 enables positive edge capture.
- ◆ CAPN0 : Capture negative.
  CAPN0 = 1 enables negative edge capture.
- ◆ MAT0 : Match.
  When MAT0 = 1, a match of the PCA counter with this module's comparator/capture register causes the CCF0 bit in C1CON to be set, flagging an interrupt.
- ◆ TOG0 : Toggle.
  When TOG0 = 1, a match of the PCA counter with this module's comparator/capture register causes the C0EX0 pin to toggle.
- ◆ PWM0 : Pulse width modulation mode.
  PWM0 = 1 enables the C0EX0 pin to be used as a pulse width modulated output.
- ◆ ECCF0 : Enable CCF interrupt.
  Enables compare/capture flag CCF0 in the C1CON register to generate an interrupt.

■ **C1CAPM1** (E3h) : Mode Control Register of PCA1 MODULE1

IPWM1	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAPM2** (E4h) : Mode Control Register of PCA1 MODULE2

IPWM2	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAPM3** (E5h) : Mode Control Register of PCA1 MODULE3

IPWM3	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAPM4** (E6h) : Mode Control Register of PCA1 MODULE4

IPWM4	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1CAPM5** (E7h) : Mode Control Register of PCA1 MODULE5

IPWM5	ECOM5	CAPP5	CAPN5	MAT5	TOG5	PWM5	ECCF5
R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **EIE** (E8h) : Extended Interrupt Enable Register

EPCA1	EPCA0	ES1	EWDT	EX5	EX4	EX3	EX2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ EPCA1 : PCA1 interrupt enable
- ◆ EPCA0 : PCA0 interrupt enable
- ◆ ES1 : UART1 interrupt enable
- ◆ EWDT : Watchdog timer interrupt enable
- ◆ EX5 : External interrupt 5 enable.
- ◆ EX4 : External interrupt 4 enable.
- ◆ EX3 : External interrupt 3 enable.
- ◆ EX2 : External interrupt 2 enable.

■ **P9PUP** (E9h) : Port 9 Pull-up Control Register

P9PUP.7	P9PUP.6	P9PUP.5	P9PUP.4	P9PUP.3	P9PUP.2	P9PUP.1	P9PUP.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- ◆ 1 = Pull-up resistor ON (Default) / 0 = Pull-up resistor OFF

■ **C1L** (EAh) : Low Byte Register of PCA1 Counter

C1L.7	C1L.6	C1L.5	C1L.4	C1L.3	C1L.2	C1L.1	C1L.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **C1H** (EBh) : High Byte Register of PCA1 Counter

C1H.7	C1H.6	C1H.5	C1H.4	C1H.3	C1H.2	C1H.1	C1H.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **ADCHEN** (ECh) : ADC Input Channel Enable Register

ADCHEN.7	ADCHEN.6	ADCHEN.5	ADCHEN.4	ADCHEN.3	ADCHEN.2	ADCHEN.1	ADCHEN.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **ADCSEL** (EDh) : ADC Clock and MUX Selection Register

ADIV2	ADIV1	ADIV0	-	-	ADCS2	ADCS1	ADCS0
R/W(0)	R/W(0)	R/W(0)			R/W(0)	R/W(0)	R/W(0)

- ◆ ADIV2, ADIV1, ADIV0 : ADC input clock divide.
  [0,0,0] : 2-divide (F_{OSC}/2)
  [0,0,1] : 4-divide (F_{OSC}/4)
  [0,1,0] : 8-divide (F_{OSC}/8)
  [0,1,1] : 16-divide (F_{OSC}/16)
  [1,0,0] : 32-divide (F_{OSC}/32)
- ◆ ADCS2, ADCS1, ADCS0 : ADC active channel MUX selection.
  The channel N among the eight. ADC channels will be transferred to ADC if ADCS[2:0] = N.
  [0,0,0] : ADC0 input channel.
  [0,0,1] : ADC1 input channel.
  [0,1,0] : ADC2 input channel.
  [0,1,1] : ADC3 input channel.
  [1,0,0] : ADC4 input channel.
  [1,0,1] : ADC5 input channel.
  [1,1,0] : ADC6 input channel.
  [1,1,1] : ADC7 input channel.

■ **ADCR** (EEh) : ADC Result High Register : Value[9:2]

SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **ADCON** (EFh) : ADC Control & ADC Result Low Register : Value[1:0]

AD_EN	AD_REQ	AD_END	ADCF	-	-	SAR1	SAR0
R/W(0)	R/W(0)	R(1)	R/W(0)			R/W(0)	R/W(0)

- ◆ AD_EN : ADC enable.
  If reset, ADC is in stand-by mode.
  Set or cleared by S/W.
- ◆ AD_REQ : Request AD conversion at current channel.
  Set by S/W and Cleared by H/W when AD_END transition from low to high.
- ◆ AD_END : Current ADC status.
  0 = ADC is running now.
- ◆ ADCF : ADC interrupt flag.
  Must be cleared by S/W.
- ◆ SAR1, SAR0 : LSB's of ADC result value.

■ **B** (F0h) : Second Accumulator

B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

■ **FAEN** (F7h) : IAP Routine Access Enable Register

-	-	-	-	-	-	-	FLASH_AEN
							R/W(0)

- ◆ FLASH_AEN : IAP routine access enable.

■ **EIP** (F8h) : Extended Interrupt Priority Register

PPCA1	PPCA0	PS1	PWDT	RX5	PX4	PX3	PX2
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- ◆ PPCA1 : PCA1 interrupt priority bit.
- ◆ PPCA0 : PCA0 interrupt priority bit.
- ◆ PS1 : UART1 interrupt priority bit.
- ◆ PWDT : Watchdog timer interrupt priority bit.
- ◆ PX5 : External interrupt 5 priority bit.
- ◆ PX4 : External interrupt 4 priority bit.
- ◆ PX3 : External interrupt 3 priority bit.
- ◆ PX2 : External interrupt 2 priority bit.

Appendix C : Update History

- V1.2
  - ✓ Page 2, 3, 7, 9, 11~15, 65, 71~73
    - PWM Contents Update
  - ✓ Page 7, 11, 12, 16, 17, 96
    - 44-TQFP → 44-MQFP (Package Replacement)
  - ✓ Page 7, 13, 18, 97
    - 64-SPDIP → 64-PDIP (Package Name Modification)
  - ✓ Page 10
    - Current Spec. Update
  - ✓ Page 76, 77
    - Table & Block Diagram Modification for LVD
  - ✓ Page 86
    - 1 sector (128 bytes) → (256 bytes)
  - ✓ Page 103
    - Slide Inserted : Appendix A Description inserted
    - Title Renumbering : Appendix A
- V1.4
  - ✓ Remove 44-pin G-type
  - ✓ Changing temperature specification
    - 0 °C to +70 °C → -20 °C to +85 °C
  - ✓ Describe the constraint of power slope
- V1.5
  - ✓ Active Current : 32mA → 30mA
  - ✓ Update Product Overviews slide
  - ✓ Update I/O Ports slide
  - ✓ Update the Power Management slide
    - Add on wake-up time
  - ✓ Update the IAP slide.
  - ✓ Update the Product Numbering System
  - ✓ Change a Package Type
    - 64–TQFP → 64-LQFP
- V1.6
  - ✓ Change a Package Type
    - Remove 80-TQFP
    - Add 64-TQFP
- V1.7
  - ✓ Add on the Power Slope slide
  - ✓ Update ISP Connection slide
  - ✓ Update Port Configuration slide
- V1.8
  - ✓ Add description about NC pins of 44-MQFP pkg.