

# INTEGRATED CIRCUITS FROM MOTOROLA



MC830 Series (0 to +75°C) MC930 Series (-55 to +125°) ISSUE A

#### **MAXIMUM RATINGS**

Rating	Value	Unit
Supply Voltage —		Vdc
Operating	4.5 to 5.5	
Continuous	8.0	
Pulsed, < 1 second	12	
Output Current (Into Outputs with		mAdc
Outputs Low)		
Buffers, Power Gates — Continuous	100	
Pulsed, < 30 ms	300	
All other types — Continuous	30	
Pulsed, < 30 ms	90	
Input Forward Current -		mAdc
Continuous	-10	
Pulsed, < 30 ms	-30	
or		
Negative Voltage at Input		Vdc
Continuous	~0.5	
Pulsed, < 30 ms	-1.5	
Input Reverse Current	1.0	mAdc
or		
Positive Voltage at Diode Input	5.5	Vdc
Operating Temperature Range		°c
MC930 Series	-55 to +125	
MC830 Series	0 to +75	
Storage Temperature Range		°c
Metal Can, Ceramic Package	-65 to +150	
Plastic Package	-55 to +125	
Maximum Junction Temperature		°c
MC930 Series	175	
MC830 Series	150	L

MDTL integrated circuits provide an excellent balance of sceed power dissipation, and noise immunity for general purpose digital applications. The line includes many multifunction types, Accitional logic power is provided by the "wired OR" capability of the basic MDTL gate.



G SUFFIX METAL PACKAGE CASE 603-02 TO-100



P SUFFIX PLASTIC PACKAGE CASE 646



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



FUNCTIONS AND CHARACTERISTICS (V<sub>CC</sub> = 5.0 Vdc, T<sub>A</sub> = 25°C)

Function	Type ① 0 to +75°C	Case	Type ① -55 to +125 <sup>o</sup> C	Case	Loading Factor Each Output	Propaga- tion Delay ns typ	Power Dissipation mW typ/pkg
Expandable Dual 4-Input NAND Gate	MC830	607,632,646	MC930	607,632	8	30	22
Expandable Dual 3-2 Input NAND Gate	MC830	603	мс930	603	8	30	22
Expandable Dual 4-Input Buffer	MC832	607,632,646	MC932	607,632	25	35	85
Expandable Dual 3-2 Input Buffer	MC832	603	MC932	603	25	35	85
Qual 4 Input Expander	MC833	607,632,646	MC933	607,632	-	-	-
Dual 4-Input Expander	MC833	603	MC933	603	_	-	-
Hex Inverter	MC834	607,632,646	MC934	607,632	8	30	66
Hex Inverter  Hex Inverter (without output resistors)	MC835	607,632,646	MC935	607,632	8	30	42 66
Hex Inverter	MC836	607,632,646	MC936	607,632	8	30	
	MC837	607,632,646	MC937	607,632	7	25	90 150
Hex Inverter	MC838	607,632,646	MC938	607,632	8	30 MHz 3	150
Decade Counter Divide-by-Sixteen Counter	MC839	607,632,646	MC939	607,632	8	30 MHz 3	66
Hex Inverter (without input diodes)	MC840	607,632,646	MC940	607,632	8	30	90
Hex Inverter (without output resistors and input diodes)	MC841	607,632,646	MC941	607,632	8	30	42
		607,632,646	MC944	607,632	27	30	65
Expandable Dual 4-Input Power Gate	MC844	603	MC944	603	27	30	65
Expandable Dual 3-2 Input Power Gate	MC844		MC945	603,607,632	12/10 ②	40	60
Clocked Flip-Flop	MC845	603,607,632,646	MC945 MC946	607,632	8	30	44
Quad 2-Input NAND Gate	MC846	607,632,646	MC946	607,632	L		
	MC846	603	MC946	603	8	30	44
Quad Inverter	MC847	607,632,646	MC947	607,632	-	-	·
Quad 2-Input Gate Expander	MC848	603,607,632,646	MC948	603,607,632	11/9 ②	40	70
Clocked Flip-Flop	MC849	607,632,646	MC949	607,632	7	25	- 66
Quad 2-Input NAND Gate (2 k pullup resistor)	MC849	603	MC949	603	7	25	60
Quad Inverter (2 k pullup resistor)	MC850	603.607.632,646	MC950	603,607,632	10/8 ②		50
Pulse Triggered Binary Monostable Multivibrator	MC851	603,607,632,646	MC951	603,607,632	10	40	30
Dual J-K Flip-Flop (common clock and C <sub>D</sub> , separate S <sub>D</sub> )	MC852	607,632,646	MC952	607,632	12/10 ②	! 40	120
Dual J-K Flip-Flop (separate clock and SD, no CD)	MC853	607,632,646	мс953	607,632	12/10 2	40	120

1 F suffix denotes Ceramic Flat Package, G suffix denotes Metal Can, L suffix denotes Dual in-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package. (i.e., MC830G = Metal Can, MC830F = Flat Package, MC830L = Dual In-Line Ceramic Package. MC830P = Plastic Package)

(2) Fan-out for MC830 series type/Fan-out for MC930 series type.

3 Counting frequency.

7

# MDTL LOGIC DIAGRAMS



# MDTL (continued)

Function	Type ① 0 to +75°C	Case	Type ① -55 to +125°C	Case	Loading Factor Each Output	Propaga- tion Delay ns typ	Power Dissipation mW typ/pkg
Dual J-K Flip-Flop (common clock and CD,					<del></del>		-
separate S <sub>D</sub> , 2 k pullup resistor)	MC855	607,632,646	MC955	607,632	11/9 ②	40	140
Dual J.K Flip-Flop (separate clock and SD,			İ .				
no CD, 2 k pullup resistor)	MC856	607,632,646	MC956	607,632	11/9 ②	40	140
Quad 2-Input Buffer	MC857	607,632,646	MC957	607,632	25	35	170
Quad 2-Input NAND Power Gate	MC858	607,632,646	MC958	607,632	27	30	130
Expandable Dual 4-Input NAND Gate	1						
(2 k pullup resistor)	MC861	607,632,646	MC961	607,632	7	25	33
Expandable Dual 3-2 Input NAND Gate			†	· · · · · · · · · · · · · · · · · · ·	<del> </del>		
(2 k pullup resistor)	MC861	603	MC961	603	7	25	33
Triple 3-Input NAND Gate	MC862	607,632,646	MC962	607,632	8	25 30	33 33
Dual 2-Input NAND Gate plus Inverter	MC862	603	MC962	603	8	30	
Triple 3-Input NAND Gate (2 k pullup				000	"	30	30
resistor)	MC863	607,632,646	MC963	607,632	7	25	50
Dual 2-Input NAND Gate plus Inverter					<del>                                     </del>		30
(2 k pullup resistor)	MC863	603	MC963	603	7	25	45
Dual 5 Input NAND Gate (6K pullup resistor)	MC1800	607,632,646	MC1900	607,632	g ,	30	45 22
Dual 5-Input NAND Gate (2k pullup resistor)	MC1801	607,632,646	MC1901	607,632	7	25	33
Expandable 8-Input NAND Gate	MC1802	607,632,646	MC1902	607,632	8	30	11
Expandable 8-Input NAND Gate			<del></del>				<del></del> -
(2 k pullup resistor)	MC1803	607,632,646	MC1903	607,632	7	25	
10 Input NAND Gate	MC1804	607,632,646	MC1904	607,632	8	25 30	16.5
10-Input NAND Gate (2k pullup resistor)	MC1805	607,632,646	MC1905	607,632	7	25	11
Quad 2-Input AND Gate	MC1806	607,632,646	MC1906	607,632	8	25 35	16.5
Quad 2-Input AND Gate (2k pullup resistor)	MC1807	607,632,646	MC1907	· — · · · — —			72
Quad 2-Input OR Gate	MC1808	607,632,646	MC1907	607,632	7	30	85
Quad 2-Input OR Gate (2k pullup resistor)	MC1809	607,632,646	MC1908	607,632	8	35	97
Quad 2-Input NOR Gate	MC1810	607,632,646	MC1910	607,632	7	30	115
Quad 2-Input NOR Gate (2k pullup resistor)	MC1811	607,632,646	MC1911	607,632	8	30	60
Quad 2-Input Exclusive OR Gate				607,632	7	25	72
Quad Latch	MC1812 MC1813	607,632,646	MC1912	607,632	8	40	120
Quad Latch	MC1813 MC1814	620,648		_	7	35	220
Parallel Gated Clocked Flip-Flop		607,632,646	MC1914	607,632	7	35	220
Parallel Gated Clocked Flip-Flop	MC1815	607,632,646	MC1915	607,632	12/10 ②	40	65
Quad 2-Input NAND Gate (without	MC1816	607,632,646	MC1916	607,632	11/9 ②	40	75
output resistor)	MC1010					- 1	
High Voltage Hex Inverter	MC1818	607,632,646	MC1918	607,632	8	30	32
ngn voltage nex inverter	MC1820	632,646	- 1	-	7	40	42

F suffix denotes Ceramic Flat Package, G suffix denotes Metal Can, L suffix denotes Dual in-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, (i.e., MC830G = Metal Can, MC830F = Flat Package, MC830L = Dual In-Line Ceramic Package, MC830P = Plastic Package)

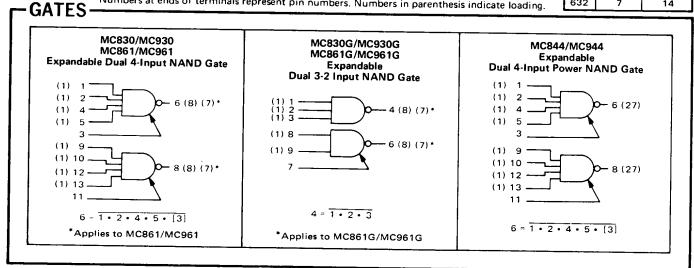
\*Unless otherwise noted

2 Fan-out for MC830 series type/Fan-out for MC930 series type.

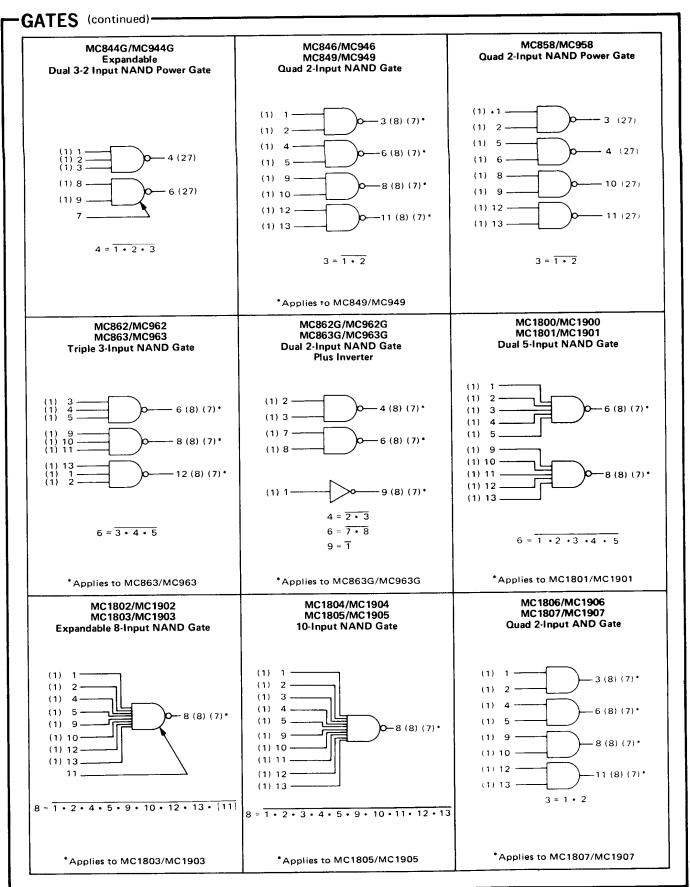
3 Counting frequency.

Case	Gnd* Pin No.	V <sub>CC</sub> * Pin No.
603	5	10
646	7	14
607	7	14
648	8	16
620	8	16
000		

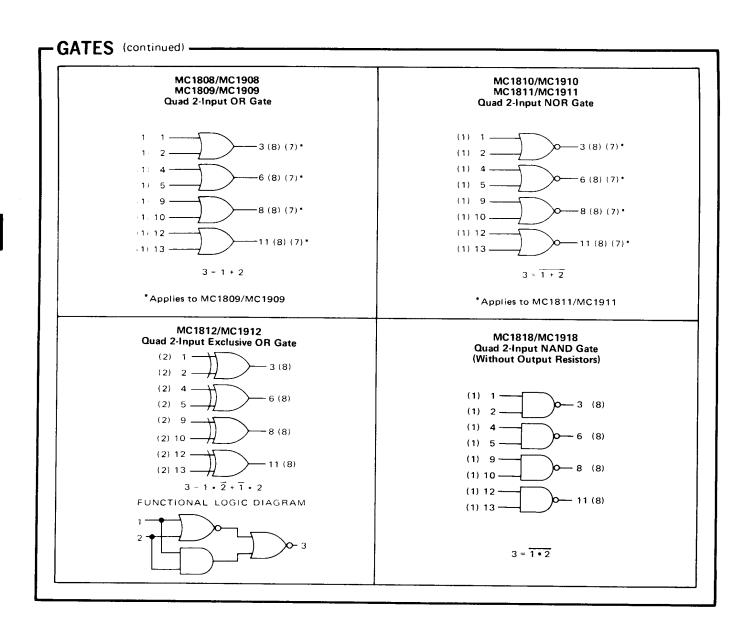
Numbers at ends of terminals represent pin numbers. Numbers in parenthesis indicate loading.

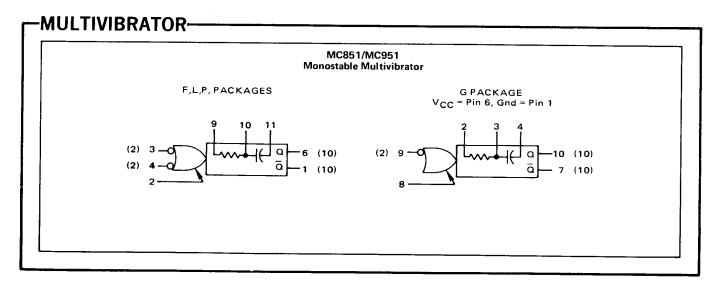


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(continued)



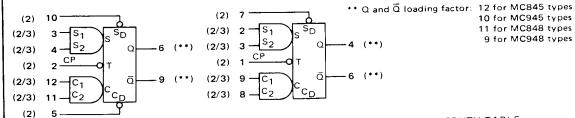


## -FLIP-FLOPS

#### MC845/MC945 MC848/MC948 Clocked Flip-Flop

#### F,L, & P PACKAGES

#### G PACKAGES



## SYNCHRONOUS TRUTH TABLE

	t <sub>n</sub>					
Sı	S <sub>2</sub>	C.	<b>C</b> 2	Q		
0	X	0	Х	Qn		
0	Х	Х	0	Qn		
X	0	0	Х	Qn		
X	0	Х	0	Q <sub>n</sub>		
0	X	1	1	0		
X	0	1	1	0		
1	1	0	Х	1		
1	1	X	0	1		
	1	1	1	U		

- 0 Low State (more negative)
- 1 High State (more positive)
- $\mathbf{X} = \mathbf{State}$  of the input does not affect the state of the
- circuit.
- U -- Indeterminate State

## J-K TRUTH TABLE (Connect S2 to Q, C2 to Q)

10 for MC945 types

11 for MC848 types

9 for MC948 types

t,	t <sub>n</sub>		
S.	C	a	
0	0	Q.	
1	0	1	
0	1	0	
1	1	Q٠	

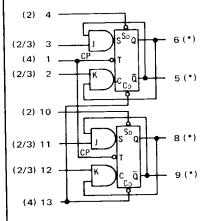
#### ASYNCHRONOUS TRUTH TABLE

So	Co	Q	ā
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

Asynchronous inputs, direct set (So and direct clear (Co), override the synchronous inputs; they are independent of all other inputs.

# MC852/MC952 MC855/MC955





 ${}^{ullet} {\bf Q}$  and  $\overline{\bf Q}$  loading factor:

12 - MC852

10 - MC952 11 - MC855

9 - MC955

### ASYNCHRONOUS TRUTH TABLE MC952/MC852 and MC955/MC855

So	<b>C</b> D	Q	ā
1	1	NC	NC
0	1	1	0
1	0	0	1
Ū	0	1	1

# ASYNCHRONOUS TRUTH TABLE MC953/MC853 and MC956/MC856

MC953/MC855 and Mc5569/MC855							
<b>S</b> D	Q	Q					
1	NC	NC					
0	1	0					

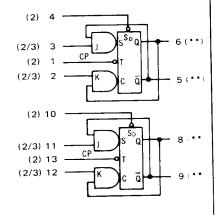
Asynchronous inputs, direct set (So) and direct clear (CD), override the synchronous inputs: they are independent of all other inputs.

# J-K TRUTH TABLE All Types

t,	t <sub>n</sub>		
J	K	Q	
0	0	Qn	
1	0	1	
0	1	0	
1	1	Q <sub>n</sub>	

J & K inputs must not change while clock is high.

# MC853/MC953 MC856/MC956 Dual J-K Flip-Flop



\*\*Q and  $\overline{\mathbf{Q}}$  loading factor

12 - MC853

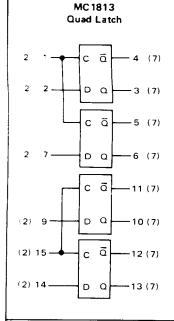
10 - MC953

11 - MC856 9 - MC956

toont nued

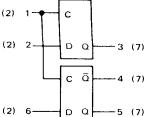
# MDTL LOGIC DIAGRAMS

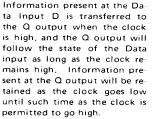




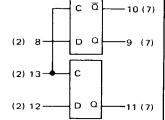
# FUNCTIONAL LOGIC DIAGRAM

# MC1814/MC1914 **Quad Latch**



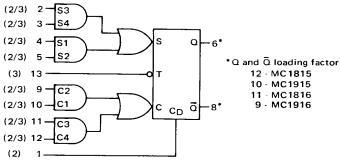


TRUTH TABLE tn tn+1 <u>a</u>• D Q 1 0 0 0 1



\*As applicable (see loading diagram)

#### MC1815/MC1915 MC1816/MC1916 Parallel Gated Clocked Flip-Flop



### SYNCHRONOUS TRUTH TABLE

	t <sub>n</sub>								t <sub>n+1</sub>
CD	СЗ	C4	C1	C2	S3	S4	S1	S2	Q
1	0	0	0	0	0	0	0	0	an
1	1	1	0	0	0	0	0	0	o o
1	0	0	1	1	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0
1	0	0	0	0	1	1	0	0	1
1	1	1	0	0	1	1	0	0	U
1	0	0	1	1	1	1	0	0	U
1	1	1	1	1	1	1	0	0	U
1	0	0	0	0	0	0	1	1	1
1	1	1	0	0	0	0	1	1	U
. 1	0	0	1	1	0	0	1	1	U
. 1	1	1	1	1	0	0	1	1	U
1	0	0	0	0	1	1	1	1	1
1	1	1	0	0	1	1	1	1	U
. 1 }	0	0	1	1	1	1	1	1	U
1	1	1	1	1	1	1	1	1	U

0 - Low State (more negative)

- High State (more positive)

NC - No Change

U - Indeterminate State

#### J-K TRUTH TABLE (Connect S2 and S4 to Q, C2 and C4 to Q)

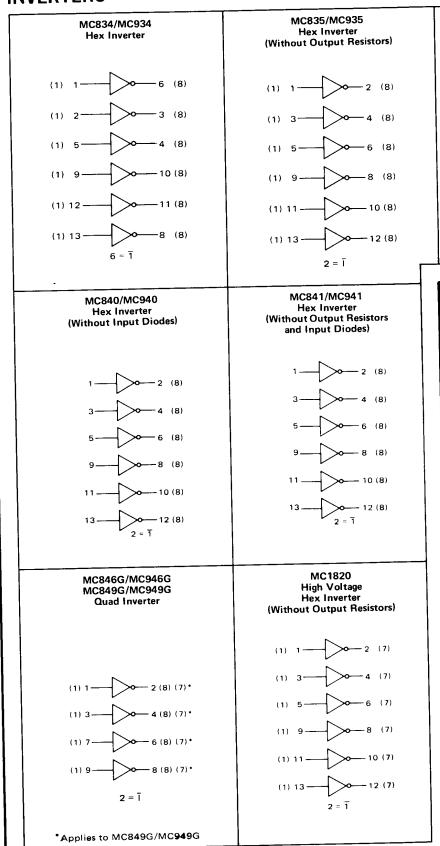
	t <sub>n</sub>						
S1	S3	C1	C3	Q			
0	0	0	0	Qn			
1	1	0	0	1			
0	0	1	1	0			
1	1	1	1	ān			

### **ASYNCHRONOUS** TRUTH TABLE

c <sub>D</sub>	Q	ā	
1	NC	NC	
0	0	1	

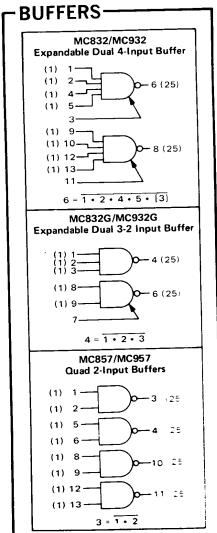
Asynchronous input, direct clear (CD), overrides the synchronous inputs. Clocked operation will occur only when CD is in the High State.

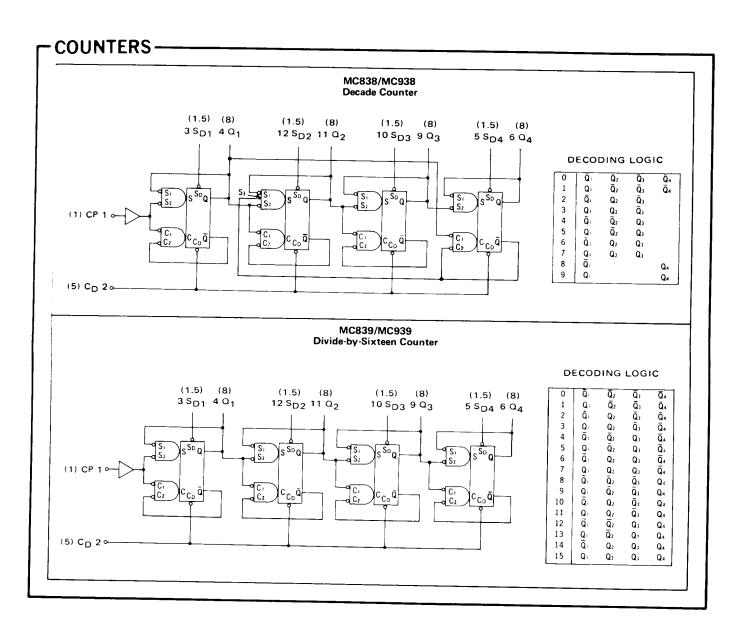
# INVERTERS

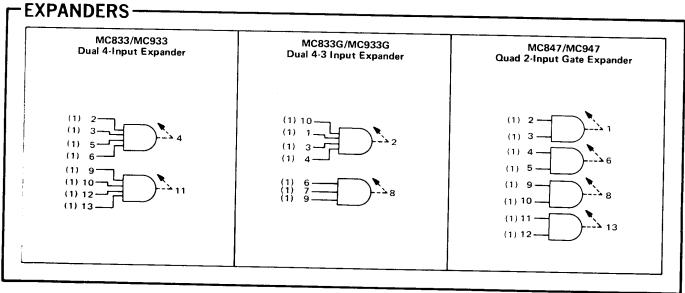


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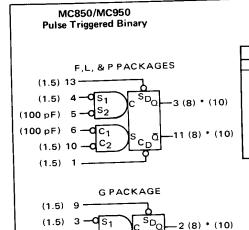
\*Applies to MC837/MC937







# -PULSE TRIGGERED BINARY-



#### SYNCHRONOUS TRUTH TABLE

t₁				<b>t</b> n+1
Sı	Sı	Ç,	C2	Q
0	0	0	0	U
1	χ	1	X	Qn
X	1	Х	1	Qn
0	1	1	0	Qn
0	0	Х	1	1
0	0	1	X	1
1	x	0	0	0
X	1	0	0	0

# ASYNCHRONOUS TRUTH TABLE

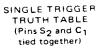
TRUTH TABLE				
SD	Съ	Q	ā	
1	1	NC	NC	
0 '	1	1	0	
1	0	0	1	
0	0	1	1	
<u> </u>				

0 = low state (more negative)1 = high state (more positive)

X = don't care

U = indeterminate state

NC = no change



	t <sub>n</sub>	t
S.	Cz	Q
0	0	U
1	0	0
0	1	1
1	1	Q-

G PACKAGE
(1.5) 9
$(1.5)  3 - 9 \\ S_1  C \\ S_{DQ} - 2 (8) \cdot (10)$
(100 pF) 4 -dS2
(100 pF) 5 -QC <sub>1</sub> S 5 -8 (8) * (10)
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$
(1.5) 1 G Pkg: V <sub>CC</sub> = Pin 10, Gnd = Pin 6
*Applies to MC950