

MPC5561 Microcontroller Product Brief

The MPC5561 32-bit embedded controller is designed for advanced driver assistance systems with Radar, CMOS imaging, Lidar and ultrasonic sensors in automotive and high temperature industrial applications. A member of Freescale Semiconductor's MPC5500 Family, it contains the Book E compliant Power Architecture™ technology core with Variable Length Encoding (VLE). This core complies with the Power Architecture embedded category, and is 100 percent user mode compatible with the original Power PC™ user instruction set architecture (UISA). It offers system performance up to five times that of its MPC500 predecessors, while bringing you the reliability and familiarity of the proven Power Architecture technology.

A comprehensive suite of hardware and software development tools is available to help simplify and speed system design. Development support is available from leading tools vendors providing compilers, debuggers and simulation development environments.

This document provides an overview of the MPC5561 microcontroller features, including the major functional components.

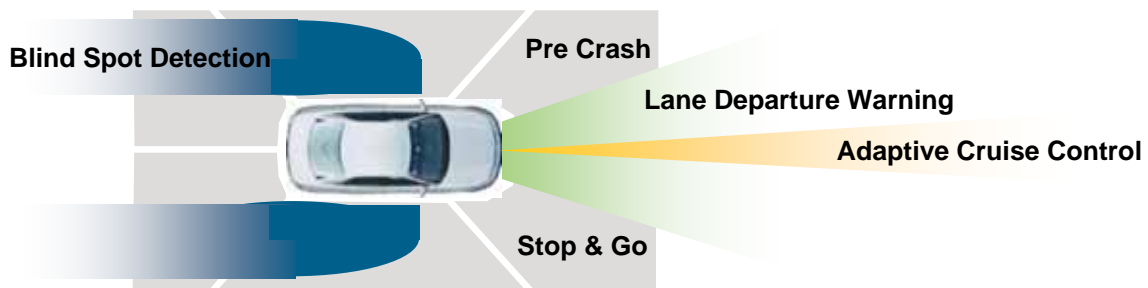
Contents

1	Applications	2
2	Features	3
2.1	MPC5500 Family Comparison	3
2.2	Block Diagram	5
2.3	Operating Parameters	6
2.4	Packages	6
2.5	Chip Level Features	6
2.6	Module Features	7
3	Developer Environment	13
4	Document Revision History	14

1 Applications

MPC5561 is ideal for driver assistance systems incorporating image sensors and radar technology:

Application	Description	Sensor
Adaptive Cruise Control	Automatically controls the speed of a vehicle with awareness of other vehicles and obstacles.	Radar Lidar Camera
Pre-Crash	Detects an imminent collision and prepares on-board safety systems in advance.	Radar Lidar Camera
Blind Spot Detection	Alerts the driver to the presence of vehicles in the blind spot when the driver is preparing to change lanes.	Radar Lidar Camera Ultrasonic
Backup/Reversing Warning	Detects the presence of obstructions behind the vehicle and provides the driver with proximity information and imminent collision warning.	Radar Camera Ultrasonic
Active Front Lighting	Improves driver's visibility at night by dynamically altering the direction and intensity of the headlight beams.	Camera (Low)
Chassis Management	Monitors load distribution and adjusts chassis setup to maintain optimum performance.	
Occupant Detection	Detects the presence of the driver and passengers and adjusts the in-car environment accordingly.	
Driver Alertness	Monitors the alertness of the driver and warns the driver when necessary.	Camera



2 Features

2.1 MPC5500 Family Comparison

Table 1. MPC5500 Family Members

MPC5500 Device	MPC5533	MPC5534	MPC5553	MPC5554	MPC5561	MPC5565	MPC5566	MPC5567
Power Core	e200z3	e200z3	e200z6	e200z6	e200z6	e200z6	e200z6	e200z6
Variable Length Instruction Support	Yes	Yes	No	No	Yes	Yes	Yes	Yes
Cache	None	None	8 Kbyte Unified ¹	32 Kbyte Unified ²	32 Kbyte Unified ³	8 Kbyte Unified ¹	32 Kbyte Unified ³	8 Kbyte Unified ¹
Memory Management Unit (MMU)	16 entry	16 entry	32 entry	32 entry	32 entry	32 entry	32 entry	32 entry
Crossbar	4x5	4x5	4x5	3x5	4x6	3 ⁴ x5	4x5	5x5
Core Nexus	Class 3+ (NZ3C3)	Class 3+ (NZ3C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)
SRAM	48 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	192 Kbyte	80 Kbyte	128 Kbyte	80 Kbyte
Flash	Main Array	768 Kbyte ⁵	1 Mbyte ⁵	1.5 Mbyte ⁶	2 Mbyte ⁶	1 Mbyte ⁶	2 Mbyte ⁶	3 Mbyte ⁶
	Shadow Block	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte
External Bus (EBI)	Data Bus	16-bit ⁷	16 bit ⁷	32 bit ⁷	32 bit ⁷	32-bit ⁷	32-bit ⁷	32-bit ⁷
	Address Bus	24	24	24	24	26 ⁸	26 ⁸	26 ⁸
Calibration Bus	Yes	Yes	Partial	No	Yes	Yes	Yes	Yes
Direct Memory Access (DMA)	32 channel	32 channel	32 channel	64 channel	32 channel	32 channel	64 channel	32 channel
DMA Nexus	None	None	Class 3	Class 3	Class 3	Class 3	Class 3	Class 3
Serial		1	2	2	2	4	2	2
	eSCI_A	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	eSCI_B	No	Yes	Yes	Yes	Yes	Yes	Yes
	eSCI_C	No	No	No	No	Yes	No	No
	eSCI_D	No	No	No	No	Yes	No	No
Controller Area Network (CAN)		2	2	2	3	2 ⁹	3 ⁹	4 ⁹
	CAN_A	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf
	CAN_B	No	No	No	64 buf	No	64 buf	64 buf
	CAN_C	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf
	CAN_D	No	No	No	No	No	No	64 buf
	CAN_E	No	No	No	No	No	No	No
SPI		2	3	3	4	2	3	4
	DSPI_A	No	No	No	Yes	No	No	Yes
	DSPI_B	No	Yes	Yes	Yes	Yes	Yes	Yes
	DSPI_C	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	DSPI_D	Yes	Yes	Yes	Yes	No	Yes	Yes
eMIOS	0 channel	24 channel	24 channel	24 channel	24 channel	24 channel	24 channel	24 channel

Table 1. MPC5500 Family Members (continued)

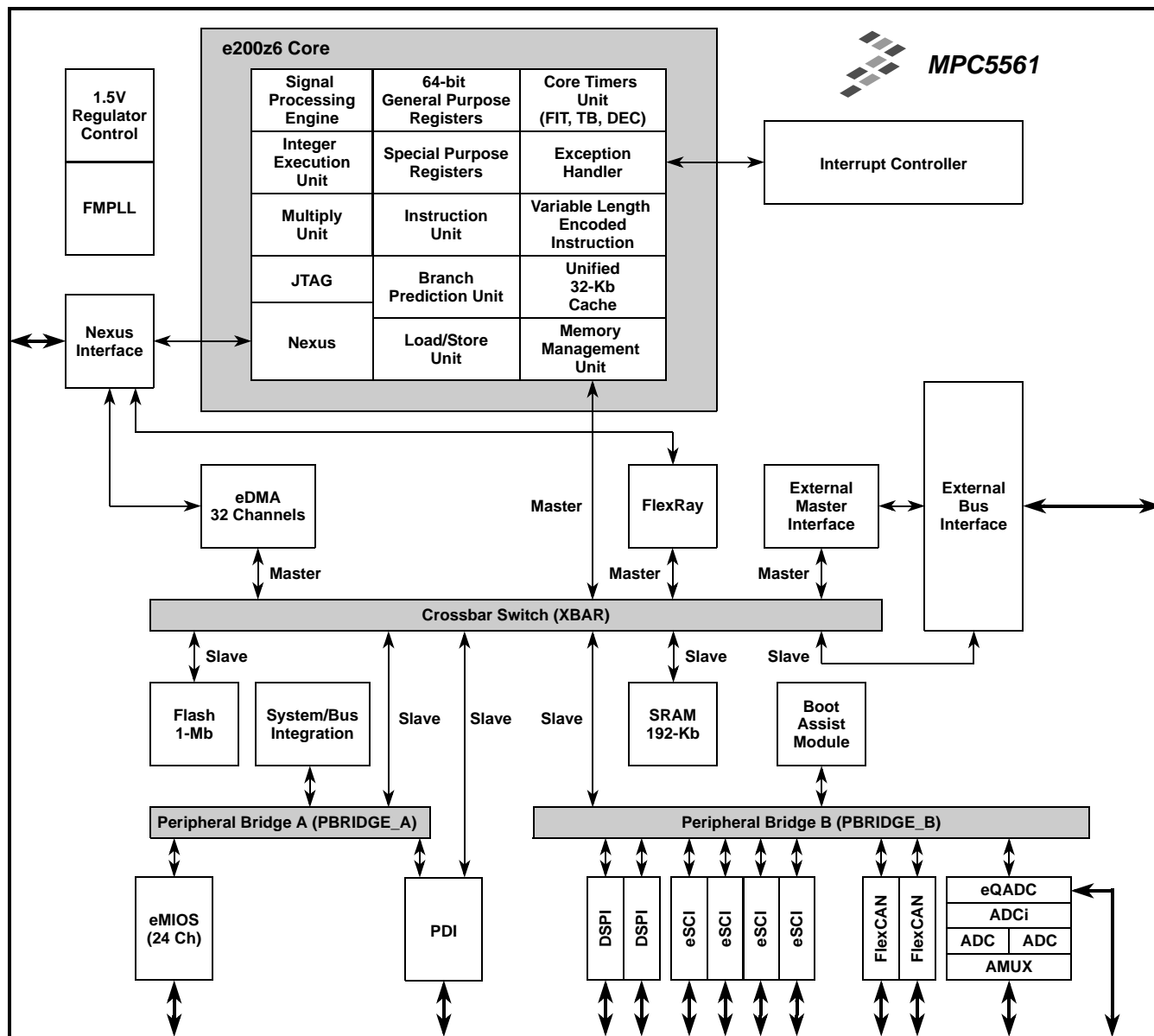
MPC5500 Device	MPC5533	MPC5534	MPC5553	MPC5554	MPC5561	MPC5565	MPC5566	MPC5567
eTPU	32 channel	32 channel	32 channel	64 channel	0 channel	32 channel	64 channel	32 channel
eTPU_A	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes
eTPU_B	No	No	No	Yes	No	No	Yes	No
Code Memory	12 Kbyte	12 Kbyte	12 Kbyte	16 Kbyte	0 Kbyte	12 Kbyte	20 Kbyte	12 Kbyte
Parameter RAM	2.5 Kbyte	2.5 Kbyte	2.5 Kbyte	3 Kbyte	0 Kbyte	2.5 Kbyte	4 Kbyte	2.5 Kbyte
Nexus	Class 3	Class 3	Class 3	Class 3	No	Class 3	Class 3	Class 3
Interrupt Controller	178 channel	210 channel	210 channel	300 channel	231 channel	231 channel	329 channel	281 channel
Analog to Digital Converter (eQADC)	40 channel	40 channel	40 channel	40 channel	40 channel	40 channel	40 channel	40 channel
ADC_0	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ADC_1	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Fast Ethernet Controller (FEC)	No	No	Yes ¹⁰	No	No	No	Yes ¹⁰	Yes ¹¹
FlexRay	No	No	No	No	Yes	No	No	Yes
FlexRay Nexus	No	No	No	No	Class 3	No	No	Class 3
Phase Lock Loop (PLL)	FM	FM	FM	FM	FM	FM	FM	FM
Maximum System Frequency ¹²	80 MHz	80 MHz	132 MHz	132 MHz	132 MHz	132 MHz	144 MHz	132 MHz
Crystal Range	8–20 MHz	8–20 MHz	8–20 MHz	8–20 MHz	8–40 MHz	8–20 MHz	8–20 MHz	8–40 MHz
Voltage Regulator Controller (VRC)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

NOTES:

- ¹ 2-way associative
- ² 8-way associative
- ³ 4-way or 8-way associative
- ⁴ The actual crossbar is implemented as a 5x5 crossbar with two unused ports
- ⁵ 16-byte flash page size for programming
- ⁶ 32-byte flash page size for programming
- ⁷ May not be externally available in some package configurations
- ⁸ Either ADDR[8:31] or ADDR[6:29] can be selected.
- ⁹ Updated FlexCAN module with optional individual receive filters
- ¹⁰ The FEC signals are shared with data bus pins DATA[16:31]
- ¹¹ The FEC signals are shared with the calibration bus
- ¹² Initial automotive temperature range qualification

2.2 Block Diagram

Figure 1 shows a top-level block diagram of the MPC5561.



LEGEND

MPC5500 Device Module Acronyms

- CAN – Controller area network (FlexCAN)
- DSPI – Deserial/serial peripheral interface
- eDMA – Enhanced direct memory access
- eMIOS – Enhanced modular I/O system
- eQADC – Enhanced queued analog/digital converter
- eSCI – Enhanced serial communications interface
- eTPU – Enhanced time processing units
- FMPLL – Frequency modulated phase-locked loop
- PDI – Parallel digital interface
- SRAM – Static RAM

e200z6 Core Component Acronyms

- DEC – Decrementer
- FIT – Fixed interval timer
- TB – Time base
- WDT – Watchdog timer

Figure 1. MPC5561 Block Diagram

2.3 Operating Parameters

- Fully static operation, up to 132 MHz
- -40° to 150° C junction temperature
- 1.5 V Core, 3.0–5.25 V I/O, 1.8–3.3 V external bus and Nexus pins

2.4 Packages

- 324-pin plastic ball grid array (TEPBGA)
- 416-pin plastic ball grid array (TEPBGA)

2.5 Chip Level Features

- Low power design
 - Less than 1.0 W power dissipation
 - Designed for dynamic power management of core and peripherals
 - Software-controlled clock gating of peripherals
 - Separate power supply for stand-by operation for portion of internal SRAM
- Fabricated in 0.13 μm process
- Single issue, 32-bit Book E compliant Power Architecture™ technology e200z6 CPU core
- 32-channel enhanced direct memory access controller (eDMA)
- Interrupt controller (INTC) capable of handling 208 selectable-priority interrupt sources
- Frequency modulated phase-locked loop (FMPLL)
- External bus interface (EBI) with error correction status module (ECSM)
- System integration unit (SIU)
- 1 MB on-chip Flash with Flash bus interface unit (FBIU)
- 192 KB on-chip static RAM
- Boot assist module (BAM)
- 24-channel enhanced modular I/O system (eMIOS)
- Two enhanced queued analog-to-digital converter (eQADC) modules
- Two deserial serial peripheral interface (DSPI) modules
- Four enhanced serial communication interface (eSCI) modules
- Two controller area network (FlexCAN) modules
- Dual channel FlexRay controller
- Parallel digital interface (PDI)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard
- Device/board test support per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator controller for regulating 3.3 V down to 1.5 V for core logic

2.6 Module Features

The following is a brief summary of the functional blocks in the MPC5561. For more detailed information, refer to the MPC5561 Reference Manual (MPC5561RM).

2.6.1 High Performance e200z6 Core Processor

- 32-bit CPU built on Power Architecture™ technology
- Freescale Variable Length Encoding (VLE) enhancements for code size footprint reduction
- Thirty-two 64-bit general-purpose registers (GPRs)
- Memory management unit (MMU) with 32-entry fully-associative translation look-aside buffer (TLB)
- Branch processing unit
- Fully pipelined load/store unit
- 32 KB unified cache with line locking
 - Four or eight-way set associative
 - Two 32-bit fetches per clock
 - Eight-entry store buffer
 - Way locking
 - Supports assigning cache as instruction or data only on a per way basis
 - Supports tag and data parity
- Vectored interrupt support
- Interrupt latency less than 70 ns @ 132 MHz (measured from interrupt request to execution of first instruction of interrupt exception handler)
- Reservation instructions for implementing read-modify-write constructs (internal SRAM and Flash)
- Signal processing engine (SPE) auxiliary processing unit (APU) operating on 64-bit general purpose registers
- Floating point
 - IEEE® 754 compatible with software wrapper
 - Single precision in hardware; double precision with software library
 - Conversion instructions between single precision floating point and fixed point
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency in the MPC5561; to reduce latency, long cycle time instructions are aborted upon interrupt requests.
- Extensive system development support through Nexus debug module

2.6.2 System Bus Crossbar Switch (XBAR)

- Four master ports, six slave ports
- 32-bit address bus, 64-bit data bus

Features

- Simultaneous accesses from different masters to different slaves (there is no clock penalty when a parked master accesses a slave)

2.6.3 Enhanced Direct Memory Access (eDMA) Controller

- 32 channels support independent 8-, 16-, 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer

2.6.4 Interrupt Controller (INTC)

- 231 total interrupt vectors
 - 208 peripheral interrupt requests¹
 - 8 software settable sources
 - 16 reserved
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resources

2.6.5 Frequency Modulated Phase-locked Loop (FMPLL)

- Input clock frequency:
 - 8 to 20 MHz
- Current controlled oscillator (ICO) range from 48 MHz to maximum device frequency
- Reduced frequency divider (RFD) for reduced frequency operation without re-lock
- Four selectable modes of operation
- Programmable frequency modulation
- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- On-chip loop filter (reduces number of external components required)
- Engineering clock output configurable to divide-by-2 to divide-by-510 of the system clock frequency or the crystal/external clock input

1. Although this device has a maximum of 231 interrupts, the logic requires that the total number of interrupts be divisible by four. Therefore, the total number of interrupts specified for this device is 232.

2.6.6 External Bus Interface (EBI)

- 1.8–3.3 V nominal I/O voltage
- 324 BGA: 16-bit data bus, 24-bit address bus is default ADDR[8:31], but configurable to 26-bit address bus.
- Memory controller with support for various memory types
 - Non-burst SDR flash and SRAM
 - Asynchronous/legacy flash and SRAM
 - Most standard memories used with the MPC5xx family
- Configurable bus speed modes
 - 50% of system frequency
 - 25% of system frequency
- Support for external master accesses to internal addresses (master/slave system only)
- Burst support
- Bus monitor
 - User selectable
 - Programmable timeout period (with eight external bus clock resolution)
- Four chip selects: $\overline{CS}[0:3]$ multiplexed with ADDR[8:11]
- Two write/byte enable ($\overline{WE}/\overline{BE}[0:1]$) signals in the 324-pin package
- Configurable wait states (via chip selects)
- Optional automatic CLKOUT gating to save power and reduce EMI
- Compatible with MPC5xx external bus (with some limitations):
Selectable drive strengths; 10 pF, 20 pF, 30 pF, 50 pF

2.6.7 System Integration Unit (SIU)

- Centralized GPIO control of bus pins:
 - 324 BGA package: 150 pins
- Centralized pad control on a per-pin basis
- System reset monitoring and generation
- External interrupt inputs, filtering and control

2.6.8 Error Correction Status Module (ECSM)

- Configurable error-correcting codes (ECC) reporting for internal SRAM and flash memories

2.6.9 On-chip Flash Memory

- 1 MB burst flash memory
- 128 KB × 64-bit configuration
- Censorship protection scheme to prevent flash content visibility

Features

- Hardware read-while-write feature that can erase/program blocks while other blocks are read (used for EEPROM emulation and data calibration)
- 12 blocks with sizes ranging from 16–128 KB to support features such as boot block, operating system block, and EEPROM emulation. Blocks are structured as follows:
 - 2 x 16 KB
 - 2 x 48 KB
 - 2 x 64 KB
 - 6 x 128 KB
- Read while write with multiple partitions
- Parallel programming mode to support rapid end of line programming
- Hardware programming state machine

2.6.10 Configurable Cache Memory, 0–32 KB

- Four-way or eight-way set-associative unified (instruction and data) cache
 - Two 32-bit fetches per clock
 - Eight-entry store buffer
 - Way locking
 - Supports assigning cache as instruction or data only on a per way basis
 - Supports tag and data parity
- Decouples processor performance from system memory performance

2.6.11 On-chip Internal Static RAM (SRAM)

- 192 KB general-purpose SRAM of which 32 KB are on standby power
- ECC performs single-bit correction, double-bit error detection

2.6.12 Boot Assist Module (BAM)

- Enables and manages the transition of MCU from reset to user code execution in the following configurations:
 - User application can boot from internal or external Flash memory
 - Download and execution of code via FlexCAN or eSCI
 - User application can boot with either classic Power Architecture code or VLE code

2.6.13 Enhanced Modular I/O System (eMIOS)

- 24 orthogonal channels with double action, PWM, and modulus counter functionality
- Supports all DASM and PWM modes of MIOS14 (MPC5xx)
- Two selectable timebases
- DMA and interrupt request support

- Motor control capability

2.6.14 Parallel Digital Interface (PDI)

- Support for external ADC and CMOS image sensors
- Interface operation up to 66 MHz (derived from ½ or ¼ of MCU system bus)
- Selectable data capture from rising or falling edge or both edges
- Receive FIFO with adjustable trigger thresholds.
- Data width for 8, 10, 12, and 16 bits.
- Data Packing Unit with Configurable data width of 16, 32, or 64.
- Binary increasing channel select that allows up to 8 channels to be selected
- Frame synchronization through Vsync, Hsync, PIXCLK or psuedo-BT.656 protocol

2.6.15 Enhanced Queued Analog/digital Converter (eQADC)

- Two independent ADCs with 12-bit A/D resolution
- Common mode conversion range of 0–5 V
- 40 single-ended input channels, expandable to 65 channels with external multiplexers
- Eight channels can be used as four pairs of differential analog input channels
- 10-bit accuracy at 400 ksamples/second; 8-bit accuracy at 800 ksamples/second
- Supports eight FIFO queues with fixed priority
- Queue modes with priority-based preemption; initiated by software command, internal (eMIOS), or external triggers
- DMA and interrupt request support
- Supports all functional modes from QADC (MPC5xx family)

2.6.16 Two Deserial Serial Peripheral Interface Modules (DSPI)

- Serial peripheral interface (SPI)
 - Full duplex communication ports with interrupt and eDMA request support
 - Supports all functional modes from QSPI submodule of QSMCM (MPC5xx family)
 - Support for queues in RAM
 - Six chip selects, expandable to 64 with external demultiplexers
 - Programmable frame size, baud rate, clock delay and clock phase on a per frame basis
 - Modified SPI mode for interfacing to peripherals with longer setup time requirements
- Deserial serial interface (DSI)
 - Pin reduction by hardware serialization and deserialization of eTPU and eMIOS channels
 - Chaining of DSI submodules
 - Triggered transfer control and change in data transfer control (for reduced EMI)

2.6.17 Four Enhanced Serial Communication Interface (eSCI) Modules

- UART mode provides NRZ format and half or full duplex interface
- eSCI bit rate up to 1 Mb/s
- Advanced error detection, and optional parity generation and detection
- Word length programmable as 8 or 9 bits
- Separately enabled transmitter and receiver
- LIN Support
- DMA support
- Interrupt request support

2.6.18 Two FlexCANs

- 64 message buffers each
- Full implementation of the CAN protocol specification, Version 2.0B
- Based on and including all existing features of the Freescale TouCAN module
- Programmable acceptance filters
- Individual RX filtering per message buffer
- Short latency time for high priority transmit messages
- Arbitration scheme according to message ID or message buffer number
- Listen only mode capabilities
- Programmable clock source: system clock or oscillator clock
- Reception queue possible by setting more than one RX message buffer with the same ID
- Backwards compatible with previous FlexCAN modules

2.6.19 Nexus Development Interface (NDI)

- Per IEEE®-ISTO 5001-2003
- Real time development support for Power Architecture core through Nexus class 3 (some class 4 support)
- Data trace of eDMA accesses
- Data trace of FlexRay accesses
- Read and write access
- Configured via the IEEE® 1149.1 (JTAG) port
- High bandwidth mode for fast message transmission
- Reduced bandwidth mode for reduced pin usage

2.6.20 IEEE® 1149.1 JTAG Controller (JTAGC)

- IEEE® 1149.1-2001 Test Access Port (TAP) interface

- JCOMP input that provides the ability to share the TAP. Selectable modes of operation include JTAGC/debug or normal system operation.
- 5-bit instruction register that supports IEEE® 1149.1-2001 defined instructions
- 5-bit instruction register that supports additional public instructions
- Three test data registers: a bypass register, a boundary scan register, and a device identification register
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

2.6.21 Dual FlexRay controller

- Full implementation of FlexRay Protocol Specification 2.1
- 128 configurable message buffers can be handled
- Message buffers configurable as TX, RX, or RXFIFO
- Message buffer size configurable
- Message filtering for all message buffers based on FrameID, cycle count and message ID
- Programmable acceptance filters for RXFIFO message buffers
- Dual channel, each at up to 10 Mbit/s data rate
- Bus guardian support for each channel

2.6.22 Voltage Regulator Controller

- Provides a low-cost solution to powering the core logic; reduces the number of power supplies required from the customer power supply chip.

2.6.23 POR Block

- Provides initial reset condition up to the voltage at which pins ($\overline{\text{RESET}}$) can be read safely; it does not guarantee the safe operation of the chip at specified minimum operating voltages.

3 Developer Environment

The MPC5500 family of MCUs supports similar tools and third party developers as other Power Architecture products, offering a widespread, established network of tools and software vendors.

The following development support is available.

- Evaluation/development boards and systems
- Emulators, simulators, and probes
- Flash programmers
- IDE/tool chains
- C/C++ compilers
- Hardware and software debuggers

Document Revision History

- Initialization/boot code generators
- Software libraries
- Device/module drivers
- C-header and equate files
- JTAG interfaces
- Code examples
- Third party real-time operating systems (RTOS)

4 Document Revision History

Table 2 provides a revision history of this document.

Table 2. Revision History

Revision	Substantive Change(s)
Rev. 0	First public release.
Rev. 1	Document completely revised.

How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MPC5561PB
Rev. 1
12/2007

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

The described product contains a PowerPC processor core. The PowerPC name is a trademark of IBM Corp. and used under license.

© Freescale Semiconductor, Inc. 2007. All rights reserved.

