Freescale Semiconductor
Data Sheet: Advance Information

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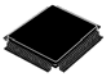
RoHS

MPC5602D



100 LQFP
14 mm x 14 mm

64 LQFP
10 mm x 10 mm

MPC5602D Microcontroller Data Sheet

- Single issue, 32-bit CPU core complex (e200z0)
  - Compliant with the Power Architecture® embedded category
  - Includes an instruction set enhancement allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Up to 256 KB on-chip Code Flash supported with Flash controller and ECC
- 64 KB on-chip Data Flash with ECC
- Up to 16 KB on-chip SRAM with ECC
- Interrupt controller (INTC) with multiple interrupt vectors, including 20 external interrupt sources and 18 external interrupt/wakeup sources
- Frequency modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, Flash, or SRAM from multiple bus masters
- Boot assist module (BAM) supports internal Flash programming via a serial link (CAN or SCI)
- Timer supports input/output channels providing a range of 16-bit input capture, output compare, and pulse width modulation functions (eMIOS-lite)
- Up to 33 channel 12-bit analog-to-digital converter (ADC)
- 2 serial peripheral interface (DSPI) modules
- 3 serial communication interface (LINFlex) modules
- 1 enhanced full CAN (FlexCAN) module with configurable buffers
- Up to 79 configurable general purpose pins supporting input and output operations (package dependent)
- Real Time Counter (RTC) with clock source from 128 kHz or 16 MHz internal RC oscillator supporting autonomous wakeup with 1 ms resolution with max timeout of 2 seconds
- Up to 4 periodic interrupt timers (PIT) with 32-bit counter resolution
- 1 System Module Timer (STM)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class 1 standard
- Device/board boundary Scan testing supported with per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator (VREG) for regulation of input supply for all internal levels

This document contains information on a new product. Specifications and information herein are subject to change without notice.

freescale semiconductor

Preliminary—Subject to Change Without Notice

Table of Contents

1 Introduction

1.1 Document overview

This document describes the device features and highlights the important electrical and physical characteristics.

1.2 Description

These 32-bit automotive microcontrollers are a family of system-on-chip (SoC) devices designed to be central to the development of the next wave of central vehicle body controller, smart junction box, front module, peripheral body, door control and seat control applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology and designed specifically for embedded applications.

The advanced and cost-efficient e200z0 host processor core of this automotive controller family complies with the Power Architecture technology and only implements the VLE (variable-length encoding) APU (auxiliary processing unit), providing improved code density. It operates at speeds of up to 48 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with the user's implementations.

The device platform has a single level of memory hierarchy and can support a wide range of on-chip static random access memory (SRAM) and internal flash memory.

Table 1. MPC5602D device comparison

Feature	Device			
	MPC5601DxLH	MPC5601DxLL	MPC5602DxLH	MPC5602DxLL
CPU	e200z0			
Execution speed	Static – up to 48 MHz			
Code Flash	128 KB		256 KB	
Data Flash	64 KB (4 × 16 KB)			
SRAM	12 KB		16 KB	
eDMA	16 ch			
ADC	16 ch, 12-bit	33 ch, 12-bit	16 ch, 12-bit	33 ch, 12-bit
CTU	16 ch			
Total timer I/O[1] eMIOS	13 ch, 16-bit	28 ch, 16-bit	13 ch, 16-bit	28 ch, 16-bit
• Type X[2]	2 ch	5 ch	2 ch	5 ch
• Type Y[3]	—	9 ch	—	9 ch
• Type G[4]	7 ch	7 ch	7 ch	7 ch
• Type H[5]	4 ch	7 ch	4 ch	7 ch
SCI (LINFlex)	3			
SPI (DSPI)	2			
CAN (FlexCAN)	1			
GPIO[6]	45	79	45	79

Table 1. MPC5602D device comparison (continued)

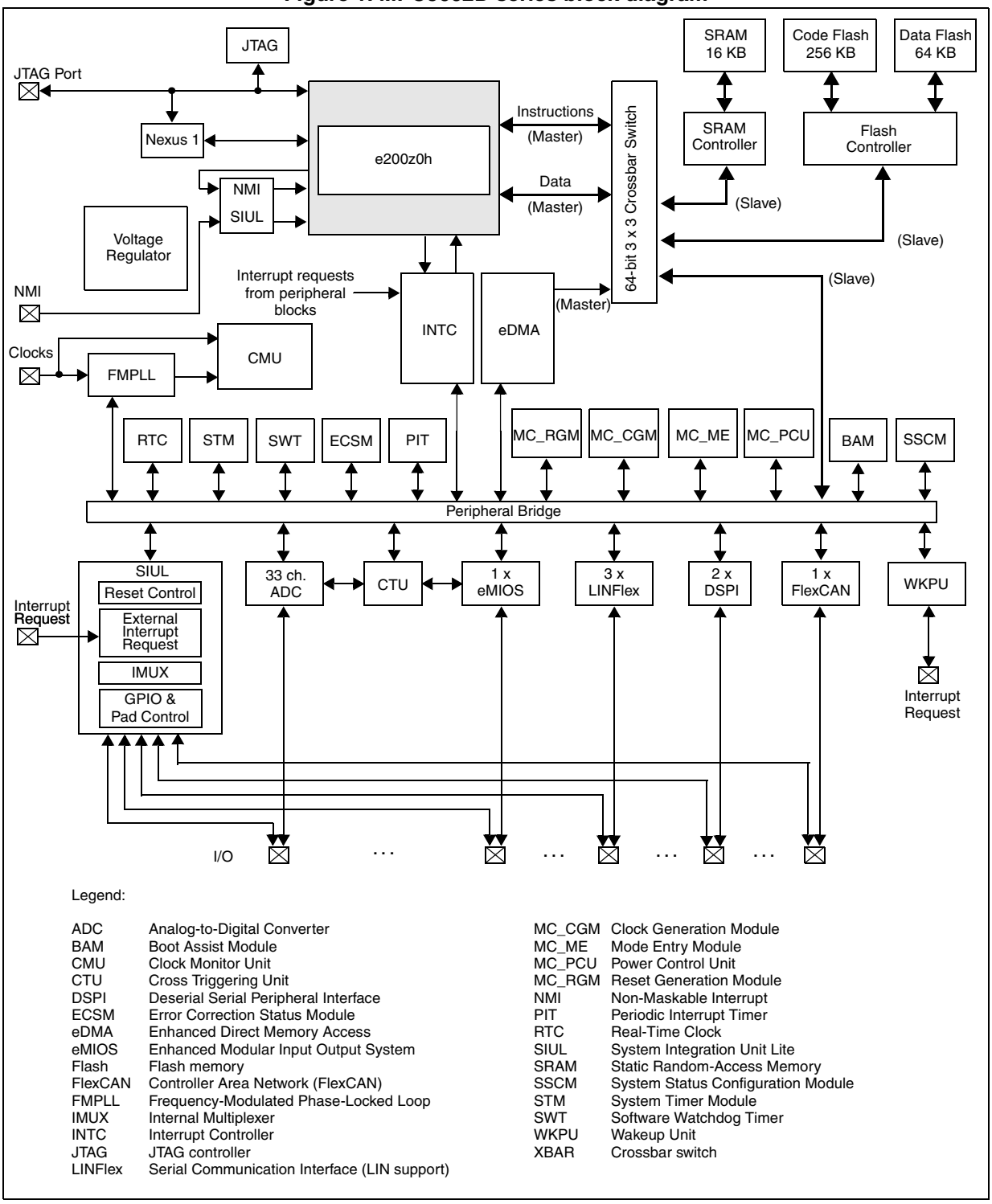
Feature	Device			
	MPC5601DxLH	MPC5601DxLL	MPC5602DxLH	MPC5602DxLL
Debug	JTAG			
Package	64 LQFP	100 LQFP	64 LQFP	100 LQFP

1 Refer to eMIOS section of device reference manual for information on the channel configuration and functions.
2 Type X = MC + MCB + OPWMT + OPWMB + OPWFMB + SAIC + SAOC
3 Type Y = OPWMT + OPWMB + SAIC + SAOC
4 Type G = MCB + IPWM + IPM + DAOC + OPWMT + OPWMB + OPWFMB + OPWMCB + SAIC + SAOC
5 Type H = IPWM + IPM + DAOC + OPWMT + OPWMB + SAIC + SAOC
6 I/O count based on multiplexing with peripherals

2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5602D device series.

Figure 1. MPC5602D series block diagram



Legend:

ADC	Analog-to-Digital Converter
BAM	Boot Assist Module
CMU	Clock Monitor Unit
CTU	Cross Triggering Unit
DSPI	Deserial Serial Peripheral Interface
ECSM	Error Correction Status Module
eDMA	Enhanced Direct Memory Access
eMIOS	Enhanced Modular Input Output System
Flash	Flash memory
FlexCAN	Controller Area Network (FlexCAN)
FMPLL	Frequency-Modulated Phase-Locked Loop
IMUX	Internal Multiplexer
INTC	Interrupt Controller
JTAG	JTAG controller
LINFlex	Serial Communication Interface (LIN support)
MC_CGM	Clock Generation Module
MC_ME	Mode Entry Module
MC_PCU	Power Control Unit
MC_RGM	Reset Generation Module
NMI	Non-Maskable Interrupt
PIT	Periodic Interrupt Timer
RTC	Real-Time Clock
SIUL	System Integration Unit Lite
SRAM	Static Random-Access Memory
SSCM	System Status Configuration Module
STM	System Timer Module
SWT	Software Watchdog Timer
WKPU	Wakeup Unit
XBAR	Crossbar switch

Table 2 summarizes the functions of all blocks present in the MPC5602D series of microcontrollers. Please note that the presence and number of blocks varies by device and package.

Table 2. MPC5602D series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 12-bit analog-to digital-converter
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Error Correction Status Module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels.
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU

Table 2. MPC5602D series block summary (continued)

Block	Function
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Non-Maskable Interrupt (NMI)	Handles external events that must produce an immediate response, such as power down detection
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Real-time counter (RTC)	Provides a free-running counter and interrupt generation capability that can be used for timekeeping applications
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup Unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.

3 Package pinouts and signal descriptions

3.1 Package pinouts

The available LQFP pinouts are provided in the following figures. For pin signal descriptions, please refer to Table 3.

Figure 2 shows the MPC5602D in the 100 LQFP package.

Figure 2. 100 LQFP pin configuration (top view)

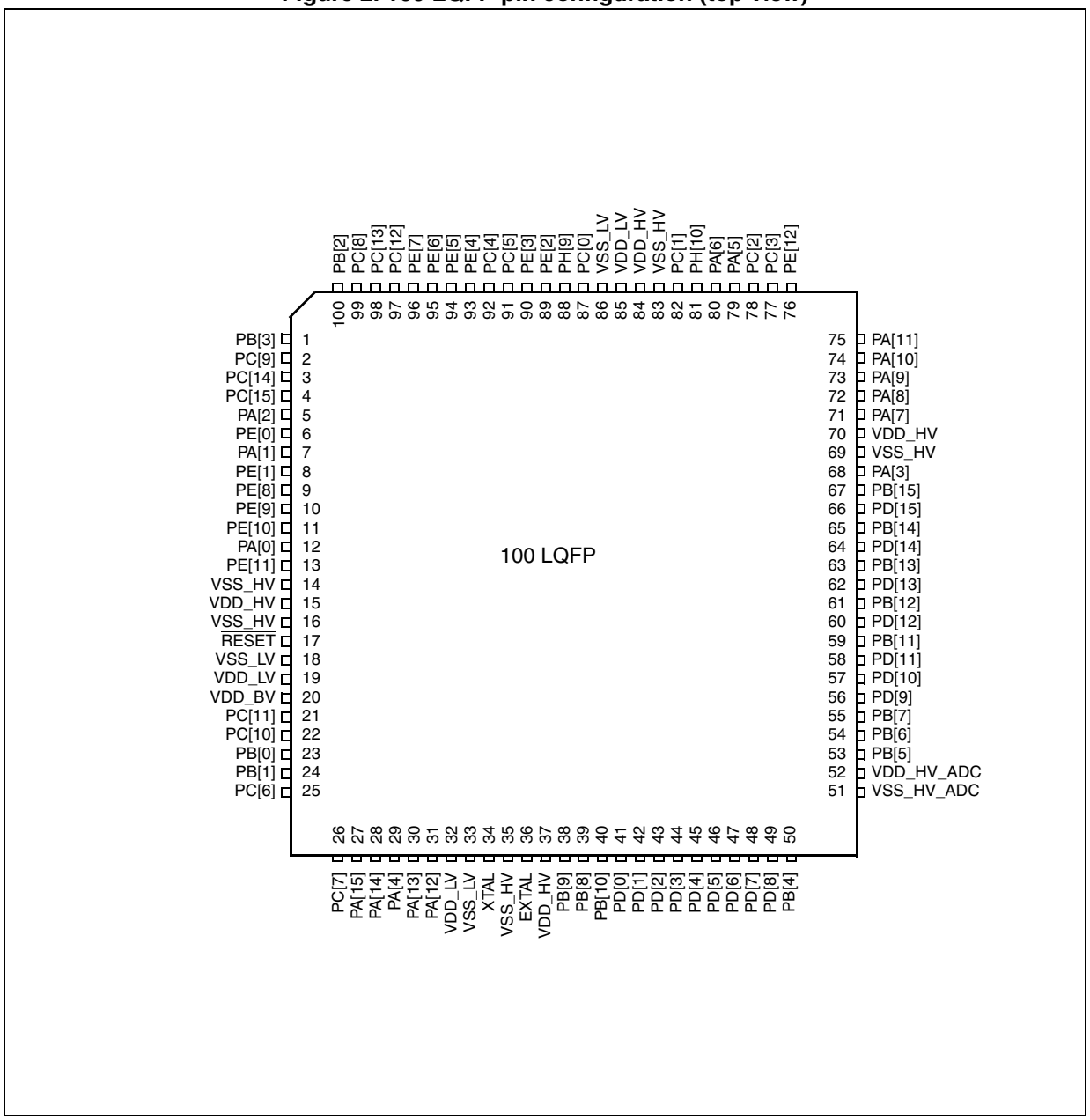
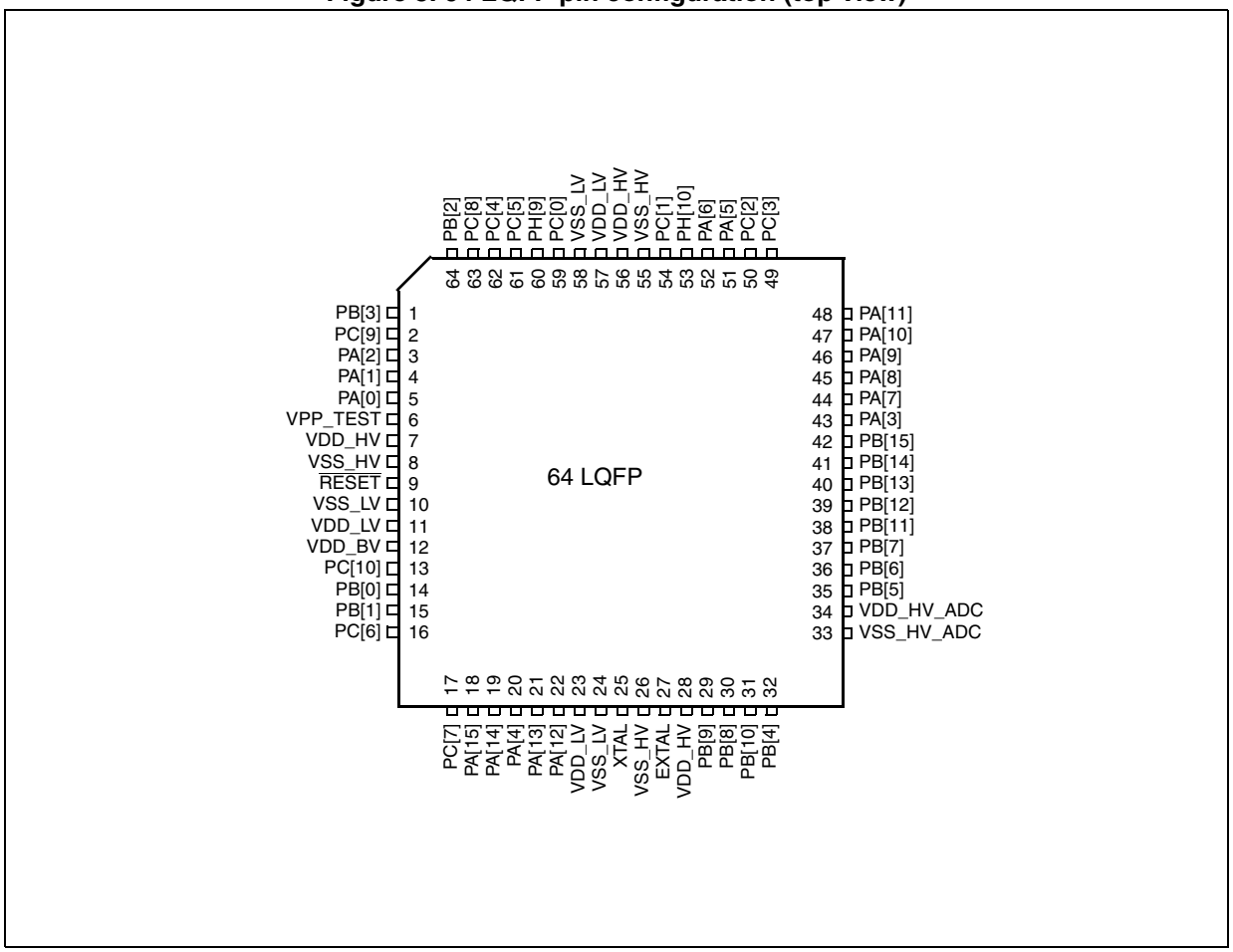


Figure 3 shows the MPC5602D in the 64 LQFP package.

Figure 3. 64 LQFP pin configuration (top view)



3.2 Pin muxing

Table 3 defines the pin list and muxing for this device.

Each entry of Table 3 shows all the possible configurations for each pin, via the alternate functions. The default function assigned to each pin after reset is indicated by AF0.

Table 3. Functional port pin descriptions

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin No.	
								64 LQFP	100 LQFP
Port A									
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKUP[19][3]	SIUL eMIOS_0 CGL eMIOS_0 WKPU	I/O I/O O I/O I	M	Tristate	5	12

Table 3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin No.	
								64 LQFP	100 LQFP
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — —	GPIO[1] E0UC[1] — — NMI[4] WKUP[2][3]	SIUL eMIOS_0 — — WKPU WKPU	I/O I/O — — I I	S	Tristate	4	7
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — — WKUP[3][3]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	3	5
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — —‘	GPIO[3] E0UC[3] — — EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 — — SIUL ADC	I/O I/O — — I I	S	Tristate	43	68
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — — WKUP[9][3]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	20	29
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	51	79
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — — EIRQ[1]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	52	80
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — —	GPIO[7] E0UC[7] — — EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 — — SIUL ADC	I/O I/O — — I I	S	Tristate	44	71
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[5]	GPIO[8] E0UC[8] E0UC[14] — EIRQ[3] ABS[0]	SIUL eMIOS_0 eMIOS_0 — SIUL BAM	I/O I/O — — I I	S	Input, weak pull-up	45	72

Table 3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin No.	
								64 LQFP	100 LQFP
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[5]	GPIO[9] E0UC[9] — — FAB	SIUL eMIOS_0 — — BAM	I/O I/O — — I	S	Pull-down	46	73
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 —	GPIO[10] E0UC[10] — LIN1TX ADC1_S[2]	SIUL eMIOS_0 — LINFlex_1 ADC	I/O I/O — O I	S	Tristate	47	74
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — —	GPIO[11] E0UC[11] — — EIRQ[16] ADC1_S[3] LIN2RX	SIUL eMIOS_0 — — SIUL ADC LINFlex_2	I/O I/O — — I I I	S	Tristate	48	75
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — — — EIRQ[17] SIN_0	SIUL — — — SIUL DSPI_0	I/O — — — I I	S	Tristate	22	31
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 — —	SIUL DSPI_0 — —	I/O O — —	M	Tristate	21	30
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M	Tristate	19	28
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKUP[10][3]	SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU	I/O I/O I/O I/O I	M	Tristate	18	27
Port B									
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX — —	SIUL FlexCAN_0 — —	I/O O — —	M	Tristate	14	23

Table 3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin No.	
								64 LQFP	100 LQFP
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — —	GPIO[17] — — — WKUP[4][3] CAN0RX	SIUL — — — WKPU FlexCAN_0	I/O — — — I I	S	Tristate	15	24
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX — —	SIUL LINFlex_0 — —	I/O O — —	M	Tristate	64	100
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] — — — WKUP[11][3] LIN0RX	SIUL — — — WKPU LINFlex_0	I/O — — — I I	S	Tristate	1	1
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 —	GPIO[20] — — — ADC1_P[0]	SIUL — — — ADC	I — — — I	I	Tristate	32	50
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 —	GPIO[21] — — — ADC1_P[1]	SIUL — — — ADC	I — — — I	I	Tristate	35	53
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 —	GPIO[22] — — — ADC1_P[2]	SIUL — — — ADC	I — — — I	I	Tristate	36	54
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — — ADC1_P[3]	SIUL — — — ADC	I — — — I	I	Tristate	37	55
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — — ADC1_S[4] WKUP[25][3]	SIUL — — — ADC WKPU	I — — — I I	I	Tristate	30	39

Table 3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin No.	
								64 LQFP	100 LQFP
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — ADC1_S[5] WKUP[26][3]	SIUL — — — ADC WKPU	I — — — I I	I	Tristate	29	38
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ADC1_S[6] WKUP[8][3]	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	31	40
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC1_S[12]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	59
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC1_X[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	61
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC1_X[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	63
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC1_X[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	65
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC1_X[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	67
Port C									
PC[0][6]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	87
PC[1][6]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F	Tristate	54	82

Table 3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin No.	
								64 LQFP	100 LQFP
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 — — EIRQ[5]	SIUL DSPI_1 — — SIUL	I/O I/O — — I	M	Tristate	50	78
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 —	GPIO[35] CS0_1 MA[0] — EIRQ[6]	SIUL DSPI_1 ADC — SIUL	I/O I/O O — I	S	Tristate	49	77
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — —	GPIO[36] — — — SIN_1 EIRQ[18]	SIUL — — — DSPI_1 SIUL	I/O — — — I I	M	Tristate	62	92
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 — — EIRQ[7]	SIUL DSPI_1 — — SIUL	I/O O — — I	M	Tristate	61	91
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX — —	SIUL LINFlex_1 — —	I/O O — —	S	Tristate	16	25
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — — — LIN1RX WKUP[12][3]	SIUL — — — LINFlex_1 WKPU	I/O — — — I I	S	Tristate	17	26
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX — —	SIUL LINFlex_2 — —	I/O O — —	S	Tristate	63	99
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — — — LIN2RX WKUP[13][3]	SIUL — — — LINFlex_2 WKPU	I/O — — — I I	S	Tristate	2	2
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] — — MA[1]	SIUL — — ADC	I/O — — O	M	Tristate	13	22

Table 3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin No.	
								64 LQFP	100 LQFP
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 —	GPIO[43] — — MA[2] WKUP[5][3]	SIUL — — ADC WKPU	I/O — — O I	S	Tristate	—	21
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — EIRQ[19]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	97
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	98
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] — — EIRQ[8]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	—	3
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] — — EIRQ[20]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	4
Port D									
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 — —	GPIO[48] — — — WKUP[27][3] ADC1_P[4]	SIUL — — — WKPU ADC	I — — — I I	I	Tristate	—	41
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 — —	GPIO[49] — — — WKUP[28][3] ADC1_P[5]	SIUL — — — WKPU ADC	I — — — I I	I	Tristate	—	42
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 —	GPIO[50] — — — ADC1_P[6]	SIUL — — — ADC	I — — — I	I	Tristate	—	43

Table 3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin No.	
								64 LQFP	100 LQFP
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 —	GPIO[51] — — — ADC1_P[7]	SIUL — — — ADC	I — — — I	I	Tristate	—	44
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 —	GPIO[52] — — — ADC1_P[8]	SIUL — — — ADC	I — — — I	I	Tristate	—	45
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 —	GPIO[53] — — — ADC1_P[9]	SIUL — — — ADC	I — — — I	I	Tristate	—	46
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 —	GPIO[54] — — — ADC1_P[10]	SIUL — — — ADC	I — — — I	I	Tristate	—	47
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 —	GPIO[55] — — — ADC1_P[11]	SIUL — — — ADC	I — — — I	I	Tristate	—	48
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 —	GPIO[56] — — — ADC1_P[12]	SIUL — — — ADC	I — — — I	I	Tristate	—	49
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 —	GPIO[57] — — — ADC1_P[13]	SIUL — — — ADC	I — — — I	I	Tristate	—	56
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 —	GPIO[58] — — — ADC1_P[14]	SIUL — — — ADC	I — — — I	I	Tristate	—	57
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 —	GPIO[59] — — — ADC1_P[15]	SIUL — — — ADC	I — — — I	I	Tristate	—	58

Table 3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin No.	
								64 LQFP	100 LQFP
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC1_S[8]	SIUL DSPI_0 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	60
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ADC1_S[9]	SIUL DSPI_1 eMIOS_0 — ADC	I/O I/O I/O — I	J	Tristate	—	62
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] — ADC1_S[10]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	64
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] — ADC1_S[11]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	66
Port E									
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 —	GPIO[64] E0UC[16] — — WKUP[6][3]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	—	6
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	8
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 — —	GPIO[66] E0UC[18] — — EIRQ[21] SIN_1	SIUL eMIOS_0 — — SIUL DSPI_1	I/O I/O — — I I	M	Tristate	—	89
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 —	SIUL eMIOS_0 DSPI_1 —	I/O I/O O —	M	Tristate	—	90
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 —	GPIO[68] E0UC[20] SCK_1 — EIRQ[9]	SIUL eMIOS_0 DSPI_1 — SIUL	I/O I/O I/O — I	M	Tristate	—	93

Table 3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin No.	
								64 LQFP	100 LQFP
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC	I/O I/O I/O O	M	Tristate	—	94
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[21]	SIUL eMIOS_0 DSPI_0 ADC SIUL	I/O I/O O O I	M	Tristate	—	95
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[21]	SIUL eMIOS_0 DSPI_0 ADC SIUL	I/O I/O O O I	M	Tristate	—	96
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] — E0UC[22] —	SIUL — eMIOS_0 —	I/O — I/O —	M	Tristate	—	9
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 —	GPIO[73] — E0UC[23] — WKUP[7][3]	SIUL — eMIOS_0 — WKPU	I/O — I/O — I	S	Tristate	—	10
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] — CS3_1 — EIRQ[10]	SIUL — DSPI_1 — SIUL	I/O — O — I	S	Tristate	—	11
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 —	GPIO[75] E0UC[24] CS4_1 — WKUP[14][3]	SIUL eMIOS_0 DSPI_1 — WKPU	I/O I/O O — I	S	Tristate	—	13
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — —	GPIO[76] — — — ADC1_S[7] EIRQ[11]	SIUL — — — ADC SIUL	I/O — — — I I	S	Tristate	—	76
Port H									
PH[9][6]	PCR[121]	AF0 AF1 AF2 AF3	GPIO[121] — TCK —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	60	88

Table 3. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET config.	Pin No.	
								64 LQFP	100 LQFP
PH[10][6]	PCR[122]	AF0 AF1 AF2 AF3	GPIO[122] — TMS —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	53	81

1 Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00 → AF0; PCR.PA = 01 → AF1; PCR.PA = 10 → AF2; PCR.PA = 11 → AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

2 Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

3 All WKUP pins also support external interrupt capability. See "wakeup unit" chapter for further details.

4 NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.

5 "Not applicable" because these functions are available only while the device is booting. Refer to "BAM" chapter of the device reference manual for details.

6 Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
PC[0:1] are available as JTAG pins (TDI and TDO respectively).
PH[9:10] are available as JTAG pins (TCK and TMS respectively).
It is up to the user to configure these pins as GPIO when needed.

4 Electrical characteristics

4.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol "CC" for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol "SR" for System Requirement is included in the Symbol column.

CAUTION

All of the following parameter values can vary depending on the application and must be confirmed during silicon validation, silicon characterization or silicon reliability trial.

4.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 4 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 4. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.3 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the non-volatile user options register (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the MPC5602D reference manual.

4.3.1 NVUSRO[PAD3V5V] field description

Table 5 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 5. PAD3V5V field description[1]

Value[2]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1 See the device reference manual for more information on the NVUSRO register.

2 '1' is delivery value. It is part of shadow Flash, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V bit value.

4.3.2 NVUSRO[OSCILLATOR_MARGIN] field description

Table 6 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 6. OSCILLATOR_MARGIN field description[1]

Value[2]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

1 See the device reference manual for more information on the NVUSRO register.

2 '1' is delivery value. It is part of shadow Flash, thus programmable by customer.

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value.

4.4 Absolute maximum ratings

Table 7. Absolute maximum ratings

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SS}	SR	—	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}	SR	—	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	–0.3	6.0	V
V_{SS_LV}	SR	—	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}	SR	—	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	–0.3	6.0	V
				Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{SS_ADC}	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	–0.3	6.0	V
				Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{IN}	SR	—	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
				Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
I_{INJPAD}	SR	—	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	—	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
I_{AVGSEG}	SR	—	Sum of all the static I/O current within a supply segment[1]	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	64	
I_{CORELV}	SR	—	Low voltage static current sink through VDD_BV	—	—	150	mA
$T_{STORAGE}$	SR	—	Storage temperature	—	–55	150	°C

1 Supply segments are described in Section 4.7.5, “I/O pad current specification.

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

4.5 Recommended operating conditions

Table 8. Recommended operating conditions (3.3 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SS}	SR	—	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	—	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS_LV}[2]	SR	—	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}[3]	SR	—	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
				Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SS_ADC}	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}[4]	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	3.0[5]	3.6	V
				Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	SR	—	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
				Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	SR	—	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	—	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
TV_{DD}	SR	—	V_{DD} slope to ensure correct power up[6]	—	TBD	0.25	V/µs
T_A	SR	—	Ambient temperature under bias	$f_{CPU} \leq 48$ MHz	–40	125	°C
T_J	SR	—	Junction temperature under bias	—	–40	150	

1 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

2 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

3 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).

4 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

5 Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.

6 Guaranteed by device validation

Table 9. Recommended operating conditions (5.0 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SS}	SR	—	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	—	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	4.5	5.5	V
				Voltage drop[2]	3.0	5.5	
V_{SS_LV}[3]	SR	—	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}[4]	SR	—	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	4.5	5.5	V
				Voltage drop(2)	3.0	5.5	
				Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SS_ADC}	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}[5]	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
				Voltage drop(2)	3.0	5.5	
				Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	SR	—	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
				Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	SR	—	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	—	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	—	V_{DD} slope to ensure correct power up[6]	—	TBD	0.25	V/µs
T_A	SR	—	Ambient temperature under bias	$f_{CPU} \leq 48$ MHz	–40	125	°C
T_J	SR	—	Junction temperature under bias	—	–40	150	

1 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

2 Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.6 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.

3 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

4 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).

5 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

6 Guaranteed by device validation

NOTE

SRAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

4.6 Thermal characteristics

4.6.1 Package thermal characteristics

Table 10. LQFP thermal characteristics[1]

Symbol		C	Parameter	Conditions[2]	Pin count	Value[3]	Unit
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[4]	Single-layer board —1s	64	72.1	°C/W
					100	65.2	
				Four-layer board — 2s2p	64	57.3	
					100	51.8	
$R_{\theta JB}$	CC	D	Thermal resistance, junction-to-board[5]	Single-layer board — 1s	64	45.6	°C/W
					100	42.6	
				Four-layer board — 2s2p	64	44.1	
					100	41.3	
$R_{\theta JC}$	CC	D	Thermal resistance, junction-to-case[6]	Single-layer board — 1s	64	26.5	°C/W
					100	23.9	
				Four-layer board — 2s2p	64	26.2	
					100	23.7	
Ψ_{JB}	CC	D	Junction-to-board thermal characterization parameter, natural convection	Single-layer board — 1s	64	41	°C/W
					100	41.6	
				Four-layer board — 2s2p	64	43	
					100	43.4	
Ψ_{JC}	CC	D	Junction-to-case thermal characterization parameter, natural convection	Single-layer board — 1s	64	11.5	°C/W
					100	10.4	
				Four-layer board — 2s2p	64	11.1	
					100	10.2	

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C

3 All values need to be confirmed during device validation.

4 Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA} and R_{thJMA}.

5 Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as R_{thJB}.

6 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer. When Greek letters are not available, the symbols are typed as R_{thJC}.

4.6.2 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times R_{\theta JA}) \quad \textit{Eqn. 1}$$

Where:

T_A is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273\ °C) + R_{\theta JA} \times P_D^2 \quad \textit{Eqn. 3}$$

Where:

K is a constant for the particular part, which may be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations 1 and 2 iteratively for any value of T_A.

4.7 I/O pad electrical characteristics

4.7.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Input only pads—These pads are associated to ADC channels (ADC_P[X]) providing low input leakage.

Medium pads can use slow configuration to reduce electromagnetic emission except for PC[1], that is medium only, at the cost of reducing AC performance.

4.7.2 I/O input DC characteristics

Table 11 provides input DC electrical characteristics as described in Figure 4.

Figure 4. I/O input DC electrical characteristics definition

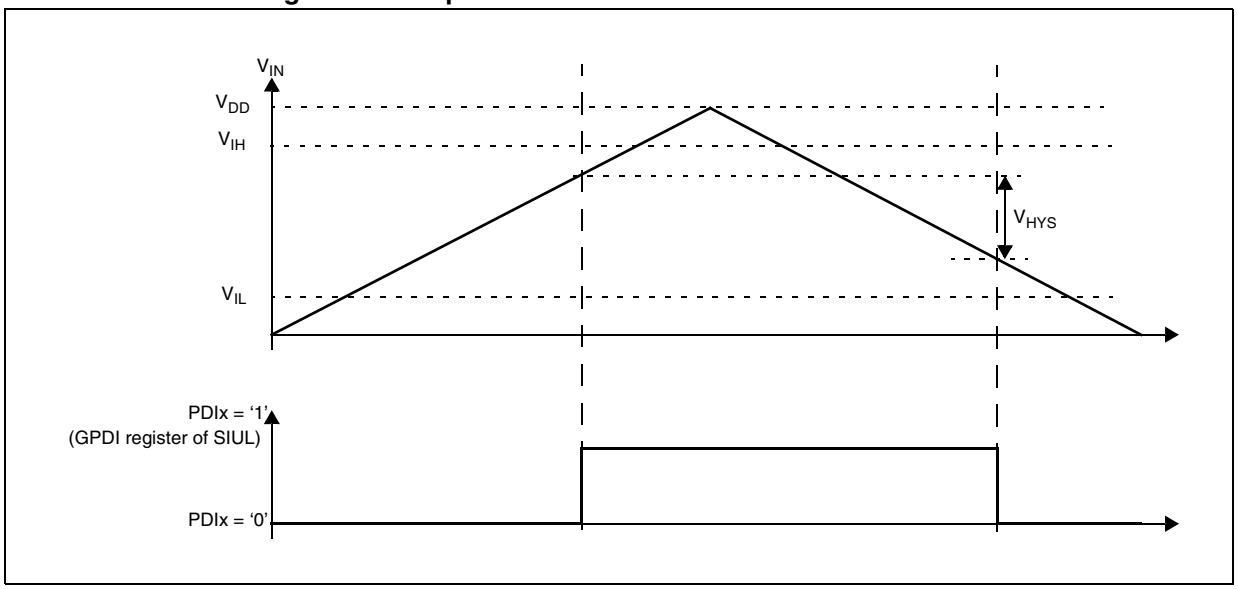


Table 11. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		–0.4	—	$0.35V_{DD}$	
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		$0.1V_{DD}$	—	—	
I_{LKG}	CC	P	Digital input leakage	No injection on adjacent pin	T_A = –40 °C	—	2	—	nA
		P			T_A = 25 °C	—	2	—	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}[3]	SR	P	Digital input filtered pulse	—		—	—	40	ns
W_{NFI}[3]	SR	P	Digital input not filtered pulse	—		1000	—	—	ns

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

4.7.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 12 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 13 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 14 provides output driver characteristics for I/O pads when in MEDIUM configuration.

Table 12. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[2]	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\lvert I_{WPD} \rvert$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[2]	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 13. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V_{DD}	—	—	V
		C			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	0.8V_{DD}	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V_{DD}	V
		C			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(2)	—	—	0.1V_{DD}	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 14. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		P			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
		C			I_{OH} = –100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		P			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(2)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
		C			I_{OH} = 100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

4.7.4 Output pin transition times

Table 15. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[3] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
T_{tr}	CC	D	Output transition time output pin(3) MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 C_L includes device and package capacitances (C_{PKG} < 5 pF).

4.7.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 16.

Table 17 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 16. I/O supply segment

Package	Supply segment			
	1	2	3	4
100 LQFP	pin 16 – pin 35	pin 37 – pin 69	pin 70 – pin 83	pin 84 – pin 15
64 LQFP	pin 8 – pin 26	pin 28 – pin 55	pin 56 – pin 7	—

Table 17. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
I_{SWTSLW}[3]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}(3)	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{RMSSLW}	CC	D	Root medium square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root medium square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 18 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below 100%.

Table 18. I/O weight[1]

PAD	100/64 LQFP			
	Weight 5V SRC = 0	Weight 5V SRC = 1	Weight 3.3V SRC = 0	Weight 3.3V SRC = 1
PB[3]	9%	9%	10%	10%
PC[9]	8%	8%	10%	10%
PC[14]	8%	8%	10%	10%
PC[15]	8%	11%	9%	10%
PA[2]	8%	8%	9%	9%
PE[0]	7%	7%	9%	9%
PA[1]	7%	7%	8%	8%
PE[1]	7%	10%	8%	8%
PE[8]	6%	9%	8%	8%
PE[9]	6%	6%	7%	7%
PE[10]	6%	6%	7%	7%
PA[0]	5%	7%	6%	7%
PE[11]	5%	5%	6%	6%
PC[11]	7%	7%	9%	9%
PC[10]	8%	11%	9%	10%
PB[0]	8%	11%	9%	10%
PB[1]	8%	8%	10%	10%
PC[6]	8%	8%	10%	10%
PC[7]	8%	8%	10%	10%
PA[15]	8%	11%	9%	10%
PA[14]	7%	11%	9%	9%
PA[4]	7%	7%	8%	8%
PA[13]	7%	10%	8%	9%
PA[12]	7%	7%	8%	8%
PB[9]	1%	1%	1%	1%
PB[8]	1%	1%	1%	1%
PB[10]	5%	5%	6%	6%
PD[0]	1%	1%	1%	1%
PD[1]	1%	1%	1%	1%
PD[2]	1%	1%	1%	1%
PD[3]	1%	1%	1%	1%
PD[4]	1%	1%	1%	1%
PD[5]	1%	1%	1%	1%

Table 18. I/O weight[1] (continued)

PAD	100/64 LQFP			
	Weight 5V SRC = 0	Weight 5V SRC = 1	Weight 3.3V SRC = 0	Weight 3.3V SRC = 1
PD[6]	1%	1%	1%	1%
PD[7]	1%	1%	1%	1%
PD[8]	1%	1%	1%	1%
PB[4]	1%	1%	1%	1%
PB[5]	1%	1%	1%	1%
PB[6]	1%	1%	1%	1%
PB[7]	1%	1%	1%	1%
PD[9]	1%	1%	1%	1%
PD[10]	1%	1%	1%	1%
PD[11]	1%	1%	1%	1%
PB[11]	9%	9%	11%	11%
PD[12]	8%	8%	10%	10%
PB[12]	8%	8%	10%	10%
PD[13]	8%	8%	9%	9%
PB[13]	8%	8%	9%	9%
PD[14]	7%	7%	9%	9%
PB[14]	7%	7%	8%	8%
PD[15]	7%	7%	8%	8%
PB[15]	6%	6%	7%	7%
PA[3]	6%	6%	7%	7%
PA[7]	4%	4%	5%	5%
PA[8]	4%	4%	5%	5%
PA[9]	4%	4%	5%	5%
PA[10]	5%	5%	6%	6%
PA[11]	5%	5%	6%	6%
PE[12]	5%	5%	6%	6%
PC[3]	5%	5%	6%	6%
PC[2]	5%	7%	6%	6%
PA[5]	5%	6%	5%	6%
PA[6]	4%	4%	5%	5%
PC[1]	5%	17%	4%	12%
PC[0]	6%	9%	7%	8%
PE[2]	7%	10%	8%	9%

Table 18. I/O weight[1] (continued)

PAD	100/64 LQFP			
	Weight 5V SRC = 0	Weight 5V SRC = 1	Weight 3.3V SRC = 0	Weight 3.3V SRC = 1
PE[3]	7%	10%	9%	9%
PC[5]	8%	11%	9%	10%
PC[4]	8%	11%	9%	10%
PE[4]	8%	12%	10%	10%
PE[5]	8%	12%	10%	11%
PE[6]	9%	12%	10%	11%
PE[7]	9%	12%	10%	11%
PC[12]	9%	13%	11%	11%
PC[13]	9%	9%	11%	11%
PC[8]	9%	9%	11%	11%
PB[2]	9%	13%	11%	12%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.8 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 5. Start-up reset requirements

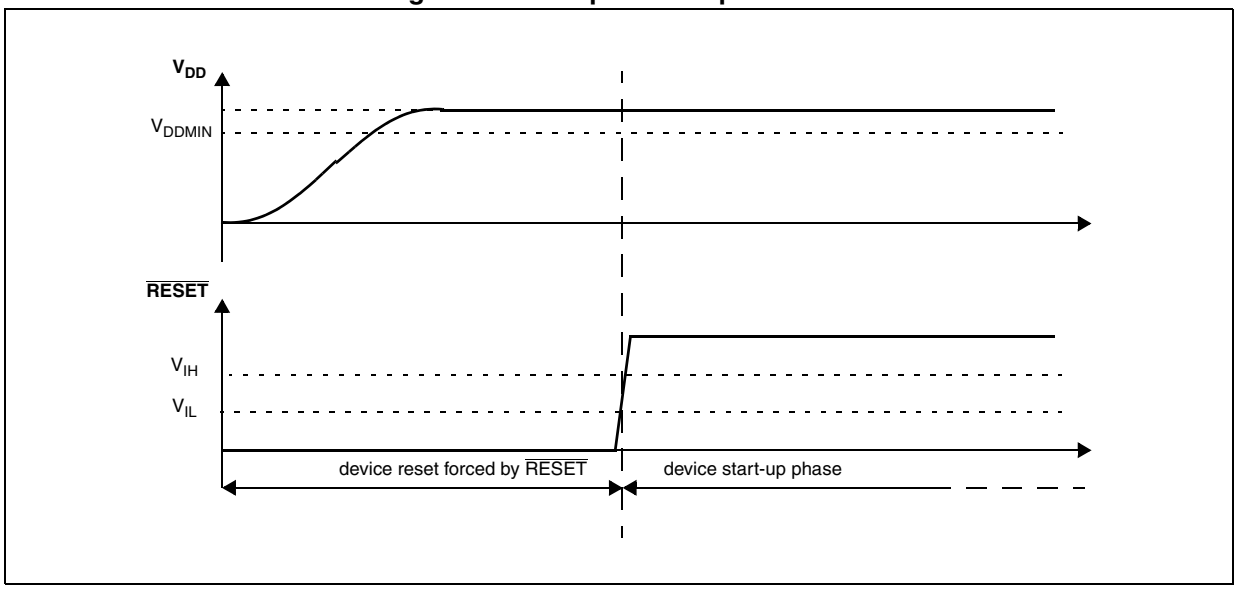


Figure 6. Noise filtering on reset signal

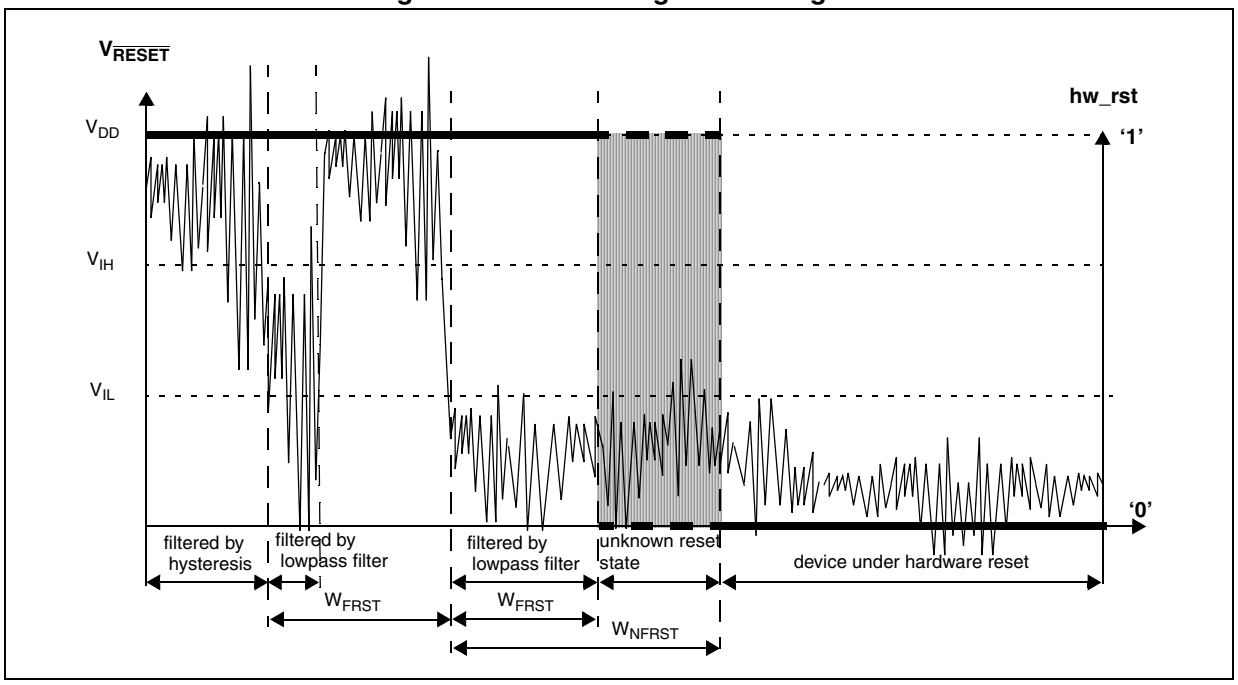


Table 19. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	D	Output transition time output pin[4] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	1000	—	—	ns
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[5]	10	—	250	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of the device reference manual).

4 C_L includes device and package capacitance (C_{PKG} < 5 pF).

5 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

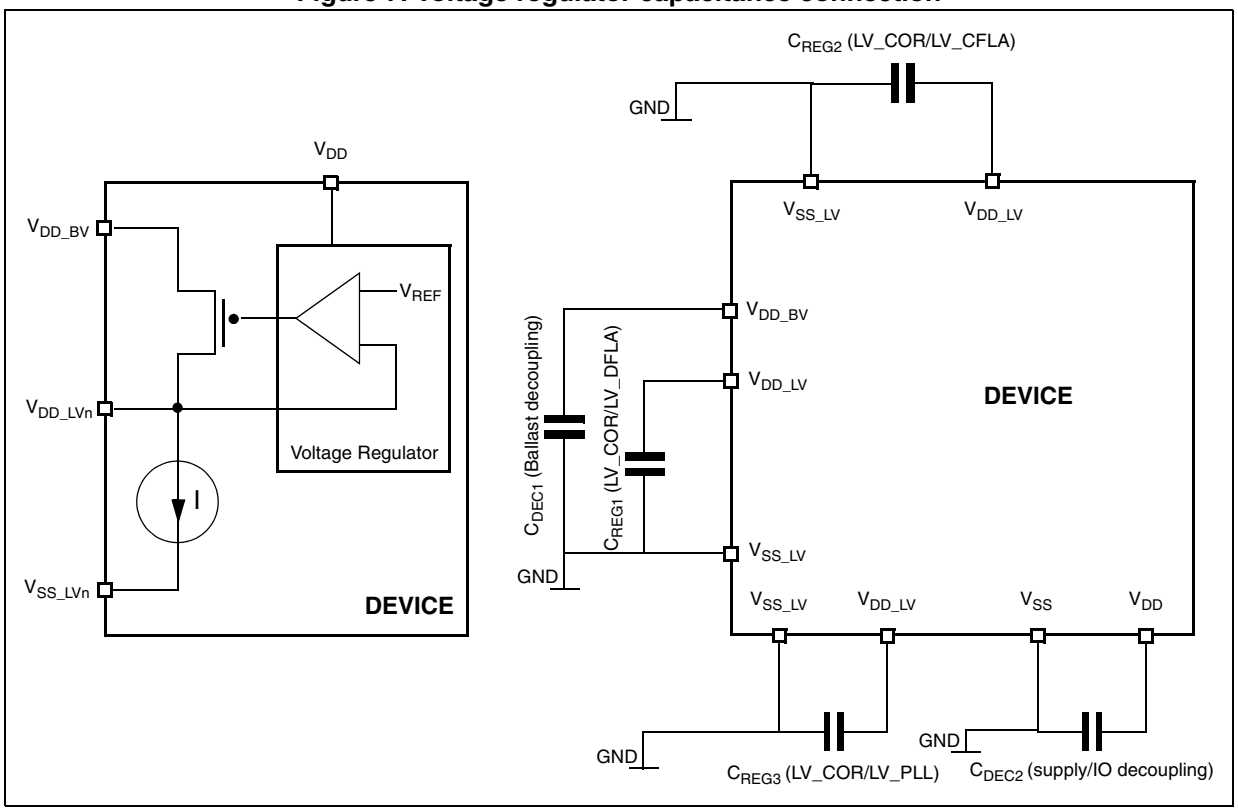
4.9 Power management electrical characteristics

4.9.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply V_{DD_BV}. The regulator itself is supplied by the common I/O supply V_{DD}. The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through V_{DD} power pin.
- BV: High voltage external power supply for internal ballast module. This must be provided externally through V_{DD_BV} power pin. Voltage values should be aligned with V_{DD}.
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
  - LV_CFLA: Low voltage supply for Code Flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_DFLA: Low voltage supply for Data Flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

Figure 7. Voltage regulator capacitance connection



The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see Section 4.5, "Recommended operating conditions).

Table 20. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	—	—	—	0.2	Ω
C_{DEC1}	SR	—	Decoupling capacitance[3] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100[4]	470[5]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	TBD	1.28	TBD	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low power regulator output voltage	After trimming	TBD	1.23	TBD	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	—	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	TBD	1.23	TBD	V
I_{ULPREG}	SR	—	Ultra low power regulator current provided to V_{DD_LV} domain	—	—	—	5	mA
$I_{ULPREGINT}$	CC	D	Ultra low power regulator module current consumption	I_{ULPREG} = 5 mA; T_A = 55 °C	—	—	100	µA
				I_{ULPREG} = 0 mA; T_A = 55 °C	—	2	—	
I_{DD_BV}	CC	D	In-rush current on V_{DD_BV} during power-up	—	—	—	400[6]	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 All values need to be confirmed during device validation.

3 This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.

4 This value is acceptable to guarantee operation from 4.5 V to 5.5 V.

5 External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.

6 In-rush current is seen only for short time during power-up and on standby exit (max 20 µs, depending on external capacitances to be load).

4.9.2 Voltage monitor electrical characteristics

The device implements a power-on reset (POR) module to ensure correct power-up initialization, as well as four low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

NOTE

When enabled, power domain No. 2 is monitored through LVD_DIGBKP.

Figure 8. Low voltage monitor vs. reset

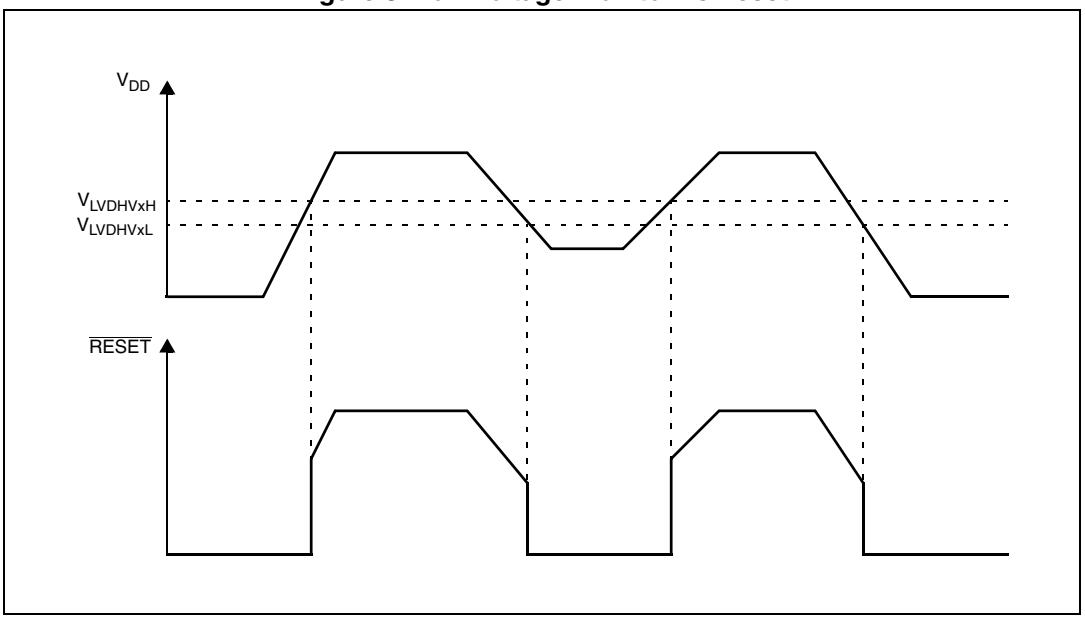


Table 21. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{PORUP}	SR	P	Supply for functional POR module	—	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold	T_A = 25 °C, after trimming	1.5	—	2.6	
		T		—	1.5	—	2.6	
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold	—	—	—	2.9	
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold	—	2.6	—	TBD	
$V_{LVDHV5H}$[3]	CC	T	LVDHV5 low voltage detector high threshold	—	—	—	4.4	
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold	—	3.8	—	TBD	
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold	—	1.08	—	—	
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold	—	1.08	—	1.11	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 Data based on characterization results, not tested in production

4.10 Low voltage domain power consumption

Table 22 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 22. Low voltage power domain electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{DDMAX}[2]	CC	D	RUN mode maximum average current	—		—	100	TBD[3]	mA
I_{DDRUN}[4]	CC	T	RUN mode typical average current[5]	f_{CPU} = 8 MHz		—	TBD	—	mA
		T		f_{CPU} = 16 MHz		—	TBD	—	
		T		f_{CPU} = 32 MHz		—	TBD	—	
		P		f_{CPU} = 48 MHz		—	TBD	—	
I_{DDHALT}	CC	C	HALT mode current[6]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	TBD	TBD	mA
		P			T_A = 125 °C	—	TBD	TBD	
I_{DDSTOP}	CC	P	STOP mode current[7]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	150	TBD[8]	µA
		D			T_A = 55 °C	—	TBD	—	
		D			T_A = 85 °C	—	TBD	—	mA
		D			T_A = 105 °C	—	TBD	—	
		P			T_A = 125 °C	—	TBD	TBD[8]	

Table 22. Low voltage power domain electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$I_{DDSTDBY}$	CC	P	STANDBY mode current[9]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	25	TBD	µA
		D			T_A = 55 °C	—	TBD	—	
		D			T_A = 85 °C	—		—	
		D			T_A = 105 °C	—		—	
		P			T_A = 125 °C	—		TBD	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Running consumption is given on voltage regulator supply (V_{DDREG}). It does not include consumption linked to I/Os toggling. This value is **highly** dependent on the application. The given value is thought to be a **worst case value** with all peripherals running, and code fetched from Code Flash while modify operation on-going on Data Flash. Note that this value can be significantly reduced by application: switch off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from SRAM most used functions, use low power mode when possible.

3 Higher current may be sinked by device during power-up and standby exit. Please refer to in rush current on Table 20.

4 RUN current measured with typical application with accesses on both Flash and SRAM.

5 Only for the “P” classification: Code fetched from SRAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled.

6 Data Flash Power Down. Code Flash in Low Power. RC-OSC 128 kHz & RC-OSC 16 MHz on. 10 MHz XTAL clock. FlexCAN: 0 ON (clocked but no reception or transmission). LINFlex: instances: 0, 1, 2 ON (clocked but no reception or transmission), instance: 3 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication). RTC/API ON.PIT ON. STM ON. ADC ON but no conversion except 2 analog watchdogs.

7 Only for the “P” classification: No clock, RC-OSC 16 MHz off, RC-OSC 128 kHz on, PLL off, HPVreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

8 When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.

9 Only for the “P” classification: ULPVreg on, HP/LPVreg off, 16 KB SRAM on, device configured for minimum consumption, all possible modules switched off.

4.11 Flash memory electrical characteristics

The Data Flash operation depends strongly on the Code Flash operation. If Code Flash is switched-off, the Data Flash is disabled.

4.11.1 Program/Erase characteristics

Table 23 shows the program and erase characteristics.

Table 23. Program and erase specifications (Code Flash)

Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	—	22	50	500	µs
$T_{16KpperaseC}$			16 KB block preprogram and erase time	—	300	500	5000	ms
$T_{32KpperaseC}$			32 KB block preprogram and erase time	—	400	600	5000	ms
$T_{128KpperaseC}$			128 KB block preprogram and erase time	—	800	1300	7500	ms
T_{esus}			Erase suspend latency	TBD	TBD	TBD	TBD	µs

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 24. Program and erase specifications (Data Flash)

Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{swprogram}$	CC	C	Single word (32 bits) program time[4]	—	30	70	300	µs
$T_{16Kpperase}$			16 KB block preprogram and erase time	—	700	800	1500	ms
T_{Bank_D}			64 KB block preprogram and erase time	—	1900	2300	4800	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 25. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100	—	—	kcycles
P/E	CC	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10	100[1]	—	kcycles
P/E	CC	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1	100(1)	—	kcycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[2]	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	years
				Blocks with 10,001–100,000 P/E cycles	5	—	—	years

1 To be confirmed

2 Ambient temperature averaged over application duration. It is recommended not to exceed the product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 26. Flash read access timing

Symbol		C	Parameter	Conditions[1]	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	48	MHz
		C		1 wait state	40	
		C		0 wait states	20	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.11.2 Flash power supply DC characteristics

Table 27 shows the power supply DC characteristics on external supply.

NOTE

Power supply for Data Flash is actually provided by Code Flash, this means that Data Flash cannot work if Code Flash is not powered.

Table 27. Flash power supply DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
I_{CFREAD}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} on read access	Flash module read f_{CPU} = 48 MHz	Code Flash	—	—	33	mA
I_{DFREAD}					Data Flash	—	—	4	
I_{CFMOD}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} on matrix modification (program/erase)	Program/Erase on-going while reading Flash registers, f_{CPU} = 48 MHz	Code Flash	—	—	33	mA
I_{DFMOD}					Data Flash	—	—	6	
I_{FLPW}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} during Flash low-power mode	—	Code Flash	—	—	910	µA
I_{CFPWD}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} during Flash power-down mode	—	Code Flash	—	—	125	µA
I_{DFPWD}					Data Flash	—	—	25	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

4.11.3 Start-up/Switch-off timings

Table 28. Start-up time/Switch-off time

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$T_{FLARSTEXIT}$	CC	T	Delay for Flash module to exit reset mode	Code Flash	—	—	125	µs
				Data Flash	—	—	150	
$T_{FLALPEXIT}$	CC	T	Delay for Flash module to exit low-power mode[2]	Code Flash	—	—	0.5	
$T_{FLAPDEXIT}$	CC	T	Delay for Flash module to exit power-down mode	Code Flash	—	—	30	
				Data Flash			30[3]	
$T_{FLALPENTRY}$	CC	T	Delay for Flash module to enter low-power mode	Code Flash	—	—	0.5	
$T_{FLAPDENTRY}$	CC	T	Delay for Flash module to enter power-down mode	Code Flash	—	—	1.5	
				Data Flash	—	—	4(3)	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Data Flash does not support low-power mode

3 If Code Flash is already switched-on.

4.12 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

4.12.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter
  - Unexpected reset
  - Critical data corruption (control registers...)
- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.12.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC 61967-1 standard, which specifies the general conditions for EMI measurements.

Table 29. EMI radiated emission measurement[1,2]

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150	—	1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	48	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, 100 LQFP package Test conforming to IEC 61967-2, f_{OSC} = 8 MHz/f_{CPU} = 48 MHz	No PLL frequency modulation	—	—	TBD	dBµV
					± 2% PLL frequency modulation	—	—	TBD[3]	dBµV

1 EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

2 For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

3 All values need to be confirmed during device validation

4.12.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

4.12.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts * (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 30. ESD absolute maximum ratings[1] [2]

Symbol		C	Ratings	Conditions	Class	Max value	Unit
$V_{ESD(HBM)}$	CC	T	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	CC	T	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	CC	T	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
						750 (corners)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.12.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 31. Latch-up results

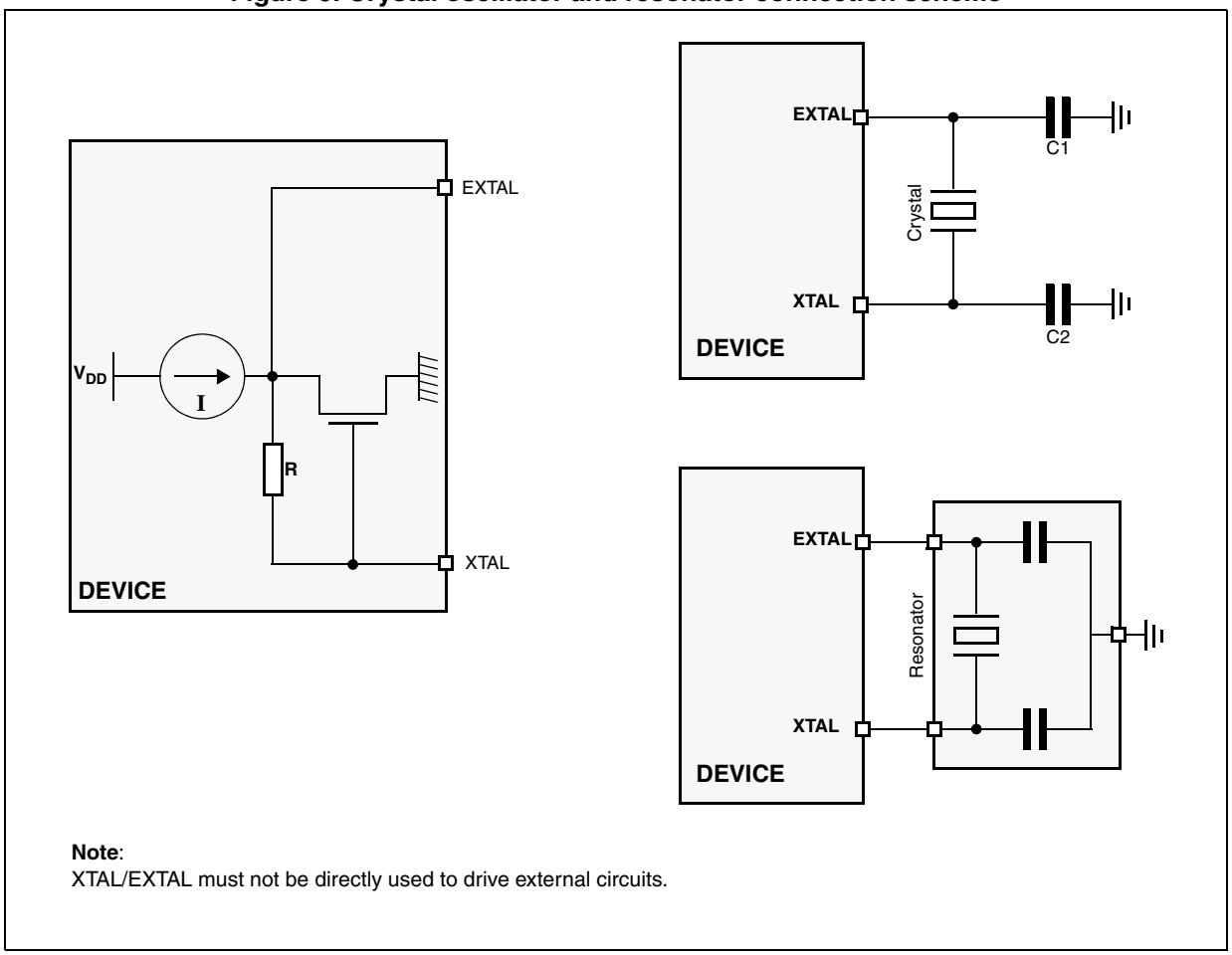
Symbol		C	Parameter	Conditions	Class
LU	CC	T	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

4.13 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 9 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 32 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

Figure 9. Crystal oscillator and resonator connection scheme



Note:
XTAL/EXTAL must not be directly used to drive external circuits.

Table 32. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout $C_1 = C_2$ (pF)[1]	Shunt capacitance between xtalout and xtalin $C0$[2] (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

1 The values specified for C_1 and C_2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

2 The value of C_0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

Figure 10. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

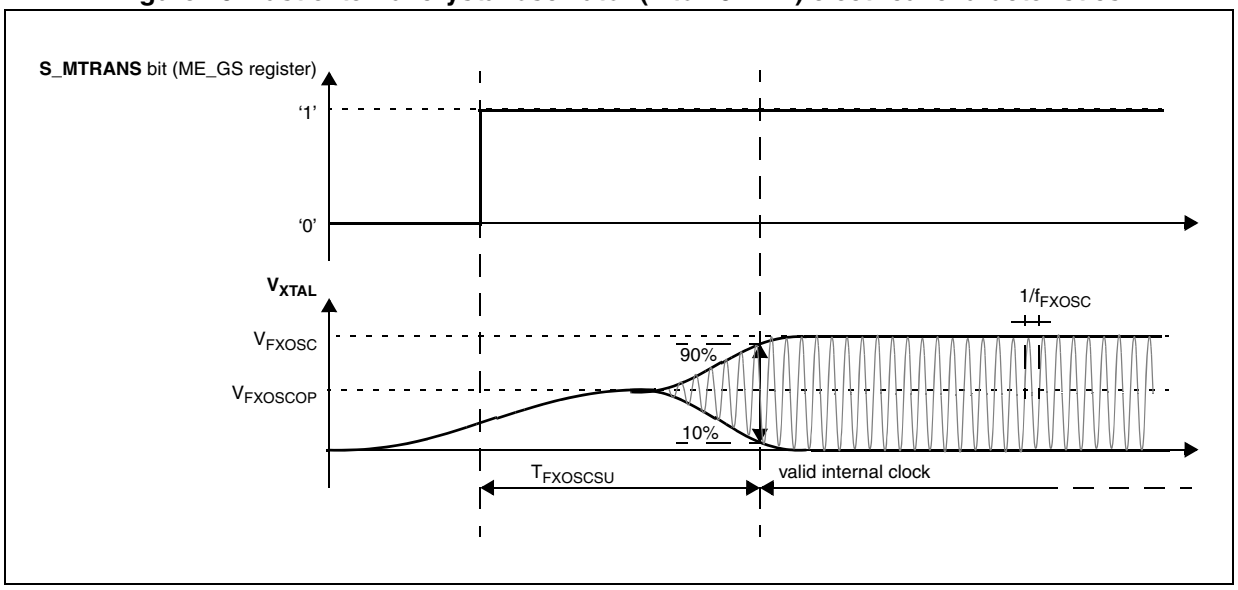


Table 33. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FXOSC}	SR	—	Fast external crystal oscillator frequency	—	4.0	—	16.0	MHz
Δ_{FXOSC}	CC	T	Fast external crystal oscillator frequency duty cycle	—	30	—	70	%
Δt_{FXJIT}	CC	T	Fast external crystal oscillator jitter	—	—	—	TBD	ns
g_{mFXOSC}	CC	C	Fast external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0	2.2	—	8.2	mA/V
	CC	P		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0	2.0	—	7.4	
	CC	C		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1	2.7	—	9.7	
	CC	C		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1	2.5	—	9.2	
V_{FXOSC}	CC	T	Oscillation amplitude at EXTAL	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	1.3	—	—	V
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	1.3	—	—	
$V_{FXOSCOP}$	CC	P	Oscillation operating point	—	—	0.95		V
I_{FXOSC},[3]	CC	T	Fast external crystal oscillator consumption	—	—	2	3	mA
$T_{FXOSCSU}$	CC	T	Fast external crystal oscillator start-up time	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6	ms
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	$0.65V_{DD}$	—	V_{DD}+0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	–0.4	—	$0.35V_{DD}$	V

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals)

4.14 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 34. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[3]	—	4	—	48	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[(3)]	—	40	—	60	%
f_{PLLOUT}	CC	D	FMPLL output clock frequency	—	16	—	48	MHz
f_{VCO}[4]	CC	P	VCO frequency without frequency modulation	—	256	—	512	MHz
			VCO frequency with frequency modulation	—	245.76	—	532.48	
f_{CPU}	SR	—	System clock frequency	—	—	—	48	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	40	100	µs
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} at 48 MHz, 4,000 cycles	—	—	10	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	4	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 All values need to be confirmed during device validation.

3 PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

4 Frequency modulation is considered ±4%.

4.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz fast internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 35. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	
$I_{FIRCRUN}$[3,]	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed	—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C	—	—	10	µA

Table 35. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
$I_{FIRCSTOP}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	500	—	µA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	
T_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	T_A = 55 °C	V_{DD} = 5.0 V ± 10%	—	1.1	2.0	µs
		—			V_{DD} = 3.3 V ± 10%	—	1.2	TBD	
		—		T_A = 125 °C	V_{DD} = 5.0 V ± 10%	—	—	2.0	
		—			V_{DD} = 3.3 V ± 10%	—	—	TBD	
$\Delta_{FIRCPRE}$	CC	C	Fast internal RC oscillator precision after software trimming of f_{FIRC}	T_A = 25 °C		–1	—	1	%
$\Delta_{FIRCTRIM}$	CC	C	Fast internal RC oscillator trimming step	T_A = 25 °C		—	1.6		%
$\Delta_{FIRCVAR}$	CC	C	Fast internal RC oscillator variation in temperature and supply with respect to f_{FIRC} at T_A = 55 °C in high-frequency configuration	—		–5	—	5	%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 All values need to be confirmed during device validation.

3 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.16 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz slow internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 36. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz
	SR	—		—	100	—	150	
I_{SIRC}[3],	CC	C	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA
T_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs

Table 36. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	P	Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at T_A = 55 °C in high frequency configuration	High frequency configuration	–10	—	10	%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 All values need to be confirmed during device validation.

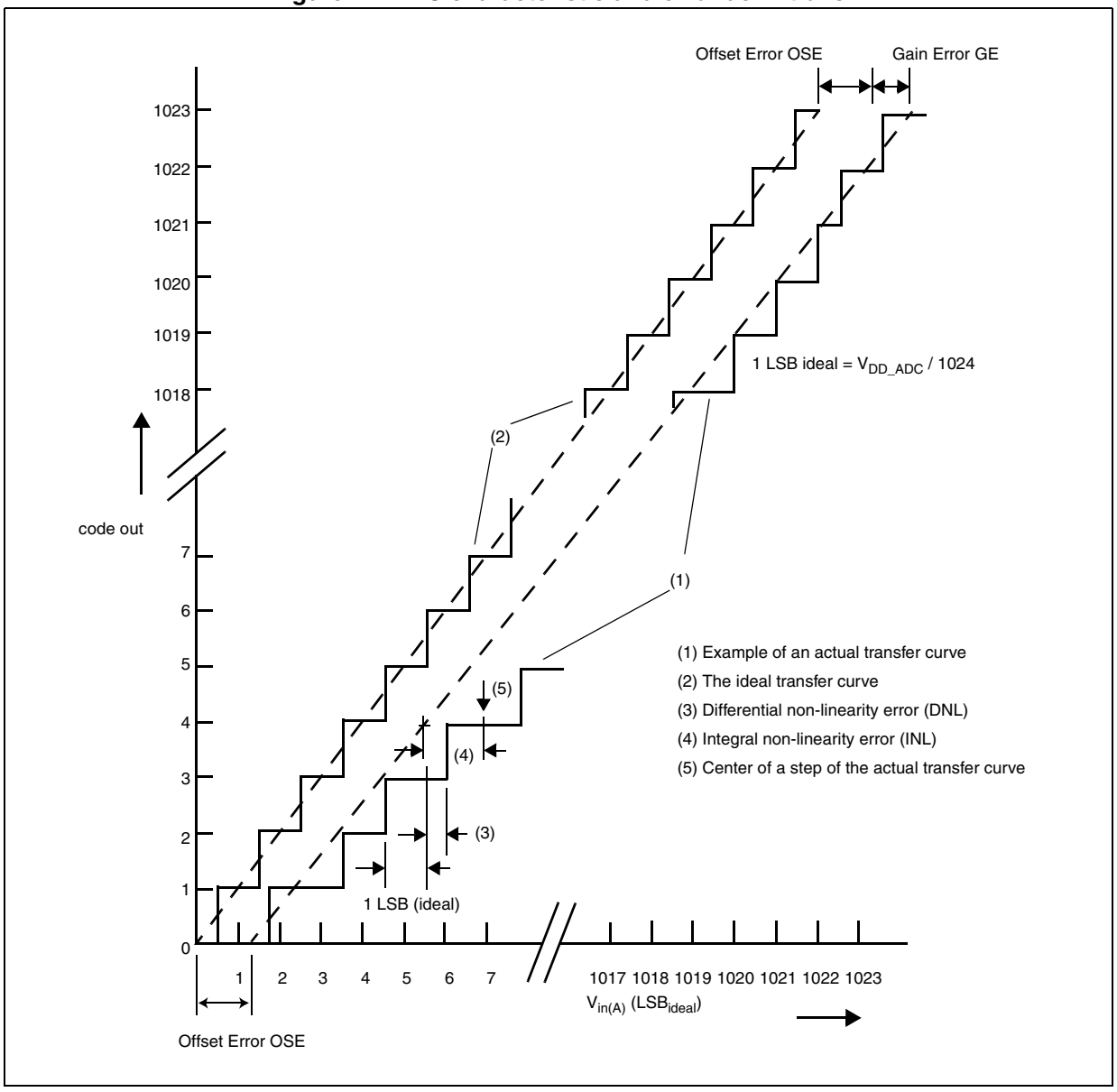
3 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.17 ADC electrical characteristics

4.17.1 Introduction

The device provides a 12-bit Successive Approximation Register (SAR) analog-to-digital converter.

Figure 11. ADC characteristic and error definitions



4.17.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as

possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

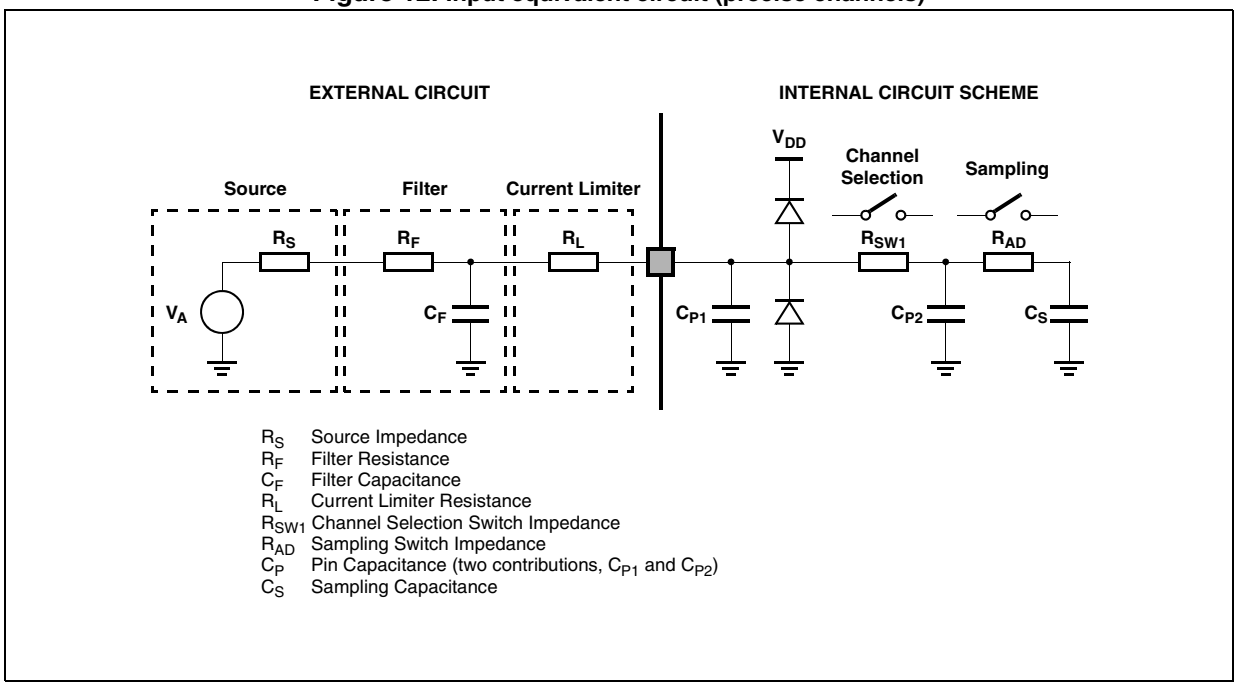
In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_c * C_S)$), where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

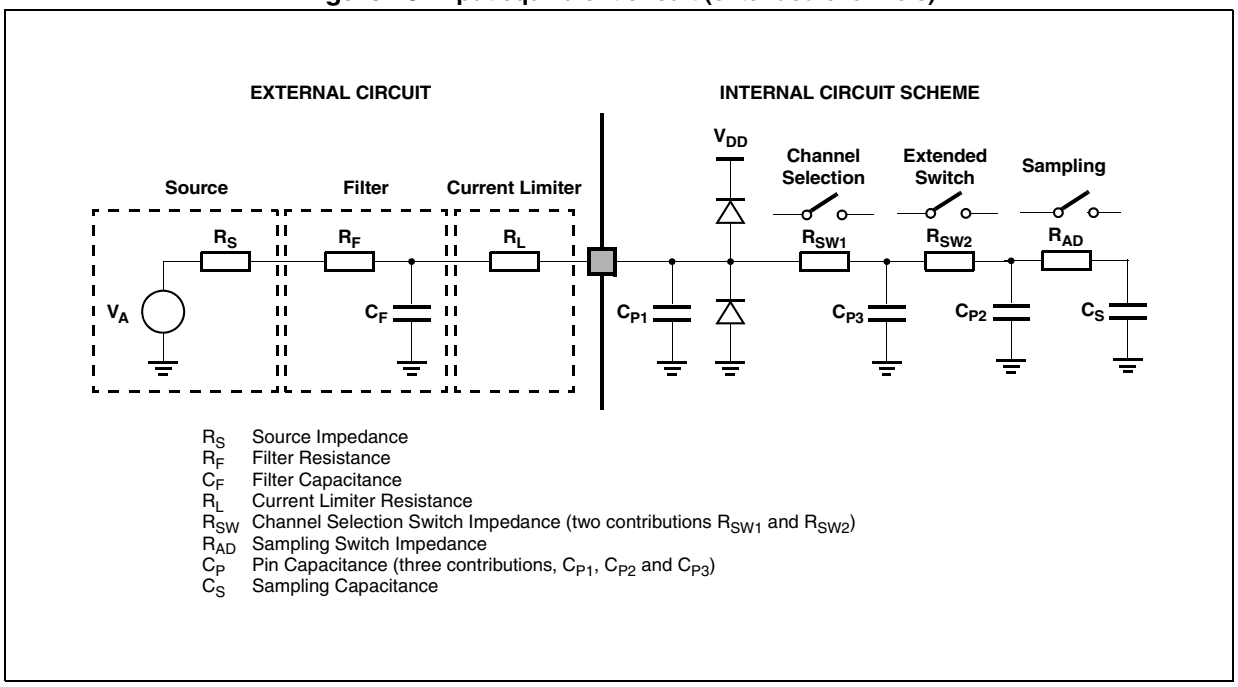
Equation 4 generates a constraint for external network design, in particular on a resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

Figure 12. Input equivalent circuit (precise channels)



R_S Source Impedance
R_F Filter Resistance
C_F Filter Capacitance
R_L Current Limiter Resistance
R_{SW1} Channel Selection Switch Impedance
R_{AD} Sampling Switch Impedance
C_P Pin Capacitance (two contributions, C_{P1} and C_{P2})
C_S Sampling Capacitance

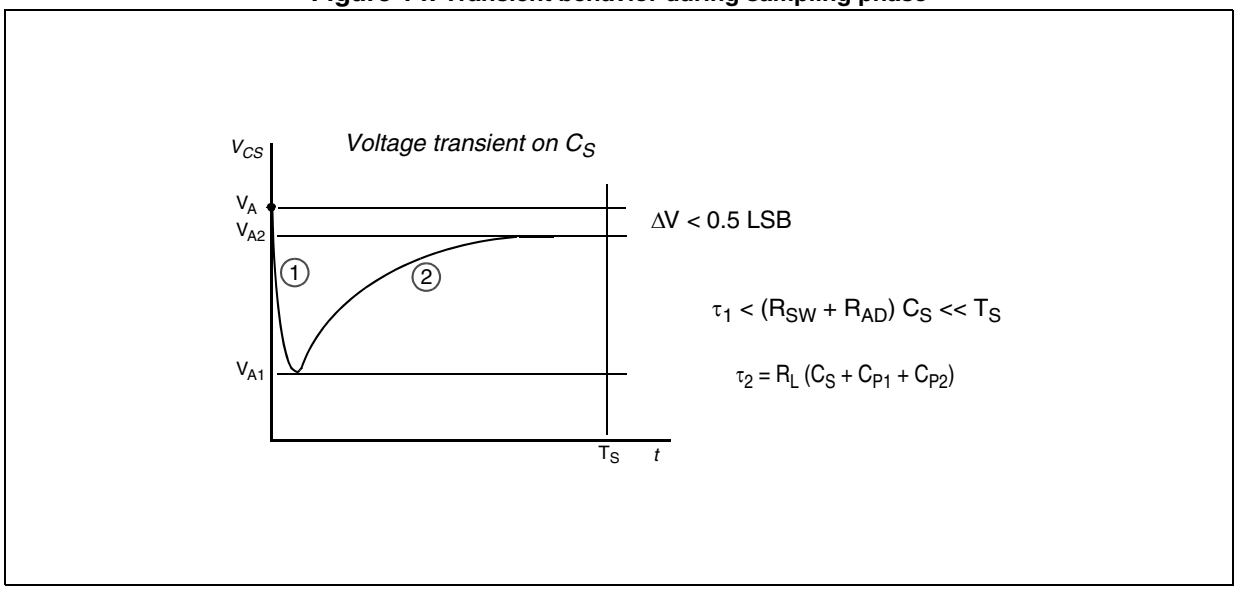
Figure 13. Input equivalent circuit (extended channels)



R_S Source Impedance
R_F Filter Resistance
C_F Filter Capacitance
R_L Current Limiter Resistance
R_{SW} Channel Selection Switch Impedance (two contributions R_{SW1} and R_{SW2})
R_{AD} Sampling Switch Impedance
C_P Pin Capacitance (three contributions, C_{P1}, C_{P2} and C_{P3})
C_S Sampling Capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit in Figure 13): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Figure 14. Transient behavior during sampling phase



In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Eqn. 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

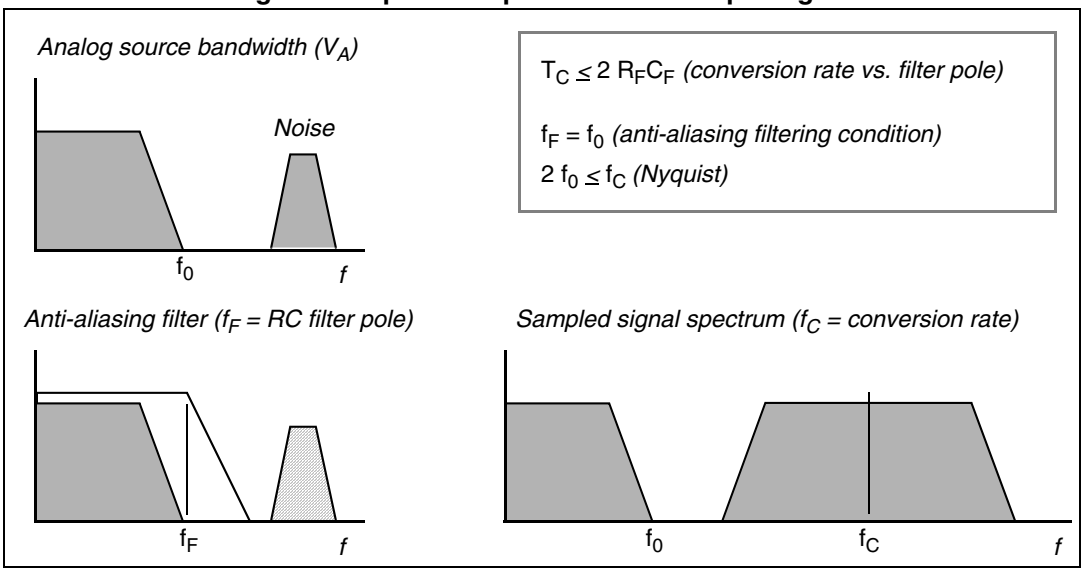
Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

Figure 15. Spectral representation of input signal



Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 12

$$C_F > 2048 \bullet C_S$$

4.17.3 ADC electrical characteristics

Table 37. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	C	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	—	nA
		C		T_A = 25 °C		—	1	—	
		C		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 38. ADC conversion characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC}	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DD_ADC}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC} – 0.1	—	V_{DD_ADC} + 0.1	V
f_{ADC}	SR	—	ADC analog frequency	V_{DD} = 5.0 V	3.33	—	32 + 4%	MHz
				V_{DD} = 3.3 V	3.33	—	20 + 4%	
Δ_{ADC_SYS}	SR	—	ADC clock duty cycle (ipg_clk)	ADCLKSEL = 1[4]	45	—	55	%
t_{ADC_PU}	SR	—	ADC power up delay	—	—	—	1.5	µs

Table 38. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{ADC_S}	CC	T	Sample time[5] V_{DD} = 3.3 V	f_{ADC} = 20 MHz, INPSAMP = 12		600	—	—	ns
		T	Sample time[5] V_{DD} = 5.0 V	f_{ADC} = 32 MHz, INPSAMP = 17		500	—	—	
		T	Sample time[5] V_{DD} = 3.3 V	f_{ADC} = 3.33 MHz, INPSAMP = 255		—	—	76.2	µs
		T	Sample time[5] V_{DD} = 5.0 V	f_{ADC} = 3.33 MHz, INPSAMP = 255		—	—	76.2	
t_{ADC_C}	CC	P	Conversion time[6] V_{DD} = 3.3 V	f_{ADC} = 20 MHz, INPCMP = 0		2.4	—	—	µs
		P	Conversion time[6] V_{DD} = 5.0 V	f_{ADC} = 13.33 MHz, INPCMP = 0		1.5	—	—	µs
		P	Conversion time[6] V_{DD} = 3.3 V	f_{ADC} = 13.33 MHz, INPCMP = 0		—	—	3.6	µs
		P	Conversion time[6] V_{DD} = 5.0 V	f_{ADC} = 32 MHz, INPCMP = 0		—	—	3.6	µs
C_S	CC	D	ADC input sampling capacitance	—		5			pF
C_{P1}	CC	D	ADC input pin capacitance 1	—		3			pF
C_{P2}	CC	D	ADC input pin capacitance 2	—		1			pF
C_{P3}	CC	D	ADC input pin capacitance 3	—		1.5			pF
R_{SW1}	CC	D	Internal resistance of analog source	—		—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—		—	—	0.3	kΩ
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
INLP	CC	T	Absolute Integral non-linearity-precise channels	No overload		—	1	3	LSB
INLX	CC	T	Absolute Integral non-linearity-extended channels	No overload		—	1.5	5	LSB

Table 38. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
DNL	CC	T	Absolute Differential non-linearity	No overload	—	0.5	1	LSB
OFS	CC	T	Absolute Offset error	—	—	2	—	LSB
GNE	CC	T	Absolute Gain error	—	—	2	—	LSB
TUEP[7]	CC	P	Total unadjusted error for precise channels, input only pins	Without current injection	–6		6	LSB
		T		With current injection	–8		8	
TUEX[7]	CC	T	Total unadjusted error for extended channel	Without current injection	–10		10	LSB
		T		With current injection	–12		12	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 Analog and digital V_{SS} **must** be common (to be tied together externally).

3 V_{AINx} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.

4 Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

5 During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.

6 This parameter does not include the sample time t_{ADC_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

7 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

4.18 On-chip peripherals

4.18.1 Current consumption

Table 39. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Value[2] Typ	Unit
$I_{DD\_BV(CAN)}$	CC	T	CAN (FlexCAN) supply current on V_{DD_BV}	500 Kbps	Total (static + dynamic) consumption: • FlexCAN in loop-back mode • XTAL at 8 MHz used as CAN engine clock source • Message sending period is 580 µs	8 * f_{periph} + 85	µA
				125 Kbps		8 * f_{periph} + 27	
$I_{DD\_BV(eMIOS)}$	CC	T	eMIOS supply current on V_{DD_BV}	Static consumption: • eMIOS channel OFF • Global prescaler enabled		29 * f_{periph}	
				Dynamic consumption: • It does not change varying the frequency (0.003 mA)		3	
$I_{DD\_BV(SCI)}$	CC	T	SCI (LINFlex) supply current on V_{DD_BV}	Total (static + dynamic) consumption: • LIN mode • Baudrate: 20 Kbps		5 * f_{periph} + 31	
$I_{DD\_BV(SPI)}$	CC	T	SPI (DSPI) supply current on V_{DD_BV}	Ballast static consumption (only clocked)		1	
				Ballast dynamic consumption (continuous communication): • Baudrate: 2 Mbit • Transmission every 8 µs • Frame: 16 bits		16 * f_{periph}	
$I_{DD\_BV(ADC)}$	CC	T	ADC supply current on V_{DD_BV}	V_{DD} = 5.5 V	Ballast static consumption (no conversion)	41 * f_{periph}	µA
				V_{DD} = 5.5 V	Ballast dynamic consumption (continuous conversion)[3]	5 * f_{periph}	
$I_{DD\_HV\_ADC(ADC)}$	CC	T	ADC supply current on $V_{DD\_HV\_ADC}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	2 * f_{periph}	
				V_{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	75 * f_{periph} + 32	
$I_{DD\_HV(FLASH)}$	CC	T	CFlash + DFlash supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	TBD	
$I_{DD\_HV(PLL)}$	CC	T	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	30 * f_{periph}	

1 Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 48 MHz

2 f_{periph} is in absolute value.

3 During the conversion, the total current consumption is given from the sum of the static and dynamic consumption, i.e., (41 + 5) * f_{periph}

4.18.2 DSPI characteristics

Table 40. DSPI characteristics[1]

No.	Symbol		C	Parameter		DSPI0/DSPI1			Unit
						Min	Typ	Max	
1	t_{SCK}	SR	D	SCK cycle time	Master mode (MTFE = 0)	125	—	—	ns
			D		Slave mode (MTFE = 0)	125	—	—	
			D		Master mode (MTFE = 1)	83	—	—	
			D		Slave mode (MTFE = 1)	83	—	—	
—	f_{DSPI}	SR	D	DSPI digital controller frequency		—	—	f_{CPU}	MHz
—	Δt_{CSC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode	Master mode	—	—	130[2]	ns
—	Δt_{ASC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1→1	Master mode	—	—	130(2)	ns
2	t_{CSCext}[3]	SR	D	CS to SCK delay	Slave mode	32	—	—	ns
3	t_{ASCext}[4]	SR	D	After SCK delay	Slave mode	$1/f_{DSPI} + 5$	—	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	Master mode	—	$t_{SCK}/2$	—	ns
		SR	D		Slave mode	$t_{SCK}/2$	—	—	
5	t_A	SR	D	Slave access time	—	$1/f_{DSPI} + 70$	—	—	ns
6	t_{DI}	SR	D	Slave SOUT disable time	—	7	—	—	ns
9	t_{SUI}	SR	D	Data setup time for inputs	Master mode	43	—	—	ns
					Slave mode	5	—	—	
10	t_{HI}	SR	D	Data hold time for inputs	Master mode	0	—	—	ns
					Slave mode	2[5]	—	—	
11	t_{SUO}[6]	CC	D	Data valid after SCK edge	Master mode	—	—	32	ns
					Slave mode	—	—	52	
12	t_{HO}(6)	CC	D	Data hold time for outputs	Master mode	0	—	—	ns
					Slave mode	8	—	—	

1 Operating conditions: C_{OUT} = 10 to 50 pF, $Slew_{IN}$ = 3.5 to 15 ns.

2 Maximum is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM pad.

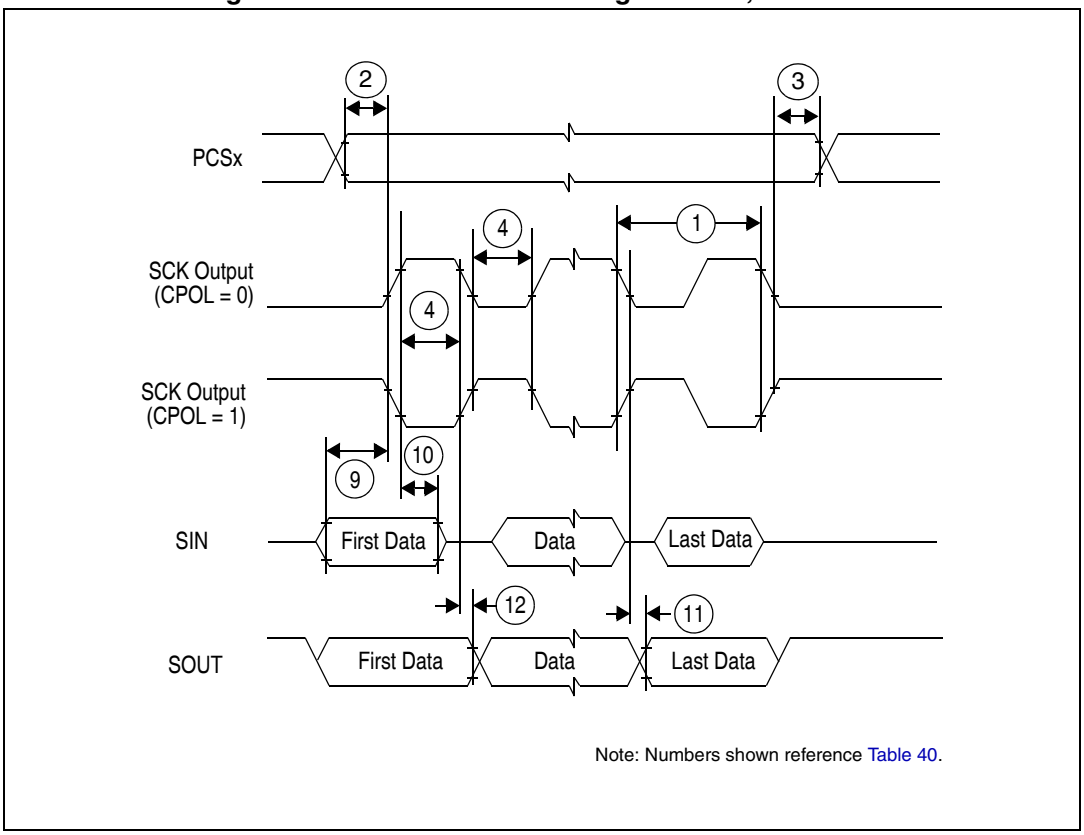
3 The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext}.

4 The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext}.

5 This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR register.

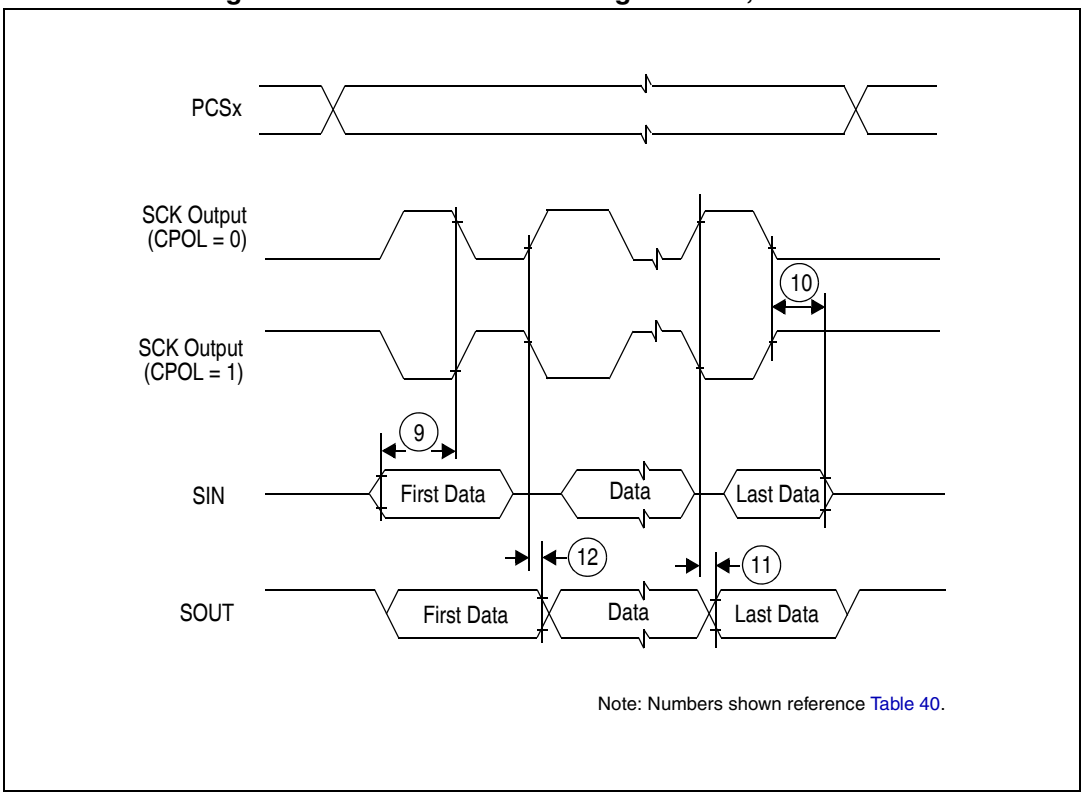
6 SCK and SOUT configured as MEDIUM pad

Figure 16. DSPI classic SPI timing – master, CPHA = 0



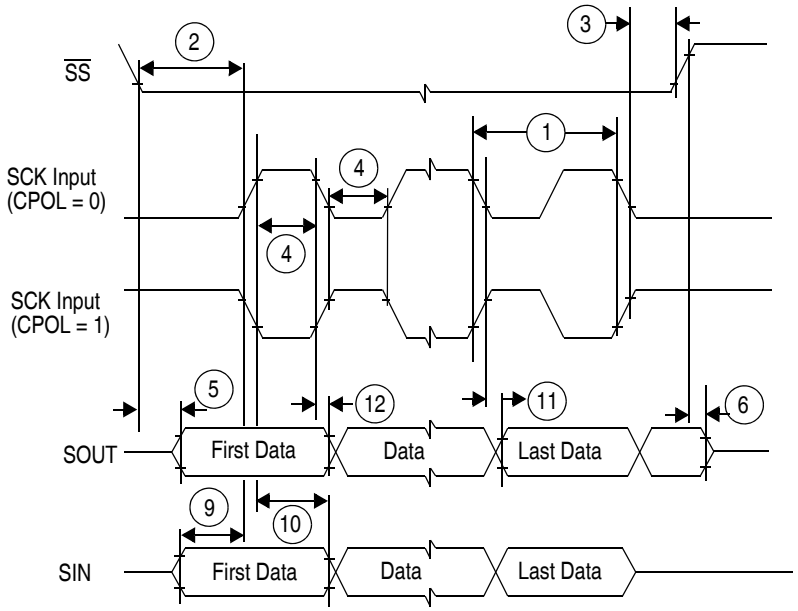
Note: Numbers shown reference Table 40.

Figure 17. DSPI classic SPI timing – master, CPHA = 1



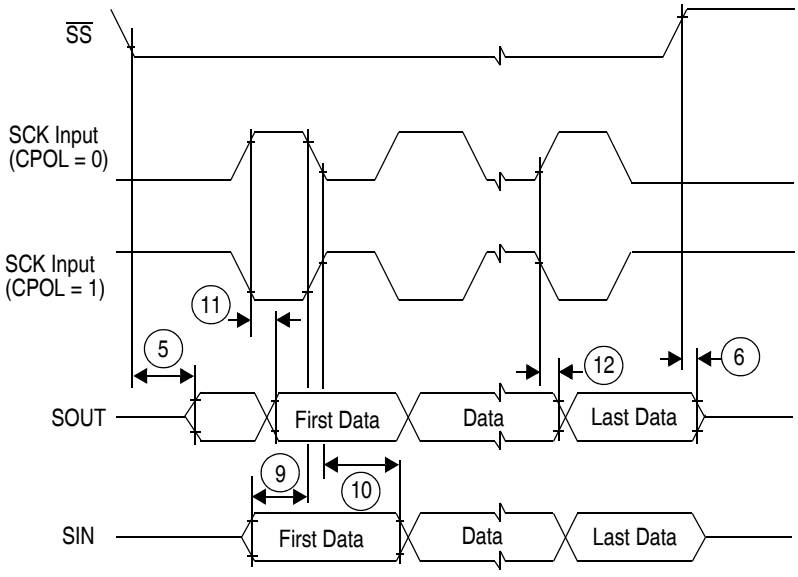
Note: Numbers shown reference Table 40.

Figure 18. DSPI classic SPI timing – slave, CPHA = 0



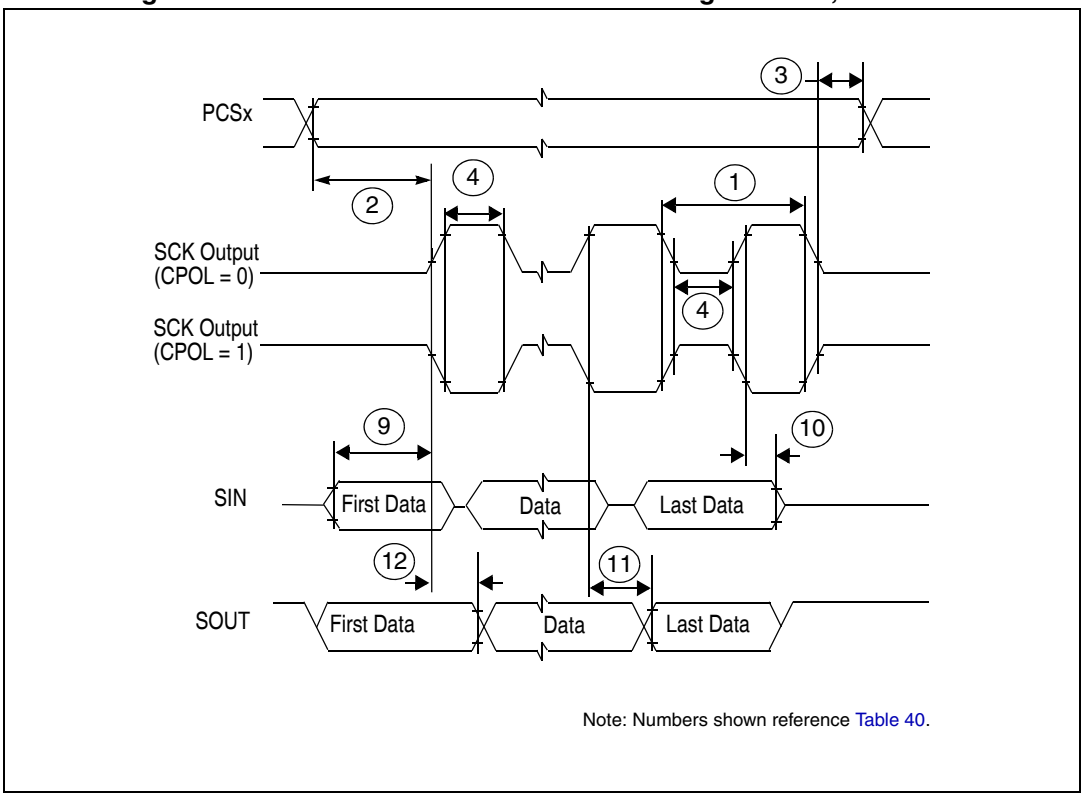
Note: Numbers shown reference Table 40.

Figure 19. DSPI classic SPI timing – slave, CPHA = 1



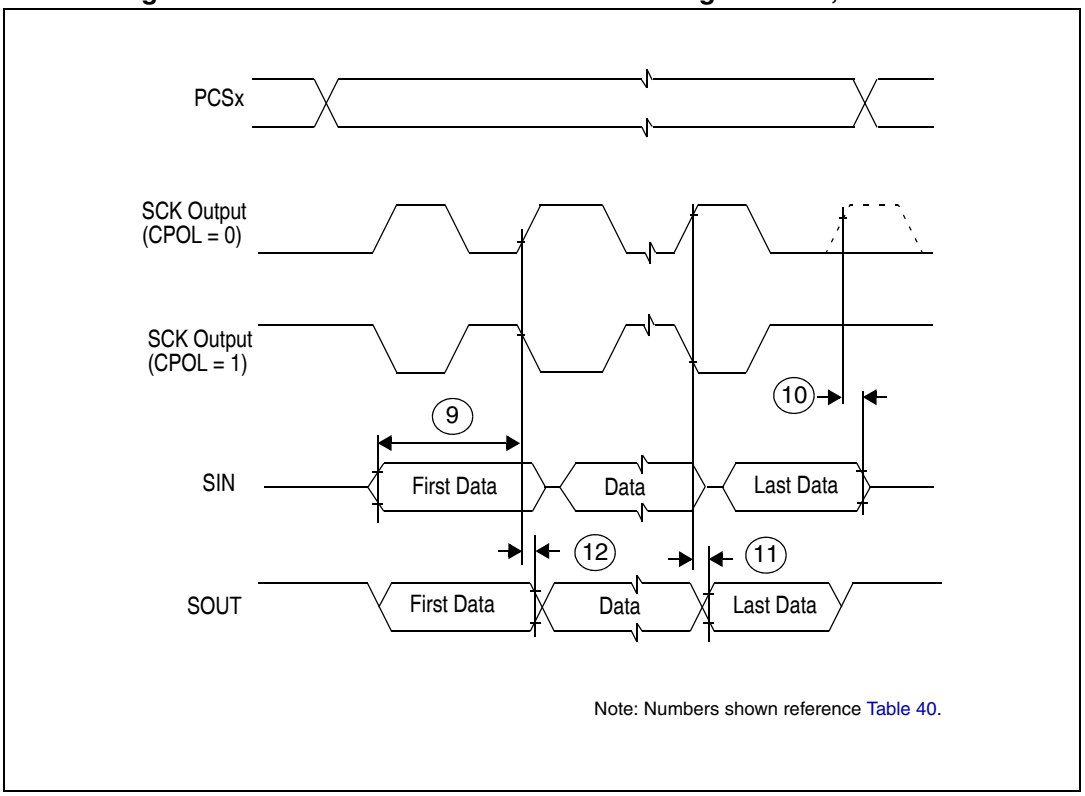
Note: Numbers shown reference Table 40.

Figure 20. DSPI modified transfer format timing – master, CPHA = 0



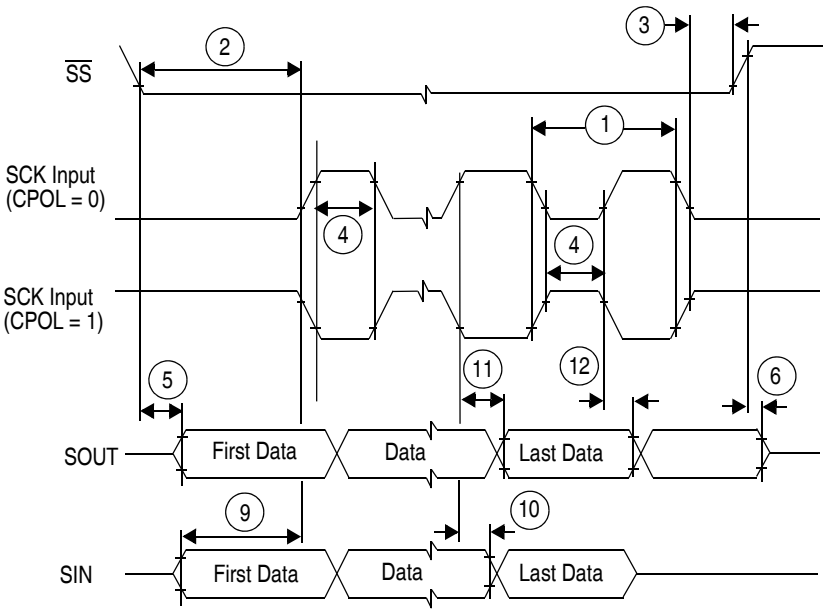
Note: Numbers shown reference Table 40.

Figure 21. DSPI modified transfer format timing – master, CPHA = 1



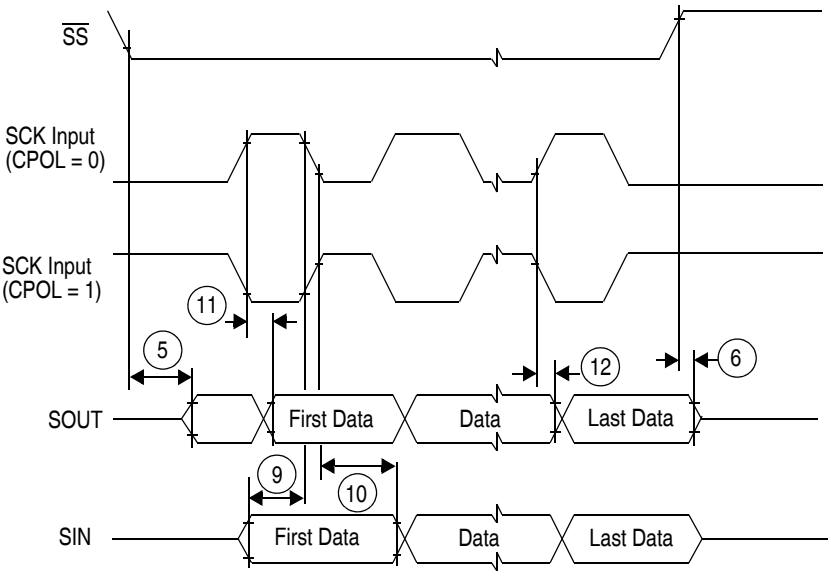
Note: Numbers shown reference Table 40.

Figure 22. DSPI modified transfer format timing – slave, CPHA = 0



Note: Numbers shown reference Table 40.

Figure 23. DSPI modified transfer format timing – slave, CPHA = 1



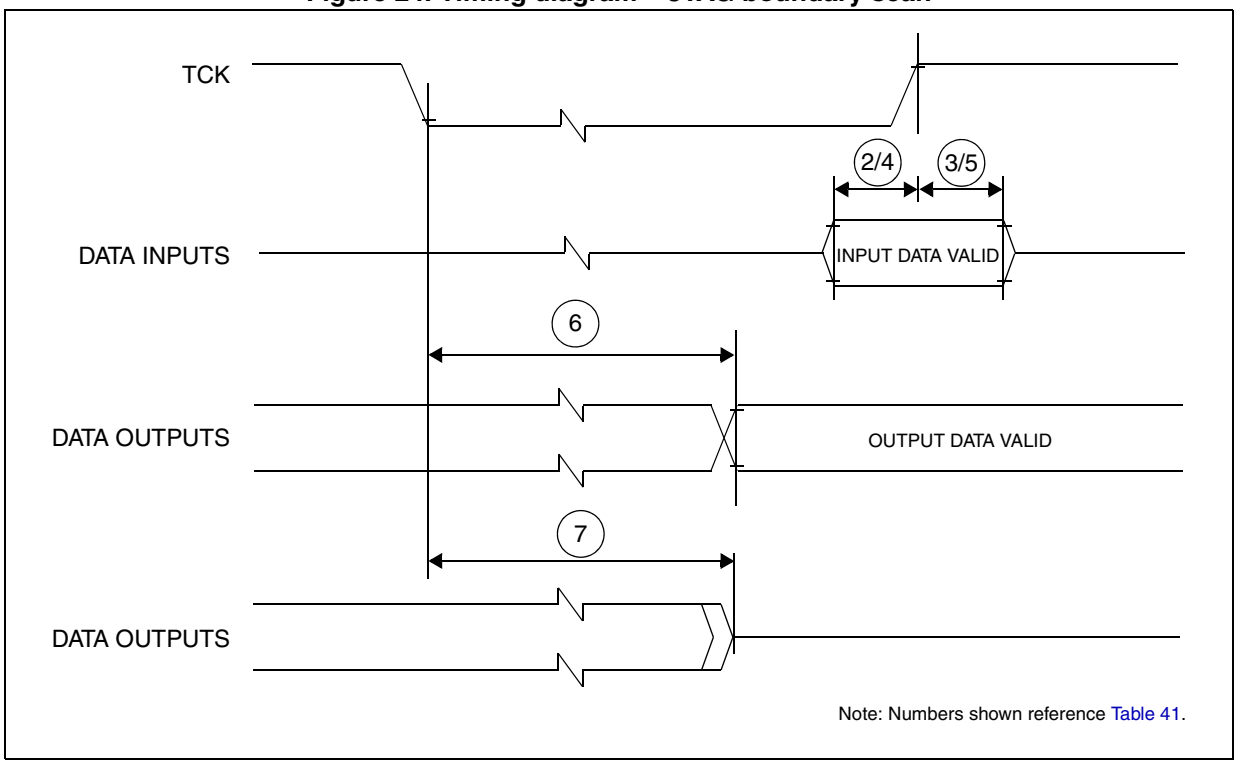
Note: Numbers shown reference Table 40.

4.18.3 JTAG characteristics

Table 41. JTAG characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{JCYC}	CC	D	TCK cycle time	83.33	—	—	ns
2	t_{TDIS}	CC	D	TDI setup time	15	—	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	—	ns
4	t_{TMSS}	CC	D	TMS setup time	15	—	—	ns
5	t_{TMSH}	CC	D	TMS hold time	5	—	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO valid	—	—	49	ns
7	t_{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns

Figure 24. Timing diagram – JTAG boundary scan



5 Package characteristics

5.1 Package mechanical data

5.1.1 100 LQFP mechanical outline drawing

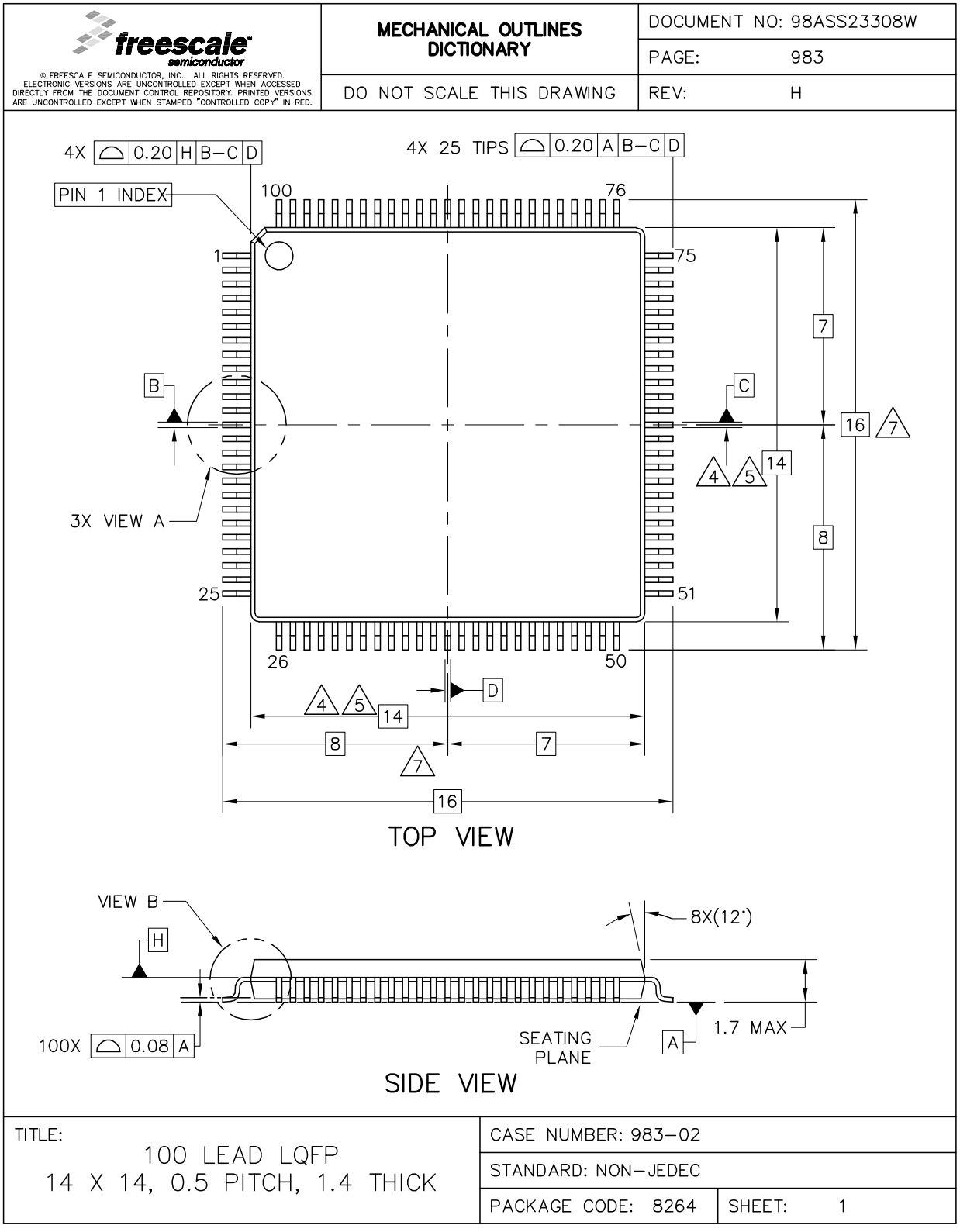


Figure 25. 100 LQFP package mechanical drawing (part 1 of 3)

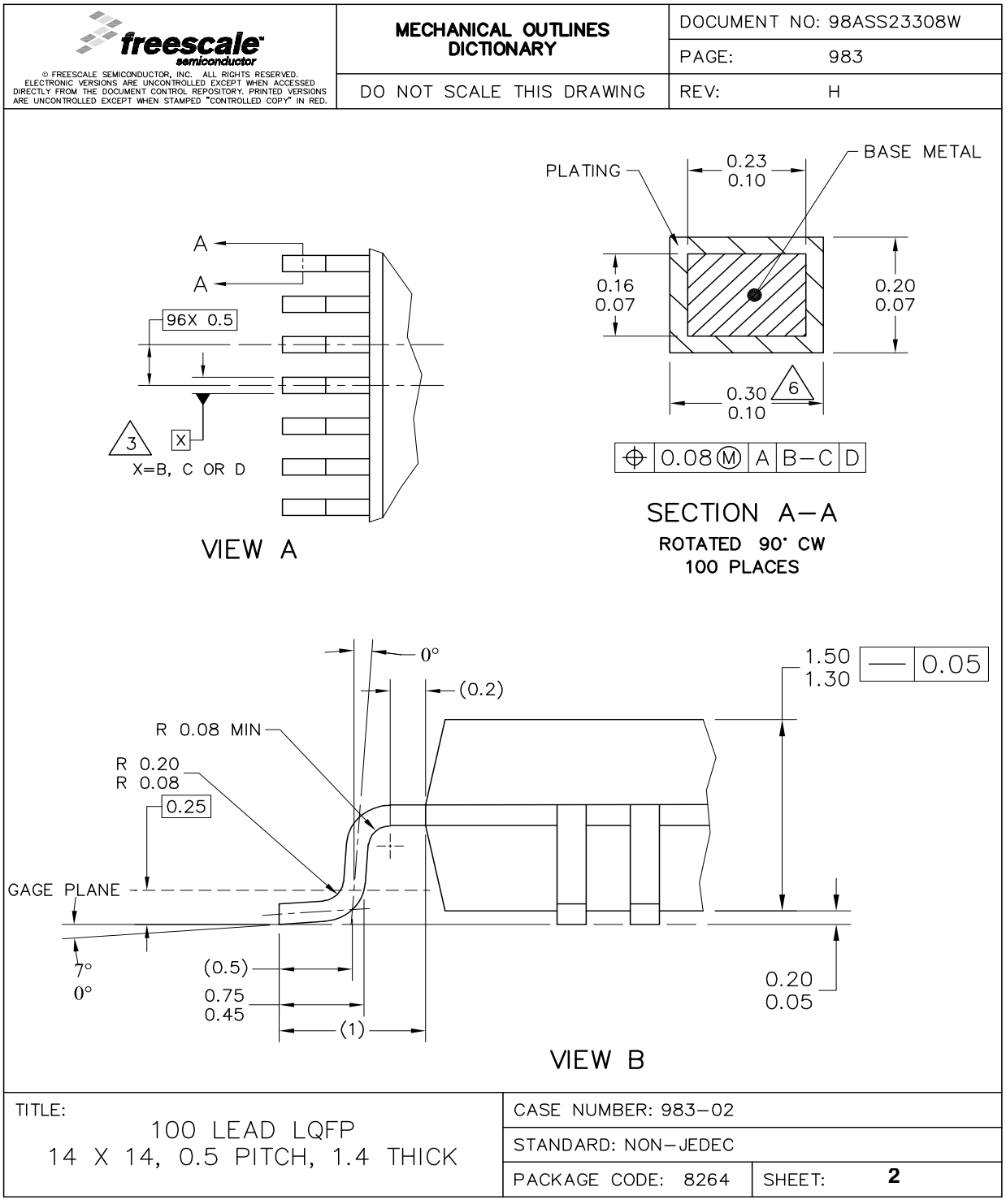
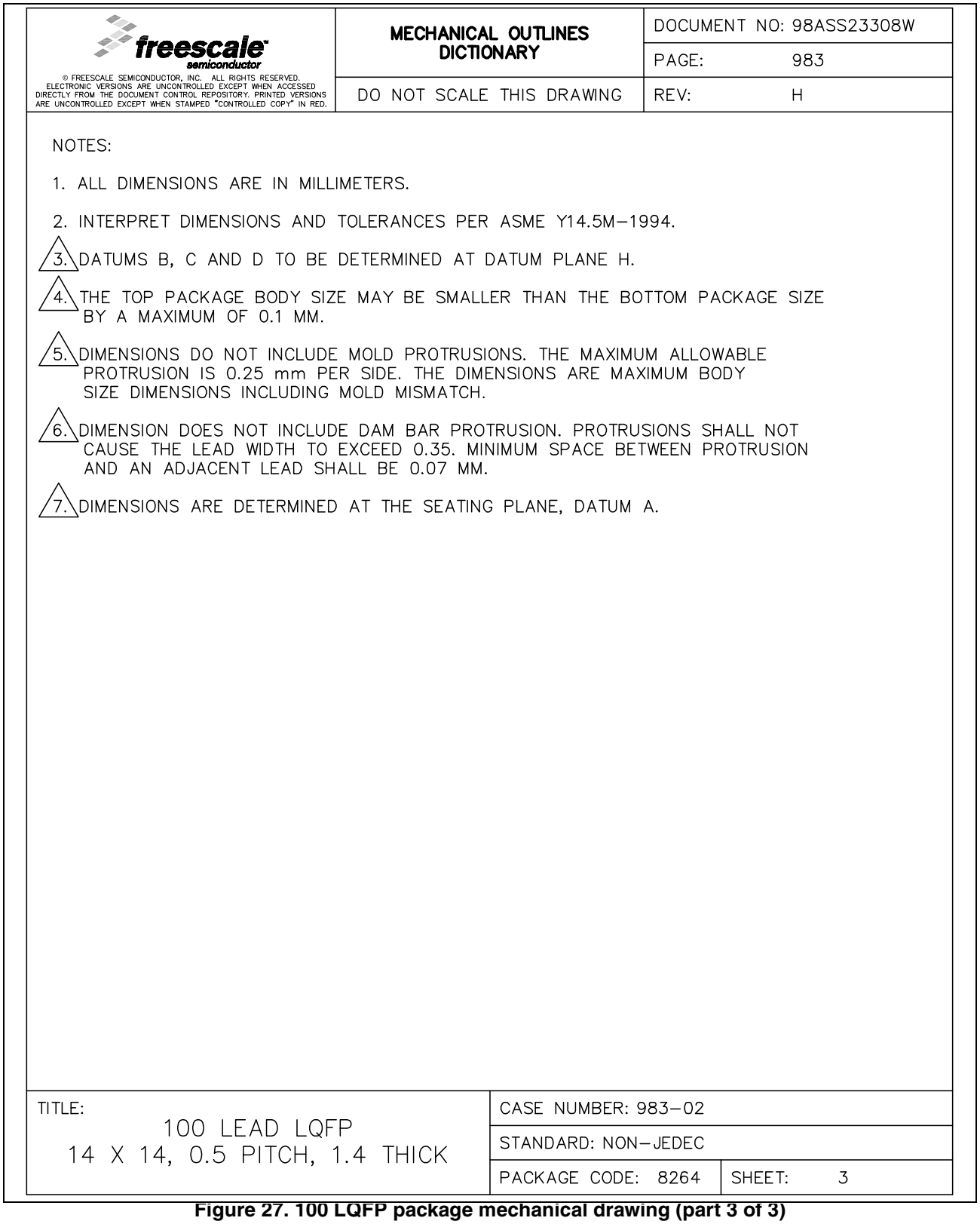


Figure 26. 100 LQFP package mechanical drawing (part 2 of 3)



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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.

5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

TITLE:
100 LEAD LQFP
14 X 14, 0.5 PITCH, 1.4 THICK

CASE NUMBER: 983–02

STANDARD: NON–JEDEC

PACKAGE CODE: 8264

SHEET: 3

Figure 27. 100 LQFP package mechanical drawing (part 3 of 3)

5.1.2 64 LQFP mechanical outline drawing

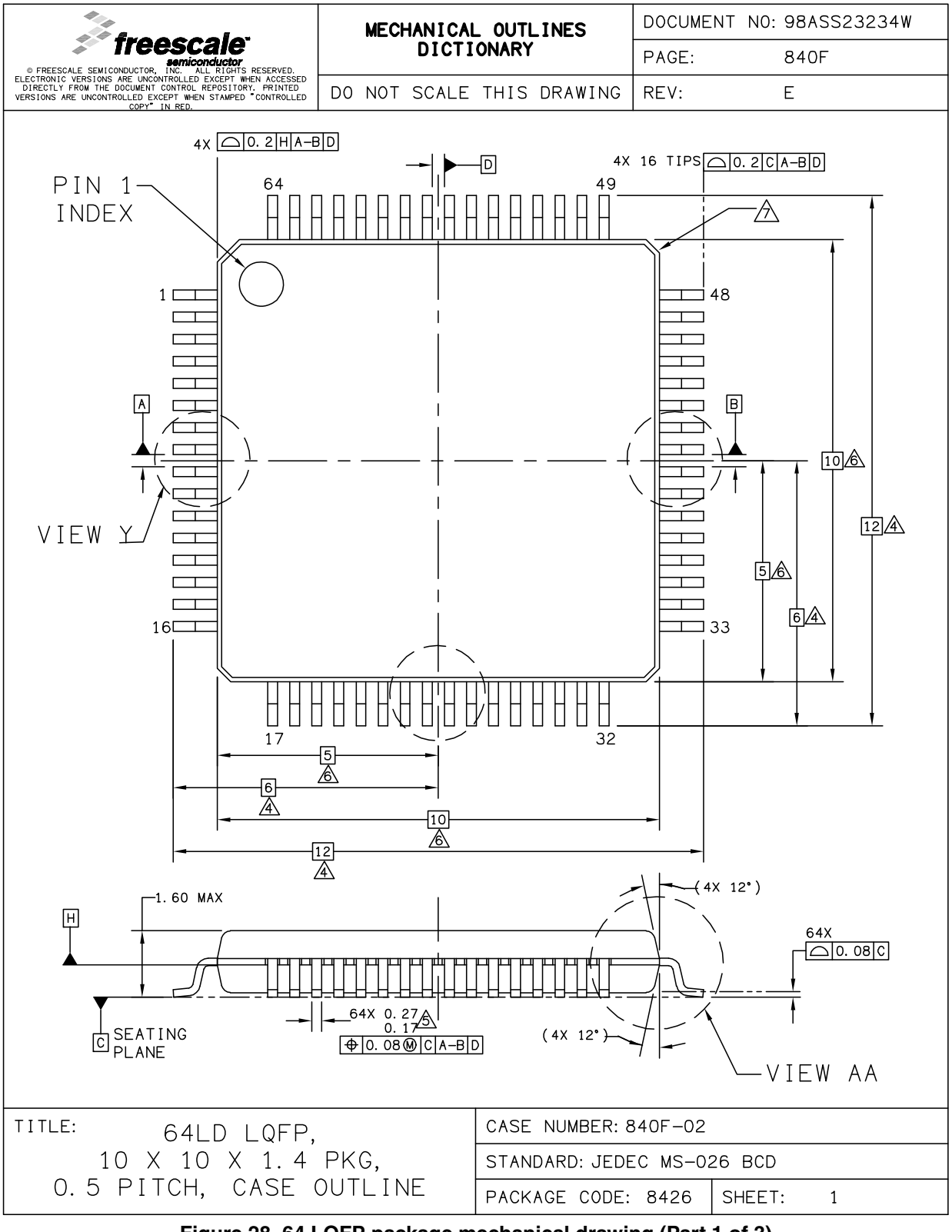

Figure 28. 64 LQFP package mechanical drawing (Part 1 of 3)

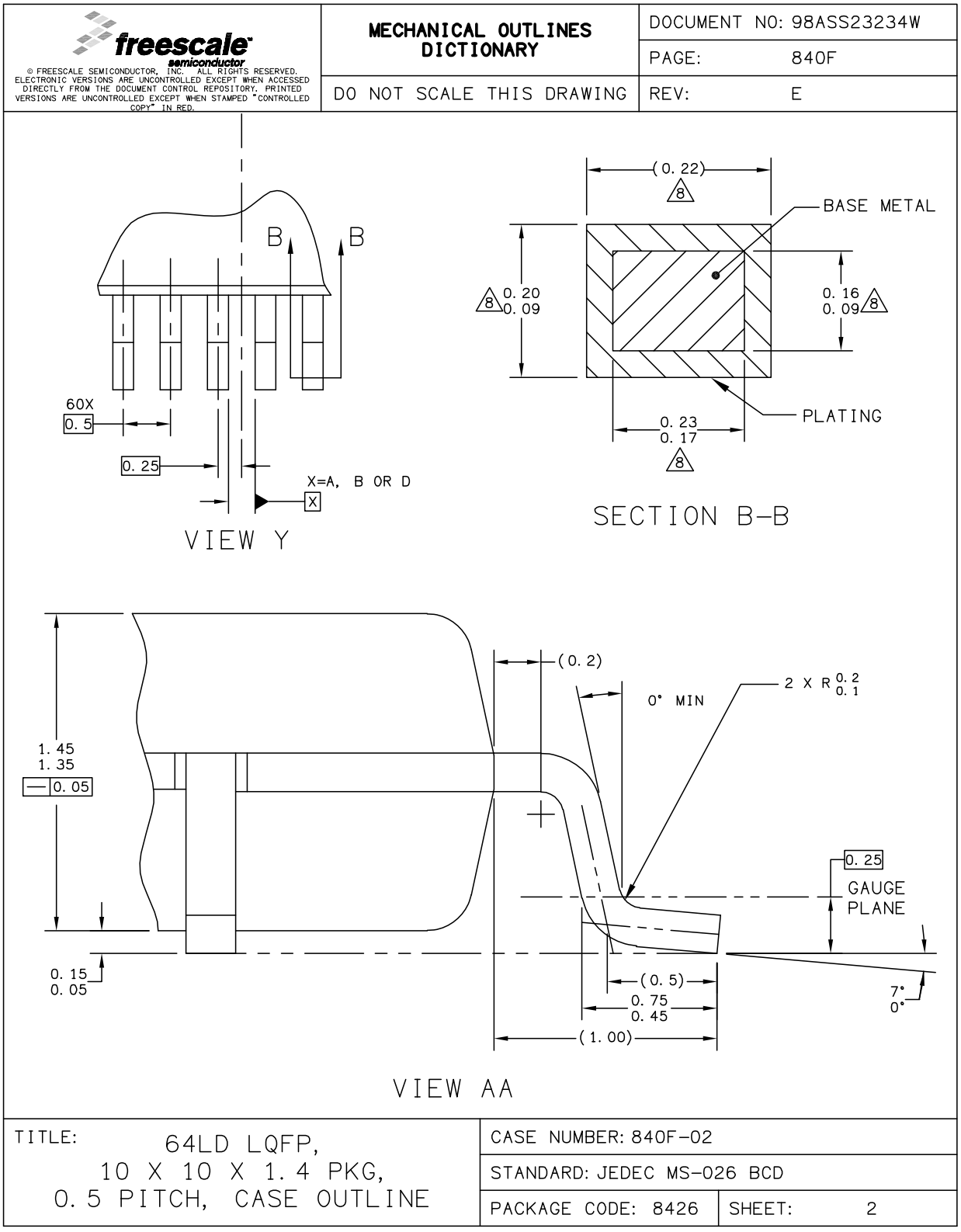

Figure 29. 64 LQFP package mechanical drawing (Part 2 of 3)

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		PAGE: 840F
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NOTES:

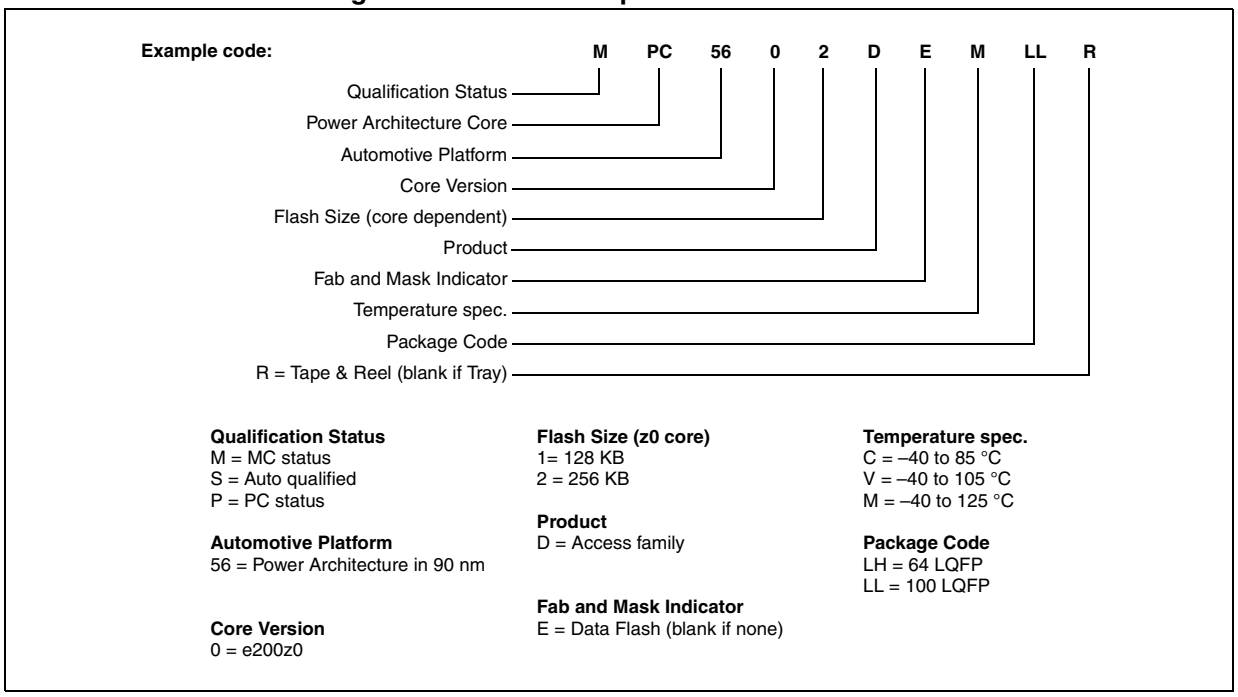
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 3

Figure 30. 64 LQFP package mechanical drawing (Part 3 of 3)

6 Ordering information

Figure 31. Commercial product code structure



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