Freescale Semiconductor
Data Sheet: Advance Information

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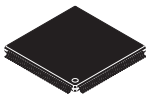
MPC5604P



144 LQFP
20 mm x 20 mm

100 LQFP
14 mm x 14 mm

MPC5604P Microcontroller Data Sheet

- Single issue, 32-bit Power Architecture™ CPU core complex (e200z0h) with Harvard architecture
- Up to 512 KB on-chip code flash memory with ECC plus 64 KB on-chip data flash with ECC
- Up to 40 KB SRAM on-chip with ECC
- Interrupt controller (INTC) capable of handling 144 selectable-priority interrupt sources
- Up to two FMPLL modules
- Clock Monitor Unit (CMU) to monitor the integrity of the main crystal oscillator and the PLL and act as a frequency meter, measuring the frequency of one clock source and comparing it to a reference clock
- 16 MHz internal RC Oscillator (RCOSC) (trimmable)
- Periodic Interrupt Timer (PIT) includes four timer channels with 32-bit counter resolution
- Windowed software watchdog (SWT)
- Output compare system timer (STM) to support AUTOSAR task protection
- Crossbar switch (XBAR) architecture for concurrent access to peripherals, flash memory or RAM from multiple bus masters (AMBA 2.0 v6 AHB)
- 16-channel Enhanced Direct Memory Access (eDMA) controller with multiple transfer request sources using DMA MUX
- System Integration Unit (SIU) Lite; controls the GPIO mode of the pads, the pads alternate function, and the pads configuration
- Boot assist module (BAM) supports downloading operation to internal SRAM via serial link (FlexCAN or LINFlex or FlexRay)
- FlexPWM motor control PWM module (1 x 8 PWM channels)
- Two enhanced eTimer timer modules (six channels each) with dedicated motor control and quadrature decode features integrated
- Embedded junction temperature sensor
- Safety Port to support functional safety architectures on the ECU level. Can be optionally used as a second FlexCAN module with 32 message buffers.
- Two independent 10-bit analog-to-digital converters (ADCs) with a conversion time target of 700 ns for the analog section. Each converter supports 16 channels (ADC0: channel 15 dedicated to the Temperature sensor; ADC1: channel 15 for the internal 1.2 V rail; channels 11 to 14 shared between the two converters)
- FlexPWM to ADC and eTimer Cross Triggering Unit (CTU)
- Fault Collection Unit (FCU) for functional safety
- Four Serial Peripheral Interface (DSPI) modules
- Two Serial Communication Interface (LINFlex) modules with LIN support
- FlexCAN Controller Area Network module with 32 message buffers
- Dual channel FlexRay™ Controller with 32 message buffers (512 KB device only)
- GPIO
  - 144-pin package: 82 general-purpose pins supporting input/output operations plus 26 general-purpose pins supporting input operations (108 in total). Out of these 108 pins, 32 have external interrupt capability.
  - 100-pin package: 51 general-purpose pins supporting input/output operations plus 16 general-purpose pins supporting input operations (67 in total). Out of these 67 pins, 25 have external interrupt capability.
  - Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard Class 2+
  - JTAG (IEEE 1149.1) 4-pin interface
- Voltage regulator (VREG) for regulation into 3.3 V - 5 V input down to 1.2 V nominal core logic level with external transistor

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

Preliminary—Subject to Change Without Notice

Table of Contents

1 Overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5604P series of microcontroller units (MCUs). For functional characteristics, refer to the *MPC5604P Microcontroller Reference Manual.*

MPC5604P microcontrollers are members of a new family of next generation microcontrollers built on the Power Architecture™. This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

The MPC5604P family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address electrical hydraulic power steering (EHPS), electric power steering (EPS) and airbag applications. The advanced and cost-efficient host processor core of the MPC5604P automotive controller family complies with the Power Architecture embedded category, which is 100 percent user-mode compatible with the original PowerPC user instruction set architecture (UISA). It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.1 Device Comparison

Table 1 provides a summary of different members of the MPC5604P family and their features to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 1. MPC5604P Device Comparison

Feature	MPC5602P	MPC5603P	MPC5604P
Code flash memory (ECC)	256 KB	384 KB	512 KB
Data flash memory (ECC)	64 KB (4 × 16 KB blocks)		
RAM (ECC)	20 KB	36 KB	40 KB
Processor core	32-bit e200z0h		
Instruction set	VLE		
CPU performance	0 MHz - 64 MHz		
FMPLL (frequency-modulated phase-locked loop) modules	1	2	2
INTC (interrupt controller) channels	100	144	144
PIT (periodic interrupt timer)	1 (includes 4 32-bit timers)		
Enhanced DMA (direct memory access) channels	16		
FlexRay	—	Yes[1]	
FlexCAN (controller area network)	2[2,3]		
FCU (fault collection unit)	Yes		
CTU (cross triggering unit)	Yes		
eTimer channels	2 × 6		
FlexPWM (pulse-width modulation) channels	8		
Analog-to-digital converters (ADC)	2 10-bit ADCs 26 (2 x13) channels on LQFP144 pkg 16 (2 x8) channels on LQFP100 pkg		

Table 1. MPC5604P Device Comparison (continued)

Feature		MPC5602P	MPC5603P	MPC5604P
LINFlex modules		2		
DSPI (deserial serial peripheral interface) modules		3	4	
CRC (cyclic redundancy check) unit		Yes		
Junction temperature sensor		Yes		
JTAG interface		Yes		
Nexus port controller (NPC)		Yes (Level 1+)	Yes (Level 2+)	
Supply	Digital power supply[4]	3.3 V or 5 V single supply with external transistor		
	Analog power supply	3.3 V or 5 V		
	Internal RC oscillator	16 MHz		
	External crystal oscillator	4 MHz - 40 MHz		
Packages		100 LQFP	100 LQFP 144 LQFP	
Temperature	Standard ambient temperature	-40 to 125 °C		
	Extended ambient temperature[5]	-40 to 145 °C		

1 32 message buffers, dual-channel

2 Each FlexCAN module has 32 message buffers

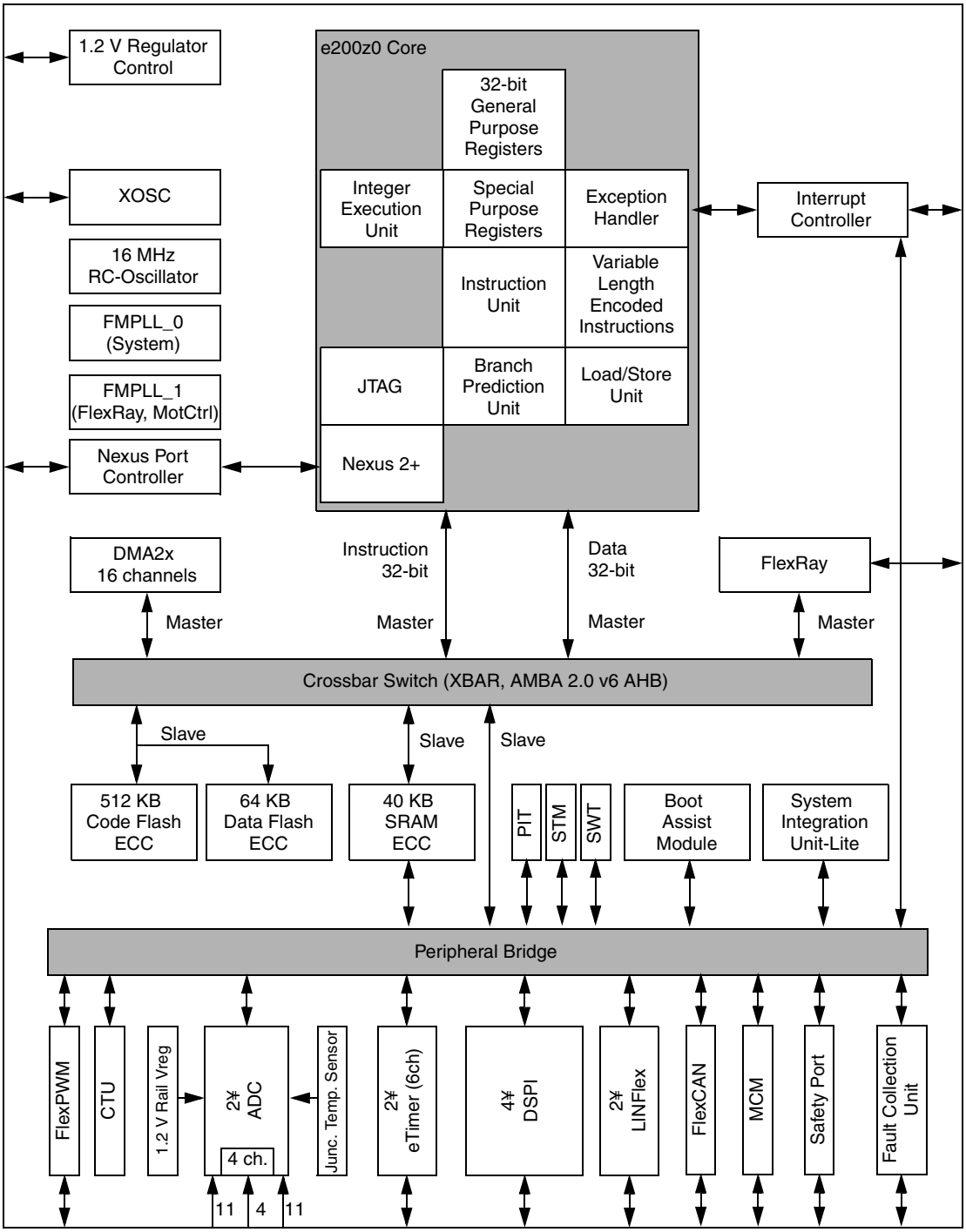
3 One FlexCAN module can act as a Safety Port with a data rate of up to 7.5 MHz

4 A given orderable part can be software-configured for either 3 V or 5 V operation.

5 Thermally enhanced 100-pin and 144-pin LQFP packages are under analysis to support an extended ambient temperature range of -40 to 145 °C. The packages are not yet available.

1.2 Block Diagram

Figure 1 shows a top-level block diagram of the MPC5604P MCU.



CANController Area Network (FlexCAN)
DSPIDeserial Serial Peripheral Interface
LINFlexSerial Communication Interface (LIN support)
FMPLLFrequency-Modulated Phase-Locked Loop
SRAMStatic Random-Access Memory
FlexPWMFlexible Pulse Width Modulation
eTimerEnhanced Timer
PITPeriodic Interrupt Timer
SWTSoftware Watchdog Timer
STMSystem Timer Module

Figure 1. MPC5604P block diagram

2 Package Pinouts and Signal Descriptions

2.1 Package Pinouts

The LQFP pinouts are shown in the following figures.

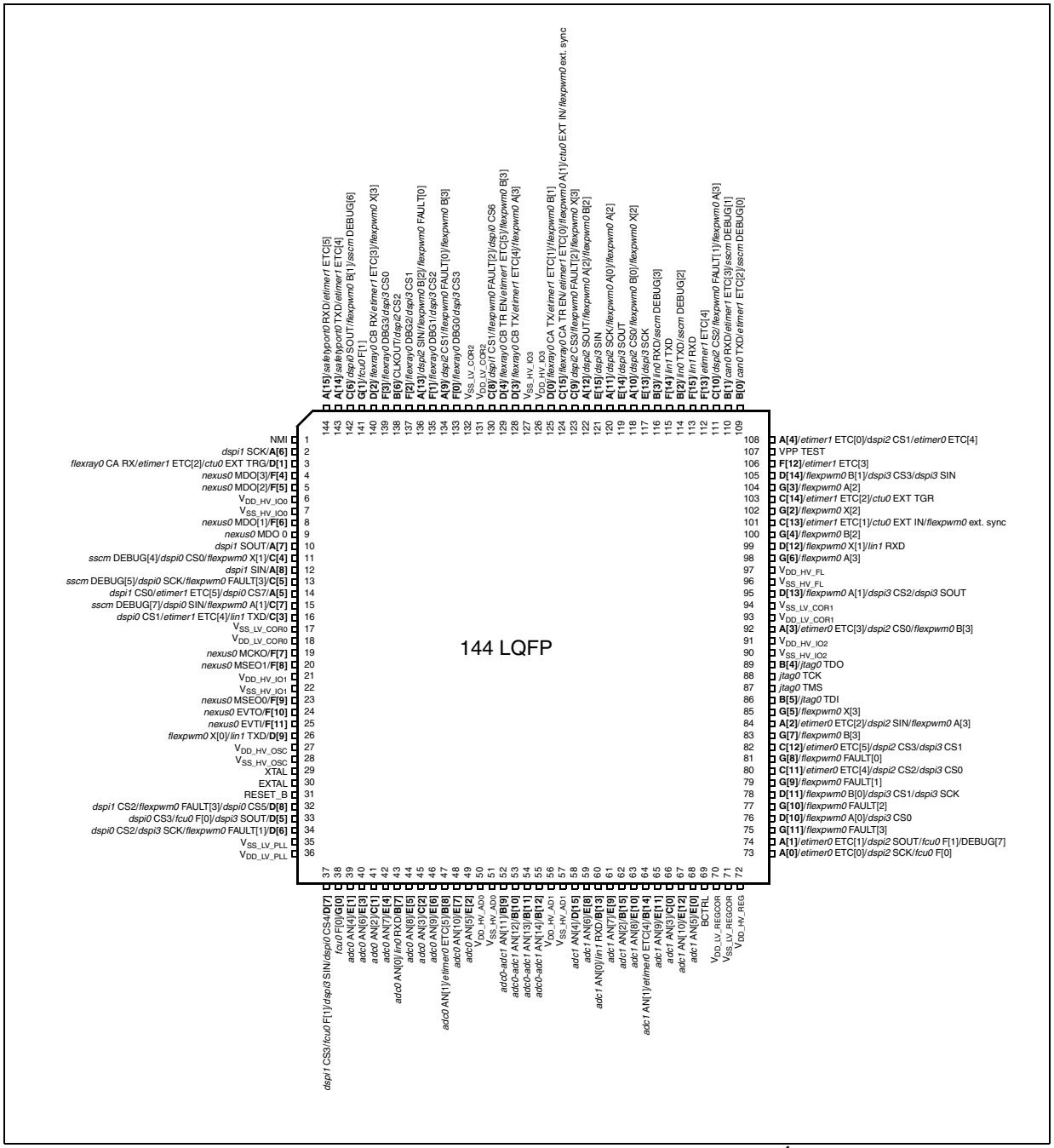


Figure 2. LQFP 144-pin Configuration (top view)[1]

1. Availability of port pin alternate functions depends on product selection

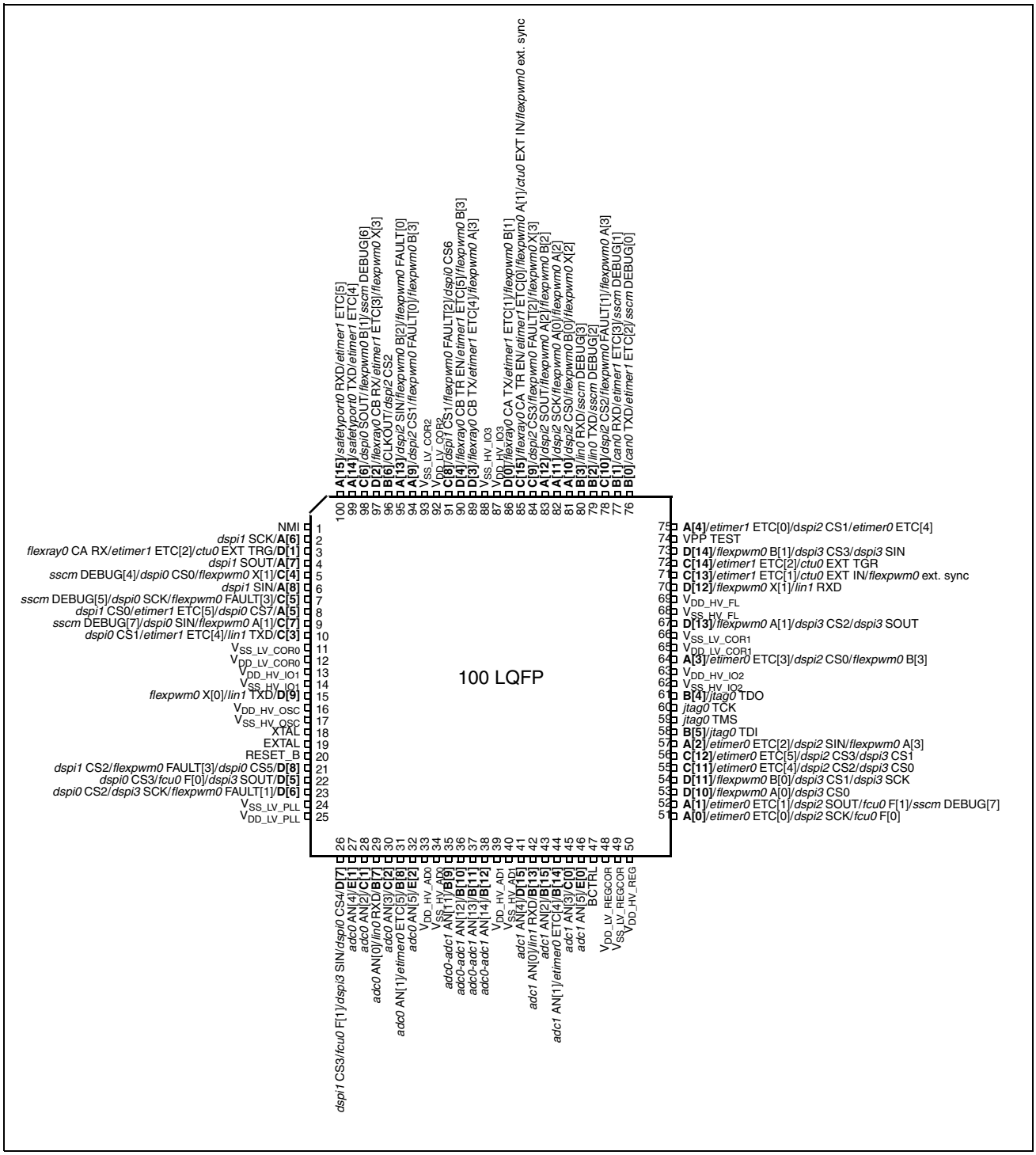


Figure 3. LQFP 100-pin Configuration (top view)[1]

1. Availability of port pin alternate functions depends on product selection

2.2 Pin Descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the MPC5604P devices.

2.2.1 Power Supply and Reference Voltage Pins

Table 2 lists the power supply and reference voltage for the MPC5604P devices.

Table 2. Supply Pins

Supply		Pin	
Symbol	**Description**	**100-pin**	**144-pin**
VREG control and power supply pins. Pins available on 100-pin and 144-pin package.			
BCTRL	Voltage Regulator external NPN Ballast base control pin	47	69
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	50	72
$V_{DD\_LV\_REGCOR}$	1.2 V Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	48	70
$V_{SS\_LV\_REGCOR}$	1.2 V decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	49	71
ADC0/ADC1 reference and supply voltage. Pins available on 100-pin and 144-pin package.			
$V_{DD\_HV\_AD0}$[1]	ADC0 supply and high reference voltage	33	50
$V_{SS\_HV\_AD0}$	ADC0 ground and low reference voltage	34	51
$V_{DD\_HV\_AD1}$	ADC1 supply and high reference voltage	39	56
$V_{SS\_HV\_AD1}$	ADC1 ground and low reference voltage	40	57
Power supply pins (3.3 V or 5.0 V). All pins available on 144-pin package. Five pairs (V_{DD}; V_{SS}) available on 100-pin package.			
$V_{DD\_HV\_IO0}$[2]	Input/Output supply voltage	—	6
$V_{SS\_HV\_IO0}$[2]	Input/Output ground	—	7
$V_{DD\_HV\_IO1}$	Input/Output supply voltage	13	21
$V_{SS\_HV\_IO1}$	Input/Output ground	14	22
$V_{DD\_HV\_IO2}$	Input/Output supply voltage	63	91
$V_{SS\_HV\_IO2}$	Input/Output ground	62	90
$V_{DD\_HV\_IO3}$	Input/Output supply voltage	**87**	126
$V_{SS\_HV\_IO3}$	Input/Output ground	**88**	127
$V_{DD\_HV\_FL}$	Code and data flash supply voltage	69	97
$V_{SS\_HV\_FL}$	Code and data flash supply ground	68	96
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	16	27
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	17	28

Table 2. Supply Pins (continued)

Supply		Pin	
Symbol	**Description**	**100-pin**	**144-pin**
Power supply pins (1.2 V). All pins available on 100-pin and 144-pin package.			
$V_{DD\_LV\_COR0}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	12	18
$V_{SS\_LV\_COR0}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	11	17
$V_{DD\_LV\_COR1}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	65	93
$V_{SS\_LV\_COR1}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	66	94
$V_{DD\_LV\_COR2}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	92	131
$V_{SS\_LV\_COR2}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	93	132
$V_{DD\_LV\_PLL}$	1.2 V Decoupling pins for on-chip PLL modules. Decoupling capacitor must be connected between this pin and $V_{SS\_LV\_PLL}$.	25	36
$V_{SS\_LV\_PLL}$	1.2 V Decoupling pins for on-chip PLL modules. Decoupling capacitor must be connected between this pin and $V_{DD\_LV\_PLL}$.	24	35

1 Analog supply/ground and high/low reference lines are internally physically separate, but are shorted via a double-bonding connection on $V_{DD\_HV\_ADx}$/$V_{SS\_HV\_ADx}$ pins.

2 Not available on 100-pin package

2.2.2 System Pins

Table 3 and Table 4 contain information on pin functions for the MPC5604P devices. The pins listed in Table 3 are single-function pins. The pins shown in Table 4 are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

Table 3. System Pins

Symbol	Description	Direction	Pad Speed[1]		Pin	
			SRC=0	SRC=1	100-pin	144-pin
Dedicated pins. All pins available on 144-pin package. MDO 0 not available on 100-pin package.						
MDO 0	Nexus Message Data Output - line 0	Output Only	Slow	Fast	—	9
NMI	Non Maskable Interrupt	Input Only	Slow	—	1	1
XTAL	Input for oscillator amplifier circuit and internal clock generator.	—	—	—	18	29
EXTAL	Oscillator amplifier output	—	—	—	19	30
TMS	JTAG state machine control	Bidirectional	Slow	Fast	59	87
TCK	JTAG clock	Input Only	Slow	—	60	88
Reset pin, available on 100-pin and 144-pin package.						
RESET_B	Bidirectional reset with Schmitt-Trigger characteristics and noise filter	Bidirectional	Medium	—	20	31
Test pin, available on 100-pin and 144-pin package.						
VPP TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	74	107

[1] SCR values refer to the value assigned to the Slew Rate Control bits of the pad configuration register

2.2.3 Pin Muxing

Table 4 defines the pin list and muxing for the MPC5604P devices.

Each row of Table 4 shows all the possible ways of configuring each pin, via “alternate functions”. The default function assigned to each pin after reset is the ALT0 function.

Some pins have more than four alternate functions. These additional alternate functions are shown in the column “Other functions”. This column also contains information related to the External Interrupt capability and the boot configuration. Pins marked as external interrupt capable can also be used to resume from STOP and HALT mode.

MPC5604P devices provide four main I/O pad types depending of the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.
- *Symmetric pads* are designed to meet FlexRay requirements.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

Table 4. Pin Muxing

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
Port A (16-bit). Fully available on 100-pin and 144-pin package.										
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3	GPIO[0] ETC[0] SCK F[0]	SIU Lite eTimer0 DSPI2 FCU0	Ext. IRQ #0	I/O	Slow	Medium	51	73
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3	GPIO[1] ETC[1] SOUT F[1]	SIU Lite eTimer0 DSPI2 FCU0	Ext. IRQ #1	I/O	Slow	Medium	52	74
A[2]	PCR[2]	ALT0 ALT1 ALT2 ALT3	GPIO[2] ETC[2] SIN A[3]	SIU Lite eTimer0 DSPI2 FlexPWM0	Ext. IRQ #2 Boot pin ABS[0]	I/O	Slow	Medium	57	84
A[3]	PCR[3]	ALT0 ALT1 ALT2 ALT3	GPIO[3] ETC[3] CS0 B[3]	SIU Lite eTimer0 DSPI2 FlexPWM0	Ext. IRQ #3 Boot pin ABS[2]	I/O	Slow	Medium	64	92
A[4]	PCR[4]	ALT0 ALT1 ALT2 ALT3	GPIO[4] ETC[0] CS1 ETC[4]	SIU Lite eTimer1 DSPI2 eTimer0	Ext. IRQ #4 Boot pin FAB Weak pull down during reset	I/O	Slow	Medium	75	108
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3	GPIO[5] CS0 ETC[5] CS7	SIU Lite DSPI1 eTimer1 DSPI0	Ext. IRQ #5	I/O	Slow	Medium	8	14
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3	GPIO[6] SCK — —	SIU Lite DSPI1 — —	Ext. IRQ #6	I/O	Slow	Medium	2	2
A[7]	PCR[7]	ALT0 ALT1 ALT2 ALT3	GPIO[7] SOUT — —	SIU Lite DSPI1 — —	Ext. IRQ #7	I/O	Slow	Medium	4	10

Table 4. Pin Muxing (continued)

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3	GPIO[8] SIN — —	SIU Lite DSPI1 — —	Ext. IRQ #8	I/O	Slow	Medium	6	12
A[9]	PCR[9]	ALT0 ALT1 ALT2 ALT3	GPIO[9] CS1 FAULT[0] B[3]	SIU Lite DSPI2 FlexPWM0 FlexPWM0	—	I/O	Slow	Medium	94	134
A[10]	PCR[10]	ALT0 ALT1 ALT2 ALT3	GPIO[10] CS0 B[0] X[2]	SIU Lite DSPI2 FlexPWM0 FlexPWM0	Ext. IRQ #9	I/O	Slow	Medium	81	118
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3	GPIO[11] SCK A[0] A[2]	SIU Lite DSPI2 FlexPWM0 FlexPWM0	Ext. IRQ #10	I/O	Slow	Medium	82	120
A[12]	PCR[12]	ALT0 ALT1 ALT2 ALT3	GPIO[12] SOUT A[2] B[2]	SIU Lite DSPI2 FlexPWM0 FlexPWM0	Ext. IRQ #11	I/O	Slow	Medium	83	122
A[13]	PCR[13]	ALT0 ALT1 ALT2 ALT3	GPIO[13] SIN B[2] FAULT[0]	SIU Lite DSPI2 FlexPWM0 FlexPWM0	Ext. IRQ #12	I/O	Slow	Medium	95	136
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3	GPIO[14] TXD ETC[4] —	SIU Lite Safety Port0 eTimer1 —	Ext. IRQ #13	I/O	Slow	Medium	99	143
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3	GPIO[15] RXD ETC[5] —	SIU Lite Safety Port0 eTimer1 —	Ext. IRQ #14	I/O	Slow	Medium	100	144

Table 4. Pin Muxing (continued)

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
Port B (16-bit). Fully available on 100-pin and 144-pin package.										
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3	GPIO[16] TXD ETC[2] DEBUG[0]	SIU Lite CAN0 eTimer1 SSCM	Ext. IRQ #15	I/O	Slow	Medium	76	109
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3	GPIO[17] RXD ETC[3] DEBUG[1]	SIU Lite CAN0 eTimer1 SSCM	Ext. IRQ #16	I/O	Slow	Medium	77	110
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3	GPIO[18] TXD — DEBUG[2]	SIU Lite LIN0 — SSCM	Ext. IRQ #17	I/O	Slow	Medium	79	114
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3	GPIO[19] RXD — DEBUG[3]	SIU Lite LIN0 — SSCM	—	I/O	Slow	Medium	80	116
B[4]	PCR[20]	ALT0 ALT1 ALT2 ALT3	— TDO — —	— JTAG0 — —	—	I/O	Slow	Fast	61	89
B[5]	PCR[21]	ALT0 ALT1 ALT2 ALT3	— TDI — —	— JTAG0 — —	—	I/O	Slow	Medium	58	86
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3	GPIO[22] CLKOUT CS2 —	SIU Lite Control DSPI2 —	Ext. IRQ #18	I/O	Slow	Medium	96	138
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3	GPIO[23] AN[0] RXD —	SIU Lite ADC0 LIN0 —	—	Input Only	—	—	29	43

Table 4. Pin Muxing (continued)

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3	GPIO[24] AN[1] ETC[5] —	SIU Lite ADC0 eTimer0 —	—	Input Only	—	—	31	47
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3	GPIO[25] AN[11] — —	SIU Lite ADC0 - ADC1 — —	—	Input Only	—	—	35	52
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3	GPIO[26] AN[12] — —	SIU Lite ADC0 - ADC1 — —	—	Input Only	—	—	36	53
B[11]	PCR[27]	ALT0 ALT1 ALT2 ALT3	GPIO[27] AN[13] — —	SIU Lite ADC0 - ADC1 — —	—	Input Only	—	—	37	54
B[12]	PCR[28]	ALT0 ALT1 ALT2 ALT3	GPIO[28] AN[14] — —	SIU Lite ADC0 - ADC1 — —	—	Input Only	—	—	38	55
B[13]	PCR[29]	ALT0 ALT1 ALT2 ALT3	GPIO[29] AN[0] RXD —	SIU Lite ADC1 LIN1 —	—	Input Only	—	—	42	60
B[14]	PCR[30]	ALT0 ALT1 ALT2 ALT3	GPIO[30] AN[1] ETC[4] —	SIU Lite ADC1 eTimer0 —	Ext. IRQ #19	Input Only	—	—	44	64
B[15]	PCR[31]	ALT0 ALT1 ALT2 ALT3	GPIO[31] AN[2] — —	SIU Lite ADC1 — —	Ext. IRQ #20	Input Only	—	—	43	62

Table 4. Pin Muxing (continued)

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
Port C (16-bit). Fully available on 100-pin and 144-pin package.										
C[0]	PCR[32]	ALT0 ALT1 ALT2 ALT3	GPIO[32] AN[3] — —	SIU Lite ADC1 — —	—	Input Only	—	—	45	66
C[1]	PCR[33]	ALT0 ALT1 ALT2 ALT3	GPIO[33] AN[2] — —	SIU Lite ADC0 — —	—	Input Only	—	—	28	41
C[2]	PCR[34]	ALT0 ALT1 ALT2 ALT3	GPIO[34] AN[3] — —	SIU Lite ADC0 — —	—	Input Only	—	—	30	45
C[3]	PCR[35]	ALT0 ALT1 ALT2 ALT3	GPIO[35] CS1 ETC[4] TXD	SIU Lite DSPI0 eTimer1 LIN1	Ext. IRQ #21	I/O	Slow	Medium	10	16
C[4]	PCR[36]	ALT0 ALT1 ALT2 ALT3	GPIO[36] CS0 X[1] DEBUG[4]	SIU Lite DSPI0 FlexPWM0 SSCM	Ext. IRQ #22	I/O	Slow	Medium	5	11
C[5]	PCR[37]	ALT0 ALT1 ALT2 ALT3	GPIO[37] SCK FAULT[3] DEBUG[5]	SIU Lite DSPI0 FlexPWM0 SSCM	Ext. IRQ #23	I/O	Slow	Medium	7	13
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3	GPIO[38] SOUT B[1] DEBUG[6]	SIU Lite DSPI0 FlexPWM0 SSCM	Ext. IRQ #24	I/O	Slow	Medium	98	142
C[7]	PCR[39]	ALT0 ALT1 ALT2 ALT3	GPIO[39] SIN A[1] DEBUG[7]	SIU Lite DSPI0 FlexPWM0 SSCM	—	I/O	Slow	Medium	9	15

Table 4. Pin Muxing (continued)

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
C[8]	PCR[40]	ALT0 ALT1 ALT2 ALT3	GPIO[40] CS1 FAULT[2] CS6	SIU Lite DSPI1 FlexPWM0 DSPI0	—	I/O	Slow	Medium	91	130
C[9]	PCR[41]	ALT0 ALT1 ALT2 ALT3	GPIO[41] CS3 FAULT[2] X[3]	SIU Lite DSPI2 FlexPWM0 FlexPWM0	—	I/O	Slow	Medium	84	123
C[10]	PCR[42]	ALT0 ALT1 ALT2 ALT3	GPIO[42] CS2 FAULT[1] A[3]	SIU Lite DSPI2 FlexPWM0 FlexPWM0	—	I/O	Slow	Medium	78	111
C[11]	PCR[43]	ALT0 ALT1 ALT2 ALT3	GPIO[43] ETC[4] CS2 CS0	SIU Lite eTimer0 DSPI2 DSPI3	—	I/O	Slow	Medium	55	80
C[12]	PCR[44]	ALT0 ALT1 ALT2 ALT3	GPIO[44] ETC[5] CS3 CS1	SIU Lite eTimer0 DSPI2 DSPI3	—	I/O	Slow	Medium	56	82
C[13]	PCR[45]	ALT0 ALT1 ALT2 ALT3	GPIO[45] ETC[1] EXT IN EXT. SYNC	SIU Lite eTimer1 ctu0 FlexPWM0	—	I/O	Slow	Medium	71	101
C[14]	PCR[46]	ALT0 ALT1 ALT2 ALT3	GPIO[46] ETC[2] EXT TGR —	SIU Lite eTimer1 ctu0 —	—	I/O	Slow	Medium	72	103
C[15]	PCR[47]	ALT0 ALT1 ALT2 ALT3	GPIO[47] CA TR EN ETC[0] A[1]	SIU Lite FlexRay0 eTimer1 FlexPWM0	ALT 4 Mode ctu0 EXT IN ALT 5 Mode FlexPWM0 EXT. SYNC	I/O	Slow	Symmetric	85	124

Table 4. Pin Muxing (continued)

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
Port D (16-bit). Fully available on 100-pin and 144-pin package.										
D[0]	PCR[48]	ALT0 ALT1 ALT2 ALT3	GPIO[48] CA TX ETC[1] B[1]	SIU Lite FlexRay0 eTimer1 FlexPWM0	—	I/O	Slow	Symmetric	86	125
D[1]	PCR[49]	ALT0 ALT1 ALT2 ALT3	GPIO[49] CA RX ETC[2] EXT TRG	SIU Lite FlexRay0 eTimer1 ctu0	—	I/O	Slow	Medium	3	3
D[2]	PCR[50]	ALT0 ALT1 ALT2 ALT3	GPIO[50] CB RX ETC[3] X[3]	SIU Lite FlexRay0 eTimer1 FlexPWM0	—	I/O	Slow	Medium	97	140
D[3]	PCR[51]	ALT0 ALT1 ALT2 ALT3	GPIO[51] CB TX ETC[4] A[3]	SIU Lite FlexRay0 eTimer1 FlexPWM0	—	I/O	Slow	Symmetric	89	128
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] CB TR EN ETC[5] B[3]	SIU Lite FlexRay0 eTimer1 FlexPWM0	—	I/O	Slow	Symmetric	90	129
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3 F[0] SOUT	SIU Lite DSPI0 FCU0 DSPI3	—	I/O	Slow	Medium	22	33
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3	GPIO[54] CS2 SCK FAULT[1]	SIU Lite DSPI0 DSPI3 FlexPWM0	—	I/O	Slow	Medium	23	34
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3	GPIO[55] CS3 F[1] SIN	SIU Lite DSPI1 FCU0 DSPI3	ALT 4 Mode DSPI0 CS4	I/O	Slow	Medium	26	37

Table 4. Pin Muxing (continued)

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3	GPIO[56] CS2 FAULT[3] CS5	SIU Lite DSPI1 FlexPWM0 DSPI0	—	I/O	Slow	Medium	21	32
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] X[0] TXD —	SIU Lite FlexPWM0 LIN1 —	—	I/O	Slow	Medium	15	26
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] A[0] CS0 —	SIU Lite FlexPWM0 DSPI3 —	—	I/O	Slow	Medium	53	76
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] B[0] CS1 SCK	SIU Lite FlexPWM0 DSPI3 DSPI3	—	I/O	Slow	Medium	54	78
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3	GPIO[60] X[1] RXD	SIU Lite FlexPWM0 LIN1	—	I/O	Slow	Medium	70	99
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] A[1] CS2 SOUT	SIU Lite FlexPWM0 DSPI3 DSPI3	—	I/O	Slow	Medium	67	95
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3	GPIO[62] B[1] CS3 SIN	SIU Lite FlexPWM0 DSPI3 DSPI3	—	I/O	Slow	Medium	73	105
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3	GPIO[63] AN[4] — —	SIU Lite ADC1 — —	—	Input Only	—	—	41	58

Table 4. Pin Muxing (continued)

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
Port E(16-bit). Fully available on 144-pin package. E[0], E[1] and E[2] available on 100-pin package.										
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3	GPIO[64] AN[5] — —	SIU Lite ADC1 — —	—	Input Only	—	—	46	68
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3	GPIO[65] AN[4] — —	SIU Lite ADC0 — —	—	Input Only	—	—	27	39
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3	GPIO[66] AN[5] — —	SIU Lite ADC0 — —	—	Input Only	—	—	32	49
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3	GPIO[67] AN[6] — —	SIU Lite ADC0 — —	—	Input Only	—	—	—	40
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3	GPIO[68] AN[7] — —	SIU Lite ADC0 — —	—	Input Only	—	—	—	42
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3	GPIO[69] AN[8] — —	SIU Lite ADC0 — —	—	Input Only	—	—	—	44
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3	GPIO[70] AN[9] — —	SIU Lite ADC0 — —	—	Input Only	—	—	—	46
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3	GPIO[71] AN[10] — —	SIU Lite ADC0 — —	—	Input Only	—	—	—	48

Table 4. Pin Muxing (continued)

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
E[8]	PCR[72]	ALT0 ALT1 ALT2 ALT3	GPIO[72] AN[6] — —	SIU Lite ADC1 — —	—	Input Only	—	—	—	59
E[9]	PCR[73]	ALT0 ALT1 ALT2 ALT3	GPIO[73] AN[7] — —	SIU Lite ADC1 — —	—	Input Only	—	—	—	61
E[10]	PCR[74]	ALT0 ALT1 ALT2 ALT3	GPIO[74] AN[8] — —	SIU Lite ADC1 — —	—	Input Only	—	—	—	63
E[11]	PCR[75]	ALT0 ALT1 ALT2 ALT3	GPIO[75] AN[9] — —	SIU Lite ADC1 — —	—	Input Only	—	—	—	65
E[12]	PCR[76]	ALT0 ALT1 ALT2 ALT3	GPIO[76] AN[10] — —	SIU Lite ADC1 — —	—	Input Only	—	—	—	67
E[13]	PCR[77]	ALT0 ALT1 ALT2 ALT3	GPIO[77] SCK — —	SIU Lite DSPI3 — —	Ext. IRQ #25	I/O	Slow	Medium	—	117
E[14]	PCR[78]	ALT0 ALT1 ALT2 ALT3	GPIO[78] SOUT — —	SIU Lite DSPI3 — —	Ext. IRQ #26	I/O	Slow	Medium	—	119
E[15]	PCR[79]	ALT0 ALT1 ALT2 ALT3	GPIO[79] SIN — —	SIU Lite DSPI3 — —	Ext. IRQ #27	I/O	Slow	Medium	—	121

Table 4. Pin Muxing (continued)

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
Port F (16-bit). Fully available on 144-pin package										
F[0]	PCR[80]	ALT0 ALT1 ALT2 ALT3	GPIO[80] DBG0 CS3 —	SIU Lite FlexRay0 DSPI3 —	Ext. IRQ #28	I/O	Slow	Medium	—	133
F[1]	PCR[81]	ALT0 ALT1 ALT2 ALT3	GPIO[81] DBG1 CS2 —	SIU Lite FlexRay0 DSPI3 —	Ext. IRQ #29	I/O	Slow	Medium	—	135
F[2]	PCR[82]	ALT0 ALT1 ALT2 ALT3	GPIO[82] DBG2 CS1 —	SIU Lite FlexRay0 DSPI3 —	—	I/O	Slow	Medium	—	137
F[3]	PCR[83]	ALT0 ALT1 ALT2 ALT3	GPIO[83] DBG3 CS0 —	SIU Lite FlexRay0 DSPI3 —	—	I/O	Slow	Medium	—	139
F[4]	PCR[84]	ALT0 ALT1 ALT2 ALT3	GPIO[84] MDO[3] — —	SIU Lite nexus0 — —	—	I/O	Slow	Fast	—	4
F[5]	PCR[85]	ALT0 ALT1 ALT2 ALT3	GPIO[85] MDO[2] — —	SIU Lite nexus0 — —	—	I/O	Slow	Fast	—	5
F[6]	PCR[86]	ALT0 ALT1 ALT2 ALT3	GPIO[86] MDO[1] — —	SIU Lite nexus0 — —	—	I/O	Slow	Fast	—	8
F[7]	PCR[87]	ALT0 ALT1 ALT2 ALT3	GPIO[87] MCKO — —	SIU Lite nexus0 — —	—	I/O	Slow	Fast	—	19

Table 4. Pin Muxing (continued)

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
F[8]	PCR[88]	ALT0 ALT1 ALT2 ALT3	GPIO[88] MSEO1 — —	SIU Lite nexus0 — —	—	I/O	Slow	Fast	—	20
F[9]	PCR[89]	ALT0 ALT1 ALT2 ALT3	GPIO[89] MSEO0 — —	SIU Lite nexus0 — —	—	I/O	Slow	Fast	—	23
F[10]	PCR[90]	ALT0 ALT1 ALT2 ALT3	GPIO[90] EVTO — —	SIU Lite nexus0 — —	—	I/O	Slow	Fast	—	24
F[11]	PCR[91]	ALT0 ALT1 ALT2 ALT3	GPIO[91] EVTI — —	SIU Lite nexus0 — —	—	I/O	Slow	Medium	—	25
F[12]	PCR[92]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[3] — —	SIU Lite eTimer1 — —	—	I/O	Slow	Medium	—	106
F[13]	PCR[93]	ALT0 ALT1 ALT2 ALT3	GPIO[93] ETC[4] — —	SIU Lite eTimer1 — —	—	I/O	Slow	Medium	—	112
F[14]	PCR[94]	ALT0 ALT1 ALT2 ALT3	GPIO[94] TXD — —	SIU Lite LIN1 — —	—	I/O	Slow	Medium	—	115
F[15]	PCR[95]	ALT0 ALT1 ALT2 ALT3	GPIO[95] RXD — —	SIU Lite LIN1 — —	—	I/O	Slow	Medium	—	113

Table 4. Pin Muxing (continued)

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
Port G (12-bit). Fully available on 144-pin package.										
G[0]	PCR[96]	ALT0 ALT1 ALT2 ALT3	GPIO[96] F[0] — —	SIU Lite FCU0 — —	Ext. IRQ #30	I/O	Slow	Medium	—	38
G[1]	PCR[97]	ALT0 ALT1 ALT2 ALT3	GPIO[97] F[1] — —	SIU Lite FCU0 — —	Ext. IRQ #31	I/O	Slow	Medium	—	141
G[2]	PCR[98]	ALT0 ALT1 ALT2 ALT3	GPIO[98] X[2] — —	SIU Lite FlexPWM0 — —	—	I/O	Slow	Medium	—	102
G[3]	PCR[99]	ALT0 ALT1 ALT2 ALT3	GPIO[99] A[2] — —	SIU Lite FlexPWM0 — —	—	I/O	Slow	Medium	—	104
G[4]	PCR[100]	ALT0 ALT1 ALT2 ALT3	GPIO[100] B[2] — —	SIU Lite FlexPWM0 — —	—	I/O	Slow	Medium	—	100
G[5]	PCR[101]	ALT0 ALT1 ALT2 ALT3	GPIO[101] X[3] — —	SIU Lite FlexPWM0 — —	—	I/O	Slow	Medium	—	85
G[6]	PCR[102]	ALT0 ALT1 ALT2 ALT3	GPIO[102] A[3] — —	SIU Lite FlexPWM0 — —	—	I/O	Slow	Medium	—	98
G[7]	PCR[103]	ALT0 ALT1 ALT2 ALT3	GPIO[103] B[3] — —	SIU Lite FlexPWM0 — —	—	I/O	Slow	Medium	—	83

Table 4. Pin Muxing (continued)

Port Pin	PCR Register	Alternate Function[1,2]	Functions	Peripheral[3]	Other functions	I/O Direction	Pad Speed[4]		Pin	
							SRC=0	SRC=1	100-pin	144-pin
G[8]	PCR[104]	ALT0 ALT1 ALT2 ALT3	GPIO[104] FAULT[0] — —	SIU Lite FlexPWM0 — —	—	I/O	Slow	Medium	—	81
G[9]	PCR[105]	ALT0 ALT1 ALT2 ALT3	GPIO[105] FAULT[1] — —	SIU Lite FlexPWM0 — —	—	I/O	Slow	Medium	—	79
G[10]	PCR[106]	ALT0 ALT1 ALT2 ALT3	GPIO[106] FAULT[2] — —	SIU Lite FlexPWM0 — —	—	I/O	Slow	Medium	—	77
G[11]	PCR[107]	ALT0 ALT1 ALT2 ALT3	GPIO[107] FAULT[3] — —	SIU Lite FlexPWM0 — —	—	I/O	Slow	Medium	—	75

1 ALT0 is the primary (default) function for each port after reset.

2 Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIU module. PCR.PA = 00 -> Option 0; PCR.PA = 01 -> Option 1; PCR.PA = 10 -> Option 2; PCR.PA = 11-> Option 3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

3 Module included on the MCU.

4 Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.

3 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5604P MCU.

The “Symbol” column of the electrical parameter and timings tables contains an additional column containing “SR”, “P”, “C”, “T” or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the *input* voltage of a voltage regulator.
- “P”, “C”, “T” or “D” apply only to controller characteristics—specifications that define normal device operation. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

NOTE

All values are preliminary and subject to change during characterization.

3.1 Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings[1]

Symbol		Parameter	Conditions	Min	Max[2]	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V / 5.0 V voltage regulator supply voltage	—	-0.3	6.0	V
$V_{DD\_HV\_IOx}$	SR	3.3 V / 5.0 V input/output supply voltage	—	-0.3	6.0	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	-0.1	0.1	V
$V_{DD\_HV\_FL}$	SR	3.3 V / 5.0 V code and data flash supply voltage	—	-0.3	3.6 / 6.0	V
$V_{SS\_HV\_FL}$	SR	Code and data flash ground	—	-0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier supply voltage	—	-0.3	6.0	V
$V_{SS\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier reference voltage	—	-0.1	0.1	V
$V_{DD\_HV\_AD0}$[3]	SR	3.3 V / 5.0 V ADC0 supply and high reference voltage	—	- 0.3	6.0	V
$V_{SS\_HV\_AD0}$	SR	ADC0 ground and low reference voltage	—	-0.1	0.1	V
$V_{DD\_HV\_AD1}$[3]	SR	3.3 V / 5.0 V ADC1 supply and high reference voltage	—	- 0.3	6.0	V
$V_{SS\_HV\_AD1}$	SR	ADC1 ground and low reference voltage	—	-0.1	0.1	V

Table 5. Absolute Maximum Ratings[1] (continued)

Symbol		Parameter	Conditions	Min	Max[2]	Unit
TV_{DD}	SR	Slope characteristics on all V_{DD} during power up[4]	—	0.5 V/µs	3 V/S	—
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$)	—	-0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$	-0.3	$V_{DD\_HV\_IOx}$ + 0.3[5]	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	-10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	-50	50	mA
T_{STG}	SR	Storage temperature	—	-55	150	°C

1 Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.

3 The power supply voltage must be identical for ADC0 and ADC1 (both at 3.3 V or both at 5 V).

4 Guaranteed by device validation

5 Only when $V_{DD\_HV\_IOx}$ <5.2 V

3.2 Recommended Operating Conditions

Table 6. Recommended Operating Conditions (5.0 V)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
$V_{DD\_HV\_REG}$	SR	5.0 V voltage regulator supply voltage	—	4.5	5.5	V
$V_{DD\_HV\_IOx}$	SR	5.0 V input/output supply voltage	—	4.5	5.5	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FL}$	SR	5.0 V code and data flash supply voltage	—	4.5	5.5	V
$V_{SS\_HV\_FL}$	SR	Code and data flash ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier supply voltage	—	4.5	5.5	V
$V_{SS\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_AD0}$[2]	SR	5.0 V ADC0 supply and high reference voltage	—	4.5	5.5	V
$V_{SS\_HV\_AD0}$	SR	ADC0 ground and low reference voltage	—	0	0	V
$V_{DD\_HV\_AD1}$[2]	SR	5.0 V ADC1 supply and high reference voltage	—	4.5	5.5	V
$V_{SS\_HV\_AD1}$	SR	ADC1 ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$[3,4]	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$[3]	SR	Internal reference voltage	—	0	0	V

Table 6. Recommended Operating Conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
$V_{DD\_LV\_CORx}$[3,4]	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$[3]	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_PLL}$[3,4,5]	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_PLL}$[3,5]	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	f_{CPU} = 64 MHz	-40	105	°C
			f_{CPU} = 60 MHz	-40	125	
T_J	SR	Junction temperature under bias	—	-40	150	°C

1 Full functionality cannot be guaranteed when voltage drops below 4.5 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

2 The power supply voltage must be identical for ADC0 and ADC1

3 To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.

4 The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.

$V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.

$V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_RECORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

$V_{DD\_LV\_PLL}$ and $V_{SS\_LV\_PLL}$ are independent of other supplies.

5 Low voltage supply/ground lines of the FMPLLs internally are physically separate but are shorted with a double-bonding connection on the $V_{DD\_LV\_PLL}$ and $V_{SS\_LV\_PLL}$ pins.

Table 7. Recommended Operating Conditions (3.3 V)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FL}$	SR	3.3 V code and data flash supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_FL}$	SR	Code and data flash ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_AD0}$[2]	SR	3.3 V ADC0 supply and high reference voltage	—	3.0	3.6	V
$V_{SS\_HV\_AD0}$	SR	ADC0 ground and low reference voltage	—	0	0	V
$V_{DD\_HV\_AD1}$[2]	SR	3.3 V ADC1 supply and high reference voltage	—	3.0	3.6	V

Table 7. Recommended Operating Conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
$V_{SS\_HV\_AD1}$	SR	ADC1 ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$[3,4]	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$[3]	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$[3,4]	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$[3]	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_PLL}$[3,4,5]	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_PLL}$[3,5]	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	f_{CPU} = 64 MHz	-40	105	°C
			f_{CPU} = 60 MHz	-40	125	
T_J	SR	Junction temperature under bias	—	-40	150	°C

1 Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

2 The power supply voltage must be identical for ADC0 and ADC1. As long as that condition is met, ADC0 and ADC1 can be operated at 5 V with the rest of the device operating at 3.3 V.

3 To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.

4 The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.

$V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.

$V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_RECORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

$V_{DD\_LV\_PLL}$ and $V_{SS\_LV\_PLL}$ are independent of other supplies.

5 Low voltage supply/ground lines of the FMPLLs internally are physically separate but are shorted with a double-bonding connection on the $V_{DD\_LV\_PLL}$ and $V_{SS\_LV\_PLL}$ pins.

3.3 Thermal Characteristics

Table 8. Thermal Characteristics for 144-pin LQFP[1]

No.	Symbol	Parameter	Conditions	Typical Value	Unit
1	$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection[2]	Single layer board - 1s	52	°C/W
2	$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection[2]	Four layer board - 2s2p	43	°C/W
3	$R_{\theta JMA}$	Thermal resistance junction-to-ambient[2]	@ 200 ft./min.[3], single layer board - 1s	43	°C/W

Table 8. Thermal Characteristics for 144-pin LQFP[1] (continued)

No.	Symbol	Parameter	Conditions	Typical Value	Unit
4	$R_{\theta JMA}$	Thermal resistance junction-to-ambient[2]	@ 200 ft./min.[3], four layer board - 2s2p	37	°C/W
5	$R_{\theta JB}$	Thermal resistance junction to board[4]		31	°C/W
6	$R_{\theta JCtop}$	Thermal resistance junction to case (top)[5]		12	°C/W
7	Ψ_{JT}	Junction to package top natural convection[6]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Flow rate of forced air flow.

4 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

5 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 9. Thermal Characteristics for 100-pin LQFP[1]

No.	Symbol	Parameter	Conditions	Typical Value	Unit
1	$R_{\theta JA}$	Thermal resistance junction-to-ambient natural convection[2]	Single layer board - 1s	52	°C/W
2	$R_{\theta JA}$	Thermal resistance junction-to-ambient natural convection[2]	Four layer board - 2s2p	39	°C/W
3	$R_{\theta JMA}$	Thermal resistance junction-to-ambient[2]	@ 200 ft./min., single layer board - 1s	42	°C/W
4	$R_{\theta JMA}$	Thermal resistance junction-to-ambient[2]	@ 200 ft./min., four layer board - 2s2p	33	°C/W
5	$R_{\theta JB}$	Thermal resistance junction to board[3]		24	°C/W
6	$R_{\theta JCtop}$	Thermal resistance junction to case (Top)[4]		12	°C/W
7	Ψ_{JT}	Junction to package top natural convection[5]		3	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.3.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in Equation 2 as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 U.S.A.
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, *An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*, Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. G. Kromann, S. Shidore, and S. Addison, *Thermal Modeling of a PBGA for Air-Cooled Applications*, Electronic Packaging and Production, pp. 53-58, March 1998.

3. B. Joiner and V. Adams, *Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*, Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

3.4 Electromagnetic Interference (EMI) Characteristics

Table 10. EMI Testing Specifications[1]

Symbol	Parameter	Conditions	f_{OSC}/f_{BUS}	Frequency	Level (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DD} = 5.5 V; T_A = +25 °C 150 kHz - 30 MHz RBW 9 kHz, Step Size 5kHz 30 MHz - 1 GHz - RBW 120 kHz, Step Size 80 kHz	16 MHz crystal 40 MHz bus No PLL frequency modulation4	150 kHz - 50 MHz	20	dBµV
				50 - 150 MHz	20	
				150 - 500 MHz	26	
				500 - 1000 MHz	26	
				IEC Level	K	—
				SAE Level	3	—
			16 MHz crystal 40 MHz bus +/-2% PLL frequency modulation	150 kHz- 50 MHz	18	dBµV
				50 - 150 MHz	18	
				150 - 500 MHz	15	
				500 - 1000 MHz	15	
				IEC Level	L	—
				SAE Level	2	—

1 EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03.

3.5 Electrostatic Discharge (ESD) Characteristics

Table 11. ESD ratings[1,2]

Symbol		Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)		2000	V
$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)		750 (corners)	V
				500 (other)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

[2] A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification

3.6 Power management electrical characteristics

3.6.1 Voltage Regulator Electrical Characteristics

The internal voltage regulator requires an external NPN (BCP56 or BCP68) ballast to be connected as shown in Figure 4 as well as an external capacitance (C_{REG}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

NOTE

The voltage regulator output cannot be used to drive external circuits. Output pins are to be used only for decoupling capacitance.

For the MPC5604P microcontroller , 10 µF should be placed between each of the three $V_{DD\_LV\_CORx}/V_{SS\_LV\_CORx}$ supply pairs and also between the $V_{DD\_LV\_REGCOR}/V_{SS\_LV\_REGCOR}$ pair. Additionally, 40 µF should be placed between the $V_{DD\_HV\_REG}/V_{SS\_HV\_REG}$ pins.

V_{DD} = 3.0 V to 3.6 V / 4.5 V to 5.5 V, T_A = -40 to 125 °C, unless otherwise specified.

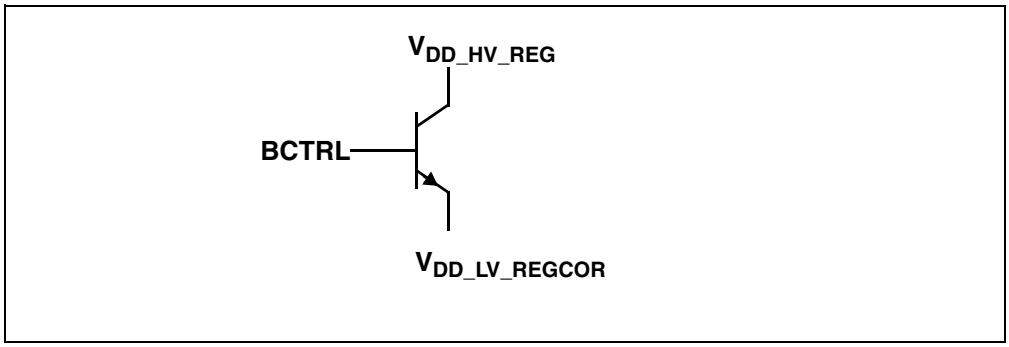


Figure 4. External NPN Ballast Connections

Table 12. Voltage Regulator Electrical Characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	$V_{DD\_LV\_REGCOR}$	P	Output voltage under maximum load	Post-trimming	1.145	1.4	V
2		SR	External decoupling/stability capacitor	4 capacitances of 10 µF each	4 × 10		µF
				ESR of external cap	0.05	0.2	Ω
3		SR	External decoupling/stability capacitor on VDD_HV_REG		47		µF

3.6.2 Voltage monitor electrical characteristics

The device implements a Power On Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0V ± 10% range
- LVDLVCOR monitors power domain No. 1

Table 13. Low voltage monitor electrical characteristics

Symbol		Parameter	Conditions[1]	Value		Unit
				Min	Max	
V_{POR}	T	Power-on reset threshold		1.5	2.7	V
$V_{REGLVDMOK\_H}$	P	Regulator low voltage detector high threshold		—	2.9	V
$V_{REGLVDMOK\_L}$	P	Regulator low voltage detector low threshold		2.6	—	V
$V_{FLLVDMOK\_H}$	P	Flash low voltage detector high threshold		—	2.9	V
$V_{FLLVDMOK\_L}$	P	Flash low voltage detector low threshold		2.6	—	V
$V_{IOLVDMOK\_H}$	P	I/O low voltage detector high threshold		—	2.9	V
$V_{IOLVDMOK\_L}$	P	I/O low voltage detector low threshold		2.6	—	V
$V_{IOLVDM5OK\_H}$	P	I/O 5V low voltage detector high threshold		—	4.3	V
$V_{IOLVDM5OK\_L}$	P	I/O 5V low voltage detector low threshold		4.0	—	V
$V_{MLVDDOK\_H}$	P	Digital supply low voltage detector high		—	1.185	V
$V_{MLVDDOK\_L}$	P	Digital supply low voltage detector low		1.095	—	V

1 V_{DD} = 3.3V ± 10% / 5.0V ± 10%, T_A = -40 / +125°C, unless otherwise specified

3.7 Power Up/Down Sequencing

The maximum slope (TV_{DD}) must be granted on all power supplies (see Table 5).

3.8 DC electrical Characteristics

3.8.1 NVUSRO Register

Portions of the MPC5604P device configuration, i.e., high voltage supply, oscillator margin, and watchdog enable/disable after reset) are controlled via bit values in the NVUSRO register. NVUSRO[PAD3V5V] controls the device configuration as follows:

Table 14. NVUSRO[PAD3V5V] Field Description[1]

Value[2]	Description
0	High Voltage supply is 5.0 V
1	High Voltage supply is 3.3 V

1 See the MPC5604P Reference Manual for more information on the NVUSRO register.

2 Default manufacturing value before flash initialization is '1' (3.3 V).

The DC electrical characteristics in the following sections are dependent on the PAD3V5V value as described above.

3.8.2 DC Electrical Characteristics (5 V)

Table 15 gives the DC electrical characteristics at 5 V ($4.5\ V < V_{DD\_HV\_IOx} < 5.5\ V$, NVUSRO[PAD3V5V]=0).

Table 15. DC Electrical Characteristics (5.0 V, NVUSRO[PAD3V5V]=0)

Symbol		Parameter	Conditions	Min	Max	Unit
V_{IL}	D	Minimum low level input voltage		-0.1[1]	—	V
V_{IL}	P	Maximum level input voltage		—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	Minimum high level input voltage		0.65 $V_{DD\_HV\_IOx}$	—	V
V_{IH}	D	Maximum high level input voltage		—	$V_{DD\_HV\_IOx}$ + 0.1[1]	V
V_{PP}	P	Input leakage current		-5	5	µA
V_{HYS}	T	Schmitt trigger hysteresis		0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = -3 mA	0.8$V_{DD_HV_IOx}$	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = -3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = -3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_SYM}	P	Symmetric, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = -3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
I_{PU}	P	Equivalent pull-up current	$V_{IN} = V_{IL}$	-130	—	µA
			$V_{IN} = V_{IH}$	—	-10	
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	µA
			$V_{IN} = V_{IH}$	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = -40 to 125 °C	-1	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = -40 to 125 °C	-0.5	0.5	µA
V_{ILR}	D	Minimum RESET_B, low level input voltage		-0.1[1]	—	V
V_{ILR}	P	Maximum RESET_B, low level input voltage		—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IHR}	P	Minimum RESET_B, high level input voltage		0.65 $V_{DD\_HV\_IOx}$	—	V
V_{IHR}	D	Maximum RESET_B, high level input voltage		—	$V_{DD\_HV\_IOx}$ + 0.1[1]	V

Table 15. DC Electrical Characteristics (5.0 V, NVUSRO[PAD3V5V]=0) (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
V_{HYSR}	D	RESET_B, Schmitt trigger hysteresis		0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OLR}	D	RESET_B, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
I_{PUR}	D	RESET_B, equivalent pull-up current	$V_{IN} = V_{IL}$	-130	—	µA
			$V_{IN} = V_{IH}$	—	-10	

1 "SR" parameter values must not exceed the absolute maximum ratings shown in Table 5.

Table 16. Supply Current (5.0 V, NVUSRO[PAD3V5V]=0, Normal Mode)[1]

Symbol		Parameter		Conditions		Typical Value	Unit
I_{DD}	T	Supply Current	RUN (fetch from flash)	VDD_LV_CORE externally forced at 1.3 V	40 MHz	92	mA
					64 MHz	100	
	P		HALT	VDD_LV_CORE externally forced at 1.3 V		10	
						10	
	P		STOP	VDD_LV_CORE externally forced at 1.3 V		10	
						10	

1 Normal mode: FlexPWM, ADCs, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, 1st and 2nd PLL enabled, 125 °C ambient. I/O supply current excluded.

Table 17. Supply Current (5.0 V, NVUSRO[PAD3V5V]=0, Airbag Mode)[1]

Symbol		Parameter		Conditions		Value	Unit
I_{DD}	T	Supply Current	RUN (fetch from flash)	VDD_LV_CORE externally forced at 1.3 V	40 MHz	64	mA
					64 MHz	74	
	P		HALT	VDD_LV_CORE externally forced at 1.3 V		10	
						10	
	P		STOP	VDD_LV_CORE externally forced at 1.3 V		10	
						10	

1 Airbag mode: DSPI, LINFlex, FlexCAN, 15 output pins, 1st PLL only, 105 °C ambient. I/O supply current excluded.

3.8.3 DC Electrical characteristics (3.3 V)

Table 18 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD\_HV\_IOx}$ < 3.6 V, NVUSRO[PAD3V5V]=1).

Table 18. DC Electrical Characteristics (3.3 V, NVUSRO[PAD3V5V]=1)[1]

Symbol		Parameter	Conditions	Min	Max	Unit
V_{IL}	D	Minimum low level input voltage		-0.1[2]	—	V
V_{IL}	P	Maximum low level input voltage		—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	Minimum high level input voltage		0.65 $V_{DD\_HV\_IOx}$	—	V
V_{IH}	D	Maximum high level input voltage		—	$V_{DD\_HV\_IOx}$ + 0.1[2]	V
V_{PP}	P	Input leakage current		—	5	µA
V_{HYS}	T	Schmitt trigger hysteresis		0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = -1.5 mA	$V_{DD\_HV\_IOx}$ - 0.8	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = -2 mA	$V_{DD\_HV\_IOx}$ - 0.8	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = -1.5 mA	$V_{DD\_HV\_IOx}$ - 0.8	—	V
V_{OL_SYM}	P	Symmetric, high level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = -1.5 mA	$V_{DD\_HV\_IOx}$ - 0.8	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	-130	—	µA
			V_{IN} = V_{IH}	—	-10	
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
			V_{IN} = V_{IH}	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = -40 to 125 °C	—	1 µA	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = -40 to 125 °C	—	0.5 µA	µA
V_{ILR}	D	Minimum RESET_B, low level input voltage		-0.1[2]	—	V
V_{ILR}	P	Maximum RESET_B, low level input voltage		—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IHR}	P	Minimum RESET_B, high level input voltage		0.65 $V_{DD\_HV\_IOx}$	—	V
V_{IHR}	D	Maximum RESET_B, high level input voltage		—	$V_{DD\_HV\_IOx}$ + 0.1[2]	V

Table 18. DC Electrical Characteristics (3.3 V, NVUSRO[PAD3V5V]=1)[1] (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
V_{HYSR}	D	RESET_B, Schmitt trigger hysteresis		0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OLR}	D	RESET_B, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
I_{PUR}	D	RESET_B, equivalent pull-up current	$V_{IN} = V_{IL}$	-130	—	µA
			$V_{IN} = V_{IH}$	—	-10	

1 These specifications are design targets and subject to change per device characterization.

2 “SR” parameter values must not exceed the absolute maximum ratings shown in Table 5.

Table 19. Supply Current (3.3 V, NVUSRO[PAD3V5V]=1, Normal Mode)[1]

Symbol		Parameter		Conditions		Value	Unit
I_{DD}	T	Supply Current	RUN (fetch from flash)	VDD_LV_CORE externally forced at 1.3 V	40 MHz	89	mA
					64 MHz	98	
	P		HALT	VDD_LV_CORE externally forced at 1.3 V		10	
						10	
	P		STOP	VDD_LV_CORE externally forced at 1.3 V		10	
						10	

1 Normal mode: FlexPWM, ADCs, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, 1st and 2nd PLL enabled, 125 °C ambient. I/O supply current excluded.

Table 20. Supply Current (3.3 V, NVUSRO[PAD3V5V]=1, Airbag Mode)[1]

Symbol		Parameter		Conditions		Value	Unit
I_{DD}	T	Supply Current	RUN (fetch from flash)	VDD_LV_CORE externally forced at 1.3 V	40 MHz	62	mA
					64 MHz	72	
	P		HALT	VDD_LV_CORE externally forced at 1.3 V		10	
						10	
	P		STOP	VDD_LV_CORE externally forced at 1.3 V		10	
						10	

1 Airbag mode: DSPI, LINFlex, FlexCAN, 15 output pins, 1st PLL only, 105 °C ambient. I/O supply current excluded.

3.9 Temperature Sensor Electrical Characteristics

Table 21. Temperature Sensor Electrical Characteristics

Symbol		Parameter	Conditions	Min	Max	Unit
—	P	Accuracy	T_J = -40 °C to T_A = 25 °C	-10	10	°C
			T_J = T_A to 125 °C	-7	7	°C
T_S	D	Minimum sampling period		1.5	—	µS

3.10 Main Oscillator Electrical Characteristics

The MPC5604P provides an oscillator/resonator driver.

Table 22. Main Oscillator Electrical Characteristics (5.0 V, NVUSRO[PAD3V5V]=0)

Symbol		Parameter	Min	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	40	MHz
g_m	P	Transconductance	6.5	25	mA/V
V_{OSC}	C	Oscillation amplitude on EXTAL pin	1.3	2.25	V
t_{OSCSU}	C	Start-up time[1,2]	8	—	ms

1 The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.

2 Value captured when amplitude reaches 90% of EXTAL

Table 23. Main Oscillator Electrical Characteristics (3.3 V, NVUSRO[PAD3V5V]=1)

Symbol		Parameter	Min	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	40	MHz
g_m	P	Transconductance	4	20	mA/V
V_{OSC}	C	Oscillation amplitude on EXTAL pin	1.3	2.25	V
t_{OSCSU}	C	Start-up time[1,2]	8	—	ms

1 The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.

2 Value captured when amplitude reaches 90% of EXTAL

Table 24. Input Clock Characteristics

Symbol		Parameter	Min	Typ	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	—	40	MHz
f_{CLK}	SR	Frequency in bypass	—	—	100	MHz
t_{rCLK}	SR	Rise/fall time in bypass	—	—	1	ns
t_{DC}	SR	Duty cycle	47.5	50	52.5	%

3.11 FMPLL Electrical Characteristics

Table 25. FMPLL Electrical Characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	—	4		120	MHz
f_{FREE}	P	Free running frequency	Measured using clock division—typically /16	20		150	MHz
t_{LOCK}	P	Lock time	Stable oscillator ($f_{FMPLLIN}$ = 4 MHz), stable $V_{DD\_LV\_PLL}$	—	—	200	µs
Δt_{LTJIT}	T	Long term jitter (4000 cycles)[1]	$f_{FMPLLCLK}$ @ 64 MHz, $f_{FMPLLIN}$ @ 8 MHz	—	±6	—	ns

[1] Measured using divide by 4 on $f_{FMPLLCLK}$.

3.12 16 MHz RC Oscillator Electrical Characteristics

Table 26. 16 MHz RC Oscillator Electrical Characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
ΔRCMVAR	P	Frequency Spread: The variation in output frequency from PTF[1] across temperature and the supply voltage range	T_A = 25 °C	-5	—	5	%
ΔRCMTRIM	P	Post Trim Accuracy: The variation of the PTF[1] from the 16 MHz	T_A = 25 °C	-1	—	1	%

[1] PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

3.13 Analog-to-Digital Converter (ADC) Electrical Characteristics

The device provides a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

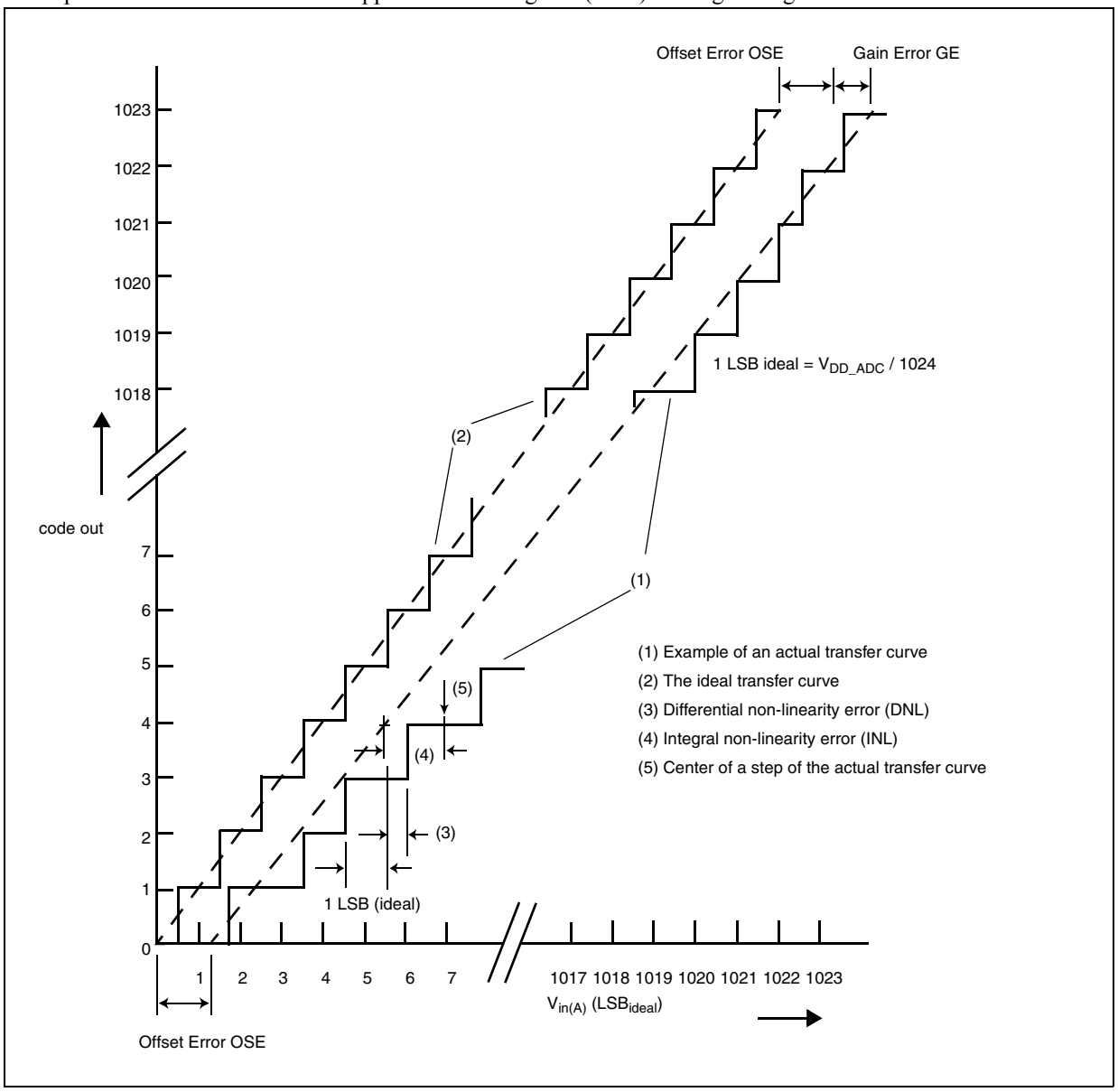


Figure 5. ADC Characteristics and Error Definitions

3.13.1 Input Impedance and ADC Accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to

be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (fc \times C_S)$, where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

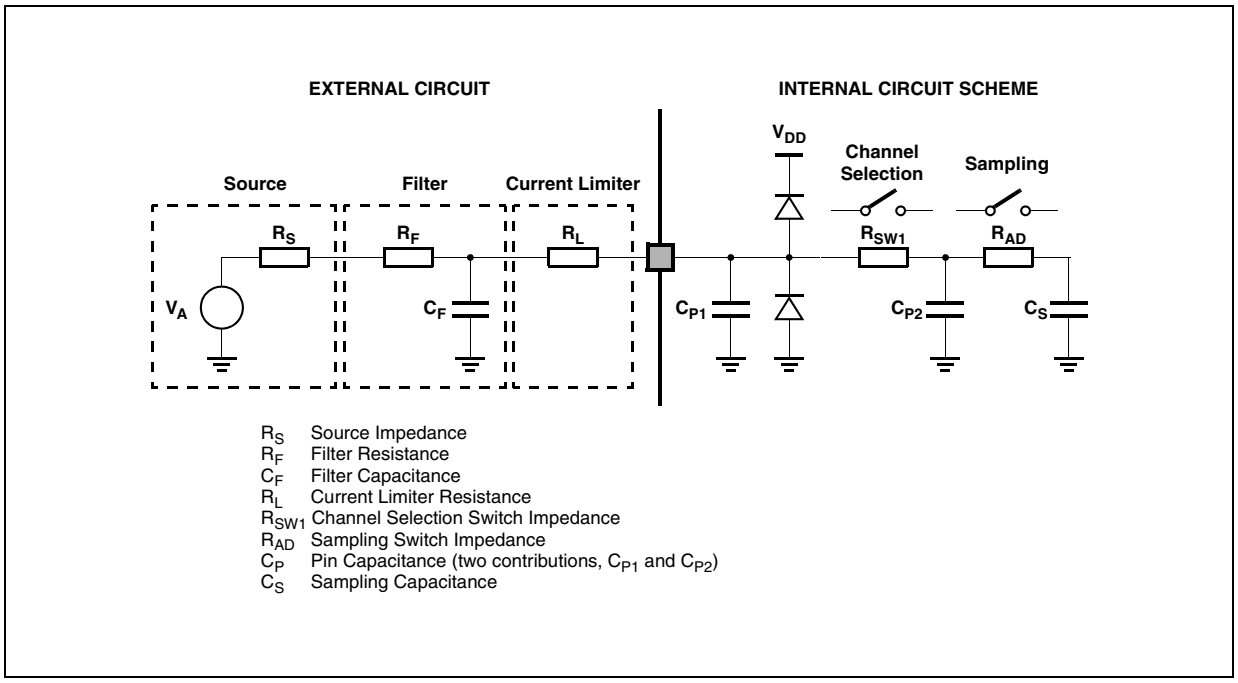


Figure 6. Input Equivalent Circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 6): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

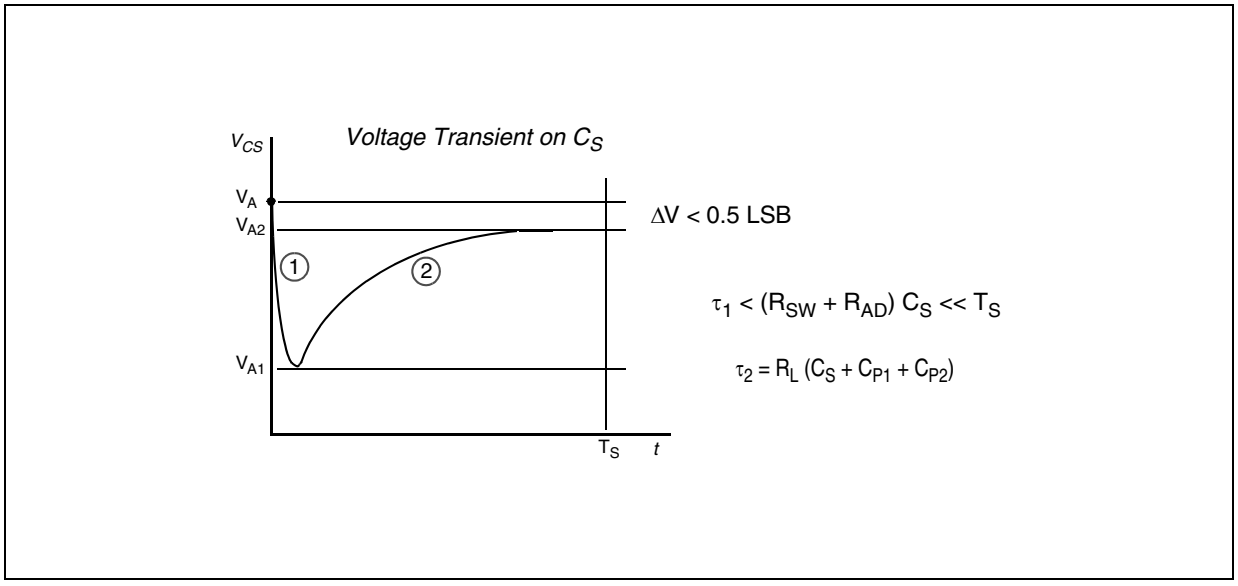


Figure 7. Transient Behavior during Sampling Phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Eqn. 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

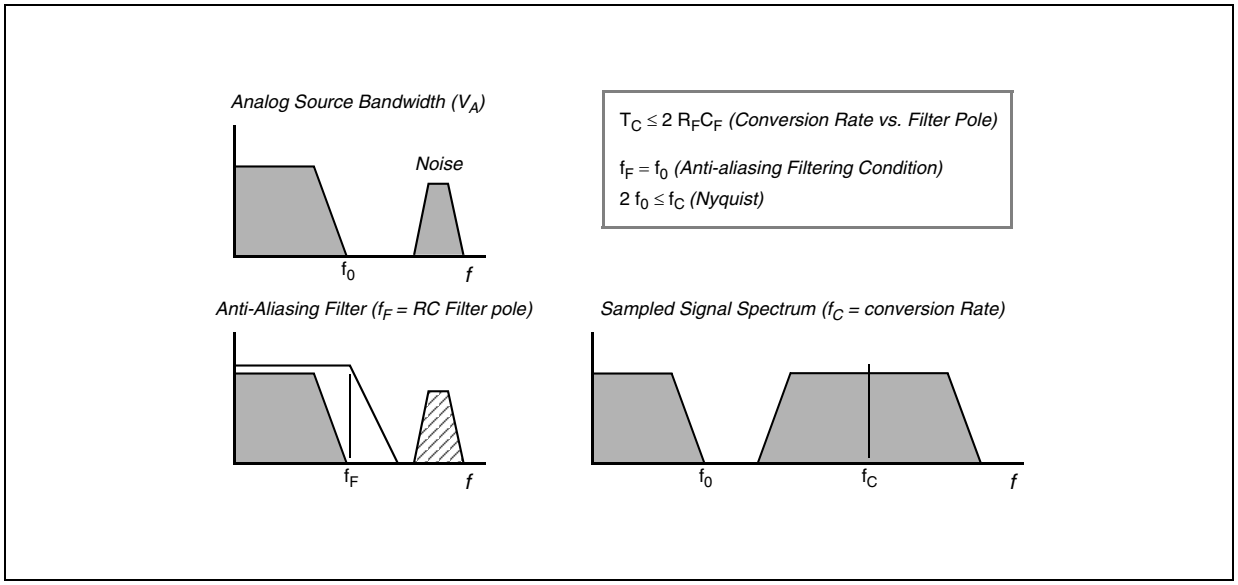


Figure 8. Spectral Representation of Input Signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 12

$$C_F > 2048 \bullet C_S$$

3.13.2 ADC Conversion Characteristics

Table 27. ADC Conversion Characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
f_{CK}	SR	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_ck[2] frequency)		3[3]	—	60	MHz
f_s	SR	Sampling frequency		—	—	1.53	MHz
t_{ADC_C}	P	Conversion time[4]	f_{ADC} = 20 MHz[5], ADC_conf_comp = 3	0.625	—	—	µs
C_S[6]	D	ADC input sampling capacitance		—	—	2.5	pF
C_{P1}[6]	D	ADC input pin capacitance 1		—	—	0.8[7]	pF
C_{P2}[6]	D	ADC input pin capacitance 2		—	—	1	pF
C_{P3}[6]	D	ADC input pin capacitance 3		—	—	1	pF
R_{SW1}[6]	D	Internal resistance of analog source		—	—	0.6	kΩ
R_{SW2}[6]	D	Internal resistance of analog source		—	—	0.7	kΩ
R_{AD}[6]	D	Internal resistance of analog source		—	—	2	kΩ
I_{INJ}	T	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE spec.	-3	—	3	mA
INL	P	Integral Non Linearity	No overload	-1.5	—	1.5	LSB
DNL	P	Differential Non Linearity	No overload	-1.0	—	1.0	LSB
OFS	T	Offset error		—	±1	—	LSB
GNE	T	Gain error		—	±1	—	LSB
TUE	P	Total unadjusted error		-3	—	3	LSB

1 V_{DD} = 3.3 V to 3.6 V / 5.0 V to 5.5 V, T_A = -40 to +125 °C, unless otherwise specified.

2 AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

3 When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which precision is lost.

4 This parameter does not include the sample time t_{ADC_S}, but only the time for determining the digital result and the time to load the result register with the conversion result.

5 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.

6 See Figure 6.

7 Does not include packaging and bonding capacitances

3.14 Flash Memory Electrical Characteristics

Table 28. Program and Erase Specifications[1]

Symbol		Parameter	Min Value	Typical Value[2]	Initial Max[3]	Max[4]	Unit
$T_{dwprogram}$	P	Double Word (64 bits) Program Time[5]	—	TBD	22	500	µs
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	—	TBD	500	5000	ms
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	—	TBD	600	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	—	TBD	1300	7500	ms

1 TBD: To be defined

2 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

3 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

4 The maximum program & erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

5 Actual hardware programming times. This does not include software overhead.

Table 29. Flash Module Life[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10,000	100,000 (TBD)	cycles
P/E	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1,000	100,000 (TBD)	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature[2]	Blocks with 0 - 1,000 P/E cycles	20	—	years
			Blocks with 10,000 P/E cycles	10	—	years
			Blocks with 100,000 P/E cycles	1 - 5 (TBD)	—	years

1 TBD: To be defined

2 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

3.15 AC Specifications

3.15.1 Pad AC Specifications

Table 30 gives the AC electrical characteristics at 5 V ($4.5\ V < V_{DD\_HV\_IOx} < 5.5\ V$, NVUSRO[PAD3V5V]=0) operation.

Table 30. Pad AC Specifications (5.0 V, NVUSRO[PAD3V5V]=0)[1]

No.		Pad	Rise/Fall[2] (ns)			Load drive (pF)
			Min	Typ	Max	
1	T	Slow	6	—	50	25
			9	—	100	50
			12	—	125	100
2	T	Medium	3	—	10	25
			5	—	20	50
			9	—	40	100
3	T	Fast	1	—	4	25
			1.5	—	6	50
			3	—	12	100
4	T	Symmetric	1	—	4	25
5	D	Pullup and pulldown (5.5 V max)	—	—	5000	50

1 Propagation delay from $V_{DD\_HV\_IOx}/2$ of internal signal to Pchannel/Nchannel switch-on condition

2 Slope at rising/falling edge

Table 31 gives the AC electrical characteristics at 3.3 V ($3.0\ V < V_{DD\_HV\_IOx} < 3.6\ V$, NVUSRO[PAD3V5V]=1) operation.

Table 31. Pad AC Specifications (3.3 V, INVUSRO[PAD3V5V]=1)[1]

No		Pad	Rise/Fall[2] (ns)			Load drive (pF)
			Min	Typ	Max	
1	T	Slow	4	—	40	25
			6	—	50	50
			10	—	75	100
2	T	Medium	2	—	12	25
			4	—	25	50
			8	—	40	100
3	T	Fast	1	—	4	25
			1.5	—	7	50
			3	—	12	100

Table 31. Pad AC Specifications (3.3 V, INVUSRO[PAD3V5V]=1)[1] (continued)

No		Pad	Rise/Fall[2] (ns)			Load drive (pF)
			Min	Typ	Max	
4	T	Symmetric	1	—	5	25
5	D	Pullup and pulldown (3.6 V max)	—	—	7500	50

1 Propagation delay from $V_{DD\_HV\_IOx}/2$ of internal signal to Pchannel/Nchannel switch-on condition

2 Slope at rising/falling edge

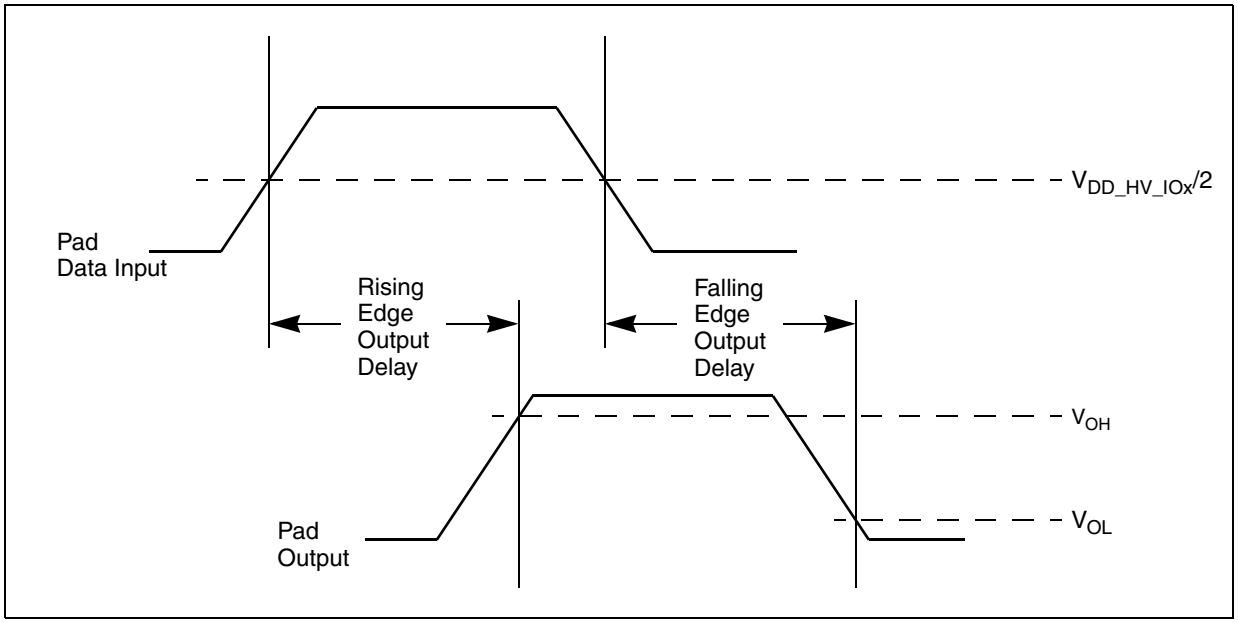


Figure 9. Pad Output Delay

3.16 AC Timing Characteristics

3.16.1 Generic Timing Diagrams

The generic timing diagrams in Figure 10 and Figure 11 apply to all I/O pins with pad types fast, slow and medium. See Section 2.2, “Pin Descriptions for the pad type for each pin.

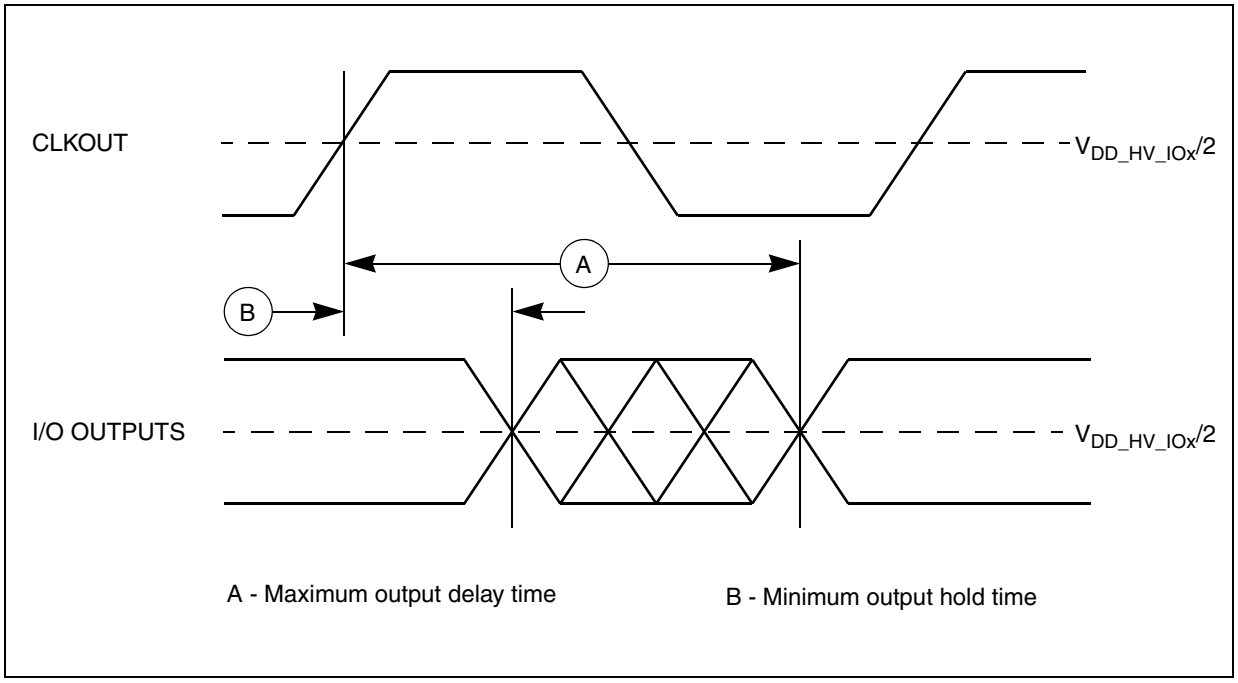


Figure 10. Generic Output Delay/Hold Timing

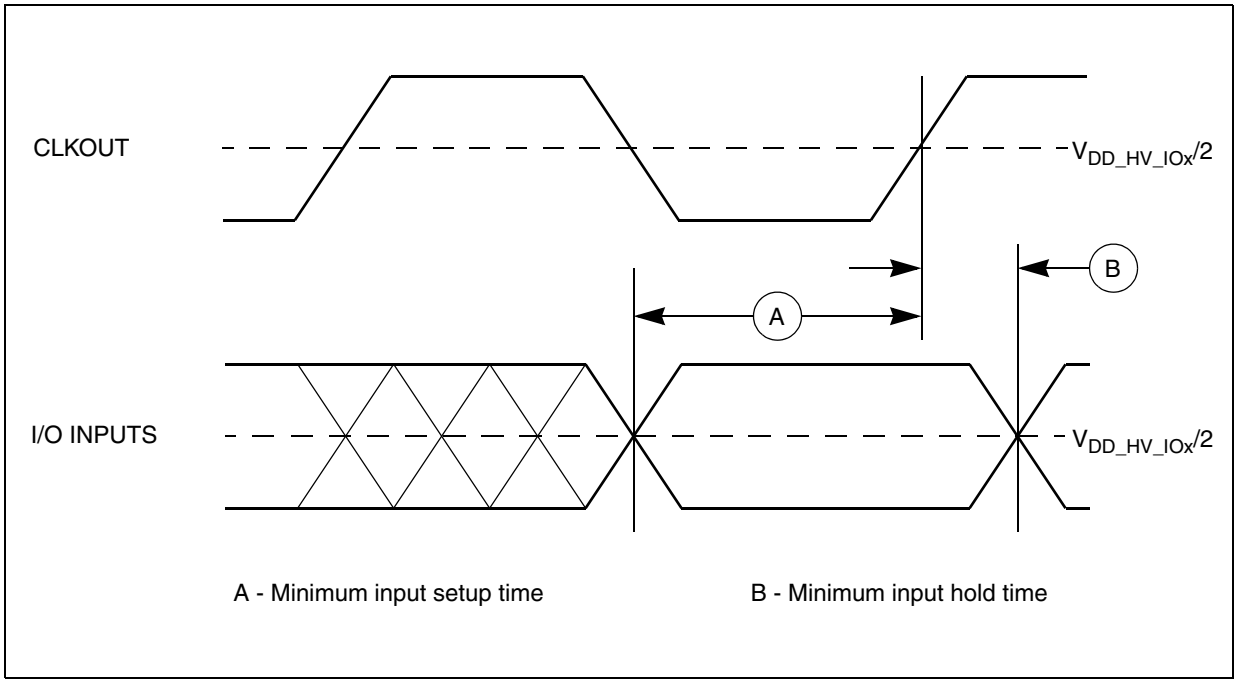


Figure 11. Generic Input Setup/Hold Timing

3.16.2 RESET_B Pin Characteristics

Table 32 gives the RESET_B pin characteristics at 5 V (4.5 V < $V_{DD\_HV\_IOx}$ < 5.5 V, NVUSRO[PAD3V5V]=0) operation.

Table 32. RESET_B Pin[1] and Wakeup Characteristics (3.3 V and 5.0 V)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	W_{FRST}	P	RESET pulse is sure to be filtered[2]	$V_{DD}=V_{DD\_LV\_CORx}$	—	40	ns
2	W_{NFRST}	P	RESET pulse is sure not to be filtered	$V_{DD}=V_{DD\_LV\_CORx}$	500	—	ns
3	W_{FWKUP}	P	Wakeup pulse is sure to be filtered	$V_{DD}=V_{DD\_LV\_CORx}$	—	45	ns
4	W_{NFWKUP}	P	Wakeup pulse is sure not to be filtered	$V_{DD}=V_{DD\_LV\_CORx}$	205	—	ns

1 The RESET_B pin is weak pull-up during reset.

2 Pulse in between 70 ns and 500 ns may be either filtered or provided.

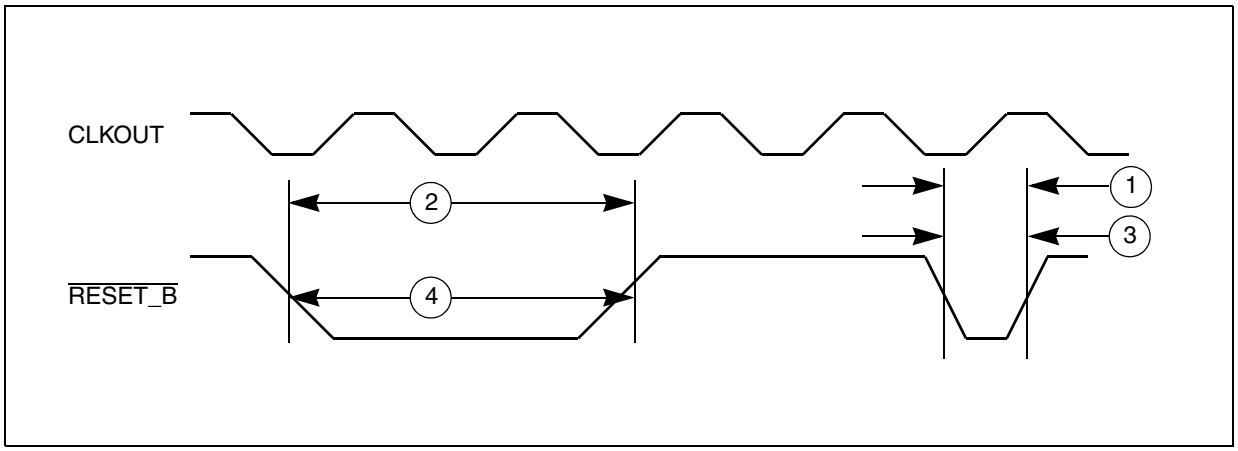


Figure 12. $\overline{\text{RESET\_B}}$ pin and Wakeup

4 Package Characteristics

4.1 Package Mechanical Data

4.1.1 144 LQFP Mechanical Outline Drawing

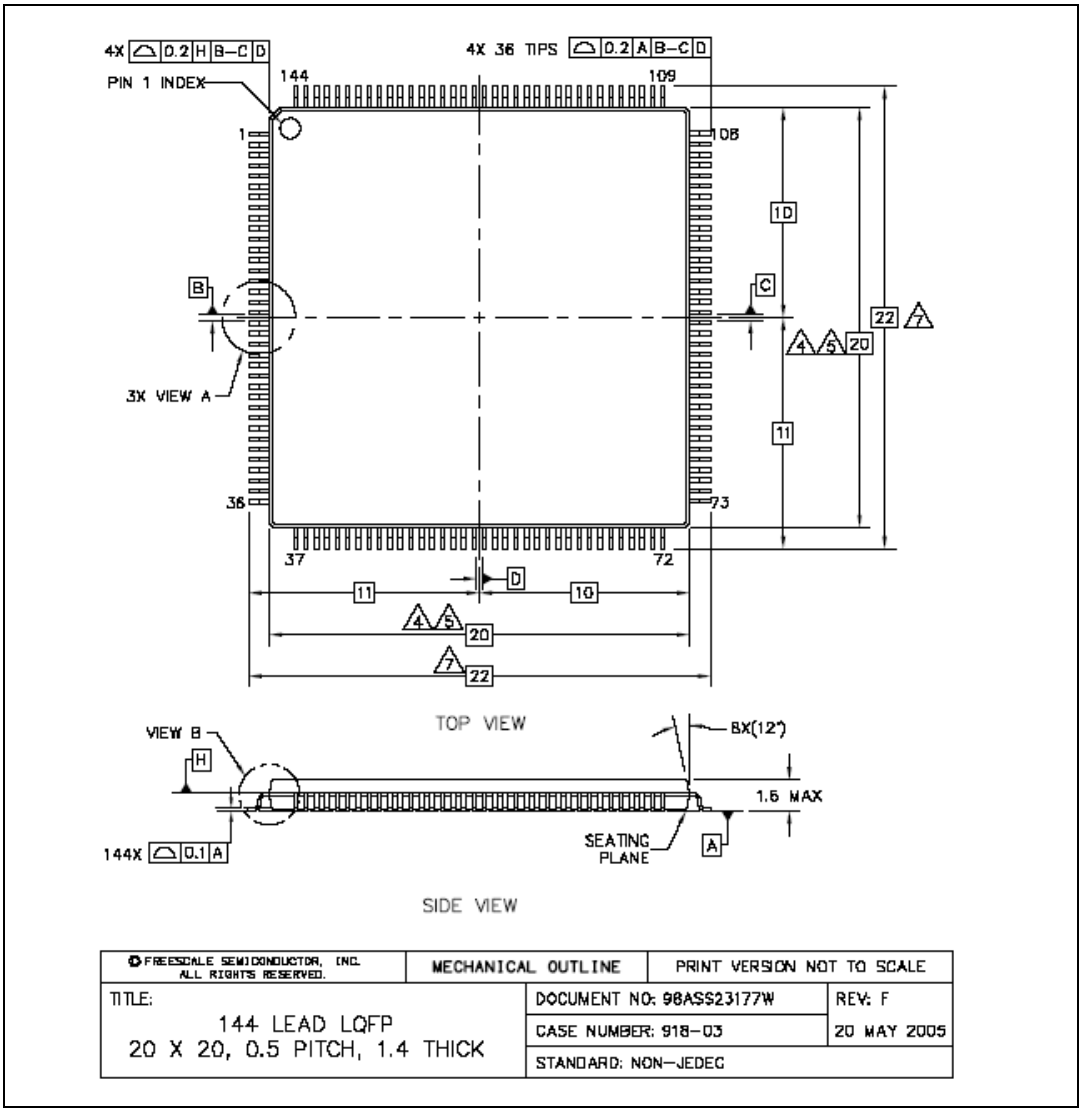


Figure 13. 144 LQFP Package Mechanical Drawing (part 1)

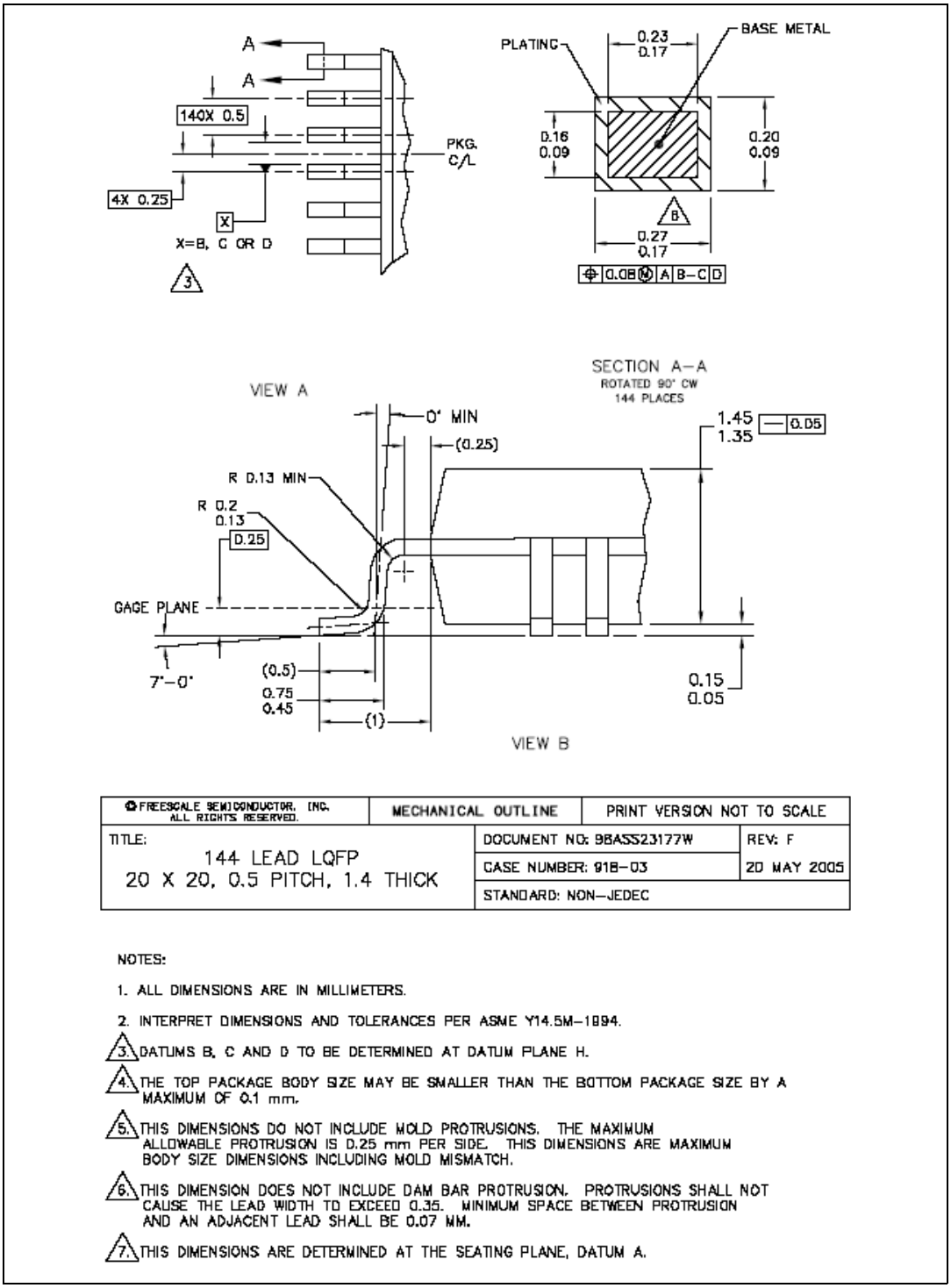


Figure 14. 144 LQFP Package Mechanical Drawing (part 2)

4.1.2 100 LQFP Mechanical Outline Drawing

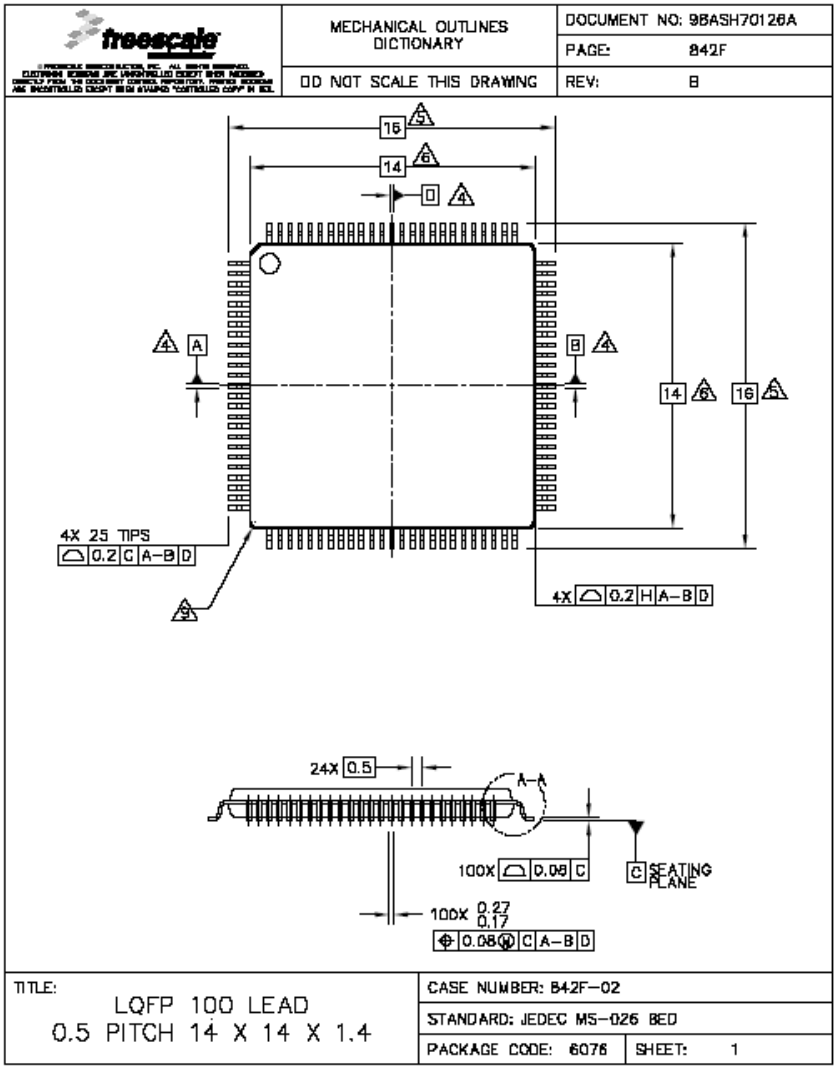


Figure 15. 100 LQFP Package Mechanical Drawing (part 1)

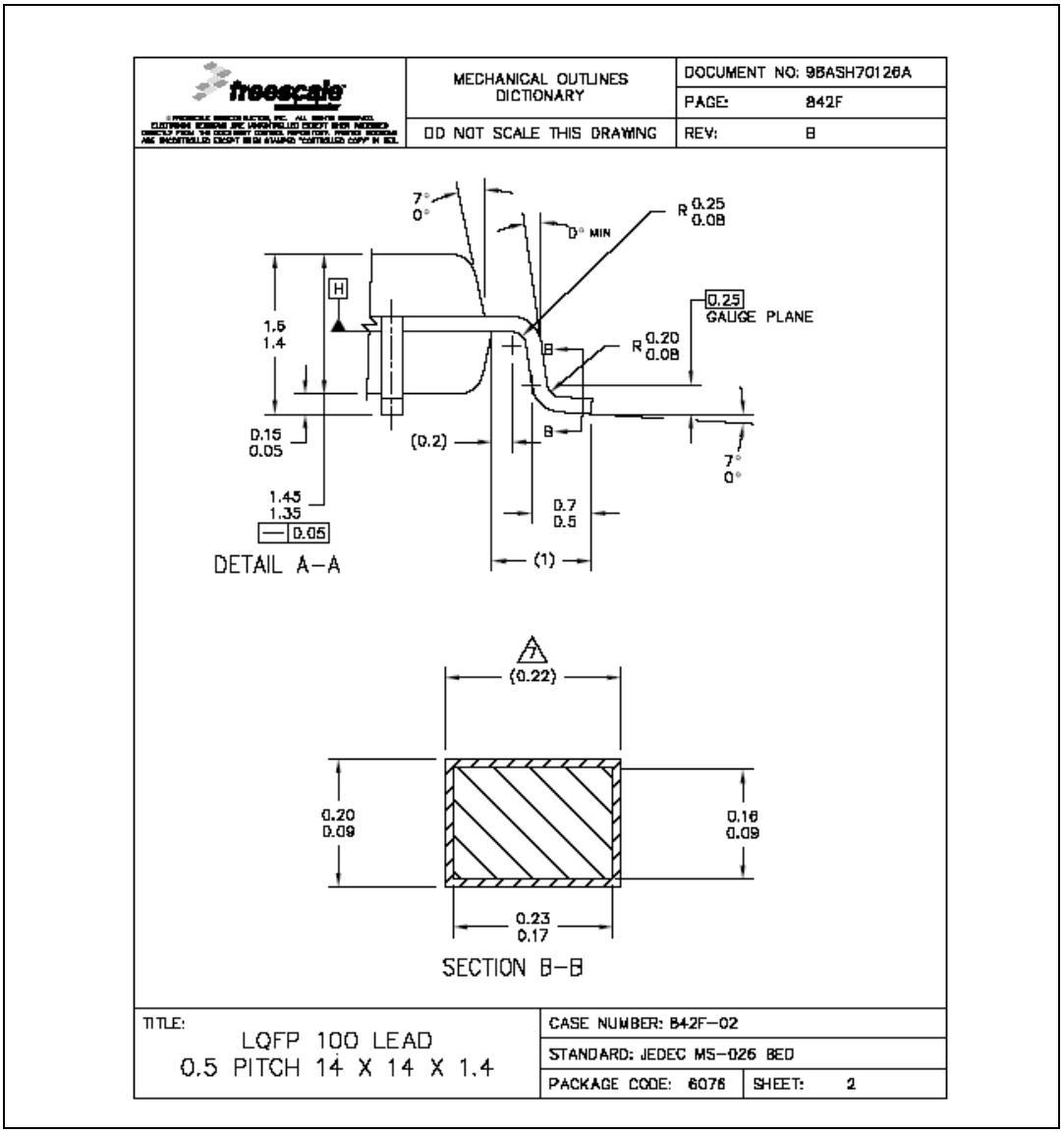
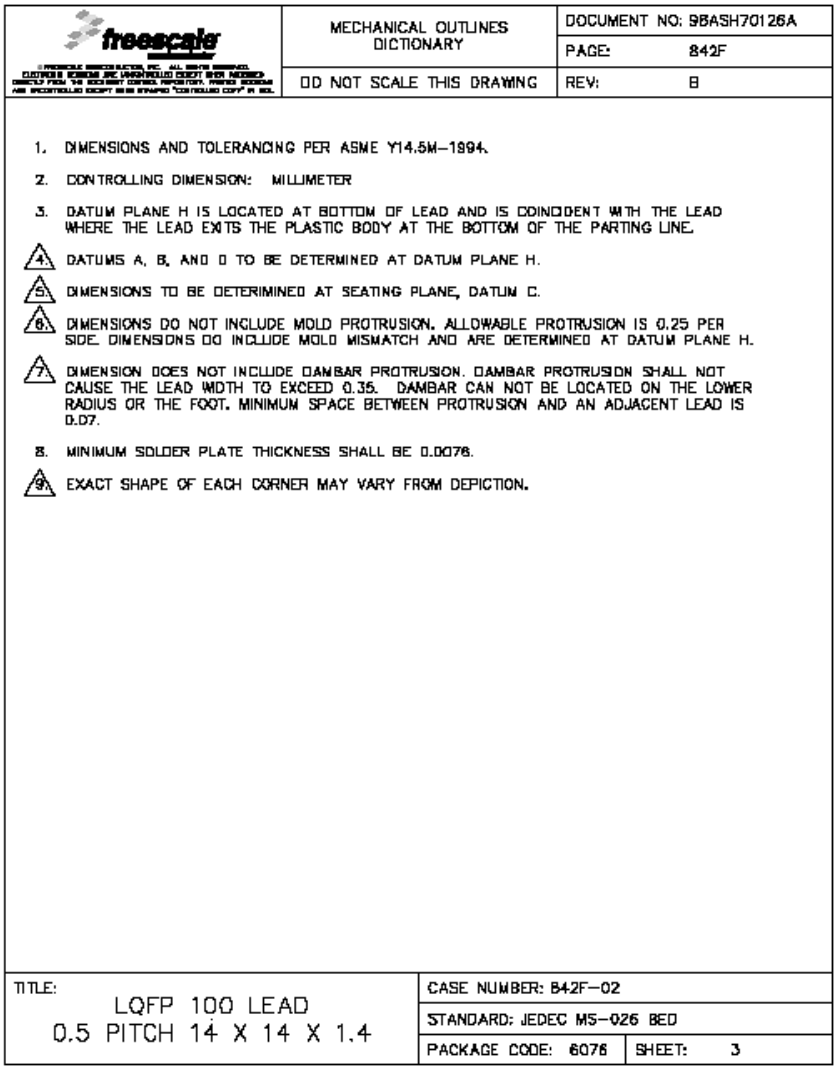


Figure 16. 100 LQFP Package Mechanical Drawing (part 2)



freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASH70126A
		PAGE: 842F
	DO NOT SCALE THIS DRAWING	REV: B

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERIMINED AT SEATING PLANE, DATUM C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

TITLE: LQFP 100 LEAD 0.5 PITCH 14 X 14 X 1.4	CASE NUMBER: 842F–02	
	STANDARD: JEDEC MS–026 BED	
	PACKAGE CODE: 6076	SHEET: 3

Figure 17. 100 LQFP Package Mechanical Drawing (part 3)

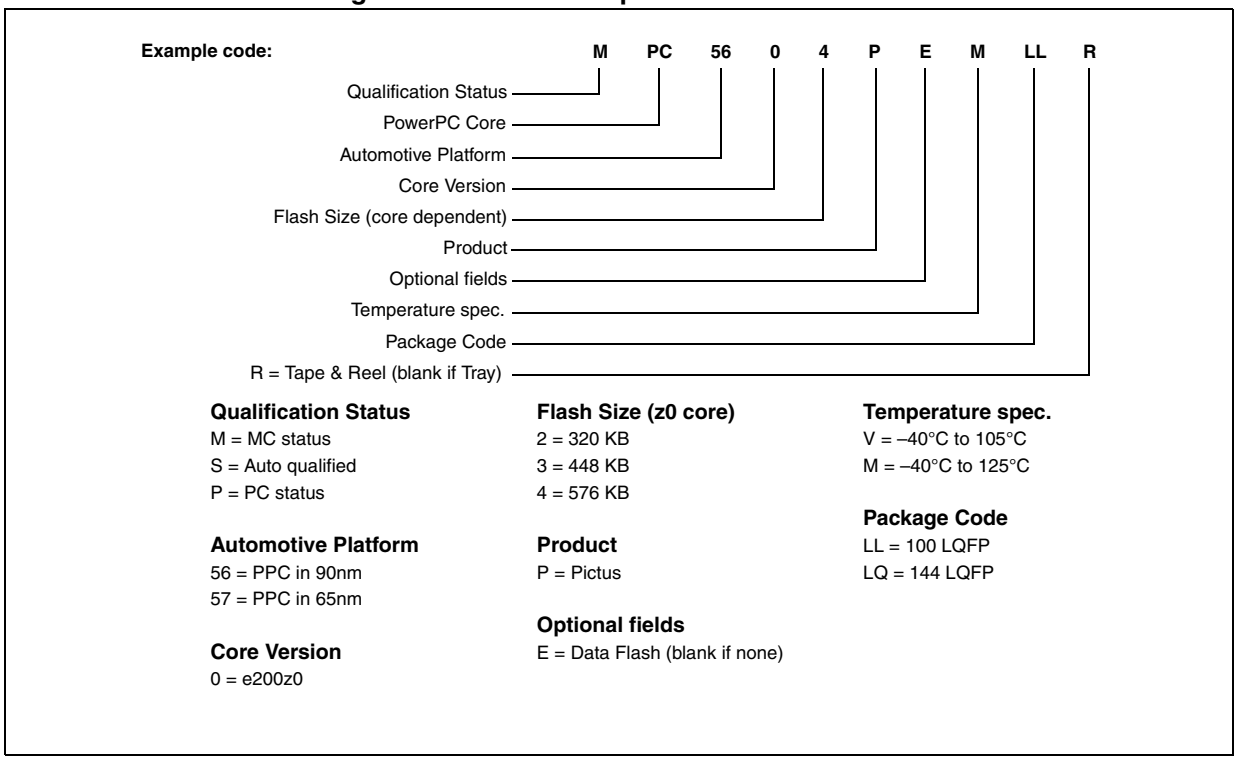
5 Ordering Information

Table 33 shows the orderable part numbers for the MPC5604P series.

Table 33. Orderable Part Number Summary

Part Number	Flash (KB)	SRAM (KB)	Package	Characteristics
MPC5604PEFMLQSPC560P50L5CEFA	576	40	144 LQFPLQFP144	Data flash; FlexRay; 5 V
SPC560P50L5CEFB	576	40	LQFP144	Data flash; FlexRay; 3.3 V
MPC5604PEFMLLSPC560P50L3CEFA	576	40	100 LQFPLQFP100	Data flash; FlexRay; 5 V
SPC560P50L3CEFB	576	40	LQFP100	Data flash; FlexRay; 3.3 V
MPC5603PEFMLQSPC560P44L5CEFA	448	32	144 LQFPLQFP144	Data flash; FlexRay; 5 V
SPC560P44L5CEFB	448	32	LQFP144	Data flash; FlexRay; 3.3 V
MPC5603PEFMLLSPC560P44L3CEFA	448	32	100 LQFPLQFP100	Data flash; FlexRay; 5 V
SPC560P44L3CEFB	448	32	LQFP100	Data flash; FlexRay; 3.3 V
MPC5602PEFMLQ	320	24	144 LQFP	Data flash; FlexRay
MPC5602PEFMLL	320	24	100 LQFP	Data flash; FlexRay

Figure 18. Commercial product code structure



6 Document Revision History

Table 34 summarizes revisions to this document.

Table 34. Revision history

Revision	Date	Substantive changes
Rev. 1	8/2008	Initial release
Rev. 2	11/2008	Table 5: TDO and TDI pins (Port pins B[4:5] are single function pins. Table 9, Table 10: Thermal characteristics added. Table 11, Table 12: EMI testing specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision. Table 17, Table 18, Table 20, Table 21: Supply current specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision. Table 19: • Values for I_{OL} and I_{OH} (in Conditions column) changed. • Max values for V_{OH_S}, V_{OH_M}, V_{OH_F} and V_{OH_SYM} deleted. • V_{ILR} max value changed. • I_{PUR} min and max values changed. Table 22: Sensitivity value changed. Table 32: Most values in table changed.
Rev. 3	2/2009	• Description of system requirements, controller characteristics and how controller characteristics are guaranteed updated. • Electrical parameters updated. • EMI characteristics are now in one table; values have been updated. • ESD characteristics are now in one table. • Electrical parameters are identified as either system requirements or controller characteristics. Method used to guarantee each controller characteristic is noted in table. • AC Timings: 1149.1 (JTAG) Timing, Nexus Timing, External Interrupt Timing, and DSPI Timing sections deleted

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