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MC68L11D3

Supplement to Technical Data
Low Voltage Devices

The MC68L11D3 is an extended-voltage version of the MC68HC11D3 microcontroller that can operate in applications that require supply voltages as low as 3.0 Volts. Operation of the MC68L11D3 is identical to that of the MC68HC11D3 in all aspects other than electrical parameters.

This document provides MC68L11D3 electrical characteristics. It is a supplement to Appendix A of the *MC68HC11D3 Technical Data* (MC68HC11D3/D). Refer to the data book for technical information regarding use and operation of the microcontroller. The extended-range electrical characteristics in this supplement will be incorporated into the data book in a subsequent revision.

Features

- Suitable for Battery-Powered Portable and Hand-Held Applications
- Excellent for use in Devices such as Remote Sensors and Actuators
- Reduced RF Noise
- Operating Performance is Same at 5V and 3V

Ordering Information

Package	Temperature	Frequency	Features	MC Order Number
44-Pin PLCC	0° to + 70° C	2 MHz	Custom ROM	MC68L11D3FN2
			No ROM	MC68L11D0FN2
44-Pin QFP	0° to + 70° C	2 MHz	Custom ROM	MC68L11D3FB2
			No ROM	MC68L11D0FB2

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SUPPLEMENT TO APPENDIX A ELECTRICAL CHARACTERISTICS: LOW VOLTAGE DEVICES

Table A–1a. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	– 0.3 to + 7.0	V
Input Voltage	V_{in}	– 0.3 to + 7.0	V
Operating Temperature Range MC68L11D3	T_A	T_L to T_H – 20 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C
Current Drain per Pin* Excluding V_{DD}, V_{SS}, AV_{DD}, V_{RH}, and V_{RL}	I_D	25	mA

*One pin at a time, observing maximum power dissipation limits.

Internal circuitry protects the inputs against damage caused by high static voltages or electric fields; however, normal precautions are necessary to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Extended operation at the maximum ratings can adversely affect device reliability. Tying unused inputs to an appropriate logic voltage level (either GND or V_{DD}) enhances reliability of operation.

Table A–2a. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Average Junction Temperature	T_J	$T_A + (P_D \times \Theta_{JA})$	°C
Ambient Temperature	T_A	User-determined	°C
Package Thermal Resistance (Junction-to-Ambient) 40-Pin Plastic DIP 44-Pin Plastic Leaded Chip Carrier (PLCC) 44-Pin Quad Flat Pack (QFP)	Θ_{JA}	 50 50 85	°C/W
Total Power Dissipation (Note 1)	P_D	$P_{INT} + P_{I/O}$ $K / (T_J + 273°C)$	W
Device Internal Power Dissipation	P_{INT}	$I_{DD} \times V_{DD}$	W
I/O Pin Power Dissipation (Note 2)	$P_{I/O}$	User-determined	W
A Constant (Note 3)	K	$P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2$	W · °C

NOTES:
1. This is an approximate value, neglecting $P_{I/O}$.
2. For most applications $P_{I/O} \ll P_{INT}$ and can be neglected.
3. K is a constant pertaining to the device. Solve for K with a known T_A and a measured P_D (at equilibrium). Use this value of K to solve for P_D and T_J iteratively for any value of T_A.

Table A–3a. DC Electrical Characteristics

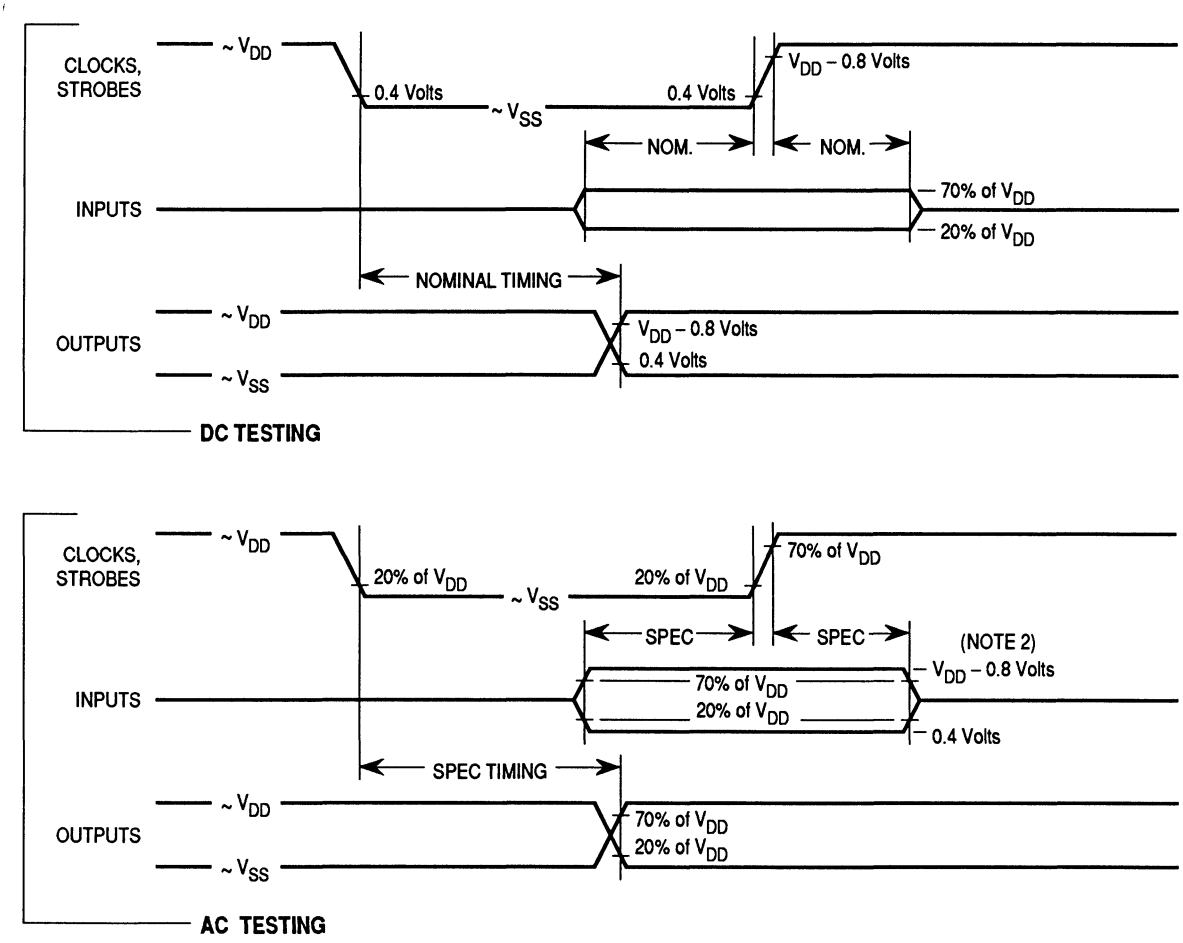
V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Characteristic	Symbol	Min	Max	Unit
Output Voltage (Note 1) All Outputs except XTAL	V_{OL}	—	0.1	V
All Outputs Except XTAL, RESET, and MODA I_{Load} = ± 10.0 µA	V_{OH}	V_{DD} – 0.1	—	V
Output High Voltage (Note 1) All Outputs Except XTAL, RESET, and MODA	V_{OH}	V_{DD} – 0.8	—	V
I_{Load} = – 0.5mA, V_{DD} = 3.0 V				
I_{Load} = – 0.8 mA, V_{DD} = 4.5 V				
Output Low Voltage All Outputs Except XTAL	V_{OL}	—	0.4	V
I_{Load} = 1.6 mA, V_{DD} = 5.0 V				
I_{Load} = 1.0 mA, V_{DD} = 3.0 V				
Input High Voltage All Inputs Except $\overline{\text{RESET}}$	V_{IH}	0.7 x V_{DD}	V_{DD} + 0.3	V
$\overline{\text{RESET}}$		0.8 x V_{DD}	V_{DD} + 0.3	V
Input Low Voltage All Inputs	V_{IL}	V_{SS} – 0.3	0.2 x V_{DD}	V
I/O Ports, Three-State Leakage PA7, PA3, PB[7:0], PC[7:0], PD[7:0],	I_{OZ}	—	±10	µA
V_{in} = V_{IH} or V_{IL} MODA/LIR, $\overline{\text{RESET}}$				
Input Leakage Current	I_{in}			
V_{in} = V_{DD} or V_{SS} PA[2:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$		—	±1	µA
V_{in} = V_{DD} or V_{SS} MODB/V_{STBY}		—	±10	µA
RAM Standby Voltage Power down	V_{SB}	2.0	V_{DD}	V
RAM Standby Current Power down	I_{SB}	—	10	µA
Input Capacitance PA[2:0], $\overline{\text{IRQ}}$, $\overline{\text{XIRQ}}$, $\overline{\text{EXTAL}}$	C_{in}	—	8	pF
PA7, PA3, PB[7:0], PC[7:0], PD[7:0], MODA/LIR, $\overline{\text{RESET}}$		—	12	pF
Output Load Capacitance All Outputs Except PD[4:1]	C_L	—	90	pF
PD[4:1]		—	100	pF

Characteristic		Symbol	1 MHz	2 MHz	Unit
Maximum Total Supply Current (Note 2)					
RUN:		I_{DD}			
Single-Chip Mode	V_{DD} = 5.5 V		8	15	mA
	V_{DD} = 3.0 V		4	8	mA
Expanded Multiplexed Mode	V_{DD} = 5.5 V		14	27	mA
	V_{DD} = 3.0 V		7	14	mA
WAIT: (All Peripheral Functions Shut Down)		W_{IDD}			
Single-Chip Mode	V_{DD} = 5.5 V		3	6	mA
	V_{DD} = 3.0 V		1.5	3	mA
Expanded Multiplexed Mode	V_{DD} = 5.5 V		5	10	mA
	V_{DD} = 3.0 V		2.5	5	mA
STOP:		S_{IDD}			
Single-Chip Mode, No Clocks	V_{DD} = 5.5 V		50	50	µA
	V_{DD} = 3.0 V		25	25	µA
Maximum Power Dissipation		P_D			
Single-Chip Mode	V_{DD} = 5.5 V		44	85	mW
	V_{DD} = 3.0 V		12	24	mW
Expanded Multiplexed Mode	V_{DD} = 5.5 V		77	150	mW
	V_{DD} = 3.0 V		21	42	mW

NOTES:

1. V_{OH} specification for $\overline{\text{RESET}}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wired-OR mode.
2. EXTAL is driven with a square wave, and
   t_{cyc} = 1000 ns for 1 MHz rating; t_{cyc} = 500 ns for 2 MHz rating;
   $V_{IL} \le 0.2$ V; $V_{IH} \ge V_{DD} - 0.2$ V; No dc loads.



NOTES:
1. Full test loads are applied during all DC electrical tests and AC timing measurements.
2. During AC timing measurements, inputs are driven to 0.4 volts and V_{DD} – 0.8 volts while timing measurements are taken at the 20% and 70% of V_{DD} points.

Figure A–1. Test Methods

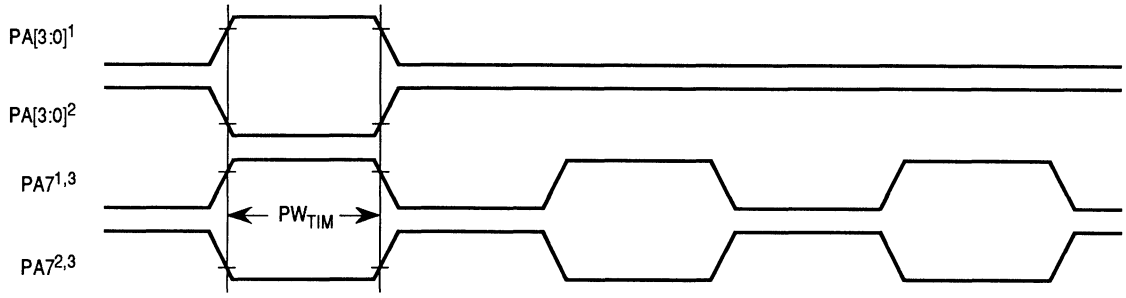
Table A–4a. Control Timing

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
		Min	Max	Min	Max	
Frequency of Operation	f_o	dc	1.0	dc	2.0	MHz
E-Clock Period	t_{cyc}	1000	—	500	—	ns
Crystal Frequency	f_{XTAL}	—	4.0	—	8.0	MHz
External Oscillator Frequency	$4 f_o$	dc	4.0	dc	8.0	MHz
Processor Control SetupTime t_{PCSU} = 1/4 t_{cyc} + 75 ns	t_{PCSU}	325	—	200	—	ns
Reset Input Pulse Width To Guarantee External Reset Vector Minimum Input Time (Can Be Preempted by Internal Reset)	PW_{RSTL}	 8 1	 — —	 8 1	 — —	 t_{cyc} t_{cyc}
Mode Programming Setup Time	t_{MPS}	2	—	2	—	t_{cyc}
Mode Programming Hold Time	t_{MPH}	10	—	10	—	ns
Interrupt Pulse Width, $\overline{IRQ}$ Edge-Sensitive Mode $PW_{IRQ} = t_{cyc} + 20$ ns	PW_{IRQ}	1020	—	520	—	ns
Wait Recovery Startup Time	t_{WRS}	—	4	—	4	t_{cyc}
Timer Pulse Width, Input Capture Pulse Accumulator Input $PW_{TIM} = t_{cyc} + 20$ ns	PW_{TIM}	1020	—	520	—	ns

NOTES:

1. RESET is recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt. Refer to **SECTION 5 RESETS AND INTERRUPTS** for further detail.
2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.



NOTES:

1. Rising edge sensitive input
2. Falling edge sensitive input
3. Maximum pulse accumulator clocking rate is E-clock frequency divided by 2.

Figure A–2. Timer Inputs

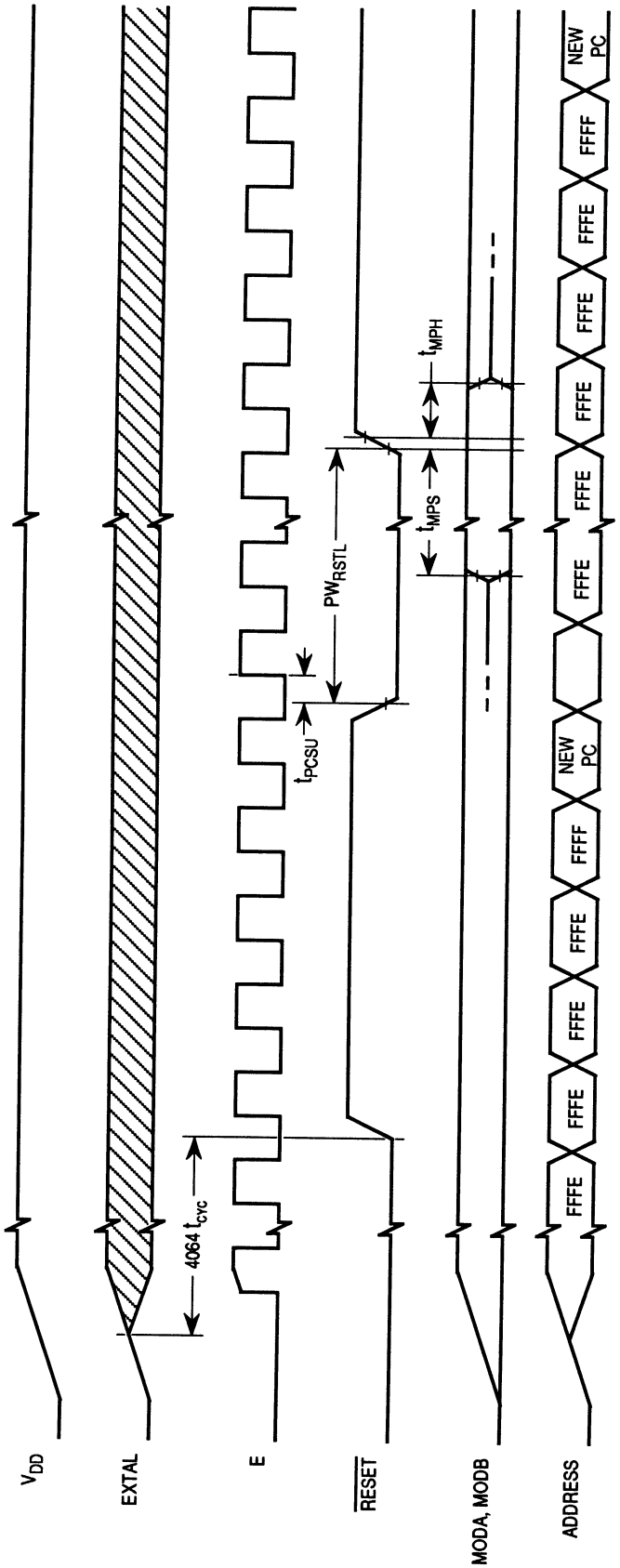
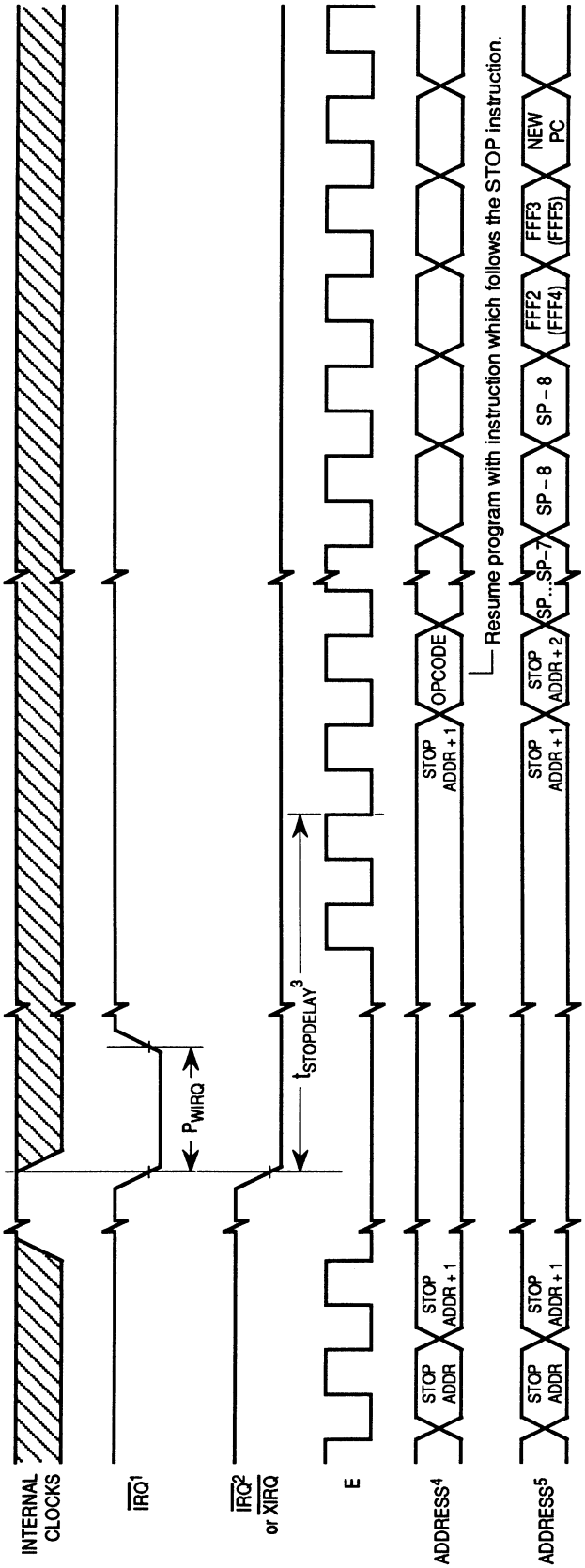
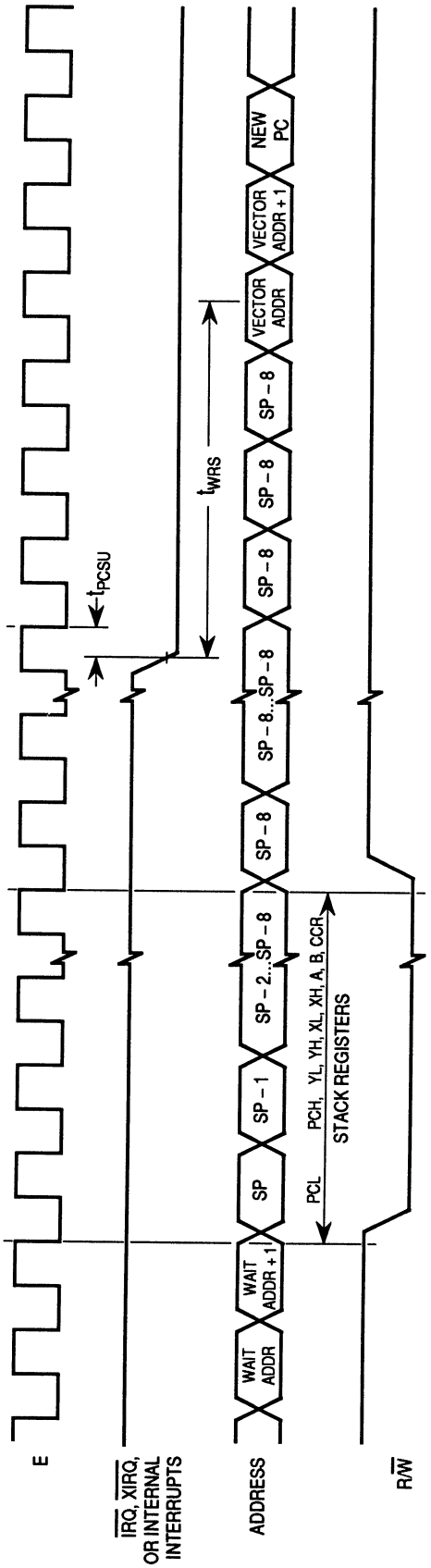


Figure A–3. POR External Reset Timing Diagram



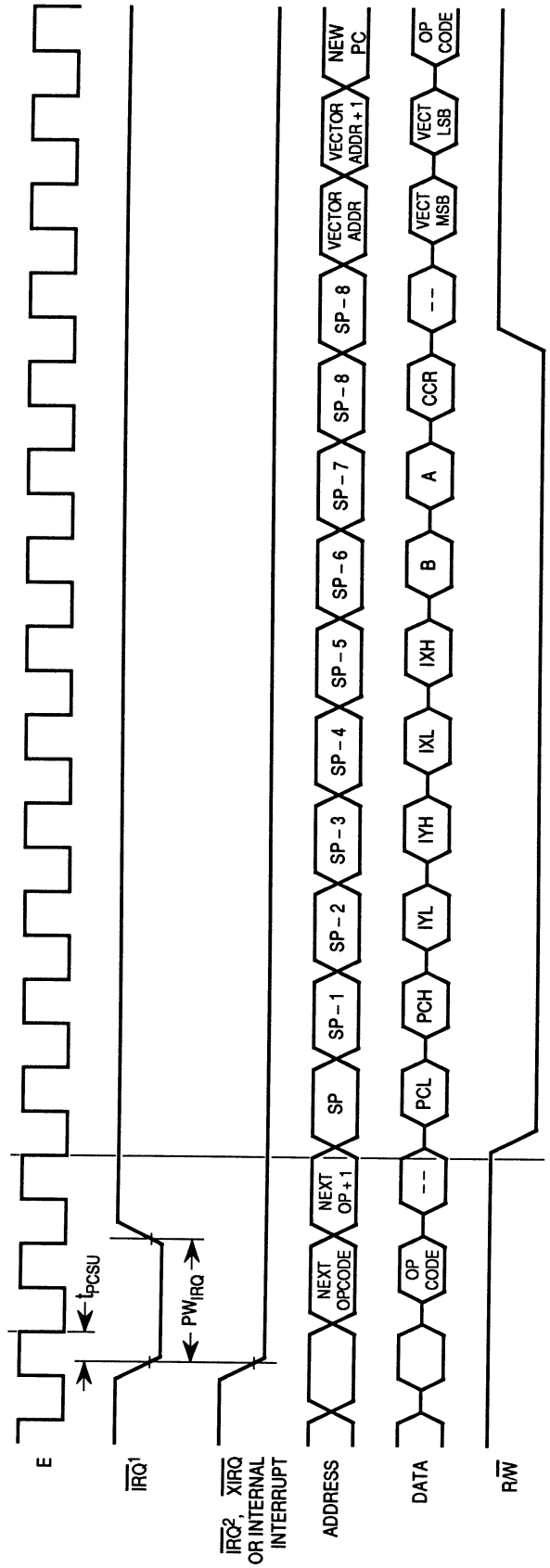
NOTES:
1. Edge Sensitive $\overline{IRQ}$ pin (IRQE bit = 1)
2. Level sensitive $\overline{IRQ}$ pin (IRQE bit = 0)
3. $t_{STOPDELAY}$ = 4064 t_{CYC} if DLY bit = 1 or 4 t_{CYC} if DLY = 0.
4. $\overline{XIRQ}$ with X bit in CCR = 1.
5. $\overline{IRQ}$ or ($\overline{XIRQ}$ with X bit in CCR = 0).

Figure A–4. STOP Recovery Timing Diagram



NOTE: $\overline{\text{RESET}}$ also causes recovery from WAIT.

Figure A–5. WAIT Recovery from Interrupt Timing Diagram



NOTES:
1. Edge sensitive $\overline{IRQ}$ pin (IRQE bit = 1)
2. Level sensitive $\overline{IRQ}$ pin (IRQE bit = 0)

Figure A–6. Interrupt Timing Diagram

Table A–5a. Peripheral Port Timing

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
		Min	Max	Min	Max	
Frequency of Operation (E-Clock Frequency)	f_o	dc	1.0	dc	2.0	MHz
E-Clock Period	t_{cyc}	1000	—	500	—	ns
Peripheral Data Setup Time MCU Read of Ports A, B, C, and D	t_{PDSU}	100	—	100	—	ns
Peripheral Data Hold Time MCU Read of Ports A, B, C, and D	t_{PDH}	50	—	50	—	ns
Delay Time, Peripheral Data Write MCU Write to Port A MCU Writes to Ports B, C, and D t_{PWD} = 1/4 t_{cyc} + 150 ns	t_{PWD}	 — —	 250 400	 — —	 250 275	 ns ns

NOTES:
1. Port C and D timing is valid for active drive (CWOM and DWOM bits not set in PIOC and SPCR registers respectively).
2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.

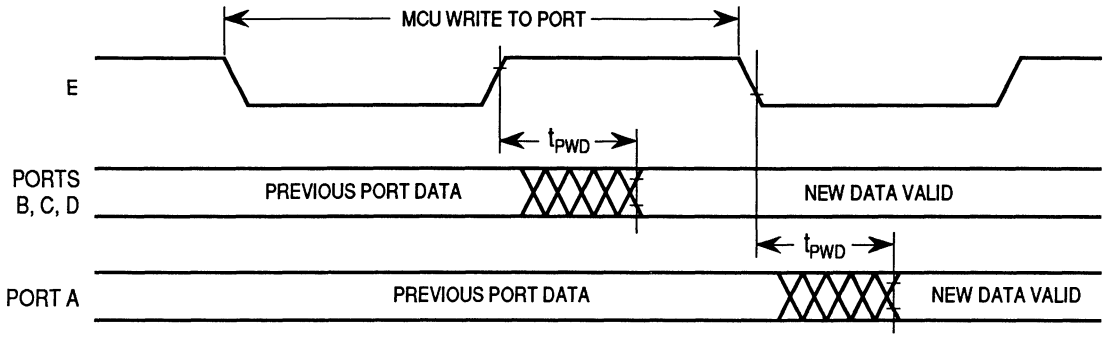


Figure A–7. Port Write Timing Diagram

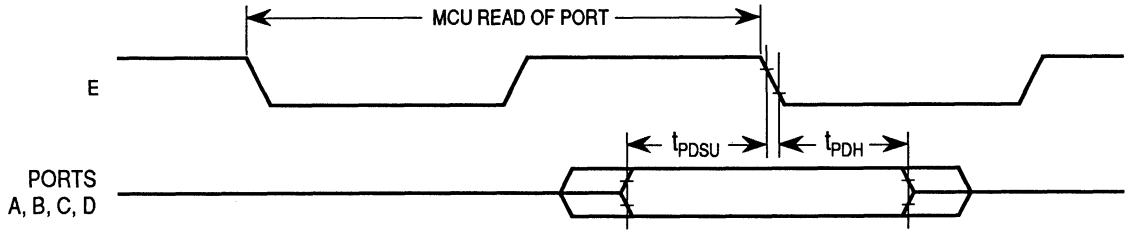


Figure A–8. Port Read Timing Diagram

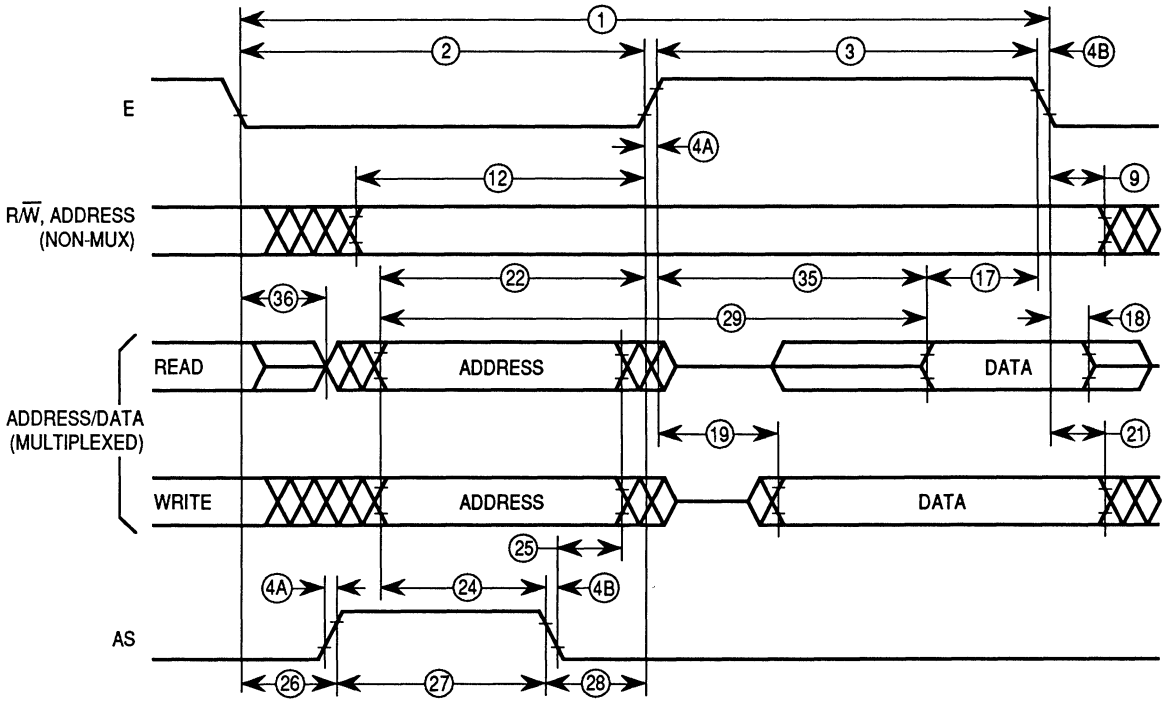
Table A–6a. Expansion Bus Timing

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Num	Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
			Min	Max	Min	Max	
	Frequency of Operation (E-Clock Frequency)	f_o	dc	1.0	dc	2.0	MHz
1	Cycle Time	t_{cyc}	1000	—	500	—	ns
2	Pulse Width, E Low PW_{EL} = 1/2 t_{cyc} – 25 ns	PW_{EL}	475	—	225	—	ns
3	Pulse Width, E High PW_{EH} = 1/2 t_{cyc} – 30 ns	PW_{EH}	470	—	220	—	ns
4A 4B	E and AS Rise Time E and AS Fall Time	t_r t_f	— —	25 25	— —	25 25	ns ns
9	Address Hold Time t_{AH} = 1/8 t_{cyc} – 30 ns (Note 1a)	t_{AH}	95	—	33	—	ns
12	Non-Muxed Address Valid Time to E Rise $t_{AV} = PW_{EL} – (t_{ASD} + 80$ ns) (Note 1a)	t_{AV}	275	—	88	—	ns
17	Read Data Setup Time	t_{DSR}	30	—	30	—	ns
18	Read Data Hold Time (Max = t_{MAD})	t_{DHR}	0	150	0	88	ns
19	Write Data Delay Time t_{DDW} = 1/8 t_{cyc} + 70 ns (Note 1a)	t_{DDW}	—	195	—	133	ns
21	Write Data Hold Time t_{DHW} = 1/8 t_{cyc} – 30 ns (Note 1a)	t_{DHW}	95	—	33	—	ns
22	Muxed Address Valid Time to E Rise $t_{AVM} = PW_{EL} – (t_{ASD} + 90$ ns) (Note 1a)	t_{AVM}	265	—	78	—	ns
24	Muxed Address Valid Time to AS Fall $t_{ASL} = PW_{ASH} – 70$ ns	t_{ASL}	150	—	25	—	ns
25	Muxed Address Hold Time t_{AHL} = 1/8 t_{cyc} – 30 ns (Note 1b)	t_{AHL}	95	—	33	—	ns
26	Delay Time, E to AS Rise t_{ASD} = 1/8 t_{cyc} – 5 ns (Note 1a)	t_{ASD}	120	—	58	—	ns
27	Pulse Width, AS High PW_{ASH} = 1/4 t_{cyc} – 30 ns	PW_{ASH}	220	—	95	—	ns
28	Delay Time, AS to E Rise t_{ASED} = 1/8 t_{cyc} – 5 ns (Note 1b)	t_{ASED}	120	—	58	—	ns
29	MPU Address Access Time (Note 1a) $t_{ACCA} = t_{cyc} – (PW_{EL} – t_{AVM}) – t_{DSR} – t_f$	t_{ACCA}	735	—	298	—	ns
35	MPU Access Time $t_{ACCE} = PW_{EH} – t_{DSR}$	t_{ACCE}	—	440	—	190	ns
36	Muxed Address Delay (Previous Cycle MPU Read) $t_{MAD} = t_{ASD} + 30$ ns (Note 1a)	t_{MAD}	150	—	88	—	ns

NOTES:

1. Input clocks with duty cycles other than 50% affect bus performance. Timing parameters affected by input clock duty cycle are identified by (a) and (b). To recalculate the approximate bus timing values, substitute the following expressions in place of 1/8 t_{cyc} in the above formulas, where applicable:
   (a) (1-DC) × 1/4 t_{cyc}
   (b) DC × 1/4 t_{cyc}
   Where:
   DC is the decimal value of duty cycle percentage (high time).
2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.



NOTE: Measurement points shown are 20% and 70% of V_{DD}.

Figure A–9. Multiplexed Expansion Bus Timing Diagram

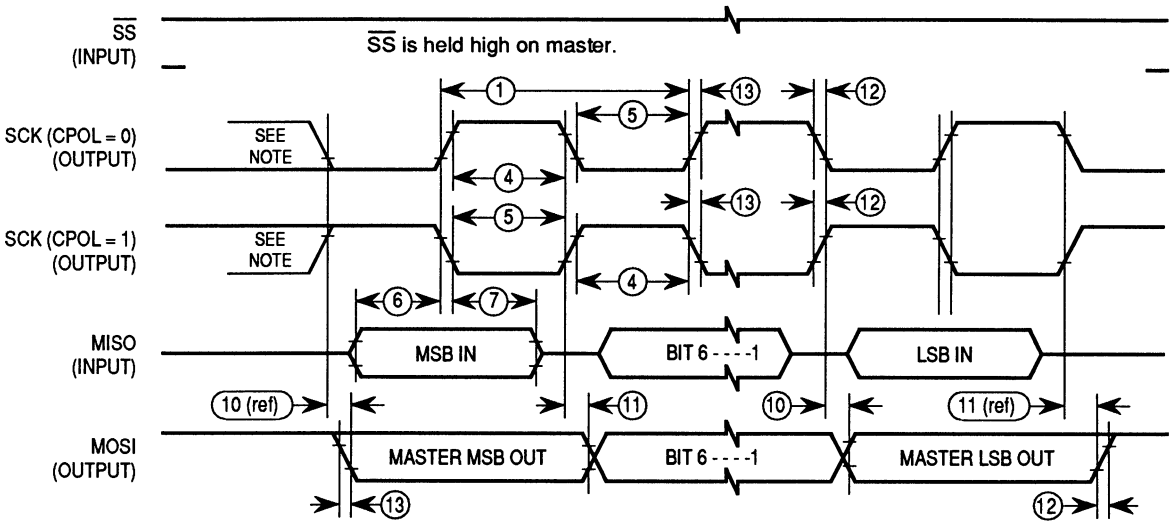
Table A–7a. Serial Peripheral Interface Timing

V_{DD} = 3.0 Vdc to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H

Num	Characteristic	Symbol	1.0 MHz		2.0 MHz		Unit
			Min	Max	Min	Max	
	Operating Frequency Master Slave	$f_{op(m)}$ $f_{op(s)}$	dc dc	0.5 1.0	dc dc	0.5 2.0	f_{op} MHz
1	Cycle Time Master Slave	$t_{cyc(m)}$ $t_{cyc(s)}$	2.0 1000	— —	2.0 500	— —	t_{cyc} ns
2	Enable Lead Time Master (Note 2) Slave	$t_{lead(m)}$ $t_{lead(s)}$	— 500	— —	— 250	— —	ns ns
3	Enable Lag Time Master (Note 2) Slave	$t_{lag(m)}$ $t_{lag(s)}$	— 500	— —	— 250	— —	ns ns
4	Clock (SCK) High Time Master Slave	$t_{w(SCKH)m}$ $t_{w(SCKH)s}$	680 380	— —	340 190	— —	ns ns
5	Clock (SCK) Low Time Master Slave	$t_{w(SCKL)m}$ $t_{w(SCKL)s}$	680 380	— —	340 190	— —	ns ns
6	Data Setup Time (Inputs) Master Slave	$t_{su(m)}$ $t_{su(s)}$	100 100	— —	100 100	— —	ns ns
7	Data Hold Time (Inputs) Master Slave	$t_{h(m)}$ $t_{h(s)}$	100 100	— —	100 100	— —	ns ns
8	Access Time (Time to Data Active from High-Imp. State) Slave	t_a	0	120	0	120	ns
9	Disable Time (Hold Time to High-Impedance State) Slave	t_{dis}	—	240	—	240	ns
10	Data Valid (After Enable Edge) (Note 3)	$t_{v(s)}$	—	240	—	240	ns
11	Data Hold Time (Outputs) (After Enable Edge)	t_{ho}	0	—	0	—	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	t_{rm} t_{rs}	— —	100 2.0	— —	100 2.0	ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	t_{fm} t_{fs}	— —	100 2.0	— —	100 2.0	ns µs

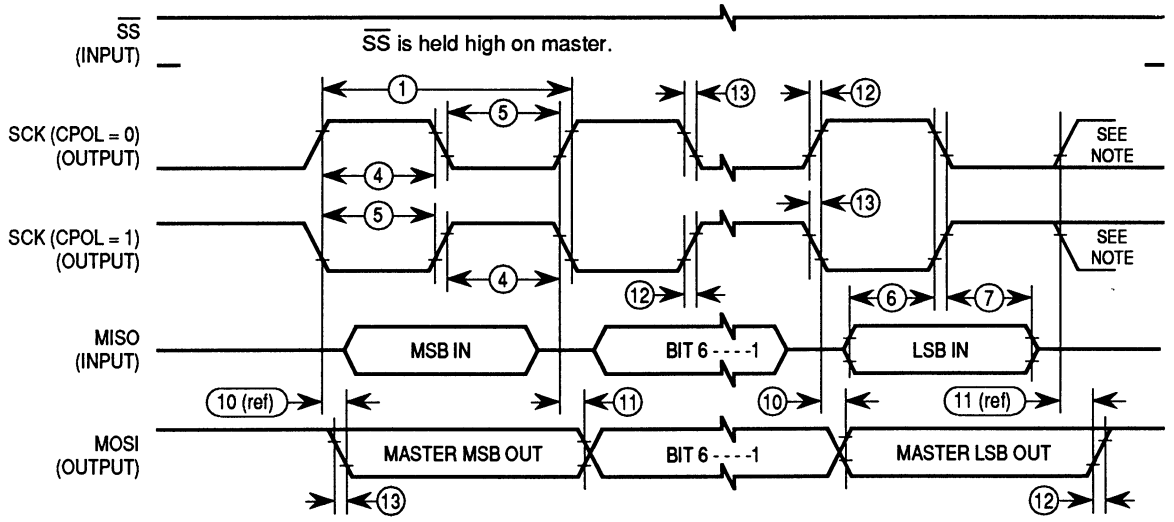
NOTES:

1. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Signal production depends on software.
3. Assumes 100 pF load on all SPI pins.



NOTE: This first clock edge is generated internally but is not seen at the SCK pin.

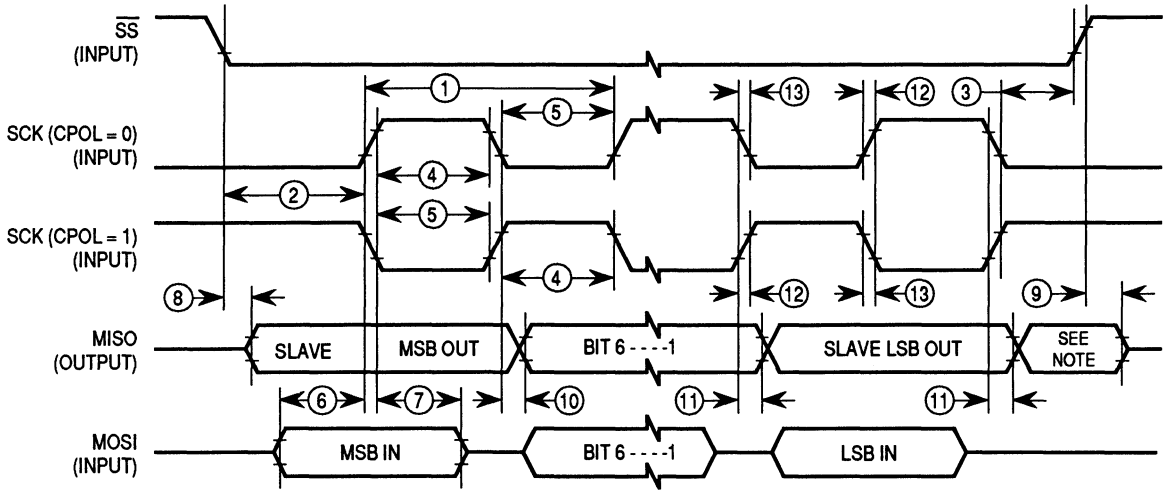
a) SPI Master Timing (CPHA = 0)



NOTE: This last clock edge is generated internally but is not seen at the SCK pin.

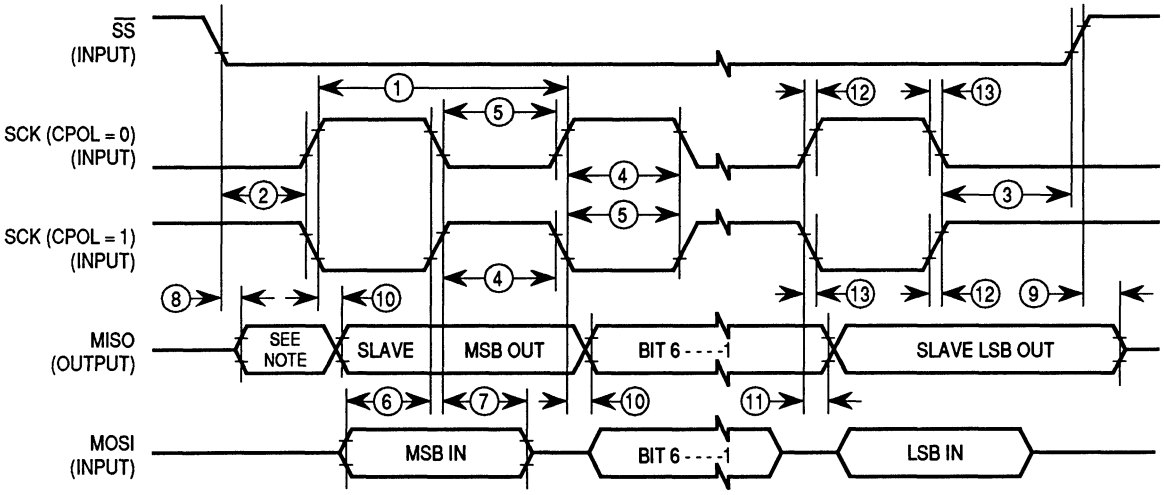
b) SPI Master Timing (CPHA = 1)

Figure A–10. SPI Timing Diagram (1 of 2)



NOTE: Not defined but normally MSB of character just received.

a) SPI Slave Timing (CPHA = 0)



NOTE: Not defined but normally LSB of character previously transmitted.

b) SPI Slave Timing (CPHA = 1)

Figure A–10. SPI Timing Diagram (2 of 2)

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