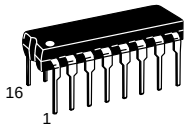
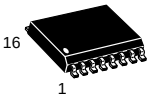
MC68HC68T1

Real-Time Clock plus RAM with Serial Interface

CMOS



P SUFFIX
PLASTIC DIP
CASE 648

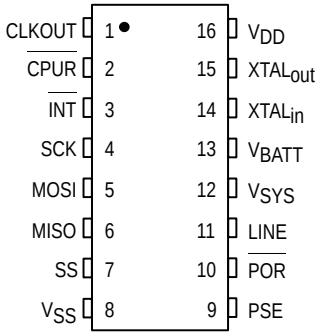


DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

MC68HC68T1P	Plastic DIP
MC68HC68T1DW	SOG Package

PIN ASSIGNMENT



The MC68HC68T1 HCMOS Clock/RAM peripheral contains a real–time clock/calendar, a 32 x 8 static RAM, and a synchronous, serial, three–wire interface for communication with a microcontroller or processor. Operating in a burst mode, successive Clock/RAM locations can be read or written using only a single starting address. An on–chip oscillator allows acceptance of a selectable crystal frequency or the device can be programmed to accept a 50/60 Hz line input frequency.

The LINE and system voltage (V_{SYS}) pins give the MC68HC68T1 the capability for sensing power–up/power–down conditions, a capability useful for battery–backup systems. The device has an interrupt output capable of signaling a microcontroller or processor of an alarm, periodic interrupt, or power sense condition. An alarm can be set for comparison with the seconds, minutes, and hours registers. This alarm can be used in conjunction with the power supply enable (PSE) output to initiate a system power–up sequence if the V_{SYS} pin is powered to the proper level.

A software power–down sequence can be initiated by setting a bit in the interrupt control register. This applies a reset to the CPU via the CPUR pin, sets the clock out (CLKOUT) and PSE pins low, and disables the serial interface. This condition is held until a rising edge is sensed on the V_{SYS} input pin, signaling system power coming on, or by activation of a previously enabled interrupt if the V_{SYS} pin is powered up.

A watchdog circuit can be enabled that requires the microcontroller or processor to toggle the slave select (SS) pin of the MC68HC68T1 periodically without performing a serial transfer. If this condition is not met, the CPUR line resets the CPU.

- Full Clock Features — Seconds, Minutes, Hours (AM/PM), Day–of–Week, Date, Month, Year (0 – 99), Auto Leap Year
- 32–Byte General Purpose RAM
- Direct Interface to Motorola SPI and National MICROWIRE™ Serial Data Ports
- Minimum Timekeeping Voltage: 2.2 V
- Burst Mode for Reading/Writing Successive Addresses in Clock/RAM
- Selectable Crystal or 50/60 Hz Line Input Frequency
- Clock Registers Utilize BCD Data
- Buffered Clock Output for Driving CPU Clock, Timer, Colon, or LCD Backplane
- Power–On Reset with First Time–Up Bit
- Freeze Circuit Eliminates Software Overhead During a Clock Read
- Three Independent Interrupt Modes — Alarm, Periodic, or Power–Down
- CPU Reset Output — Provides Orderly Power–Up/Power–Down
- Watchdog Circuit
- Pin–for–Pin Replacement for CDP68HC68T1
- Chip Complexity: 8500 FETs or 2125 Equivalent Gates
- Also See Application Notes ANE425 “Use of the MC68HC68T1 RTC with M6805 Microprocessor”, AN457 “Providing a Real–Time Clock for the MC68302”, and AN1065 “Use of the MC68HC68T1 Real–Time Clock with Multiple Time Bases”

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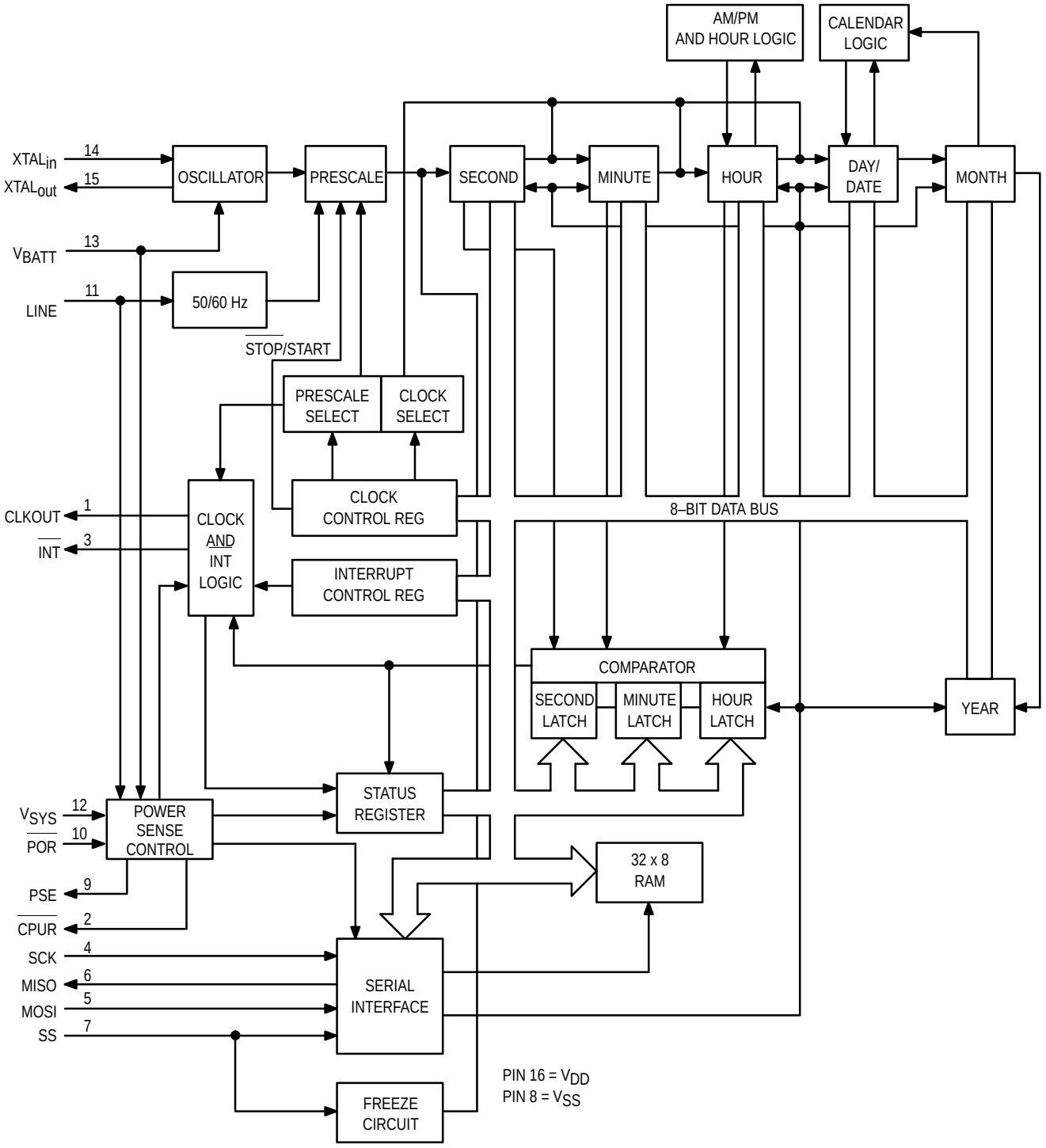
MOTOROLA

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (except Line Input**)	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package***	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (10–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
** See Electrical Characteristics Table.
*** Power Dissipation Temperature Derating: — 12 mW/°C from 65 to 85°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (T_A = – 40 to + 85°C, Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	3.0 to 6.0	V
$V_{(stdby)}$	Minimum Standby (Timekeeping) Voltage*		—	2.2	V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 6.0	0.9 1.35 1.8	V
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 6.0	2.1 3.15 4.2	V
V_{in}	Maximum Input Voltage, Line Input	Power Sense Mode	5.0	12	V p–p
V_{OL}	Maximum Low–Level Output Voltage	I_{out} = 0 μA I_{out} = 1.6 mA	4.5	0.1 0.4	V
V_{OH}	Minimum High–Level Output Voltage	I_{out} = 0 μA I_{out} = 1.6 mA	4.5	4.4 3.7	V
I_{in}	Maximum Input Current, Except SS	$V_{in} = V_{DD}$ or V_{SS}	6.0	± 1	μA
I_{IL}	Maximum Low–Level Input Current, SS	$V_{in} = V_{SS}$	6.0	– 1.0	μA
I_{IH}	Maximum Pull–Down Current, SS	$V_{in} = V_{DD}$	6.0	100	μA
I_{OZ}	Maximum Three–State Leakage Current	$V_{out} = V_{DD}$ or V_{SS}	6.0	± 10	μA
I_{DD}	Maximum Quiescent Supply Current	$V_{in} = V_{DD}$ or V_{SS}, All Input; I_{out} = 0 μA	6.0	50	μA
I_{DD}	Maximum RMS Operating Supply Current Crystal Operation	I_{out} = 0 μA, $V_{in} = V_{DD}$ or V_{SS}, all inputs except $XTAL_{in}$, Clock Out Disabled, No Serial Access Cycles; $f_{XTAL_{in}}$ = 32 kHz / 1 MHz / 2 MHz / 4 MHz	5.0	0.1 0.6 0.84 1.2	mA
	Maximum RMS Operating Supply Current External Frequency Source Driving $XTAL_{in}$, $XTAL_{out}$ Open	I_{out} = 0 μA, $V_{in} = V_{DD}$ or V_{SS}, Clock Out Disabled, No Serial Access Cycles; $f_{XTAL_{in}}$ = 32 kHz / 1 MHz / 2 MHz / 4 MHz	5.0	0.024 0.12 0.24 0.5	
I_{batt}	Maximum RMS Standby Current Crystal Operation	V_{BATT} = 3.0 V, V_{SYS} = 0.0 V, V_{DD} = 0.0 V, I_{out} = 0 μA, V_{in} = Don't Care, all inputs except $XTAL_{in}$, Clock Out Disabled, No Serial Access Cycles; $f_{XTAL_{in}}$ = 32 kHz / 1 MHz / 2 MHz / 4 MHz	0.0	25 250 360 600	μA

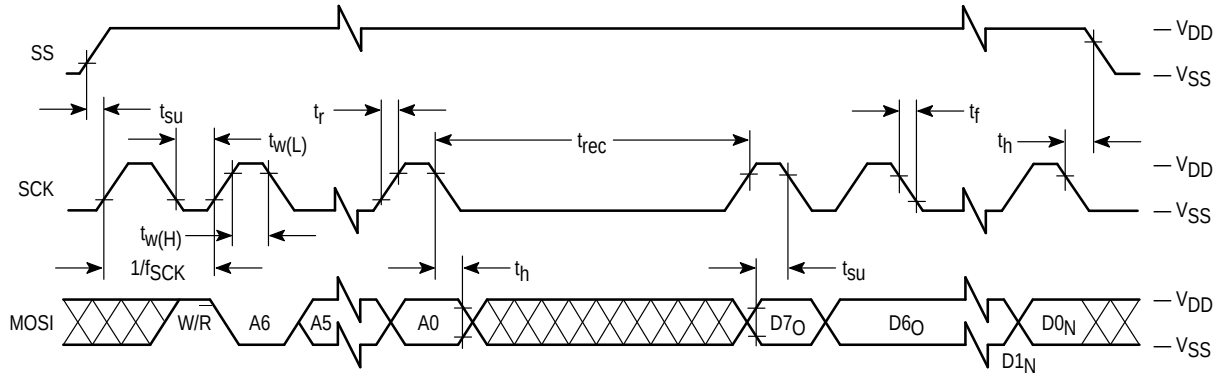
* Timekeeping function only, no read/write accesses. Data in the registers and RAM retained.

AC ELECTRICAL CHARACTERISTICS (T_A = – 40 to + 85°C, C_L = 200 pF, Input $t_r = t_f$ = 6 ns, Voltages Referenced to V_{SS})

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit	Unit
f_{SCK}	Maximum Clock Frequency (Refer to SCK t_w, below)	1, 2, 3	3.0 4.5 6.0	— 2.1 2.1	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, SCK to MISO	2, 3	3.0 4.5 6.0	200 100 100	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, SS to MISO	2, 4	3.0 4.5 6.0	200 100 100	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, SCK to MISO	2, 4	3.0 4.5 6.0	200 100 100	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Measured Between 70% V_{DD} and 20% V_{DD})	2, 3	3.0 4.5 6.0	200 100 100	ns
C_{in}	Maximum Input Capacitance		—	10	pF

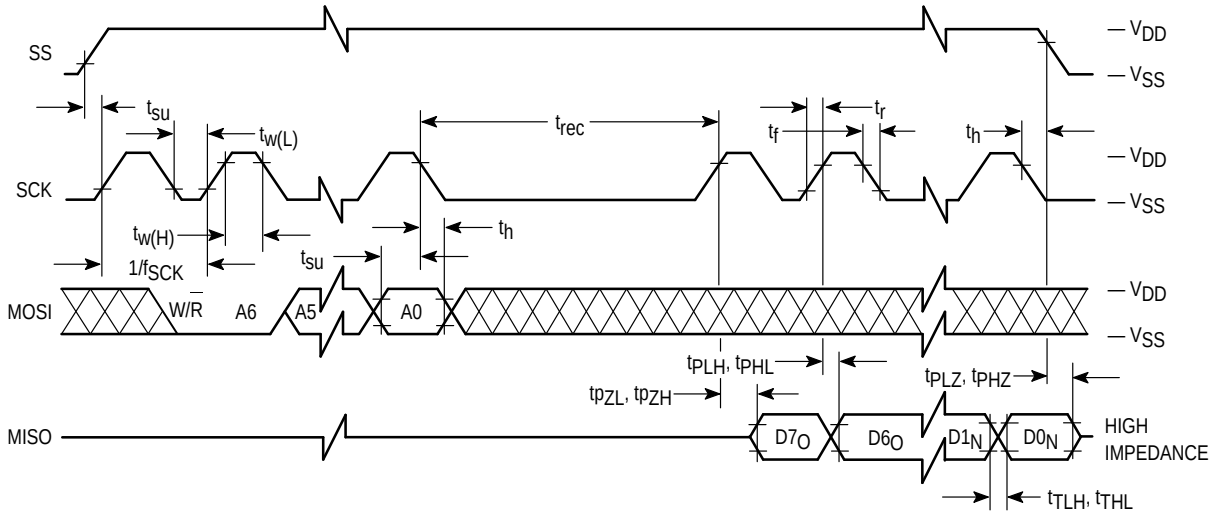
TIMING REQUIREMENTS (T_A = – 40 to + 85°C, Input $t_r = t_f$ = 6 ns, Voltages Referenced to V_{SS})

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit	Unit
t_{su}	Minimum Setup Time, SS to SCK	1, 2	3.0 4.5 6.0	200 100 100	ns
t_{su}	Minimum Setup Time, MOSI to SCK	1, 2	3.0 4.5 6.0	200 100 100	ns
t_h	Minimum Hold Time, SCK to SS	1, 2	3.0 4.5 6.0	250 125 125	ns
t_h	Minimum Hold Time, SCK to MOSI	1, 2	3.0 4.5 6.0	200 100 100	ns
t_{rec}	Minimum Recovery Time, SCK	1, 2	3.0 4.5 6.0	200 200 200	ns
$t_{w(H)}$, $t_{w(L)}$	Minimum Pulse Width, SCK	1, 2	3.0 4.5 6.0	400 200 200	ns
t_w	Minimum Pulse Width, POR		3.0 4.5 6.0	— 100 100	ns
t_r, t_f	Maximum Input Rise and Fall Times (Except $XTAL_{in}$ and POR) (Measured Between 70% V_{DD} and 20% V_{DD})	1, 2	3.0 4.5 6.0	— 2 2	μs



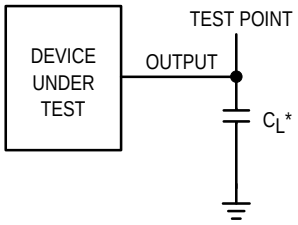
NOTE: Measurement points are V_{IL} and V_{IH} unless otherwise noted on the **AC Electrical Characteristics** table.

Figure 1. Write Cycle



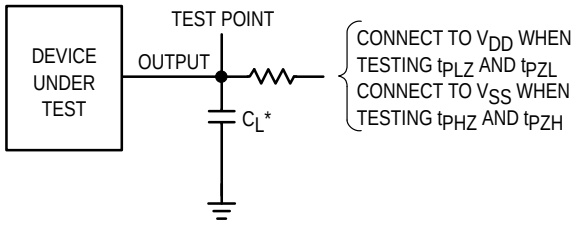
NOTE: Measurement points are V_{OL}, V_{OH}, V_{IL}, and V_{IH} unless otherwise noted on the **AC Electrical Characteristics** table.

Figure 2. Read Cycle



* Includes all probe and fixture capacitance.

Figure 3. Test Circuit



* Includes all probe and fixture capacitance.

Figure 4. Test Circuit

OPERATING CHARACTERISTICS

The real–time clock consists of a clock/calendar and a 32 x 8 RAM (see Figure 5). Communication with the device may be established via a serial peripheral interface (SPI) or MICROWIRE bus. In addition to the clock/calendar data from seconds to years, and systems flexibility provided by the 32–byte RAM, the clock features computer handshaking with an interrupt output and a separate square–wave clock output that can be one of seven different frequencies. An alarm circuit is available that compares the alarm latches with the seconds, minutes, and hours time counters and activates the interrupt output when they are equal. The clock is specifically designed to aid in power–up/power–down applications and offers several pins to aid the designer of battery–backup systems.

CLOCK/CALENDAR

The clock/calendar portion of this device consists of a long string of counters that is toggled by a 1 Hz input. The 1 Hz input is derived from the on–chip oscillator that utilizes one of four possible external crystals or that can be driven by an external frequency source. The 1 Hz trigger to the counters can also be supplied by a 50 or 60 Hz source that is connected to the LINE input pin.

The time counters offer seconds, minutes, and hours data in 12– or 24–hour format. An AM/PM indicator is available that once set, toggles at 12:00 AM and 12:00 PM. The calendar counters consist of day of week, date of month, month, and year information. Data in the counters is in BCD format. The hours counter utilizes BCD for hours data plus bits for 12/24 hour and AM/PM modes. The seven time counters are read serially at addresses $20 through $26. The time counters are written to at addresses $A0 through $A6. (See Figures 5 and 6 and Table 1.)

32 x 8 GENERAL–PURPOSE RAM

The real–time clock also has a static 32 x 8 RAM. The RAM is read at addresses $00 through $1F and written to at addresses $80 through $9F (see Figure 5).

ALARM

The alarm is set by accessing the three alarm latches and loading the desired data. (See **Serial Peripheral Interface**.) The alarm latches consist of seconds, minutes, and hours registers. When their outputs equal the values of the seconds, minutes, and hours time counters, an interrupt is generated. The interrupt output goes low if the alarm bit in the status register is set and the interrupt output is activated after an alarm time is sensed (see **Pin Descriptions, INT Pin**). To preclude a false interrupt when loading the time counters, the alarm interrupt bit in the interrupt control register should be reset. This procedure is not required when the alarm time is being loaded.

WATCHDOG FUNCTION

When Watchdog (bit 7) in the interrupt control register is set high, the clock's slave select pin must be toggled at regular intervals without a serial data transfer. If SS is not toggled at the rate shown in Table 2, the MC68HC68T1 supplies a CPU reset pulse at Pin 2 and Watchdog (bit 6) in the status register is set (see Figure 7). Typical service and reset times are shown in Table 2.

CLOCK OUT

The value in the three least significant bits of the clock control register selects one of seven possible output frequencies. (See **Clock Control Register**.) This square–wave signal is available at the CLKOUT pin. When the power–down operation is initialized, the output is reset low.

CONTROL REGISTER AND STATUS REGISTER

The operation of the real–time clock is controlled by the clock control and interrupt control registers, which are read/write registers. Another register, the status register, is available to indicate the operating conditions. The status register is a read–only register, and a read operation resets status bits.

MODE SELECT

The voltage level that is present at the V_{SYS} input pin at the end of power–on reset selects the device to be in the single–supply mode or battery–backup mode.

Single–Supply Mode

If V_{SYS} is powered up when power–on reset is completed; CLKOUT, PSE, and CPUR are enabled high and the device is completely operational. CPUR is asserted low if the voltage level at the V_{SYS} pin subsequently falls below V_{BATT} + 0.7 V. If CLKOUT, PSE, and CPUR are reset low due to a power–down instruction, V_{SYS} brought low and then powered high re–enables these outputs.

An example of the single–supply mode is where only one supply is available and V_{DD}, V_{BATT}, and V_{SYS} are tied together to the supply.

Battery–Backup Mode

If V_{SYS} is not powered up (V_{SYS} = 0 V) at the end of power–on reset, CLKOUT, PSE, CPUR, and SS are disabled (CLKOUT, PSE, and CPUR low). This condition is held until V_{SYS} rises to a threshold (approximately 0.7 V) above V_{BATT}. CLKOUT, PSE, and CPUR are then enabled and the device is operational. If V_{SYS} falls below a threshold above V_{BATT}, the outputs CLKOUT, PSE, and CPUR are reset low.

An example of battery–backup operation occurs if V_{SYS} is tied to the 5 V supply and is not receiving voltage from a supply. A rechargeable battery is connected to the V_{BATT} pin, causing a POR while V_{SYS} = 0 V. The device retains data and keeps time down to a minimum V_{BATT} voltage of 2.2 V.

The power consumption may not settle to the specified limit until main power is cycled once.

POWER CONTROL

Power control is composed of two operations, power–sense and power–down/power–up. Two pins are involved in power sensing, the LINE input pin and the INT output pin. Two additional pins, PSE and V_{SYS}, are utilized during power–down/power–up operation.

FREEZE FUNCTION

The freeze function prevents an increment of the time counters, if any of the registers are being read. Also, alarm operation is delayed if the registers are being read. This causes the clock to lose time with increasing rates of acceleration.

POWER SENSING

When power sensing is enabled (Power Sense Bit in the interrupt control register), ac/dc transitions are sensed at the LINE input pin. Threshold detectors determine when transitions cease. After a delay of 2.68 to 4.64 ms plus the external input RC circuit time constant, an interrupt true bit is set high in the status register. This bit can then be sampled to see if system power has turned back on (see Figure 8).

The power–sense circuitry operates by sensing the level of the voltage present at the LINE input pin. This voltage is centered around V_{DD}, and as long as the voltage is either plus or minus a threshold (approximately 0.7 V) from V_{DD}, a power sense failure is not indicated. With an ac signal present, remaining in this V_{DD} window longer than a maximum of 4.64 ms activates the power–sense circuit. The larger the amplitude of the signal, the less likely a power failure would be detected. A 50 or 60 Hz, 10 V p–p sine–wave voltage is an acceptable signal to present at the LINE input pin to set up the power–sense function. When ac power fails, an internal circuit pulls the voltage at the line pin within the detection window.

Power–Down

Power–down is a processor–directed operation. The power–down bit is set in the interrupt control register to initiate power–down operation. During power–down, the power supply enable (PSE) output, normally high, is driven low. The CLKOUT pin is driven low. The CPUR output, connected to the processor reset input pin, is also driven low. In addition, the serial interface (MOSI and MISO) is disabled (see Figure 9).

Power–Up

There are four methods that can initiate the power–up mode. Two of the methods require an interrupt to the microcontroller or processor by programming the interrupt control register. The interrupts can be generated by the alarm circuit by setting the alarm bit and the appropriate alarm registers. Also, an interrupt can be generated by programming the periodic interrupt bits in the interrupt control register. V_{SYS} must be at 5 volts for this operation to occur.

The third method is by initiating the power sense circuit with the power sense bit in the interrupt control register set to sense power loss along with the V_{SYS} pin to sense subsequent power–up condition (see Figure 10). (Reference Figure 19 for application circuit for third method.)

The fourth method that initiates power–up occurs when the level on the V_{SYS} pin rises 0.7 V above the level of the V_{BATT} pin, after previously falling to the level of V_{BATT} while in the battery–backup mode. An interrupt is not generated when the fourth method is utilized.

While in the single–supply mode, power–up is initiated when the V_{SYS} pin loses power and then returns high. There is no interrupt generated when using this method (see Figure 11).

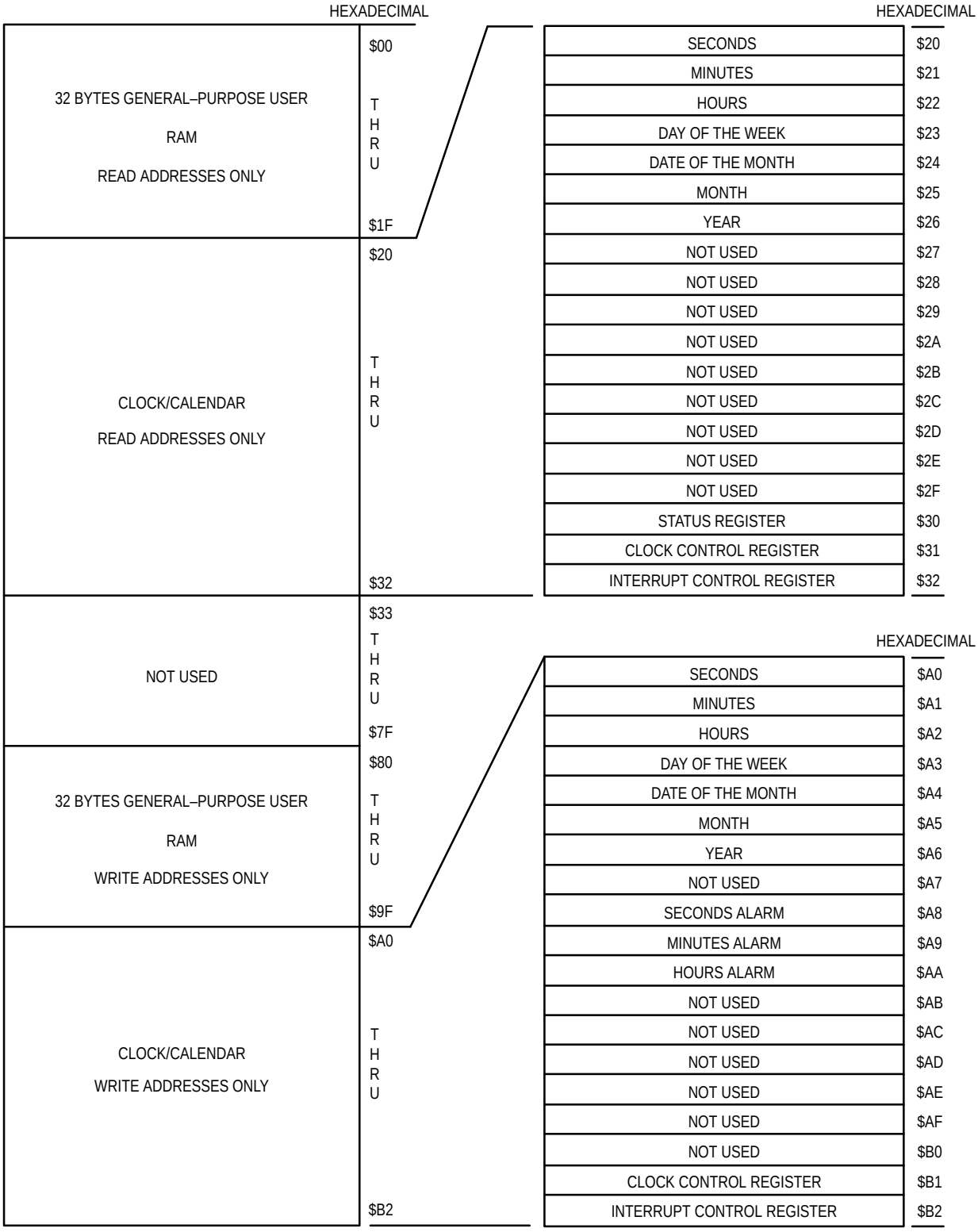
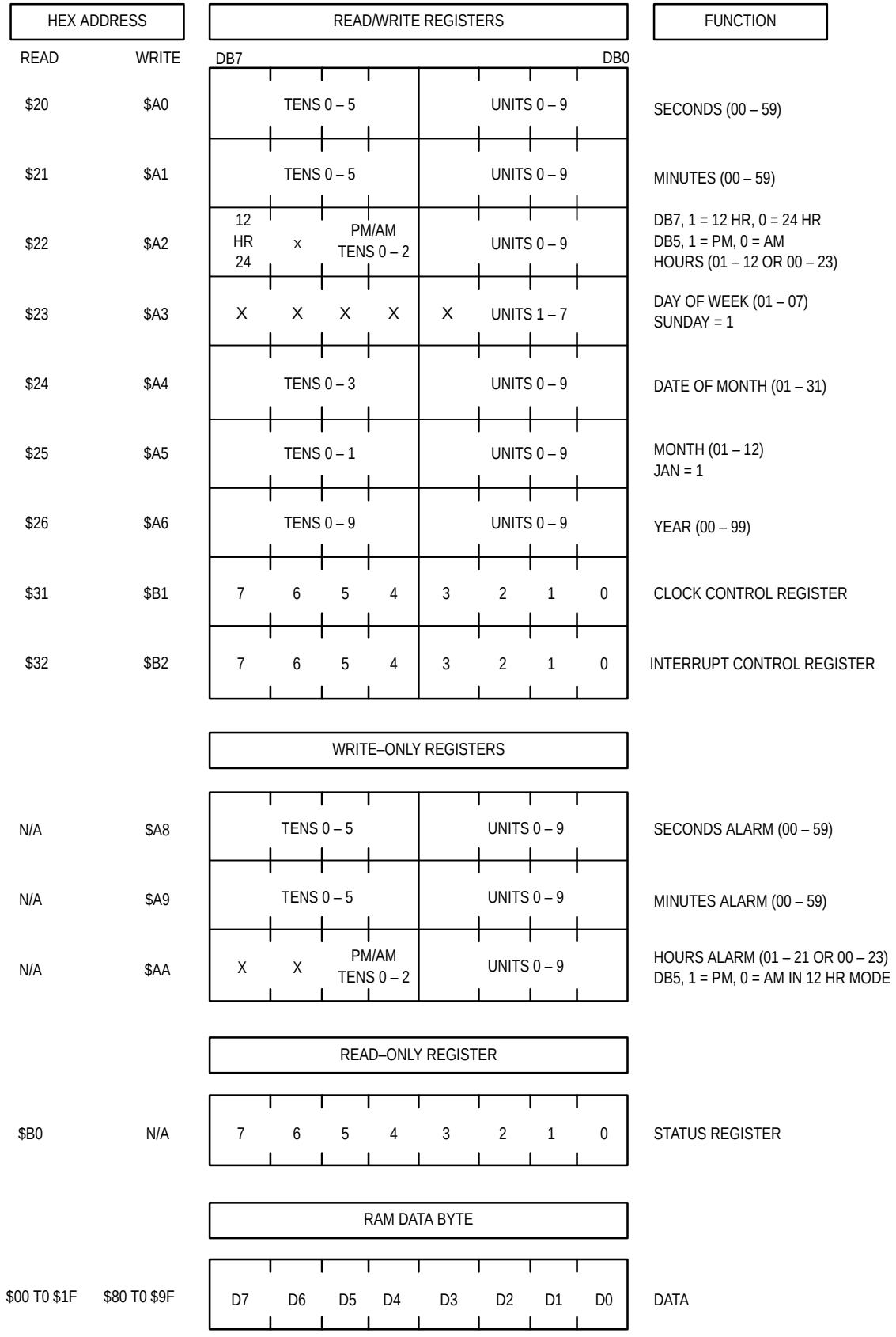


Figure 5. Address Map



NOTE:
X = Don't Care for Write
X = 0 for Read
N/A = Not Applicable

Figure 6. Clock/RAM Registers

Table 1. Clock/Calendar and Alarm Data Modes

Address Location		Function	Decimal Range	BCD Data Range	BCD Date* Example
Read	Write				
$20	$A0	Seconds	0 – 59	00 – 59	21
$21	$A1	Minutes	0 – 59	00 – 59	40
$22	$A2	Hours** (12 Hour Mode)	1 – 12	81 – 92 (AM) A1 – B2 (PM)	90
		Hours (24 Hour Mode)	0 – 23	00 – 23	10
$23	$A3	Day of Week (Sunday = 1)	1 – 7	01 – 07	03
$24	$A4	Date of Month	1 – 31	01 – 31	16
$25	$A5	Month (Jan = 1)	1 – 12	01 – 12	06
$26	$A6	Year	0 – 99	00 – 99	87
N/A	$A8	Seconds Alarm	0 – 59	00 – 59	21
N/A	$A9	Minutes Alarm	0 – 59	00 – 59	40
N/A	$AA	Hours Alarm*** (12 Hour Mode)	1 – 12	01 – 12 (AM) 21 – 32 (PM)	10
		Hours Alarm (24 Hour Mode)	0 – 23	00 – 23	10

N/A = Not Applicable

* Example: 10:40:21 AM, Tuesday, June 16, 1987.

** Most significant data bit, D7, is “0” for 24–hour mode and “1” for 12–hour mode. Data bit D5 is “1” for PM and “0” for AM in 12–hour mode.

*** Data bit D5 is “1” for PM and “0” for AM in 12–hour mode. Data bits D7 and D6 are Don’t Cares.

Table 2. Watchdog Service and Reset Times

	50 Hz		60 Hz		XTAL	
	Min	Max	Min	Max	Min	Max
Service Time	—	10 ms	—	8.3 ms	—	7.8 ms
Reset Time	20 ms	40 ms	16.7 ms	33.3 ms	15.6 ms	31.3 ms

NOTE: Reset does not occur immediately after slave select is toggled. Approximately two clock cycles later, reset initiates.

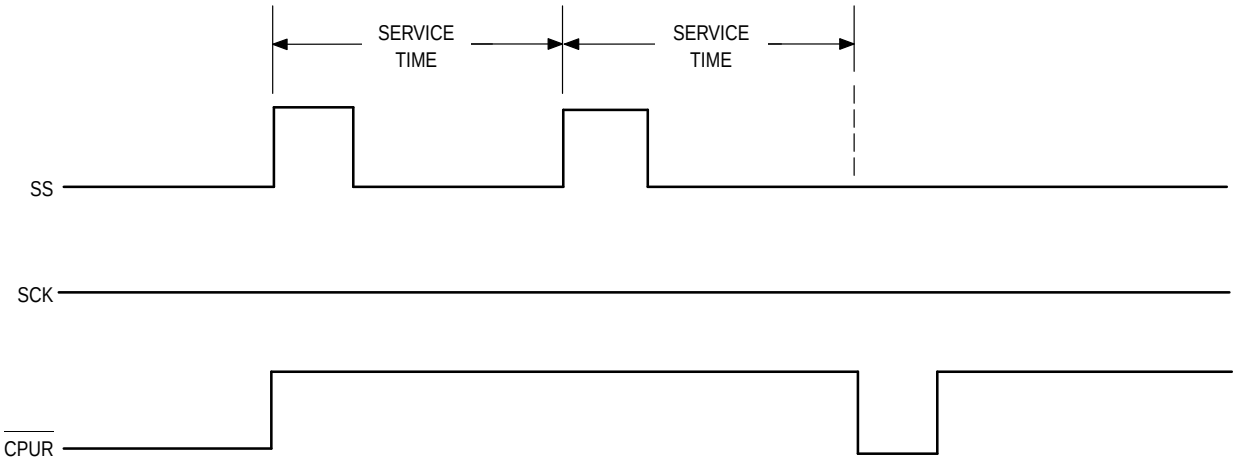
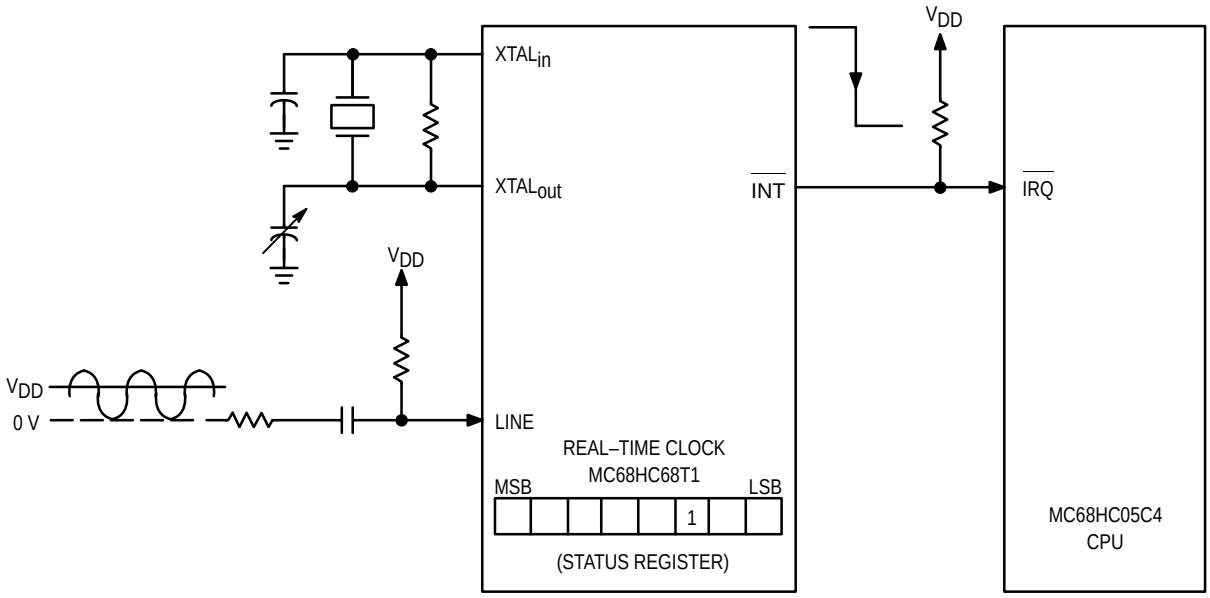


Figure 7. Watchdog Operation Waveforms



NOTE: A 60 Hz, 10 V p–p sine–wave voltage is an acceptable signal to present at the LINE input pin.

Figure 8. Power Sensing Functional Diagram

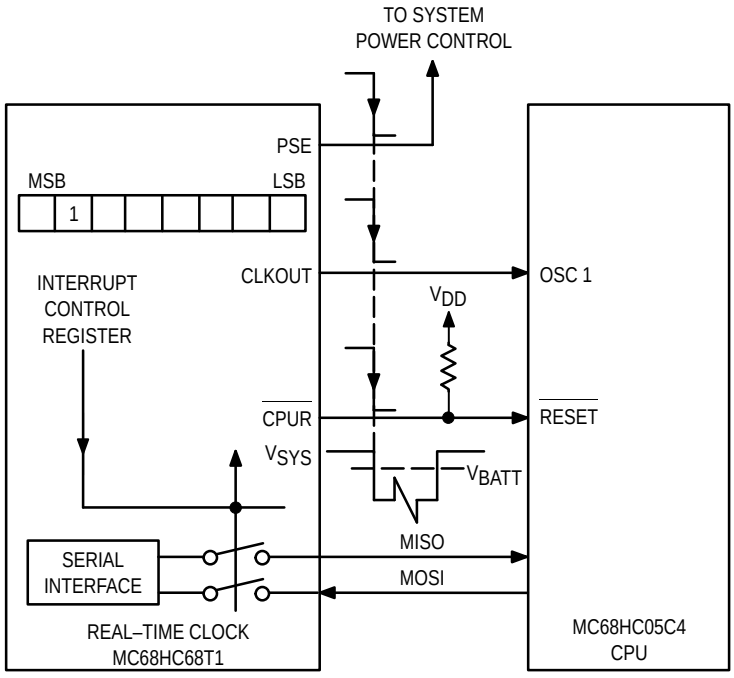
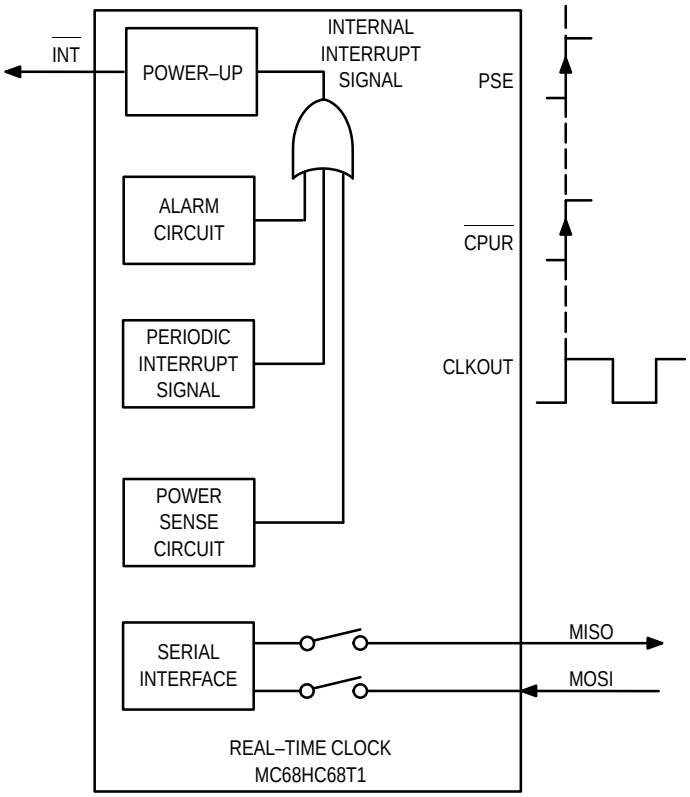


Figure 9. Software Power–Down Functional Diagram



NOTE: The V_{SYS} pin must be powered up.

Figure 10. Power–Up Functional Diagram (Initiated by Internal Interrupt Signal Generation)

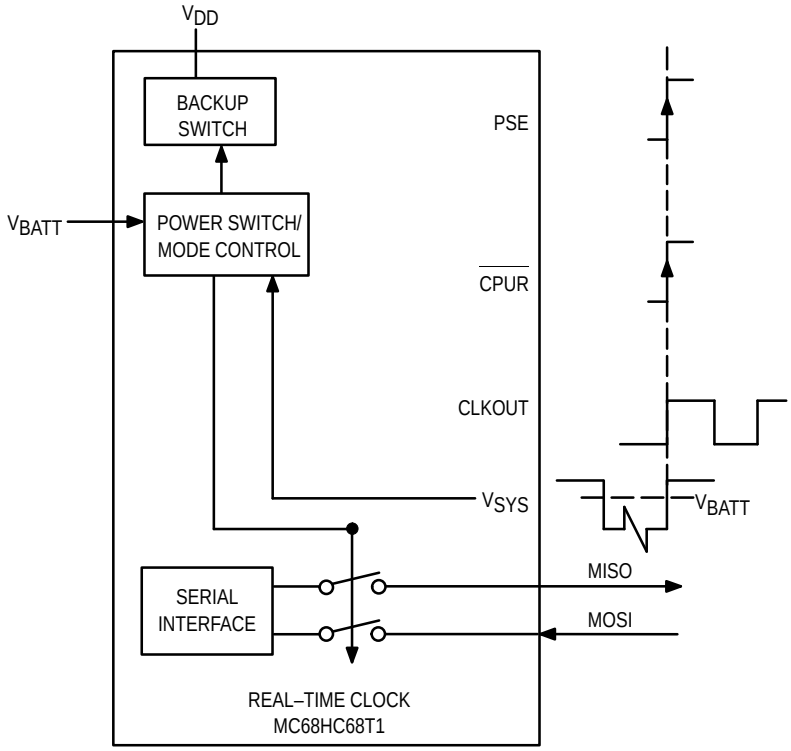


Figure 11. Power–Up Functional Diagram (Initiated by a Rise in Voltage on the V_{SYS} Pin)

PIN DESCRIPTIONS

CLKOUT
Clock Output (Pin 1)

This signal is the buffered clock output which can provide one of the seven selectable frequencies (or this output can be reset low). The contents of the three least significant bit positions in the clock control register determine the output frequency (50% duty cycle, except 2 Hz in the 50 Hz time–base mode). During power–down operation (Power–Down bit in the interrupt control register set high), the CLKOUT pin is reset low.

$\overline{\text{CPUR}}$
CPU Reset (Pin 2)

This pin provides an N channel, open–drain output and requires an external pullup resistor. This active low output can be used to drive the reset pin of a microprocessor to permit orderly power–up/power–down. The $\overline{\text{CPUR}}$ output is low from 15 to 40 ms when the watchdog function detects a CPU failure (see Table 2). The low level time is determined by the input frequency source selected as the time standard. $\overline{\text{CPUR}}$ is reset low when power–down is initiated.

$\overline{\text{INT}}$
Interrupt (Pin 3)

This active–low output is driven from a single N channel transistor and must be tied to an external pullup resistor. Interrupt is activated to a low level when any one of the following takes place:

1. Power sense operation is selected (Power Sense Bit in the interrupt control register is set high) and a power failure occurs.
2. A previously set alarm time occurs. The alarm bit in the status register and the interrupt signal are delayed 30.5 ms when 32 kHz or 1 MHz operation is selected, 15.3 ms for 2 MHz operation, and 7.6 ms for 4 MHz operation.
3. A previously selected periodic interrupt signal activates.

The status register must be read to reset the interrupt output after the selected periodic interval occurs. This is also true when conditions 1 and 2 activate the interrupt. If power–down has been previously selected, the interrupt also sets the power–up function only if power is supplied to the V_{SYS} pin to the proper threshold level above V_{BATT}.

SCK
Serial Clock (Pin 4)

This serial clock input is used to shift data into and out of the on–chip interface logic. SCK retains its previous state if the line driving it goes into a high–impedance state. In other words, if the source driving SCK goes to the high–impedance state, the previous low or high level is retained by on–chip control circuitry.

MOSI
Master Out Slave In (Pin 5)

The serial data present at this port is latched into the interface logic by SCK if the logic is enabled. Data is shifted in, either on the rising or falling edges of SCK, with the most significant bit (MSB) first.

In Motorola's microcomputers with SPI, the state of the CPOL bit determines which is the active edge of SCK. If SCK is high when SS goes high, the state of the CPOL bit is high. Likewise, if a rising edge of SS occurs while SCK is low (see Figure 13), then the CPOL bit in the microcomputer is low.

MOSI retains its previous state if the line driving it goes into high–impedance state. In other words, if the source driving MOSI goes to the high–impedance state, the previous low or high level is retained by on–chip control circuitry.

MISO
Master In Slave Out (Pin 6)

The serial data present at this port is shifted out of the interface logic by SCK if the logic is enabled. Data is shifted out, either on the rising or falling edge of SCK, with the most significant bit (MSB) first. The state of the CPOL bit in the microcomputer determines which is the active edge of SCK (see Figure 13).

SS
Slave Select (Pin 7)

When high, the slave select input activates the interface logic; otherwise the logic is in a reset state and the MISO pin is in the high–impedance state. The watchdog circuit is toggled at this pin. SS has an internal pulldown device. Therefore, if SS is in a low state before going to high impedance, SS can be left in a high–impedance state. That is, if the source driving SS goes to the high–impedance state, the previous low level is retained by on–chip control circuitry.

V_{SS}
Ground (Pin 8)

This pin is connected to ground.

PSE
Power Supply Enable (Pin 9)

The power supply enable output is used to control system power and is enabled high under any one of the following conditions:

1. V_{SYS} rises above the V_{BATT} voltage after V_{SYS} is reset low by a system failure.
2. An interrupt occurs (if the V_{SYS} pin is powered up 0.7 V above V_{BATT}).
3. A power–on reset occurs (if the V_{SYS} pin is powered up 0.7 V above V_{BATT}).

PSE is reset low by writing a high into the power–down bit of the interrupt control register.

$\overline{\text{POR}}$
Power–On Reset (Pin 10)

This active–low Schmitt–trigger input generates an internal power–on reset signal using an external RC network (see Figures 18 through 21). Both control registers and frequency dividers for the oscillator and line inputs are reset. The status register is reset except for the first time–up bit (bit 4), which is set high. At the end of the power–on reset, single–supply or battery–backup mode is selected at this time, determined by the state of V_{SYS}.

This pin may be more aptly named first–time–up reset.

LINE
Line Sense (Pin 11)

The LINE sense input can be used to drive one of two functions. The first function utilizes the input signal as the frequency source for the timekeeping counters. This function is selected by setting the line/XTAL bit high in the clock control register. The second function enables the LINE input to detect a power failure. Threshold detectors operating above and below V_{DD} sense an ac voltage loss. The Power Sense bit in the interrupt control register must be set high, and crystal or external clock source operation is required. The line/XTAL bit in the clock control register must be low to select crystal operation. When Power Sense is enabled, this pin, left unconnected, floats to V_{DD}.

This output has no ESD protection diode tied to V_{DD} which allows this pin's voltage to rise above V_{DD}. Care must be taken in the handling of this device.

V_{SYS}
System Voltage (Pin 12)

This input is connected to system voltage. The level on this pin initiates power–up if it rises 0.7 V above the level at the V_{BATT} input pin after previously falling below 0.7 V below V_{BATT}. When power–up is initiated, the PSE pin returns high and the CLKOUT pin is enabled. The CPUR output pin is also set high. Conversely, if the level of the V_{SYS} pin falls below V_{BATT} + 0.7 V, the PSE, CLKOUT, and CPUR pins are placed low. The voltage level present at this pin at the end of POR determines the device's operating mode.

V_{BATT}
Battery Voltage (Pin 13)

This pin is the *only* oscillator power source and should be connected to the positive terminal of the battery. The V_{BATT} pin **always** supplies power to the MC68HC68T1, even when the device is not in the battery–backup mode. To maintain timekeeping, the V_{BATT} pin must be at least 2.2 V. When the level on the V_{SYS} pin falls below V_{BATT} + 0.7 V, **V_{BATT} is internally connected to the V_{DD} pin.**

When the LINE input is used as the frequency source, the unused V_{BATT} and XTAL pins may be tied to V_{SS}. Alternatively, if V_{BATT} is connected to V_{DD}, $XTAL_{in}$ can be tied to either V_{SS} or V_{DD}.

This output has no ESD protection diode tied to V_{DD} which allows this pin's voltage to rise above V_{DD}. Care must be taken in the handling of this device.

$XTAL_{in}$, $XTAL_{out}$
Crystal Input/Output (Pins 14, 15)

For crystal operation, these two pins are connected to a 32.768 kHz, 1.048576 MHz, 2.097152 MHz, or 4.194304 MHz crystal. If crystal operation is not desired and Line Sense is used as frequency source, connect $XTAL_{in}$ to V_{DD} or V_{SS} (caution: see V_{BATT} pin description) and leave XTA_{out} open. If an external clock is used, connect the external clock to $XTAL_{in}$ and leave $XTAL_{out}$ open. The external clock must swing from at least 30 to 70% of ($V_{DD} - V_{SS}$). Preferably, this input should swing from V_{SS} to V_{DD}.

V_{DD}
Positive Power Supply (Pin 16)

For full functionality, the positive power supply pin may range from 3.0 to 6.0 V with respect to V_{SS}. To maintain timekeeping, the minimum standby voltage is 2.2 V with respect to V_{SS}. For proper operation in battery–backup mode, a diode **must** be placed in series with V_{DD}.

CAUTION

Data transfer to/from the MC68HC68T1 must not be attempted if the supply voltage falls below 3.0 V.

REGISTERS

CLOCK CONTROL REGISTER (READ/WRITE) — READ ADDRESS $31/WRITE ADDRESS $B1

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
START	LINE	XTAL SELECT	XTAL SELECT	50 Hz	CLK OUT	CLK OUT	CLK OUT
$\overline{\text{STOP}}$	$\overline{\text{XTAL}}$	1	0	$\overline{\text{60 Hz}}$	2	1	0

All bits are reset low by a power–on reset.

Start–$\overline{\text{Stop}}$

A high written into this bit enables the counter stages of clock circuitry. A low holds all bits reset in the divider chain from 32 Hz to 1 Hz. The clock out signal selected by bits D0, D1, and D2 is not affected by the stop function except the 1 and 2 Hz outputs.

Line/ $\overline{\text{XTAL}}$

When this bit is high, clock operation uses the 50 or 60 cycle input present at the LINE input pin. When the bit is low, the $XTAL_{in}$ pin is the source of the time update.

XTAL Select

Accommodation of one of four possible crystals are selected by the value in bits D4 and D5.

0 = 4.194304 MHz 2 = 1.048576 MHz

1 = 2.097152 MHz 3 = 32.768 kHz

The MC68HC68T1 has an on–chip 150 kΩ resistor that is switched in series with the internal inverter when 32 kHz is selected via the clock control register. At power–up, the device sets up for a 4 MHz oscillator and the series resistor is not part of the oscillator circuit. Until this resistor is switched in, oscillations may be unstable with the 32 kHz crystal. (See Figure 12.)

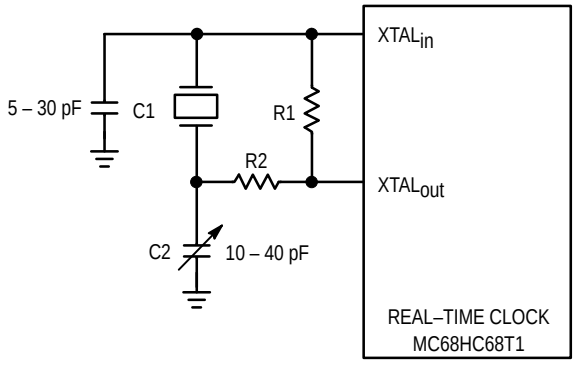


Figure 12. Recommended Oscillator Circuit (C1, C2 Values Depend Upon the Crystal Frequency)

Resistor R1 is recommended to be 10 MΩ for 32 kHz operation. Consult crystal manufacturer for R1 value for other frequencies. Resistor R2 must be used in 32 kHz operation only. Use a 200 to 300 kΩ range. This stabilizes the oscillator until the control register is set properly and reduces standby current.

50 Hz – 60 Hz

50 Hz may be used as the input frequency at the LINE input when this bit is set high; a low accommodates 60 Hz. The power sense bit in the interrupt control register must be reset low for line frequency operation.

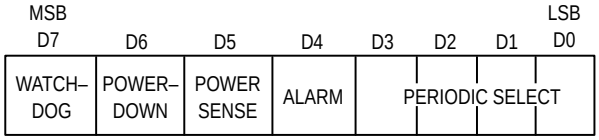
Clock Out

Three bits specify one of the seven frequencies to be used as the square–wave clock output (CLKOUT).

0 = XTAL	4 = Disable (low output)
1 = XTAL/2	5 = 1 Hz
2 = XTAL/4	6 = 2 Hz
3 = XTAL/8	7 = 50/60 Hz for LINE operation
	7 = 64 Hz for XTAL operation

All bits in the clock control register are reset by a power–on reset. Therefore, XTAL is selected as the clock output at this time.

INTERRUPT CONTROL REGISTER (READ/WRITE) — READ ADDRESS $32/WRITE ADDRESS $B2



All bits are reset low by power–on reset.

Watchdog

When this bit is set high, the watchdog operation is enabled. This function requires the CPU to toggle the SS pin periodically without a serial transfer requirement. In the event this does not occur, a CPU reset is issued at the CPUR pin. The status register must be read before re–enabling the watchdog function.

Power–Down

A high in this location initiates a power–down. A CPU reset occurs via the CPUR output, the CLKOUT and PSE output pins are reset low, and the serial interface is disabled.

Power Sense

When set high, this bit is used to enable the LINE input pin to sense a power failure. When power sense is selected, the input to the 50/60 Hz prescaler is disconnected; therefore, crystal operation is required. An interrupt is generated when a power failure is sensed and the power sense and interrupt true bit in the status register are set. When power sense is activated, a logic low must be written to this location followed by a high to re–enable power sense.

Alarm

The output of the alarm comparator is enabled when this bit is set high. When an equal comparison occurs between the seconds, minutes, and hours time counters and alarm latches, the interrupt output is activated. When loading the time counters, this bit should be reset low to avoid a false interrupt. This is not required when loading the alarm latches. See INT pin description for explanation of alarm delay.

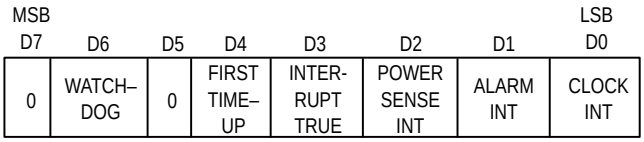
Periodic Select

The value in these four bits (D0, D1, D2, and D3) selects the frequency of the periodic output (see Table 3).

Table 3. Periodic Interrupt Output Frequencies (at INT Pin)

D3 – D0 Value (Hex)	Periodic Interrupt Output Frequency	Frequency Timebase	
		XTAL	Line
0	Disable		
1	2048 Hz	X	
2	1024 Hz	X	
3	512 Hz	X	
4	256 Hz	X	
5	128 Hz	X	
6	64 Hz	X	
	50 or 60 Hz		X
7	32 Hz	X	
8	16 Hz	X	
9	8 Hz	X	
A	4 Hz	X	
B	2 Hz	X	X
C	1 Hz	X	X
D	1 Cycle per Minute	X	X
E	1 Cycle per Hour	X	X
F	1 Cycle per Day	X	X

STATUS REGISTER (READ ONLY) — ADDRESS $30



NOTE

All bits are reset low by a power–on reset except the first time–up bit which is set high. All bits except the power sense bit are reset after a read of the status register.

Watchdog

If this bit is set high, the watchdog circuit has detected a CPU failure.

First Time–Up

Power–on reset sets this bit high. This signifies the data in the RAM and Clock is not valid and should be initialized.

After the status register is read, the first time–up bit is set low if the POR pin is high. Conversely, if the POR pin is held low, the first time–up bit remains set high.

Interrupt True

A high in this bit signifies that one of the three interrupts (power sense, alarm, or clock) is valid.

Power–Sense Interrupt

This bit set high signifies that the power–sense circuit has generated an interrupt. This bit is not reset after a read of this register.

Alarm Interrupt

When the contents of the seconds, minutes, and hours time counters and alarm latches are equal, this bit is set high. The status register must be read before loading the interrupt control register for valid alarm indication after the alarm activates.

Clock Interrupt

A periodic interrupt sets this bit high (see Table 3).

SERIAL PERIPHERAL INTERFACE (SPI)

The serial peripheral interface (SPI) utilized by the MC68HC68T1 is a serial synchronous bus for address and data transfers. The shift clock (SCK), which is generated by the microcomputer, is active only during address and data transfer. In systems using the MC68HC05C4 or MC68HC11A8, the inactive clock polarity is determined by the clock polarity (CPOL) bit in the microcomputer's control register.

A unique feature of the MC68HC68T1 is that the level of the inactive clock is determined by sampling SCK when SS becomes active. Therefore, either SCK polarity is accommodated. Input data (MOSI) is latched internally on the internal strobe edge and output data (MISO) is shifted out on the shift edge (see Table 4 and Figure 13). There is one clock for each bit transferred. Address as well as data bits are transferred in groups of eight.

Table 4. Function Table

Mode	Signal			
	SS	SCK	MOSI	MISO
Disabled Reset	L	Input Disabled	Input Disabled	High–Z
Write	H	CPOL = 1  CPOL = 0	Data Bit Latch	High–Z
Read	H	CPOL = 1  CPOL = 0	X	Next Data Bit Shifted Out*

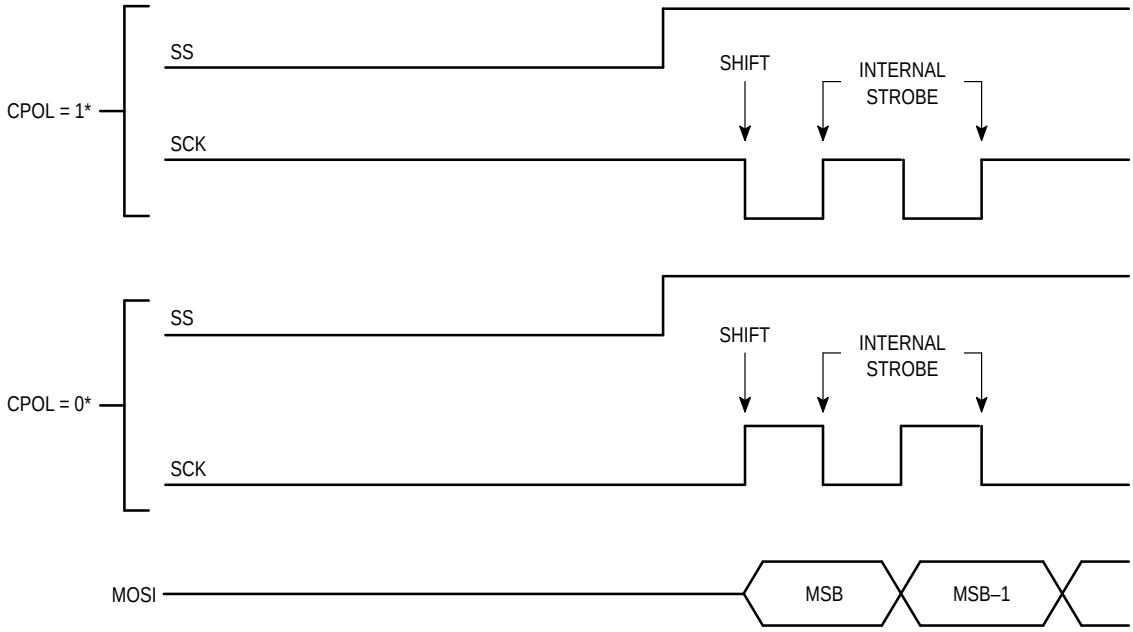
* MISO remains at a High–Z until eight bits of data are ready to be shifted out during a read. MISO remains at a High–Z during the entire write cycle.

ADDRESS AND DATA FORMAT

There are three types of serial transfers:

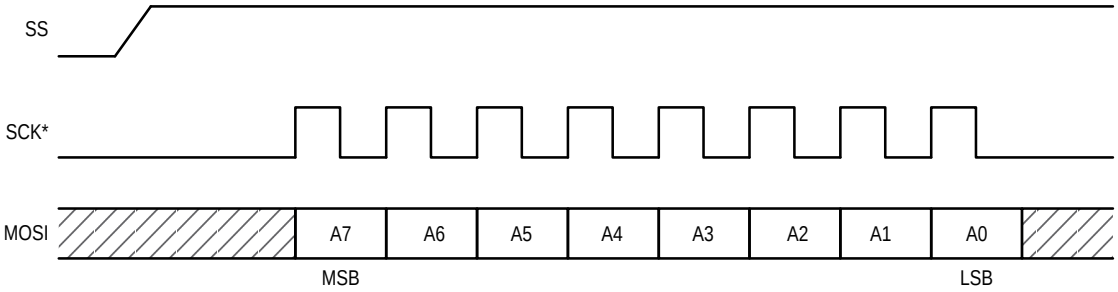
1. Read or write address
2. Read or write data
3. Watchdog reset (actually a non–transfer)

The address and data bytes are shifted MSB first, into the serial data input (MOSI) and out of the serial data output (MISO). Any transfer of data requires the address of the byte to specify a write or read Clock or RAM location, followed by one or more bytes of data. Data is transferred out of MISO for a read operation and into MOSI for a write operation (see Figures 14 and 15).



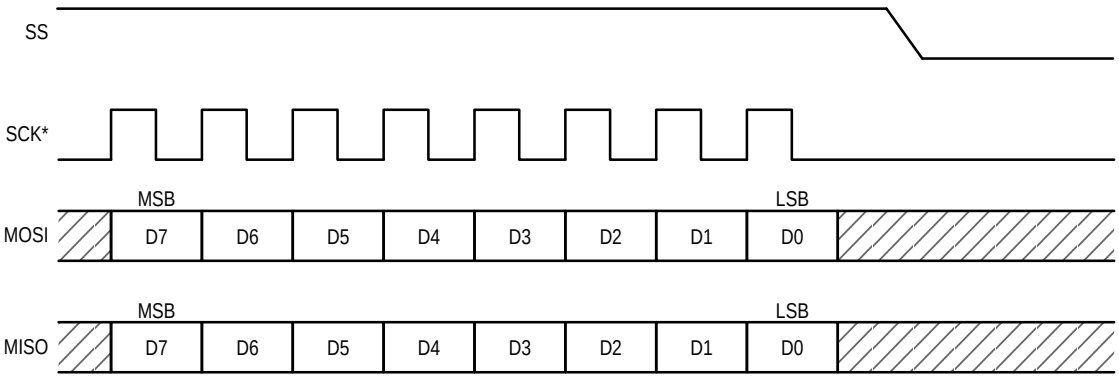
* CPOL is a bit that is set in the microcomputer's Control Register.

Figure 13. Serial Clock (SCK) as a Function of MCU Clock Polarity (CPOL)



* SCK can be either polarity.

Figure 14. Address Byte Transfer Waveforms

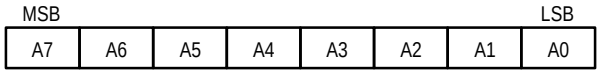


* SCK can be either polarity.

Figure 15. Read/Write Data Transfer Waveforms

Address Byte

The address byte is always the first byte entered after SS goes true. To transmit a new address, SS must first be brought low and then taken high again.



A7 — High initiates one or more write cycles.
Low initiates one or more read cycles.

A6 — Must be low (zero) for normal operation.

A5 — High signifies a clock/calendar location.
Low signifies a RAM location.

A0 – A4 — Remaining address bits (see Figure 5).

Address and Data

Data transfers can occur one byte at a time or in multi–byte burst mode (see Figures 16 and 17). After the MC68HC68T1 is enabled (SS = high), an address byte selects either a read or a write of the Clock/Calendar or RAM. For a single–byte read or write, one byte is transferred to or from the Clock/Calendar register or RAM location specified by an address. Additional reading or writing requires re–enabling the device and providing a new address byte. If the MC68HC68T1 is not disabled, additional bytes can be read or written in a burst mode. Each read or write cycle causes the Clock/Calendar register or RAM address to automatically increment. Incrementing continues after each byte transfer until the device is disabled. After incrementing to $1F or $9F, the address wraps to $00 and continues if the RAM is selected. When the Clock/Calendar is selected, the address wraps to $20 after incrementing to $32 to $B2.

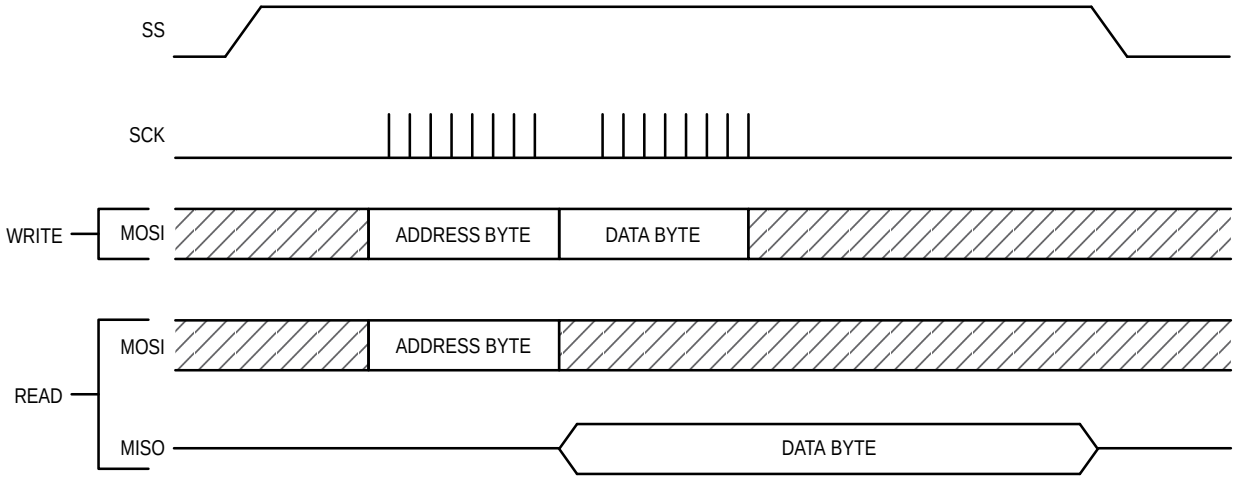


Figure 16. Single–Byte Transfer Waveforms

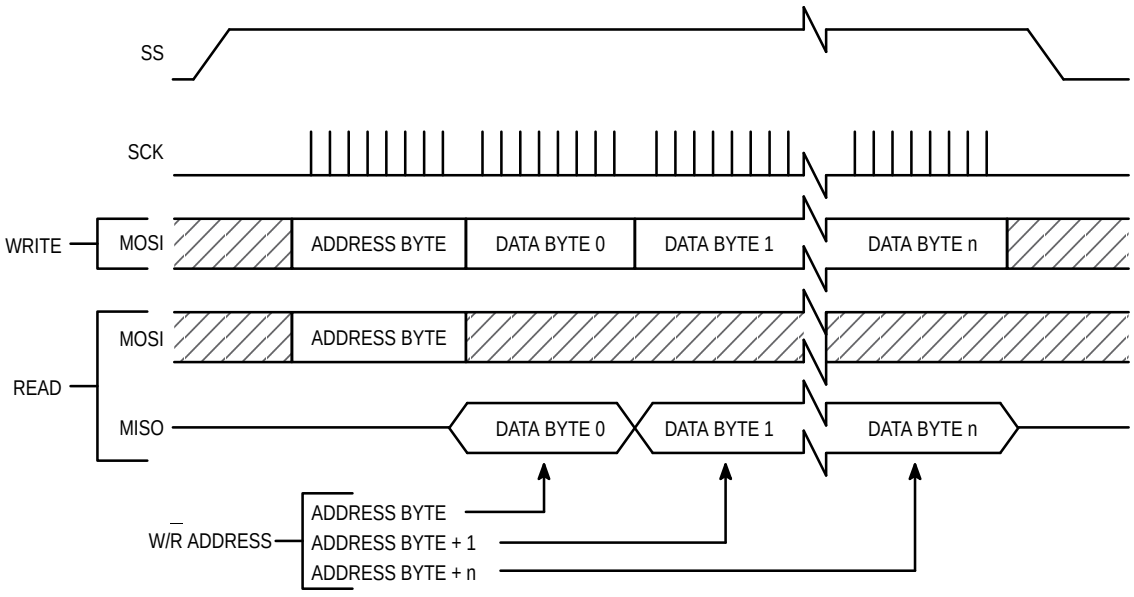
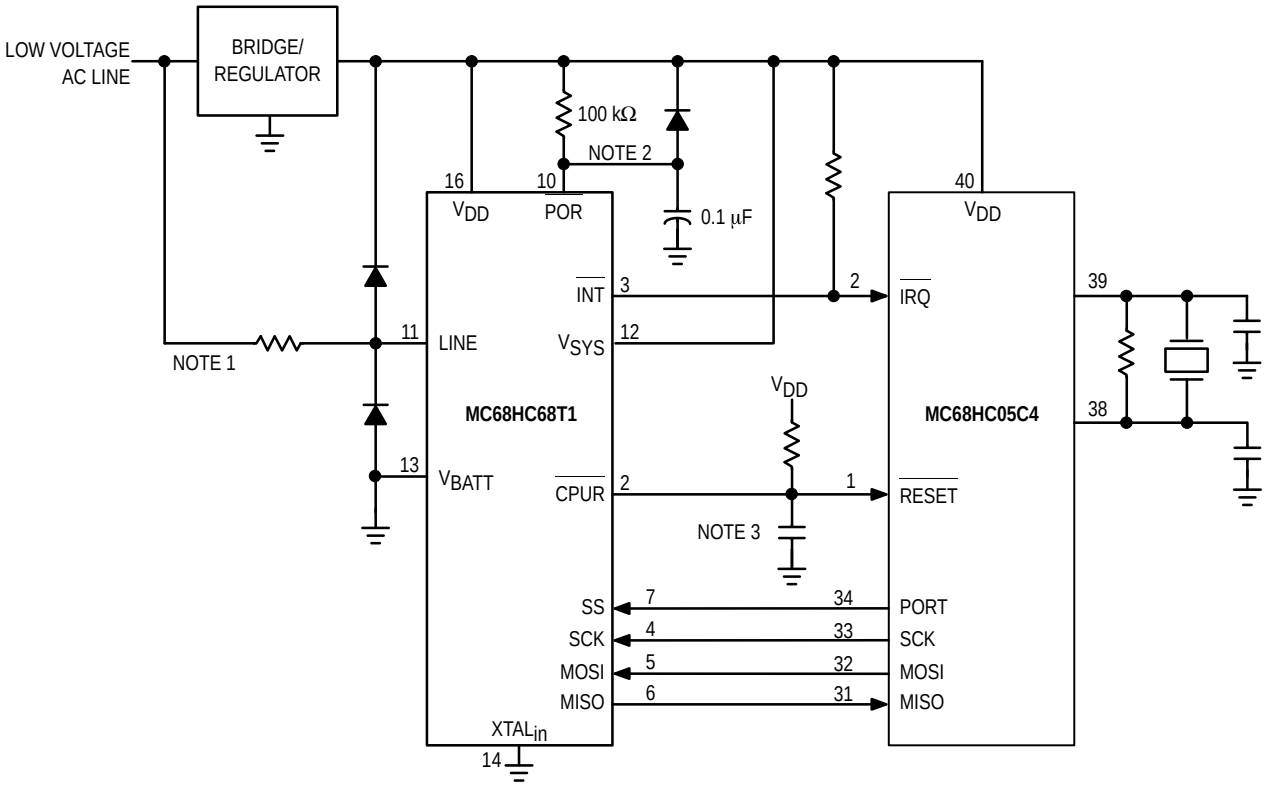


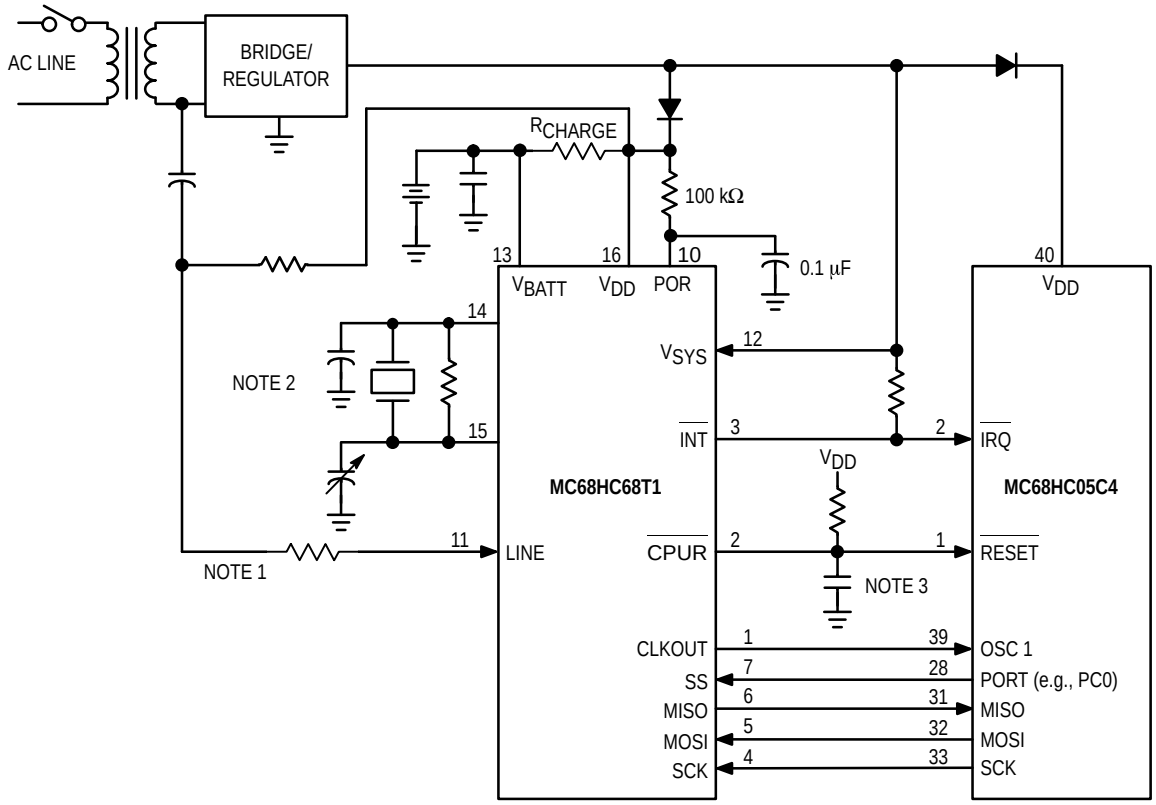
Figure 17. Multiple–Byte Transfer Waveforms

APPLICATION CIRCUITS



NOTES:
1. Clock circuit driven by line input frequency.
2. Power–on reset circuit included to detect power failure.
3. If an MC68HC11 MCU is used, delete the capacitor at the $\overline{\text{RESET}}$ pin.

Figure 18. Power–Always–On System



NOTES:

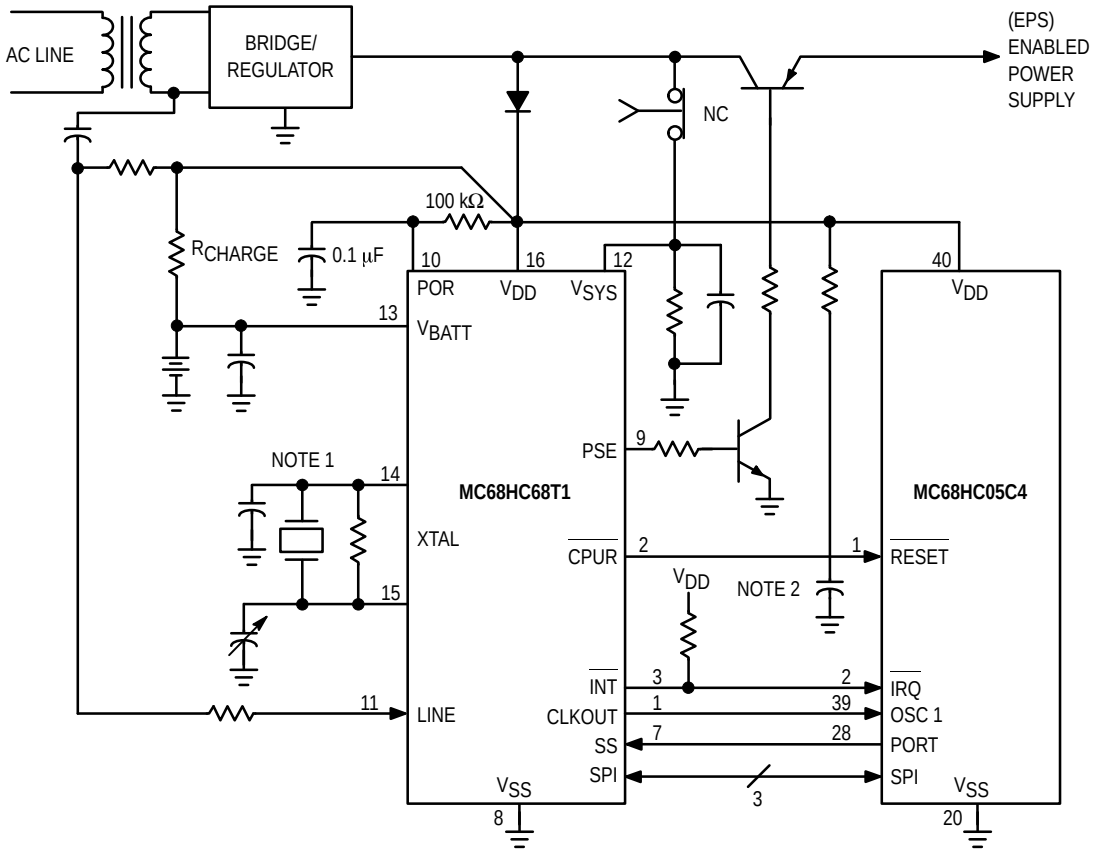
1. The LINE input pin can sense when the switch opens by use of the power sense interrupt. The MC68HC68T1 crystal drives the clock input to the CPU using the CLKOUT pin. On power–down when $V_{SYS} < V_{BATT} + 0.7$ V, V_{BATT} powers the clock. A threshold detect activates an on–chip P channel switch, connecting V_{BATT} to V_{DD}. V_{BATT} always supplies power to the oscillator, keeping voltage frequency variation to a minimum.
2. For 32.768 kHz oscillator, see Figure 12. This configuration, when the MC68HC68T1 supplies the MCU clock, usually requires a 1 to 4 MHz clock.
3. If an MC68HC11 MCU is used, delete the capacitor at the $\overline{\text{RESET}}$ pin.

Figure 19. Externally–Controlled Power System

POWER–SENSING POWER–DOWN PROCEDURE

A procedure for power–down operation consists of the following:

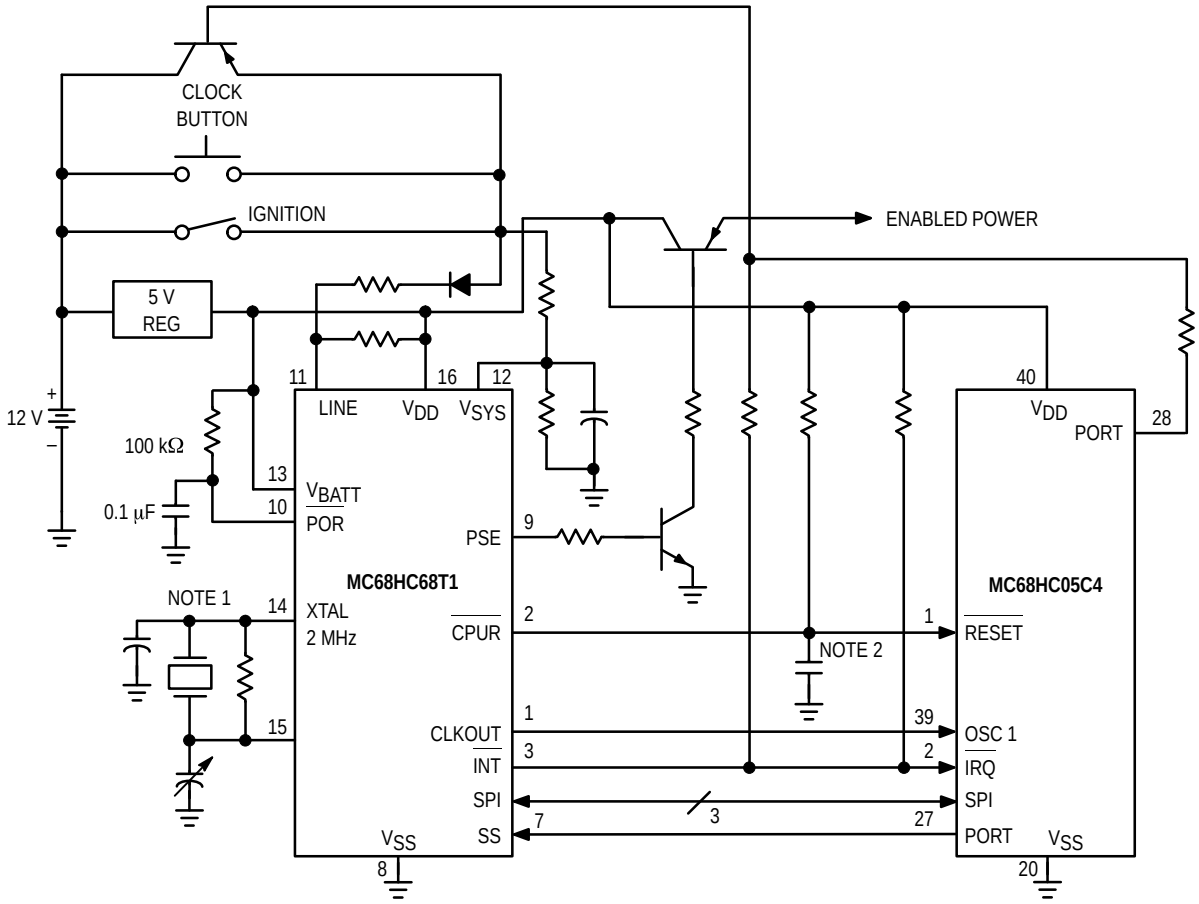
1. Set power sense operation by writing bit 5 high in the interrupt control register.
2. When an interrupt occurs, the CPU reads the status register to determine the interrupt source.
3. Sensing a power failure, the CPU does the necessary housekeeping to prepare for shutdown.
4. The CPU reads the status register again after several milliseconds to determine validity of power failure.
5. The CPU sets power–down (bit 6) and disables all interrupts in the interrupt control register when power–down is verified. This causes the CPU reset and Clock Out pins to be held low and disconnects the serial interface.
6. When power returns and V_{SYS} rises above V_{BATT} + 0.7 V, power–up is initiated. The CPU reset is released and serial communication is established.



NOTES:

1. See Figure 12 for 32.768 kHz operation. This configuration, where the MC68HC68T1 supplies the MCU clock, usually requires a 1 to 4 MHz crystal.
2. If an MC68HC11 MCU is used, delete the capacitor at the $\overline{\text{RESET}}$ pin.

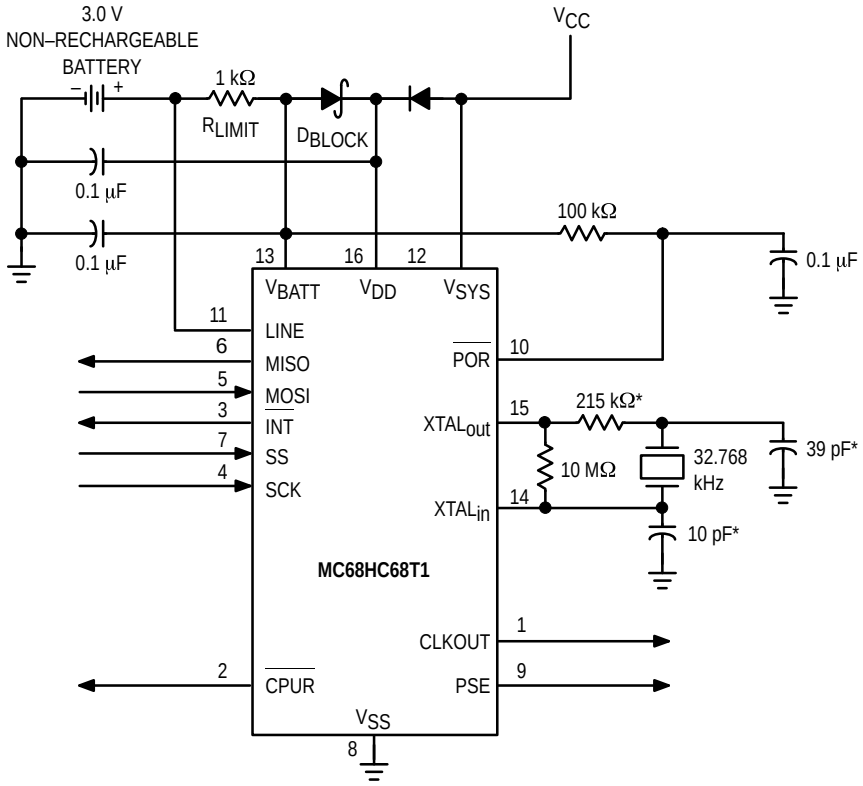
Figure 20. Rechargeable Battery–Backup System



NOTES:

1. The V_{SYS} and Line inputs can be used to sense the ignition turning on and off. An external switch is included to activate the system without turning on the ignition. Also, the CMOS CPU is not powered down with the system V_{DD}, but is held in a low power reset mode during power–down. When restoring power, the MC68HC68T1 enables the CLKOUT pin and sets the PSE and CPUR pins high.
2. If an MC68HC11 MCU is used, delete the capacitor at the $\overline{\text{RESET}}$ pin.
3. Voltage at pin must not exceed absolute maximum V_{in} specification.

Figure 21. Automotive System



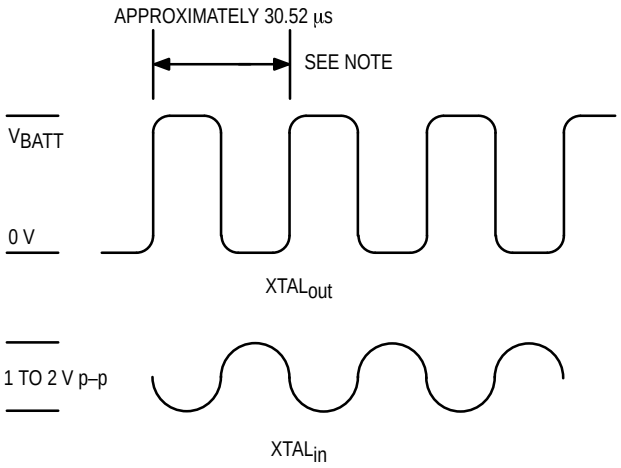
* Actual values may vary, depending on recommendations of crystal manufacturer.

Figure 22. Non–Rechargeable Battery–Backup System

TROUBLESHOOTING

1. *The circuit works, but the standby current is well above the spec. How can the standby current be reduced?*

   a. If using a 32.768 kHz crystal, include a series resistor in the circuit per Figure 12 of the data sheet. A good value to start with is 200 kΩ. The signals at $XTAL_{out}$ and $XTAL_{in}$ pins should look similar to Figure 23 when the correct value is selected. The sharp, clean edges on the $XTAL_{out}$ pin reduces current on the totem pole drivers internal to the device.



NOTE: Refer to item 8.

Figure 23. XTAL Waveforms

   b. Connect the LINE pin to something other than V_{DD} (e.g., V_{BATT}, V_{SS}, V_{SYS})

   c. Ensure that the Power–On–Reset (POR) has a time constant of at least 100 ms.

   d. Ensure that there is a diode from V_{DD} to + 5 V of the system, in battery–backup applications. See **Application Circuits**.

2. *When power is applied, the clock does not start up nor does it hold data in the control registers.*

   Make sure the POR circuit is connected and working.

3. *The clock loses time, but the oscillator is tuned.*

   Do not make constant accesses to the clock. When a read or write cycle is started, the clock stops incrementing time.

4. *When the part is power cycled, the clock loses all time and data.*

   Check the battery installation and ensure that a diode is in the circuit from V_{DD} to + 5 V.

5. *Can a non–rechargeable lithium battery be used?*

   Yes, but the battery must have a large capacity. Careful attention MUST be given if the end unit needs to be UL approved. The circuit of Figure 22 is a good start.

6. *Able to read/write data to the RAM but not to the clock registers, or vice versa.*

   There is a software problem. There is no internal difference from reading/writing to the RAM or clock locations.

7. *How is the oscillator tuned?*

   The best way to tune the oscillator is to set the clock out bits of the Clock Control Register (bits 0, 1, and 2) to output the primary XTAL frequency (000). The frequency can then be more accurately measured from the CLKOUT pin. This prevents the measuring device from loading the oscillator circuit, which may shift the frequency.

8. *What is the accuracy of the oscillator?*

   The oscillator accuracy is dependent on the quality of the crystal used. For every 1 ppm variance in crystal frequency, the clock gains or loses 2.6 seconds per month. 25 ppm is a typical spec for a crystal, which translates to ± 65 seconds per month.

9. *Can the Line pin sense a dc failure?*

   Yes, the Line input is threshold triggered in a window from one diode drop above and below V_{DD}. If supply is removed in the low cycle of a sine wave, the internal network pulls the line pin to within the threshold in a few milliseconds. In the absence of a dc voltage outside the V_{DD} ± 0.7 V window, the internal network pulls the signal to within the window and triggers the interrupt.

10. *Can the V_{SYS} line be more than 0.5 V above V_{DD}?*

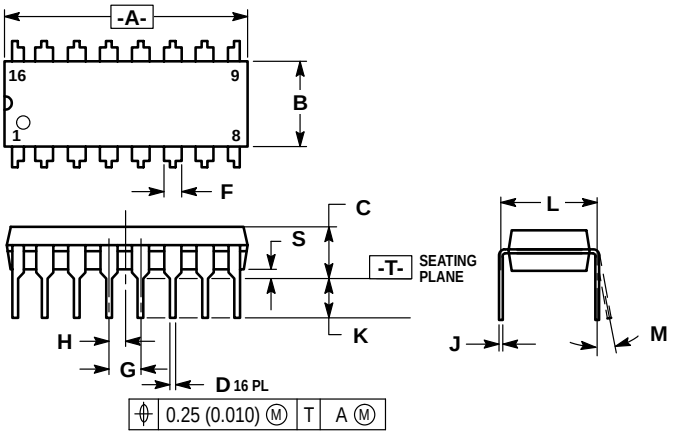
    No. There is an ESD protection network that causes a supply problem with this application.

11. *The CLKOUT, $\overline{CPUR}$, and PSE pins do not go inactive when V_{DD} and V_{SYS} are removed. The CLKOUT, $\overline{CPUR}$, and PSE are not active immediately when V_{DD} and V_{SYS} is applied.*

    The problem is related to the power up procedure (battery–backup mode or single–supply mode). See these sections in the data sheet for more information.

PACKAGE DIMENSIONS

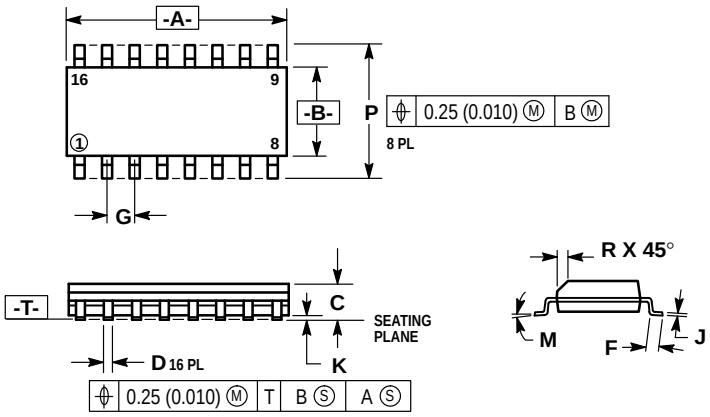
P SUFFIX
PLASTIC DIP (DUAL IN–LINE PACKAGE)
CASE 648–08



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

DW SUFFIX
SOG (SMALL OUTLINE GULL–WING) PACKAGE
CASE 751G–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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