PCF8534A

Universal LCD driver for low multiplex rates

Rev. 03 — 10 November 2008 Product data sheet

1. General description

The PCF8534A is a peripheral device which interfaces to almost any LCD with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 60 segments. In addition, the PCF8534A can be easily cascaded for larger LCD applications. The PCF8534A is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized using display RAM with auto-incremented addressing, hardware subaddressing and display memory switching (static and duplex drive modes).

The PCF8534A complies with AEC-Q100 (automotive).

2. Features

- Single-chip LCD controller and driver
- Selectable backplane drive configurations: static or 2, 3 or 4 backplane multiplexing
- 60 segment drives:
  - 30 8-segment numeric characters
  - 16 15-segment alphanumeric characters
  - Any graphics of up to 240 elements
- Cascading supported for larger applications
- 60 × 4-bit display data storage RAM
- Wide LCD supply range: from 2.5 V for low threshold LCDs up to 6.5 V for guest-host LCDs and high threshold (automobile) twisted nematic LCDs
- Internal LCD bias generation with voltage follower buffers
- Selectable display bias configurations: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Wide logic power supply range: from 1.8 V to 5.5 V
- LCD and logic supplies may be separated
- Low power consumption
- 400 kHz I^2C-bus interface
- Compatible with any microprocessors or microcontrollers
- No external components
- Display memory bank switching in static and duplex drive modes
- Auto-incremented display data loading
- Versatile blinking modes
- Silicon gate CMOS process

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Name	Description	Delivery form	Version
PCF8534AH/1	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	tape and reel	SOT315-1
PCF8534AU/DA/1	PCF8534AU	wire bond die; 76 bonding pads; 2.91 × 2.62 × 0.38 mm	chip in tray	PCF8534AU

4. Marking

Table 2. Marking codes

Type number	Marking code
PCF8534AH/1	PCF8534AH
PCF8534AU/DA/1	PC8534A-1

5. Block diagram

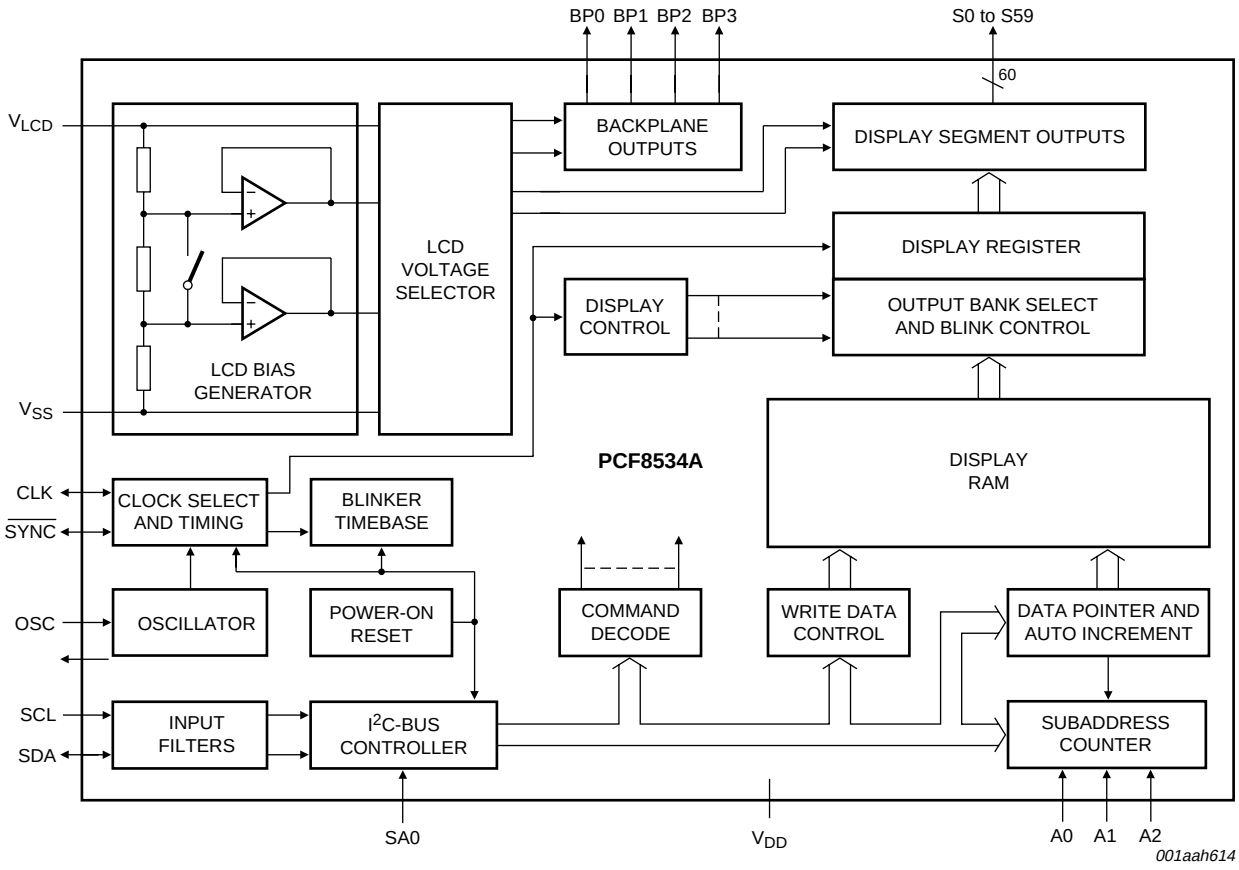
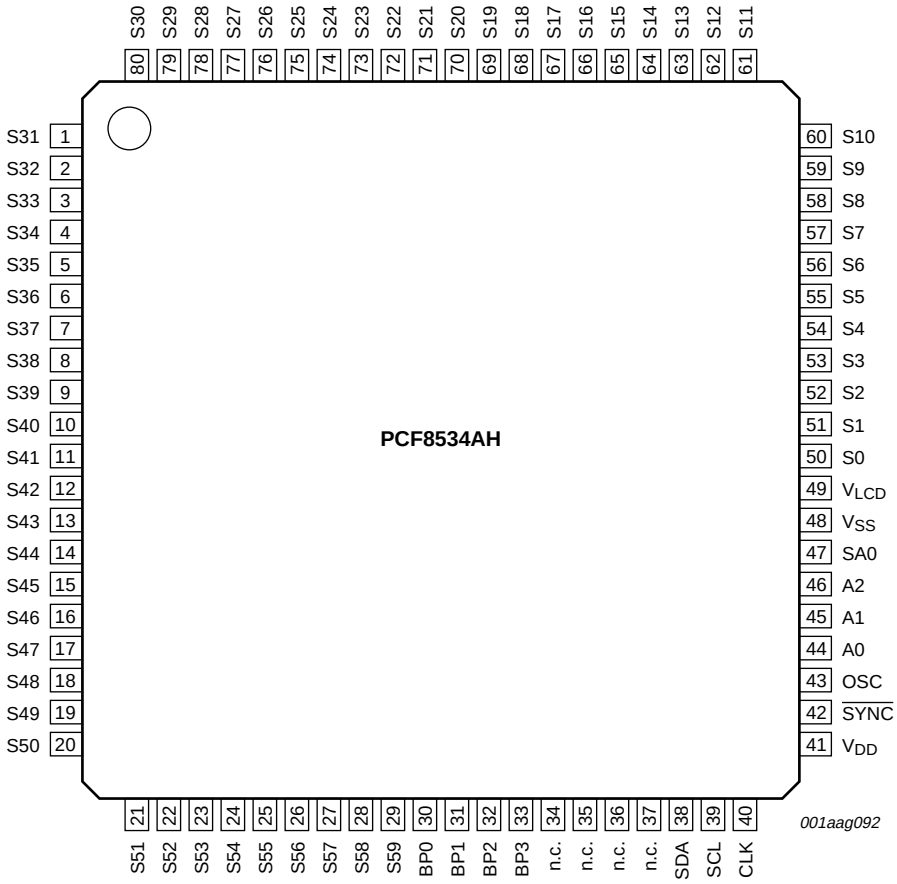


Fig 1. Block diagram of PCF8534A

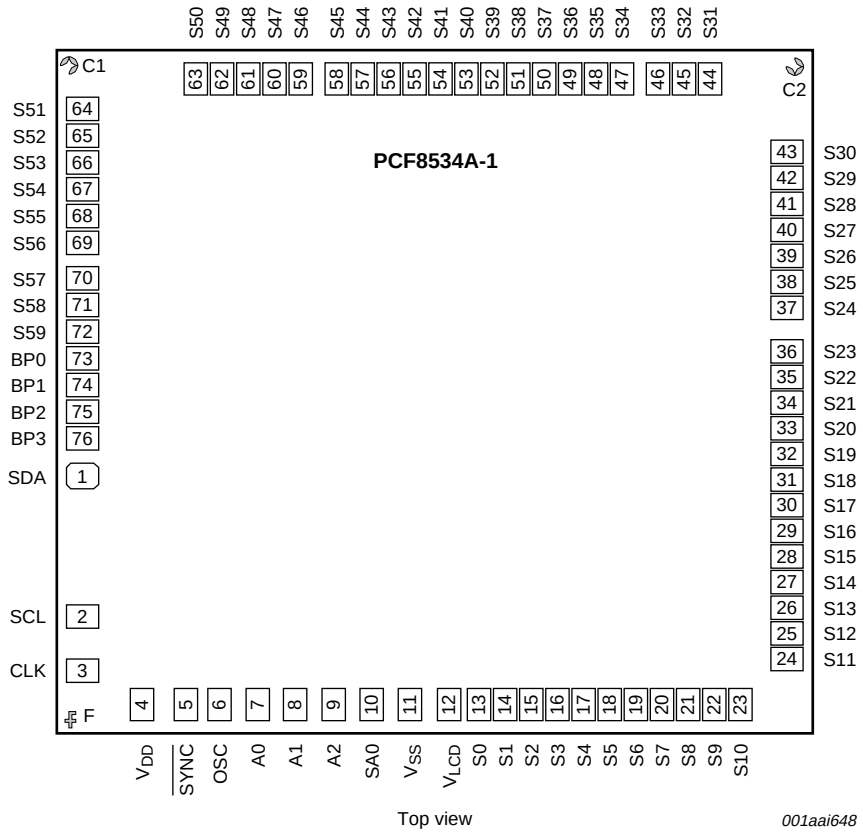
6. Pinning information

6.1 Pinning



Top view. For mechanical details, see Figure 23.

Fig 2. PCF8534AH/1 pin configuration (SOT315-1)



For mechanical details, see Figure 24.

Fig 3. PCF8534AU/DA/1 pin configuration (bare die)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT315	Bare die	
S31 to S59	1 to 29	44 to 72	LCD segment output 31 to 59
BP0 to BP3	30 to 33	73 to 76	LCD backplane output 0 to 3
n.c.	34 to 37	-	not connected
SDA	38	1	I^2C-bus serial data input and output
SCL	39	2	I^2C-bus serial clock input
CLK	40	3	external clock input and output
V_{DD}	41	4	supply voltage
$\overline{SYNC}$	42	5	cascade synchronization input and output (active LOW)
OSC	43	6	enable input for internal oscillator
A0 to A2	44 to 46	7 to 9	subaddress counter input 0 to 2
SA0	47	10	I^2C-bus slave address input 0
V_{SS}	48	11[1]	ground
V_{LCD}	49	12	input of LCD supply voltage
S0 to S30	50 to 80	13 to 43	LCD segment output 0 to 30

[1] The substrate (rear side of the die) is wired to V_{SS} but should not be electrically connected.

7. Functional description

The PCF8534A is a versatile peripheral device designed to interface any microprocessor or microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 60 segments.

The display configurations possible with the PCF8534A depend on the number of active backplane outputs required. Display configuration selection is shown in Table 4. All of the display configurations can be implemented in the typical system shown in Figure 4.

Table 4. Selection of display configurations

Backplanes	Segments	7-segment numeric		14-segment numeric		Dot matrix
		Digits	Indicator symbols	Characters	Indicator symbols	
4	240	30	30	16	16	240 (4 × 60)
3	180	22	26	12	12	180 (3 × 60)
2	120	15	15	8	8	120 (2 × 60)
1	60	7	11	4	4	60 (1 × 60)

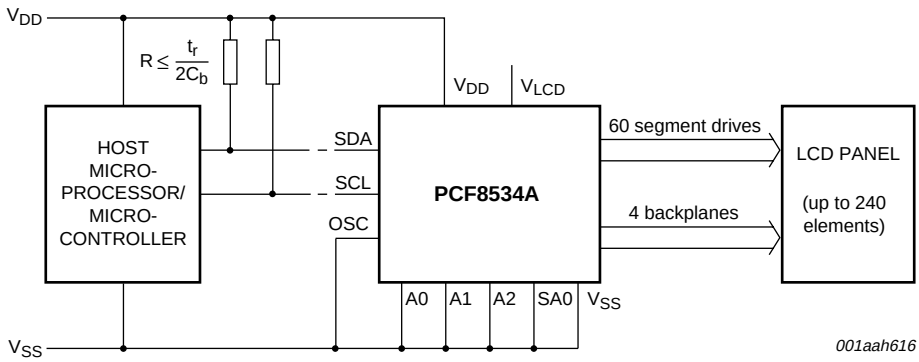


Fig 4. Typical system configuration

The host microprocessor or microcontroller maintains the 2-line I²C-bus communication channel with the PCF8534A.

Biasing voltages for the multiplexed LCD waveforms are generated internally, removing the need for an external bias generator. The internal oscillator is selected by connecting pin OSC to V_{SS}. The only other connections required to complete the system are the power supplies (pins V_{DD}, V_{SS} and V_{LCD}) and the LCD panel selected for the application.

7.1 Power-on reset

At power-on the PCF8534A resets to a default starting condition:

- All backplane outputs are set to V_{LCD}
- All segment outputs are set to V_{LCD}
- The selected drive mode is: 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I²C-bus interface is initialized
- The data pointer and the subaddress counter are cleared (set to logic 0)
- The display is disabled

Do not transfer data on the I²C-bus after a power-on for 1 ms to enable the reset action to complete.

7.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider comprising three series resistors connected between pins V_{LCD} and V_{SS}. The center resistor is switched out of the circuit to provide the $\frac{1}{2}$ bias voltage level for the 1:2 multiplex configuration.

7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD based on the selected LCD drive configuration. The operation of the voltage selector is controlled by mode set commands from the command decoder.

Table 5 shows the biasing configurations applicable to the preferred operating modes together with the biasing characteristics as functions of V_{oper} and the resulting discrimination ratios (D).

A practical value for V_{oper} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{oper} > 3V_{th}$.

Multiplex drive ratios of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller e.g.:

$\sqrt{3} = 1.732$ for 1:3 multiplex or $\left(\frac{\sqrt{21}}{3} = 1.528\right)$ for 1:4 multiplex

The advantage of these modes is the reduction of the LCD full-scale voltage V_{oper} as follows:

- 1:3 multiplex (½ bias): $V_{oper} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{oper} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

These compare with $V_{oper} = 3V_{off(RMS)}$ when ⅓ bias is used. It should be noted that $V_{oper} = V_{LCD}$.

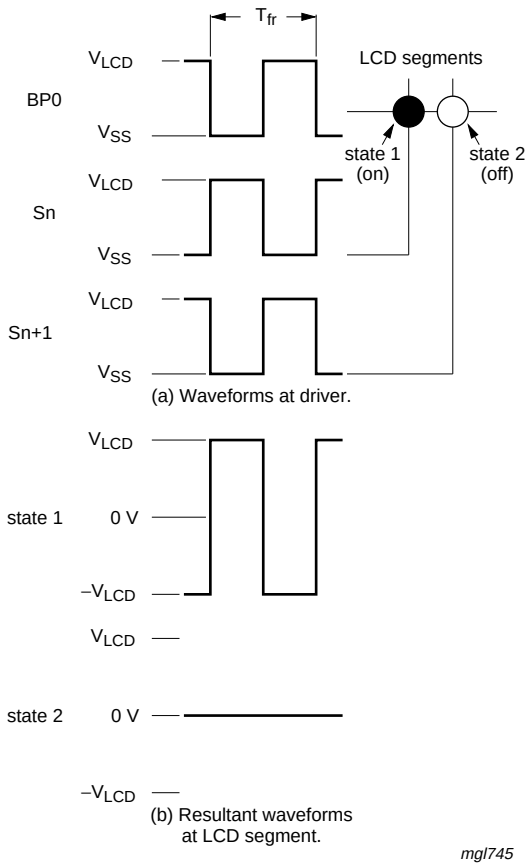
Table 5. Preferred LCD drive modes: summary of characteristics

LCD drive mode	Number of		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{oper}}$	$\frac{V_{on(RMS)}}{V_{oper}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2	2	3	½	0.354	0.791	2.234
1:2	2	4	⅓	0.333	0.745	2.237
1:3	3	4	⅓	0.333	0.638	1.915
1:4	4	4	⅓	0.333	0.577	1.732

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 5.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

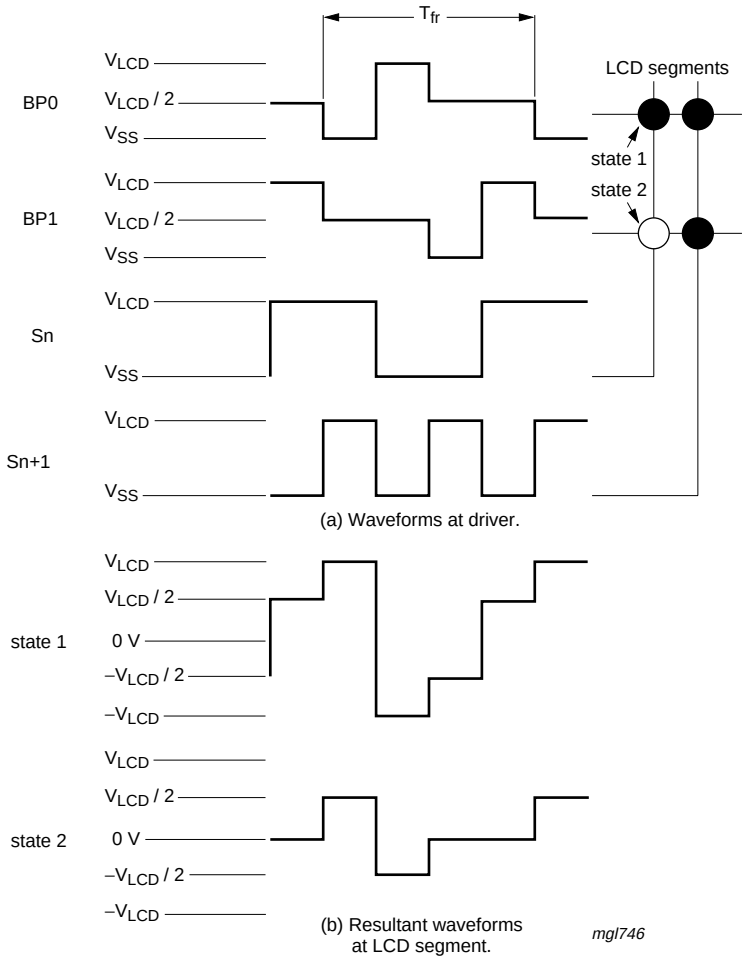
$V_{state2}(t) = V_{(Sn + 1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 5. Static drive mode waveforms

7.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF8534A allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 6 and Figure 7.



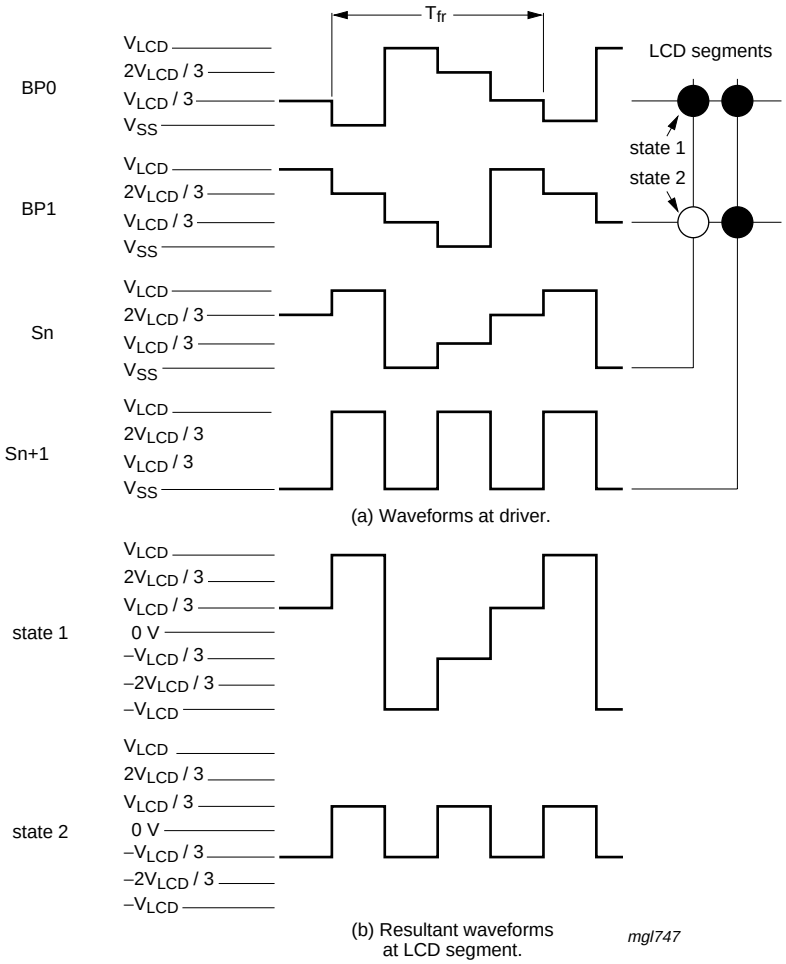
$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$.

Fig 6. Waveforms for the 1:2 multiplex drive mode with ½ bias



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

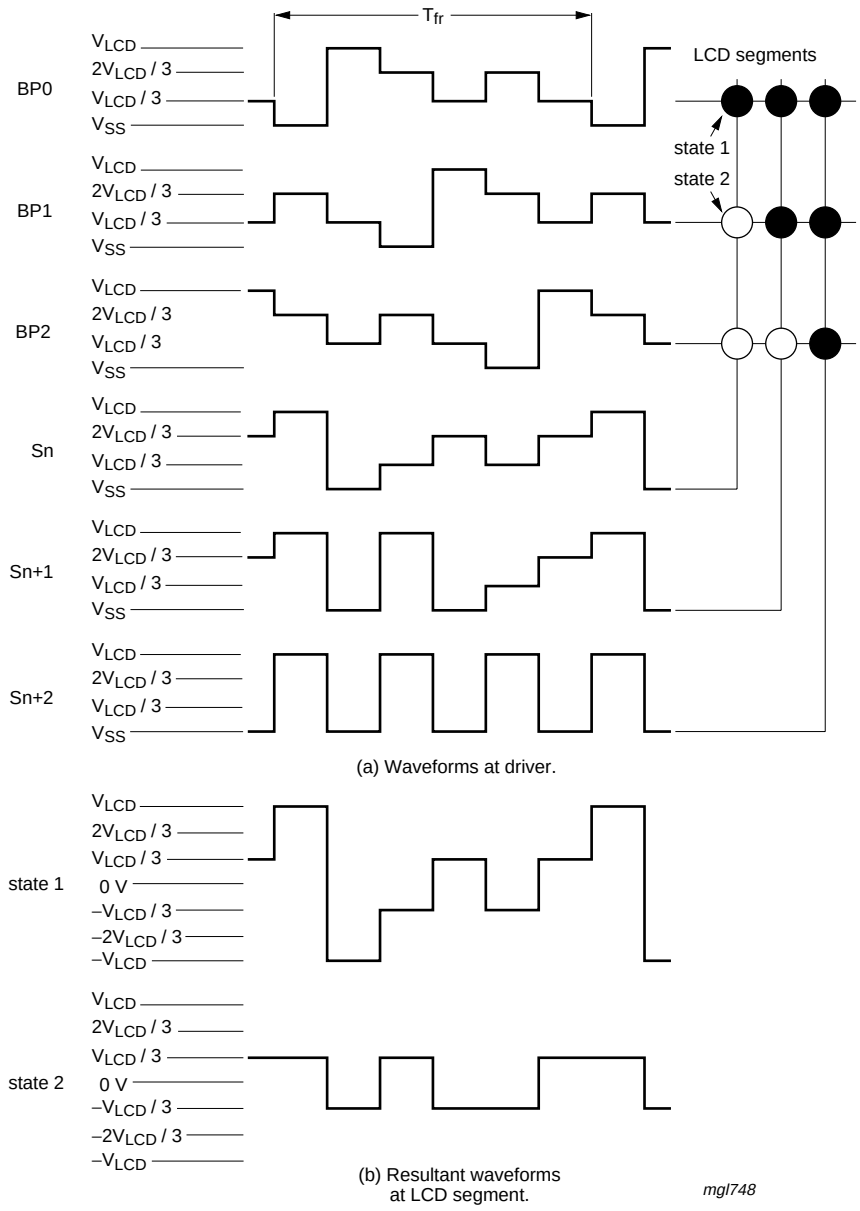
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 7. Waveforms for the 1:2 multiplex drive mode with ⅓ bias

7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 8.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

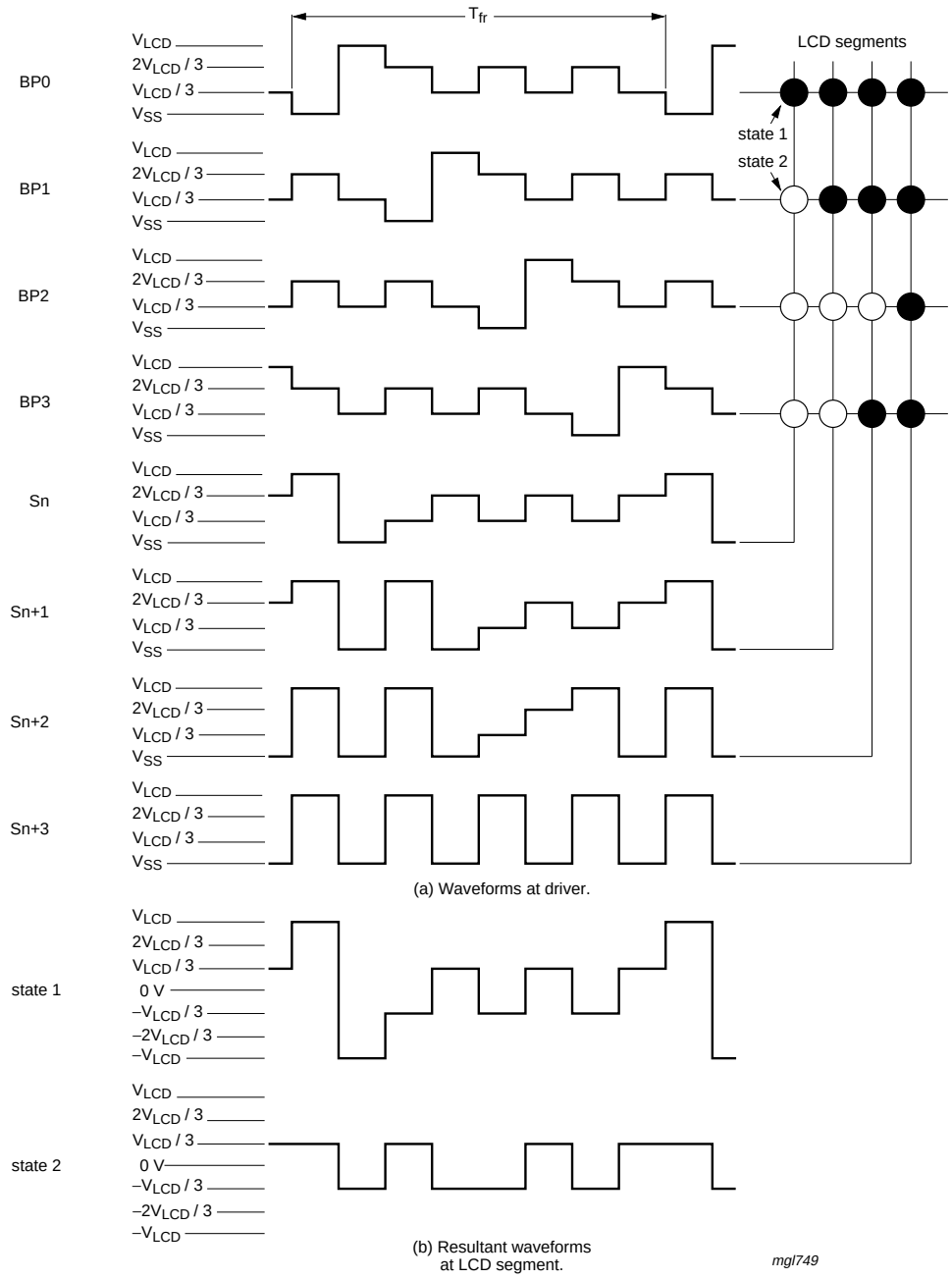
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 8. Waveforms for the 1:3 multiplex drive mode with $\frac{1}{3}$ bias

7.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 9.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 9. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

7.5 Oscillator

The internal logic and the LCD drive signals of the PCF8534A are timed by the frequency f_{clk}, which equals either the built-in oscillator frequency f_{osc} or the external clock frequency $f_{clk(ext)}$. The clock frequency f_{clk} determines the LCD frame frequency (f_{fr}).

7.5.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. In this case, the output from pin CLK is the clock signal for any cascaded PCF8534A in the system. After power-on, SDA must be HIGH to guarantee that the clock starts.

7.5.2 External clock

Connecting pin OSC to V_{DD} enables an external clock source. Pin CLK becomes the external clock input. A clock signal must always be applied to the device, removing the clock can freeze the LCD in a DC state.

7.6 Timing

The timing of the PCF8534A sequences the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal ($\overline{SYNC}$) maintains the correct timing relationship between all the PCF8534As in the system. The timing also generates the LCD frame frequency which is derived as an integer division of the clock frequency (see Table 6). When an external clock is used, the frame frequency is a fixed division of the internal clock or the frequency applied to pin CLK.

Table 6. LCD frame frequencies

Frame frequency	Nominal frame frequency (Hz)
$f_{fr} = \frac{f_{clk}}{24}$	64

7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display register, the LCD segment outputs and one column of the display RAM.

7.8 Segment outputs

The LCD drive section includes 60 segment outputs (S0 to S59) which must be connected directly to the LCD. The segment output signals are generated based on the multiplexed backplane signals and with data resident in the display register. When less than 60 segment outputs are required the unused segment outputs must be left open-circuit.

7.9 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated based on the selected LCD drive mode.

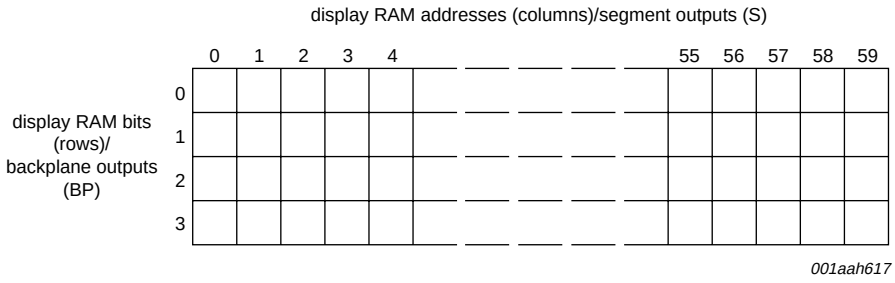
- In 1:4 multiplex drive mode: BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required the unused outputs can be left as an open-circuit.

- In 1:3 multiplex drive mode: BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode: BP0 and BP2, BP1 and BP3 respectively carry the same signals and can also be paired to increase the drive capabilities.
- In static drive mode: the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.10 Display RAM

The display RAM is static 60 × 4-bit RAM which stores LCD data. Logic 1 in the RAM bit map indicates the on-state of the corresponding LCD segment, logic 0 indicates the off-state. There is a direct relationship between RAM addresses and the segment outputs and the individual bits of a RAM word and the backplane outputs. The first RAM row corresponds to the 60 segments operated with respect to backplane BP0 (see Figure 10). In multiplexed LCD applications, the segment data of rows 1 to 4 of the display RAM are time-multiplexed with BP0, BP1, BP2 and BP3, respectively.



Display RAM bit map showing the direct relationship between backplane outputs, display RAM addresses and segment outputs and between bits in a RAM word and backplane outputs.

Fig 10. Display RAM bit map

When display data is transmitted to the PCF8534A, the display bytes received are stored in the display RAM based on the selected LCD drive mode. Data is stored as it arrives and does not wait for the acknowledge cycle. Depending on the current multiplexer mode data is stored singularly, in pairs, triplets or quadruplets. In 1:2 multiplexer mode for example, RAM data is stored every second bit. An example of a 7-segment numeric display illustrating the storage order for all drive modes is shown in Figure 11. The RAM storage organization applies equally to other LCD types.

The following applies to Figure 11:

- Static drive mode: the eight transmitted data bits are placed in row 0 to eight successive display RAM addresses.
- 1:2 multiplex drive mode: the eight transmitted data bits are placed in row 0 and 1 to four successive display RAM addresses.
- 1:3 multiplex drive mode: the eight transmitted data bits are placed in row 0, 1 and 2 to three successive addresses. However, bit 2 of the third address is left unchanged. This last bit can, if necessary, be controlled by an additional transfer to this address but avoid overriding adjacent data because full bytes are always transmitted.
- 1:4 multiplex drive mode: the eight transmitted data bits are placed in row 0, 1, 2 and 3 to two successive display RAM addresses.

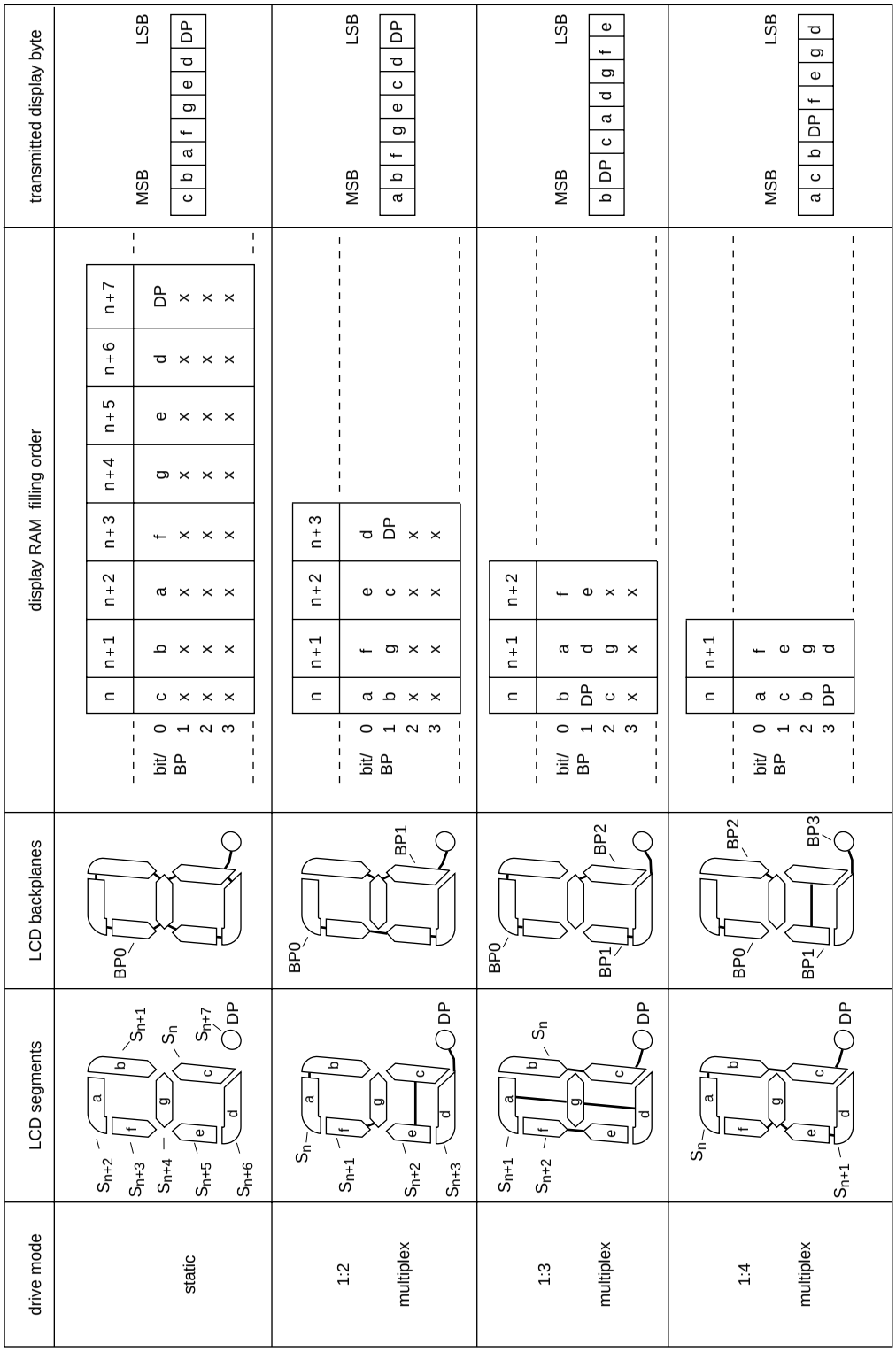
7.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load data pointer command. After this, the data byte is stored starting at the display RAM address indicated by the data pointer (see Figure 11). Once each byte is stored, the data pointer is automatically incremented based on the selected LCD configuration.

The contents of the data pointer are incremented as follows:

- In static drive mode by eight.
- In 1:2 multiplex drive mode by four.
- In 1:3 multiplex drive mode by three.
- In 1:4 multiplex drive mode by two.

If an I^2C-bus data access terminates early, the state of the data pointer is unknown. Consequently, the data pointer must be rewritten prior to further RAM accesses.



x = data bit unchanged.

Fig 11. Relationship between LCD layout, drive mode, display RAM storage order and display data transmitted over the I²C-bus

7.12 Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the device select command (see Table 12). If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is blocked but the data pointer will be incremented as if data storage had taken place.

In cascaded applications each PCF8534A in the cascade must be addressed separately. Initially, the first PCF8534A is selected by sending the device select command matching the first device's hardware subaddress. Then the data pointer is set to the preferred display RAM address by sending the load data pointer command.

Once the display RAM of the first PCF8534A has been written, the second PCF8534A is selected by sending the device select command again. This time however the command matches the second device's hardware subaddress. Next the load data pointer command is sent to select the preferred display RAM address of the second PCF8534A.

This last step is very important because during writing data to the first PCF8534A, the data pointer of the second PCF8534A is incremented. In addition, the hardware subaddress should not be changed whilst the device is being accessed on the I^2C-bus interface.

7.13 Output bank selector

The output bank selector (see Table 13), selects one of the four bits per display RAM address for transfer to the display register. The actual bit selected depends on the LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode: all RAM addresses of bit 0 are selected, followed sequentially by the contents of bit 1, bit 2 and then bit 3.
- In 1:3 multiplex mode: bits 0, 1 and 2 are selected sequentially.
- In 1:2 multiplex mode: bits 0 and 1 are selected.
- In the static mode: bit 0 is selected.

The $\overline{\text{SYNC}}$ signal resets these sequences to the following starting points: bit 3 for 1:4 multiplex, bit 2 for 1:3 multiplex, bit 1 for 1:2 multiplex and bit 0 for static mode.

The PCF8534A includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In static drive mode, the bank select command may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In 1:2 multiplex drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This enables preparation of display information in an alternative bank and the ability to switch to it once it has been assembled.

7.14 Input bank selector

The input bank selector loads display data into the display RAM based on the selected LCD drive configuration. Using the bank select command, display data can be loaded in bit 2 into static drive mode or in bits 2 and 3 into 1:2 multiplex drive mode. The input bank selector functions independently to the output bank selector.

7.15 Blinker

The display blinking capabilities of the PCF8534A are very versatile. The whole display can be blinked at frequencies set by the blink select command (see Table 14). The blinking frequencies are fractions of the clock frequency. The ratios between the clock and blinking frequencies depend on the mode in which the device is operating (see Table 7).

Table 7. Blink frequencies

Assuming that f_{clk} = 1536 Hz.

Blink mode	Operating mode ratio	Blink frequency
Off	-	Blinking off
1	$f_{blink} = \frac{f_{clk}}{768}$	2 Hz
2	$f_{blink} = \frac{f_{clk}}{1536}$	1 Hz
3	$f_{blink} = \frac{f_{clk}}{3072}$	0.5 Hz

An additional feature is for the arbitrary selection of LCD segments to be blinked. This applies to the static and 1:2 multiplex drive modes and is implemented without any communication overheads. Using the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the blink select command.

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display needs to be blinked at a frequency other than the nominal blinking frequency, this can be done using the mode set command to set and reset the display enable bit E at the required rate (see Table 10).

8. Basic architecture

8.1 Characteristics of the I²C-bus

The I²C-bus provides bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). When connected to the output stages of a device, both lines must be connected to a positive supply via a pull-up resistor. Data transfer is initiated only when the bus is not busy.

8.1.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 12.

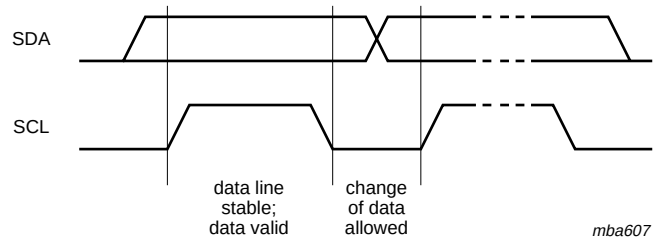


Fig 12. Bit transfer

8.1.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S).
A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 13.

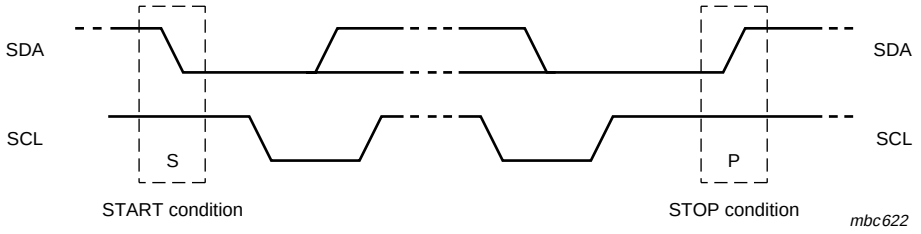


Fig 13. Definition of START and STOP conditions

8.1.2 System configuration

A device generating a message is a ‘transmitter’ and a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’. The system configuration is illustrated in Figure 14.

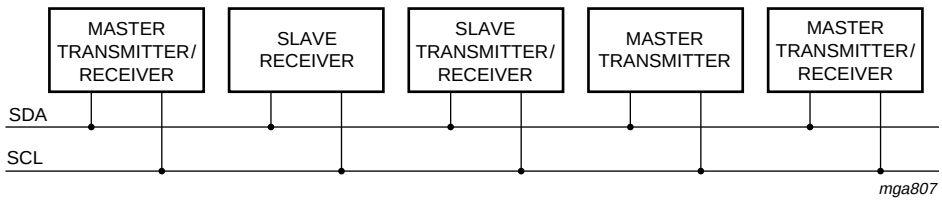


Fig 14. System configuration

8.1.3 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the master receiver must leave the data line HIGH during the 9th pulse to not acknowledge. The master will now generate a STOP condition.

Acknowledgement on the I²C-bus is illustrated in Figure 15.

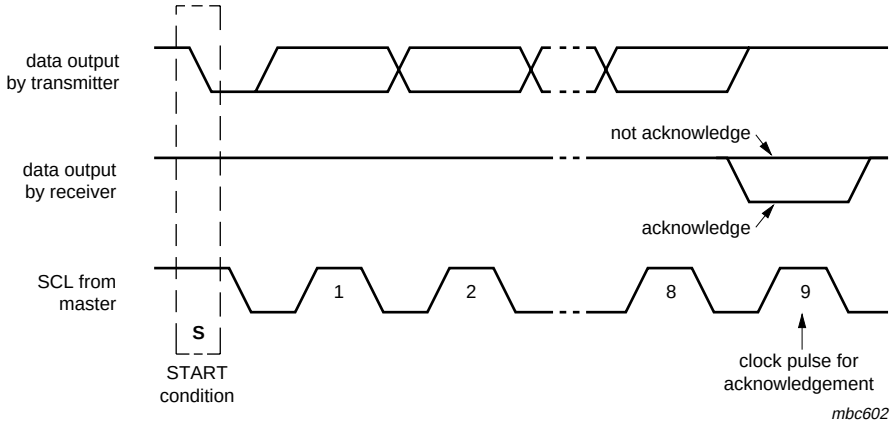


Fig 15. Acknowledgement of the I²C-bus

8.1.4 PCF8534A I²C-bus controller

The PCF8534A acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8534A are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, the transferred command data and the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} using a binary coding scheme so that no two devices with a common I²C-bus slave address have the same hardware subaddress.

8.1.5 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

8.2 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are reserved for the PCF8534A. The least significant bit of the slave address is bit R/$\overline{W}$. The PCF8534A is a write-only device. It will not respond to a read access, so this bit should always be logic 0. The second bit of the slave address is defined by the level tied at input SA0. Two displays controlled by PCF8534A can be recognized on the same I²C-bus which allows:

- Up to 16 PCF8534As on the same I²C-bus for very large LCD applications
- The use of two types of LCD multiplex on the same I²C-bus

The I²C-bus protocol is shown in Figure 17. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the available PCF8534A slave addresses. All PCF8534As with the same SA0 level acknowledge in parallel to the slave address. All PCF8534As with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, the control byte is sent defining if the next byte is RAM or command information. The control byte also defines if the next byte is a control byte or further RAM/command data (see Figure 16 and Table 8). In this way it is possible to configure the device and then fill the display RAM with little overhead.

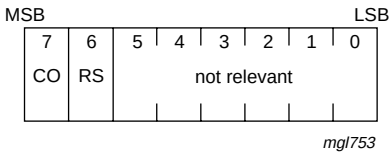


Fig 16. Control byte format

Table 8. Load data pointer command bit description

Bit	Symbol	Value	Description
7	CO		**continue bit**
		0	last control byte
		1	control bytes continue
6	RS		**register selection**
		0	command register
		1	data register
5 to 0	-		not relevant

The command bytes and control bytes are also acknowledged by all addressed PCF8534As connected to the bus.

The display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated.

The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed PCF8534A. After the last display byte, the I²C-bus master issues a STOP condition (P). Alternatively a START may be issued to RESTART I²C-bus access.

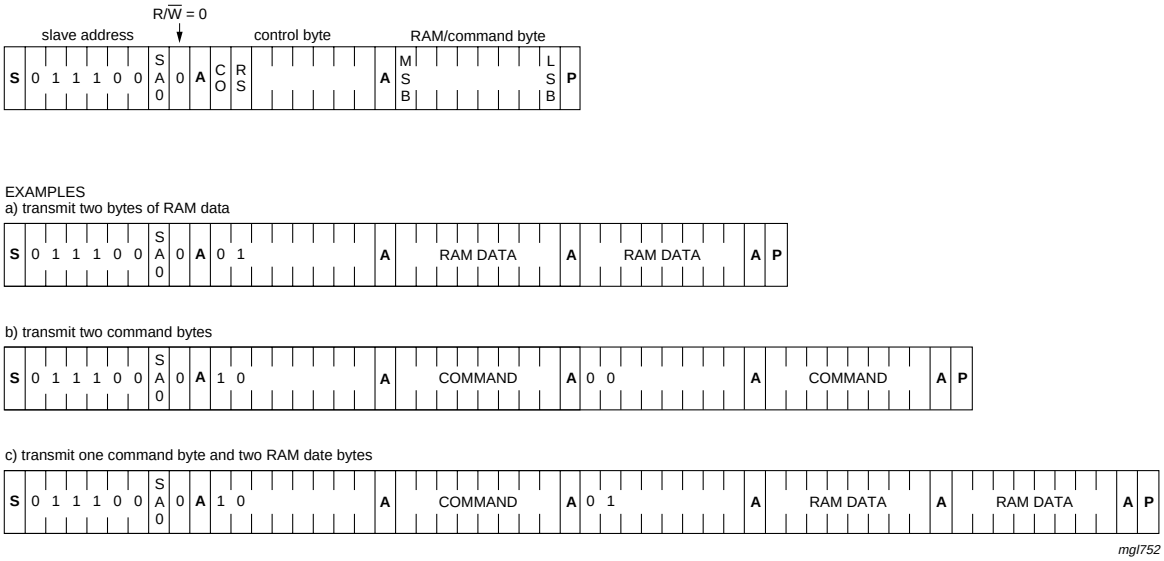


Fig 17. I²C-bus protocol

8.3 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. There are five commands:

Table 9. Definition of commands

Command	Opcode								Reference
Mode set	1	1	0	0	E	B	M1	M0	Table 10
Load data pointer	0	P6	P5	P4	P3	P2	P1	P0	Table 11
Device select	1	1	1	0	0	A2	A1	A0	Table 12
Bank select	1	1	1	1	1	0	I	O	Table 13
Blink select	1	1	1	1	0	A	BF1	BF0	Table 14

Table 10. Mode set command bit description

Bit	Symbol	Value	Description
7 to 4	-	1100	fixed value
3	E		**display status** the possibility to disable the display allows implementation of blinking under external control
		0	disabled (blank)
		1	enable
2	B		**LCD bias configuration**
		0	1/3 bias
		1	1/2 bias

Table 10. Mode set command bit description *...continued*

Bit	Symbol	Value	Description
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; 1 backplane
		10	1:2 multiplex; 2 backplanes
		11	1:3 multiplex; 3 backplanes
		00	1:4 multiplex; 4 backplanes

Table 11. Load data pointer command bit description

See Section 7.11.

Bit	Symbol	Value	Description
7	-	0	fixed value
6 to 0	P[6:0]	000 0000 to 011 1011	7-bit binary value of 0 to 59

Table 12. Device select command bit description

See Section 7.12.

Bit	Symbol	Value	Description
7 to 3	-	1 1100	fixed value
2 to 0	A[2:0]	000 to 111	3-bit binary value of 0 to 7

Table 13. Bank select command bit description

See Section 7.10, Section 7.11, Section 7.12, Section 7.13 and Section 7.14.

Bit	Symbol	Value	Description	
			Static	**1:2 multiplex[1]**
7 to 2	-	11 1110	fixed value	
1	I		**input bank selection**: storage of arriving display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3
0	O		**output bank selection**: retrieval of LCD display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3

[1] The bank select command has no effect in 1:3 or 1:4 multiplex drive modes.

Table 14. Blink select command bit description

See Section 7.15.

Bit	Symbol	Value	Description
7 to 3	-	1 1110	fixed value
2	A		**blink mode selection**
		0	normal blinking[1]
		1	blinking by alternating display RAM banks
1 to 0	BF[1:0]		**blink frequency selection**
		00	off
		01	1
		10	2
		11	3

[1] Only normal blinking can be selected in multiplexer 1:3 or 1:4 drive modes.

8.4 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8534A and coordinates their effects.
The controller also loads display data into the display RAM as required by the storage order.

9. Internal circuitry

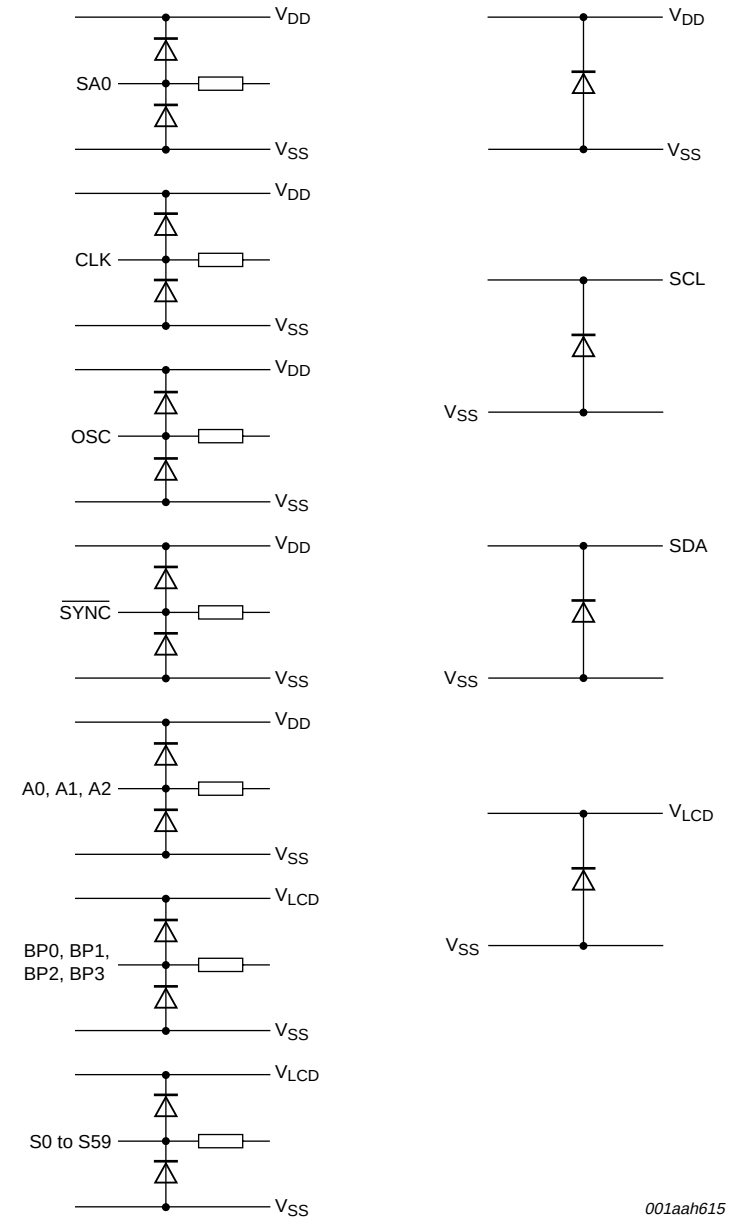


Fig 18. Device protection diagram

10. Limiting values

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

Table 15. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+6.5	V
I_{DD}	supply current			–50	+50	mA
V_{LCD}	LCD supply voltage			–0.5	+7.5	V
$I_{DD(LCD)}$	LCD supply current			–50	+50	mA
I_{SS}	ground supply current			–50	+50	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_I	input current		[1]	–10	+10	mA
V_O	output voltage		[1]	–0.5	+6.5	V
			[2]	–0.5	+7.5	V
I_O	output current		[1][2]	–10	+10	mA
P_{tot}	total power dissipation			-	400	mW
P/out	power dissipation per output			-	100	mW
T_{stg}	storage temperature			–65	+150	°C
V_{esd}	electrostatic discharge voltage	HBM	[3]	-	±2000	V
		MM	[4]	-	±200	V
		CDM	[5]	-	±2000	V
I_{lu}	latch-up current		[6]	-	100	mA

[1] Pins SDA, SCL, CLK, $\overline{SYNC}$, SA0, OSC and A0 to A2.

[2] Pins S0 to S59 and BP0 to BP3.

[3] HBM: Human Body Model, according to JESD22-A114.

[4] MM: Machine Model, according to JESD22-A115.

[5] CDM: Charged Device Model, according to JESD22-C101.

[6] Latch-up testing, according to JESD78.

11. Static characteristics

Table 16. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			1.8	-	5.5	V
V_{LCD}	LCD supply voltage			2.5	-	6.5	V
I_{DD}	supply current	f_{clk} = 1536 Hz	[1]	-	8	20	µA
$I_{DD(LCD)}$	LCD supply current	f_{clk} = 1536 Hz	[1]	-	24	60	µA
Logic							
V_I	input voltage			V_{SS} − 0.5		V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2 and SA0		V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2 and SA0		$0.7V_{DD}$	-	V_{DD}	V
V_{POR}	power-on reset voltage			1.0	1.3	1.6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V; on pins CLK and $\overline{SYNC}$		1	-	-	mA
I_{OH}	HIGH-level output current	V_{OH} = 4.6 V; V_{DD} = 5 V; on pin CLK		−1	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}; on pins SA0, A0 to A2 and CLK		−1	-	+1	µA
		V_I = V_{DD}; on pin OSC		−1	-	+1	µA
C_I	input capacitance		[2]	-	-	7	pF
I^2C-bus; pins SDA and SCL							
V_I	input voltage			V_{SS} − 0.5	-	5.5	V
V_{IL}	LOW-level input voltage	pin SCL		V_{SS}	-	$0.3V_{DD}$	V
		pin SDA		V_{SS}	-	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V; on pin SDA		3	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}		−1	-	+1	µA
C_i	input capacitance		[2]	-	-	7	pF
LCD outputs							
Output pins BP0, BP1, BP2 and BP3							
V_{BP}	voltage on pin BP	C_{bpl} = 35 nF	[3]	−100	-	+100	mV
R_{BP}	resistance on pin BP	V_{LCD} = 5 V	[4]	-	1.5	10	kΩ
Output pins S0 to S59							
V_S	voltage on pin S	C_{sgm} = 35 nF	[5]	−100	-	+100	mV
R_S	resistance on pin S	V_{LCD} = 5 V	[4]	-	6.0	13.5	kΩ

[1] LCD outputs are open circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I^2C-bus inactive.

[2] Not tested, design specification only.

[3] C_{bpl} = backplane capacitance.

[4] Outputs measured individually and sequentially.

[5] C_{sgm} = segment capacitance.

12. Dynamic characteristics

Table 17. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
Internal: output pin CLK							
f_{osc}	oscillator frequency	V_{DD} = 5 V	[1]	960	1536	3046	Hz
External: input pin CLK							
$f_{clk(ext)}$	external clock frequency	V_{DD} = 5 V		797	1536	3046	Hz
$t_{clk(H)}$	HIGH-level clock time			130	-	-	µs
$t_{clk(L)}$	LOW-level clock time			130	-	-	µs
Synchronization: input pin $\overline{SYNC}$							
$t_{PD(SYNC\_N)}$	$\overline{SYNC}$ propagation delay			-	30	-	ns
t_{SYNC_NL}	$\overline{SYNC}$ LOW time			1	-	-	µs
Outputs: pins BP0 to BP3 and S0 to S59							
$t_{PD(drv)}$	driver propagation delay	V_{LCD} = 5 V		-	-	30	µs
I^2C-bus: timing	[2]						
Pin SCL							
f_{SCL}	SCL frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
Pin SDA							
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
Pins SCL and SDA							
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
t_r	rise time of both SDA and SCL signals			-	-	0.3	µs
t_f	fall time of both SDA and SCL signals			-	-	0.3	µs
C_b	capacitive load for each bus line			-	-	400	pF
$t_{w(spike)}$	spike pulse width			-	-	50	ns

[1] Typical output (duty cycle δ = 50 %).

[2] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

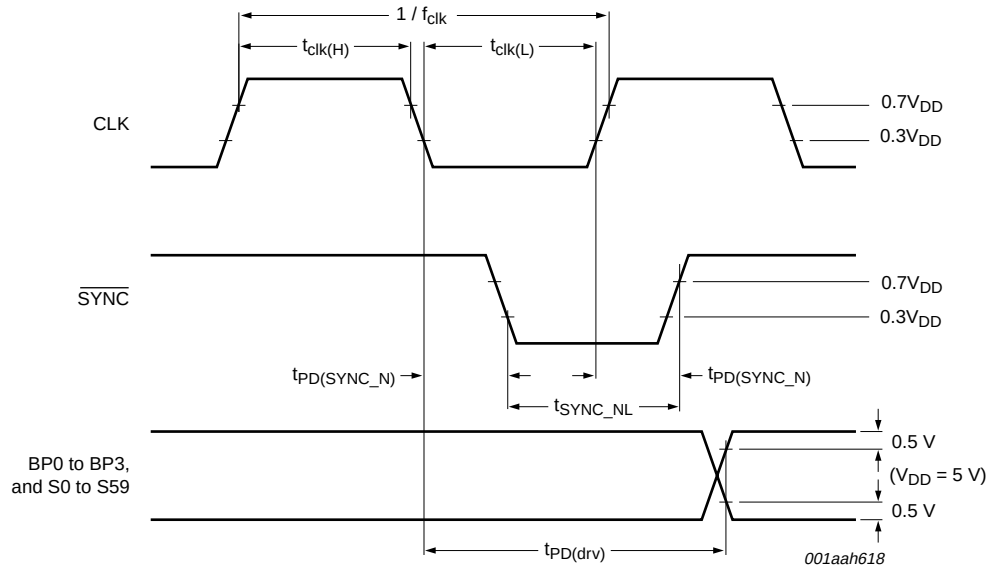


Fig 19. Driver timing waveforms

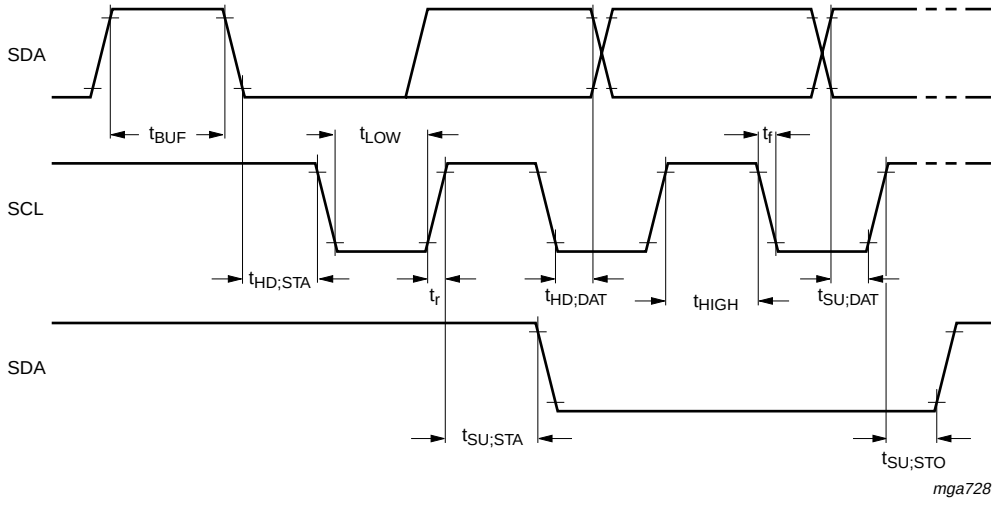


Fig 20. I²C-bus timing waveforms

13. Application information

13.1 Cascaded operation

Large display configurations of up to 16 PCF8534As can be recognized on the same I^2C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I^2C-bus slave address (SA0).

Table 18. Addressing cascaded PCF8534A

Cluster	Bit SA0	Pin A2	Pin A1	Pin A0	Device
1	0	0	0	0	0
		0	0	1	1
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
2	1	0	0	0	8
		0	0	1	9
		0	1	0	10
		0	1	1	11
		1	0	0	12
		1	0	1	13
		1	1	0	14
		1	1	1	15

If cascaded PCF8534As are synchronized, they can share the backplane signals from one of the devices in the cascade. This is cost-effective in large LCD applications because the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8534As in the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (see Figure 21).

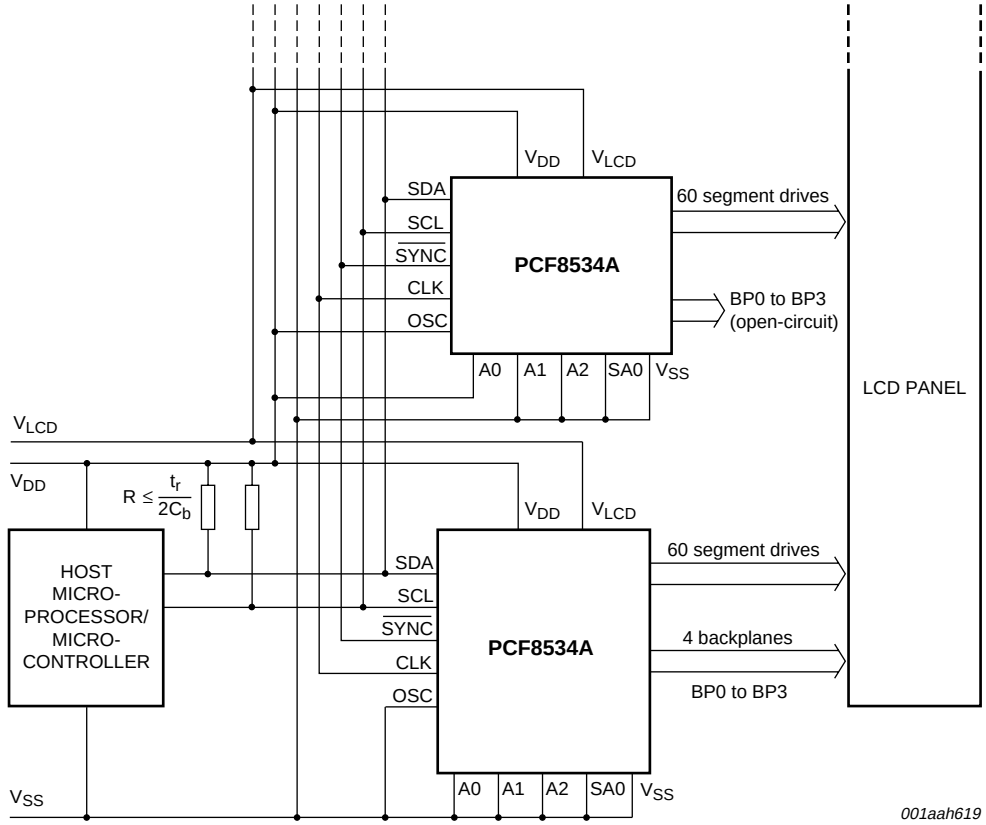


Fig 21. Cascaded PCF8534A configuration

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8534As. Synchronization is guaranteed after a power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments or by defining a multiplex mode when PCF8534As with different SA0 levels are cascaded).

$\overline{\text{SYNC}}$ is organized as an input/output pin. The output selection is realized as an open-drain driver with an internal pull-up resistor. A PCF8534A asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. If synchronization in the cascade is lost, it is restored by the first PCF8534A to assert $\overline{\text{SYNC}}$. The timing relationship between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8534A are shown in Figure 22.

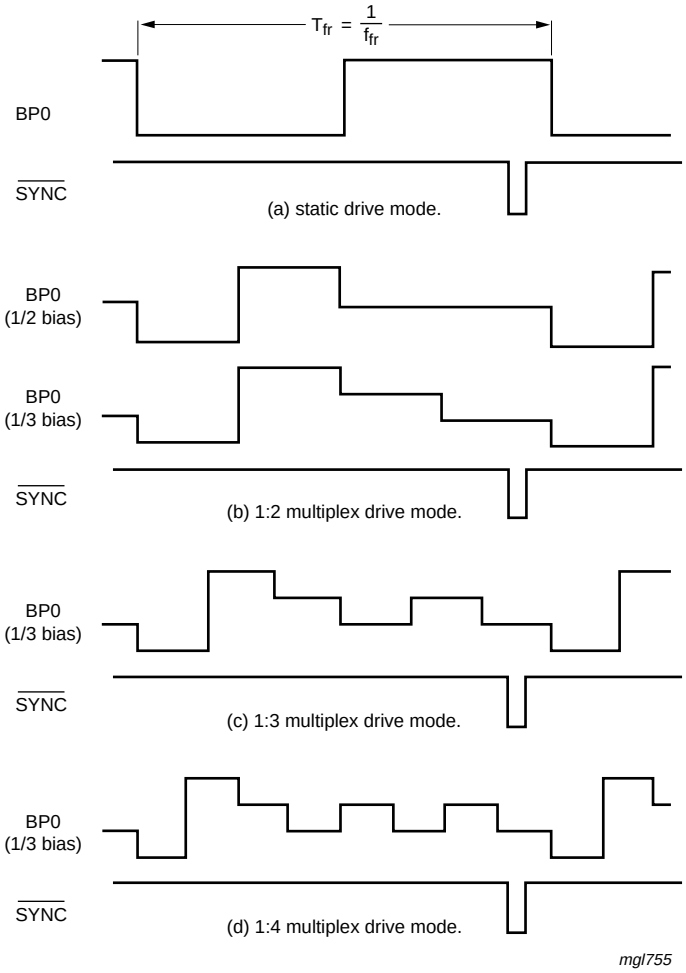


Fig 22. Synchronization of the cascade for various PCF8534A drive modes

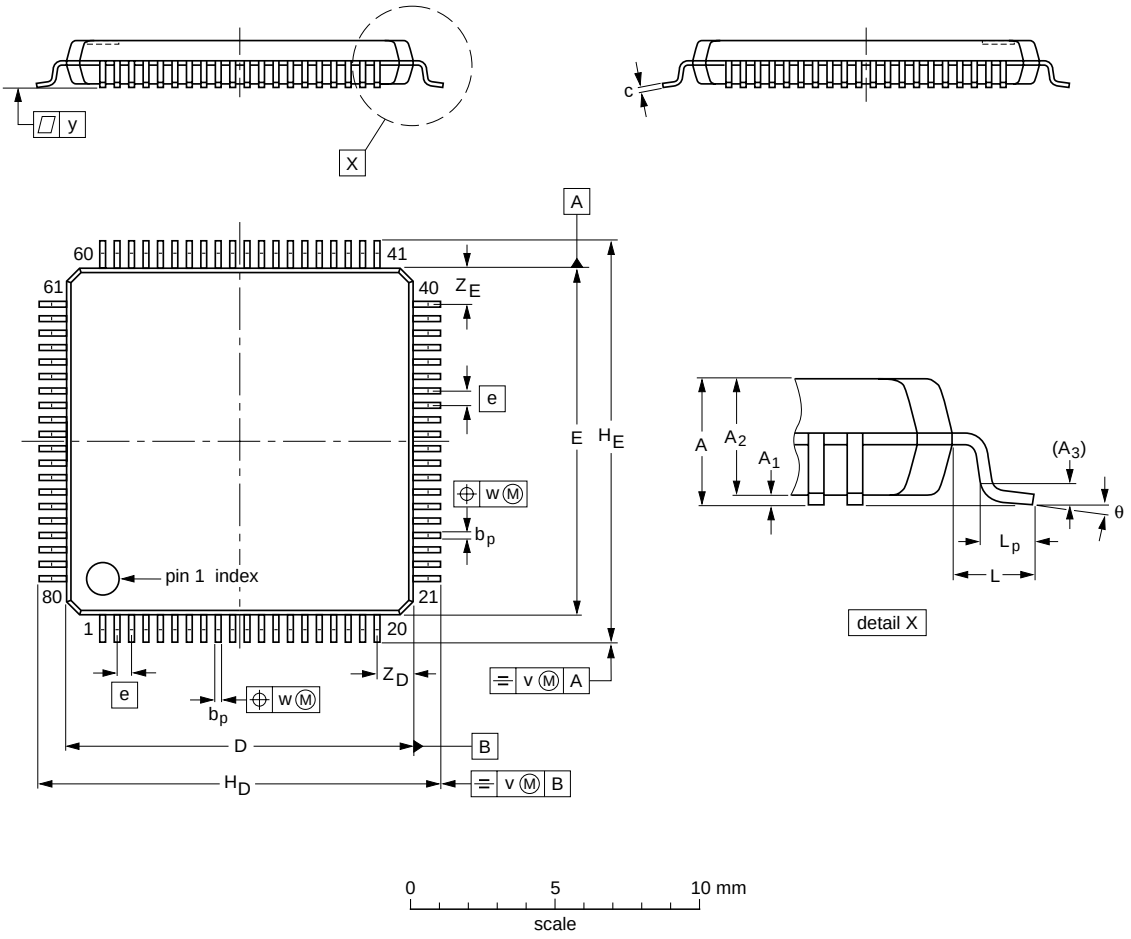
The contact resistance between the $\overline{SYNC}$ pins of cascaded devices must be controlled. If the resistance is too high, the device will not be able to synchronize properly. Table 19 shows the maximum contact resistance values.

Table 19. $\overline{SYNC}$ contact resistance

Number of devices	Maximum contact resistance
2	6000 Ω
3 to 5	2200 Ω
6 to 10	1200 Ω
11 to 16	700 Ω

14. Package outline

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

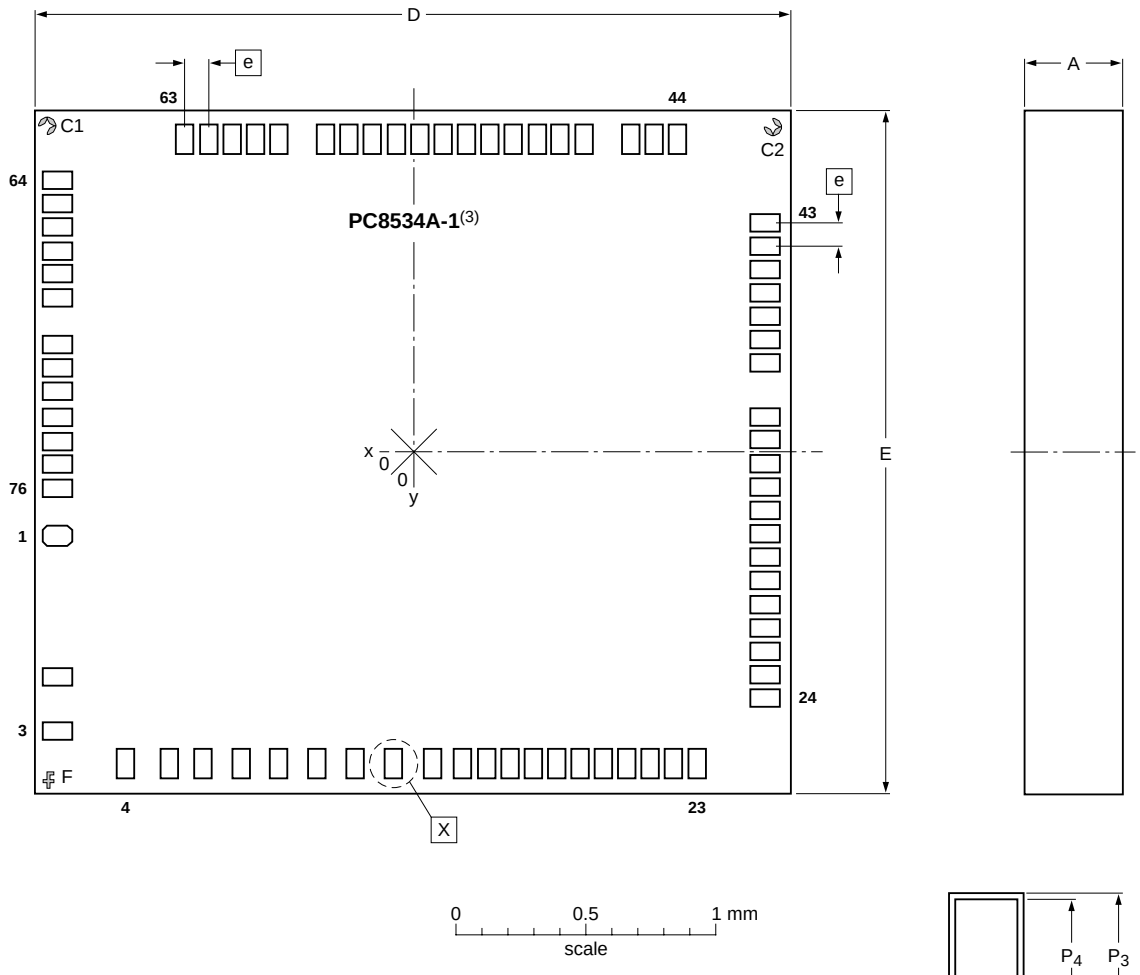
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT315-1	136E15	MS-026				~~00-01-19~~ 03-02-25

Fig 23. Package outline SOT315-1 (LQFP80)

15. Bare die outline

Wire bond die; 76 bonding pads; 2.91 x 2.62 x 0.38 mm **PCF8534AU**



DIMENSIONS (mm are the original dimensions)

UNIT		A	D	E	e	P_1(1)	P_2(2)	P_3(1)	P_4(2)
mm	max	0.38	2.91	2.62		0.06	0.05	0.10	0.09
	nom				0.08				
	min								

Notes
1. Pad size
2. Passivation opening
3. Marking code

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
PCF8534AU						08-08-06

Fig 24. PCF8534AU die outline

Table 20. Bonding pad locations

Symbol	Pad	Coordinates[1]		Description
		X (μm)	Y (μm)	
SDA	1	–1384.4	–280	I^2C-bus serial data input and output
SCL	2	–1384.4	–760.5	I^2C-bus serial clock input
CLK	3	–1384.4	–945	external clock input and output
V_{DD}	4	–978.7	–1238	supply voltage
$\overline{SYNC}$	5	–829.3	–1238	cascade synchronization input and output
OSC	6	–714.3	–1238	enable input for internal oscillator
A0	7	–584.3	–1238	subaddress counter input
A1	8	–454.3	–1238	
A2	9	–324.3	–1238	
SA0	10	–194.3	–1238	I^2C-bus slave address input 0
V_{SS}	11	–64.3	–1238	ground
V_{LCD}	12	68.7	–1238	input of LCD supply voltage
S0	13	173.7	–1238	LCD segment output
S1	14	253.7	–1238	
S2	15	333.7	–1238	
S3	16	413.7	–1238	
S4	17	493.7	–1238	
S5	18	573.7	–1238	
S6	19	653.7	–1238	
S7	20	733.7	–1238	
S8	21	813.7	–1238	
S9	22	893.7	–1238	
S10	23	973.7	–1238	
S11	24	1384.4	–841	
S12	25	1384.4	–761	
S13	26	1384.4	–681	
S14	27	1384.4	–601	
S15	28	1384.4	–521	
S16	29	1384.4	–441	
S17	30	1384.4	–361	
S18	31	1384.4	–281	
S19	32	1384.4	–201	
S20	33	1384.4	–121	
S21	34	1384.4	–41	
S22	35	1384.4	39	
S23	36	1384.4	119	
S24	37	1384.4	301.6	
S25	38	1384.4	381.6	
S26	39	1384.4	461.6	
S27	40	1384.4	541.6	

Table 20. Bonding pad locations *…continued*

Symbol	Pad	Coordinates[1]		Description
		X (μm)	Y (μm)	
S28	41	1384.4	621.6	LCD segment output
S29	42	1384.4	701.6	
S30	43	1384.4	781.6	
S31	44	896.5	1239.4	
S32	45	816.5	1239.4	
S33	46	736.5	1239.4	
S34	47	576.5	1239.4	
S35	48	496.5	1239.4	
S36	49	416.5	1239.4	
S37	50	336.5	1239.4	
S38	51	256.5	1239.4	
S39	52	176.5	1239.4	
S40	53	96.5	1239.4	
S41	54	16.5	1239.4	
S42	55	−63.5	1239.4	
S43	56	−143.5	1239.4	
S44	57	−223.5	1239.4	
S45	58	−303.5	1239.4	
S46	59	−463.5	1239.4	
S47	60	−543.5	1239.4	
S48	61	−623.5	1239.4	
S49	62	−703.5	1239.4	
S50	63	−783.5	1239.4	
S51	64	−1384.4	935	
S52	65	−1384.4	855	
S53	66	−1384.4	775	
S54	67	−1384.4	695	
S55	68	−1384.4	615	
S56	69	−1384.4	535	
S57	70	−1384.4	375	
S58	71	−1384.4	295	
S59	72	−1384.4	215	
BP0	73	−1384.4	125	LCD backplane output
BP1	74	−1384.4	45	
BP2	75	−1384.4	−35	
BP3	76	−1384.4	−115	

[1] All coordinates are referenced in μm to the center of the die (see Figure 24).

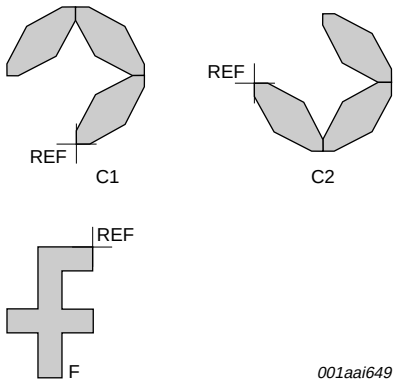


Fig 25. Alignment marks

Table 21. Alignment mark locations [1]

Symbol	X (μm)	Y (μm)
C1	–1387	1190
C2	1335	1242
F	–1345	–1173

[1] All coordinates are referenced in μm to the center of the die (see Figure 24).

16. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A and/or IEC61340-5*.

17. Packing information

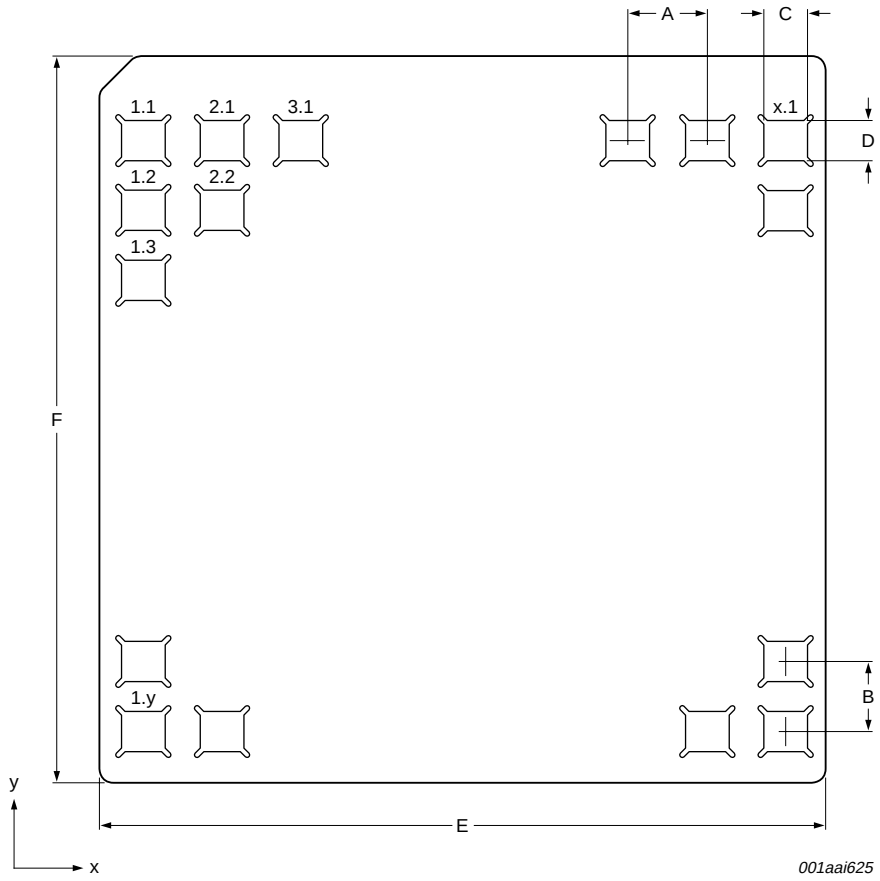


Fig 26. Tray details for PCF8534AU/DA/1

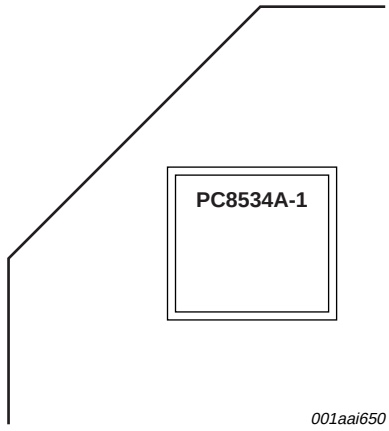


Fig 27. Tray alignment for PCF8534AU/DA/1

Table 22. Tray dimensions

Symbol	Description	Value
A	pocket pitch in x direction	5.5 mm
B	pocket pitch in y direction	4.9 mm
C	pocket width in x direction	3.08 mm
D	pocket width in y direction	2.79 mm
E	tray width in x direction	50.8 mm
F	tray width in y direction	50.8 mm
N	number of pockets, x direction	8
M	number of pockets, y direction	9

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages

- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 28) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 23 and 24

Table 23. SnPb eutectic process (from J-STD-020C)

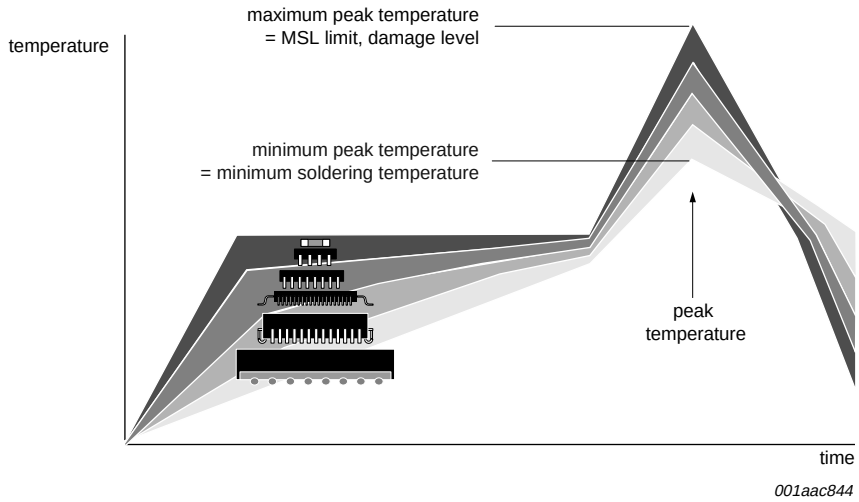
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 24. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 28.



MSL: Moisture Sensitivity Level

Fig 28. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Abbreviations

Table 25. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
IC	Integrated Circuit
LCD	Liquid Crystal Display
MM	Machine Model
RAM	Random Access Memory

20. Revision history

Table 26. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8534A_3	20081110	Product data sheet	-	PCF8534A_2
Modifications:	• Added bare die product and document sections			
PCF8534A_2	20080604	Product data sheet	-	PCF8534A_1
Modifications:	• Changes in Section 7.10 on page 14 and Section 7.12 on page 17. • Added Caution to Section 10 on page 26. • Changed Figure 22 on page 32.			
PCF8534A_1	20080423	Product data sheet	-	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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