PCF2127A

Integrated RTC, TCXO and quartz crystal

Rev. 01 — 21 January 2010 Product data sheet

1. General description

The PCF2127A is a CMOS[1] real time clock and calendar with an integrated Temperature Compensated Crystal Oscillator (TCXO) and a 32.768 kHz quartz crystal optimized for very high accuracy and very low power consumption. The PCF2127A has 512 bytes of general purpose static RAM, a selectable I^2C-bus or SPI-bus, a backup battery switch-over circuit, a programmable watchdog function, a timestamp function, and many other features.

2. Features

- Temperature Compensated Crystal Oscillator (TCXO) with integrated capacitors
- Typical accuracy: ±3 ppm from –15 °C to +60 °C
- Integration of a 32.768 kHz quartz crystal and oscillator in the same package
- Provides year, month, day, weekday, hours, minutes, and seconds
- 512 bytes of general purpose static RAM
- Timestamp function
  - with interrupt capability
  - detection of two different events on one multilevel input pin (e.g. for tamper detection)
- Two line bidirectional 1 MHz Fast-mode Plus (Fm+) I^2C-bus interface (I_{OL} = 20 mA at pin SDA)
- 3 line SPI-bus with separate data input and output (maximum speed 6.5 Mbit/s)
- Battery backup input pin and switch-over circuitry
- Battery backed output voltage pin
- Battery low detection function
- Extra power fail detection function with input and output pins
- Power-On Reset Override (PORO)
- Oscillator stop detection function
- Interrupt output and system reset pin (open-drain)
- Programmable 1 second or 1 minute interrupt
- Programmable countdown timer with interrupt capability
- Programmable watchdog timer with interrupt and reset capability
- Programmable alarm function with interrupt capability
- Programmable square wave open-drain output pin
- Clock operating voltage: 1.2 V to 4.2 V
- Low supply current: typical 0.65 μA at V_{DD} = 3.0 V and T_{amb} = 25 °C

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 17.

founded by Philips

- Automatic leap year correction

3. Applications

- Electronic metering for electricity, water, and gas
- Timekeeping instruments with high precision
- GPS equipment to reduce time to first fix
- Applications that require an accurate process timing
- Products with long automated unattended operation time

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF2127AT/1	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

5. Marking

Table 2. Marking codes

Type number	Marking code
PCF2127AT/1	PCF2127AT

6. Block diagram

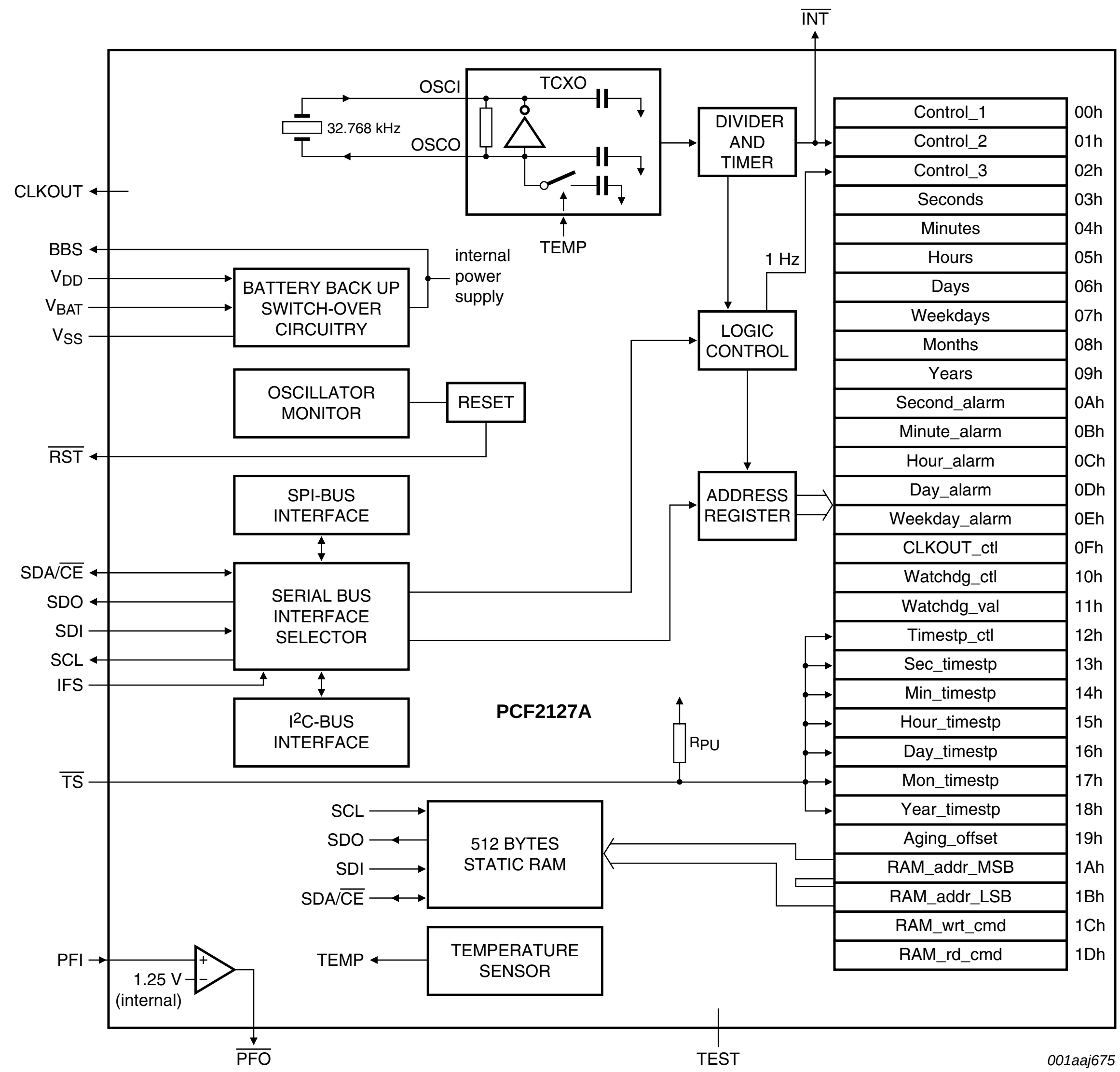
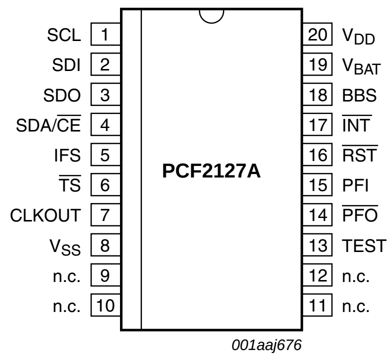


Fig 1. Block diagram of PCF2127A

7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 52.

Fig 2. Pin configuration for PCF2127A (SO20)

7.2 Pin description

Table 3. Pin description of PCF2127A

Symbol	Pin	Description
SCL	1	combined serial clock input for both I²C-bus and SPI-bus; may float when $\overline{\text{CE}}$ inactive
SDI	2	serial data input for SPI-bus; may float when $\overline{\text{CE}}$ inactive
SDO	3	serial data output for SPI-bus, push-pull
SDA/$\overline{\text{CE}}$	4	combined serial data input and output for the I²C interface and chip enable input (active LOW) for the SPI-bus
IFS	5	interface selector input connect to pin V_{SS} to select the SPI-bus connect to pin BBS to select the I²C interface
$\overline{\text{TS}}$	6	timestamp input (active LOW) with 200 kΩ internal pull-up resistor (R_{PU})
CLKOUT	7	clock output (open-drain)
V_{SS}	8	ground supply voltage
n.c.	9 to 12	do not connect; do not use as feed through
TEST	13	do not connect; do not use as feed through
$\overline{\text{PFO}}$	14	power fail output (open-drain; active LOW)
PFI	15	power fail input
$\overline{\text{RST}}$	16	reset output (open-drain; active LOW)
$\overline{\text{INT}}$	17	interrupt output (open-drain; active LOW)
BBS	18	output voltage (battery backed)
V_{BAT}	19	battery supply voltage (backup)
V_{DD}	20	supply voltage

8. Functional description

The PCF2127A is a Real Time Clock (RTC) and calendar with an on-chip Temperature Compensated Crystal Oscillator (TCXO) and a 32.768 kHz quartz crystal integrated into the same package.

Address and data are transferred by a selectable 1 MHz Fast-mode Plus (Fm+) I^2C-bus or a 3 line SPI-bus with separate data input and output (see Section 9). The maximum speed of the SPI-bus is 6.5 Mbit/s.

The PCF2127A contains 30 8-bit registers, that are used for many different functions, such as clock, alarm, watchdog, timer, timestamp etc. (see Section 8.1).

The PCF2127A has an output reset pin: the output reset is activated on Power-On Reset (POR), and whenever the oscillator is stopped (see Section 8.7).

The PCF2127A features 512 bytes of general purpose static RAM, which is battery backed and can be used independent of the RTC functionality (see Section 8.5).

The PCF2127A has a backup battery input pin and backup battery switch-over circuit which monitors the main power supply and automatically switches to the backup battery when a power failure condition is detected (see Section 8.6.1). Accurate timekeeping is maintained even when the main power supply is interrupted.

A battery low detection circuit monitors the status of the battery (see Section 8.6.3). When the battery voltage goes below a certain threshold value, a flag is set to indicate that the battery must be replaced. This can be used to ensure the integrity of the data during periods of battery backup.

A power failure detection circuit monitors the voltage of the power fail input pin PFI. When the voltage on the power fail input pin PFI goes below an internal reference (1.25 V), the power fail output pin $\overline{\text{PFO}}$ is activated (see Section 8.6.4).

8.1 Register overview

The PCF2127A contains 30 8-bit registers (see Table 4) with an auto-incrementing address register: the register address will be incremented automatically after each read or write data byte up to the register 1Bh. After register 1Bh the auto-incrementing will wrap around to address 00h. The registers 1Ch and 1Dh must be addressed directly (see Figure 3).

- The first three registers (memory address 00h, 01h, and 02h) are used as control registers (see Section 8.2).
- The memory addresses 03h through to 09h are used as counters for the clock function (seconds up to years). The date is automatically adjusted for months with fewer than 31 days, including corrections for leap years. The clock can operate in 12-hour mode with an AM/PM indication or in 24-hour mode (see Section 8.9).
- Addresses 0Ah through 0Eh define the alarm function. It can be selected that an interrupt is generated when an alarm event occurs (see Section 8.10).

- The register 0Fh defines the temperature measurement period and the clock out mode. The temperature measurement period can be selected from every 4 minutes (default) down to every 30 seconds (see Table 9). CLKOUT frequencies of 32.768 kHz (default) down to 1 Hz for use as a system clock, a microcontroller clock etc. can be chosen (see Section 8.3.2).
- Address registers 10h and 11h are used for the watchdog and countdown timer functions. The timer has four selectable source clocks allowing for timer periods from less than 1 ms to greater than 4 hours. Either the watchdog timer **or** the countdown timer can be enabled (see Section 8.11). For the watchdog timer it is possible to select whether an interrupt or a pulse on the reset pin will be generated when the watchdog times out. For the countdown timer it is only possible that an interrupt will be generated at the end of the countdown.
- Address registers 12h to 18h are used for the timestamp function. When the trigger-event happens the actual time is saved in the timestamp registers (see Section 8.12).
- Address register 19h is used for the correction of the crystal aging effect (see Section 8.4.1).
- Address registers 1Ah and 1Bh define the RAM address. Address register 1Ch (RAM_wrt_cmd) is the RAM write command; address register 1Dh (RAM_rd_cmd) is the RAM read command. Data is transferred to or from the RAM via the serial interface (see Section 8.5).
- The registers Seconds, Minutes, Hours, Days, Months, and Years are all coded in Binary Coded Decimal (BCD) format to simplify application use. Other registers are either bit-wise or standard binary.

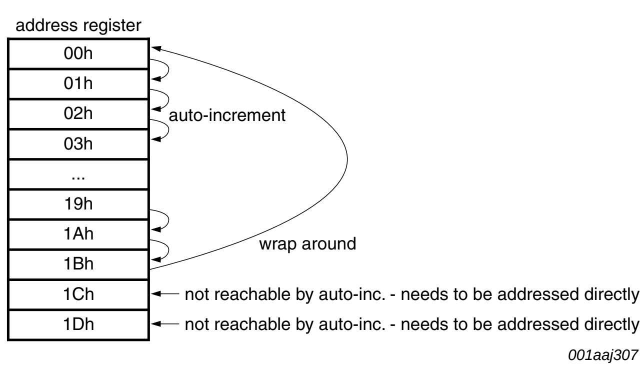


Fig 3. Handling address registers

When one of the RTC registers is written or read, the content of all counters is temporarily frozen. This prevents a faulty writing or reading of the clock and calendar during a carry condition (see Section 8.9.8).

Table 4. Register overview

Bit positions labelled as - are not implemented and will return a 0 when read. Bit T must always be written with logic 0. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value
		7	6	5	4	3	2	1	0	
Control registers										
00h	Control_1	EXT_ TEST	T	STOP	TSF1	POR_ OVRD	12_24	MI	SI	0000 0000
01h	Control_2	MSF	WDTF	TSF2	AF	CDTF	TSIE	AIE	CDTIE	0000 0000
02h	Control_3	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE	0000 0000
Time and date registers										
03h	Seconds	OSF	SECONDS (0 to 59)							1XXX XXXX
04h	Minutes	-	MINUTES (0 to 59)							- XXX XXXX
05h	Hours	-	-	AMPM	HOURS (1 to 12) in 12 h mode					- - XX XXXX
				HOURS (0 to 23) in 24 h mode						- - XX XXXX
06h	Days	-	-	DAYS (1 to 31)						- - XX XXXX
07h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)			- - - - - XXX
08h	Months	-	-	-	MONTHS (1 to 12)					- - - X XXXX
09h	Years	YEARS (0 to 99)								XXXX XXXX
Alarm registers										
0Ah	Second_alarm	AEN_S	SECOND_ALARM (0 to 59)							1XXX XXXX
0Bh	Minute_alarm	AEN_M	MINUTE_ALARM (0 to 59)							1XXX XXXX
0Ch	Hour_alarm	AEN_H	-	AMPM	HOUR_ALARM (1 to 12) in 12 h mode					1 - XX XXXX
			-	HOUR_ALARM (0 to 23) in 24 h mode						1 - XX XXXX
0Dh	Day_alarm	AEN_D	-	DAY_ALARM (1 to 31)						1 - XX XXXX
0Eh	Weekday_alarm	AEN_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)			1 - - - - XXX
CLKOUT control register										
0Fh	CLKOUT_ctl	TCR[1:0]		-	-	-	COF[2:0]			00 - - - 000
Watchdog registers										
10h	Watchdg_tim_ctl	WD_CD[1:0]		TI_TP	-	-	-	TF[1:0]		000 - - - 11
11h	Watchdg_tim_val	WATCHDG_TIM_VAL[7:0]								XXXX XXXX
Timestamp registers										
12h	Timestp_ctl	TSM	TSOFF	-	1_O_16_TIMESTP[4:0]					00 - X XXXX
13h	Sec_timestp	-	SECOND_TIMESTP (0 to 59)							- XXX XXXX
14h	Min_timestp	-	MINUTE_TIMESTP (0 to 59)							- XXX XXXX
15h	Hour_timestp	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12 h mode					- - XX XXXX
				HOUR_TIMESTP (0 to 23) in 24 h mode						- - XX XXXX
16h	Day_timestp	-	-	DAY_TIMESTP (1 to 31)						- - XX XXXX
17h	Mon_timestp	-	-	-	MONTH_TIMESTP (1 to 12)					- - - X XXXX
18h	Year_timestp	YEAR_TIMESTP (0 to 99)								XXXX XXXX
Crystal aging register										
19h	Aging_offset	-	-	-	-	AO[3:0]				- - - - 1000

Table 4. Register overview *…continued*

Bit positions labelled as - are not implemented and will return a 0 when read. Bit T must always be written with logic 0. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit								Reset value
		7	6	5	4	3	2	1	0	
RAM registers										
1Ah	RAM_addr_MSB	-	-	-	-	-	-	-	RA8	- - - - - - - 0
1Bh	RAM_addr_LSB	RA[7:0]								0000 0000
1Ch	RAM_wrt_cmd	X	X	X	X	X	X	X	X	XXXX XXXX
1Dh	RAM_rd_cmd	X	X	X	X	X	X	X	X	XXXX XXXX

8.2 Control registers

PCF2127A has 30 8-bit registers. The first 3 registers with the addresses 00h, 01h and 02h are used as control registers.

8.2.1 Register Control_1

Table 5. Control_1 - control and status register 1 (address 00h) bit description

Bit	Symbol	Value	Description	Reference
7	EXT_TEST	0 [1]	normal mode	Section 8.14
		1	external clock test mode	
6	T	0 [2]	unused	
5	STOP	0 [1]	RTC source clock runs	Section 8.15
		1	RTC clock is stopped; RTC divider chain flip-flops are asynchronously set logic 0; CLKOUT at 32.768 kHz, 16.384 kHz, or 8.192 kHz is still available	
4	TSF1	0 [1]	no timestamp interrupt generated	Section 8.12.1
		1	flag set when $\overline{TS}$ input is driven to an intermediate level between power supply and ground; flag must be cleared to clear interrupt	
3	POR_OVRD	0 [1]	Power-On Reset Override (PORO) facility disabled; **set logic 0 for normal operation**	Section 8.7.2
		1	PORO enabled	
2	12_24	0 [1]	24 hour mode selected	Table 22
		1	12 hour mode selected	
1	MI	0 [1]	minute interrupt disabled	Section 8.13.1
		1	minute interrupt enabled	
0	SI	0 [1]	second interrupt disabled	
		1	second interrupt enabled	

[1] Default value.

[2] When writing to the register this bit has always to be set logic 0.

8.2.2 Register Control_2

Table 6. Control_2 - control and status register 2 (address 01h) bit description

Bit	Symbol	Value		Description	Reference
7	MSF	0	[1]	no minute or second interrupt generated	Section 8.13
		1		flag set when minute or second interrupt generated; flag must be cleared to clear interrupt	
6	WDTF	0	[1]	no watchdog timer interrupt or reset generated	Section 8.13.3
		1		flag set when watchdog timer interrupt or reset generated; flag cannot be cleared by using the interface (read-only)	
5	TSF2	0	[1]	no timestamp interrupt generated	Section 8.12.1
		1		flag set when $\overline{TS}$ input is driven to ground; flag must be cleared to clear interrupt	
4	AF	0	[1]	no alarm interrupt generated	Section 8.10.6
		1		flag set when alarm triggered; flag must be cleared to clear interrupt	
3	CDTF	0	[1]	no countdown timer interrupt generated	Section 8.11.6
		1		flag set when countdown timer interrupt generated; flag must be cleared to clear interrupt	
2	TSIE	0	[1]	no interrupt generated from timestamp flag	Section 8.13.5
		1		interrupt generated when timestamp flag set	
1	AIE	0	[1]	no interrupt generated from the alarm flag	Section 8.13.4
		1		interrupt generated when alarm flag set	
0	CDTIE	0	[1]	no interrupt generated from countdown timer flag	Section 8.13.1.2
		1		interrupt generated when countdown timer flag set	

[1] Default value.

8.2.3 Register Control_3

Table 7. Control_3 - control and status register 3 (address 0Fh) bit description

Bit	Symbol	Value	Description	Reference
7 to 5	PWRMNG[2:0]	[1]	control of the battery switch-over, battery low detection, and extra power fail detection functions	Section 8.6
4	BTSE	0 [2]	no timestamp when battery switch-over occurs	Section 8.12.4
		1	time-stamped when battery switch-over occurs	
3	BF	0 [2]	no battery switch-over interrupt generated	Section 8.6.1
		1	flag set when battery switch-over occurs; flag must be cleared to clear interrupt	
2	BLF	0 [2]	battery status ok; no battery low interrupt generated	Section 8.6.3
		1	battery status low; flag cannot be cleared using the interface	
1	BIE	0 [2]	no interrupt generated from the battery flag (BF)	Section 8.13.6
		1	interrupt generated when BF is set	
0	BLIE	0 [2]	no interrupt generated from battery low flag (BLF)	Section 8.13.7
		1	interrupt generated when BLF is set	

[1] Values see Table 17.

[2] Default value.

8.3 Register CLKOUT_ctl

Table 8. CLKOUT_ctl - CLKOUT control register (address 03h) bit description

Bit	Symbol	Value	Description
7 to 6	TCR[1:0]	see Table 9	temperature measurement period
5 to 3	-	-	unused
2 to 0	COF[2:0]	see Table 10	CLKOUT frequency selection

8.3.1 Temperature compensated crystal oscillator

The frequency of tuning fork quartz crystal oscillators are temperature-dependent. In the PCF2127A the frequency drift caused by temperature variation is corrected by adjusting the load capacitance of the crystal oscillator.

The load capacitance is changed by switching between two load capacitance values using a modulation signal with a programmable duty cycle. Every chip is calibrated in order to produce, at the measured temperature, the correct duty cycle which compensates for the frequency drift.

The frequency accuracy can be evaluated by measuring the frequency of the square wave signal available at the output pin CLKOUT. However, the selection of f_{CLKOUT} = 32 kHz (default value) leads to inaccurate measurements. The most accurate frequency measurement occurs when f_{CLKOUT} = 1 Hz is selected (see Table 10).

8.3.1.1 Temperature measurement

The PCF2127A has a temperature sensor circuit used to perform the temperature compensation of the frequency. The temperature is measured immediately after power-on and then periodically with a period set by the temperature conversion rate TCR[1:0] in the register CLKOUT_ctl.

Table 9. Temperature measurement period

TCR[1:0]		Temperature measurement period
00	[1]	4 min
01		2 min
10		1 min
11		30 seconds

[1] Default value.

8.3.2 Clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF control bits in register CLKOUT_ctl. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

CLKOUT is an open-drain output and enabled at power-on. When disabled, the output is high-impedance.

The duty cycle of the selected clock is not controlled, however, due to the nature of the clock generation, all but the 32.768 kHz frequencies will be 50 : 50.

Table 10. CLKOUT frequency selection

COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1]
000	32768	60 : 40 to 40 : 60
001	16384	50 : 50
010	8192	50 : 50
011	4096	50 : 50
100	2048	50 : 50
101	1024	50 : 50
110	1	50 : 50
111	CLKOUT = high-Z	-

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

8.4 Register Aging_offset

Table 11. Aging_offset - crystal aging offset register (address 19h) bit description

Bit	Symbol	Value	Description
7 to 4	-	-	unused
3 to 0	AO[3:0]	see Table 12	aging offset value

8.4.1 Crystal aging correction

The PCF2127A has an aging offset register Aging_offset to correct the crystal aging effects[2].

The accuracy of the frequency of a quartz crystal depends on the aging. Crystal suppliers usually specify the first year aging (typically ±1 ppm, maximum ±3 ppm) and/or the 10 years aging (typically ±5 ppm). The aging offset adds an offset, positive or negative, in the temperature compensation circuits which allows to correct the aging effect.

The change in ppm per AO[3:0] value is different at different temperatures. At 25 °C, the aging offset bits allow a frequency correction of typically 1 ppm per AO[3:0] value, from –7 ppm to +8 ppm.

Table 12. Frequency correction at 25 °C, typical

AO[3:0]		ppm
Decimal	Binary	
0	0000	+8
1	0001	+7
2	0010	+6
3	0011	+5
4	0100	+4
5	0101	+3
6	0110	+2
7	0111	+1
8	1000 [1]	0
9	1001	–1
10	1010	–2
11	1011	–3
12	1100	–4
13	1101	–5
14	1110	–6
15	1111	–7

[1] Default value.

2. For further information please refer to the application note Ref. 3 “AN10857”.

8.5 General purpose 512 bytes static RAM

The PCF2127A contains a general purpose 512 bytes static RAM. This integrated SRAM is battery backed and can therefore be used to store data which is essential for the application to survive a power outage.

9 bits, RA[8:0], define the RAM address pointer in registers RAM_addr_MSB and RAM_addr_LSB. The register address pointer increments after each read or write automatically up to 1Bh and then wraps around to address 00h (see Figure 3).

Data is transferred to or from the RAM via the interface. To write to the RAM, the register RAM_wrt_cmd, to read from the RAM the register RAM_rd_cmd must be addressed explicitly.

8.5.1 Register RAM_addr_MSB

Table 13. RAM_addr_MSB - RAM address MSB register (address 1Ah) bit description

Bit	Symbol	Description
7 to 1	-	unused
1	RA8	RAM address, MSB (9th bit)

8.5.2 Register RAM_addr_LSB

Table 14. RAM_addr_LSB - RAM address LSB register (address 1Bh) bit description

Bit	Symbol	Description
7 to 0	RA[7:0]	RAM address, LSB (1st to 8th bit)

8.5.3 Register RAM_wrt_cmd

Table 15. RAM_wrt_cmd - RAM write command register (address 1Ch) bit description

Bit	Symbol	Description
7 to 0	RA[7:0]	data to be written into RAM

8.5.4 Register RAM_rd_cmd

Table 16. RAM_rd_cmd - RAM read command register (address 1Dh) bit description

Bit	Symbol	Description
7 to 0	RA[7:0]	data to be read from RAM

8.5.5 Operation examples

8.5.5.1 Writing to the RAM

1. Set RAM address:
   - Select register RAM_addr_MSB (send address 1Ah).
   - Set value for bit RA8 (data byte of register 1Ah);
     note: register address will be incremented automatically to 1Bh.
   - Set value for array RA[7:0] (data byte of register 1Bh).
2. Send RAM write command:
   - Select register RAM_wrt_cmd (send address 1Ch).

3. Write data into the RAM:
   – Write n data byte into RAM.

For details see Figure 44.

8.5.5.2 Reading from the RAM

1. Set RAM address:
   – Select register RAM_addr_MSB (send address 1Ah).
   – Set value for bit RA8 (data byte of register 1Ah);
     note: register address will be incremented automatically to 1Bh.
   – Set value for array RA[7:0] (data byte of register 1Bh).
2. Send RAM read command:
   – Select register RAM_rd_cmd (send address 1Dh).
3. Read from the RAM:
   – Read n data byte from the RAM.

For details see Figure 45.

8.6 Power management functions

The PCF2127A has two power supply pins and one power output pin:

- V_{DD} - the main power supply input pin
- V_{BAT} - the battery backup input pin
- BBS - battery backed output voltage pin (equal to the internal power supply)

The PCF2127A has three power management functions implemented:

- Battery switch-over function
- Battery low detection function
- Extra power fail detection function

The power management functions are controlled by the control bits PWRMNG[2:0] in register Control_3:

Table 17. Power management control bit description

PWRMNG[2:0]	Function
000 [1]	battery switch-over function is enabled in standard mode; battery low detection function is enabled; extra power fail detection function is enabled
001	battery switch-over function is enabled in standard mode; battery low detection function is disabled; extra power fail detection function is enabled
010	battery switch-over function is enabled in standard mode; battery low detection function is disabled; extra power fail detection function is disabled

Table 17. Power management control bit description *…continued*

PWRMNG[2:0]		Function
011		battery switch-over function is enabled in direct switching mode; battery low detection function is enabled; extra power fail detection function is enabled
100		battery switch-over function is enabled in direct switching mode; battery low detection function is disabled; extra power fail detection function is enabled
101		battery switch-over function is enabled in direct switching mode; battery low detection function is disabled; extra power fail detection function is disabled
110	[2]	battery switch-over function is disabled - only one power supply (V_{DD}); battery low detection function is disabled; extra power fail detection function is enabled
111	[2]	battery switch-over function is disabled - only one power supply (V_{DD}); battery low detection function is disabled; extra power fail detection function is disabled

[1] Default value.

[2] When the battery switch-over function is disabled, the PCF2127A works only with the power supply V_{DD}; V_{BAT} must be put to ground and the battery low detection function is disabled.

8.6.1 Battery switch-over function

The PCF2127A has a backup battery switch-over circuit which monitors the main power supply V_{DD} and automatically switches to the backup battery when a power failure condition is detected.

One of two operation modes can be selected:

- **Standard mode:** the power failure condition happens when:
  $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$
  $V_{th(sw)bat}$ is the battery switch threshold voltage. Typical value is 2.5 V.
- **Direct switching mode:** the power failure condition happens when $V_{DD} < V_{BAT}$. Direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below $V_{th(sw)bat}$

When a power failure condition occurs and the power supply switches to the battery the following sequence occurs:

1. The battery switch flag BF (register Control_3) is set logic 1.
2. An interrupt is generated if the control bit BIE (register Control_3) is enabled (see Section 8.13.6).
3. If the control bit BTSE (register Control_3) is logic 1, the timestamp registers store the time and date when the battery switch occurred (see Section 8.12.4).
4. The battery switch flag BF is cleared via the interface; it must be cleared to clear the interrupt.

The interface is disabled in battery backup operation:

- Interface inputs are not recognized, preventing extraneous data being written to the device

- Interface outputs are high-impedance

8.6.1.1 Standard mode

If $V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$ the internal power supply is V_{DD}.

If $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$ the internal power supply is V_{BAT}.

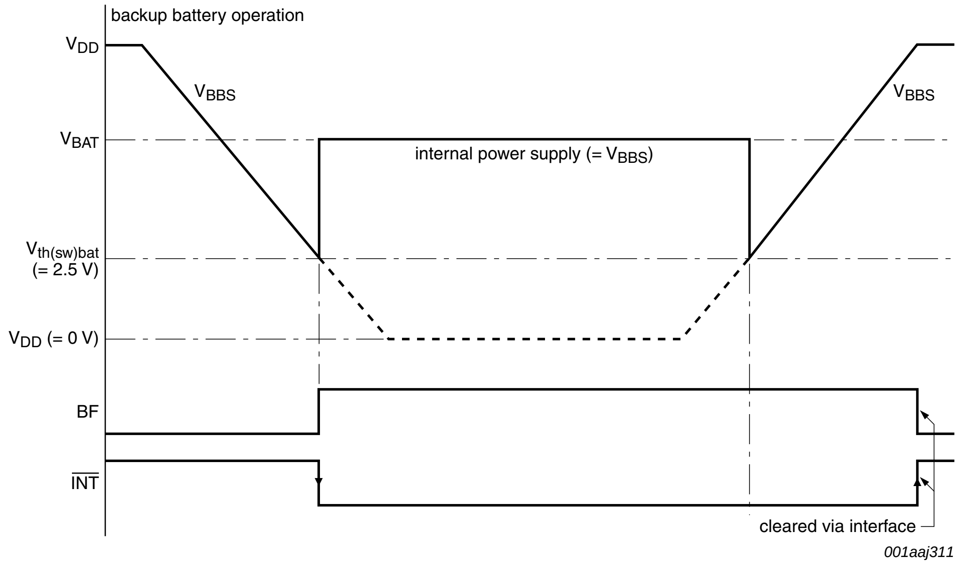


Fig 4. Battery switch-over behavior in standard mode with bit BIE logic 1 (enabled)

8.6.1.2 Direct switching mode

If $V_{DD} > V_{BAT}$ the internal power supply is V_{DD}.

If $V_{DD} < V_{BAT}$ the internal power supply is V_{BAT}.

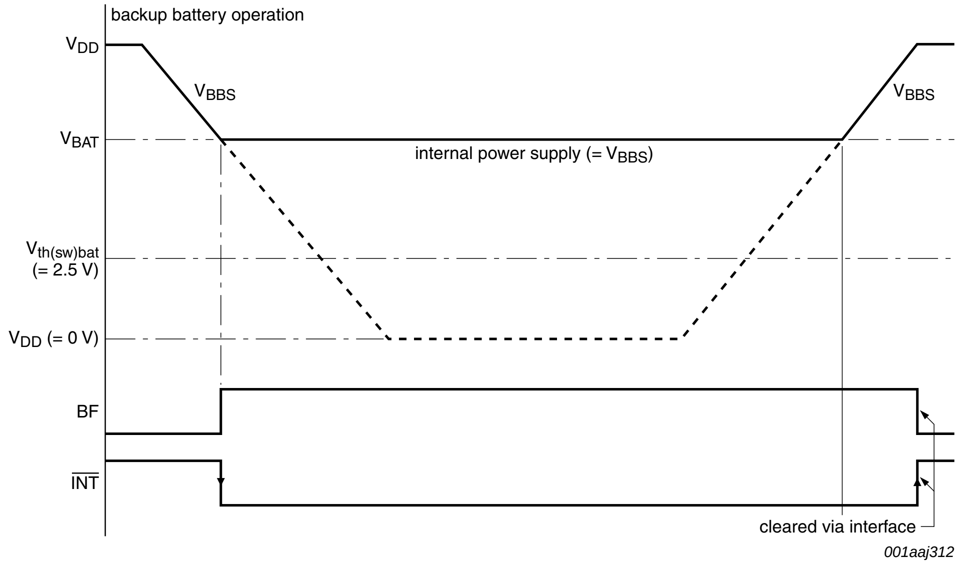


Fig 5. Battery switch-over behavior in direct switching mode with bit BIE logic 1 (enabled)

The direct switching mode is useful in systems where V_{DD} is higher than V_{BAT} at all times. The direct switching mode is not recommended if the V_{DD} and V_{BAT} values are similar (e.g. V_{DD} = 3.3 V, $V_{BAT} \geq$ 3.0 V). In direct switching mode the power consumption is reduced compared to the standard mode because the monitoring of V_{DD} and $V_{th(sw)bat}$ is not performed.

8.6.1.3 Battery switch-over disabled: only one power supply (V_{DD})

When the battery switch-over function is disabled:

- The power supply is applied on the V_{DD} pin
- The V_{BAT} pin must be connected to ground
- The internal power supply, available at the output pin BBS, is equal to V_{DD}
- The battery flag (BF) is always logic 0

8.6.1.4 Battery switch-over architecture

The architecture of the battery switch-over circuit is shown in Figure 6.

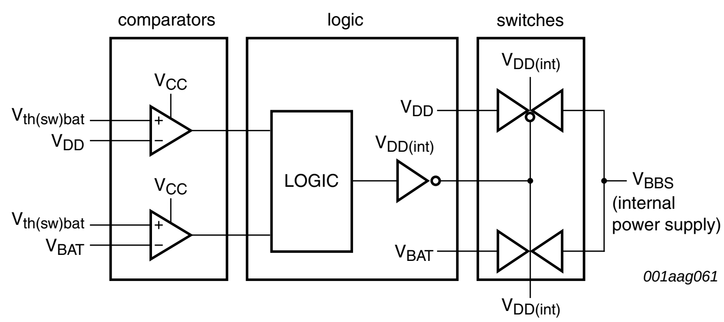


Fig 6. Battery switch-over circuit, simplified block diagram

The internal power supply (available on pin BBS) is equal to V_{DD} or V_{BAT}. It has to be assured that there are decoupling capacitors on the pins V_{DD}, V_{BAT}, and BBS.

8.6.2 Battery backup supply

The V_{BBS} voltage on the output pin BBS is equal to the internal power supply and depends on the selected battery switch-over function mode:

Table 18. Output pin BBS

Battery switch-over function mode	Conditions	V_{BBS} equals
standard	$V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$	V_{DD}
	$V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$	V_{BAT}
direct switching	$V_{DD} > V_{BAT}$	V_{DD}
	$V_{DD} < V_{BAT}$	V_{BAT}
disabled	only V_{DD} available, V_{BAT} must be put to ground	V_{DD}

The output pin BBS can be used as a supply for external devices with battery backup needs (see Ref. 3 “AN10857”). For this case, Figure 7 shows the typical driving capability when V_{BBS} is driven from V_{DD}.

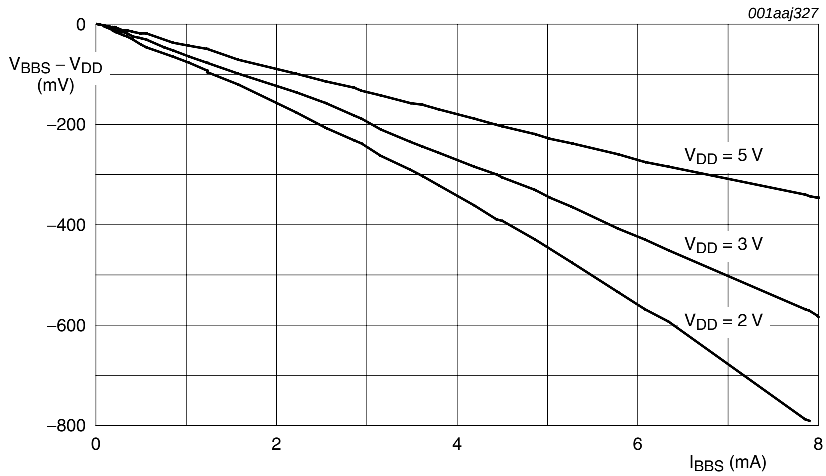


Fig 7. Typical driving capability of V_{BBS}: ($V_{BBS} - V_{DD}$) with respect to the output load current I_{BBS}

8.6.3 Battery low detection function

The PCF2127A has a battery low detection circuit which monitors the status of the battery V_{BAT}.

When V_{BAT} drops below the threshold value $V_{th(bat)low}$ (typically 2.5 V) the BLF flag (register Control_3) is set to indicate that the battery is low and that it must be replaced. Monitoring of the battery voltage also occurs during battery operation.

An unreliable battery can not prevent that the supply voltage drops below V_{low} (typical 1.2 V) and therewith the data integrity gets lost.

When V_{BAT} drops below the threshold value $V_{th(bat)low}$, the following sequence occurs (see Figure 8):

1. The battery low flag BLF is set logic 1.
2. An interrupt is generated if the control bit BLIE (register Control_3) is enabled (see Section 8.13.7).
3. The flag BLF remains logic 1 until the battery is replaced. BLF cannot be cleared using the interface. It is cleared automatically by the battery low detection circuit when the battery is replaced.

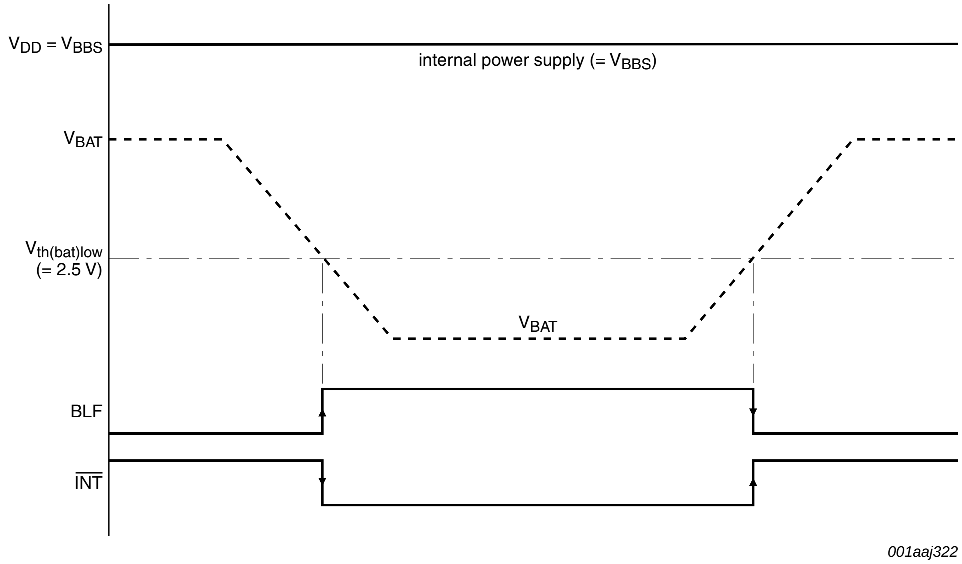


Fig 8. Battery low detection behavior with bit BLIE logic 1 (enabled)

8.6.4 Extra power fail detection function

The PCF2127A has an extra power fail detection circuit which compares the voltage at the power fail input pin (PFI) to an internal reference voltage equal to 1.25 V.

If V_{PFI} < 1.25 V the power fail output $\overline{PFO}$ is driven LOW. $\overline{PFO}$ is an open-drain, active LOW output which requires an external pull-up resistor in any application.

The extra power fail detection function is typically used as a low voltage detection for the main power supply V_{DD} (see Figure 9).

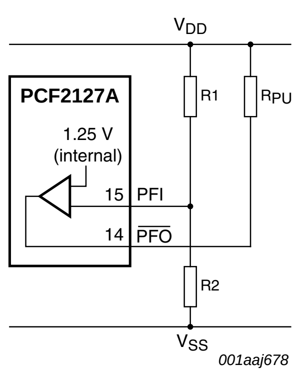


Fig 9. Typical application of the extra power fail detection function

Usually R1 and R2 should be chosen such that the voltage at pin PFI

- is higher than 1.25 V at start-up
- falls below 1.25 V when V_{DD} falls below a desired threshold voltage, $V_{th(uvp)}$, defined by Equation 1:

$$V_{th(uvp)} = \left(\frac{R_1}{R_2} + 1\right) \times 1.25V \quad (1)$$

$V_{th(uvp)}$ value is usually set to a value that there are several milliseconds before V_{DD} falls below the minimum operating voltage of the system, in order to allow the microcontroller to perform early backup operations.

If the extra power fail detection function is not used, pin PFI must be connected to V_{SS} and pin $\overline{PFO}$ must be left open circuit.

8.6.4.1 Extra power fail detection when the battery switch over function is enabled

- When the power switches to the backup battery supply V_{BAT}, the power fail comparator is switched off and the power fail output at pin $\overline{PFO}$ goes (or remains) LOW
- When the power switches back to the main V_{DD}, the pin $\overline{PFO}$ is not driven LOW anymore and is pulled HIGH through the external pull-up resistance for a certain time (t_{rec} = 15.63 ms to 31.25 ms) and then the power fail comparator is enabled again

For illustration see Figure 10 and Figure 11.

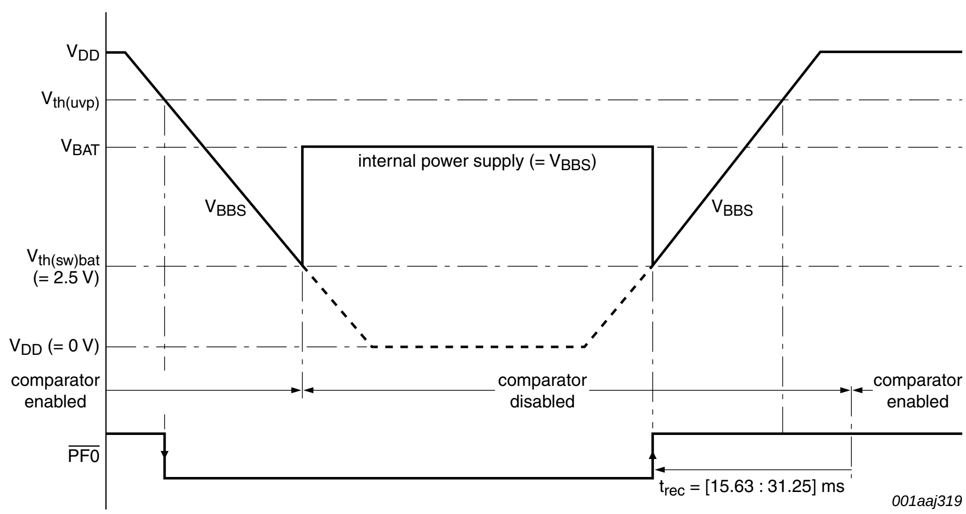


Fig 10. $\overline{PFO}$ signal behavior when battery switch-over is enabled in standard mode and $V_{th(uvp)} > (V_{BAT}, V_{th(sw)bat})$

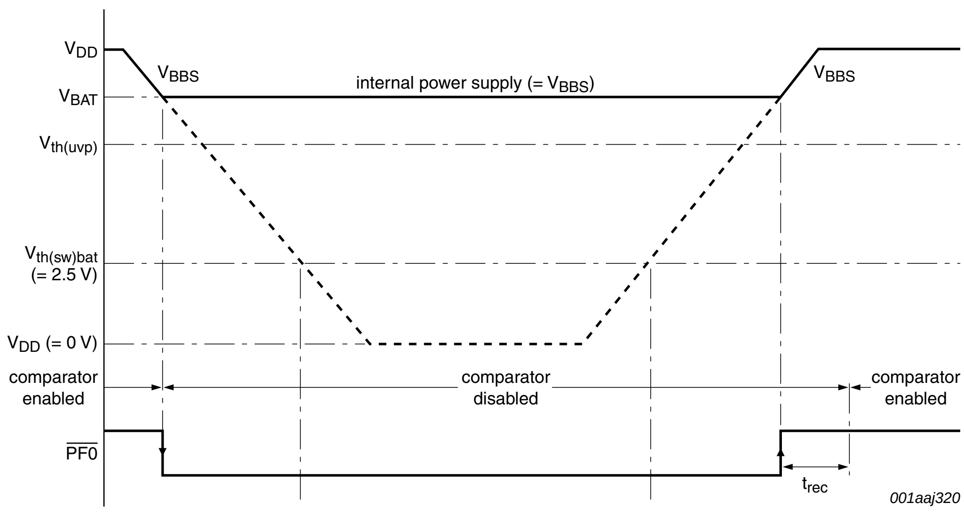


Fig 11. PFO signal behavior when battery switch-over is enabled in direct switching mode and $V_{th(uvp)} < V_{BAT}$

8.6.4.2 Extra power fail detection when the battery switch-over function is disabled

If the battery switch-over function is disabled and the power fail comparator is enabled, the power fail output at pin PFO depends only on the results of the comparison between V_{PFI} and 1.25 V:

- If V_{PFI} > 1.25 V, PFO = HIGH (through the external pull-up resistor)
- If V_{PFI} < 1.25 V, PFO = LOW

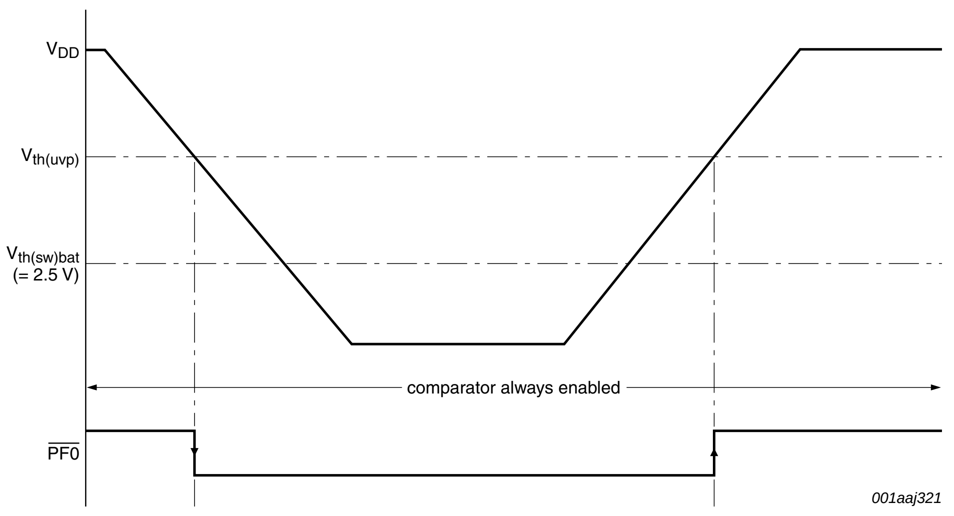


Fig 12. PFO signal behavior when battery switch-over is disabled

8.7 Reset function

The PCF2127A has an active LOW open-drain output reset pin ($\overline{RST}$). The reset output is activated at Power-On Reset (POR) and whenever the oscillator is stopped (see Section 8.8).

8.7.1 Power-On Reset (POR)

The POR is active whenever the oscillator is stopped. The oscillator is also considered to be stopped during the time between power-on and stable crystal resonance (see Figure 13). This time may be in the range of 200 ms to 2 s depending on temperature and supply voltage. Whenever an internal reset occurs, the oscillator stop flag is set (OSF set logic 1).

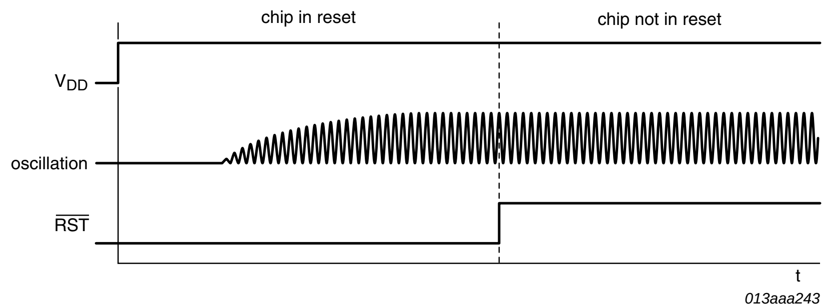


Fig 13. Power-On Reset (POR)

After POR, the following mode is entered:

- 32.768 kHz CLKOUT active
- Power-On Reset Override (PORO) available to be set
- 24 hour mode is selected
- Battery switch-over is enabled
- Battery low detection is enabled
- Extra power fail detection is enabled

The register values after power-on are shown in Table 4.

8.7.2 Power-On Reset Override (PORO)

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on-board test of the device.

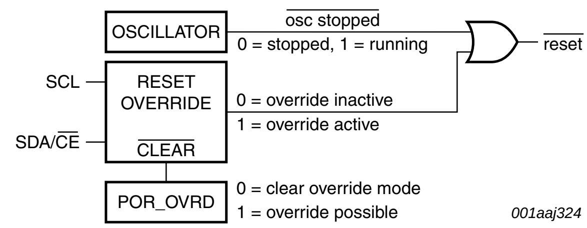


Fig 14. Power-On Reset (POR) system

The setting of the PORO mode requires that POR_OVRD in register Control_1 is set logic 1 and that the signals at the interface pins SDA/CE and SCL are toggled as illustrated in Figure 15. All timings shown are required minimums.

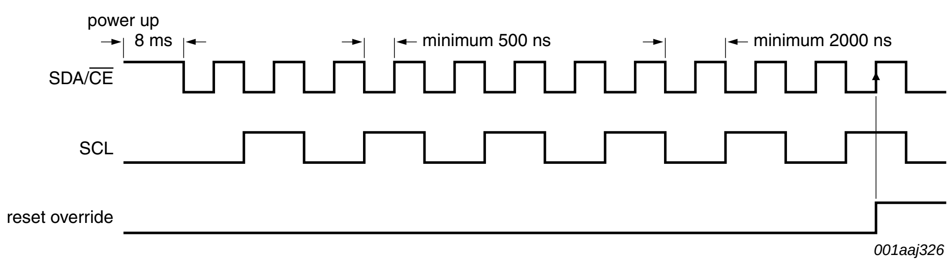


Fig 15. Power-On Reset Override (PORO) sequence, valid for both I^{2}C-bus and SPI-bus

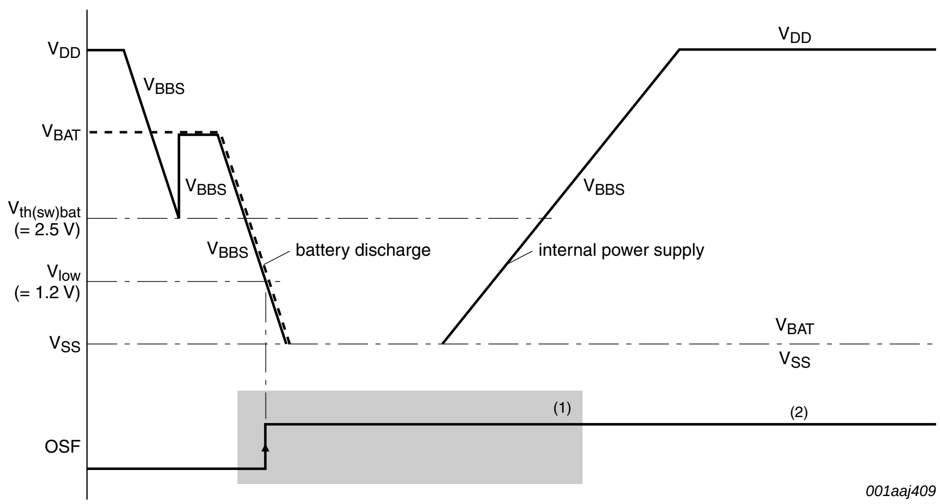
Once the override mode is entered, the device is immediately released from the reset state and the set-up operation can commence.

The PORO mode is cleared by writing logic 0 to POR_OVRD. POR_OVRD must be logic 1 before a re-entry into the override mode is possible. Setting POR_OVRD logic 0 during normal operation has no effect except to prevent accidental entry into the PORO mode.

8.8 Oscillator stop detection function

The PCF2127A has an on-chip oscillator detection circuit which monitors the status of the oscillation: whenever the oscillation stops, a reset occurs and the oscillator stop flag OSF (in register Seconds) is set logic 1.

- **Power-on:**
  a. The oscillator is not running, the chip is in reset (pin $\overline{RST}$ is LOW and flag OSF is logic 1).
  b. When the oscillator starts running and is stable after power-on, the chip exits from reset (pin $\overline{RST}$ is HIGH).
  c. The flag OSF is still logic 1 and can be cleared (OSF set logic 0) via the interface.
- **Power supply failure:**
  a. When the power supply of the chip (V_{DD} or V_{BAT}) drops below a certain value (V_{low}), typically 1.2 V, the oscillator stops running and a reset occurs.
  b. When the power supply returns to normal operation, the oscillator starts running again, the chip exits from reset.
  c. The flag OSF is still logic 1 and can be cleared (OSF set logic 0) via the interface.



(1) Theoretical state of the signals since there is no power.

(2) The oscillator stop flag (OSF), set logic 1, indicates that the oscillation has stopped and a reset has occurred since the flag was last cleared (OSF set logic 0). In this case the integrity of the clock information is not guaranteed. The OSF flag is cleared using the interface.

Fig 16. Power failure event due to battery discharge: reset occurs

8.9 Time and date function

The majority of these registers are coded in the Binary Coded Decimal (BCD) format.

8.9.1 Register Seconds

Table 19. Seconds - seconds and clock integrity register (address 03h) bit description

Bit	Symbol	Value	Place value	Description
7	OSF	0	-	clock integrity is guaranteed
		1[1]	-	clock integrity is not guaranteed: oscillator has stopped and chip reset has occurred since flag was last cleared
6 to 4	SECONDS	0 to 5	ten's place	actual seconds coded in BCD format
3 to 0		0 to 9	unit place	

[1] Start-up value.

Table 20. Seconds coded in BCD format

Seconds value in decimal	Upper-digit (ten's place)			Digit (unit place)			
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

8.9.2 Register Minutes

Table 21. Minutes - minutes register (address 04h) bit description

Bit	Symbol	Value	Place value	Description
7	-	-	-	unused
6 to 4	MINUTES	0 to 5	ten's place	actual minutes coded in BCD format
3 to 0		0 to 9	unit place	

8.9.3 Register Hours

Table 22. Hours - hours register (address 05h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
12 hour mode[1]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOURS	0 to 1	ten's place	actual hours coded in BCD format when in 12 hour mode
3 to 0		0 to 9	unit place	
24 hour mode[1]				
5 to 4	HOURS	0 to 2	ten's place	actual hours coded in BCD format when in 24 hour mode
3 to 0		0 to 9	unit place	

[1] Hour mode is set by the bit 12_24 in register Control_1.

8.9.4 Register Days

Table 23. Days - days register (address 06h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
5 to 4	DAYS[1]	0 to 3	ten's place	actual day coded in BCD format
3 to 0		0 to 9	unit place	

[1] The RTC compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

8.9.5 Register Weekdays

Table 24. Weekdays - weekdays register (address 07h) bit description

Bit	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0	WEEKDAYS	0 to 6	actual weekday value, see Table 25

Although the association of the weekdays counter to the actual weekday is arbitrary, the PCF2127A will assume Sunday is 000 and Monday is 001 for the purposes of determining the increment for calendar weeks.

Table 25. Weekday assignments

Day[1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] These bits may be re-assigned by the user.

8.9.6 Register Months

Table 26. Months - months register (address 08h) bit description

Bit	Symbol	Value	Place value	Description
7 to 5	-	-	-	unused
4	MONTHS	0 to 1	ten's place	actual month coded in BCD format, see Table 27
3 to 0		0 to 9	unit place	

Table 27. Month assignments in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

8.9.7 Register Years

Table 28. Years - years register (address 09h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0 to 9	ten's place	actual year coded in BCD format
3 to 0		0 to 9	unit place	

8.9.8 Setting and reading the time

Figure 17 shows the data flow and data dependencies starting from the 1 Hz clock tick.

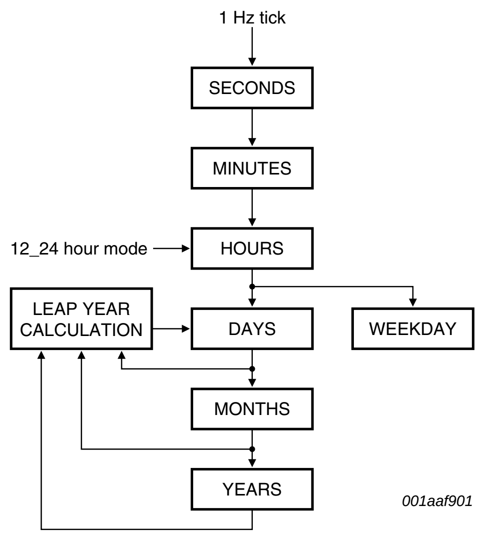


Fig 17. Data flow of the time function

During read/write operations, the time counting circuits (memory locations 03h through 09h) are blocked.

This prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 18).

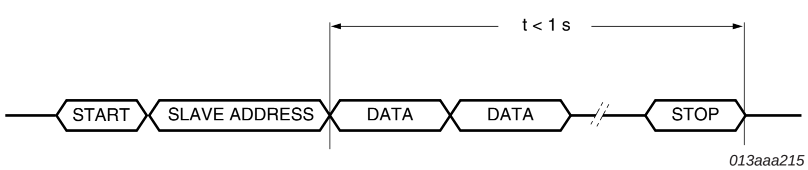


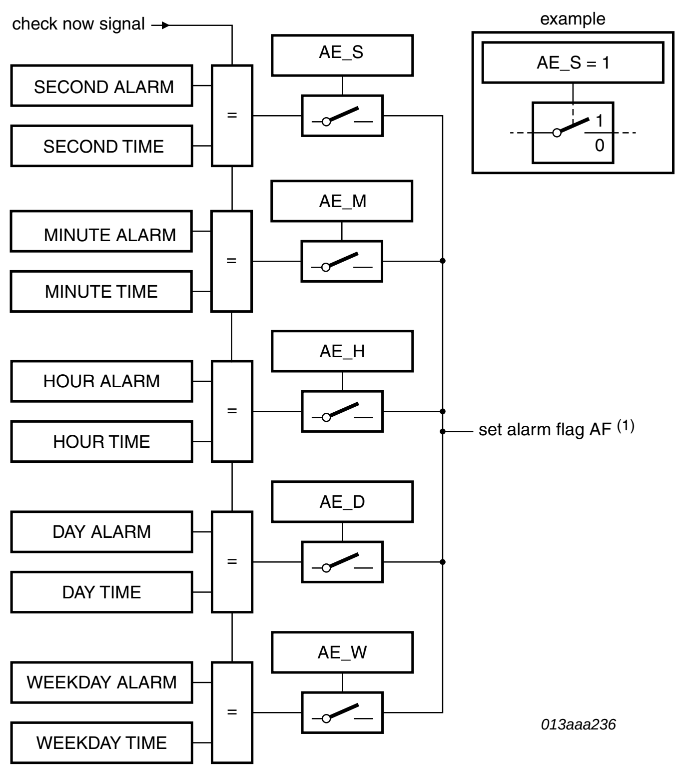
Fig 18. Access time for read/write operations

As a consequence of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time may increment between the two accesses. A similar problem exists when reading. A roll over may occur between reads thus giving the minutes from one moment and the hours from the next. Therefore it is advised to read all time and date registers in one access.

8.10 Alarm function

When one or more of the alarm bit fields are loaded with a valid second, minute, hour, day, or weekday and its corresponding alarm enable bit (AE_x) is logic 0, then that information is compared with the actual second, minute, hour, day, and weekday (see Figure 19).



(1) Only when all enabled alarm settings are matching.

Fig 19. Alarm function block diagram

The generation of interrupts from the alarm function is described in Section 8.13.4.

8.10.1 Register Second_alarm

Table 29. Second_alarm - second alarm register (address 0Ah) bit description

Bit	Symbol	Value	Place value	Description
7	AE_S	0	-	second alarm is enabled
		1[1]	-	second alarm is disabled
6 to 4	SECOND_ALARM	0 to 5	ten's place	second alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.10.2 Register Minute_alarm

Table 30. Minute_alarm - minute alarm register (address 0Bh) bit description

Bit	Symbol	Value	Place value	Description
7	AE_M	0	-	minute alarm is enabled
		1[1]	-	minute alarm is disabled
6 to 4	MINUTE_ALARM	0 to 5	ten's place	minute alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.10.3 Register Hour_alarm

Table 31. Hour_alarm - hour alarm register (address 0Ch) bit description

Bit	Symbol	Value	Place value	Description
7	AE_H	0	-	hour alarm is enabled
		1[1]	-	hour alarm is disabled
6	-	-	-	unused
12 hour mode[2]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOUR_ALARM	0 to 1	ten's place	hour alarm information coded in BCD format when in 12 hour mode
3 to 0		0 to 9	unit place	
24 hour mode[2]				
5 to 4	HOUR_ALARM	0 to 2	ten's place	hour alarm information coded in BCD format when in 24 hour mode
3 to 0		0 to 9	unit place	

[1] Default value.

[2] Hour mode is set by the bit 12_24 in register Control_1.

8.10.4 Register Day_alarm

Table 32. Day_alarm - day rearm register (address 0Dh) bit description

Bit	Symbol	Value	Place value	Description
7	AE_D	0	-	day alarm is enabled
		1[1]	-	day alarm is disabled
6	-	-	-	unused
5 to 4	DAY_ALARM	0 to 3	ten's place	day alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.10.5 Register Weekday_alarm

Table 33. Weekday_alarm - weekday alarm register (address 0Eh) bit description

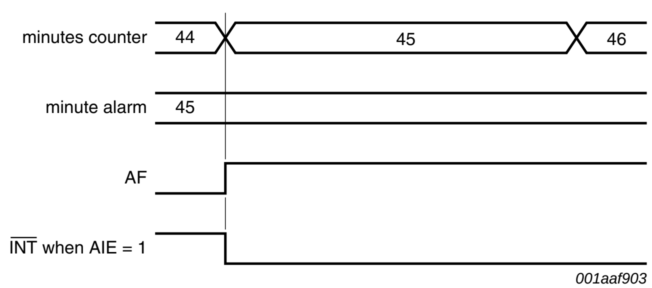
Bit	Symbol	Value	Description
7	AE_W	0	weekday alarm is enabled
		1[1]	weekday alarm is disabled
6 to 3	-	-	unused
2 to 0	WEEKDAY_ALARM	0 to 6	weekday alarm information

[1] Default value.

8.10.6 Alarm flag

When all enabled comparisons first match, the alarm flag AF (register Control_2) is set. AF will remain set until cleared by using the interface. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. For clearing the flags see Section 8.11.6

Alarm registers which have their alarm enable bit AE_x at logic 1 are ignored.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 20. Alarm flag timing diagram

8.11 Timer functions

The PCF2127A has two different timer functions, a watchdog timer and a countdown timer. The timers can be selected by using the control bits WD_CD[1:0] in the register Watchdg_tim_ctl.

- The watchdog timer has four selectable source clocks. It can be used to detect a microprocessor with interrupt and reset capability which is out of control (see Section 8.11.3)
- The countdown timer has four selectable source clocks allowing for countdown periods from less than 1 ms to more than 4 hours (see Section 8.11.4)

To control the timer functions and timer output, the registers Control_2, Watchdg_tim_ctl, and Watchdg_tim_val are used.

8.11.1 Register Watchdg_tim_ctl

Table 34. Watchdg_tim_ctl - watchdog timer control register (address 10h) bit description

Bit	Symbol	Value	Description
7 to 6	WD_CD[1:0]	00[1]	watchdog timer disabled; countdown timer disabled
		01	watchdog timer disabled; countdown timer enabled if CDTIE is set logic 1, the interrupt pin $\overline{\text{INT}}$ is activated when the countdown timed out
		10	watchdog timer enabled; the interrupt pin $\overline{\text{INT}}$ is activated when timed out; countdown timer not available
		11	watchdog timer enabled; the reset pin $\overline{\text{RST}}$ is activated when timed out; countdown timer not available
5	TI_TP	0[1]	the interrupt pin $\overline{\text{INT}}$ is configured to generate a permanent active signal when MSF and/or CDTF is set
		1	the interrupt pin $\overline{\text{INT}}$ is configured to generate a pulsed signal when MSF flag and/or CDTF flag is set (see Figure 25)
4 to 2	-	-	unused
1 to 0	TF[1:0]		timer source clock for watchdog and countdown timer
		00	4.096 kHz
		01	64 Hz
		10	1 Hz
		11[1]	$^1/_{60}$ Hz

[1] Default value.

8.11.2 Register Watchdg_tim_val

Table 35. Watchdg_tim_val - watchdog timer value register (address 11h) bit description

Bit	Symbol	Value	Description
7 to 0	WATCHDG_TIM_VAL[7:0]	00 to FF	countdown period in seconds: $CountdownPeriod = \frac{n}{SourceClockFrequency}$ where n is the countdown value

Table 36. Programmable watchdog or countdown timer

TF[1:0]	Timer source clock frequency	Units	Minimum timer period (n = 1)	Units	Maximum timer period (n = 255)	Units
00	4.096	kHz	244	μs	62.256	ms
01	64	Hz	15.625	ms	3.984	s
10	1	Hz	1	s	255	s
11	$\frac{1}{60}$	Hz	60	s	15300	s

8.11.3 Watchdog timer function

The watchdog timer function is controlled by the WD_CD[1:0] bits of the register Watchdg_tim_ctl (see Table 34).

The two bits TF[1:0] in register Watchdg_tim_ctl determine one of the four source clock frequencies for the watchdog timer: 4.096 kHz, 64 Hz, 1 Hz, or $\frac{1}{60}$ Hz (see Table 36).

When the watchdog timer function is enabled, the 8 bit timer in register Watchdg_tim_val (see Table 35) determines the watchdog timer period.

The watchdog timer counts down from the software programmed 8 bit binary value n in register Watchdg_tim_val. When the counter reaches 1 the watchdog timer flag WDTF is set logic 1.

In the case that WDTF is logic 1:

- if WD_CD[1:0] = 10 an interrupt will be generated
- if WD_CD[1:0] = 11 a reset will be generated

The counter does not automatically reload.

When WD_CD[1:0] = 10 or WD_CD[1:0] = 11 and the microcontroller unit (MCU) loads a watchdog timer value n:

- the flag WDTF is reset
- $\overline{INT}$ or $\overline{RST}$ is cleared
- the watchdog timer starts again

Loading the counter with 0 will:

- reset the flag WDTF
- clear $\overline{INT}$ or $\overline{RST}$
- stop the watchdog timer

WDTF is read only. A read of the register Control_2 will automatically reset the flag WDTF.

- When the watchdog timer counter reaches 1, the watchdog timer flag WDTF is set logic 1
- When the countdown timer counter reaches 1, the countdown timer flag CDTF is set logic 1
- When a minute or second interrupt occurs, the minute/second flag MSF is set logic 1 (see Section 8.13.1.1)

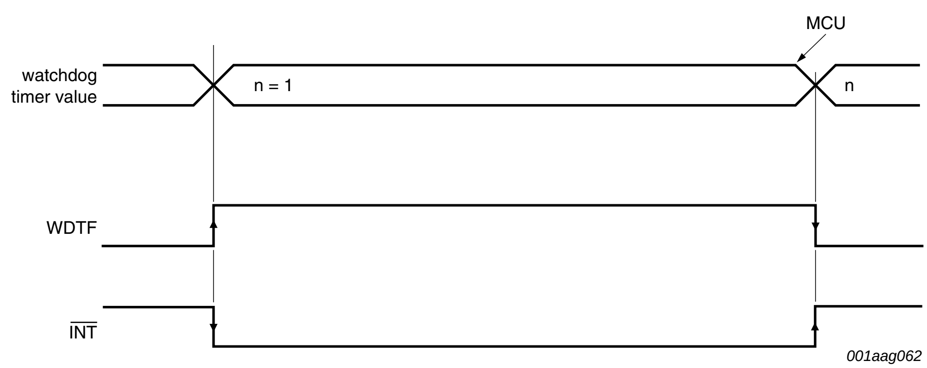
The watchdog timer flag WDTF is read only and cannot be cleared with the interface. WDTF can be cleared by

- loading a value in register Watchdg_tim_val
- reading of the register Control_2

Writing a logic 0 or logic 1 to WDTF has no effect.

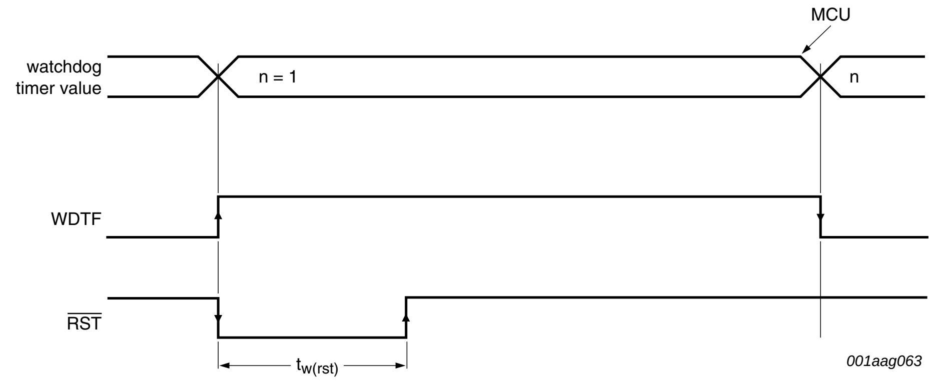
Table 37. Specification of $t_{w(rst)}$

WD_CD[1:0]	TF[1:0]	$t_{w(rst)}$
11	00	244 μs
	01	15.625 ms
	10	15.625 ms
	11	15.625 ms



Counter reached 1, WDTF is set logic 1, an interrupt is generated.

Fig 21. WD_CD[1:0] = 10: watchdog activates an interrupt when timed out



Counter reached 1, WDTF is set logic 1, reset pulse on the $\overline{RST}$ pin is generated for a time equal to $t_{w(rst)}$.

Fig 22. WD_CD[1:0] = 11: watchdog activates a reset pulse when timed out

8.11.4 Countdown timer function

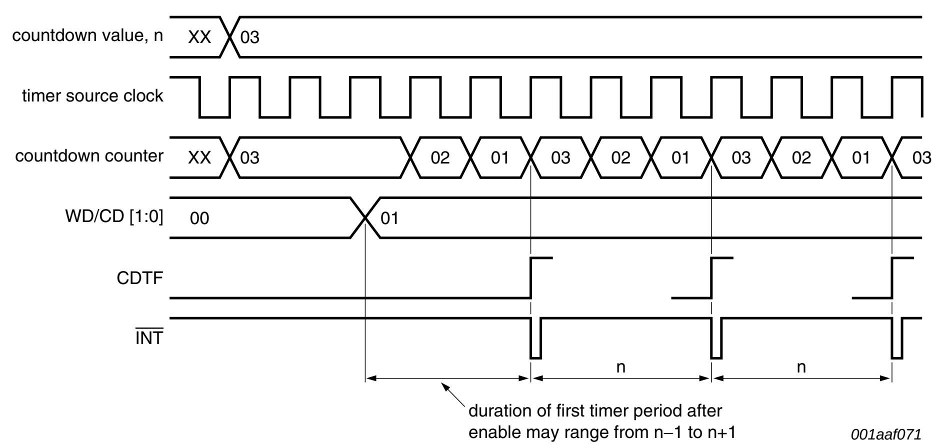
The countdown timer function is controlled by the WD_CD[1:0] bits in register Watchdg_tim_ctl (see Table 34).

The timer counts down from the software programmed 8 bit binary value n in register Watchdg_tim_val. When the counter reaches 1

- the countdown timer flag CDTF is set
- the counter automatically reloads
- and the next time period starts

Loading the counter with 0 effectively stops the timer.

Reading the timer will return the actual value of the countdown counter.



In this example it is assumed that the countdown timer flag (CDTF) is cleared before the next countdown period expires and that $\overline{INT}$ is set to pulsed mode.

Fig 23. General countdown timer behavior

If a new value of n is written before the end of the actual timer period, this value will take immediate effect. It is not recommended to change n without first disabling the counter by setting WD_CD[1:0] = 00. The update of n is asynchronous to the timer clock. Therefore changing it on the fly could result in a corrupted value loaded into the countdown counter. This can result in an undetermined countdown period for the first period. The countdown value n will, however, be correctly stored and correctly loaded on subsequent timer periods.

When the countdown timer flag CDTF is set, an interrupt signal on $\overline{INT}$ will be generated provided that this mode is enabled. See Section 8.13.1.2 for details on how the interrupt can be controlled.

When starting the countdown timer for the first time, only the first period will not have a fixed duration. The amount of inaccuracy for the first timer period will depend on the chosen source clock, see Table 38.

Table 38. First period delay for timer counter

Timer source clock	Minimum timer period	Maximum timer period
4.096 kHz	n	n + 1
64 Hz	n	n + 1
1 Hz	(n – 1) + $\frac{1}{64}$ Hz	n + $\frac{1}{64}$ Hz
$\frac{1}{60}$ Hz	(n – 1) + $\frac{1}{64}$ Hz	n + $\frac{1}{64}$ Hz

At the end of every countdown, the timer sets the countdown timer flag (CDTF). CDTF may only be cleared by software. The asserted CDTF can be used to generate an interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of CDTF. TI_TP is used to control this mode selection. The interrupt output may be disabled with the CDTIE bit, see Table 6.

When reading the timer, the actual countdown value is returned and **not** the initial value n. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

8.11.5 Pre-defined timers: second and minute interrupt

PCF2127A has two pre-defined timers which are used to generate an interrupt either once per second or once per minute. The pulse generator for the minute or second interrupt operates from an internal 64 Hz clock. It is independent of the watchdog or countdown timers.

8.11.6 Clearing flags

The flags MSF, CDTF, AF and TSFx can be cleared by using the interface. To prevent one flag being overwritten while clearing another, a logic AND is performed during the write access. A flag is cleared by writing logic 0 whilst a flag is not cleared by writing logic 1. Writing logic 1 will result in the flag value remaining unchanged.

Four examples are given for clearing the flags. Clearing the flags is made by a write command, therefore bits labelled with

- '-' must be written with their previous values
- 'WDTF' is read only and has to be written with logic 0

Repeatedly re-writing these bits has no influence on the functional behavior.

Table 39. Flag location in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	MSF	WDTF	TSF2	AF	CDTF	-	-	-

Table 40. Example values in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	1	0	1	1	1	0	0	0

The following tables show what instruction must be sent to clear the appropriate flag.

Table 41. Example to clear only CDTF (bit 3) in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	1	0	1	1	0	-[1]	-[1]	-[1]

[1] The bits labeled as - have to be rewritten with the previous values.

Table 42. Example to clear only AF (bit 4) in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	1	0	1	0	1	0[1]	0[1]	0[1]

[1] The bits labeled as - have to be rewritten with the previous values.

Table 43. Example to clear only MSF (bit 7) in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	0	0	1	1	1	0[1]	0[1]	0[1]

[1] The bits labeled as - have to be rewritten with the previous values.

Table 44. Example to clear both CDTF and MSF in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	0	0	1	1	0	0[1]	0[1]	0[1]

[1] The bits labeled as - have to be rewritten with the previous values.

8.12 Timestamp function

The PCF2127A has an active LOW timestamp input pin $\overline{TS}$, internally pulled with an on-chip pull-up resistor to the internal power supply of the device. It also has a timestamp detection circuit which can detect two different events:

1. $\overline{TS}$ input on the pin is driven to an intermediate level between the power supply and ground.
2. $\overline{TS}$ input on the pin is driven to ground.

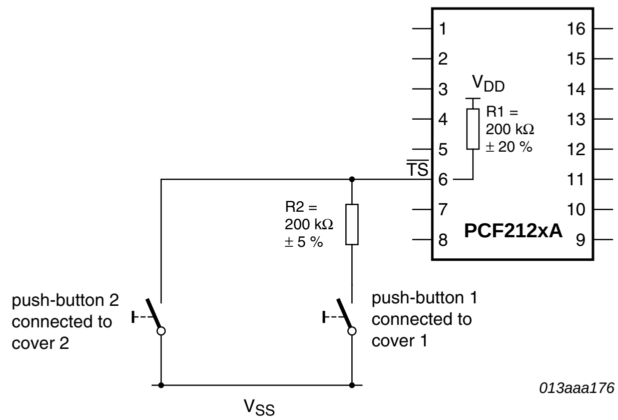


Fig 24. Timestamp detection with two push-buttons on one the $\overline{TS}$ pin (e.g. for tamper detection)

The timestamp function is enabled by default after power-on and it can be switched off by setting the control bit TSOFF (register Timestp_ctl).

A most common application of the timestamp function is described in Ref. 3 “AN10857”.

See Section 8.13.5 for a description of interrupt generation from the timestamp function.

8.12.1 Timestamp flag

1. When the $\overline{TS}$ input pin is driven to an intermediate level between the power supply and ground the following sequence occurs:
   a. The actual date and time are stored in the timestamp registers.
   b. The timestamp flag TSF1 (register Control_1) is set.
   c. If the TSIE bit (register Control_2) is active, an interrupt on the $\overline{INT}$ pin is generated.

   The TSF1 flag can be cleared by using the interface. Clearing the flag will clear the interrupt. Once TSF1 is cleared it will only be set again when a new negative edge on $\overline{TS}$ is detected.
2. When the $\overline{TS}$ input pin is driven to ground the following sequence occurs:
   a. The actual date and time are stored in the timestamp registers.
   b. In addition to the TSF1 flag the TSF2 flag (register Control_3) is set.
   c. If the TSIE bit is active, an interrupt on the $\overline{INT}$ pin is generated.

The TSF1 and TSF2 flags can be cleared by using the interface; clearing both flags will clear the interrupt. Once TSF2 is cleared it will only be set again when $\overline{TS}$ is driven to ground once again.

8.12.2 Time stamp mode

The timestamp function has two different modes selected by the control bit TSM (timestamp mode) in register Timestp_ctl:

- If TSM is logic 0 (default): in subsequent trigger events without clearing the timestamp flags, the last timestamp event is stored
- If TSM is logic 1: in subsequent trigger events without clearing the timestamp flags, the first timestamp event is stored

The timestamp function also depends on the control bit BTSE (battery switch timestamp enable) in register Control_3, see Section 8.12.4.

8.12.3 Timestamp registers

8.12.3.1 Register Timestp_ctl

Table 45. Timestp_ctl - timestamp control register (address 12h) bit description

Bit	Symbol	Value	Description
7	TSM	0[1]	in subsequent events without clearing the timestamp flags, the last event is stored
		1	in subsequent events without clearing the timestamp flags, the first event is stored
6	TSOFF	0[1]	timestamp function active
		1	timestamp function disabled
5	-	-	unused
4 to 0	1_O_16_TIMESTP[4:0]		$^{1}/_{16}$ second timestamp information coded in BCD format

[1] Default value.

8.12.3.2 Register Sec_timestp

Table 46. Sec_timestp - second timestamp register (address 13h) bit description

Bit	Symbol	Value	Place value	Description
7	-	-	-	unused
6 to 4	SECOND_TIMESTP	0 to 5	ten's place	second timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

8.12.3.3 Register Min_timestp

Table 47. Min_timestp - minute timestamp register (address 14h) bit description

Bit	Symbol	Value	Place value	Description
7	-	-	-	unused
6 to 4	MINUTE_TIMESTP	0 to 5	ten's place	minute timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

8.12.3.4 Register Hour_timestp

Table 48. Hour_timestp - hour timestamp register (address 15h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
12 hour mode[1]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOUR_TIMESTP	0 to 1	ten’s place	hour timestamp information coded in BCD format when in 12 hour mode
3 to 0		0 to 9	unit place	
24 hour mode[1]				
5 to 4	HOUR_TIMESTP	0 to 2	ten’s place	hour timestamp information coded in BCD format when in 24 hour mode
3 to 0		0 to 9	unit place	

[1] Hour mode is set by the bit 12_24 in register Control_1.

8.12.3.5 Register Day_timestp

Table 49. Day_timestp - day timestamp register (address 16h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
5 to 4	DAY_TIMESTP	0 to 3	ten’s place	day timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

8.12.3.6 Register Mon_timestp

Table 50. Mon_timestp - month timestamp register (address 17h) bit description

Bit	Symbol	Value	Place value	Description
7 to 5	-	-	-	unused
4	MONTH_TIMESTP	0 to 1	ten’s place	month timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

8.12.3.7 Register Year_timestp

Table 51. Year_timestp - year timestamp register (address 18h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEAR_TIMESTP	0 to 9	ten’s place	year timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

8.12.4 Dependency between Battery switch-over and timestamp

The timestamp function depends on the control bit BTSE in register Control_3:

Table 52. Battery switch-over and timestamp

BTSE	BF	Description
0	- [1]	the battery switch-over does not affect the timestamp registers
1		If a battery switch-over event occurs:
	0	the timestamp registers store the time and date when the switch-over occurs; after this event occurred BF is set logic 1
	1	the timestamp registers are not modified; in this condition subsequent battery switch-over events or falling edges on pin $\overline{TS}$ are not registered

[1] Default value.

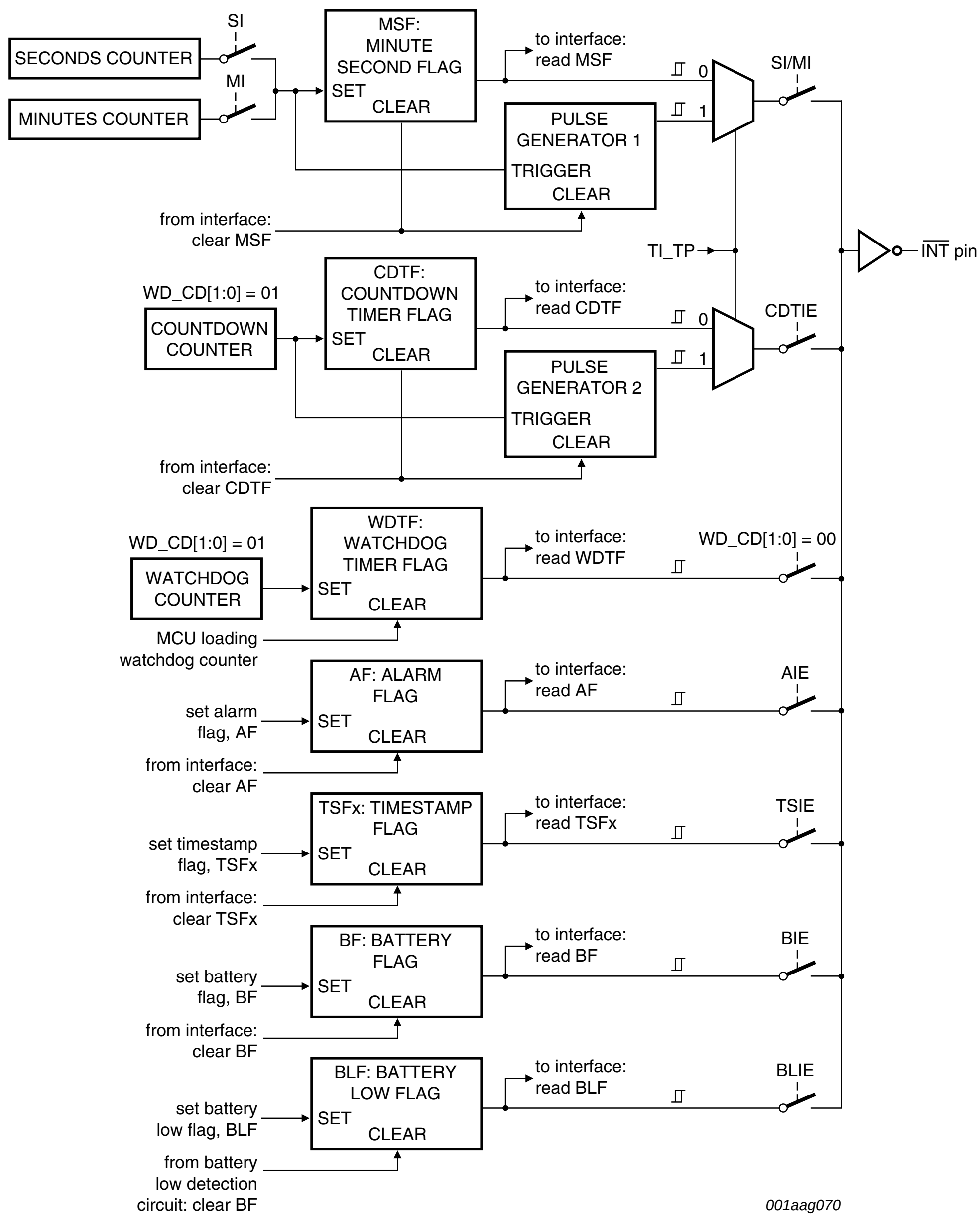
8.13 Interrupt output, $\overline{INT}$

PCF2127A has an interrupt output pin $\overline{INT}$ which is open-drain, active LOW. Interrupts may be sourced from different places:

- second or minute timer
- countdown timer
- watchdog timer
- alarm
- timestamp
- battery switch-over
- battery low detection

The control bit TI_TP (register Watchdg_tim_ctl) is used to configure whether the interrupts generated from the second/minute timer (flag MSF in register Control_2) and the countdown timer (flag CDTF in register Control_2) are pulsed signals or a permanently active signal. All the other interrupt sources generate a permanently active interrupt signal which follows the status of the corresponding flags. When the interrupt sources are all disabled, $\overline{INT}$ remains high-impedance.

- The flags MSF, CDTF, AF, TSFx and BF can be cleared by using the interface
- The flags WDTF is read only. How it can be cleared is explained in Section 8.11.6
- The flag BLF is read only. It is cleared automatically from the battery low detection circuit when the battery is replaced



When SI, MI, CDTIE, WD_CD, AIE, TSIE, BIE, BLIE are all disabled, $\overline{\text{INT}}$ will remain high-impedance.

Fig 25. Interrupt block diagram

8.13.1 Minute, second and countdown timer interrupts

8.13.1.1 Minute and second interrupts

Minute and second interrupts are generated by predefined timers. The timers can be enabled independently from one another by the bits MI and SI in register Control_1. However, a minute interrupt enabled on top of a second interrupt will not be distinguishable since it will occur at the same time.

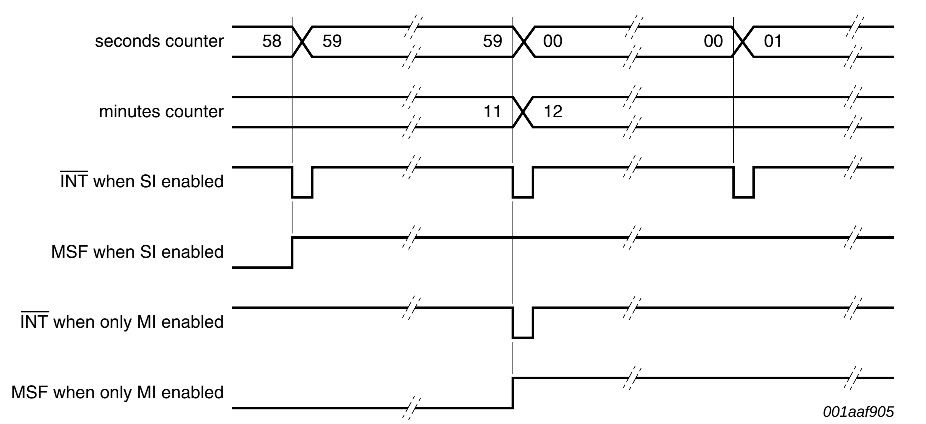
The minute/second flag MSF (register Control_2) is set logic 1 when either the seconds or the minutes counter increments according to the actually enabled interrupt (see Table 53). The MSF flag can be read and cleared by the interface.

Table 53. Effect of bits MI and SI on pin INT and bit MSF

MI	SI	Result on INT	Result on MSF
0	0	no interrupt generated	MSF never set
1	0	an interrupt once per minute	MSF set when **minutes** counter increments
0	1	an interrupt once per second	MSF set when **seconds** counter increments
1	1	an interrupt once per second	MSF set when **seconds** counter increments

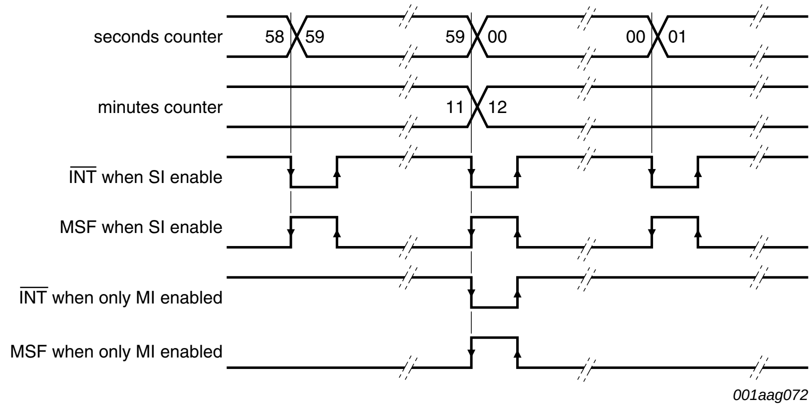
When MSF is set logic 1:

- If TI_TP is logic 1 the interrupt is generated as a pulsed signal.
- If TI_TP is logic 0 the interrupt is permanently active signal that remains until MSF is cleared.



In this example, bit TI_TP is logic 1 and the MSF flag is not cleared after an interrupt.

Fig 26. INT example for SI and MI when TI_TP is logic 1



In this example, bit TI_TP is logic 0 and the MSF flag is cleared after an interrupt.

Fig 27. INT example for SI and MI when TI_TP is logic 0

The pulse generator for the minute/second interrupt operates from an internal 64 Hz clock and generates a pulse of $^1/_{64}$ seconds in duration.

8.13.1.2 Countdown timer interrupts

The generation of interrupts from the countdown timer is controlled via the CDTIE bit (register Control_2).

The interrupt may be generated as a pulsed signal at every countdown period or as a permanently active signal which follows the status of the countdown timer flag CDTF. Bit TI_TP is used to control this flag.

8.13.2 INT pulse shortening

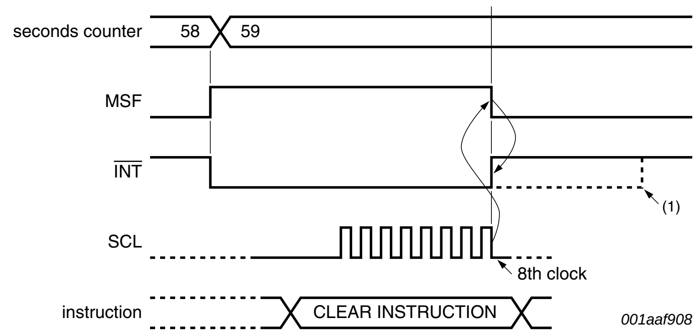
The pulse generator for the countdown timer interrupt also uses an internal clock, but this time it is dependent on the selected source clock for the countdown timer and on the countdown value n. As a consequence, the width of the interrupt pulse varies (see Table 54).

Table 54. INT operation (bit TI_TP = 1)

Source clock (Hz)	INT period (s)	
	n = 1[1]	n > 1
4096	$^1/_{8192}$	$^1/_{4096}$
64	$^1/_{128}$	$^1/_{64}$
1	$^1/_{64}$	$^1/_{64}$
$^1/_{60}$	$^1/_{64}$	$^1/_{64}$

[1] n = loaded countdown value. Timer stopped when n = 0.

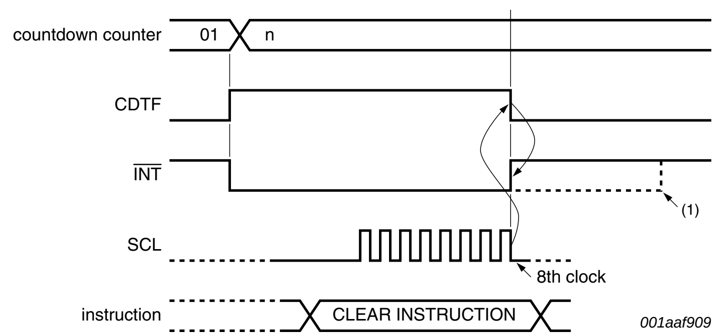
If the MSF or CDTF flag (register Control_2) is cleared before the end of the INT pulse, then the INT pulse is shortened. This allows the source of a system interrupt to be cleared immediately when it is serviced, i.e. the system does not have to wait for the completion of the pulse before continuing; see Figure 28 and Figure 29. Instructions for clearing bit MSF and bit CDTF can be found in Section 8.11.6.



(1) Indicates normal duration of $\overline{INT}$ pulse.

The timing shown for clearing bit MSF is also valid for the non-pulsed interrupt mode, i.e. when TI_TP is logic 0, where the $\overline{INT}$ pulse may be shortened by setting both bits MI and SI logic 0.

Fig 28. Example of shortening the $\overline{INT}$ pulse by clearing the MSF flag



(1) Indicates normal duration of $\overline{INT}$ pulse.

The timing shown for clearing CDTF is also valid for the non-pulsed interrupt mode, i.e. when TI_TP is logic 0, where the $\overline{INT}$ pulse may be shortened by setting CDTIE logic 0.

Fig 29. Example of shortening the $\overline{INT}$ pulse by clearing the CDTF flag

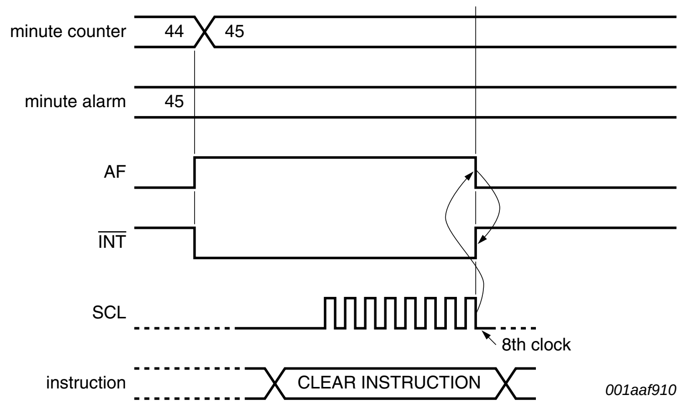
8.13.3 Watchdog timer interrupts

The generation of interrupts from the watchdog timer is controlled using the WD_CD[1:0] bits (register Watchdg_tim_ctl). The interrupt is generated as an active signal which follows the status of the watchdog timer flag WDTF (register Control_2). No pulse generation is possible for watchdog timer interrupts.

The interrupt is cleared when the flag WDTF is reset. WDTF is a read only bit and cannot be cleared by using the interface. Instructions for clearing it can be found in Section 8.11.6.

8.13.4 Alarm interrupts

Generation of interrupts from the alarm function is controlled via the bit AIE (register Control_2). If AIE is enabled, the $\overline{INT}$ pin will follow the status of bit AF (register Control_2). Clearing AF will immediately clear $\overline{INT}$. No pulse generation is possible for alarm interrupts.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 30. AF timing diagram

8.13.5 Timestamp interrupts

Interrupt generation from the timestamp function is controlled using the TSIE bit (register Control_2). If TSIE is enabled the $\overline{INT}$ pin follows the status of the flags TSFx. Clearing the flags TSFx immediately clears $\overline{INT}$. No pulse generation is possible for timestamp interrupts.

8.13.6 Battery switch-over interrupts

Generation of interrupts from the battery switch-over is controlled via the BIE bit (register Control_3). If BIE is enabled, the $\overline{INT}$ pin follows the status of bit BF (register Control_3). Clearing BF immediately clears $\overline{INT}$. No pulse generation is possible for battery switch-over interrupts.

8.13.7 Battery low detection interrupts

Generation of interrupts from the battery low detection is controlled via the BLIE bit (register Control_3). If BLIE is enabled the $\overline{INT}$ pin will follow the status of bit BLF (register Control_3). The interrupt is cleared when the battery is replaced (BLF is logic 0) or when bit BLIE is disabled (BLIE is logic 0). BLF is read only and therefore cannot be cleared via the interface.

8.14 External clock test mode

A test mode is available which allows on-board testing. In this mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit EXT_TEST logic 1 (register Control_1). Then pin CLKOUT becomes an input. The test mode replaces the internal clock signal (64 Hz) with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT generate an increment of one second.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1000 ns. The internal clock, now sourced from CLKOUT, is divided down by a 2^6 divider chain called prescaler (see prescaler in Table 55). The prescaler can be set into a known state by using bit STOP. When bit STOP is logic 1, the prescaler is reset to 0. STOP must be cleared before the prescaler can operate again.

From a stop condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

Remark: Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operating example:

1. Set EXT_TEST test mode (register Control_1, EXT_TEST is logic 1).
2. Set bit STOP (register Control_1, STOP is logic 1).
3. Set time registers to desired value.
4. Clear STOP (register Control_1, STOP is logic 0).
5. Apply 32 clock pulses to CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to CLKOUT.
8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

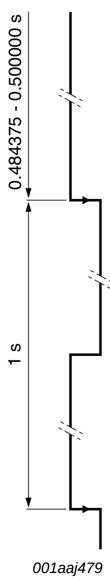
8.15 STOP bit function

The function of the STOP bit is to allow for accurate starting of the time circuits. STOP will cause the upper part of the prescaler (F_9 to F_{14}) to be held in reset and thus no 1 Hz ticks are generated. The time circuits can then be set and will not increment until the STOP bit is released. STOP will not affect the CLKOUT signal but the output of the prescaler in the range of 32 Hz to 1 Hz (see Figure 31).

The lower stages of the prescaler, F_0 to F_8, are not reset and because the I^2C-bus and the SPI-bus are asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits is between 0 and one 64 Hz cycle (0.484375 s and 0.500000 s), see Table 55 and Figure 32.

Table 55. First increment of time circuits after stop release

Bit STOP	Prescaler bits[1] F_0 to F_8 - F_9 to F_{14}	1 Hz tick	Time hh:mm:ss	Comment
Clock is running normally				
0	010000111-010100		12:45:12	prescaler counting normally
STOP bit is activated by user. F_0 to F_8 are not reset and values cannot be predicted externally				
1	XXXXXXXXX-000000		12:45:12	prescaler is reset; time circuits are frozen
New time is set by user				
1	XXXXXXXXX-000000		08:00:00	prescaler is reset; time circuits are frozen
STOP bit is released by user				
0	XXXXXXXXX-000000		08:00:00	prescaler is now running
0	XXXXXXXXX-100000		08:00:00	
0	XXXXXXXXX-100000		08:00:00	
0	XXXXXXXXX-110000		08:00:00	
:	:		:	
0	111111111-111110		08:00:00	
0	000000000-000001		08:00:01	0 to 1 transition of F14 increments the time circuits
0	100000000-000001		08:00:01	
:	:		:	
0	111111111-111111		08:00:01	
0	000000000-000000		08:00:01	
0	100000000-000000			
:	:		:	
0	111111111-111110		08:00:01	
0	000000000-000001		08:00:02	0 to 1 transition of F14 increments the time circuits



[1] F_0 is clocked at 32.768 kHz.

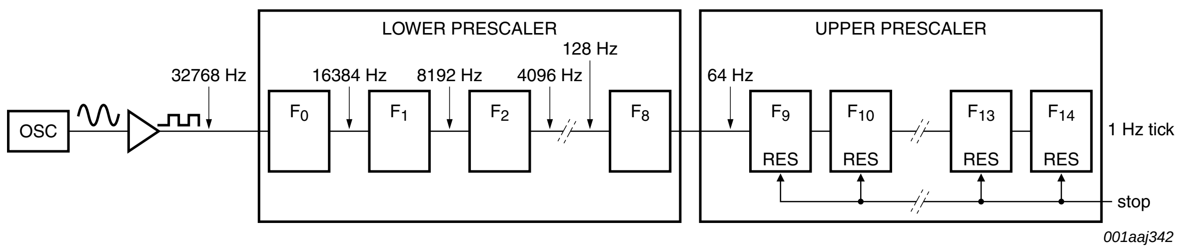


Fig 31. STOP bit functional diagram

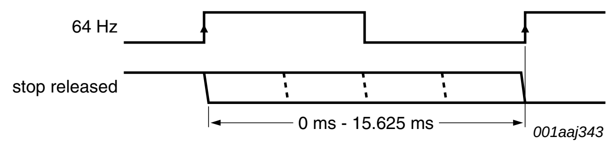


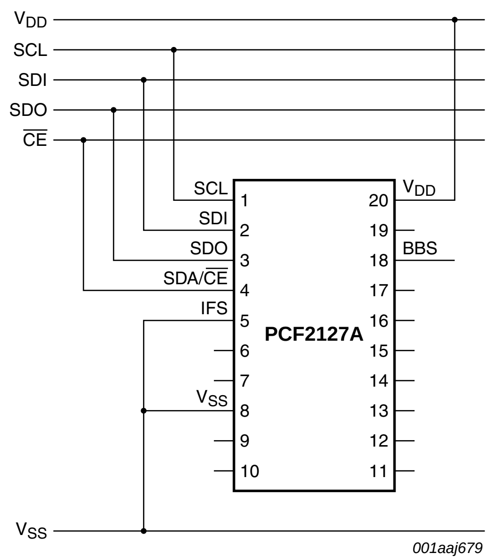
Fig 32. STOP bit release timing

9. Interfaces

The PCF2127A has a selectable I²C-bus or SPI-bus interface. The selection is done using the interface selection pin IFS (see Table 56).

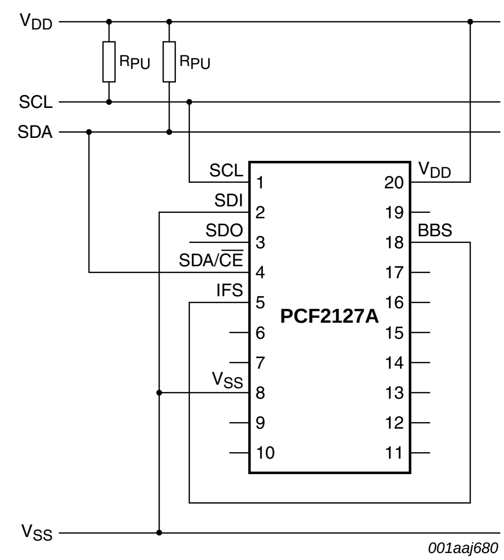
Table 56. Interface selection input pin IFS

Pin	Connection	Bus interface	Reference
IFS	V_{SS}	SPI-bus	Section 9.1
	BBS	I²C-bus	Section 9.2



To select the SPI-bus interface, pin IFS has to be connected to pin V_{SS}.

a. SPI-bus interface selection



To select the I²C-bus interface pin IFS has to be connected to pin BBS.

b. I²C-bus interface selection

Fig 33. Interface selection

9.1 SPI-bus interface

Data transfer to and from the device is made via a 3 wire SPI-bus (see Table 57). The data lines for input and output are split. The data input and output line can be connected together to facilitate a bidirectional data bus (see Figure 34).

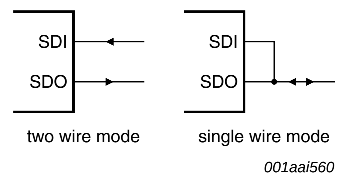


Fig 34. SDI, SDO configurations

The SPI-bus is initialized whenever the chip enable line pin $\overline{CE}$ is inactive.

Table 57. Serial interface

Symbol	Function	Description
SDA/$\overline{CE}$	chip enable input; active LOW	[1] when HIGH, the interface is reset; input may be higher than V_{DD}
SCL	serial clock input	when $\overline{CE}$ is HIGH, input may float; input may be higher than V_{DD}
SDI	serial data input	when $\overline{CE}$ is HIGH, input may float; input may be higher than V_{DD}; input data is sampled on the rising edge of SCL
SDO	serial data output	push-pull output; drives from V_{SS} to V_{BBS}; output data is changed on the falling edge of SCL

[1] The chip enable must not be wired permanently LOW.

9.1.1 Data transmission

The chip enable signal is used to identify the transmitted data. Each data transfer is a byte, with the Most Significant Bit (MSB) sent first.

The transmission is controlled by the active LOW chip enable signal SDA/$\overline{CE}$. The first byte transmitted is the command byte. Subsequent bytes will be either data to be written or data to be read (see Figure 35).

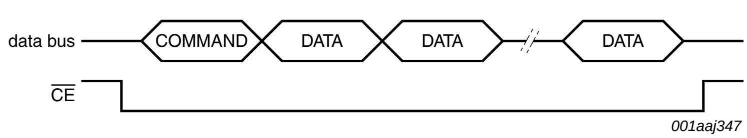
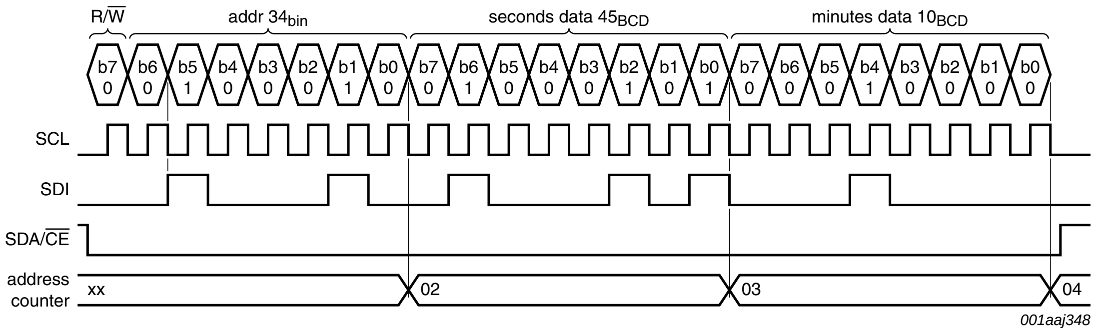


Fig 35. Data transfer overview

The command byte defines the address of the first register to be accessed and the read/write mode. The address counter will auto increment after every access and will reset to zero after the last valid register is accessed. The read/write bit (R/$\overline{W}$) defines if the following bytes will be read or write information.

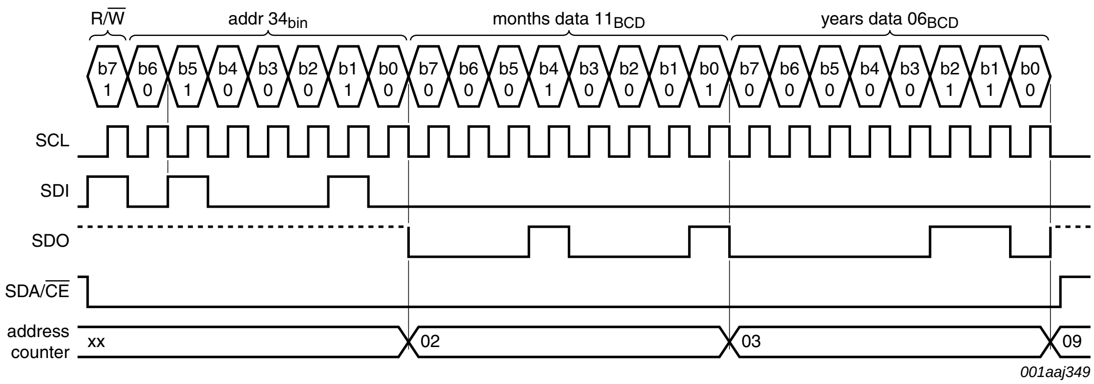
Table 58. Command byte definition

Bit	Symbol	Value	Description
7	R/$\overline{W}$		data read or write selection
		0	write data
		1	read data
6 to 5	SA	01	subaddress; other codes will cause the device to ignore data transfer
4 to 0	RA	00h to 1Dh	register address range



In this example, the register Seconds is set to 45 seconds and the register Minutes to 10 minutes.

Fig 36. SPI-bus write example



In this example, the registers Months and Years are read. In this example, pins SDI and SDO are not connected together. For this configuration, it is important that pin SDI is never left floating. It must always be driven either HIGH or LOW. If pin SDI is left open, high I_{DD} currents may result.

Fig 37. SPI-bus read example

9.2 I^{2}C-bus interface

The I^{2}C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines are connected to a positive supply via a pull-up resistor. Data transfer is initiated only when the bus is not busy.

9.2.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals (see Figure 38).

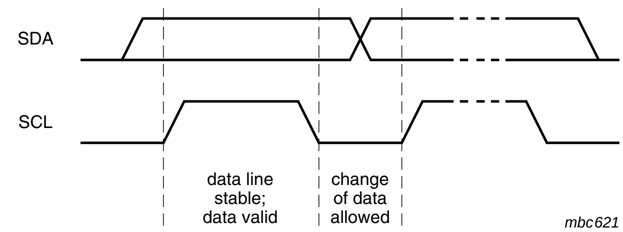


Fig 38. Bit transfer

9.2.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition S. A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the STOP condition P (see Figure 39).

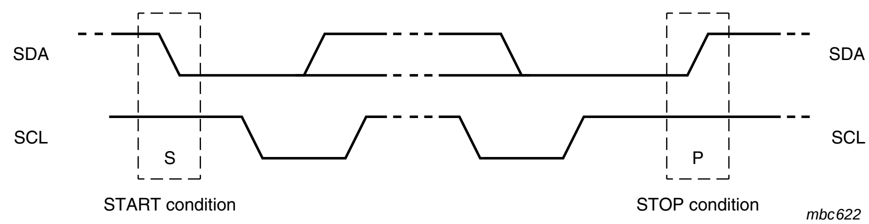


Fig 39. Definition of START and STOP conditions

For this device a repeated START is not allowed for reading. Therefore a STOP has to be released before the next START.

9.2.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves.

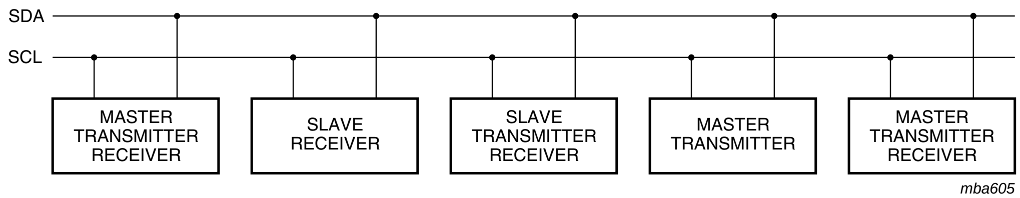


Fig 40. System configuration

The PCF2127A can act as a slave transmitter and a slave receiver.

9.2.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^{2}C-bus is illustrated in Figure 41.

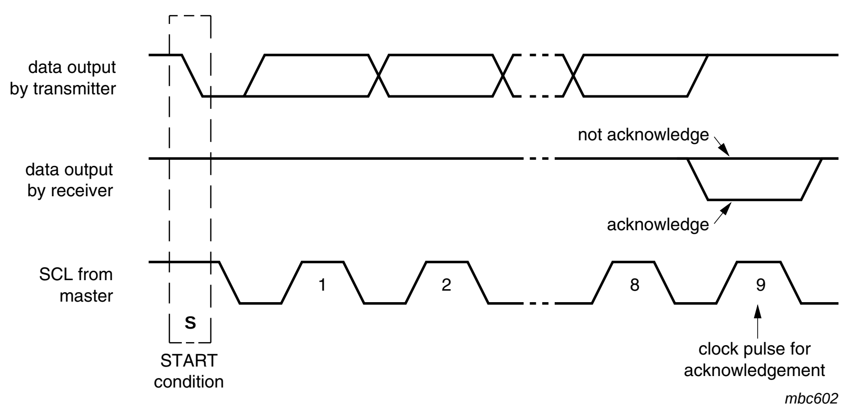


Fig 41. Acknowledgement on the I^{2}C-bus

9.2.5 I²C-bus protocol

After a start condition a valid hardware address has to be sent to a PCF2127A device. The appropriate I²C-bus slave address is 1010001. The entire I²C-bus slave address byte is shown in Table 59.

Table 59. I²C slave address byte

Bit	Slave address							
	7 MSB	6	5	4	3	2	1	0 LSB
	1	0	1	0	0	0	1	R/$\overline{W}$

The R/$\overline{W}$ bit defines the direction of the following single or multiple byte data transfer (read is logic 1, write is logic 0).

For the format and the timing of the START condition (S), the STOP condition (P), and the acknowledge bit (A) refer to the I²C-bus specification Ref. 13 "UM10204" and the characteristics table (Table 64). In the write mode a data transfer is terminated by sending either a STOP condition or the START condition of the next data transfer.

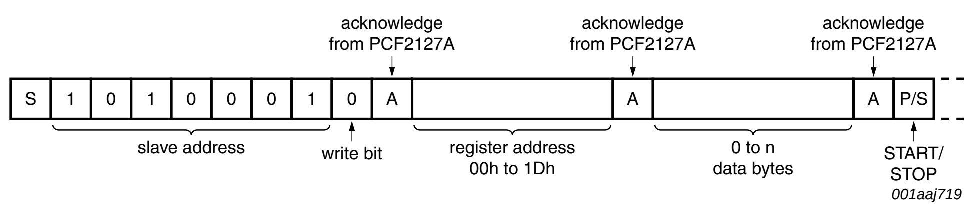


Fig 42. Bus protocol, writing to registers

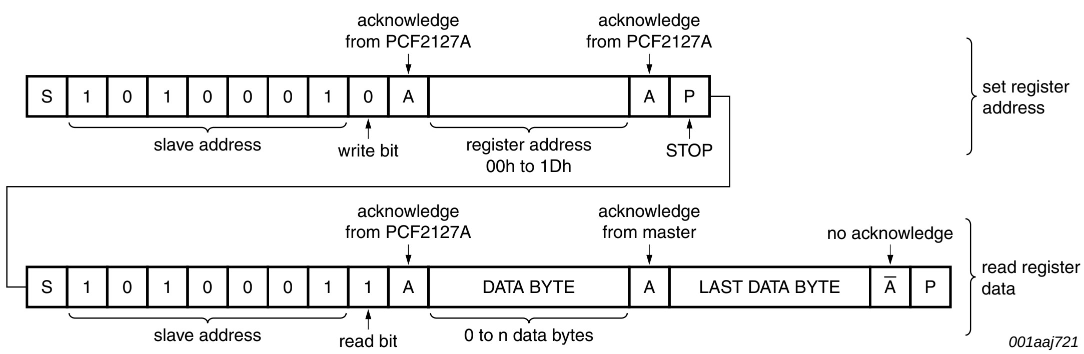


Fig 43. Bus protocol, reading from registers

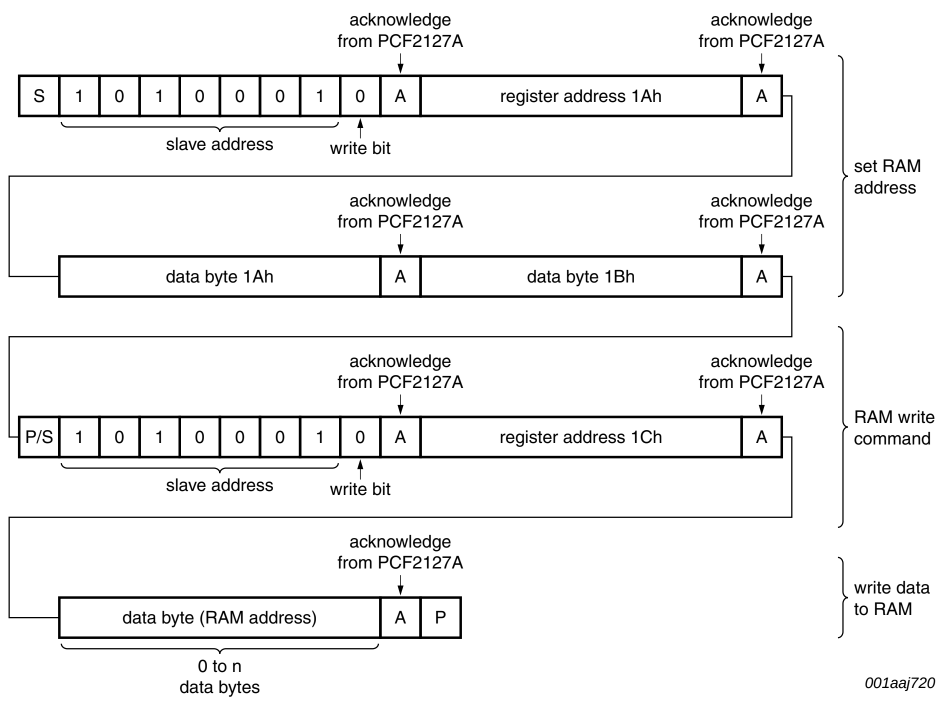


Fig 44. Bus protocol, writing to RAM

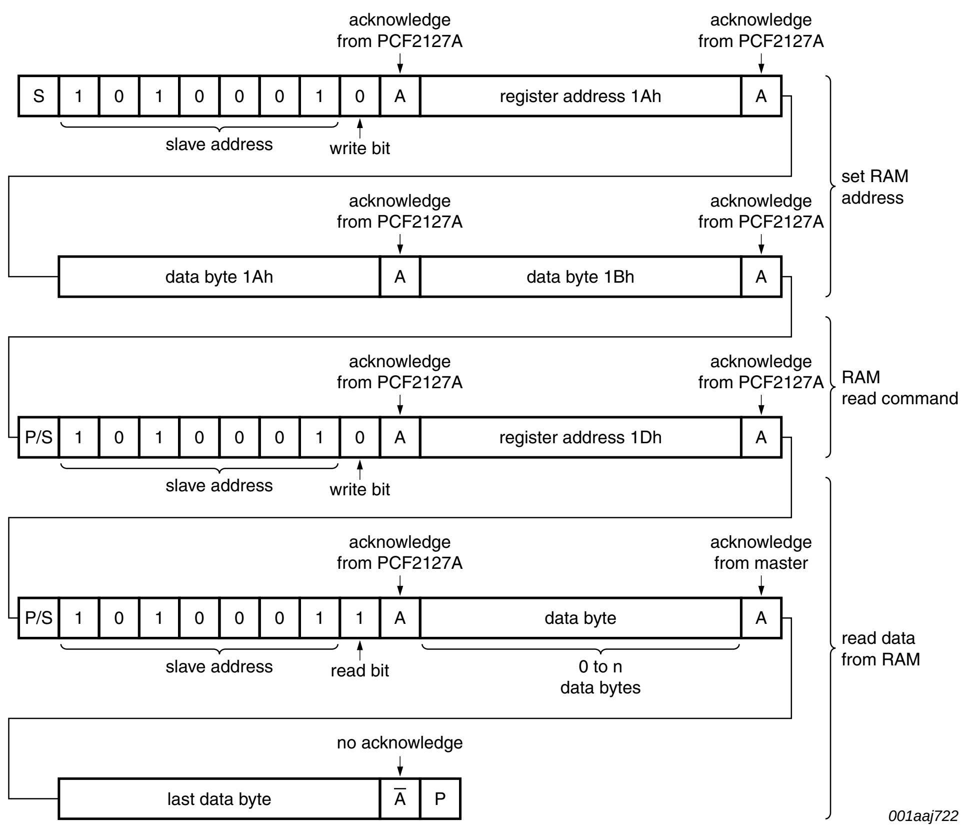


Fig 45. Bus protocol, reading from RAM

10. Internal circuitry

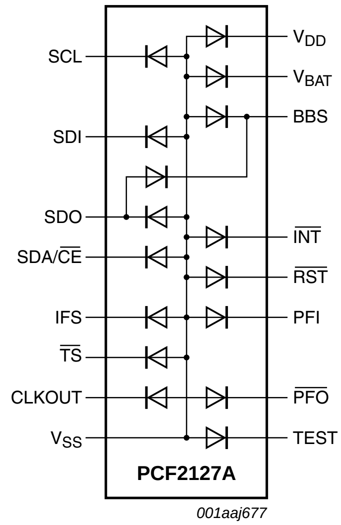


Fig 46. Device diode protection diagram of PCF2127A

11. Limiting values

Table 60. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+4.5	V
I_{DD}	supply current			–50	+50	mA
V_i	input voltage			–0.5	+6.5	V
I_I	input current			–10	+10	mA
V_O	output voltage			–0.5	+6.5	V
I_O	output current			–10	+10	mA
		at pin SDA		–10	+20	mA
V_{BAT}	battery supply voltage			–0.5	+4.5	V
P_{tot}	total power dissipation			-	300	mW
T_{amb}	ambient temperature			–40	+85	°C
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±3000	V
		MM	[2]	-	±250	V
		CDM	[3]	-	±1500	V
I_{lu}	latch-up current		[4]	-	200	mA
T_{stg}	storage temperature		[5]	–55	+85	°C

[1] Pass level; Human Body Model (HBM) according to Ref. 7 “JESD22-A114”.

[2] Pass level; Machine Model (MM), according to Ref. 8 “JESD22-A115”.

[3] Pass level; Charged-Device Model (CDM), according to Ref. 9 “JESD22-C101”.

[4] Pass level; latch-up testing according to Ref. 10 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[5] According to the NXP store and transport requirements (see Ref. 12 “NX3-00092”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long term storage products deviant conditions are described in that document.

12. Static characteristics

Table 61. Static characteristics

V_{DD} = 1.8 V to 4.2 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage		[1]	1.8	-	4.2	V
V_{BAT}	battery supply voltage			1.8	-	4.2	V
$V_{DD(cal)}$	calibration supply voltage			-	3.3	-	V
V_{low}	low voltage			-	1.2	-	V
I_{DD}	supply current	interface active					
		SPI-bus					
		f_{SCL} = 6.5 MHz		-	-	800	μA
		f_{SCL} = 1.0 MHz		-	-	200	μA
		I^2C-bus					
		f_{SCL} = 1.0 MHz		-	-	200	μA
		interface inactive (f_{SCL} = 0 Hz)					
		CLKOUT disabled (COF[2:0] = 111), one power supply V_{DD} (PWRMNG[2:0] = 111), timestamp detection disabled (TSOFF = 1)	[2]				
		V_{DD} = 2.0 V		-	500	-	nA
		V_{DD} = 3.3 V		-	700	1500	nA
		V_{DD} = 4.2 V		-	800	-	nA
		CLKOUT enabled at 32 kHz (default), one power supply V_{DD} (PWRMNG[2:0] = 111), timestamp detection disabled (TSOFF = 1)					
		V_{DD} = 2.0 V		-	600	-	nA
		V_{DD} = 3.3 V		-	850	-	nA
		V_{DD} = 4.2 V		-	1050	-	nA
		CLKOUT disabled (COF[2:0]) = 111), power management functions enabled (default), timestamp detection enabled (default)					
		V_{DD} = 2.0 V		-	1800	-	nA
		V_{DD} = 3.3 V		-	2150	-	nA
		V_{DD} = 4.2 V		-	2350	3500	nA
		CLKOUT enabled at 32 kHz (default); power management functions enabled (default), timestamp detection enabled (default)					
		V_{DD} = 2.0 V		-	1900	-	nA
		V_{DD} = 3.3 V		-	2300	-	nA
		V_{DD} = 4.2 V		-	2600	-	nA
I_{BAT}	battery supply current	V_{DD} active; V_{BAT} = 3.0 V		-	50	100	nA

Table 61. Static characteristics *...continued*

V_{DD} = 1.8 V to 4.2 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C, unless otherwise specified.

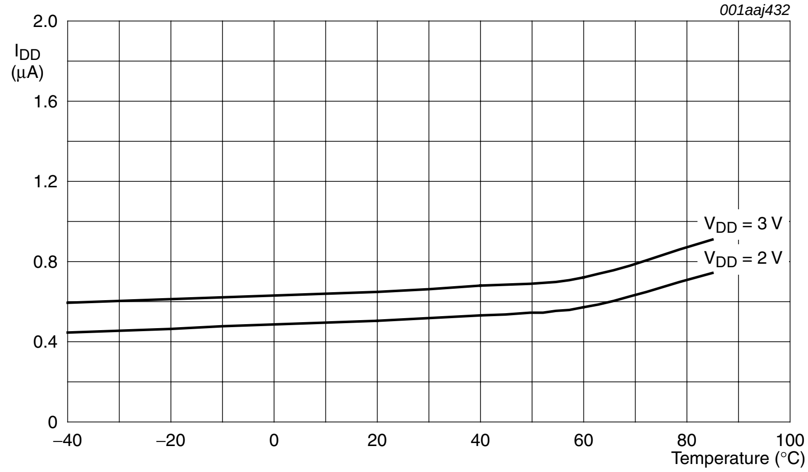
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power management						
$V_{th(sw)bat}$	battery switch threshold voltage		-	2.5	-	V
$V_{th(bat)low}$	low battery threshold voltage		-	2.5	-	V
$V_{th(PFI)}$	threshold voltage on pin PFI		-	1.25	-	V
Inputs						
V_I	input voltage		–0.5	-	V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage		-	-	$0.25V_{DD}$	V
		T_{amb} = –20 °C to +85 °C; V_{DD} > 2.0 V	-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	–1	0	+1	µA
C_i	input capacitance	[3]	-	-	7	pF
Outputs						
V_O	output voltage	on pins CLKOUT, $\overline{INT}$, $\overline{RST}$, $\overline{PFO}$, referring to external pull-up	–0.5	-	5.5	V
		on pin SDO	–0.5	-	V_{BBS} + 0.5	V
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD} = 4.2 V				
		on pin SDA	20	-	-	mA
		on all other outputs	1.0	-	-	mA
I_{OH}	HIGH-level output current	output source current; on pin SDO; V_{OH} = 3.8 V; V_{DD} = 4.2 V	1.0	-	-	mA
I_{LO}	output leakage current	$V_O = V_{DD}$ or V_{SS}	–1	0	1	µA

[1] For reliable oscillator start-up at power-on: $V_{DD(po)min} = V_{DD(min)} + 0.3$ V.

[2] Timer source clock = $\frac{1}{60}$ Hz, level of pins SDA/$\overline{CE}$, SDI and SCL is V_{DD} or V_{SS}.

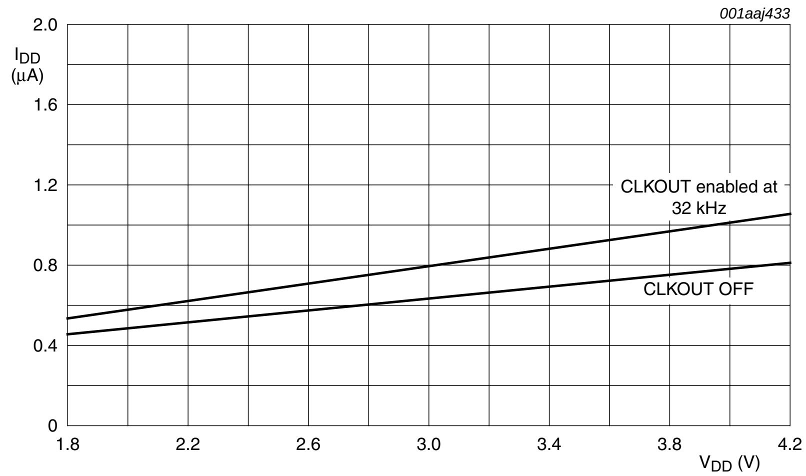
[3] Tested on sample basis.

12.1 Current consumption I_{DD} characteristics, typical

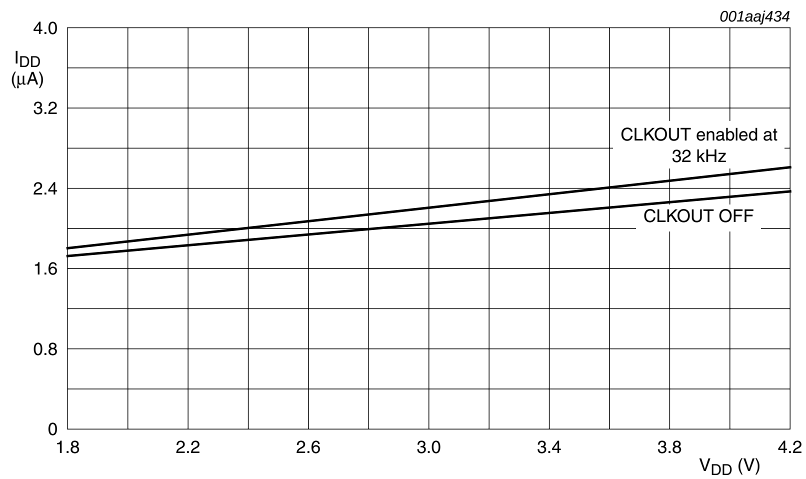


CLKOUT disabled; PWRMNG[2:0] = 111; TSOFF = 1; $\overline{TS}$ input floating.

Fig 47. I_{DD} as a function of temperature



a. PWRMNG[2:0] = 111; TSOFF = 1; T_{amb} = 25 °C; $\overline{TS}$ input floating.



b. PWRMNG[2:0] = 000; TSOFF = 0; T_{amb} = 25 °C; $\overline{TS}$ input floating.

Fig 48. I_{DD} as a function of V_{DD}

12.2 Frequency characteristics

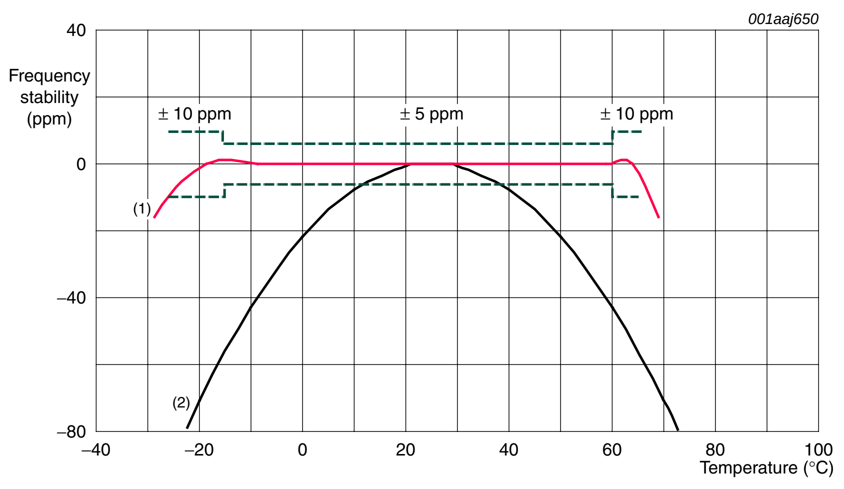
Table 62. Frequency characteristics

V_{DD} = 1.8 V to 4.2 V; V_{SS} = 0 V; T_{amb} = +25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_o	output frequency	on pin CLKOUT; V_{DD} or V_{BAT} = 3.3 V; COF[2:0] = 000; AO[3:0] = 1000		-	32.768	-	kHz
Δf/f	frequency stability	V_{DD} or V_{BAT} = 3.3 V					
		T_{amb} = –15 °C to +60 °C	[1]	-	±3	±5	ppm
		T_{amb} = –25 °C to –15 °C and T_{amb} = +60 °C to +65 °C	[1]	-	±5	±10	ppm
$\Delta f_{xtal}/f_{xtal}$	relative crystal frequency variation	crystal aging, first year; V_{DD} or V_{BAT} = 3.3 V	[2]	-	-	±3	ppm
Δf/ΔV	frequency variation with voltage	on pin CLKOUT		-	±1	-	ppm/V

[1] ±1 ppm corresponds to a time deviation of ±0.0864 seconds per day.

[2] Not production tested. Effects of reflow solder not included (see Ref. 3 “AN10857”).



(1) Temperature compensated frequency.

(2) Uncompensated typical tuning-fork crystal frequency.

Fig 49. Characteristic of frequency with respect to temperature

13. Dynamic characteristics

13.1 SPI-bus timing characteristics

Table 63. SPI-bus characteristics

V_{DD} = 1.8 V to 4.2V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C, unless otherwise specified. All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

Symbol	Parameter	Conditions	V_{DD} = 1.8 V		V_{DD} = 4.2 V		Unit
			Min	Max	Min	Max	
Pin SCL							
$f_{clk(SCL)}$	SCL clock frequency	register read/write access	-	2.0	-	6.5	MHz
		RAM write access	-	2.0	-	6.5	MHz
		RAM read access	-	1.11	-	6.25	MHz
t_{SCL}	SCL time	register read/write access	800	-	140	-	ns
		RAM write access	800	-	140	-	ns
		RAM read access	900	-	160	-	ns
$t_{clk(H)}$	clock HIGH time	register read/write access	100	-	70	-	ns
		RAM write access	100	-	70	-	ns
		RAM read access	450	-	80	-	ns
$t_{clk(L)}$	clock LOW time	register read/write access	400	-	70	-	ns
		RAM write access	400	-	70	-	ns
		RAM read access	450	-	80	-	ns
t_r	rise time	for SCL signal	-	100	-	30	ns
t_f	fall time	for SCL signal	-	100	-	30	ns
Pin $\overline{CE}$							
$t_{su(CE\_N)}$	CE_N set-up time		60	-	30	-	ns
$t_{h(CE\_N)}$	CE_N hold time		40	-	25	-	ns
$t_{rec(CE\_N)}$	CE_N recovery time		100	-	30	-	ns
$t_{w(CE\_N)}$	CE_N pulse width		-	0.99	-	0.99	s
Pin SDI							
t_{su}	set-up time	set-up time for SDI data	70	-	20	-	ns
t_h	hold time	hold time for SDI data	70	-	20	-	ns
Pin SDO							
$t_{d(R)SDO}$	SDO read delay time	C_L = 50 pF					
		register read access	-	225	-	55	ns
		RAM read access	-	410	-	55	ns
$t_{dis(SDO)}$	SDO disable time	[1]	-	90	-	25	ns
$t_{t(SDI-SDO)}$	transition time from SDI to SDO	to avoid bus conflict	0	-	0	-	ns

[1] No load value; bus will be held up by bus capacitance; use RC time constant with application values.

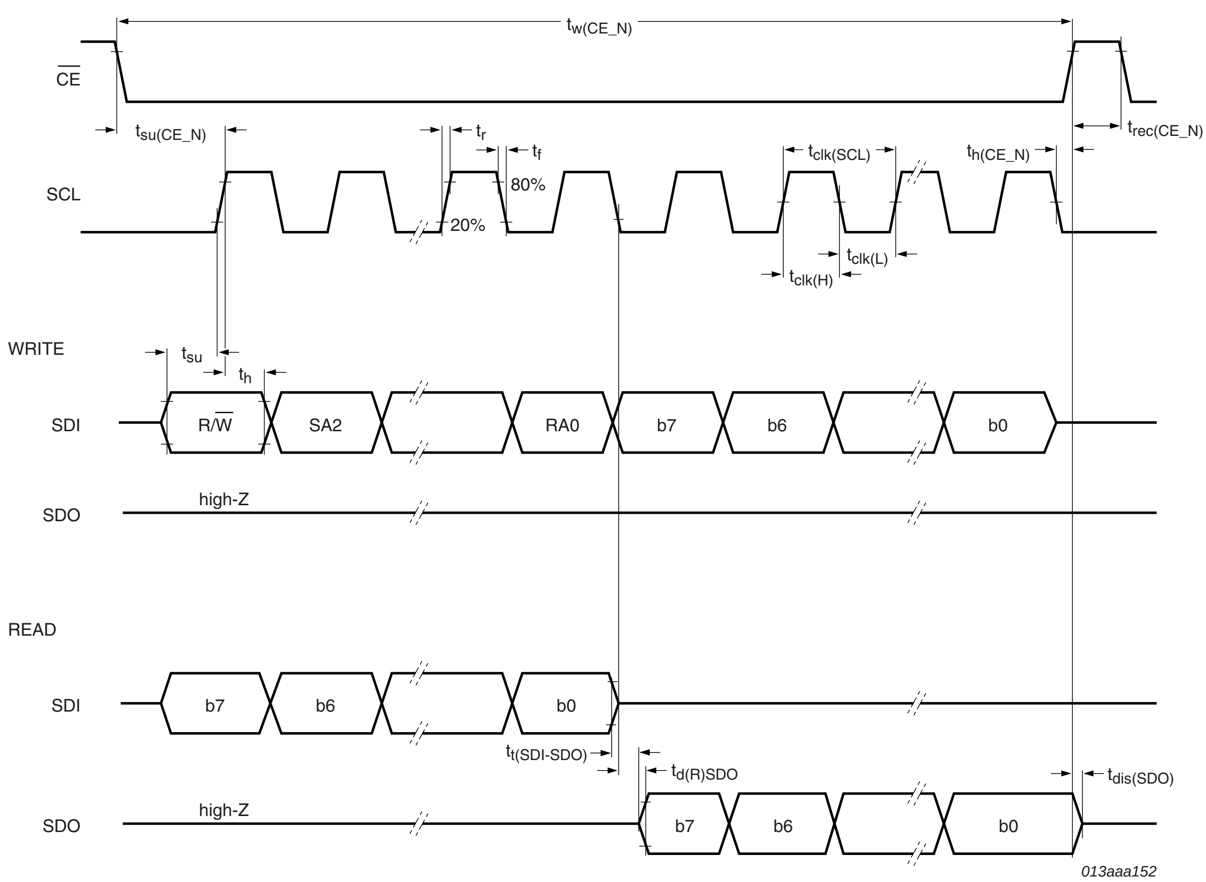


Fig 50. SPI-bus timing

13.2 I²C interface timing characteristics

Table 64. I²C-bus characteristics

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to 30 % and 70 % with an input voltage swing of V_{SS} to V_{DD} (see Figure 51).

Symbol	Parameter		Standard mode		Fast-mode (Fm)		Fast-mode Plus (Fm+)		Unit
			Min	Max	Min	Max	Min	Max	
Pin SCL									
f_{SCL}	SCL clock frequency	[1]	0	100	0	400	0	1000	kHz
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
Pin SDA									
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
Pins SCL and SDA									
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
t_r	rise time of both SDA and SCL signals	[2][3][4]	-	1000	$20 + 0.1C_b$	300	-	120	ns
t_f	fall time of both SDA and SCL signals	[2][3][4]	-	300	$20 + 0.1C_b$	300	-	120	ns
$t_{VD;ACK}$	data valid acknowledge time	[5]	0.1	3.45	0.1	0.9	0.05	0.45	µs
$t_{VD;DAT}$	data valid time	[6]	300	-	75	-	75	450	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[7]	-	50	-	50	-	50	ns

[1] The minimum SCL clock frequency is limited by the bus time-out feature which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25 ms. The bus time-out feature must be disabled for DC operation.

[2] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of the SCL's falling edge.

[3] C_b is the total capacitance of one bus line in pF.

[4] The maximum t_f for the SDA and SCL bus lines is 300 ns. The maximum fall time for the SDA output stage, t_f is 250 ns. This allows series protection resistors to be connected between the SDA pin, the SCL pin, and the SDA/SCL bus lines without exceeding the maximum t_f.

[5] $t_{VD;ACK}$ is the time of the acknowledgement signal from SCL LOW to SDA (out) LOW.

[6] $t_{VD;DAT}$ is the minimum time for valid SDA (out) data following SCL LOW.

[7] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

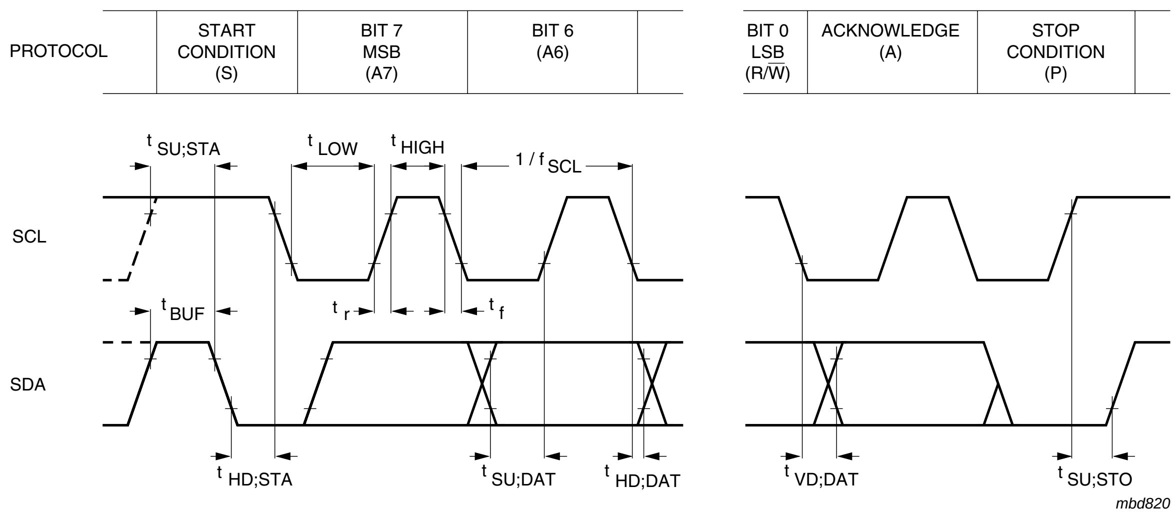


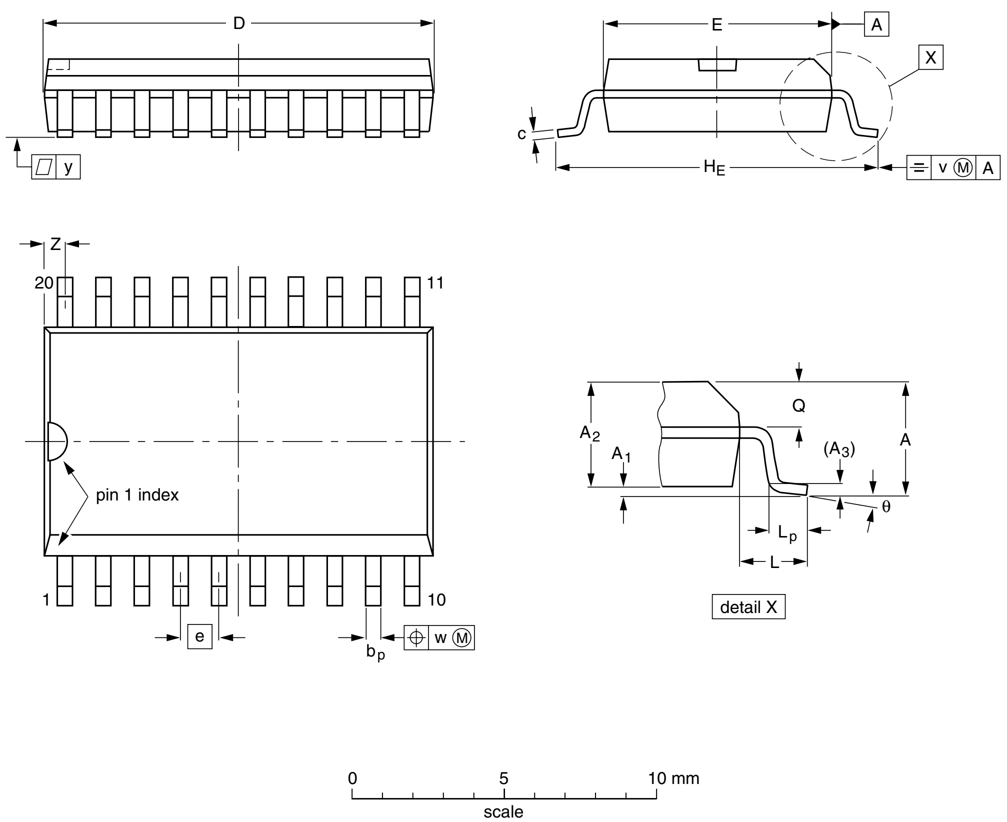
Fig 51. I²C-bus timing diagram; rise and fall times refer to 30 % and 70 %

14. Application information

For information about application configuration see Ref. 3 "AN10857".

15. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 52. Package outline SOT163-1 (SO20)

16. Soldering

For information about soldering see Ref. 3 “AN10857”.

17. Abbreviations

Table 65. Abbreviations

Acronym	Description
AM	Ante Meridiem
BCD	Binary Coded Decimal
CDM	Charged-Device Model
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
GPS	Global Positioning System
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
LSB	Least Significant Bit
MCU	Microcontroller Unit
MM	Machine Model
MSB	Most Significant Bit
PM	Post Meridiem
POR	Power-On Reset
PORO	Power-On Reset Override
PPM	Parts Per Million
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real Time Clock
SCL	Serial Clock Line
SDA	Serial DAta line
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TCXO	Temperature Compensated Crystal Oscillator

18. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **AN10853 —** Handling precautions of ESD sensitive devices

[3] **AN10857 —** Application and soldering information for PCF2127A and PCF2129A TCXO RTC

[4] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[5] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[6] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[7] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[8] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[9] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[10] **JESD78 —** IC Latch-Up Test

[11] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[12] **NX3-00092 —** NXP store and transport requirements

[13] **UM10204 —** I^2C-bus specification and user manual

19. Revision history

Table 66. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF2127A_1	20100121	Product data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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