MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC68HC001

Technical Summary

Low Power HCMOS 8-/16-/32-Bit Microprocessor

This document contains both a summary of the MC68HC001 and a detailed set of parametric specifications. For complete information refer to the M68000 UM/AD, *M68000 8-/16-/32-Bit Microprocessors User's Manual.*

The MC68HC001 provides a functional extension to the MC68HC000 HCMOS 16-/32-bit microprocessor with the addition of statically selectable 8- or 16-bit data bus operation. The MC68HC001 is object-code compatible with the MC68HC000, and code written for the MC68HC001 can be migrated without modification to any member of the M68000 Family. This is possible because the user programming model is identical for all members of the M68000 Family and the instruction sets are proper subsets for the complete architecture. The following resources are available to the MC68HC001 user:

- 17 32-Bit Data and Address Registers
- 16-Mbyte Direct Addressing Range
- 56 Powerful Instruction Types
- Operations on Five Main Data Types
- Memory-Mapped I/O
- 14 Addressing Modes

INTRODUCTION

As shown in the user programming model (see Figure 1), the MC68HC001 offers 16 32-bit registers and a 32-bit program counter. The first eight registers (D7–D0) are used as data registers for byte (8-bit), word (16-bit), and long-word (32-bit) operations. The second set of seven registers (A6–A0) and the user stack pointer (USP) can be used as software stack pointers and base address registers. In addition, the registers can be used for word and long-word operations. All 16 registers can be used as index registers.

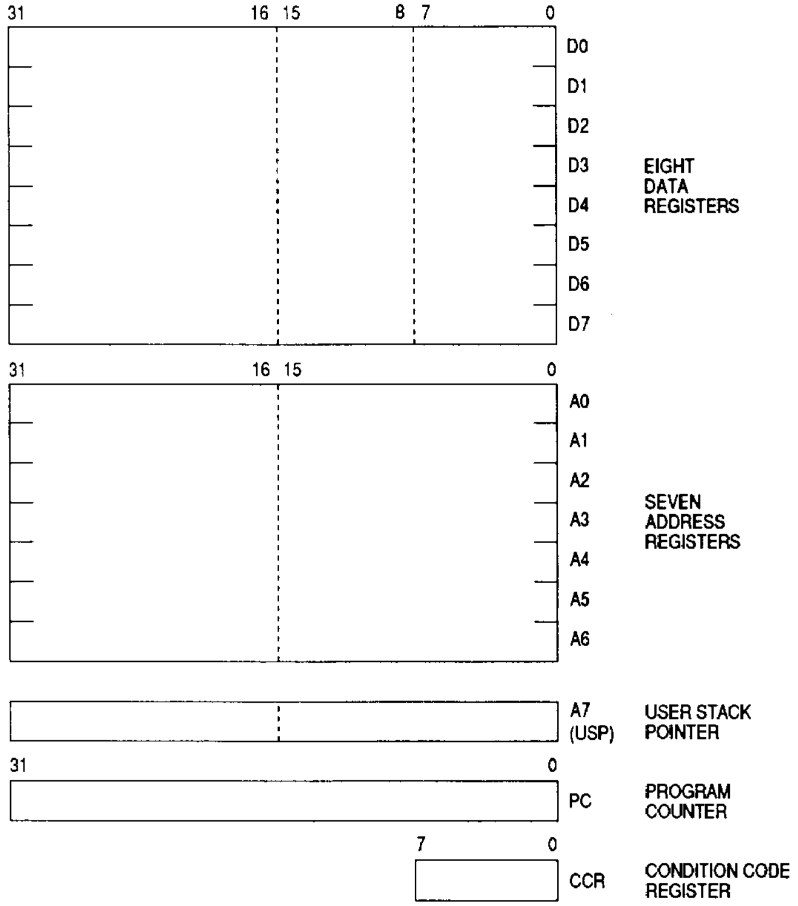


Figure 1. User Programming Model

In supervisor mode (see Figure 2), the upper byte of the status register and the supervisor stack pointer (SSP) are also available to the programmer.

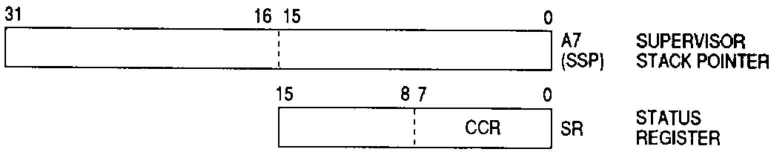


Figure 2. Supervisor Programming Model Supplement

The status register (see Figure 3) contains the interrupt mask (eight levels available) as well as the condition codes: extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and in a supervisor (S) or user state.

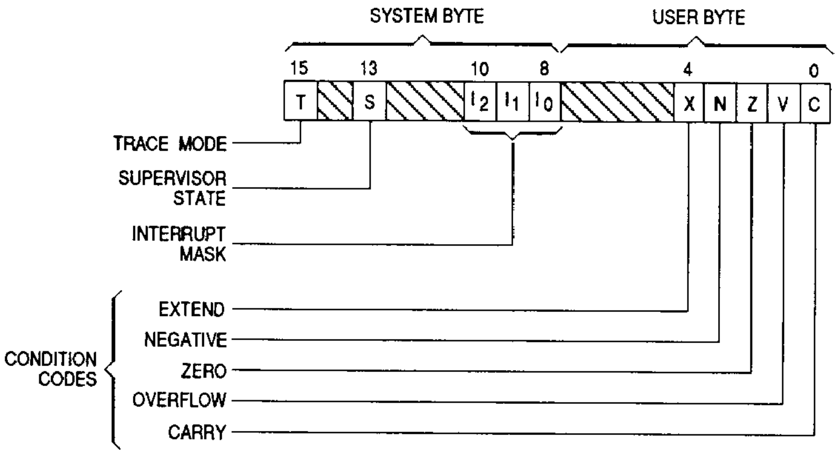


Figure 3. Status Register

DATA TYPES AND ADDRESSING MODES

Five basic data types are supported:

1. Bits
2. BCD Digits (4 Bits)
3. Bytes (8 Bits)
4. Words (16 Bits)
5. Long Words (32 Bits)

In addition, operations on other data types, such as memory addresses, status word data, etc., are provided in the instruction set.

The 14 addressing modes, listed in Table 1, include six basic types:

1. Register Direct
2. Register Indirect
3. Absolute
4. Program Counter Relative
5. Immediate
6. Implied

Included in the register indirect addressing modes is the capability to perform postincrementing, predecrementing, offsetting, and indexing. The program counter relative mode can also be modified via indexing and offsetting.

Table 1. Addressing Modes

Addressing Modes	**Syntax**
Register Direct Addressing	
Data Register Direct	Dn
Address Register Direct	An
Absolute Data Addressing	
Absolute Short	xxx.W
Absolute Long	xxx.L
Program Counter Relative Addressing	
Relative with Offset	d_{16}(PC)
Relative with Index Offset	d_8(PC,Xn)
Register Indirect Addressing	
Register Indirect	(An)
Postincrement Register Indirect	(An) +
Predecrement Register Indirect	− (An)
Register Indirect with Offset	d_{16}(An)
Indexed Register Indirect with Offset	d_8(An,Xn)
Immediate Data Addressing	
Immediate	#xxx
Quick Immediate	#1r#8
Implied Addressing	
Implied Register	SR/USP/SP/PC

NOTES:

Dn = Data Register
An = Address Register
Xn = Address of Data Register Used as Index Register
SR = Status Register
PC = Program Counter
SP = Stack Pointer
USP = User Stack Pointer
( ) = Effective Address
d_8 = 8-Bit Offset (Displacement)
d_{16} = 16-Bit Offset (Displacement)
#xxx = Immediate Data

INSTRUCTION SET OVERVIEW

The MC68HC001 instruction set is listed in Table 2. Additional instructions that are variations or subsets of these instructions are listed in Table 3. Special emphasis is given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words, and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned, multiply and divide, quick arithmetic operations, BCD arithmetic, and expanded operations (through traps). For detailed information on the MC68HC001 instruction set, refer to M68000 PM/AD, *M68000 Programmer's Reference Manual.*

Table 2. Instruction Set Summary

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
AND	Logical AND
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
Bcc	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register against Bounds
CLR	Clear Operand
CMP	Compare
DBcc	Test Condition, Decrement and Branch
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive OR
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NOP	No Operation
NOT	Ones Complement
OR	Logical OR
PEA	Push Effective Address
RESET	Reset External Devices
ROL	Rotate Left without Extend
ROR	Rotate Right without Extend
ROXL	Rotate Left with Extend
ROXR	Rotate Right with Extend
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditional
STOP	Stop
SUB	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink

Table 3. Variations of Instruction Types

Instruction Type	Variation	Description
ADD	ADD ADDA ADDQ ADDI ADDX	Add Add Address Add Quick Add Immediate Add with Extend
AND	AND ANDI ANDI to CCR ANDI to SR	Logical AND And Immediate And Immediate to Condition Codes And Immediate to Status Register
CMP	CMP CMPA CMPM CMPI	Compare Compare Address Compare Memory Compare Immediate
EOR	EOR EORI EORI to CCR EORI to SR	Exclusive OR Exclusive OR Immediate Exclusive OR Immediate to Condition Codes Exclusive OR Immediate to Status Register
MOVE	MOVE MOVEA MOVEM MOVEP MOVEQ MOVE from SR MOVE to SR MOVE to CCR MOVE USP	Move Move Address Move Multiple Registers Move Peripheral Data Move Quick Move from Status Register Move to Status Register Move to Condition Codes Move User Stack Pointer
NEG	NEG NEGX	Negate Negate with Extend
OR	OR ORI ORI to CCR ORI to SR	Logical OR OR Immediate OR Immediate to Condition Codes OR Immediate to Status Register
SUB	SUB SUBA SUBI SUBQ SUBX	Subtract Subtract Address Subtract Immediate Subtract Quick Subtract with Extend

SIGNAL DESCRIPTION

The input and output signals are illustrated functionally in Figure 4 and are described in the following paragraphs.

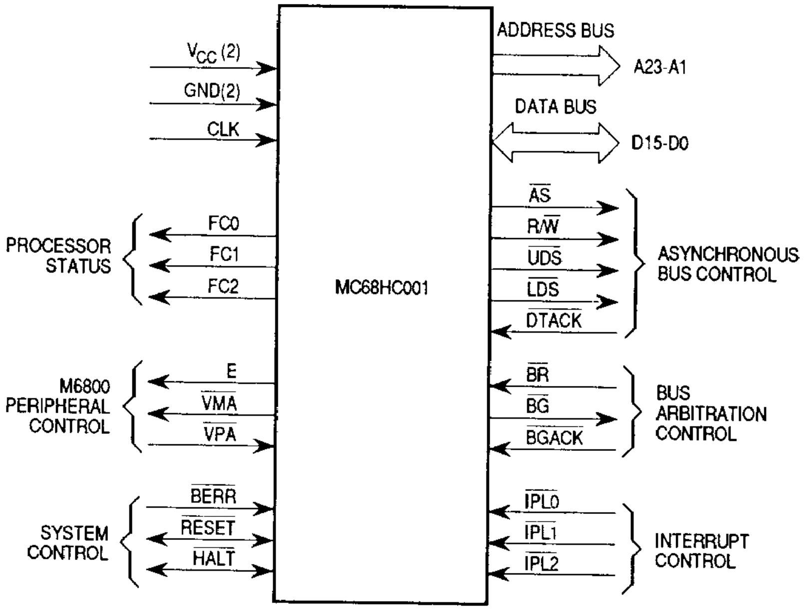


Figure 4. Functional Signal Groups

MODE (MODE)

The MODE input selects between the 8- and 16-bit operating modes. If this input is grounded at reset, the processor will come out of reset in the 8-bit mode. If this input is tied high or floating at reset, the processor will come out of reset in the 16-bit mode. This input should be changed only at reset and must be stable two clocks after $\overline{\text{RESET}}$ is negated. Changing this input during normal operation may produce unpredictable results.

ADDRESS BUS (A23–A0)

This 24-bit, unidirectional, three-state bus is capable of addressing 16 Mbytes of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A3, A2, and A1 reflect the level of the interrupt being serviced while address lines A23–A4 and A0 are set to a logic high.

DATA BUS (D15–D0)

This 16-bit, bidirectional, three-state bus is the general-purpose data path. If the processor is operating in the 16-bit mode, the data bus transfers and accepts data in either word or byte length. If the processor is operating in the 8-bit mode, the processor drives the entire bus during writes, but only the lower eight bits (D7–D0) contain valid data. In the 8-bit mode, the processor ignores the data on data lines D15–D8 during read cycles. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D7–D0.

ASYNCHRONOUS BUS CONTROL

Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge.

Address Strobe ($\overline{\text{AS}}$)

This signal indicates a valid address on the address bus.

Read/Write (R/$\overline{\text{W}}$)

This signal defines the data bus transfer as a read or write cycle. R/$\overline{\text{W}}$ also works in conjunction with the data strobes as explained in the following paragraph.

Upper and Lower Data Strobe ($\overline{\text{UDS}}$, $\overline{\text{LDS}}$)

These signals control the flow of data on the data bus, as listed in Table 4. When R/$\overline{\text{W}}$ is high, the processor will read from the data bus as indicated. When R/$\overline{\text{W}}$ is low, the processor will write to the data bus as shown. During operation in the 8-bit mode, the $\overline{\text{UDS}}$ is always forced high.

Table 4. Data Strobe Control of Data Bus for 16-Bit Mode

$\overline{\text{UDS}}$	$\overline{\text{LDS}}$	R/$\overline{\text{W}}$	D15–D8	D7–D0
1	1	—	No Valid Data	No Valid Data
0	0	1	Valid Data Bits 15–8	Valid Data Bits 7–0
1	0	1	No Valid Data	Valid Data Bits 7–0
0	1	1	Valid Data Bits 15–8	No Valid Data
0	0	0	Valid Data Bits 15–8	Valid Data Bits 7–0
1	0	0	Valid Data Bits 7–0*	Valid Data Bits 7–0
0	1	0	Valid Data Bits 15–8	Valid Data Bits 15–8*

*These conditions are a result of current implementation and may not appear on future devices.

Data Transfer Acknowledge ($\overline{\text{DTACK}}$)

This input indicates that the data transfer is complete. When the processor recognizes $\overline{\text{DTACK}}$ during a read cycle, data is latched and the bus cycle is terminated. When $\overline{\text{DTACK}}$ is recognized during a write cycle, the bus cycle is terminated.

BUS ARBITRATION CONTROL

Bus request, bus grant, and bus grant acknowledge form a bus arbitration circuit to determine which device will be the bus master device.

Bus Grant ($\overline{\text{BG}}$)

This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

Bus Grant Acknowledge ($\overline{\text{BGACK}}$)

This input indicates that some other device has become the bus master. This signal should not be asserted until the following four conditions are met:

1. A bus grant has been received.
2. Address strobe is inactive, which indicates that the microprocessor is not using the bus.
3. Data transfer acknowledge is inactive, which indicates that neither memory nor peripherals are using the bus.
4. Bus grant acknowledge is inactive, which indicates that no other device is still claiming bus mastership.

INTERRUPT CONTROL ($\overline{\text{IPL2}}$, $\overline{\text{IPL1}}$, $\overline{\text{IPL0}}$)

These inputs indicate the encoded priority level of the device requesting an interrupt. Level 7 is the highest priority; whereas, level 0 indicates that no interrupts are requested. Level 7 cannot be masked. The least significant bit is given in $\overline{\text{IPL0}}$, and the most significant bit is contained in $\overline{\text{IPL2}}$. These lines must remain stable until the processor signals interrupt acknowledge (FC2–FC0 are all high) to ensure that the interrupt is recognized.

SYSTEM CONTROL

The three system control inputs are used to reset or halt the processor and to indicate to the processor that bus errors have occurred.

Bus Error ($\overline{\text{BERR}}$)

This input informs the processor that there is a problem with the bus cycle currently being executed. Problems may be a result of:

- Nonresponding devices,
- Interrupt vector number acquisition failure,
- Illegal access request as determined by a memory management unit, or
- Other application-dependent errors.

The bus error signal interacts with the halt signal to determine if the current bus cycle should be re-executed or if exception processing should be performed.

Reset ($\overline{\text{RESET}}$)

This bidirectional signal resets (starts a system initialization sequence) the processor in response to an external reset signal. An internally generated reset (result of a RESET instruction) causes all external devices to be reset, and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ signals applied simultaneously.

Halt ($\overline{\text{HALT}}$)

When this bidirectional line is driven by an external device, it causes the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive, and all three-state lines are put in their high-impedance state.

When the processor stops executing instructions, such as in a double bus fault condition, the $\overline{\text{HALT}}$ line is driven by the processor to indicate to external devices that the processor has stopped.

M6800 PERIPHERAL CONTROL

These control signals are used to interface synchronous M6800 peripheral devices with the asynchronous MC68HC001.

Enable (E)

This signal is the standard enable signal common to all M6800-type peripheral devices. The period for this output is 10 MC68HC001 clock periods (six clocks low, four clocks high). Enable is generated by an internal ring counter that may come up in any state (i.e., at power-on, it is impossible to guarantee phase relationship of E to CLK). E is a free-running clock and runs regardless of the state of the bus on the MPU.

Valid Peripheral Address ($\overline{\text{VPA}}$)

This input indicates that the device or region addressed is an M6800 Family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt during an interrupt acknowledge cycle.

Valid Memory Address ($\overline{\text{VMA}}$)

This output is used to indicate to M6800 peripheral devices that a valid address exists on the address bus and that the processor is synchronized to enable. This signal only responds to a valid peripheral address ($\overline{\text{VPA}}$) input, which indicates that the peripheral is an M6800 Family device.

PROCESSOR STATUS (FC2, FC1, FC0)

These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed (see Table 5). The information indicated by the function code outputs is valid whenever address strobe ($\overline{\text{AS}}$) is active.

Table 5. Function Code Outputs

Function Code Output			Cycle Time
FC2	FC1	FC0	
0	0	0	(Undefined, Reserved)
0	0	1	User Data
0	1	0	User Program
0	1	1	(Undefined, Reserved)
1	0	0	(Undefined, Reserved)
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	Interrupt Acknowledge

CLOCK (CLK)

The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input should not be gated off at any time, and the clock signal must conform to minimum and maximum pulse-width times. The clock is a constant frequency square wave with no stretching or shaping techniques required.

DATA TRANSFER OPERATIONS

The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing the acknowledge and data signals from the slave device.

The MC68HC001 operates in either of two modes: an 8- or 16-bit mode. The following paragraphs explain the read, write, and read-modify-write cycles for each of the modes.

16-BIT MODE

Transfer of data between devices involves the following signals:

- Address Bus A23–A1
- Data Bus D15–D0
- Control Signals

During operation in the 16-bit mode, the A0 bit is always forced to a logic high.

Read Cycle

During a read cycle, the processor receives data from a memory or a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or long-word) operation, the processor reads both upper and lower bytes simultaneously by asserting both upper and lower data strobes. When the instruction specifies byte operation, the processor uses an internal A0 bit to determine which byte to read and then issues the data strobe required for that byte. For byte operations, when the internal A0 bit equals zero, the upper data strobe is issued. When the internal A0 bit equals one, the lower data strobe is issued. When the data is received, the processor correctly positions it internally.

Write Cycle

During a write cycle, the processor sends data to either a memory or a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word (or long-word) operation, the processor writes both upper and lower bytes simultaneously by asserting both upper and lower data strobes. When the instruction specifies byte operation, the processor uses an internal A0 bit to determine which byte to write and then issues the data strobe required for that byte. For byte operation, when A0 equals zero, the upper data strobe is issued. When A0 equals one, the lower data strobe is issued.

Read-Modify-Write Cycle

The indivisible read-modify-write cycle is the method used by the MC68HC001 for interlocked multiprocessor communications. This cycle is the same for both 8- and 16-bit modes. The read-modify-write cycle performs a read, modifies the data in the arithmetic logic unit, and writes the data back to the same address. In the MC68HC001, this cycle is indivisible in that the address strobe is asserted throughout the entire read-modify-write cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. TAS is the only instruction that uses the read-modify-write cycle; since TAS only operates on bytes, all read-modify-write cycles are byte operations.

8-BIT MODE

Transfer of data between devices involves the following signals:

- Address Bus A23–A0
- Data Bus D7–D0
- Control Signals

During operation in the 8-bit mode, the upper data strobe ($\overline{\text{UDS}}$) is always forced high, and data lines D15–D8 are undefined.

Read Cycle

During a read cycle, the processor receives data from a memory or a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or long-word) operation, the processor reads both bytes. When the instruction specifies byte operation, the processor uses the A0 bit to determine which byte to read and then issues the required data strobe.

Write Cycle

During a write cycle, the processor sends data to either a memory or a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word (or long-word) operation, the processor writes both bytes. When the instruction specifies byte operation, the processor uses the A0 bit to determine which byte to write and then issues the required data strobe.

Read-Modify-Write Cycle

The read-modify-write cycle operates the same for both 8- and 16-bit modes. Refer to **Read-Modify-Write Cycle** for the 16-bit mode of operation.

PROCESSING STATES

The MC68HC001 is always in one of three processing states: normal, exception, or halted.

NORMAL PROCESSING

The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands and to store results. A special case of the normal state is the stopped state, which the processor enters when a stop instruction is executed. In this state, no further references are made.

EXCEPTION PROCESSING

The exception processing state is associated with interrupts, trap instructions, tracing, and other exception conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, a bus error, or a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

HALTED PROCESSING

The halted processing state is an indication of catastrophic hardware failure. For example, if, during the exception processing of a bus error, another bus error occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

INTERFACE WITH M6800 PERIPHERALS

Motorola's extensive line of M6800 peripherals are directly compatible with the MC68HC001. Some devices that are particularly useful are as follows:

MC6821	Peripheral Interface Adapter
MC6840	Programmable Timer Module
MC6843	Floppy Disk Controller
MC6845	CRT Controller
MC6850	Asynchronous Communications Interface Adapter
MC6854	Advanced Data Link Controller

To interface the synchronous M6800 peripherals with the asynchronous MC68HC001, the processor modifies its bus cycle to meet the M6800 cycle requirements whenever an M6800 device address is detected. This modification is possible since both the processors use memory-mapped I/O.

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +6.5	V
Input Voltage	V_{in}	−0.3 to +6.5	V
Operating Temperature Range	T_A	T_L to T_H 0 to 70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to the appropriate logic voltage level (e.g., either GND or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Symbol	Value	Rating
Thermal Resistance (Still Air) Plastic, Type FN	θ_{JA}	45	θ_{JC}	25*	°C/W

*Estimated

CMOS CONSIDERATIONS

The MC68HC001, with its significantly lower power consumption, has other considerations. The CMOS cell is basically composed of two complementary transistors (a P channel and an N channel), and only one transistor is turned on while the cell is in the steady state. The active P-channel transistor sources current when the output is a logic high and presents a high impedance when the output is a logic low. Thus, the overall result is extremely low power consumption because no power is lost through the active P-channel transistor. Also, since only one transistor is turned on during the steady state, power consumption is determined by leakage currents.

Because the basic CMOS cell is composed of two complementary transistors, a virtual semiconductor controlled rectifier (SCR) may be formed when an input exceeds the supply voltage. The SCR that is formed by this high input causes the device to become latched in a mode that may result in excessive current drain and eventual destruction of the device. Although the MC68HC001 is implemented with input protection diodes, care should be exercised to ensure that the maximum input voltage specification is not exceeded. Some systems may require that the CMOS circuitry be isolated from voltage transients; others may require no additional circuitry.

The MC68HC001, implemented in CMOS, is applicable to designs for which the following considerations are relevant:

1. The MC68HC001 completely satisfies the input/output drive requirements of CMOS logic devices.
2. The HCMOS MC68HC001 provides an order of magnitude reduction in power dissipation when compared to the HMOS MC68000. However, the MC68HC001 does not offer a power-down mode. The minimum operating frequency of the MC68HC001 is 4 MHz.

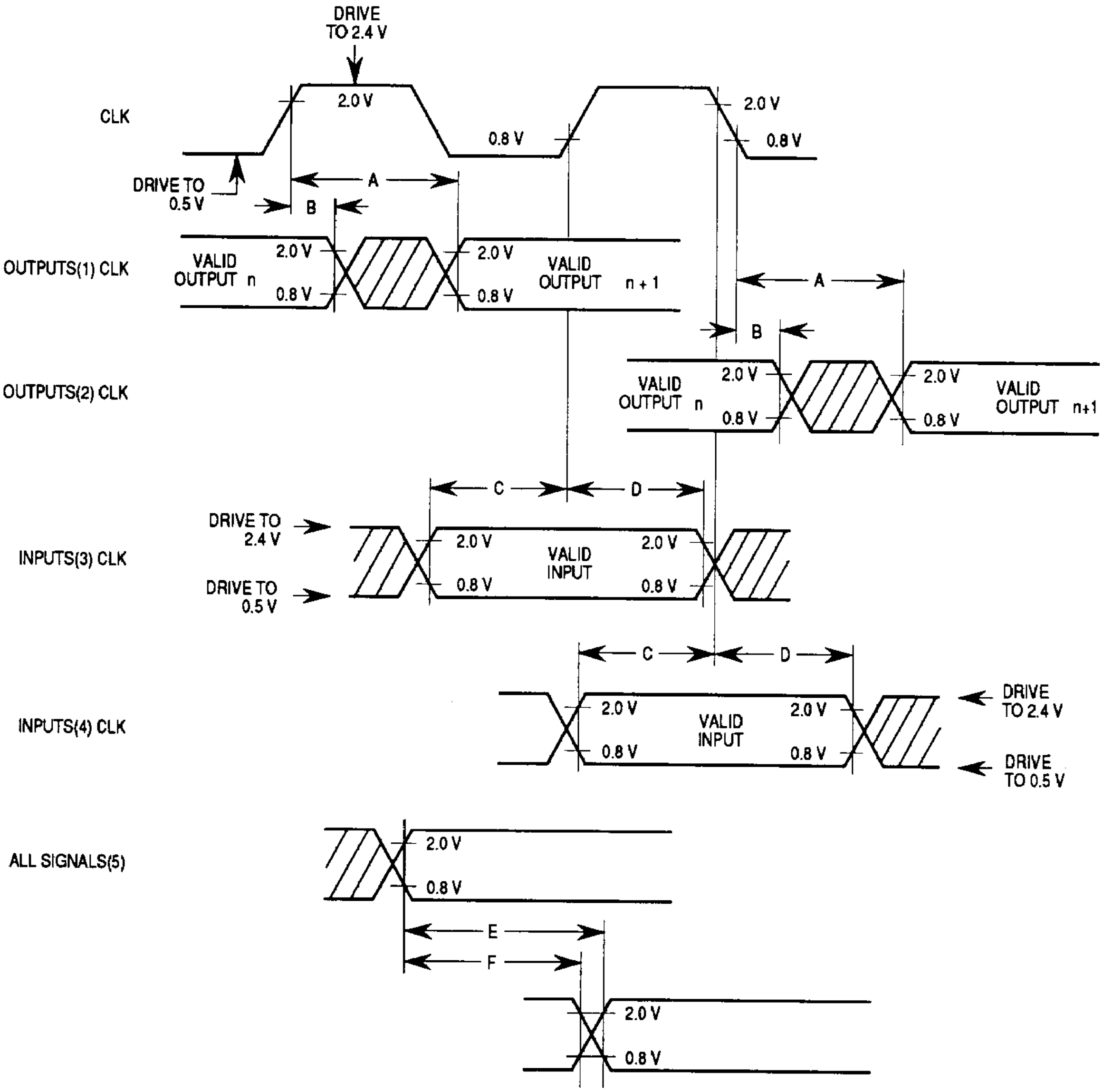
AC ELECTRICAL SPECIFICATION DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock and possibly to one or more other signals.

The measurement of the AC specifications is defined by the waveforms shown in Figure 5. To test the parameters guaranteed by Motorola, inputs must be driven to the voltage levels specified in that figure. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown in Figure 5. Inputs are specified with minimum setup and hold times, and are measured as shown. Finally, the measurement for signal-to-signal specifications is also shown.

NOTE

The testing levels used to verify conformance to the AC specifications do not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.



NOTES:

1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:

A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

Figure 5. Drive Levels and Test Points for AC Specifications

DC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H)

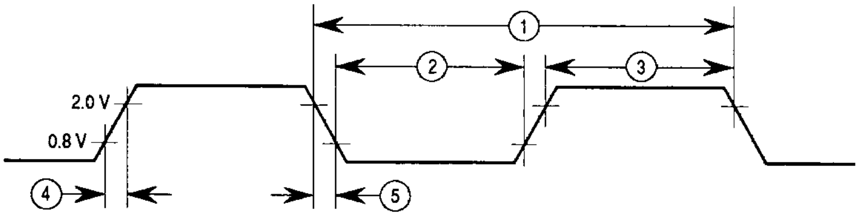
Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	V
Input Low Voltage	V_{IL}	GND − 0.3	0.8	V
Input Leakage Current $\overline{\mathrm{BERR}}$, $\overline{\mathrm{BGACK}}$, $\overline{\mathrm{BR}}$, $\overline{\mathrm{DTACK}}$, CLK, $\overline{\mathrm{IPL2}}$–$\overline{\mathrm{IPL0}}$, $\overline{\mathrm{VPA}}$ @ 5.25 V $\overline{\mathrm{HALT}}$, $\overline{\mathrm{RESET}}$	I_{in}	— —	2.5 20	μA
Three-State (Off State) Input Current $\overline{\mathrm{AS}}$, A23–A1, D15–D0, @ 2.4 V/0.4 V FC2–FC0, $\overline{\mathrm{LDS}}$, R/$\overline{\mathrm{W}}$, $\overline{\mathrm{UDS}}$, $\overline{\mathrm{VMA}}$	I_{TSI}	—	20	μA
Output High Voltage E, $\overline{\mathrm{AS}}$, A23–A1, $\overline{\mathrm{BG}}$, D15–D0, (I_{OH} = −400 μA) FC2–FC0, $\overline{\mathrm{LDS}}$, R/$\overline{\mathrm{W}}$, $\overline{\mathrm{UDS}}$, $\overline{\mathrm{VMA}}$	V_{OH}	V_{CC} −0.75	—	V
Output Low Voltage (I_{OL} = 1.6 mA) $\overline{\mathrm{HALT}}$ (I_{OL} = 3.2 mA) A23–A1, $\overline{\mathrm{BG}}$, FC2–FC0 (I_{OL} = 5.0 mA) $\overline{\mathrm{RESET}}$ (I_{OL} = 5.3 mA) E, $\overline{\mathrm{AS}}$, D15–D0, $\overline{\mathrm{LDS}}$, R/$\overline{\mathrm{W}}$, $\overline{\mathrm{UDS}}$, $\overline{\mathrm{VMA}}$	V_{OL}	 — — — —	 0.5 0.5 0.5 0.5	V
Current Dissipation* f = 8 MHz f = 10 MHz f = 12.5 MHz f = 16.67 MHz	I_D	— — —	25 30 35 50	mA
Power Dissipation f = 8 MHz f = 10 MHz f = 12.5 MHz f = 16.67 MHz	P_D	— — —	0.13 0.16 0.19 0.26	W
Capacitance (V_{in} = 0 V, T_A = 25°C, Frequency = 1 MHz)**	C_{in}	—	20.0	pF
Load Capacitance $\overline{\mathrm{HALT}}$ All Others	C_L	— —	70 130	pF

*Currents listed are with no loading.

**Capacitance is periodically sampled rather than 100% tested.

AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING (See Figure 6)

Num.	Characteristic	Symbol	8 MHz		10 MHz		12.2 MHz		16.67 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
	Frequency of Operation	f	4.0	8.0	4.0	10.0	4.0	12.5	4.0	16.67	MHz
1	Cycle Time	t_{cyc}	125	250	100	250	80	250	60	125	ns
2,3	Clock Pulse Width	t_{CL} t_{CH}	55 55	125 125	45 45	125 125	35 35	125 125	27 27	62.5 62.5	ns
4,5	Clock Rise and Fall Times	t_{Cr} t_{Cf}	— —	10 10	— —	10 10	— —	5 5	— —	5 5	ns



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 V and 2.0 V.

Figure 6. Clock Input Timing

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

(V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H; see Figures 7 and 8)

Num.	Characteristic	Symbol	8 MHz		10 MHz		12.5 MHz		16.67 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
6	Clock Low to Address Valid	t_{CLAV}	—	62	—	50	—	50	—	30	ns
6A	Clock High to FC Valid	t_{CHFCV}	—	62	—	50	—	45	0	30	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	t_{CHADZ}	—	80	—	70	—	60	—	50	ns
8	Clock High to Address, FC Invalid (Minimum)	t_{CHAFI}	0	—	0	—	0	—	0	—	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Asserted	t_{CHSL}	3	60	3	50	3	40	3	30	ns
11[2]	Address Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read)/$\overline{AS}$ Asserted (Write)	t_{AVSL}	30	—	20	—	15	—	15	—	ns
11A[2]	FC Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read)/ $\overline{AS}$ Asserted (Write)	t_{FCVSL}	90	—	70	—	60	—	45	—	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	t_{CLSH}	—	62	—	50	—	40	3	30	ns
13[2]	$\overline{AS}$, $\overline{DS}$ Negated to Address, FC Invalid	t_{SHAFI}	40	—	30	—	20	—	15	—	ns
14[2]	$\overline{AS}$ (and $\overline{DS}$ Read) Width Asserted	t_{SL}	270	—	195	—	160	—	120	—	ns
14A[2]	$\overline{DS}$ Width Asserted (Write)	t_{DSL}	140	—	95	—	80	—	60	—	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width Negated	t_{SH}	150	—	105	—	65	—	60	—	ns
16	Clock High to Control Bus High Impedance	t_{CHCZ}	—	80	—	70	—	60	—	50	ns
17[2]	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid	t_{SHRH}	40	—	30	—	20	—	15	—	ns
18[1]	Clock High to R/$\overline{W}$ High (Read)	t_{CHRH}	0	55	0	45	0	40	0	30	ns
20[1]	Clock High to R/$\overline{W}$ Low (Write)	t_{CHRL}	0	55	0	45	0	40	0	30	ns
20A[2,6]	$\overline{AS}$ Asserted to R/$\overline{W}$ Low (Write)	t_{ASRV}	—	10	—	10	—	0	—	10	ns
21[2]	Address Valid to R/$\overline{W}$ Low (Write)	t_{AVRL}	20	—	0	—	0	—	0	—	ns
21A[2]	FC Valid to R/$\overline{W}$ Low (Write)	t_{FCVRL}	60	—	50	—	30	—	30	—	ns
22[2]	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	t_{RLSL}	80	—	50	—	30	—	30	—	ns
23	Clock Low to Data-Out Valid (Write)	t_{CLDO}	—	62	—	50	—	50	—	30	ns

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

(Continued)

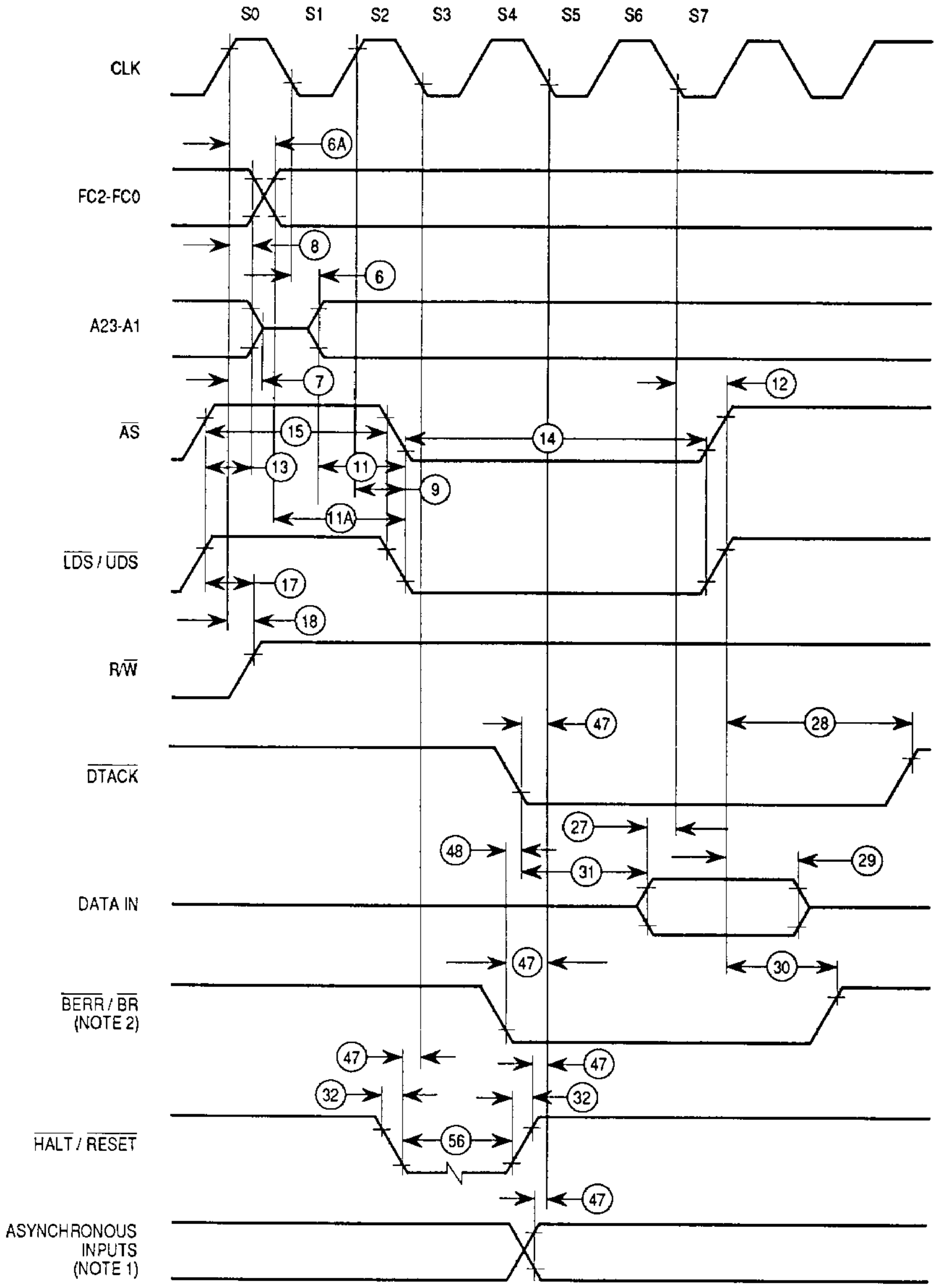
Num.	Characteristic	Symbol	8 MHz		10 MHz		12.5 MHz		16.67 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
25[2]	$\overline{\text{AS}}$, $\overline{\text{DS}}$ Negated to Data-Out Invalid (Write)	t_{SHDOI}	40	—	30	—	20	—	15	—	ns
26[2]	Data-Out Valid to $\overline{\text{DS}}$ Asserted (Write)	t_{DOSL}	40	—	30	—	20	—	15	—	ns
27[5]	Data-In Valid to Clock Low (Setup Time on Read)	t_{DICL}	10	—	10	—	10	—	5	—	ns
28[2]	$\overline{\text{AS}}$, $\overline{\text{DS}}$ Negated to $\overline{\text{DTACK}}$ Negated (Asynchronous Hold)	t_{SHDAH}	0	240	0	190	0	150	0	110	ns
28A	Clock High to $\overline{\text{DTACK}}$ Negated	t_{CHDH}	0	240	0	190	0	150	0	110	ns
29	$\overline{\text{AS}}$, $\overline{\text{DS}}$ Negated to Data-In Invalid (Hold Time on Read)	t_{SHDII}	0	—	0	—	0	—	0	—	ns
29A	$\overline{\text{AS}}$, $\overline{\text{DS}}$ Negated to Data-In High Impedance	t_{SHDZ}	—	187	—	150	—	120	—	90	ns
30	$\overline{\text{AS}}$, $\overline{\text{DS}}$ Negated to $\overline{\text{BERR}}$ Negated	t_{SHBEH}	0	—	0	—	0	—	0	—	ns
31[2,5]	$\overline{\text{DTACK}}$ Asserted to Data-In Valid (Setup Time)	t_{DALDI}	—	90	—	65	—	50	—	50	ns
32	$\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ Input Transition Time	$t_{RHr,f}$	0	200	0	200	0	200	—	150	ns
33	Clock High to $\overline{\text{BG}}$ Asserted	t_{CHGL}	—	62	—	50	—	40	0	30	ns
34	Clock High to $\overline{\text{BG}}$ Negated	t_{CHGH}	—	62	—	50	—	40	0	30	ns
35	$\overline{\text{BR}}$ Asserted to $\overline{\text{BG}}$ Asserted	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
36[7]	$\overline{\text{BR}}$ Negated to $\overline{\text{BG}}$ Negated	t_{BRHGH}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37	$\overline{\text{BGACK}}$ Asserted to $\overline{\text{BG}}$ Negated	t_{GALGH}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37A[8]	$\overline{\text{BGACK}}$ Asserted to $\overline{\text{BR}}$ Negated	t_{GALBRH}	20	1.5	20	1.5	20	1.5	10	1.5	Clks/ns
38	$\overline{\text{BG}}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{\text{AS}}$ Negated)	t_{GLZ}	—	80	—	70	—	60	—	50	ns
39	$\overline{\text{BG}}$ Width Negated	t_{GH}	1.5	—	1.5	—	1.5	—	1.5	—	Clks
40	Clock Low to $\overline{\text{VMA}}$ Asserted	t_{CLVML}	—	70	—	70	—	70	—	50	ns
41	Clock Low to E Transition	t_{CLET}	—	55	—	45	—	35	—	35	ns
42	E Output Rise and Fall Time	$t_{Er,f}$	—	15	—	15	—	15	—	15	ns
43	$\overline{\text{VMA}}$ Asserted to E High	t_{VMLEH}	200	—	150	—	90	—	80	—	ns
44	$\overline{\text{AS}}$, $\overline{\text{DS}}$ Negated to $\overline{\text{VPA}}$ Negated	t_{SHVPH}	0	120	0	90	0	70	0	50	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	t_{ELCAI}	30	—	10	—	10	—	10	—	ns
46	$\overline{\text{BGACK}}$ Width Low	t_{GAL}	1.5	—	1.5	—	1.5	—	1.5	—	Clks
47[5]	Asynchronous Input Setup Time	t_{ASI}	10	—	10	—	10	—	5	—	ns
48[2,3]	$\overline{\text{BERR}}$ Asserted to $\overline{\text{DTACK}}$ Asserted	t_{BELDAL}	20	—	20	—	20	—	10	—	ns
49[9]	$\overline{\text{AS}}$, $\overline{\text{DS}}$ Negated to E Low	t_{SHEL}	70	70	–55	55	-45	45	-35	35	ns
50	E Width High	t_{EH}	450	—	350	—	280	—	220	—	ns
51	E Width Low	t_{EL}	700	—	550	—	440	—	340	—	ns
52	Data-In Hold from Clock High	t_{CHDII}	0	—	0	—	0	—	0	—	ns
53	Data-Out Hold from Clock High	t_{CHDOI}	0	—	0	—	0	—	0	—	ns
54	E Low to Data-Out Invalid	t_{ELDOI}	30	—	20	—	15	—	10	—	ns

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES (Concluded)

Num.	Characteristic	Symbol	8 MHz		10 MHz		12.5 MHz		16.67 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
55	R/W Asserted to Data Bus Impedance Change	t_{RLDBD}	30	—	20	—	10	—	0	—	ns
56[4]	HALT/RESET Pulse Width	t_{HRPW}	10	—	10	—	10	—	10	—	Clks
57	BGACK Negated to AS, DS, R/W Driven	t_{GASD}	1.5	—	1.5	—	1.5	—	1.5	—	Clks
57A	BGACK Negated to FC, VMA Driven	t_{GAFD}	1	—	1	—	1	—	1	—	Clks
58[7]	BR Negated to AS, DS, R/W Driven	t_{RHSD}	1.5	—	1.5	—	1.5	—	1.5	—	Clks
58A[7]	BR Negated to FC, VMA Driven	t_{RHFD}	1	—	1	—	1	—	1	—	Clks

NOTES:

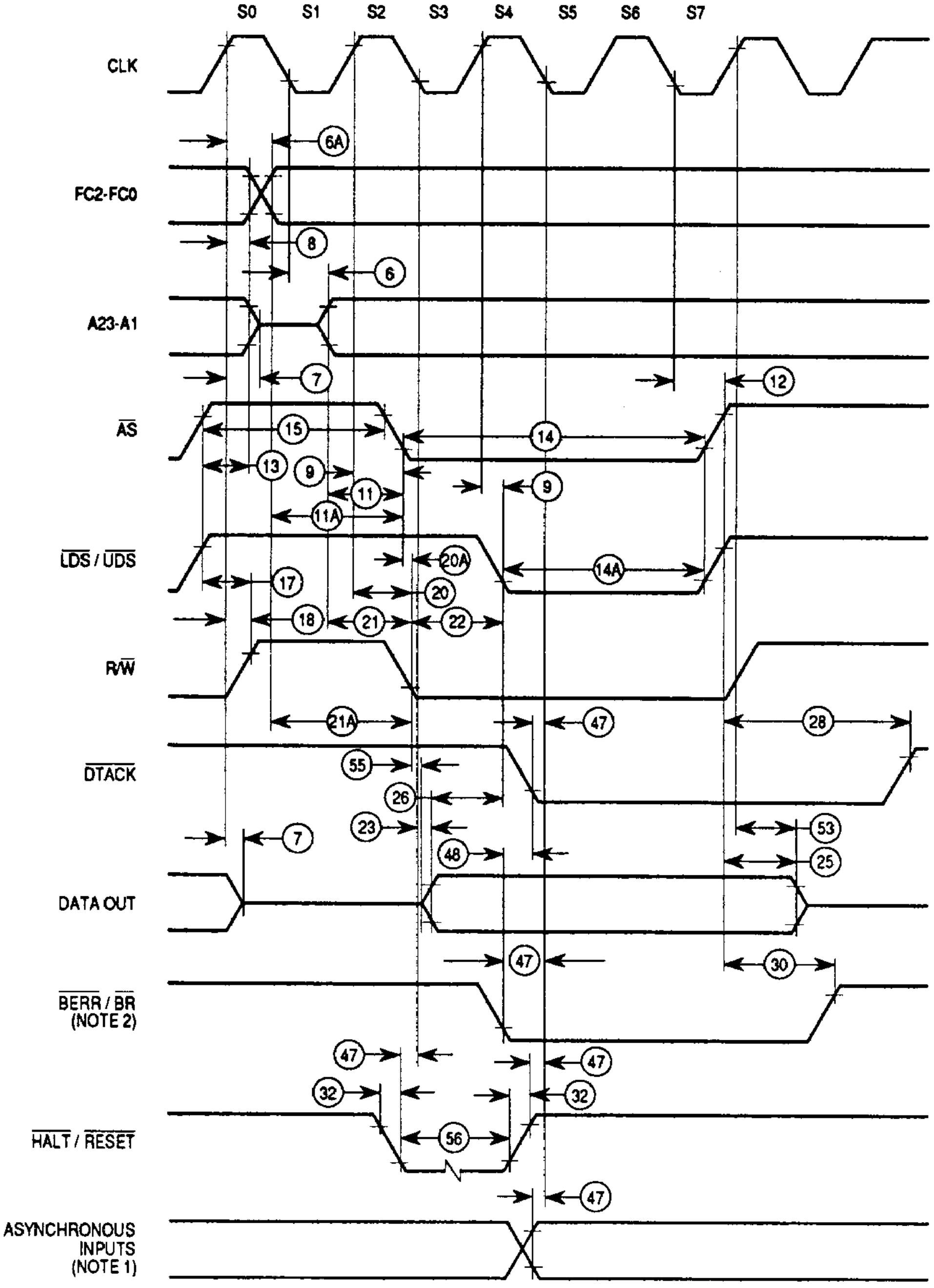
1. For a loading capacitance of less than or equal to 50 pF, subtract 5 ns from the value given in the maximum columns.
2. Actual value depends on clock period.
3. If #47 is satisfied for both DTACK and BERR, #48 may be ignored. In the absence of DTACK, BERR is an asynchronous input using the asynchronous input setup time (#47).
4. For power-up, the MC68000 must be held in the reset state for 100 ms to allow stabilization of on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the processor.
5. If the asynchronous input setup time (#47) requirement is satisfied for DTACK, the DTACK-asserted to data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle.
6. When AS and R/W are equally loaded (±20%), subtract 5 ns from the values given in these columns.
7. The processor will negate BG and begin driving the bus again if external arbitration logic negates BR before asserting BGACK.
8. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, BG may be reasserted.
9. The falling edge of S6 triggers both the negation of the strobes (AS and xDS) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of E.



NOTES:

1. Setup time for the asynchronous inputs $\overline{IPL2}$-$\overline{IPL0}$ and $\overline{VPA}$ (#47) guarantees their recognition at the next falling edge of the clock.
2. $\overline{BR}$ need fall at this time only to insure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.

Figure 7. Read Cycle Timing Diagram



NOTES:

1. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.
2. Because of loading variations, R/$\overline{W}$ may be valid after $\overline{AS}$ even though both are initiated by the rising edge of S2 (specification #20A).

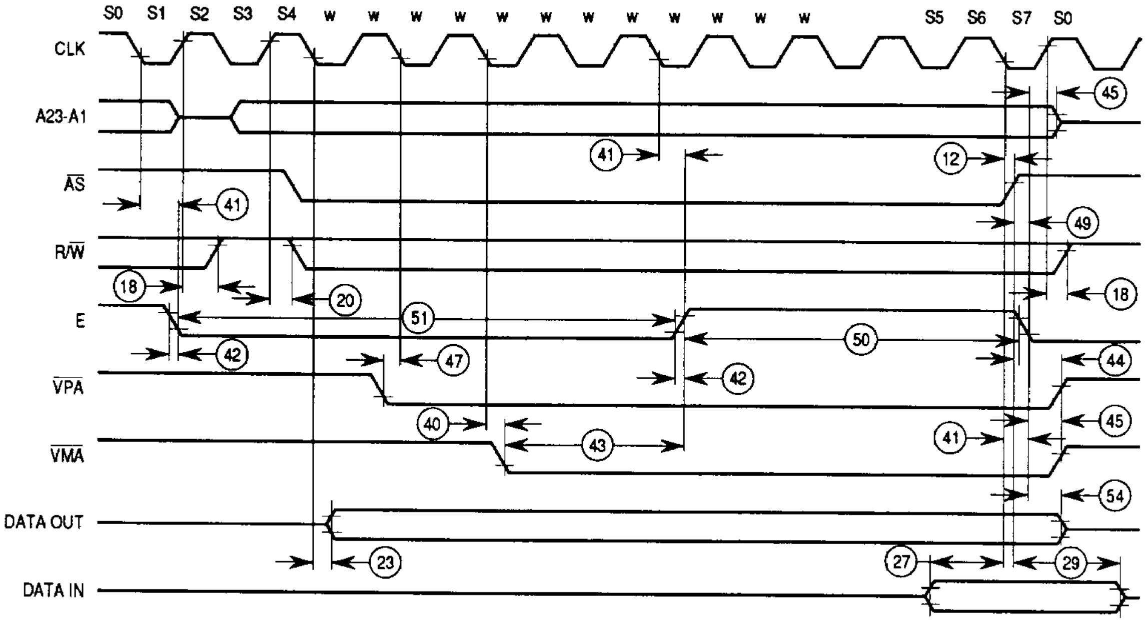
Figure 8. Write Cycle Timing Diagram

AC ELECTRICAL SPECIFICATIONS — MC68HC001 TO M6800 PERIPHERAL CYCLES (V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H; see Figures 9 and 10)

Num.	Characteristic	Symbol	8 MHz		10 MHz		12.5 MHz		16.67 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
12[1]	Clock Low to AS, DS Negated	t_{CLSH}	—	62	—	50	—	40	3	30	ns
18[1]	Clock High to R/W High	t_{CHRH}	0	55	0	45	0	40	0	30	ns
20[1]	Clock High to R/W Low	t_{CHRL}	0	55	0	45	0	40	0	30	ns
23	Clock Low to Data-Out Valid	t_{CLDO}	—	62	—	50	—	50	—	30	ns
27	Data-In Valid to Clock Low (Setup Time of Read)	t_{DICL}	10	—	10	—	10	—	5	—	ns
29	AS, DS Negated to Data-In Invalid (Hold Time on Read)	t_{SHDII}	0	—	0	—	0	—	0	—	ns
40	Clock Low to VMA Asserted	t_{CLVML}	—	70	—	70	—	70	—	50	ns
41	Clock Low to E Transition	t_{CLET}	—	55	—	45	—	35	—	35	ns
42	E Output Rise and Fall Time	$t_{Er,f}$	—	15	—	15	—	15	—	15	ns
43	VMA Asserted to E High	t_{VMLEH}	200	—	150	—	90	—	80	—	ns
44	AS, DS Negated to VPA Negated	t_{SHVPH}	0	120	0	90	0	70	0	50	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	t_{ELCAI}	30	—	10	—	10	—	10	—	ns
47	Asynchronous Input Setup Time	t_{ASI}	10	—	10	—	10	—	5	—	ns
49[2]	AS, DS, Negated to E Low	t_{SHEL}	−70	70	−55	55	−45	45	−35	35	ns
50	E Width High	t_{EH}	450	—	350	—	280	—	220	—	ns
51	E Width Low	t_{EL}	700	—	550	—	440	—	340	—	ns
54	E Low to Data-Out Invalid	t_{ELDOI}	30	—	20	—	15	—	10	—	ns

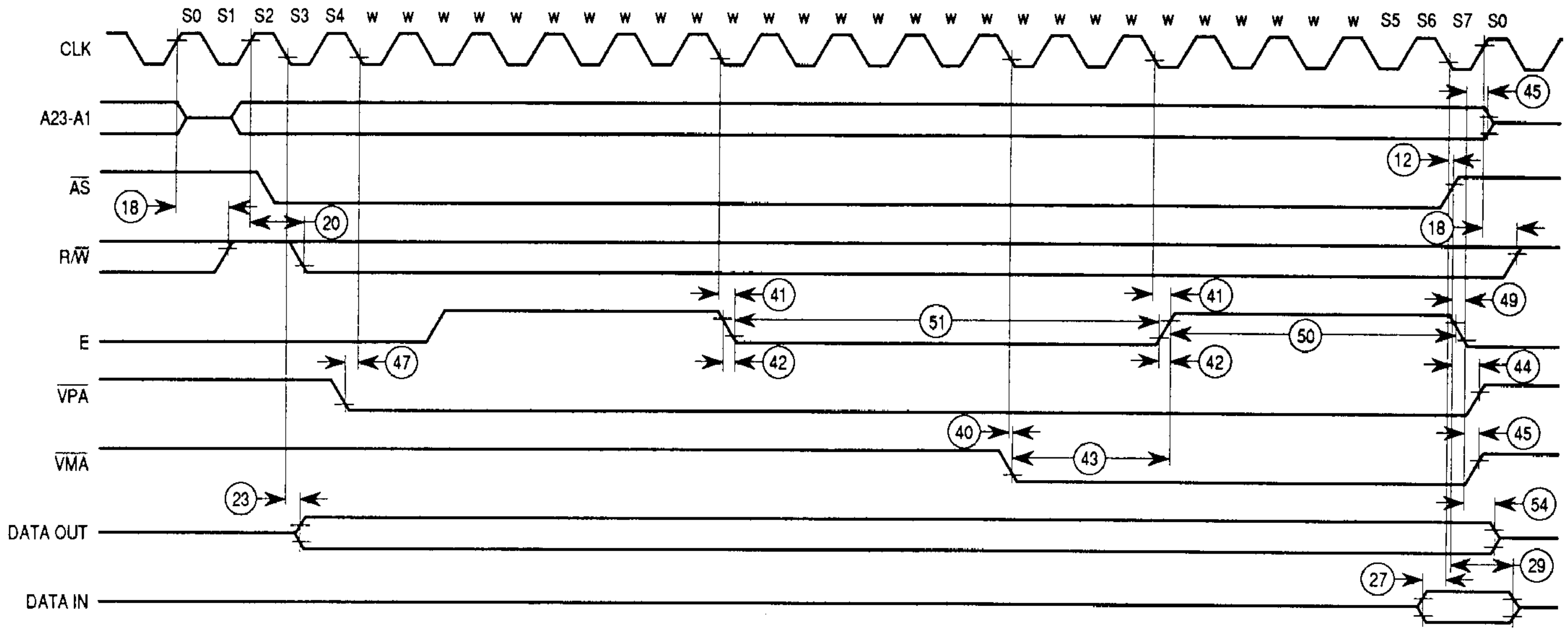
NOTES:

1. For a loading capacitance of less than or equal to 50 pF, subtract 5 ns from the value given in the maximum columns.
2. The falling edge of S6 trigger both the negation of the strobes (AS and xDS) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of E.



NOTE: This timing diagram is included for those who wish to design their own circuit to generate VMA. It shows the best case possibly attainable.

Figure 9. MC68HC001 to M6800 Peripheral Timing Diagram (Best Case)



NOTE: This timing diagram is included for those who wish to design their own circuit to generate $\overline{\text{VMA}}$. It shows the worst case possibly attainable.

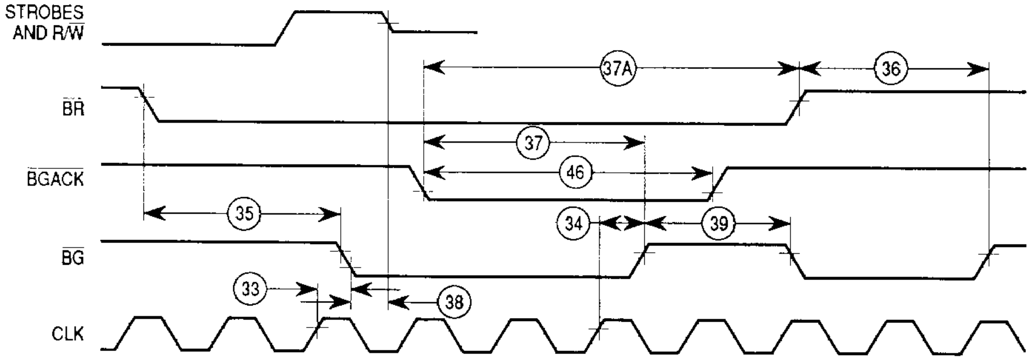
Figure 10. MC68HC001 to M6800 Peripheral Timing Diagram (Worst Case)

AC ELECTRICAL SPECIFICATIONS — BUS ARBITRATION (V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H; see Figures 11-14)

Num.	Characteristic	Symbol	8 MHz		10 MHz		12.5 MHz		16.67 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
7	Clock High to Address, Data Bus High Impedance (Maximum)	t_{CHADZ}	—	80	—	70	—	60	—	50	ns
16	Clock High to Control Bus High Impedance	t_{CHCZ}	—	80	—	70	—	60	—	50	ns
33	Clock High to BG Asserted	t_{CHGL}	—	62	—	50		40	0	30	ns
34	Clock High to BG Negated	t_{CHGH}	—	62	—	50	—	40	0	30	ns
35	BR Asserted to BG Asserted	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
36[1]	BR Negated to BG Negated	t_{BRHGH}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37	BGACK Asserted to BG Negated	t_{GALGH}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clks
37A[2]	BGACK Asserted to BR Negated	t_{GALBRH}	20	1.5	20	1.5	20	1.5	10	1.5	Clks ns
38	BG Asserted to Control, Address, Data Bus High Impedance (AS Negated)	t_{GLZ}	—	80	—	70	—	60	—	50	ns
39	BG Width Negated	t_{GH}	1.5	—	1.5	—	1.5	—	1.5	—	Clks
46	BGACK Width Low	t_{GAL}	1.5	—	1.5	—	1.5	—	1.5	—	Clks
47	Asynchronous Input Setup Time	t_{ASI}	10	—	10	—	10	—	5	—	ns
57	BGACK Negated to AS, DS, R/W Driven	t_{GASD}	1.5	—	1.5	—	1.5	—	1.5	—	Clks
57A	BGACK Negated to FC, VMA Driven	t_{GAFD}	1	—	1	—	1	—	1	—	Clks
58[1]	BR Negated to AS, DS, R/W Driven	t_{RHSD}	1.5	—	1.5	—	1.5	—	1.5	—	Clks
58A[1]	BR Negated to FC, VMA Driven	t_{RHFD}	1	—	1	—	1	—	1	—	Clks

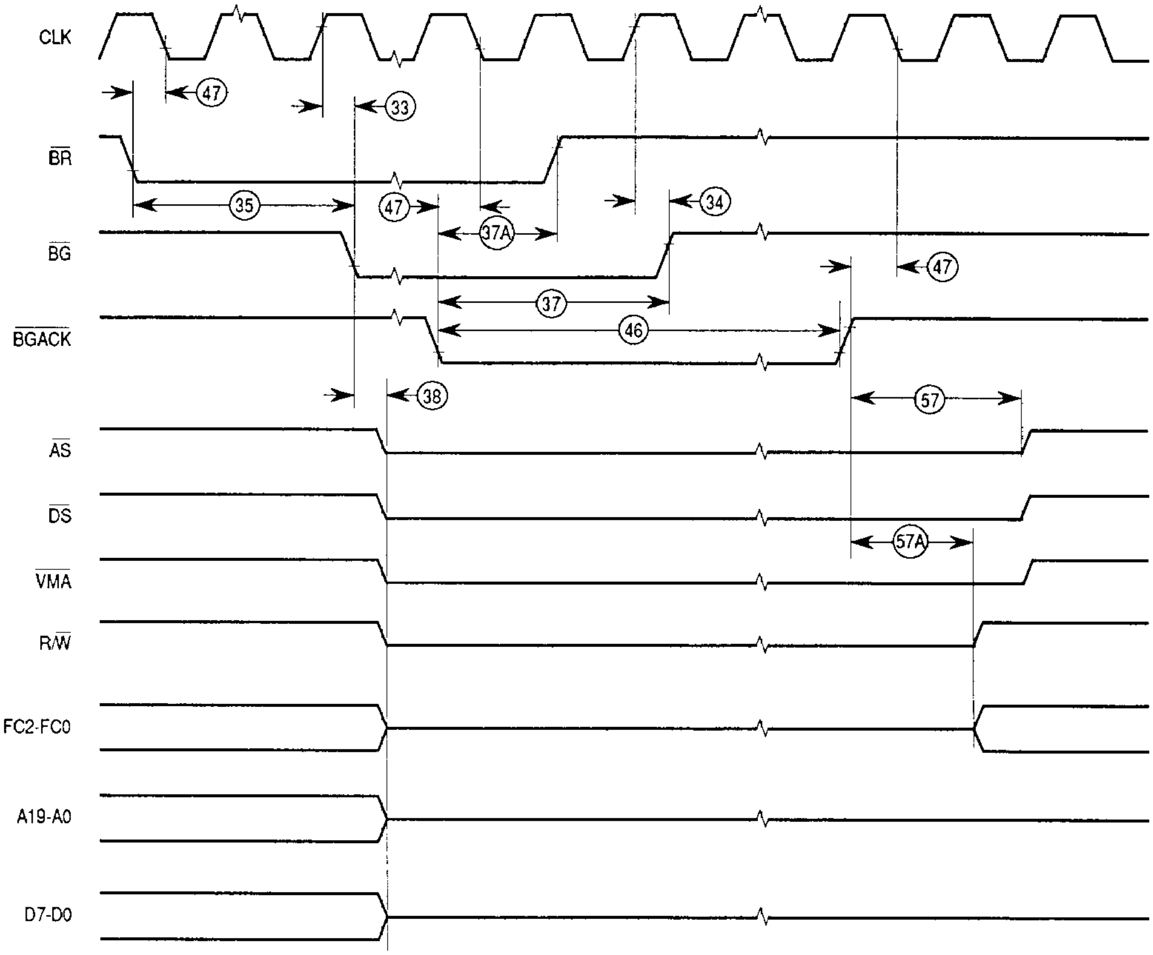
NOTES:

1. The processor will negate BG and begin driving the bus again if external arbitration logic negates BR before asserting BGACK.
2. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, BG may be reasserted.



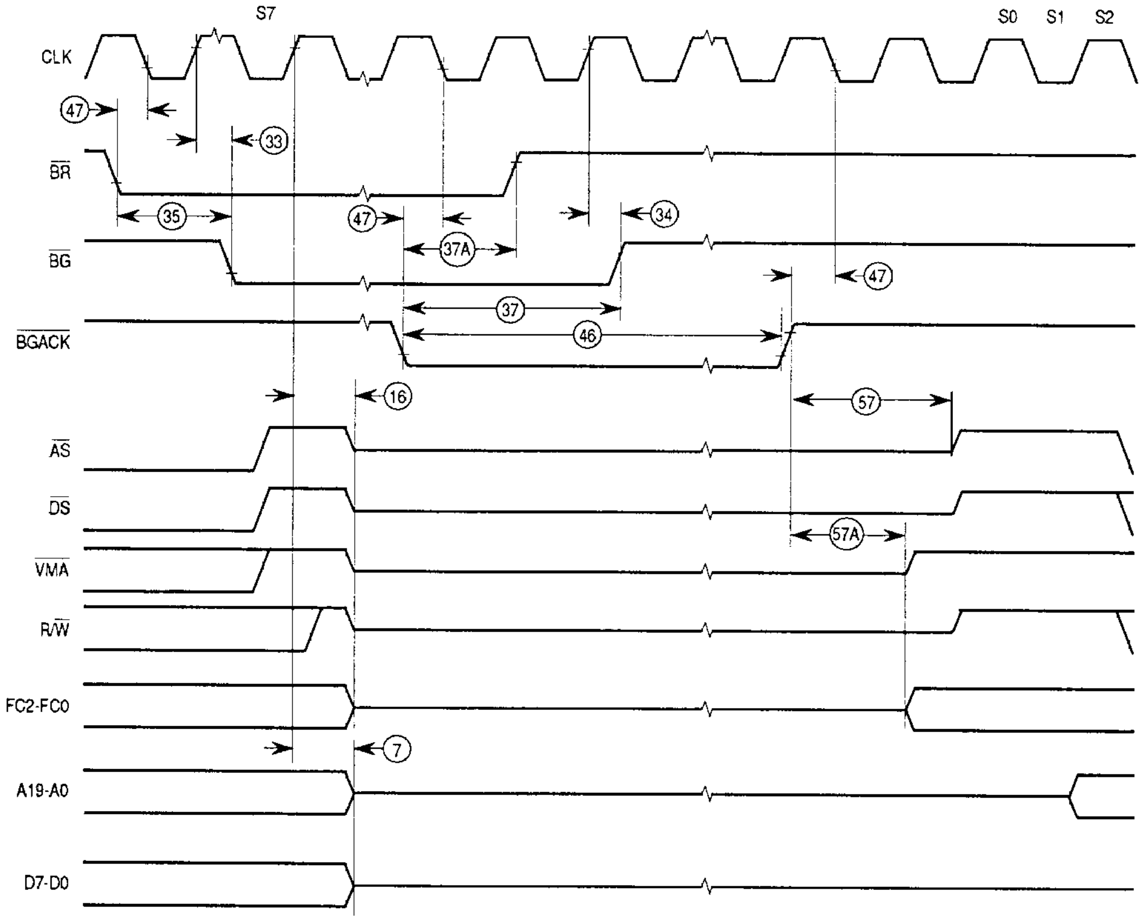
NOTE: Setup time to the clock (#47) for the asynchronous inputs BERR, BGACK, BR, DTACK, IPL2-IPL0, and VPA guarantees their recognition at the next falling edge of the clock.

Figure 11. Bus Arbitration Timing Diagram



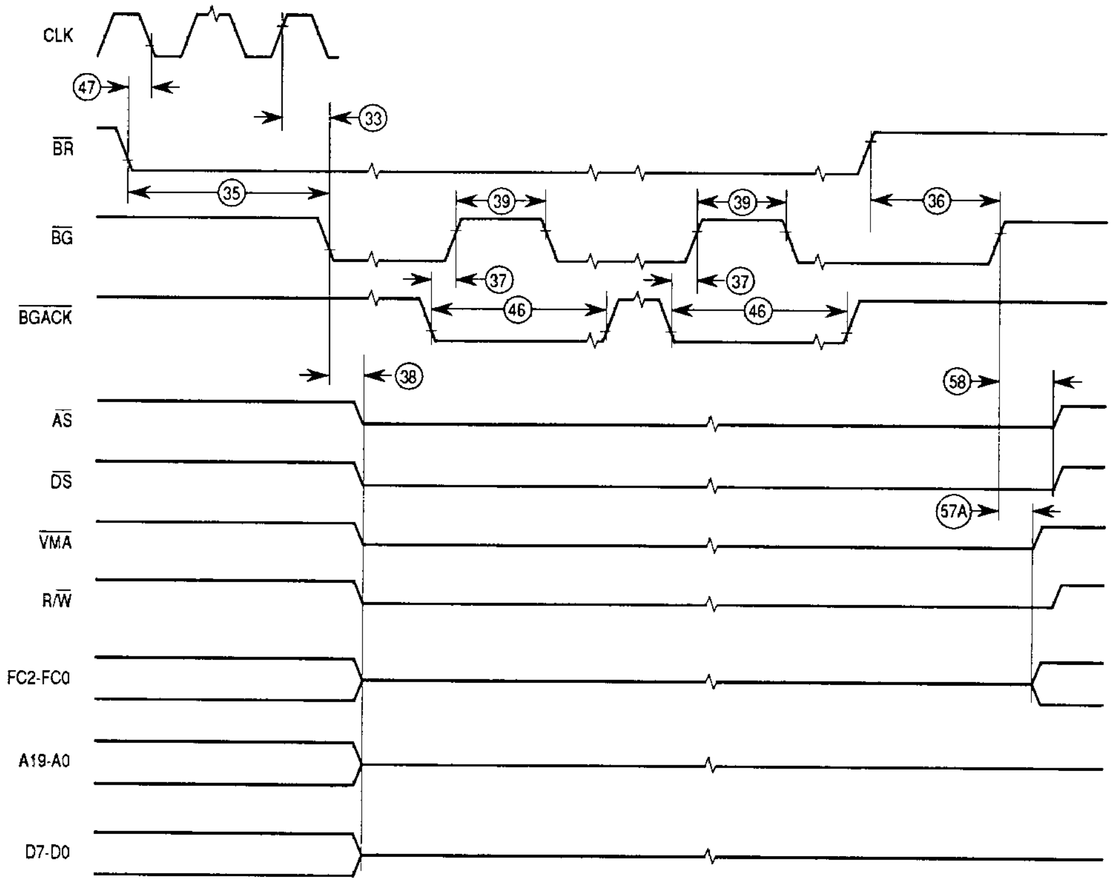
NOTE: Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V.

Figure 12. Bus Arbitration Timing — Idle Bus Case



NOTE: Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V.

Figure 13. Bus Arbitration Timing — Active Bus Case

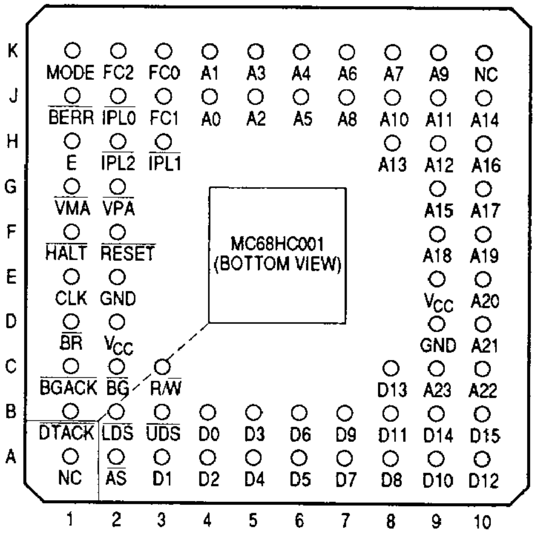


NOTE: Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V.

Figure 14. Bus Arbitration Timing — Multiple Bus Request

PIN ASSIGNMENTS

68-LEAD PIN GRID ARRAY



68-LEAD PLASTIC LEADED CHIP CARRIER