8*x*930H*x*
UNIVERSAL SERIAL BUS HUB PERIPHERAL CONTROLLER

- **USB Hub with One Upstream, One Internal Downstream, and Three External Downstream Ports on HD/HE Parts or Four on HF/HG Parts**
  - **— Complete Universal Serial Bus Specification 1.0 Compatibility**
  - **— Serves as both USB Hub and USB Embedded Function (Internal Port)**
- **USB Hub**
  - **— Connectivity Management**
  - **— Downstream Device Connect/Disconnect Detection**
  - **— Power Management, Including Suspend and Resume**
  - **— Bus Fault Detection and Recovery**
  - **— Full and Low Speed Downstream Device Support**
- **Output Pin for Port Power Switching**
- **Input Pin for Overcurrent Detection**
- **USB Embedded Function**
  - **— Supports Isochronous and Non-isochronous Data**
- **On-chip USB Transceivers**
- **Serial Bus Interface Engine (SIE)**
  - **— Packet Decoding/Generation**
  - **— CRC Generation and Checking**
  - **— NRZI Encoding/Decoding and Bit-stuffing**
- **Hub FIFO Data Buffers**
  - **— One Pair of 16-byte Transmit and Receive FIFOs**
  - **— One 1-byte Transmit Register**
- **Embedded Function FIFO Data Buffers**
  - **— Three Pairs of 16-byte Transmit and Receive FIFOs**
  - **— One Pair of Configurable Transmit and Receive FIFOs (1 Kbyte total)**
- **Automatic Transmit/Receive FIFO Management**
- **Three USB Interrupt Vectors**
  - **— Endpoint Transmit/Receive Done**
  - **— Start of Frame/Hub Endpoint Done**
  - **— Global Suspend/Resume**
- **Low Clock Mode**
- **User-selectable Configurations**
  - **— External Wait State**
  - **— External Address Range**
  - **— Page Mode**
- **Real-time Wait Function**
- **256-Kbyte External Code/Data Memory Space**
- **On-chip ROM Options**
  - **— 0, 8, or 16 Kbytes**
- **1024 bytes On-chip Data RAM**
- **Four Input/Output Ports**
- **Standard MCS® 51 UART**
- **Power-saving Idle and Powerdown Modes**
- **Register-based MCS® 251 Architecture**
- **Code-compatible with MCS 51 and MCS 251 Microcontrollers**
- **12-MHz Crystal Operation**

The 8*x*930H*x* USB hub peripheral controller is based on the MCS 251 microcontroller. It consists of standard 8XC251Sx peripherals plus a USB module. The USB module provides both USB hub and USB embedded function capabilities. The 8*x*930H*x* supports USB hub functionality, embedded function, suspend/resume modes, isochronous/non-isochronous transfers, and it is fully USB rev 1.0 specification compliant. The USB module contains one internal and three (or four) external downstream ports and integrates the USB transceivers, serial bus interface engine (SIE), hub interface unit (HIU), function interface unit (FIU), and transmit/receive FIFOs. The 8*x*930H*x* uses the standard instruction set of the MCS 251 architecture, which is binary code compatible with the MCS 51 architecture.

May 1997 **Order Number: 272928-003**

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1.0 ABOUT THIS DOCUMENT

This data sheet contains advance information about Intel's 8*x*930H*x* Universal Serial Bus hub peripheral controller, based on the MCS® 251 peripheral controller, which includes a functional overview, mechanical data, targeted electrical specifications (simulated), and bus functional waveforms. A detailed functional description, other than parametric performance, is published in the *8x930Ax, 8x930Hx Universal Serial Bus Micorcontroller User's Manual* (272949).

1.1 Additional Information Sources

Intel documentation is available from your local Intel Sales Representative or Intel Literature Sales.

Intel Corporation
Literature Sales
P.O. Box 7641
Mt. Prospect, IL 60056-7641
1-800-879-4683

1.2 Electronic Information

We offer a variety of technical and product information through the World Wide Web (see Table 2 for URL) and through FaxBack service which is an on-demand publishing system that sends documents to your fax machine. You can get product announcements, change notifications, product literature, device characteristics, design recommendations, and quality and reliability information 24 hours a day, 7 days a week. Just dial the telephone number and respond to the system prompts.

Table 1. Related Documentation

Document Title	Order/Contact
8x930Ax, 8x930Hx Universal Serial Bus Micorcontroller User's Manual	Intel Order # 272949
Universal Serial Bus Specification	Intel Order # 272962

Table 2. Electronic Information

Document Title	Order/Contact
Intel's World-Wide Web (WWW) Location:	http://www.intel.com/design/usb/
Customer Support (US and Canada):	800-628-8686
FaxBack Service:	
US and Canada	800-628-2283
Europe	+44(0)793-496646
worldwide	916-356-3105
Application Bulletin Board Service:	
up to 14.4-Kbaud line, worldwide	916-356-3600
dedicated 2400-baud line, worldwide	916-356-7209
Europe	+44(0)793-496340

ADVANCE INFORMATION

1.3 Product Summary

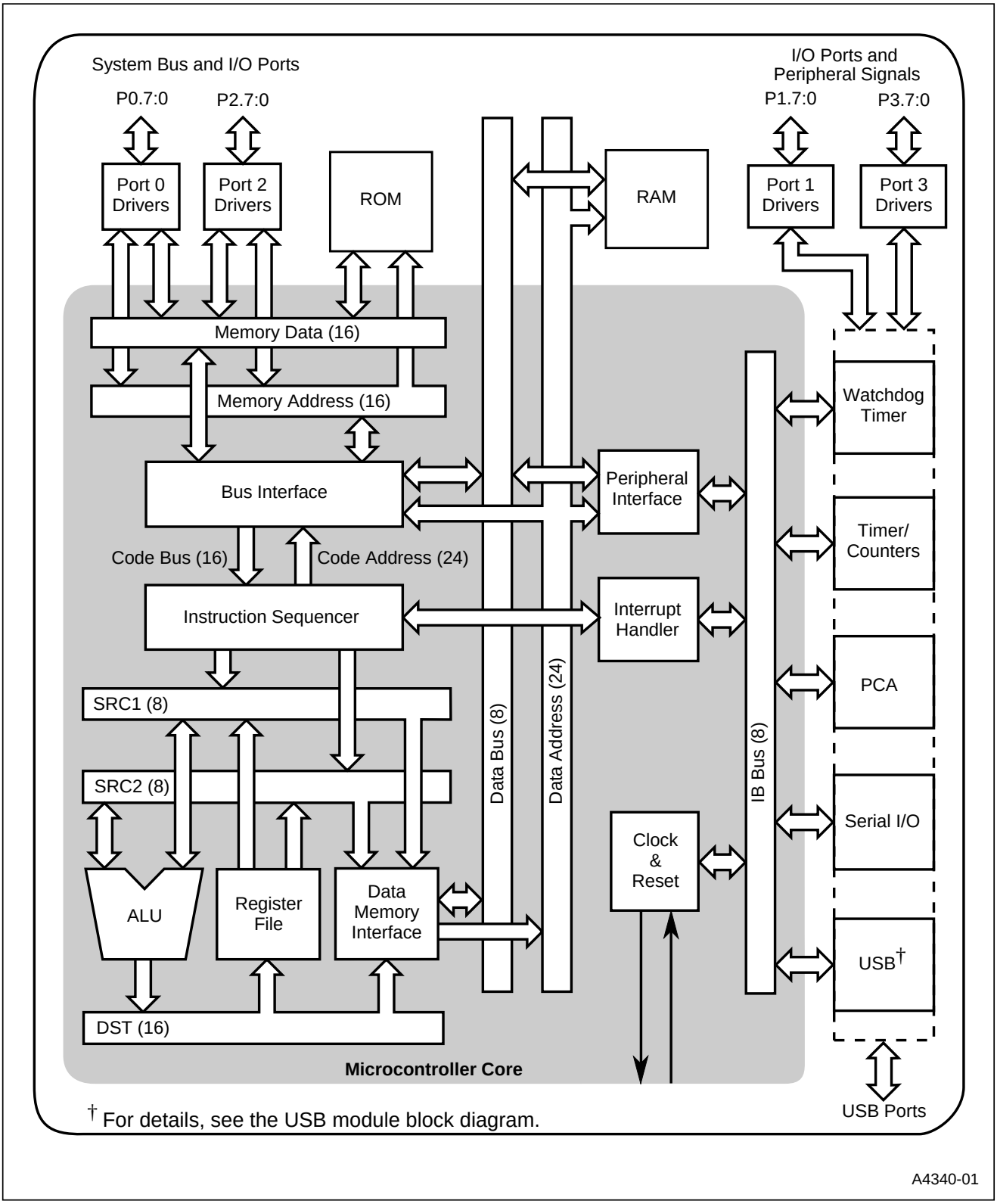

Figure 1. 8*x*930H*x* Block Diagram

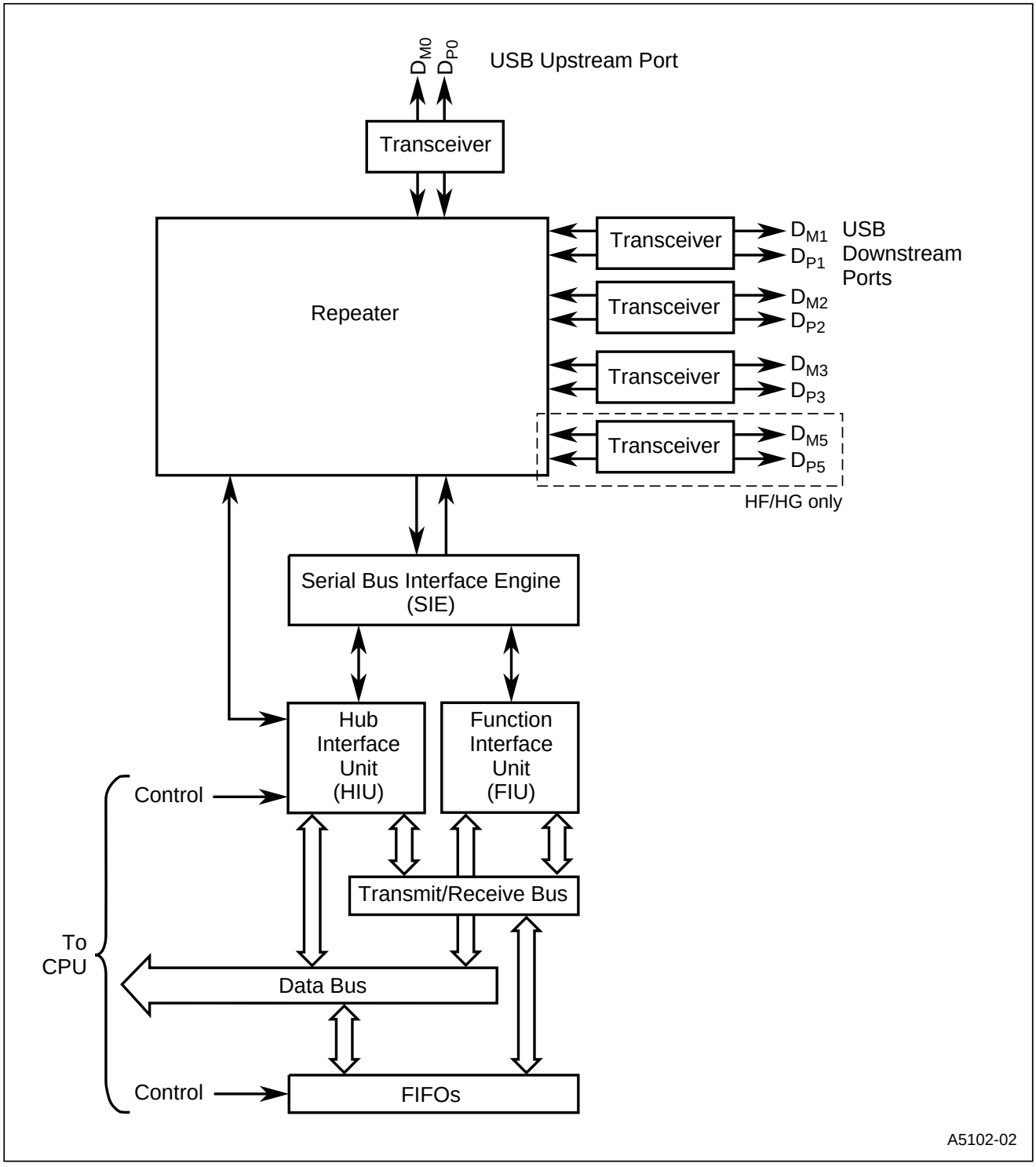

Figure 2. 8x930Hx USB Module Block Diagram

2.0 NOMENCLATURE OVERVIEW

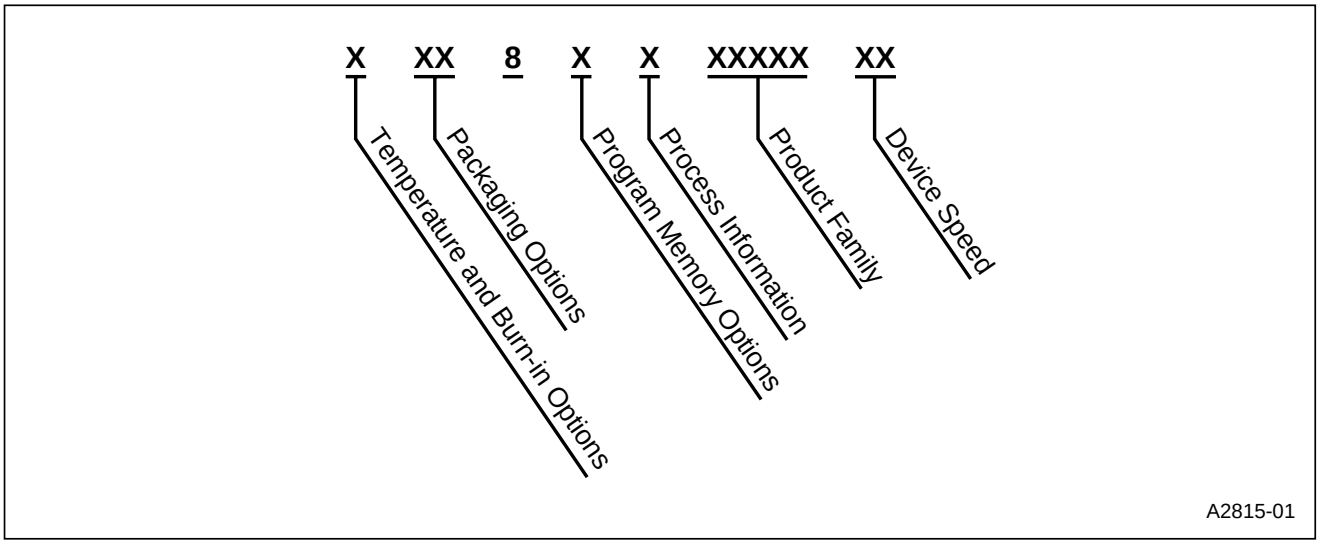

Figure 3. Product Nomenclature

Table 3. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in
Packaging Options	N	Plastic Leaded Chip Carrier (PLCC)
	U	Shrink Dual In-Line Package (SDIP)
Program Memory Options	0	Without ROM
	3	With ROM
Process and Voltage Information	no mark	CHMOS
Product Family	930Hx	Advanced 8-bit microcontroller architecture with on-chip Universal Serial Bus Hub and Function capability. Indicates ROM size, RAM size, and quantity of external downstream ports (see Table 4).
Device Speed	no mark	12 MHz crystal

Table 4. Proliferation Options

4 External Downstream Ports (HF/HG)	3 External Downstream Ports (HD/HE)	ROM Size	RAM Size	Package
N80930HF	N80930HD	0	1024 bytes	68-pin PLCC
N83930HF	N83930HD	8 Kbytes	1024 bytes	68-pin PLCC
N83930HG	N83930HE	16 Kbytes	1024 bytes	68-pin PLCC
U80930HF	U80930HD	0	1024 bytes	64-pin SDIP
U83930HF	U83930HD	8 Kbytes	1024 bytes	64-pin SDIP
U83930HG	U83930HE	16 Kbytes	1024 bytes	64-pin SDIP

Table 5. Downstream Port Allocation

Downstream Port Number	8*x*930HD/HE	8*x*930HF/HG
1	External	External
2	External	External
3	External	External
4	Internal (Embedded Function)	Internal (Embedded Function)
5	—	External

3.0 PINOUT

Figure 4 illustrates a diagram of the 8*x*930HD/HE PLCC package. Table 6 and Table 8 contain indexes of the pin arrangement. Table 10 contains the signal descriptions for all pins.

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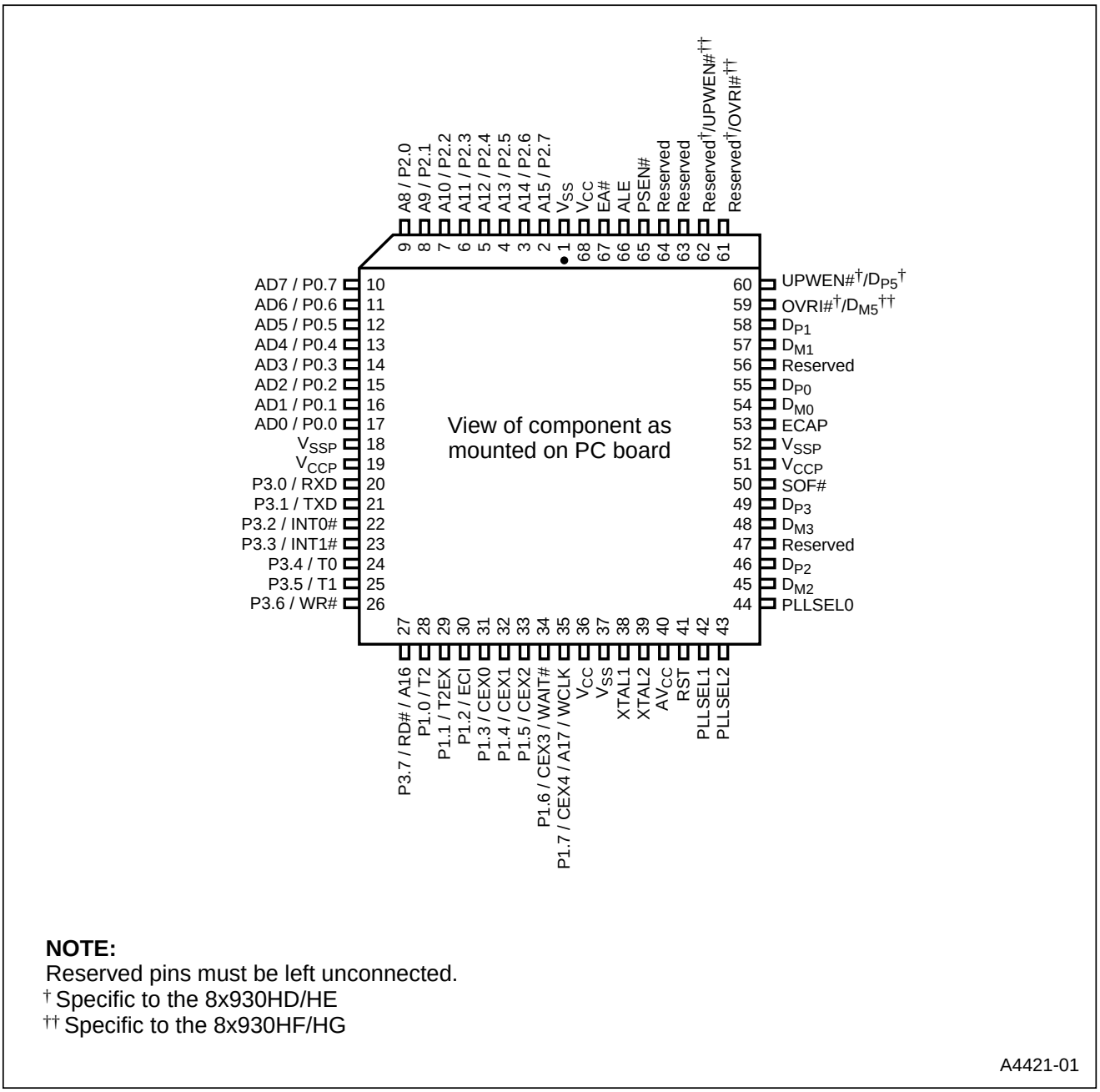

NOTE:
Reserved pins must be left unconnected.
† Specific to the 8x930HD/HE
†† Specific to the 8x930HF/HG

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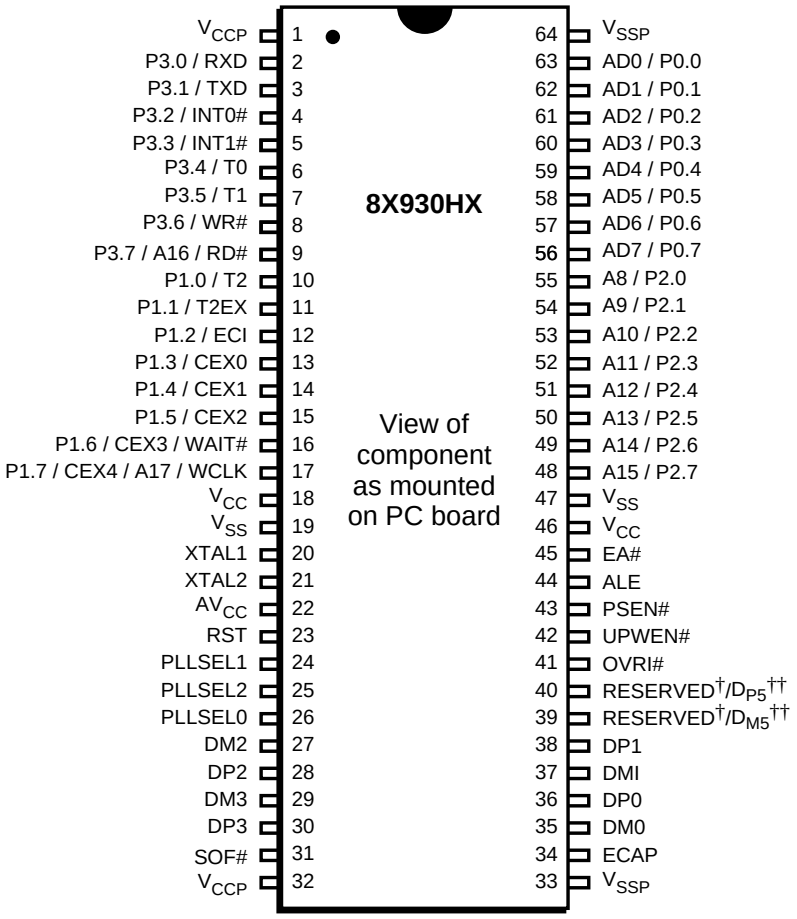
Figure 4. 8*x*930HD/HE and 8*x*930HF/HG 68-pin PLCC Package



NOTE:
Reserved pins must be left unconnected.
† Specific to the 8x930HD/HE
†† Specific to the 8x930HF/HG

A4422-01

Figure 5. 8*x*930HD/HE and 8*x*930HF/HG 64-pin SDIP Package

Table 6. 68-pin PLCC Pin Assignment

Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	24	P3.4/T0	47	Reserved
2	A15/P2.7	25	P3.5/T1	48	D_{M3}
3	A14/P2.6	26	P3.6/WR#	49	D_{P3}
4	A13/P2.5	27	P3.7/RD#/A16	50	SOF#
5	A12/P2.4	28	P1.0/T2	51	V_{CCP}
6	A11/P2.3	29	P1.1/T2EX	52	V_{SSP}
7	A10/P2.2	30	P1.2/ECI	53	ECAP
8	A9/P2.1	31	P1.3/CEX0	54	D_{M0}
9	A8/P2.0	32	P1.4/CEX1	55	D_{P0}
10	AD7/P0.7	33	P1.5/CEX2	56	Reserved
11	AD6/P0.6	34	P1.6/CEX3/WAIT#	57	D_{M1}
12	AD5/P0.5	35	P1.7/CEX4/A17/WCLK	58	D_{P1}
13	AD4/P0.4	36	V_{CC}	59	OVRI#†/D_{M5}††
14	AD3/P0.3	37	V_{SS}	60	UPWEN#†/D_{P5}††
15	AD2/P0.2	38	XTAL1	61	Reserved†/OVRI#††
16	AD1/P0.1	39	XTAL2	62	Reserved†/UPWEN#††
17	AD0/P0.0	40	AV_{CC}	63	Reserved
18	V_{SSP}	41	RST	64	Reserved
19	V_{CCP}	42	PLLSEL1	65	PSEN#
20	P3.0/RXD	43	PLLSEL2	66	ALE
21	P3.1/TXD	44	PLLSEL0	67	EA#
22	P3.2/INT0#	45	D_{M2}	68	V_{CC}
23	P3.3/INT1#	46	D_{P2}		

† Specific to the 8*x*930HD/HE

†† Specific to the 8*x*930HF/HG

Table 7. 64-pin SDIP Pin Assignment

Pin	Name
1	V_{CCP}
2	P3.0/RXD
3	P3.1/TXD
4	P3.2/INT0#
5	P3.3/ INT1#
6	P3.4/T0
7	P3.5/T1
8	P3.6/WR#
9	P3.7/A16/RD#
10	P1.0/T2
11	P1.1/T2EX
12	P1.2/ECI
13	P1.3/CEX0
14	P1.4/CEX1
15	P1.5/CEX2
16	P1.6/CEX3/WAIT#
17	P1.7/CEX4/A17/WCLK
18	V_{CC}
19	V_{SS}
20	XTAL1
21	XTAL2
22	AVCC

Pin	Name
23	RST
24	PLLSEL1
25	PLLSEL2
26	PLLSEL0
27	DM2
28	DP2
29	DM3
30	DP3
31	SOF#
32	V_{CCP}
33	V_{SSP}
34	ECAP
35	DM0
36	DP0
37	DM1
38	DP1
39	Reserved†/D_{M5}††
40	Reserved†/D_{P5}††
41	OVRI#
42	UPWEN#
43	PSEN#
44	ALE

Pin	Name
45	EA#
46	V_{CC}
47	V_{SS}
48	A15/P2.7
49	A14/P2.6
50	A13/P2.5
51	A12/P2.4
52	A11/P2.3
53	A10/P2.2
54	A9/P2.1
55	A8/P2.0
56	AD7/P0.7
57	AD6/P0.6
58	AD5/P0.5
59	AD4/P0.4
60	AD3/P0.3
61	AD2/P0.2
62	AD1/P0.1
63	AD0/P0.0
64	V_{SSP}

† Specific to the 8*x*930HD/HE

†† Specific to the 8*x*930HF/HG

Table 8. 68-pin PLCC Signal Assignments Arranged by Functional Category

Address & Data	
Name	**Pin**
AD0/P0.0	17
AD1/P0.1	16
AD2/P0.2	15
AD3/P0.3	14
AD4/P0.4	13
AD5/P0.5	12
AD6/P0.6	11
AD7/P0.7	10
A8/P2.0	9
A9/P2.1	8
A10/P2.2	7
A11/P2.3	6
A12/P2.4	5
A13/P2.5	4
A14/P2.6	3
A15/P2.7	2
P3.7/RD#/A16	27
P1.7/CEX4/A17/WCLK	35

Input/Output	
Name	**Pin**
P1.0/T2	28
P1.1/T2EX	29
P1.2/ECI	30
P1.3/CEX0	31
P1.4/CEX1	32
P1.5/CEX2	33
P1.6/CEX3/WAIT#	34
P1.7/CEX4/A17/WCLK	35
P3.0/RXD	20
P3.1/TXD	21
P3.2/INT0#	22
P3.3/INT1#	23
P3.4/T0	24
P3.5/T1	25
P3.6/WR#	26
P3.7/RD#/A16	27

USB	
Name	**Pin**
PLLSEL0	44
PLLSEL1	42
PLLSEL2	43
D_{M0}	54
D_{P0}	55
D_{M1}	57
D_{P1}	58
D_{M2}	45
D_{P2}	46
D_{M3}	48
D_{P3}	49
SOF#	50
ECAP	53
OVRI#	59†/ 61††
UPWEN#	60†/ 62††
D_{M5}	59††
D_{P5}	60††

Processor Control	
Name	**Pin**
P3.2/INT0#	22
P3.3/INT1#	23
RST	41
XTAL1	38
XTAL2	39

Power & Ground	
Name	**Pin**
V_{CC}	36, 68
V_{CCP}	19, 51
AV_{CC}	40
V_{SS}	1, 37
V_{SSP}	18, 52

Bus Control & Status	
Name	**Pin**
P3.6/WR#	26
P3.7/RD#/A16	27
PSEN#	65
ALE	66
EA#	67

† Specific to the 8*x*930HD/HE

†† Specific to the 8*x*930HF/HG

Table 9. 64-pin SDIP Signal Assignments Arranged by Functional Category

Address & Data	
Name	**Pin**
AD0/P0.0	63
AD1/P0.1	62
AD2/P0.2	61
AD3/P0.3	60
AD4/P0.4	59
AD5/P0.5	58
AD6/P0.6	57
AD7/P0.7	56
A8/P2.0	55
A9/P2.1	54
A10/P2.2	53
A11/P2.3	52
A12/P2.4	51
A13/P2.5	50
A14/P2.6	49
A15/P2.7	48
P3.7/A16/RD#	9
P1.7/CEX4/A17/WCLK	17

Input/Output	
Name	**Pin**
P1.0/T2	10
P1.1/T2EX	11
P1.2/ECI	12
P1.3/CEX0	13
P1.4/CEX1	14
P1.5/CEX2	15
P1.6/CEX3/WAIT#	16
P1.7/CEX4/A17/WCLK	17
P3.0/RXD	2
P3.1/TXD	3
P3.2/INT0#	4
P3.3/INT1#	5
P3.4/T0	6
P3.5/T1	7
P3.6/WR#	8
P3.7/A16/RD#	9

USB	
Name	**Pin**
PLLSEL0	26
PLLSEL1	24
PLLSEL2	25
D_{M0}	35
D_{P0}	36
D_{M1}	37
D_{P1}	38
D_{M2}	27
D_{P2}	28
D_{M3}	29
D_{P3}	30
SOF#	31
ECAP	34
OVRI#	41
UPWEN#	42
Reserved†/D_{M5}††	39
Reserved†/D_{P5}††	40

Processor Control	
Name	**Pin**
P3.2/INT0#	4
P3.3/INT1#	5
RST	23
XTAL1	20
XTAL2	21

Power & Ground	
Name	**Pin**
V_{CC}	46
V_{CCP}	32
AV_{CC}	22
V_{SS}	47
V_{SSP}	64

Bus Control & Status	
Name	**Pin**
P3.6/WR#	8
P3.7/RD#/A16	9
PSEN#	43
ALE	44
EA#	45

† Specific to the 8*x*930HD/HE

†† Specific to the 8*x*930HF/HG

4.0 SIGNALS

Table 10. Signal Description (Sheet 1 of 4)

Signal Name	Type	Description	Alternate Function
A17	O	**Address Line 17.** Output to memory as 18th external address bit in extended bus applications. Selected with bits RD1:0 in configuration byte UCONFIG0. See Table 11 and RD#, WR#, and PSEN#.	P1.7/CEX4/WCLK
A16	O	**Address Line 16**. Output to memory as 17th external address bit in extended bus applications. Selected with bits RD1:0 in configuration byte UCONFIG0. See Table 11 and RD#, WR#, and PSEN#.	RD#
A15:8	O	**Address Lines**. Upper address lines for external memory. Description is for nonpage mode configuration. For page mode configuration, data (D7:0) is multiplexed with the upper address byte (A15:8).	P2.7:0
AD7:0	I/O	**Address/Data Lines**. Multiplexed lower address lines and data lines for external memory. Description is for nonpage mode configuration. For page mode configuration, data (D7:0) is multiplexed with the upper address byte (A15:8).	P0.7:0
ALE	O	**Address Latch Enable**. ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. An external latch can use ALE to demultiplex the address from the address/data bus.	—
AV_{CC}	PWR	**Analog V_{CC}**. A separate V_{CC} input for the phase-locked loop circuitry.	—
CEX2:0 CEX3 CEX4	I/O	**Programmable Counter Array (PCA) Input/Output Pins**. These are input signals for the PCA capture mode and output signals for the PCA compare mode and PCA PWM mode.	P1.5:3 P1.6/WAIT# P1.7/A17/WCLK
D_{M0}, D_{P0}	I/O	**USB Port 0**. D_{P0} and D_{M0} are the data plus and data minus lines of USB port 0, the upstream differential port. These lines do not have internal pullup resistors. Provide an external 1.5 KΩ pullup resistor at D_{P0} to indicate the connection of a fullspeed device. **NOTE:** D_{P0} low **and** D_{M0} low signals an SE0 (USB reset), causing the 8*x*930H*x* to stay in reset.	—
D_{M1}, D_{P1} D_{M2}, D_{P2} D_{M3}, D_{P3} D_{M5}, D_{P5}	I/O	**USB Ports 1, 2, 3, and 5**. D_{P1}, D_{P2}, D_{P3}, D_{M1}, D_{M2}, D_{M3}, D_{M5}, and D_{P5} are the data plus and data minus lines of USB ports 1, 2, 3, and 5, the four downstream differential ports. These lines have no internal pulldown resistors. Provide an external 15 KΩ pulldown resistor at each of these pins. (See “Unused Downstream Ports” on page 33.)	—

Table 10. Signal Description (Sheet 2 of 4)

Signal Name	Type	Description	Alternate Function
EA#	I	**External Access**. Directs program memory accesses to on-chip or off-chip code memory. When EA# is connected to ground, all program memory accesses are off-chip. When EA# is connected to V_{CC}, program accesses on-chip ROM if the address is within the range of the on-chip ROM; otherwise, the access is off-chip. The value of EA# is latched at reset. For devices without on-chip ROM, EA# must be connected to ground.	—
ECAP	I	**External Capacitor**. Connect a 1 µF or larger capacitor between this pin and V_{SS} to ensure proper operation of the differential line drivers.	—
ECI	I	**PCA External Clock Input**. External clock input to the 16-bit PCA timer.	P1.2
INT1:0#	I	**External Interrupts 0 and 1**. These inputs set the IE1:0 interrupt flags in the TCON register. Bits IT1:0 in TCON select the triggering method: edge-triggered (high-to-low) or level triggered (active low). INT1:0 also serves as external run control for timer1:0 when selected by GATE1:0# in TCON.	P3.3:2
OVRI#	I	**Overcurrent Sense.** Senses input to indicate an overcurrent condition for a bus-powered USB device on an external downstream port. Active low.	—
P0.7:0	I/O	**Port 0**. This is an 8-bit, open-drain, bidirectional I/O port.	AD7:0
P1.0 P1.1 P1.2 P1.5:3 P1.6 P1.7	I/O	**Port 1**. This is an 8-bit, bidirectional I/O port with internal pull-ups.	T2 T2EX ECI CEX2:0 CEX3/WAIT# CEX4/A17/WCLK
P2.7:0	I/O	**Port 2**. An 8-bit, bidirectional I/O port with internal pull-ups.	A15:8
P3.0 P3.1 P3.3:2 P3.5:4 P3.6 P3.7	I/O	**Port 3**. An 8-bit, bidirectional I/O port with internal pull-ups.	RXD TXD INT1:0# T1:0 WR# RD#/A16
PLLSEL2:0	I	**Phase-locked Loop Select**. Three-bit code selects USB data rate (see Table 13 on page 17).	—
PSEN#	O	**Program Store Enable**. Read signal output. Asserted for the memory address range determined by bits RD1:0 in configuration byte UCONFIG0 (see RD# and Table 11).	—
RD#	O	**Read.** Read signal output to external data memory. Asserted only for RD1:0 = 11. See configuration byte UCONFIG0. (Also see PSEN# and Table 11).	P3.7/A16

Table 10. Signal Description (Sheet 3 of 4)

Signal Name	Type	Description	Alternate Function
RST	I	**Reset**. Reset input to the chip. Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pulldown resistor; connecting a capacitor between this pin and Vcc implements power-on reset. Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation.	—
RXD	I/O	**Receive Serial Data**. RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2, and 3.	P3.0
SOF#	O	**Start of Frame**. Start of frame pulse. Active low. Asserted for 8 states (see Table 13) when frame timer is locked to USB frame timing and when SOF token or artificial SOF is detected.	—
T1:0	I	**Timer 1:0 External Clock Input**. When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count.	P3.5:4
T2	I/O	**Timer 2 Clock Input/Output**. For the timer 2 capture mode, this signal is the external clock input. For the clock-out mode, it is the timer 2 clock output.	P1.0
T2EX	I	**Timer 2 External Input**. In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 registers to be reloaded. In the up-down counter mode, this signal determines the count direction: 1 = up, 0 = down.	P1.1
TXD	O	**Transmit Serial Data**. TXD outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2, and 3.	P3.1
UPWEN#	O	**USB Power Enable.** A low signal on this pin applies power to all three external downstream ports.	—
V_{CC}	PWR	**Supply Voltage**. Connect this pin to the +5V supply voltage.	—
V_{CCP}	PWR	**Supply Voltage for I/O Buffers**. Connect this pin to the +5V supply voltage.	—
V_{SS}	GND	**Circuit Ground**. Connect this pin to ground.	—
V_{SSP}	GND	**Circuit Ground for I/O Buffers**. Connect this pin to ground.	—
WAIT#	I	**Real-time Wait State Input.** The real-time WAIT# input is enabled by writing a logical ‘1’ to the WCON.0 (RTWE) bit at S:A7H. During bus cycles, the external memory system can signal ‘system ready’ to the microcontroller in real time by controlling the WAIT# input signal on the port 1.6 input.	P1.6/CEX3
WCLK	O	**Wait Clock Output.** The real-time WCLK output is driven at port 1.7 (WCLK) by writing a logical ‘1’ to the WCON.1 (RTWCE) bit at S:A7H. When enabled, the WCLK output produces a square wave signal with a period of TCLK.	P1.7/CEX4/A17

Table 10. Signal Description (Sheet 4 of 4)

Signal Name	Type	Description	Alternate Function
WR#	O	**Write.** Write signal output to external memory (See Table 11).	P3.6
XTAL1	I	**Oscillator Amplifier Input**. When implementing the on-chip oscillator, connect the external crystal/resonator across XTAL1 and XTAL2. If an external clock source is used, then connect it to this pin.	—
XTAL2	O	**Oscillator Amplifier Output**. When implementing the on-chip oscillator, connect the external crystal/resonator across XTAL1 and XTAL2. If an external oscillator is used, then leave XTAL2 unconnected.	—

Table 11. Memory Signal Selections (RD1:0) †

RD1:0	A17/P1.7/ CEX4/WCLK	A16/P3.7/RD#	PSEN#	WR#	Features
0 0	A17	A16	Asserted for all addresses	Asserted for writes to all memory locations	256-Kbyte external address space
0 1	P1.7/CEX4/WCLK	A16	Asserted for all addresses	Asserted for writes to all memory locations	128-Kbyte external address space
1 0	P1.7/CEX4/WCLK	P3.7 only	Asserted for all addresses	Asserted for writes to all memory locations	64-Kbyte external address space One additional port pin
1 1	P1.7/CEX4/WCLK	RD# asserted for addresses ≤ 7F:FFFFH	Asserted for addresses ≥ 80:0000H	Asserted only for writes to MCS® 51 microcontroller data memory locations.	Compatible with MCS 51 microcontrollers. Separate 64-Kbyte external program and data memories.

† RD1:0 are bits 3:2 of configuration byte UCONFIG0. Refer to Figure 4-3 on page 4-5 in the *8x930Ax, 8x930Hx Universal Serial Bus Micorcontroller User's Manual*.

5.0 ADDRESS MAP

Table 12. 8*x*930H*x* Address Map

Internal Address)	Description	Notes
FF:FFFFH FF:4000H	External Memory except the top eight bytes (FF:FFF8H – FF:FFFFH) which are reserved for the configuration array.	1, 2, 3
FF:FFFFH FF:0000H	External memory or on-chip nonvolatile memory (8 Kbytes FF:0000H – FF:1FFFH, 16 Kbytes FF:0000H – FF:3FFFH).	2, 4, 5
FE:FFFFH FE:0000H	External Memory	2
FD:FFFFH 02:0000H	Reserved Addresses	6
01:FFFFH 01:0000H	External Memory	2
00:FFFFH 00:0420H	External Memory	4
00:041FH 00:0080H	On-chip RAM	4
00:007FH 00:0020H	On-chip RAM	7
00:001FH 00:0000H	Storage for R0–R7 of Register File	8, 9

NOTES:
1. 18 address lines are bonded out (A15:0, A16:0, or A17:0 selected during chip configuration).
2. Data in this area is accessible by indirect addressing only.
3. Eight addresses at the top of all external memory maps are reserved for current and future device Configuration Byte information.
4. Data is accessible by direct and indirect addressing.
5. Devices reset into internal or external starting locations depending on the state of EA# and configuration byte information. See EA# signal description in Table 5. See also UCONFIG1:0 bit definitions in the *8x930Ax, 8x930Hx Universal Serial Bus Micorcontroller User's Manual.*
6. This reserved area returns unspecified values. Software can execute a write to the reserved area, but nothing is actually written.
7. Data is accessible by direct, indirect, and bit addressing.
8. The special function registers (SFRs) and the register file have separate internal address spaces.
9. Data is accessible by direct, indirect, and register addressing.

6.0 ELECTRICAL CHARACTERISTICS

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under Bias..... –40°C to +85°C
Storage Temperature ..... –65°C to +150°C
Voltage on Any Pins to V_{SS} .....–0.5 V to +6.5 V
I_{OL} per I/O Pin..... 15 mA
Power Dissipation (1)..... 1.5 W

OPERATING CONDITIONS†

T_A (Ambient Temperature Under Bias):
Commercial..... -0°C to +70°C
V_{CC} / V_{CCP} (Digital Supply Voltage) ..... 4.40 V to 5.25 V
V_{SS} / V_{SSP}..... 0 V
AV_{CC} (Analog Supply Voltage) ..... 4.40 V to 5.25 V
F_{OSC} ..... 12 MHz

NOTE: Maximum power dissipation is based on package heat-transfer limitations, not device power consumption.

† ***WARNING****: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

6.1 Operating Frequencies

Table 13. 8*x*930H*x* Operating Frequency

PLLSEL2:0 Pin 43, 42, 44 (1)	XTAL1 Frequency (F_{OSC})	USB Rate (2)	Internal Frequency for CPU and Peripherals ($1/T_{CLK}$) (3)	XTAL1 Clocks per State (T_{OSC}/state) (5)	Comments
110	12 MHz	12 Mbps (Full Speed)	12 MHz (4)	1	PLL On

NOTES:
1. Other PLLSEL*x* combinations are not valid.
2. The sampling rate is four times the USB rate.
3. The AC timing specification (Table 16) defines the following symbol: CPU frequency = F_{CLK} = $1/T_{CLK}$.
4. The 8*x*930H*x* CPU and peripheral frequency is 3 MHz (low clock mode) until the LC bit in PCON is cleared by user firmware.
5. When the CPU is operating in low clock mode (3 MHz), 1 state equals 4 T_{osc}.

6.2 DC Characteristics

Table 14. DC Characteristics at Operating Conditions (Sheet 1 of 2)

Symbol	Parameter	Min	Typical (1)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#)	–0.5		0.2 V_{CC} – 0.1	V	
V_{IL1}	Input Low Voltage (EA#)	0		0.2 V_{CC} – 0.3	V	
V_{IH}	Input High Voltage (except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (port 1, 2, 3)			0.3 0.45 1.0	V	I_{OL} = 100 µA (2) (3) I_{OL} = 1.6 mA I_{OL} = 3.5 mA
V_{OL1}	Output Low Voltage (port 0, ALE, PSEN#, SOF#)			0.3 0.45 1.0	V	I_{OL} = 200 µA (2) (3) I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (port 1, 2, 3, ALE, PSEN#, SOF#)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = –10 µA (4) I_{OH} = –30 µA I_{OH} = –60 µA
V_{OH1}	Output High Voltage (port 0 in external address space)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = –200 µA (4) I_{OH} = –3.2 mA I_{OH} = –7.0 mA
I_{IL}	Logical 0 Input Current (port 1,2,3)			–150	µA	V_{IN} = 0.45 V
I_{LI}	Input Leakage Current (port 0)			±10	µA	0.45 < V_{IN} < V_{CC}
I_{TL}	Logical 1-to-0 Transition Current (Port 1, 2,3)			-650	µA	V_{IN} = 2.0 V
R_{RST}	RST Pulldown Resistor	40		225	KΩ	
C_{IO}			10		pF	F_{OSC} = 12 MHz T_A = 25°C
I_{PD}	Powerdown Current Normal powerdown USB suspend		 25 145	 75 175	µA	

Table 14. DC Characteristics at Operating Conditions (Sheet 2 of 2)

Symbol	Parameter	Min	Typical (1)	Max	Units	Test Conditions
I_{DL}	Idle Mode I_{CC}			60	mA	Full speed (in low clock mode) PLLSEL2:0 = 110 F_{CLK} = 3 MHz
				110		Full speed (not in low clock mode) PLLSEL2:0 = 110 F_{CLK} = 12 MHz
I_{CC}	Active Current			75	mA	Full speed (in low clock mode) PLLSEL2:0 = 110 F_{CLK} = 3 MHz
				170		Full speed (not in low clock mode) PLLSEL2:0 = 110 F_{CLK} = 12 MHz

NOTE:

1. Typical values are obtained using V_{CC} = 5.0V, T_A = 25°C and are not guaranteed.
2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OH} per port pin:10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1-3: 15 mA
   Maximum Total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test conditions, then V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
3. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt trigger or CMOS-level input logic.
4. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN to drop below the V_{CC} specification when the address lines are stabilizing.

6.3 Explanation of Timing Symbols

Table 15 defines the timing symbols used in Tables 11 through 14 and the associated timing diagrams. They have the form T_{XXYY}, where the character pairs represent a signal and its condition. Timing symbols represent the time between two signal / condition points.

Table 15. AC Timing Symbol Definitions

Character	Signal(s)
A	Address: A17, A16, A15:8, A7:0
C	Wait Clock (WCLK), External Clock (XTAL1)
D	Data In: D7:0, RXD
L	ALE
Q	Data Out: D7:0, RXD
R	Read: RD#/PSEN#
W	Write: WR#
X	TXD
Y	WAIT#

Character	Condition
H	High
L	Low
V	Valid, Setup
X	No Longer Valid, Hold
Z	Floating (low impedance)

6.4 System Bus AC Characteristics

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall times = 10 ns, F_{OSC} = 12 MHz.

Table 16. AC Characteristics at Operating Conditions (Sheet 1 of 2)

Symbol	Parameter	CPU Frequency @ 12 MHz (M, N = 0)	CPU Frequency (F_{CLK}) Variable		Units
			Min	Max	
T_{CLK}	1/(CPU Frequency)	83.33 (Typical)			ns (1) (2)
T_{LHLL}	ALE Pulse Width	34.66	$(0.5+M)T_{CLK} - 7$		ns (4)
T_{AVLL}	Address Valid to ALE Low	21.66	$(0.5+M)T_{CLK} - 20$		ns (4)
T_{LLAX}	Address Hold after ALE Low	4	4		ns
T_{RLRH} (3)	RD# or PSEN# Pulse Width	73.33	$(1+N)T_{CLK} - 10$		ns (5)
T_{WLWH}	WR# Pulse Width	71.33	$(1+N)T_{CLK} - 12$		ns (5)
T_{LLRL} (3)	ALE Low to RD# or PSEN# Low	5	5		ns
T_{LHAX}	ALE High to Address Hold	40.33	$(1+M)T_{CLK} - 43$		ns (4)
T_{RLDV} (3)	RD# or PSEN# Low to Valid Data/Instruction In	50.33		$(1+N)T_{CLK} - 33$	ns (5)
T_{RHDX} (3)	Data/Instruct. Hold After RD# or PSEN# High	0	0		ns
T_{RLAZ} (3)	RD# or PSEN# Low to Address Float	0		0	ns
T_{RHDZ1} (3)	Instruct. Float After PSEN# High	10		10	ns
T_{RHDZ2} (3)	Data Float After RD# or PSEN# High	83.33		T_{CLK}	ns
T_{RHLH1} (3)	PSEN# High to ALE High (instruction)	10	10		ns
T_{RHLH2} (3)	RD# or PSEN# High to ALE High (data)	83.33	T_{CLK}		ns
T_{WHLH}	WR# High to ALE High	88.33	$T_{CLK} + 5$		ns
T_{AVDV1}	Address (Port 0) Valid to Valid Data/Instruction In	98.66		$(2+M+N)T_{CLK} - 68$	ns (4) (5)

NOTES:
1. Refer to Table 13 for CPU frequencies versus XTAL1 frequencies.
2. XTAL1 frequency is ± 0.25% for full speed and ± 1.5% for low speed.
3. Specifications for PSEN# are identical to those for RD#.
4. M = 0,1 is the extended ALE state.
5. N = 0,1,2,3 is the RD#/PSEN#/WR# wait state.

Table 16. AC Characteristics at Operating Conditions (Sheet 2 of 2)

Symbol	Parameter	CPU Frequency @ 12 MHz (M, N = 0)	CPU Frequency (F_{CLK}) Variable		Units
			Min	Max	
T_{AVDV2}	Address (Port 2) Valid to Valid Data/Instruction In	118.66		$(2+M+N)T_{CLK} - 48$	ns (4) (5)
T_{AVDV3}	Address (Port 2) Valid to Valid Instruction In	23.33		$(1+N)T_{CLK} - 60$	ns (5)
T_{AVRL} (3)	Address Valid to RD# or PSEN# Low	37.33	$(1+M)T_{CLK} - 46$		ns (4)
T_{AVWL1}	Address (Port 0) Valid to WR# Low	37.33	$(1+M)T_{CLK} - 46$		ns (4)
T_{AVWL2}	Address (Port 2) Valid to WR# Low	66.33	$(1+M)T_{CLK} - 17$		ns (4)
T_{WHQX}	Data Hold after WR# High	28.66	$0.5\ T_{CLK} - 13$		ns
T_{QVWH}	Data Valid to WR# High	68.33	$(1+N)T_{CLK} - 15$		ns (5)
T_{WHAX}	WR# High to Address Hold	70.33	$T_{CLK} - 13$		ns

NOTES:
1. Refer to Table 13 for CPU frequencies versus XTAL1 frequencies.
2. XTAL1 frequency is ± 0.25% for full speed and ± 1.5% for low speed.
3. Specifications for PSEN# are identical to those for RD#.
4. M = 0,1 is the extended ALE state.
5. N = 0,1,2,3 is the RD#/PSEN#/WR# wait state.

6.4.1 SYSTEM BUS TIMING DIAGRAMS

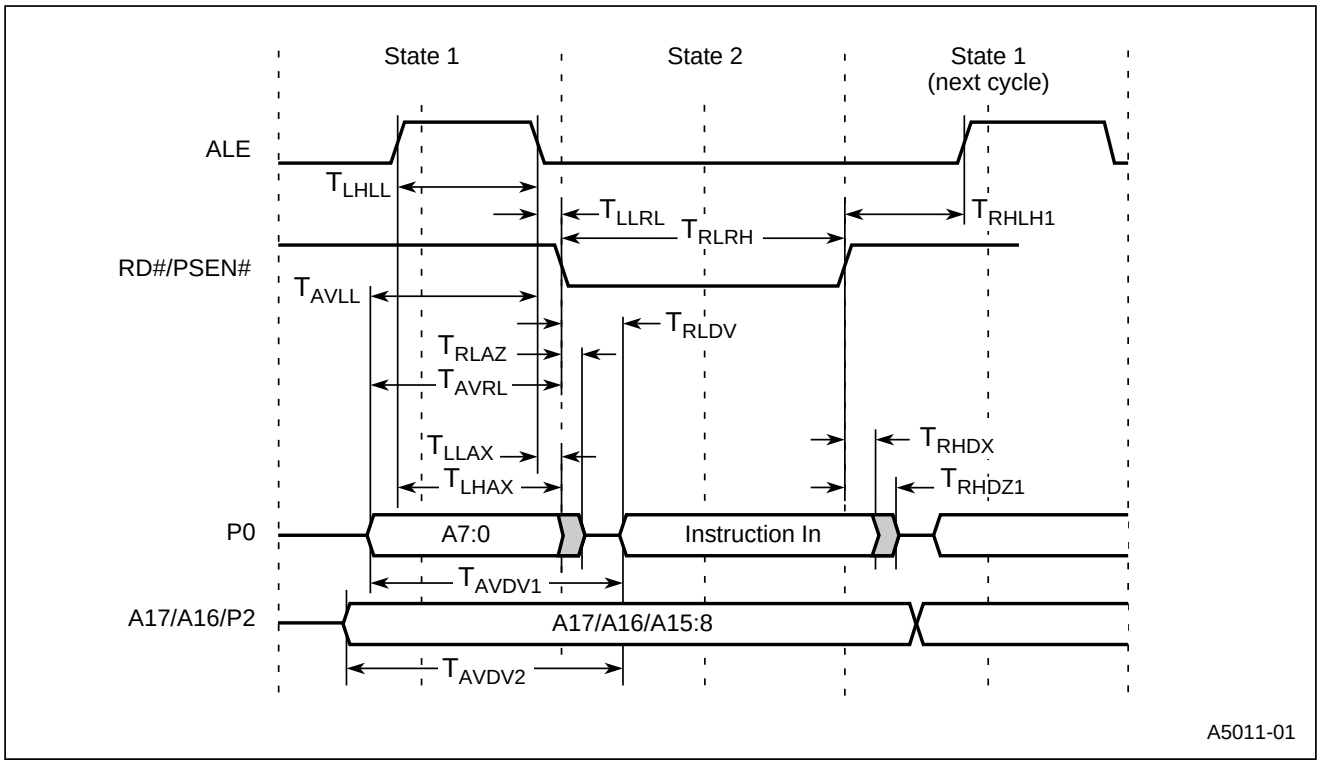


Figure 6. 8x930Hx Code Fetch, Nonpage Mode

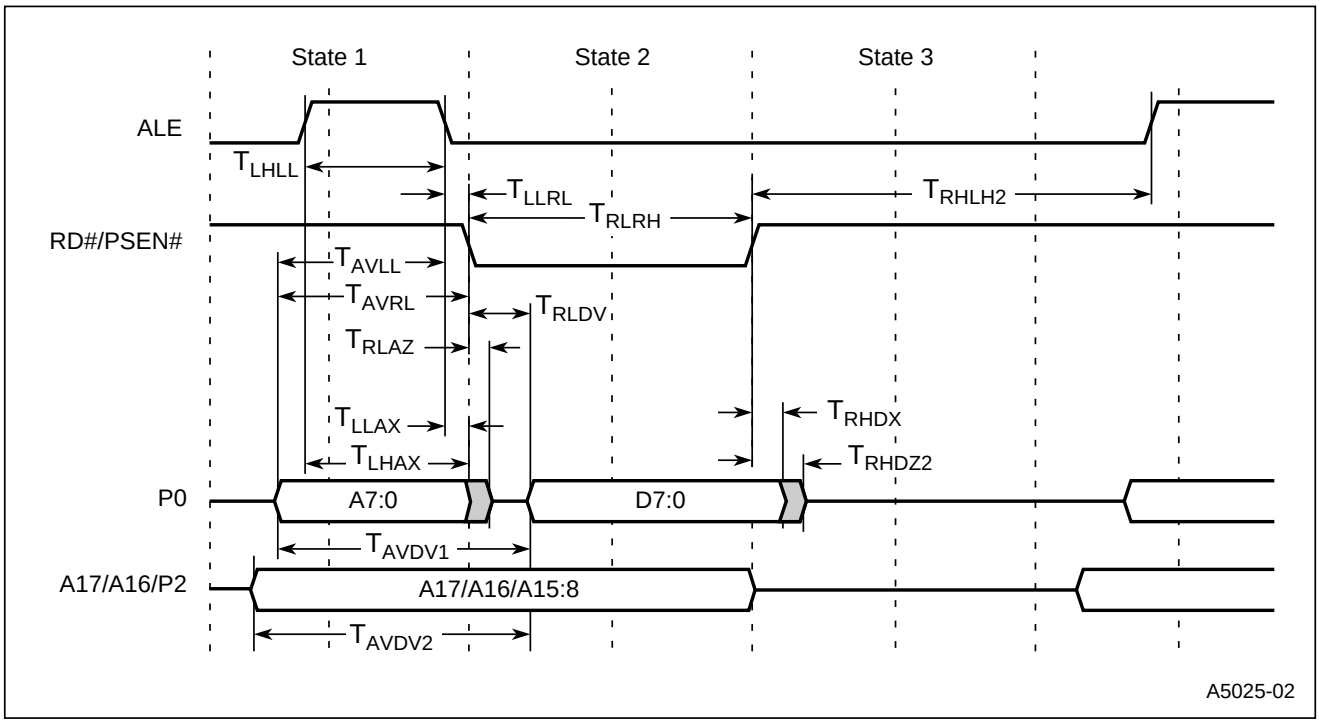


Figure 7. 8*x*930H*x* Data Read, Nonpage Mode

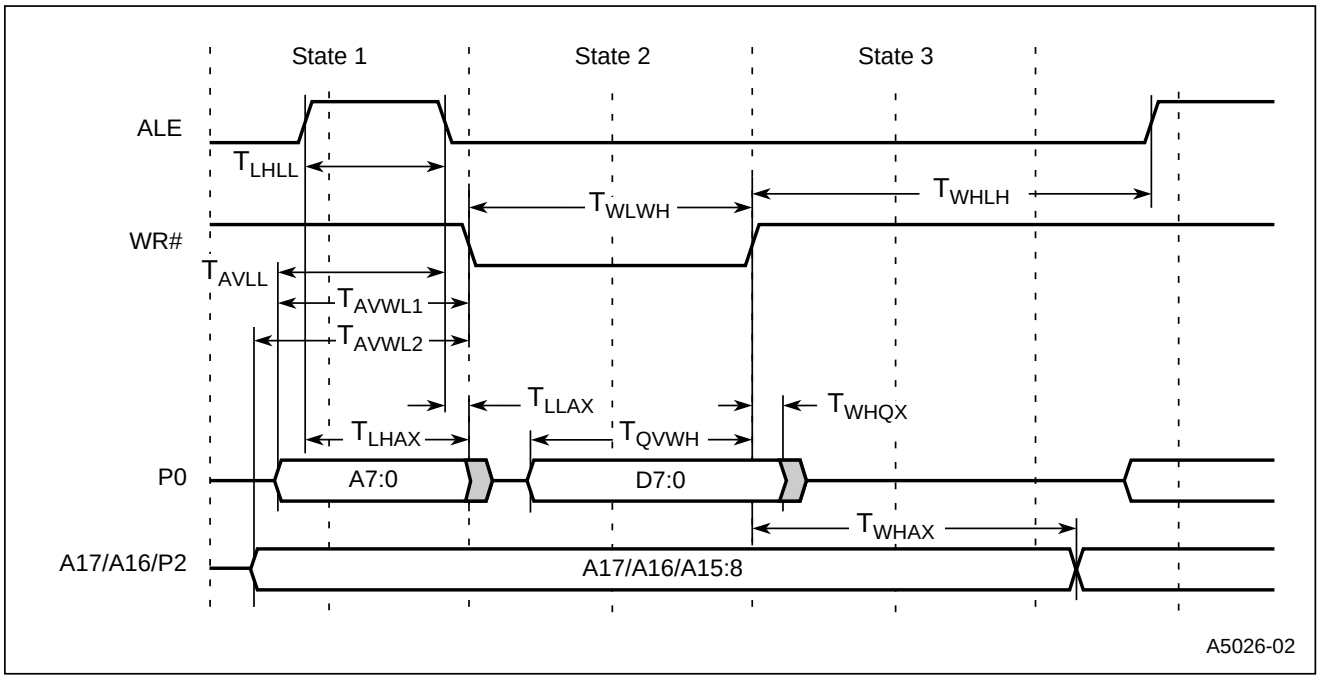


Figure 8. 8*x*930H*x* Data Write, Nonpage Mode

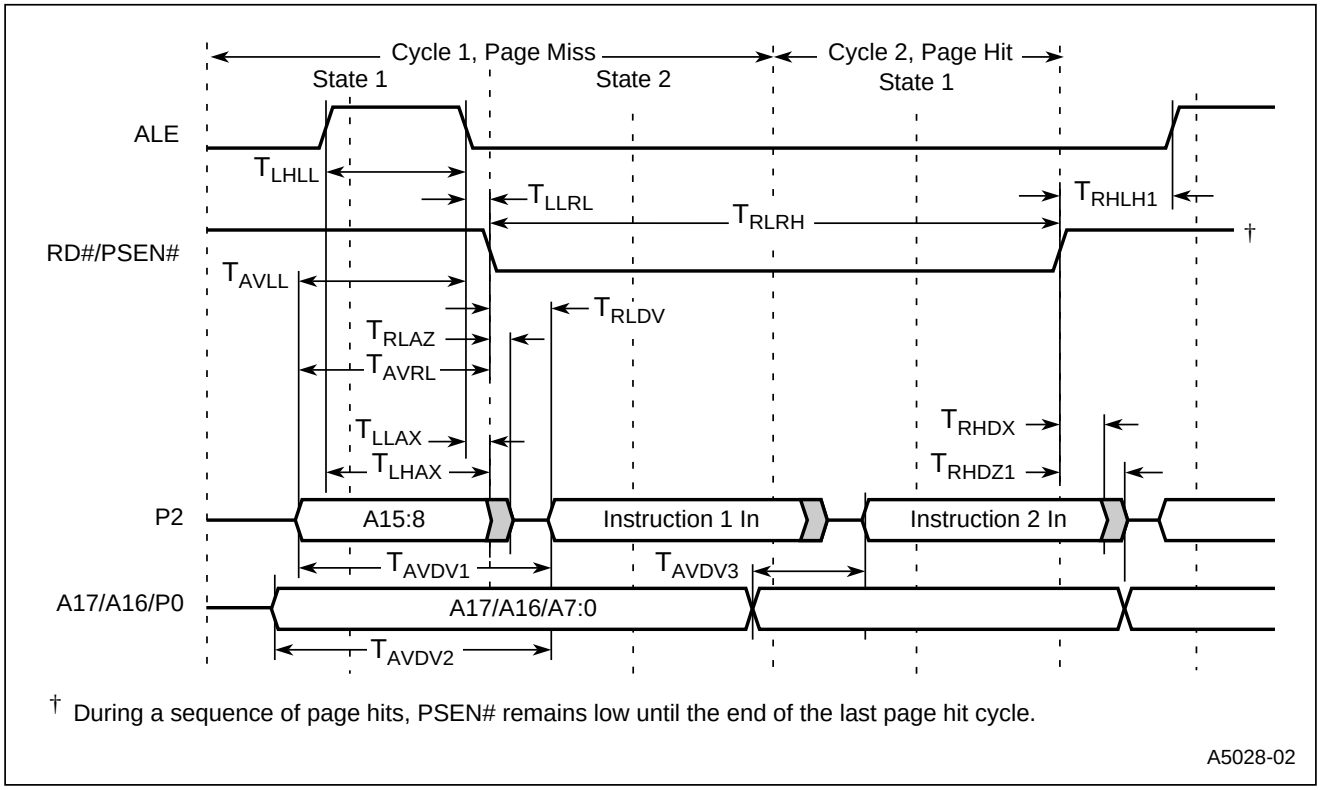


Figure 9. 8*x*930H*x* Code Fetch, Page Mode

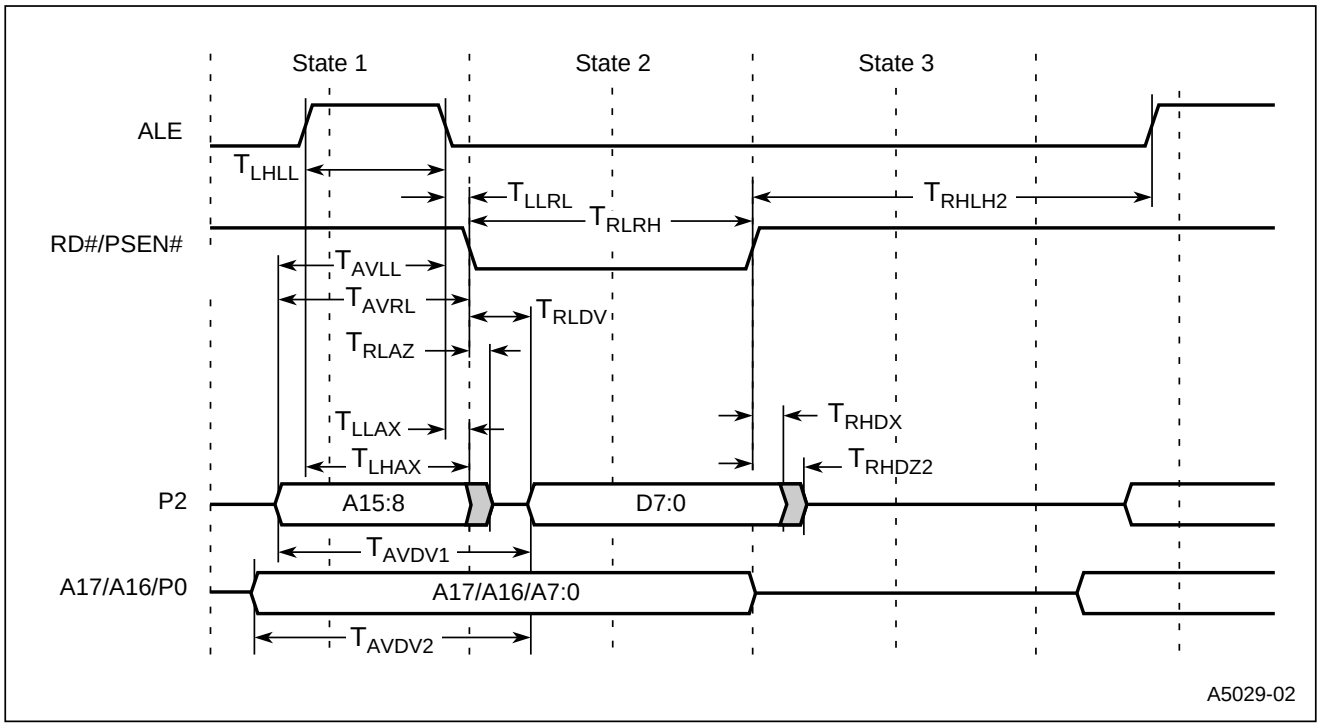


Figure 10. 8x930Hx Data Read, Page Mode

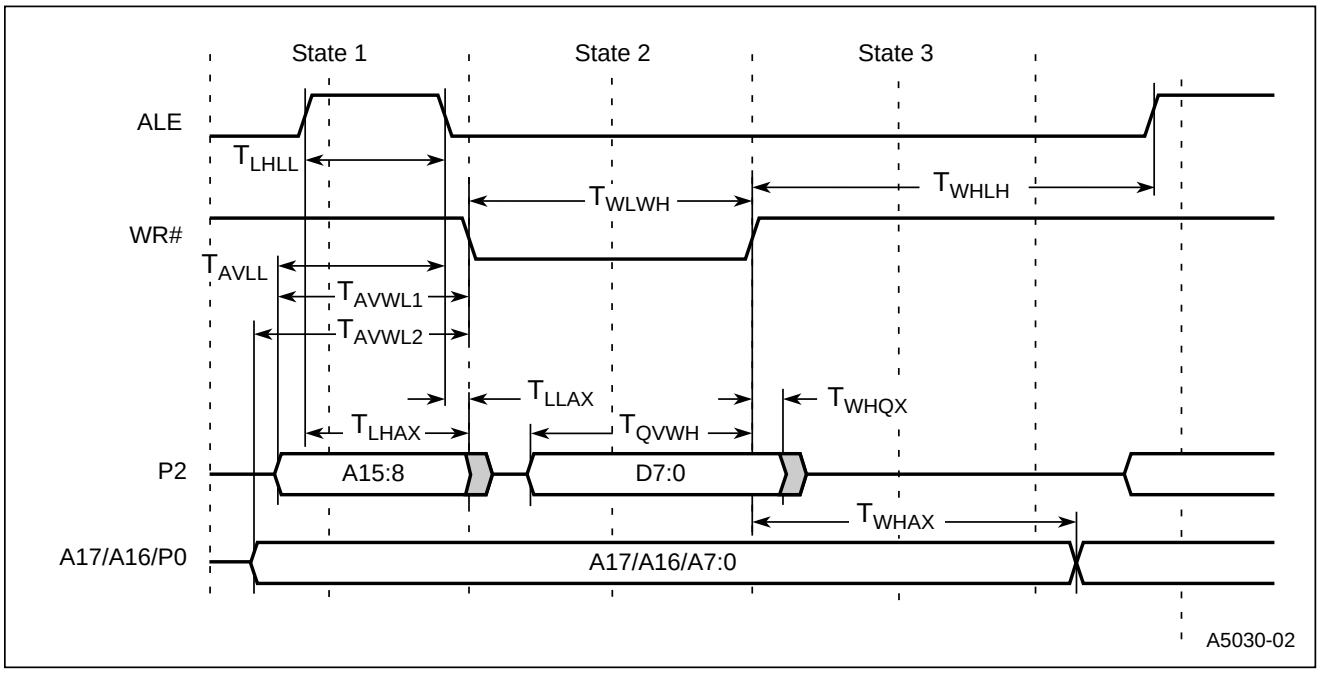


Figure 11. 8x930Hx Data Write, Page Mode

6.4.2 REAL-TIME WAIT STATE FUNCTION AC CHARACTERISTICS

Table 17. Real-time Wait State AC Timing Specifications

Symbol	Parameter	F_{CLK} Variable (1) (2)			Units
		Min	Typ	Max	
T_{CLYV}	WCLK Low to WAIT# Setup	0		0.5 T_{CLK} – 13	ns
T_{CLYX}	WAIT# Hold after WCLK Low	(W)T_{CLK} + 5		(0.5+W)T_{CLK} – 13	ns
T_{RLYV} (2)	PSEN# or RD# Low to WAIT# Setup	0		0.5 T_{CLK} – 13	ns
T_{RLYX}	WAIT# Hold after PSEN# or RD# Low	(W)T_{CLK} + 5		(0.5+W)T_{CLK} – 13	ns
T_{WLYV}	WR# Low to WAIT# Setup	0		0.5 T_{CLK} – 13	ns
T_{WLYX}	WAIT# Hold after WR# Low	(W)T_{CLK} + 5		(0.5+W)T_{CLK} – 13	ns

NOTES:
1. W is the number of real-time wait states (0, 1, 2, ... highest possible number).
2. The real-time wait function has a critical timing for instruction reads. It is not advisable to use this feature for instruction reads during page mode.

6.4.3 REAL-TIME WAIT STATE FUNCTION TIMING DIAGRAMS

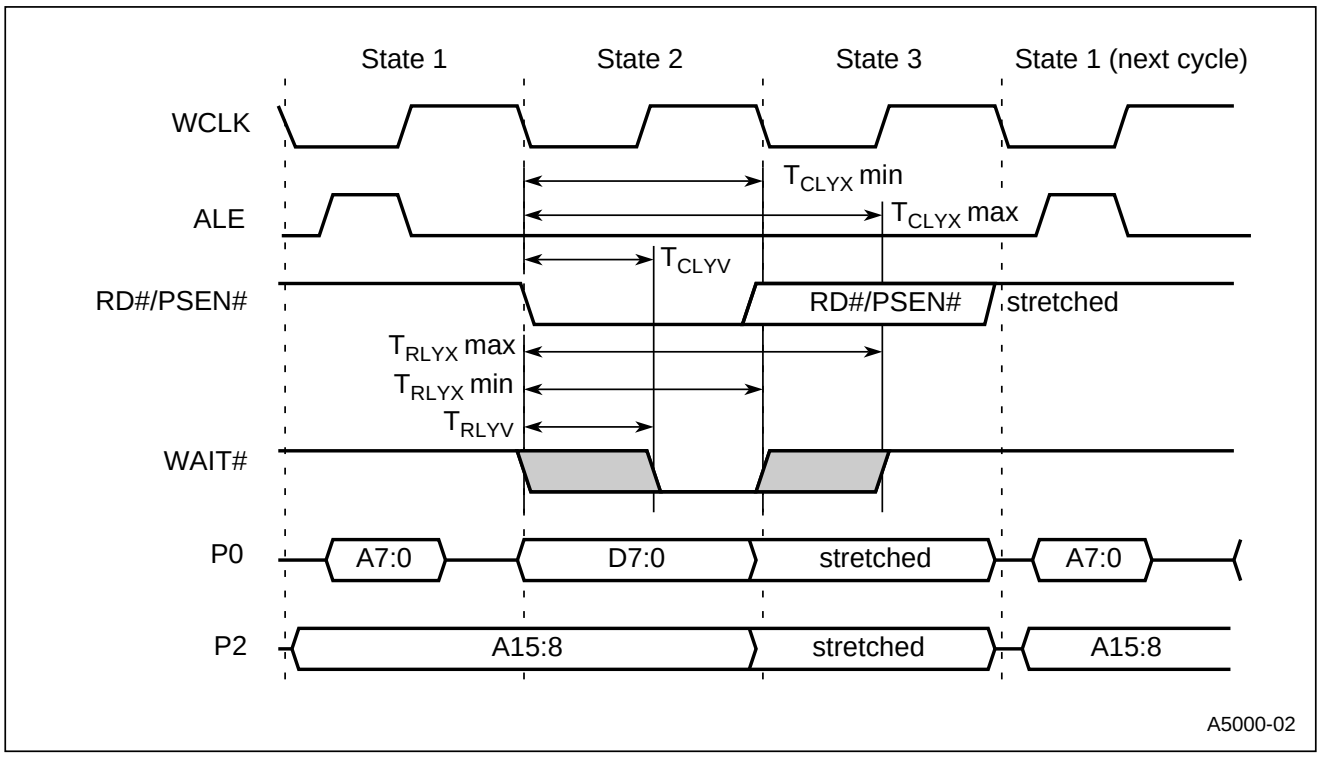


Figure 12. External Code Fetch/Data Read (Nonpage Mode, Real-time Wait State)

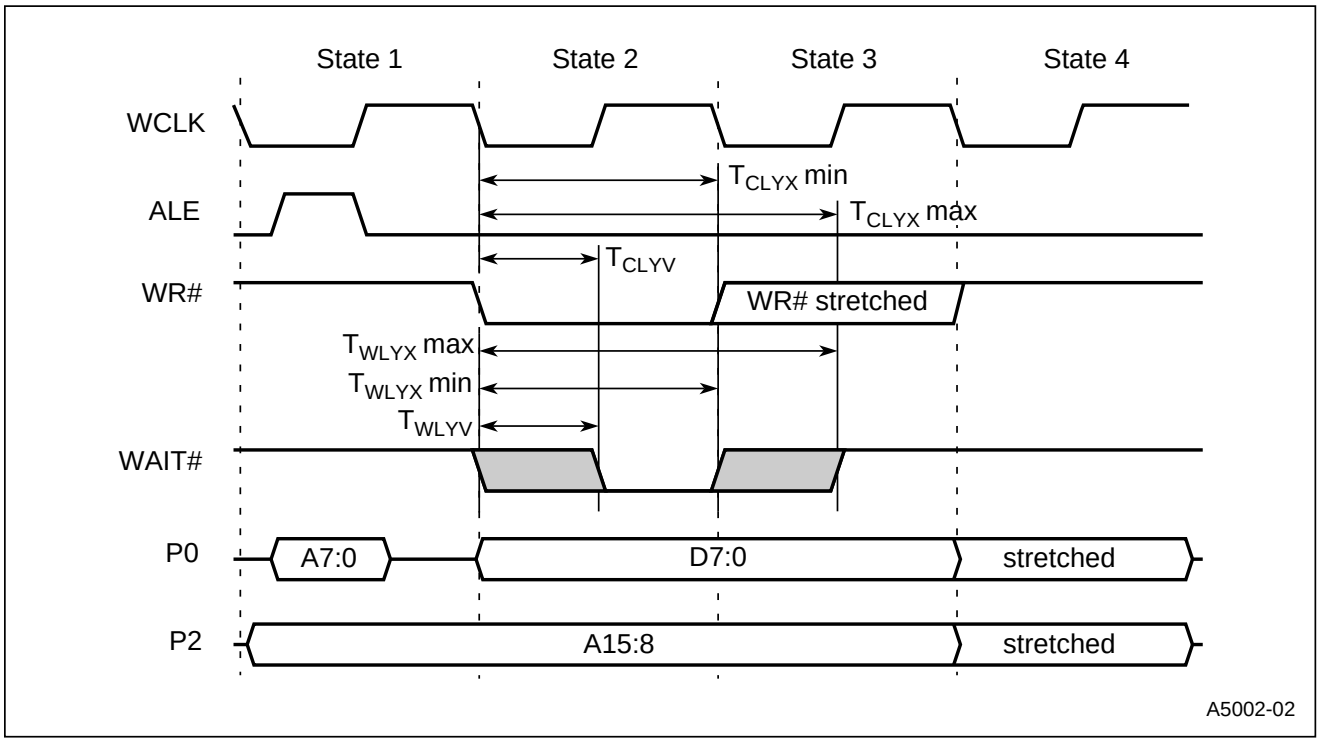


Figure 13. External Data Write (Nonpage Mode, Real-time Wait State)

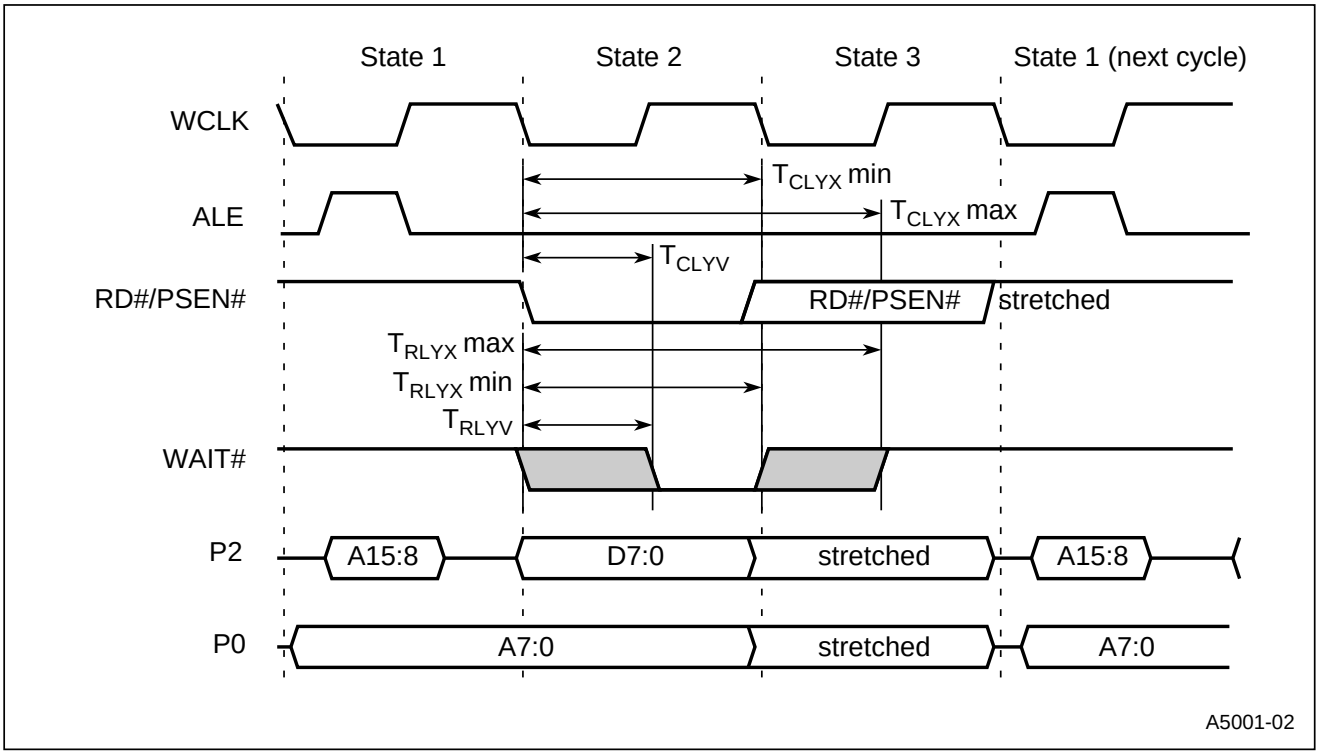


Figure 14. External Data Read (Page Mode, Real-time Wait State)

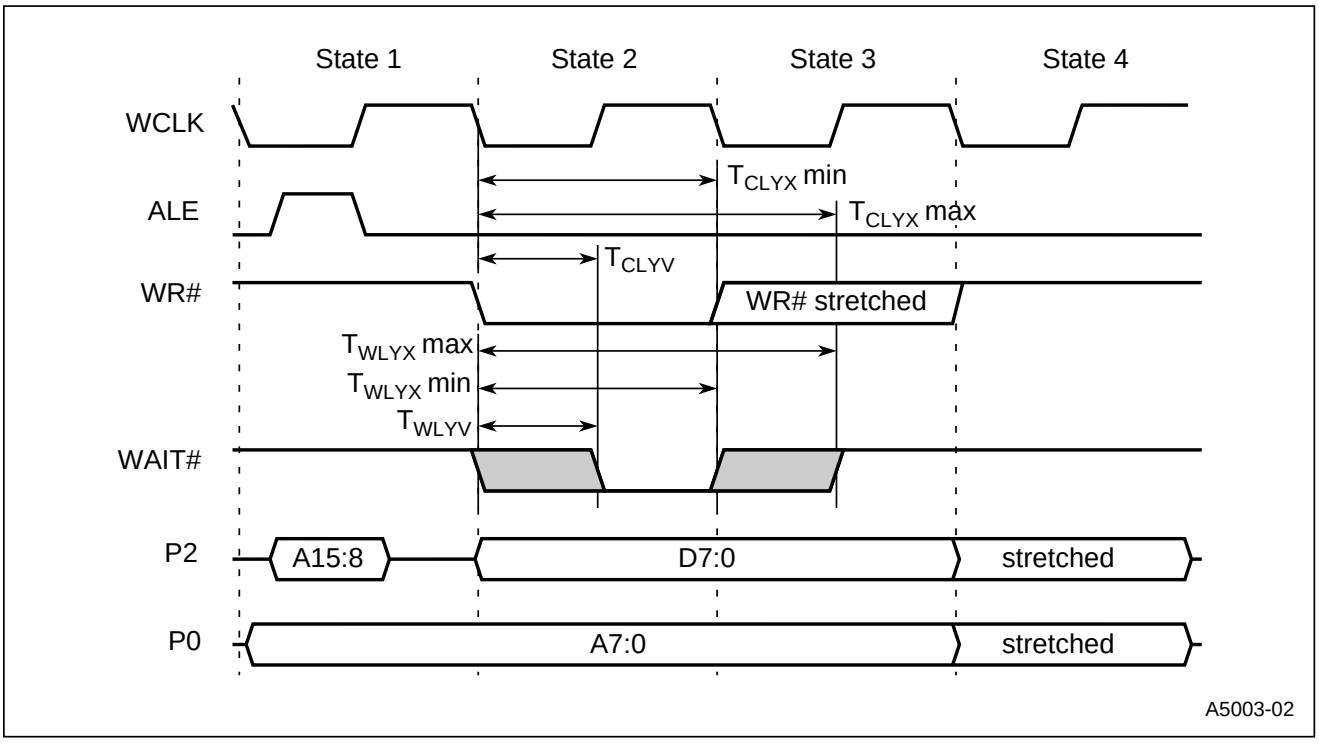


Figure 15. External Data Write (Page Mode, Real-time Wait State)

6.5 AC Characteristics — Synchronous Mode 0

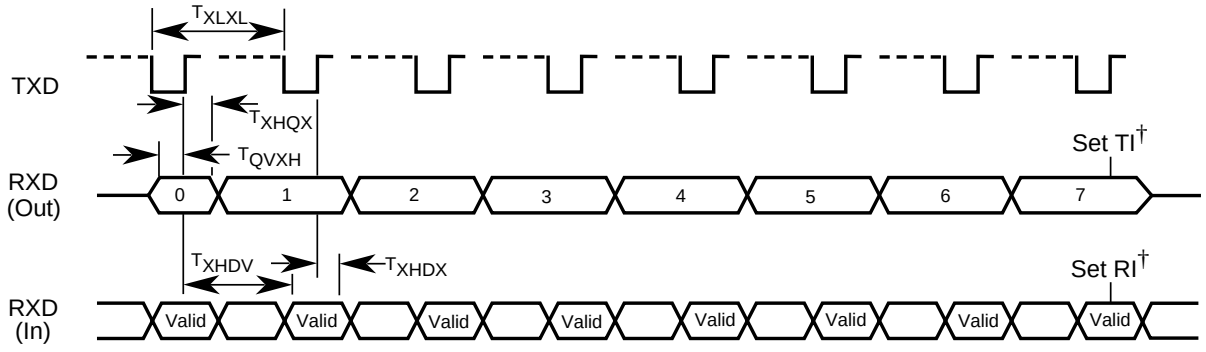


Figure 16. Serial Port Waveform — Synchronous Mode 0

Table 18. Serial Port Timing — Synchronous Mode 0

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Cycle Time	6 T_{OSC}		ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	5 T_{OSC} – 133		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	T_{OSC} – 50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		5 T_{OSC} – 133	ns

6.6 External Clock Drive

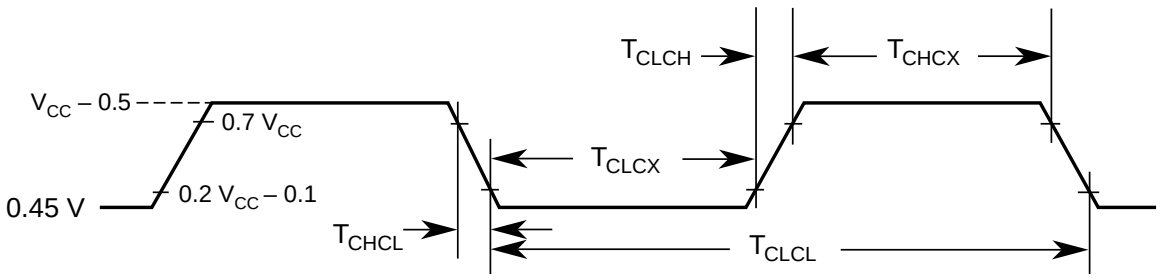
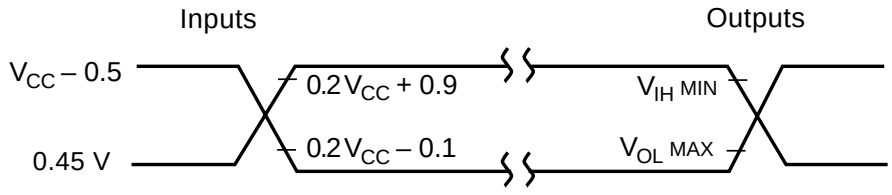


Figure 17. External Clock Drive Waveforms

Table 19. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{OSC}$	Oscillator Frequency (F_{OSC})	6	12	MHz
T_{CHCX}	High Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{CLCX}	Low Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{CLCH}	Rise Time		10	ns
T_{CHCL}	Fall Time		10	ns

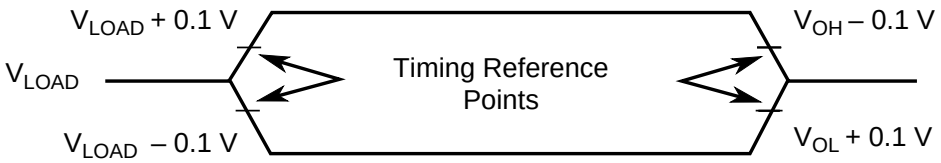
6.7 Testing Waveforms



AC inputs during testing are driven at V_{CC} – 0.5V for a logic 1 and 0.45 V for a logic 0. Timing measurements are made at a min of V_{IH} for a logic 1 and V_{OL} for a logic 0.

A4118-01

Figure 18. AC Testing Input, Output Waveforms



For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} = \pm 20$ mA.

A4117-01

Figure 19. Float Waveforms

7.0 THERMAL CHARACTERISTICS

The microcontroller operates over the commercial temperature range from 0°C to 70°C. All thermal impedance data (see Table 20) is approximate for static air conditions at 1 watt of power dissipation. Values change depending on operating conditions and application requirements. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology. The *Components Quality and Reliability Handbook* (order number 210997) provides quality and reliability information.

Table 20. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
68-pin PLCC	N/A	N/A

8.0 DESIGN CONSIDERATIONS

8.1 External Bus Timing and Peripheral Timing Affected by PLLSEL2:0 Selection

PLLSEL2 (pin 43), PLLSEL1 (pin 42), and PLLSEL0 (pin 44) determine the 8*x*930H*x* internal CPU operating frequency. See Table 13. Operate the 8*x*930H*x* at full speed by setting PLLSEL2:0 to 110.

This provides an internal clock frequency of 12 MHz ($F_{CLK} = F_{OSC}$) and sets the microcontroller state time equal to one oscillator period (T_{OSC}).

The CPU operating frequency influences the timing of all on-chip peripherals. Refer to the *8X930Ax*, 8X930H*x* *Universal Serial Bus Microcontroller User's Manual* for peripheral timing formulas (refer to Table 1 on page 1 for ordering information).

8.2 Low Clock Mode Frequency

The internal clock F_{CLK} distributed to the CPU and peripherals is 3 MHz. Peripheral timing and external bus accesses (including instruction fetch and data read/write) are affected. Refer to Table 13 for clock rates.

8.3 Setting RXFFRC Bit Clears Only the Oldest Packet in the FIFO

If the receive FIFO is set as a dual packet mode, then it can receive two packets. Setting RXFFRC (in RXCON registers) to indicate FIFO Read Complete will **not** flush the entire FIFO; it will flush only the oldest packet. The read marker will be advanced to the location of the read pointer.

8.4 Series Resistor Requirement for Impedance Matching

Per USB rev. 1.0 specification (page 111, section 7.1.1.1), the impedance of the differential driver must be between 29Ω and 44Ω. To match the cable impedance, a series resistor of 27Ω to 33Ω should be connected to each USB line; i.e., on D_{P0} (pin 55) and on D_{M0} (pin 54). If the USB line is improperly terminated or not matched, then signal fidelity will suffer. This condition can be seen on the oscilloscopes as excessive overshoot and undershoot. This condition can potentially introduce bit errors.

8.5 Pullup Resistor Requirement for 8*x*930H*x* Hub devices

The USB specification requires a pullup resistor to allow the host to identify which devices are low speed and which are full speed in order to communicate at the appropriate data rate. For 8*x*930H*x* hub devices (12 Mbps), use a 1.5KΩ pullup resistor (to 3.0 V – 3.6 V) on the D_{P0} line.

8.6 Powerdown Mode Cannot Be Invoked Before USB Suspend

If the 8*x*930H*x* is put into powerdown mode before receiving a USB suspend signal from the host, then a USB resume will not properly wake up the 8*x*930H*x* from powerdown model.

8.7 Unused Downstream Ports

If the USB downstream ports are not used, it is still required that the two data lines be pulled low externally (similar to a disconnect) so that the inputs are not floating. This will eliminate the possibility of induced system noise. When migrating from the 8*x*930HD/HE (3 external downstream port device) to the 8*x*930HF/HG (4 external downstream port device), and the additional USB port is not being used in the application, D_{M5} and D_{P5} will still require 15K external pulldown resistors. Do **not** leave the unused port disconnected.

9.0 8*x*930H*x* ERRATA

The 8*x*930H*x* may contain design defects or errors known as errata. Characterized errata that may cause the 8*x*930H*x*'s operational behavior to deviate from published specifications are documented in a specification update (order number 272962). Specification updates can be obtained from your local Intel sales office or from the World Wide Web (*www.intel.com*).

10.0 DATASHEET REVISION HISTORY

Datasheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

This (-003) revision of the 8*x*930H*x* datasheet replaces earlier product information. The following changes were made in this revision:

1. Added the 8*x*930HF/HG 4 external downstream port device.