Z86E15

CMOS Z8® 8-BIT OTP KEYBOARD CONTROLLER

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Speed (Mhz)
Z86E15	4	188	32	5

Note: *General-Purpose

- 4.5V to 5.5V Operating Range
- 0°C to +70°C Operating Temperature Range
- Low-Power Consumption: 60 mW @ 5 MHz
- Five Vectored, Priority Interrupts from FIve Different Sources
- A Programmable 8-Bit Counter/Timer, with 6-Bit Programmable Prescaler
- Power-On-Reset (POR) Timer, Hardware Watch-Dog Timer (WDT)
- Digital Inputs CMOS Levels with Internal Pull-Up Resistors
- Four Direct Connect LED Drive Ports
- On-Chip RC Oscillator
- Low System EMI Emission

GENERAL DESCRIPTION

The Z86E15 microcontroller (MCU) is a member of the single-chip Z8® MCU family with 4 KB of EPROM and 188 bytes of general-purpose RAM.

The Z86E15 is a pin-compatible, One-Time-Programmable (OTP) version of the Z86K15 Keyboard Controller.

Zilog's CMOS-microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities.

To unburden the program from coping with real-time problems such as counting/timing, the Z86E15 offers an on-chip counter/timer with a large number of user-selectable modes.

Five different internal or external interrupt sources are maskable and prioritized in which a vectored address is provided for efficient interrupt subroutine handling and multitasking functions.

The Z86E15 achieves low EMI by means of several modifications in the output drivers and clock circuitry of the device.

GENERAL DESCRIPTION (Continued)

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only). Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

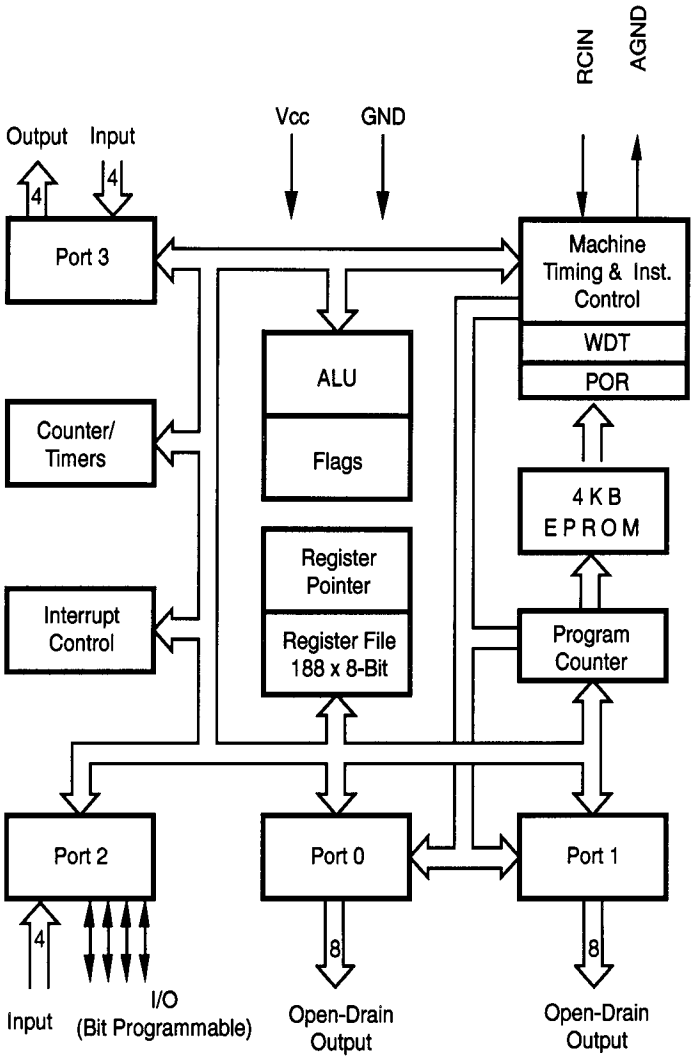
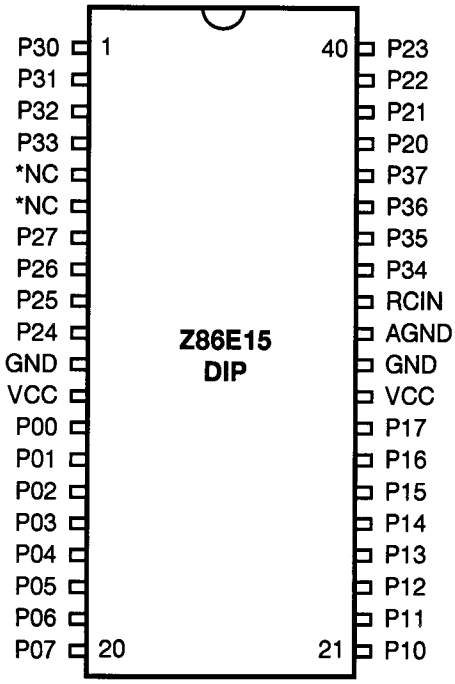


Figure 1. Z86E15 Functional Block Diagram

PIN DESCRIPTION



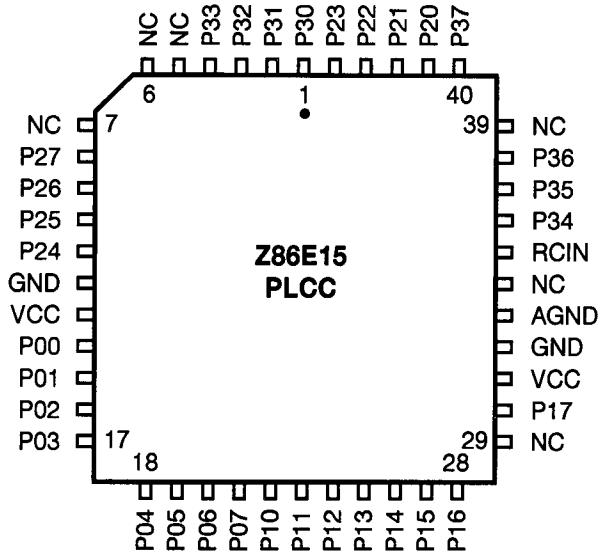
Notes:
*Pin 5 and 6 used for testing Ground during normal operation.
When Pin 5 is connected to V_{cc}. Pin 6 is CLK OUT.
When Pin 5 is connected to GND, Pin 6 outputs nothing.
These pins must be tied to ground in application.

Figure 2. 40-Pin DIP Configuration

Table 1. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1-4	P30-P33	Port 3, Pins 0,1,2,3	Input
5-6	NC	Tied to GND	
7-10	P27-P24	Port 2, Pins 7,6,5,4	In/Output
11	GND	Ground	
12	V_{cc}	Power Supply	Input
13-20	P00-P07	Port 0, Pins 0,1,2,3,4,5,6,7	Output
21-28	P10-P17	Port 1, Pins 0,1,2,3,4,5,6,7	Output
29	V_{cc}	Power Supply	
30	GND	Ground	
31	AGND	Analog Ground	
32	RCIN	RCIN	Input
33-36	P34-P37	Port 3, Pins 4,5,6,7	Output
37-40	P20-P23	Port 2, Pins 0,1,2,3	Input

PIN DESCRIPTION (Continued)

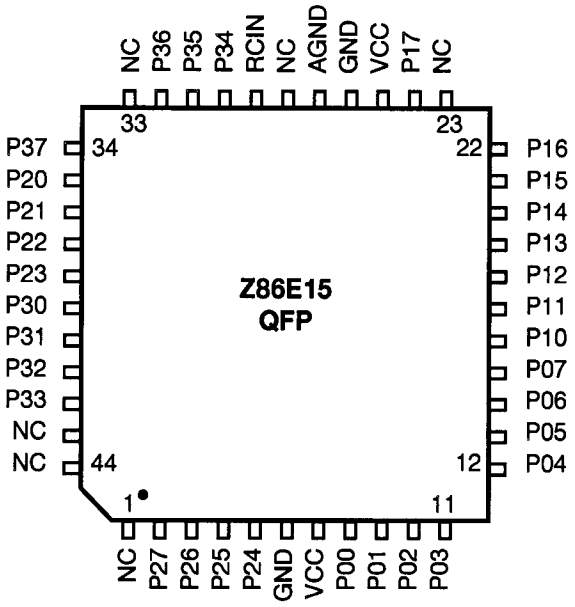


Notes:
Pins 5 and 6 used for testing. Ground during normal operation
When Pin 43 is connected to V_{cc}, Pin 44 is CLKOUT.
When Pin 43 is connected to GND. Pin 44 outputs nothing.

Figure 3. 44-Pin PLCC Pin Assignments

Table 2. 44-Pin PLCC Pin Assignments

Pin #	Symbol	Function	Direction
1-4	P30-P33	Port 3, Pins 0,1,2,3	Input
5-7	NC	Test Pins (GND)	
8-11	P27-P24	Port 2, Pins 4,5,6,7	In/Output
12	GND	Ground	
13	V_{cc}	Power Supply	
14-21	P00-P07	Port 0, Pins 0,1,2,3,4,5,6,7	Output
22-28	P10-P16	Port 1, Pins 0,1,2,3,4,5,6	Output
29	NC	Not Connected	
30	P17	Port 1, Pin 7	Output
31	V_{cc}	Power Supply	
32	GND	Ground	
33	AGND	Analog Ground	
34	NC	Not Connected	
35	RCIN	RCIN	Input
36-38	P34-P36	Port 3, Pins 4,5,6,7	Output
39	NC	Not Connected	
40	P37	Port 3, Pin 7	Output
41-44	P20-P23	Port 2, Pins 0,1,2,3	In/Output



Notes:
Pins 43 and 44 are used for testing ground during normal operation.
When Pin 45 is connected to V_{cc}, Pin 46 is CLKOUT.
When Pin 45 is connected to GND. Pin 46 outputs nothing.

Figure 4. 44-Pin QFP Pin Assignments

Table 3. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
1	NC	Not Connected	
2-5	P24-P27	Port 2, Pins 4,5,6,7	In/Output
6	GND	Ground	
7	V_{cc}	Supply Voltage	
8-15	P00-P07	Port 0, Pins 0,1,2,3,4,5,6,7,	Output
16-22	P10-P16	Port 1, Pins 0,1,2,3,4,5,6	Output
23	NC	Not Connected	
24	P17	Port 1, Pin 7	Output
25	V_{cc}	Supply Voltage	
26	GND	Ground	
27	AGND	Analog Ground	
28	NC	Not Connected	
29	RCIN	RCIN	Input
30-32	P34-P36	Port 3, Pins 4,5,6	Output
33	NC	Not Connected	
34	P37	Port 3, Pin 7	Output
35-38	P20-P23	Port 2, Pins 0,1,2,3	Input
39-42	P30-P33	Port 3, Pins 0,1,2,3	Input
43-44	NC	Test Pins (GND)	

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	°C
T_A	Oper Ambient Temp	0	+105	°C

Note: * Voltage on all pins with respect to GND.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed here apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 5).

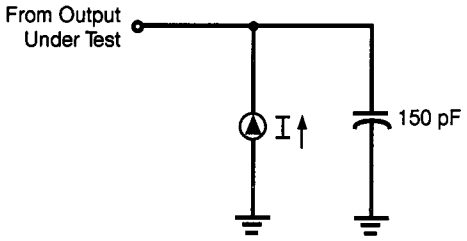


Figure 5. Test Load Diagram

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V; f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Max
Input Capacitance	12 pF
Output Capacitance	12 pF
I/O Capacitance	12 pF

Frequency tolerance ±10%

DC CHARACTERISTICS

V_{CC} = 5.0V ± 10% @ 0°C to +70°C

Sym	Parameter	Min	Max	Typ*	Unit	Condition
V_{CH}	Clock Input High Voltage	0.7 V_{CC}	V_{CC} + 0.3V	2.5	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	GND –0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.3	2.5	V	
V_{IL}	Input Low Voltage	GND –0.3	0.2 V_{CC}	1.5	V	
V_{OH}	Output High Voltage	V_{CC} –0.4		4.7	V	I_{OH} = –2.0 mA (Port 2 out. in P/P Mode)
V_{OH}	Output High Voltage	V_{CC} –0.6			V	I_{OH} = –2.0 mA (see note 1 below.)
V_{OH}	Output High Voltage	V_{CC} –1.0			V	I_{OH} = –2.0 µA (Port 0 and Port 1)
V_{OL}	Output Low Voltage		.4		V	I_{OL} = 4 mA
V_{OL}	Output Low Voltage		.8		V	I_{OL} = 4 mA (see note 1 below.)
I_{OL}	Output Low	10	20		mA	V_{OL} = V_{CC} –2.2 V (see note 1, 2 below.)
I_{OL}	Output Leakage	–1	1	<1	µA	V_{IN} = 0V, 5.25V
I_{CC}	V_{CC} Supply Current		12	6	mA	@ 5.0 MHz
I_{CC1}	HALTt Mode Current			2	mA	@ 5.0 MHz
I_{CC2}	STOP Mode Current		10		µA	
R_p	Pull Up Resistor	6.76	14.04	10.4	Kohm	Port 20-25 and Port 30-33
R_p	Pull Up Resistor (P26-P27) (P0 & P1)	1.8 200	3 500	2.4	Kohm Kohm	

Notes:
* Typical @ 25°C
1. Ports P37-P34. These may be used for LEDs or as general-purpose outputs requiring high sink current.
2. V_{cc} = 5.0V ± 5% @ 0°C to + 70°C

AC ELECTRICAL CHARACTERISTICS

No	Symbol	Parameter	V_{CC} Note[4]	T_A = 0°C to 70°C 5 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	5.0V	200	250	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times	5.0V		25	ns	1
3	TwC	Input Clock Width	5.0V	37		ns	1
4	TwTinL	Timer Input Low Width	5.0V	70		ns	1
5	TwTinH	Timer Input High Width	5.0V	2.5TpC			1
6	TpTin	Timer Input Period	5.0V	4TpC			1
7	TrTin,	Timer Input Rise & Fall Timer	5.0V		100	ns	
8A	TwIL	Int. Request Low Time	5.0V	70		ns	1,2
8B	TwIL	Int. Request Low Time	5.0V	3TpC			1,3
9	TwIH	Int. Request Input High Time	5.0V	3TpC			1,2
10	Twsm	Stop Mode Recovery Width Spec	5.0V	5TpC		ns	
11	Tost	Oscillator Start-up Time	5.0V		5TpC		
12	Twdt	Watch-Dog Timer Delay Time	5.0V	53		ms	
13	T_{POR}	Power--On Reset	5.0V	106	130	ms	

Notes:

1. Timing Reference uses 0.7 V_{cc} for a logic 1 and 0.2 V_{cc} for a logic 0.
2. Interrupt request through Port 3 (P31-P33).
3. Interrupt request through Port 3 (P30).

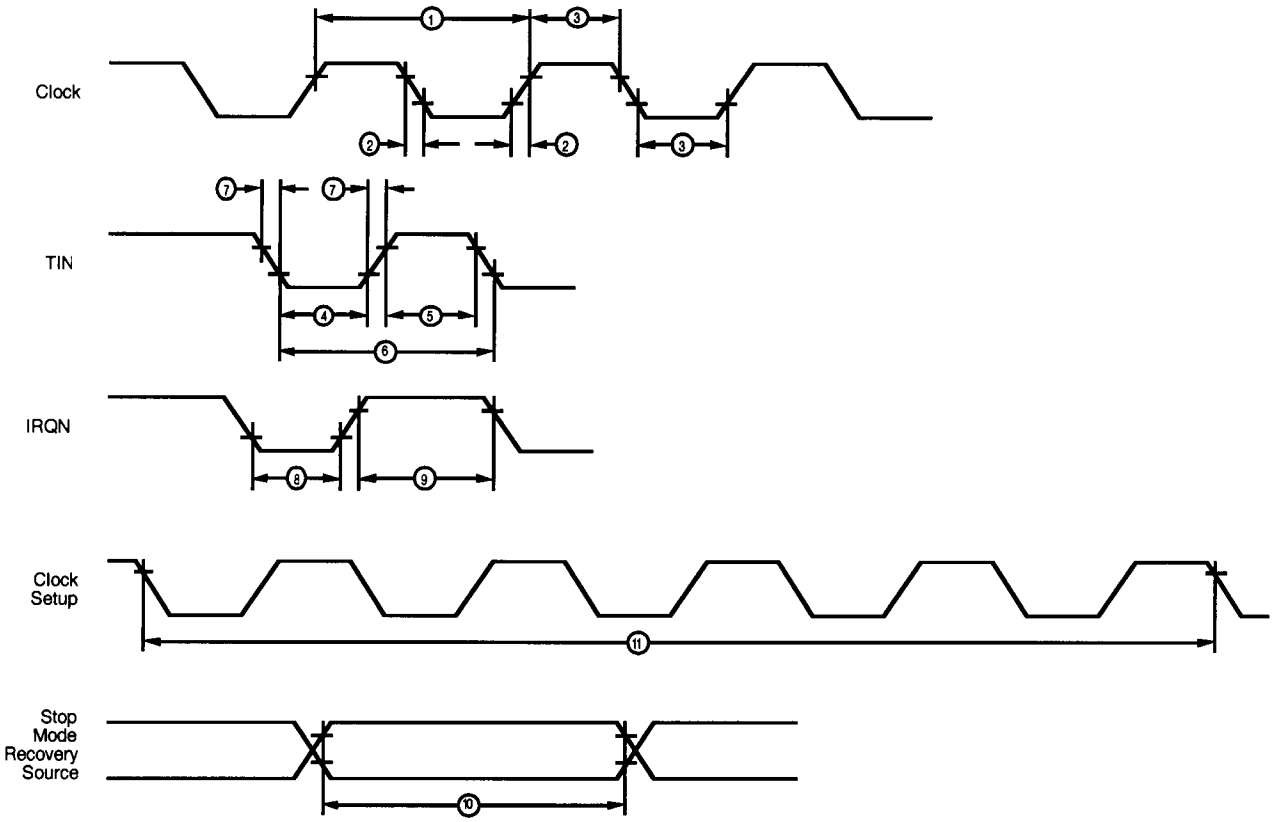


Figure 6. Additional Timing

PIN FUNCTIONS

RCIN. A precision resistor is connected between this pin and the power supply to form the precision RC oscillator.

CLKOUT. This pin is the system clock of the Z8® and runs at the frequency of the RC oscillator (Test only).

Port 0 (P07-P00). Port 0 is an 8-bit, CMOS-compatible open-drain output (Figure 7).

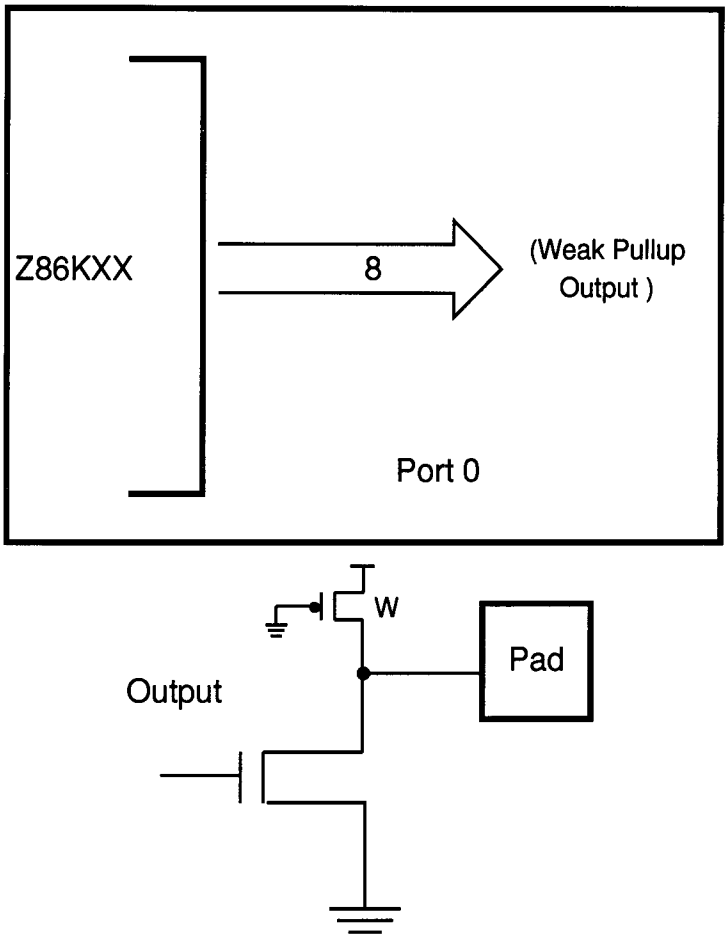


Figure 7. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, CMOS-compatible open-drain output port (Figure 8).

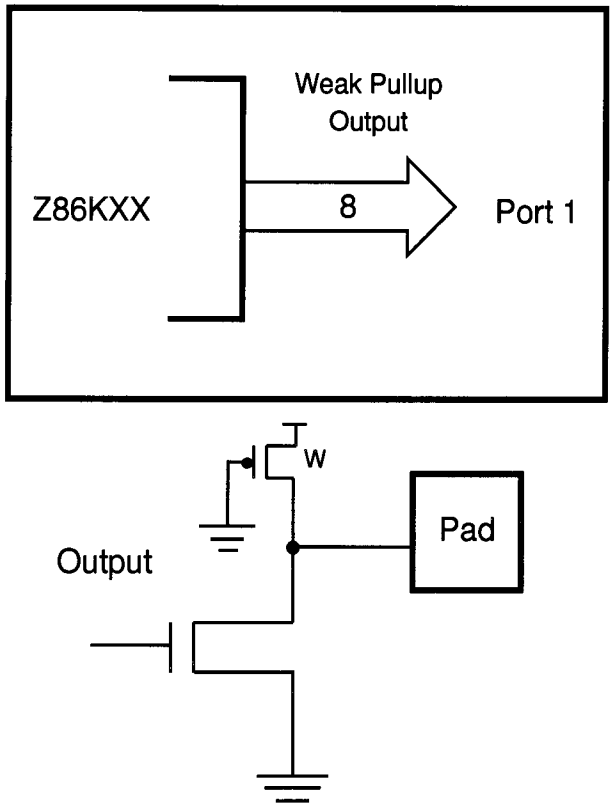


Figure 8. Port 1 Configuration

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit, CMOS-compatible Port with 4-bit input, 4-bit programmable I/O (Figure 9). P20-P25 have 10.4K (±35%) pull-up resistors. P26-P27 have 2.4K (±25%) pull-up resistors.

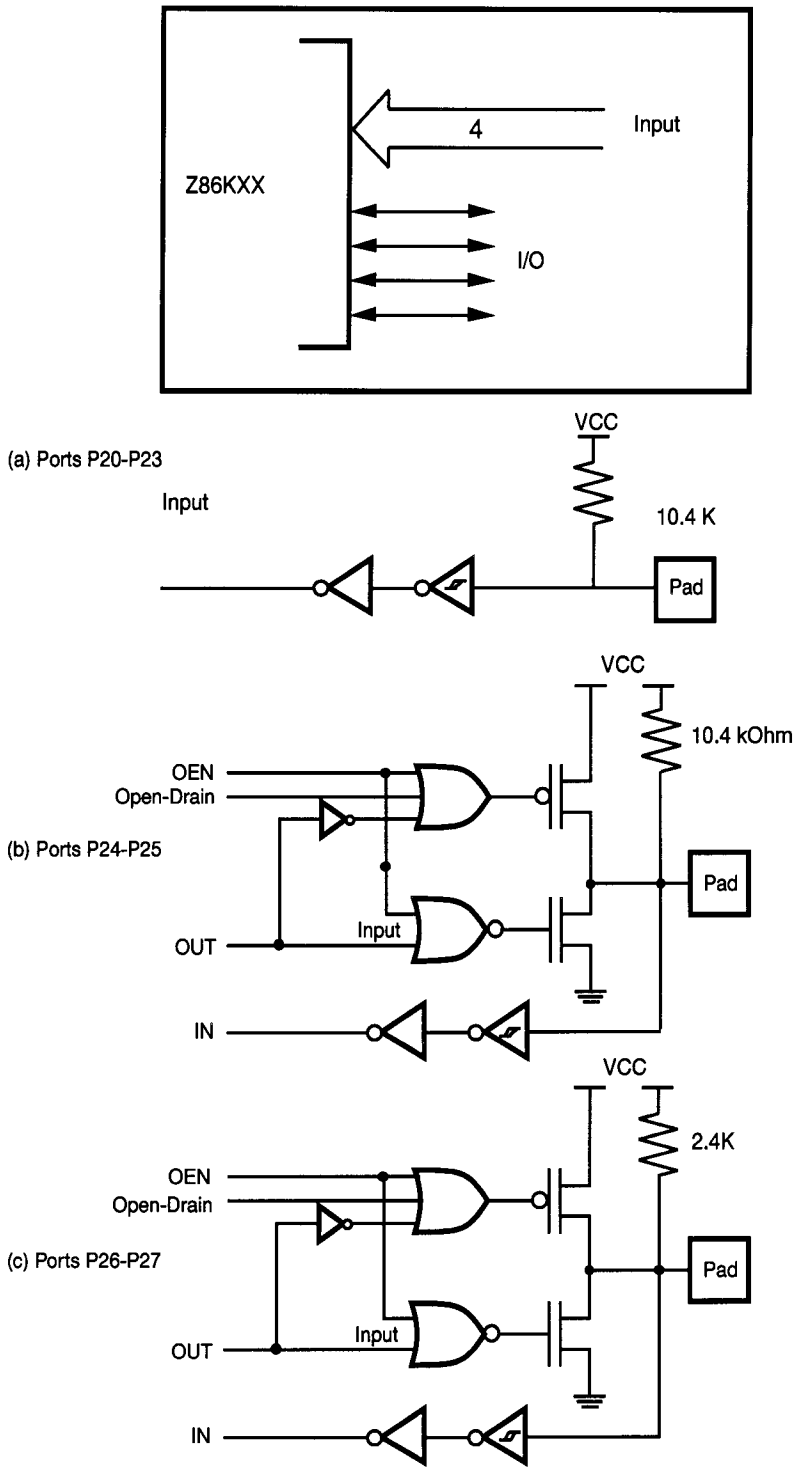


Figure 9. Port 2 Configuration

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS-compatible four-fixed input (P33-P30) and four-fixed output (P37-P34) I/O port. Port 3 inputs have 10.4 Kohm pull-up resistors. Outputs are capable of directly driving LED.

Port 3 is configured under software control to provide four external interrupt request signals (IRQ0-IRQ3).

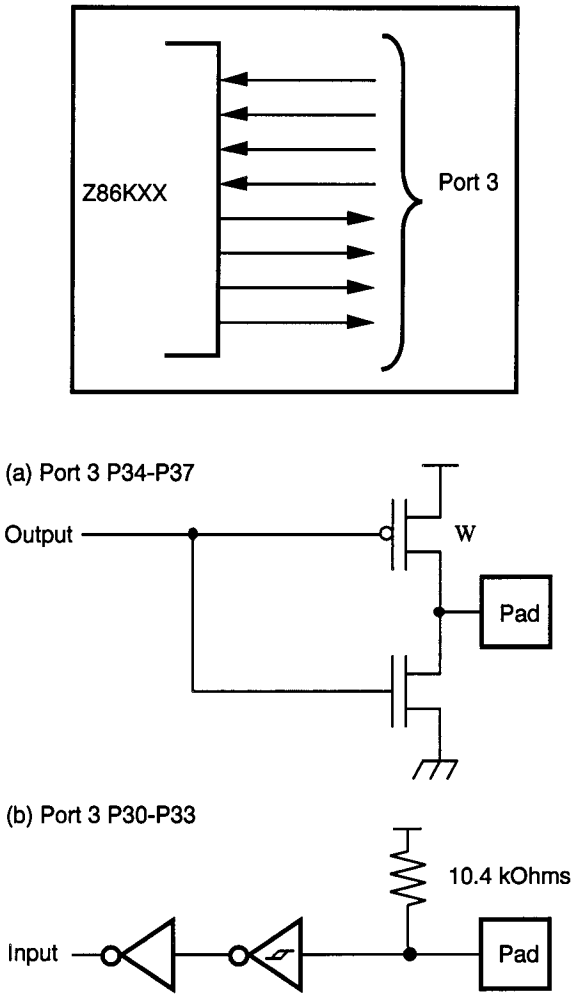


Figure 10. Port 3 Configuration

PIN FUNCTIONS (Continued)

Program Memory. The 16-bit program counter addresses 4 KB of program memory space at internal locations (Figure 11).

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations have six 16-bit vectors that correspond to the five available interrupts.

Byte 12 to byte 4095 consists of on-chip, mask programmed ROM. Addresses 4096 and greater are reserved.

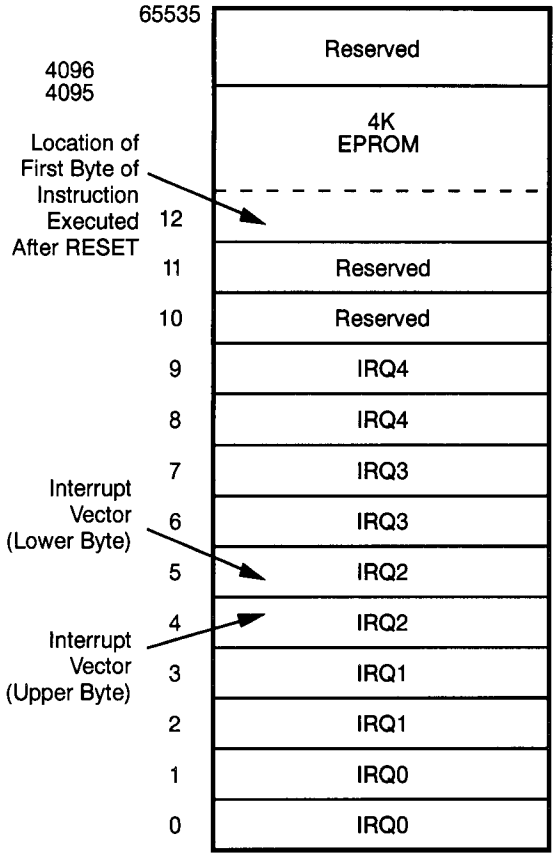


Figure 11. Program Memory Map

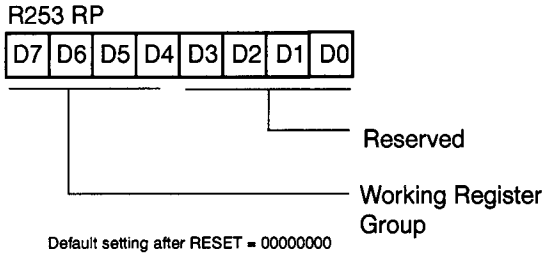
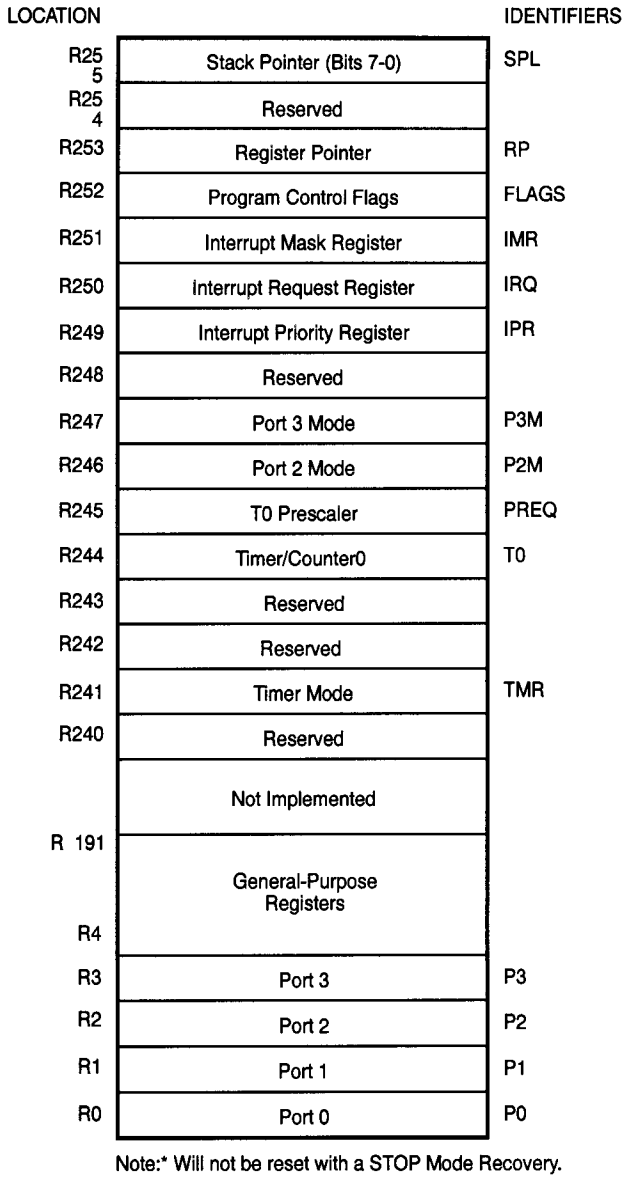


Figure 12. Register Pointer Register

Register File. The register file (Figure 13) consists of four I/O port registers, 188 general-purpose registers (excluding P00-P03), and 11 control and status registers (R3-R0, R191-R4, and R255-R240, respectively). The instructions can access registers directly or indirectly through an 8-bit address field. This allows short, 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into nine working-register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.



Note:* Will not be reset with a STOP Mode Recovery.

Figure 13. Register File Configuration

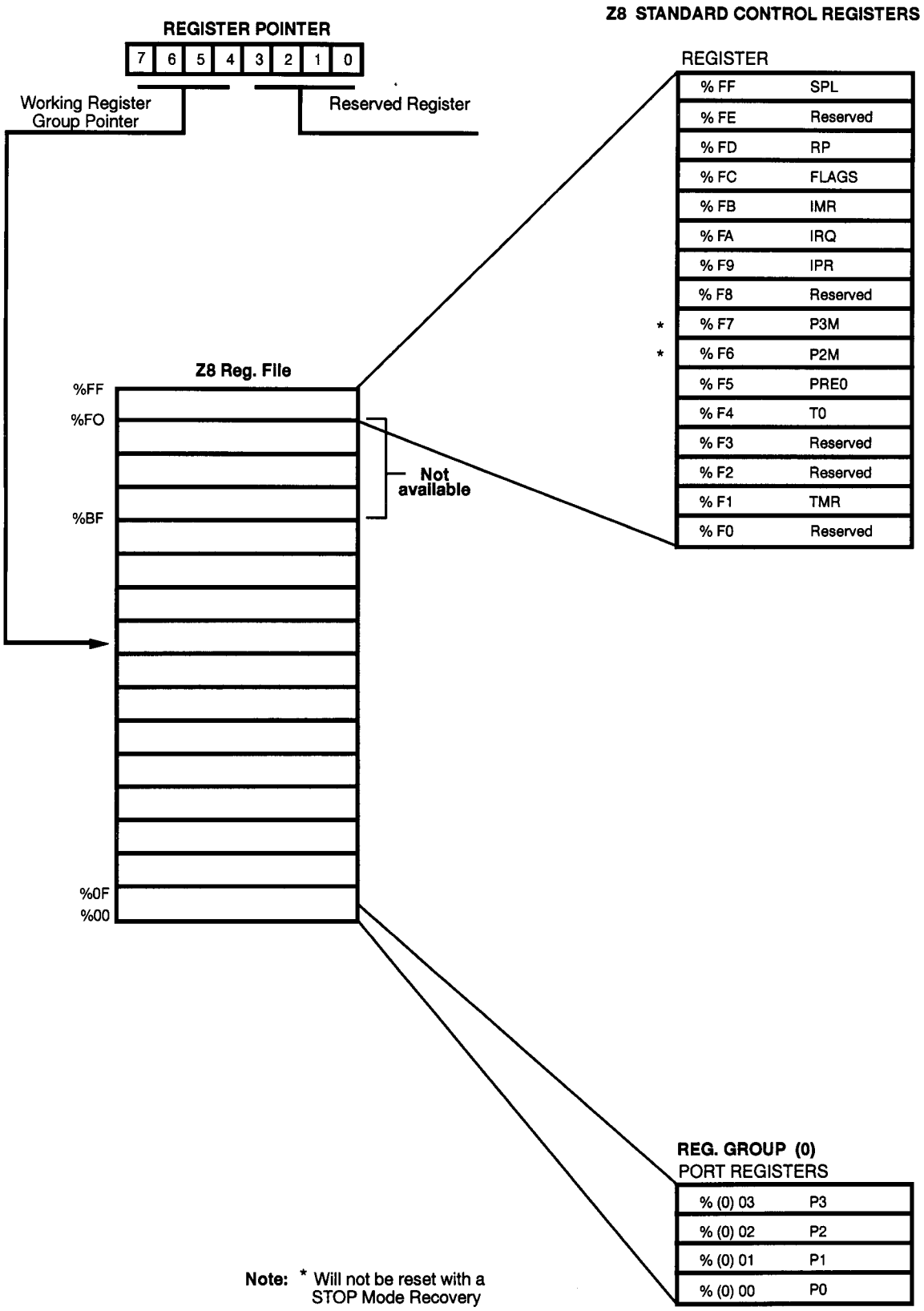


Figure 14. Register File Architecture

PIN FUNCTIONS (Continued)

Counter/Timers. There is an 8-bit programmable counter/timer (T0) driven by its own 6-bit programmable prescaler (Figure 15).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. The prescaler drives its counter, which decrements the value (1 to 256) on the prescaler overflow. When both the counter and prescaler reach the end of count, a timer interrupt request, IRQ4, is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counter can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode) The counter, but not the prescaler, is read at any time without disturbing its value or count mode.

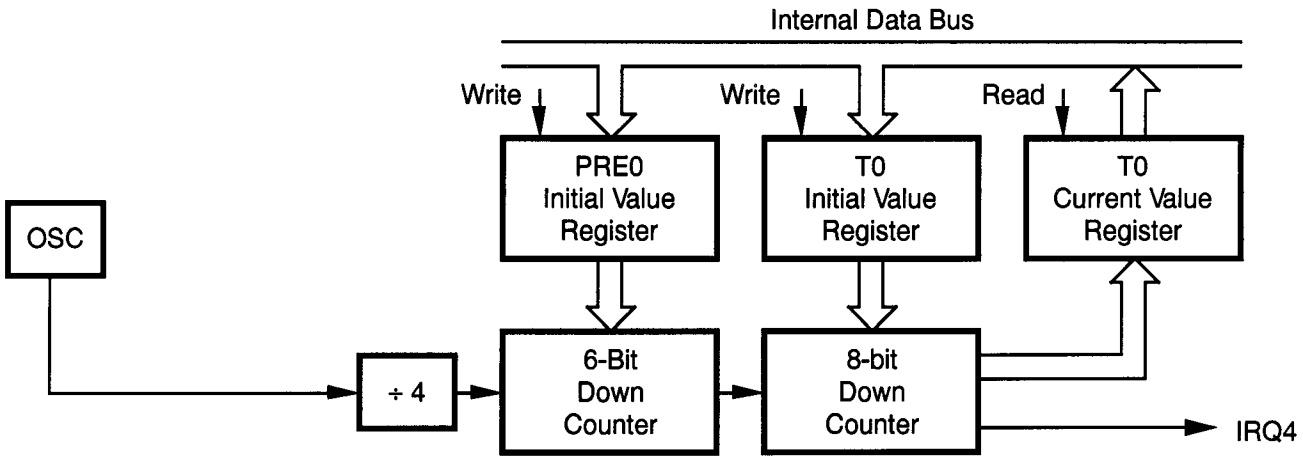


Figure 15. Counter/Timers Block Diagram

Interrupts. The Z86E15 has five different interrupts from five different sources. These interrupts are maskable and prioritized (Figure 16). The five sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and the other is claimed by the counter/timer. The Interrupt Masked Register globally or individually enables or disables the five interrupts requests.

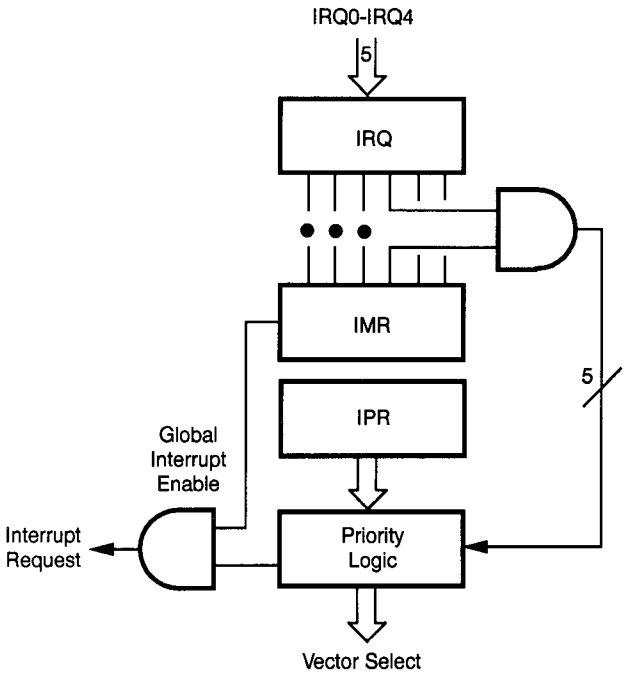


Figure 16. Interrupt Block Diagram

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and status flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt request needs service.

RC Oscillator. The Z86E15 provides an internal capacitor to accommodate an RC oscillator configuration. A 1% precision resistor is necessary to achieve ±10% accurate frequency oscillation.

The Z86E15 also accepts external clock from (RCIN) with (AGND) connected to V_{CC} (Figure 17).

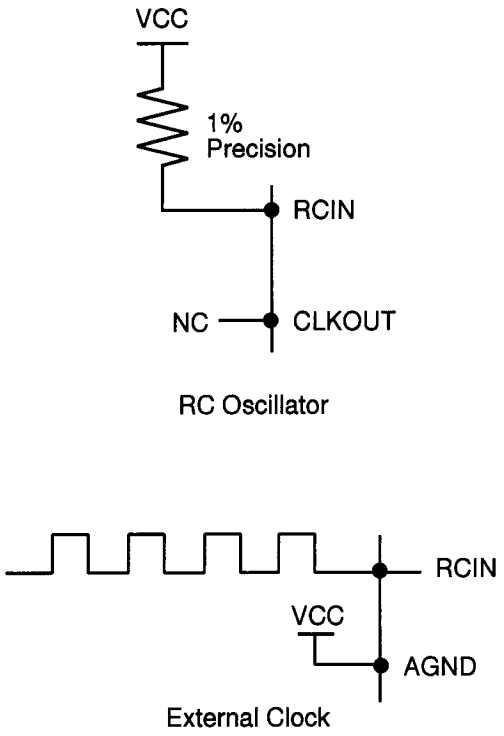


Figure 17. RC Oscillator Configuration

PIN FUNCTIONS (Continued)

Watch-Dog Timer. The Watch-Dog Timer (WDT) is activated automatically by power-on if it is enabled in the Mask Option. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is driven by the system clock. It must be refreshed at least once during each time cycle by executing the WDT instruction. WDT can be enabled by Mask Option. (Figure 18)

WDT Hot bit. Bit 7 of the Interrupt Request register (IRQ register FAH) determines whether a hot start or cold start occurred. A cold start is defined as reset occurring from power-up of the Z86E15 (the default upon power-up is 0). A hot start occurs when a WDT time-out has occurred (bit 7 is set to 1). Bit 7 of the IRQ register is read-only and is automatically reset to 0 when read.

Watch-Dog Timer . The WDT time-out is $\frac{294912 \text{ ms}}{f(\text{Hz})}$.

WDT During HALT (D5-R250). This bit determines whether or not the WDT is active during HALT Mode. The default is 1, and a 1 indicates active during HALT.

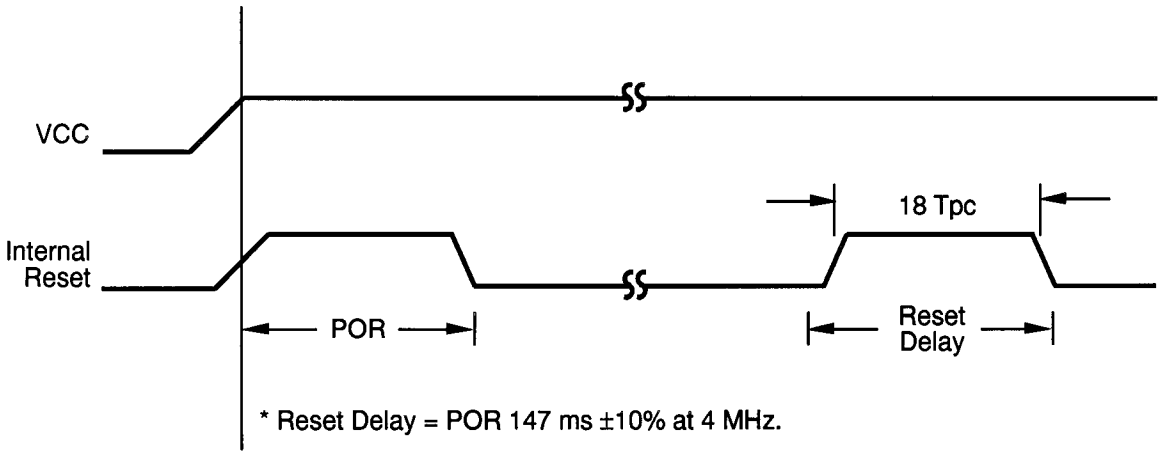


Figure 18. WDT Turn-On Timing After Reset

Power-On-Reset (POR). A timer circuit is triggered by the system oscillator and is used for the Power-On Reset (POR) timer function. The POR time allows V_{cc} and the oscillator circuit to stabilize before instruction execution begins. POR period is defined as:

$$\text{POR (ms)} = \frac{589824}{f_{(Hz)}}$$

The POR timer circuit is a one-shot timer triggered by one of two conditions:

1. Power fail to Power OK status
2. Stop-Mode Recovery

The POR time is a nominal 147 ms ±10%. At 4 MHz the POR timer is bypassed after Stop-Mode Recovery.

HALT. HALT turns off the internal CPU clock, but not the RC oscillator. The counter/timer and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The Z86E15 is recovered by interrupts, either externally or internally (Figure 19).

STOP. This instruction turns off the internal clock and oscillator. It reduces the standby current to less than 10 µA. The STOP Mode is terminated by a reset only or external reset. This causes the processor to restart the application program at address 000C (HEX) or the active external interrupt vector. In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (Opcode=FFH) immediately before the appropriate sleep instruction, such as:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
                or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

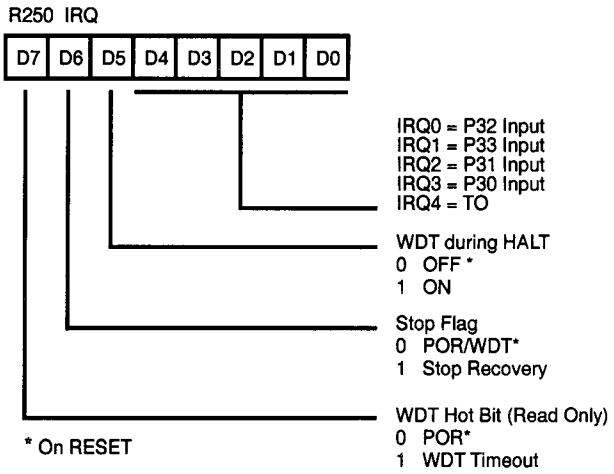


Figure 19. IRQ Register

The Bit 6 of IRQ Registers are flags for Stop Mode Recovery (Figure 20).

Cold or Warm Start (D6). This bit is set upon entering STOP Mode. A 0 (cold) indicates that the device is awakened by a POR/WDT RESET. A 1 (warm) indicates that the device is awakened by a SMR source. This bit is reset when read.

Negative transition on any of the designated row input pins or host data line will recover Z86E15 from STOP Mode.

Figure 20. Stop-Mode Recovery Source

Z8® CONTROL REGISTER DIAGRAMS

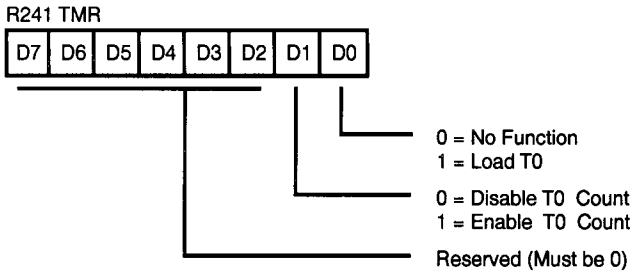
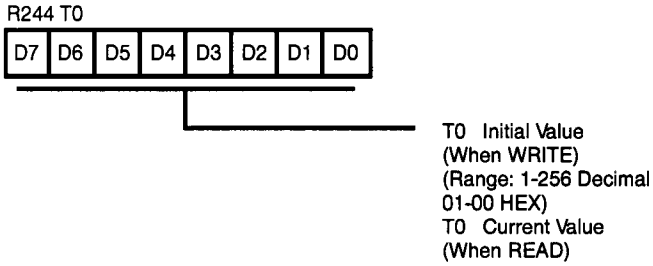
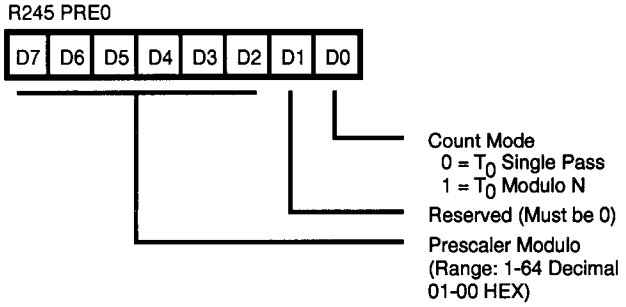


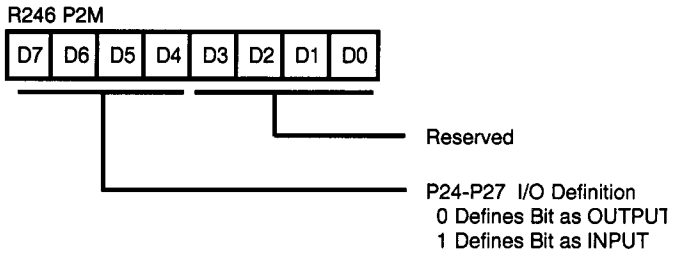
Figure 21. Timer Mode Register ($F1_H$: Read/Write)



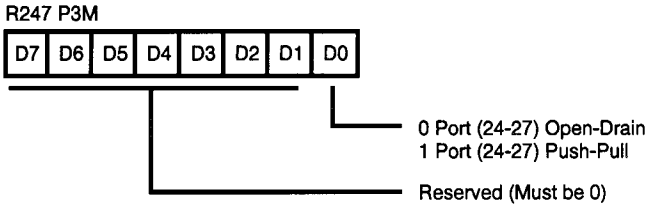
Counter/Timer 0 Register
Figure 22. ($F4_H$: Read/Write)



Prescaler 0 Register
Figure 23. ($F5_H$: Write Only)



Port 2 Mode Register
Figure 24. ($F6_H$: Write Only)



Port 2 Open Drain Mode Register
Figure 25. ($F7_H$: Write Only)

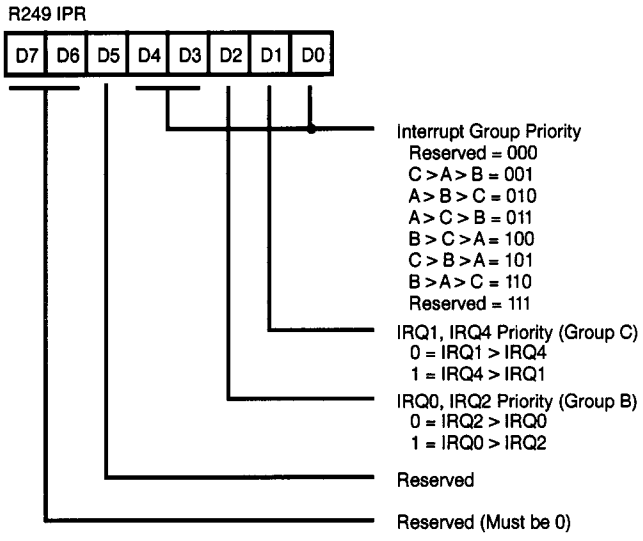


Figure 26. Interrupt Priority Register ($F9_H$: Write Only)

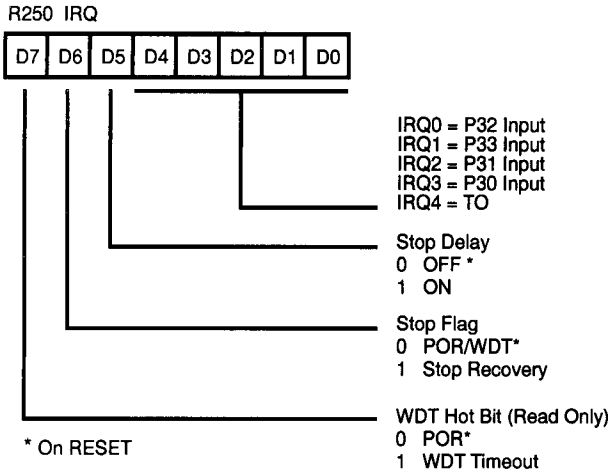


Figure 27. Interrupt Request Register (FA_H: Read/Write)

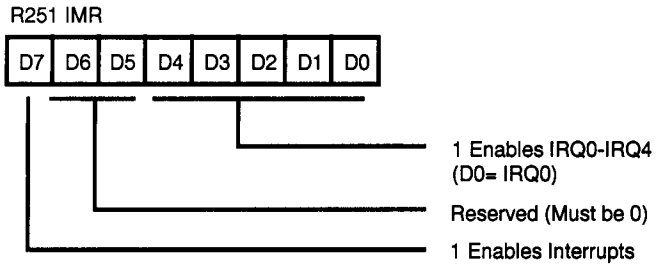


Figure 28. Interrupt Mask Register (FB_H: Read/Write)

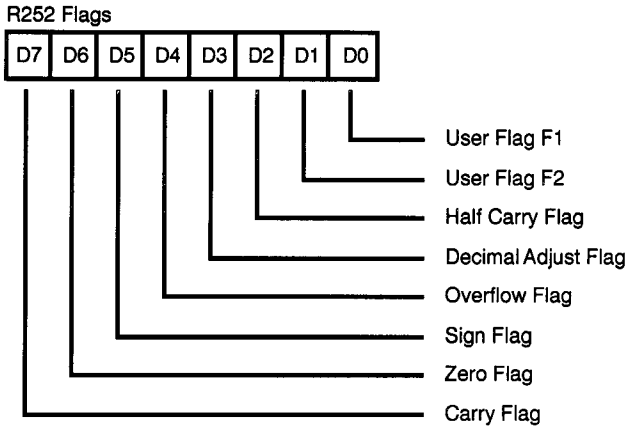
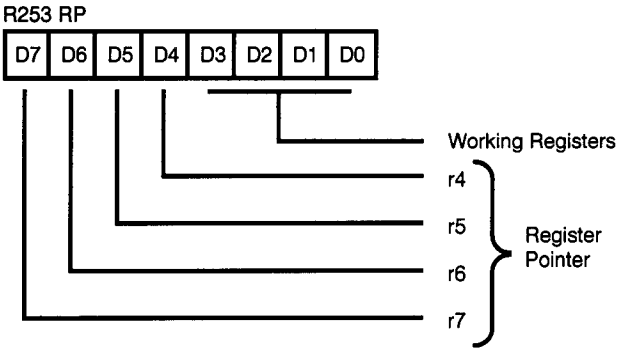
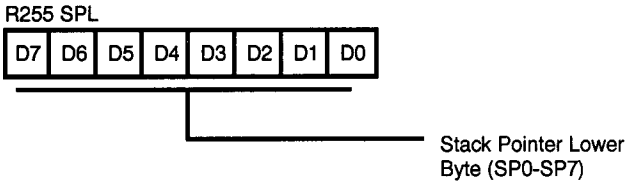


Figure 29. Flag Register (FC_H: Read/Write)



Register Pointer
Figure 30. (FD_H: Read/Write)



Stack Pointer
Figure 31. (FF_H: Read/Write)

PROGRAMMING

Signals Required for E15 EPROM

The TEST1 pin will be used as a high voltage pin. The high voltage from this pin will be used to program the EPROM. It will also need to be at high voltage in order for any EPROM operation to be done. When this pin is at high voltage, then an internal signal V_{pph} is generated from the high voltage detect circuitry and the signal being active will be used to multiplex the remaining pins that are required in all the EPROM operations.

TEST1 (Vpp)
This pin is designated a high voltage pin on the Z86E15. All EPROM operations will require a high voltage on this pin. The V_{pp} supplies the high voltage for the programming of the EPROM.

Note: The pins listed below are based on the condition that the V_{pp} is in high voltage.

P33 (Mode Latch)
The Z86E15 utilizes this pin when high will be used to latch the mode. This condition will only happen when the V_{pph} is active.

P32 (Oeb-Output Enable)
This regular pin controls the direction of the data bus. The signal generated goes into the EPROM as the precharge signal.

When this signal is low, the data is output from the EPROM. When the signal is high, data is input to the EPROM.

When the signal is high, the EPROM is precharged. When the signal is low, the EPROM is evaluated.

P31 (EPMH)
This regular pin is used to read the option bits when the EPROM is protected.

When the signal is high, during POR, the option bits can be read from the EPROM.

P30 (Volt_Clamp)
This regular pin used the signal to disable the voltage clamp circuit.

When the signal is low, the voltage clamp circuit is enabled. When the signal is high, the voltage clamp circuit is disabled and margin testing can be done.

P20 (CEb)
This regular pin on the Z86E15 is the chip enable signal for the EPROM. This signal will be input to the EPROM when Vpph is high. This is an active low signal.

P21 (PGMb-Program Mode)
This regular pin on the Z86E15 allows the EPROM to be programmed when the signal is logic low, and when the signal V_{pph} is high. The data on the databus will be programmed into the location that is addressed by the internal counter that generates the address for the EPROM.

P22 (epadr_clk) and P23 (epadr_rst)
The address is generated by an internal address counter which is clocked through the signal epadr_clk. Each clock increments the counter by one. The counter can be reset to zero by the epadr_rst signal. Both epadr_clk and epadr_rst are external signals.

The epadr_rst signal is an active high signal.

Data to the EPROM

The data to the EPROM are multiplexed with the pins as shown below in Figure 32: (Data <7.0>)

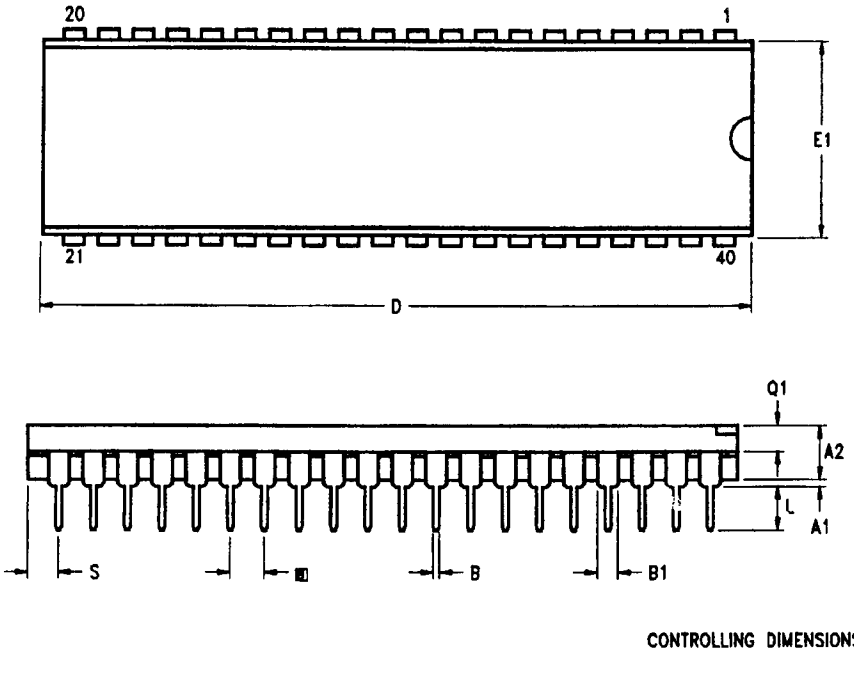
Data	Pin
D0	P34
D1	P35
D2	P36
D3	P37
D4	P27
D5	P26
D6	P25
D7	P24

Figure 32. Data Pin Assignments

Option Bit Programming
In order to program the option bits, the Mode 3 should be used. This can be done as follows:

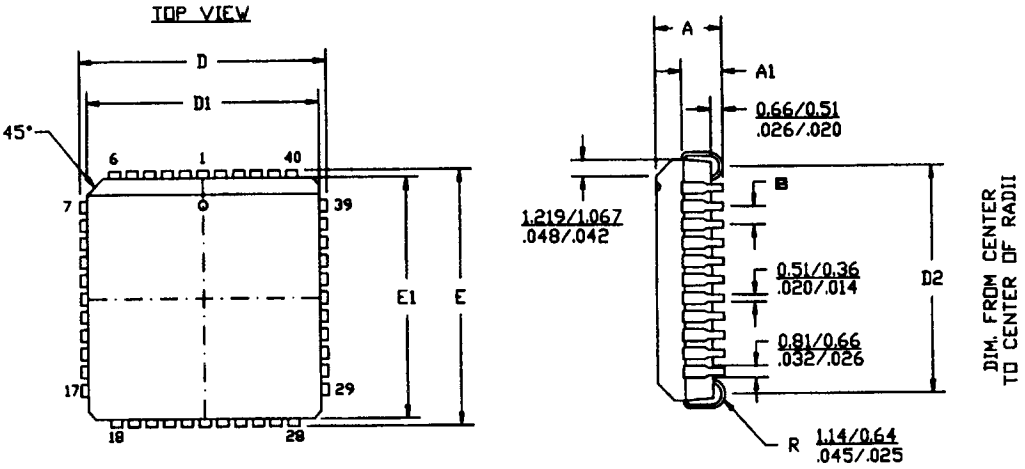
- The V_{pp} pin is set to high voltage (device pin TEST1 is driven to high voltage).
- The epadr_rst signal is driven high for one cycle to reset the address counter (device pin P23).
- Three clocks are given on the epadr_clk pin (P22), which will advance the counter to the count of 3.
- The Mode Latch signal (P33) is driven high for one cycle to latch in the data into the Mode Register.
- The address counter is again reset and the required data is programmed into location 0, which will program the 8 locations of the option bits. In the Z86E15, bits 0, 1 and 2 will be used as there are only 3 option bits for this device.

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

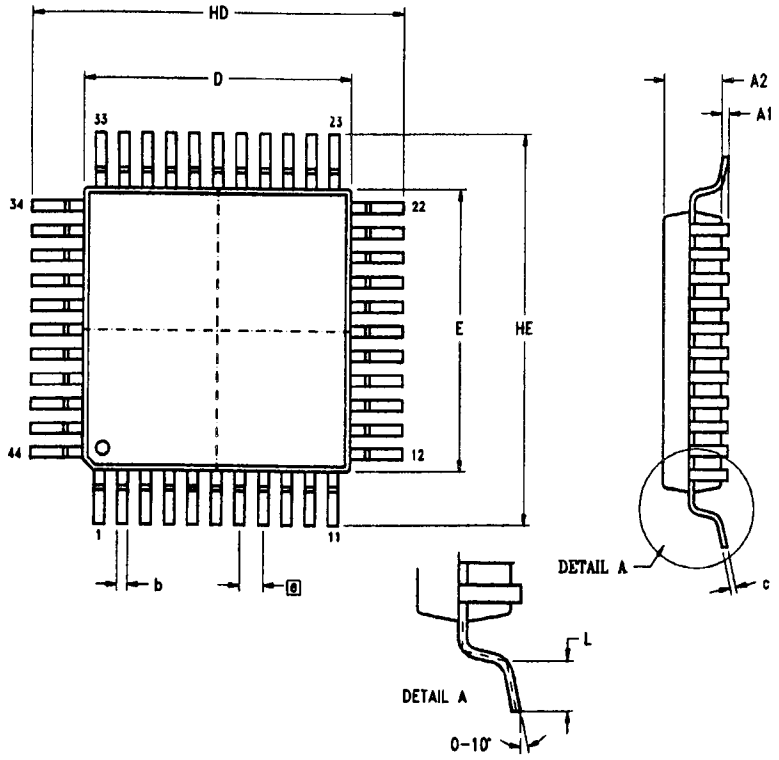
Figure 33. 40-Pin DIP Package Diagram



NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.41	2.92	.095	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

Figure 34. 44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 (.004")

Figure 35. 44-Pin QFP Package Diagram

ORDERING INFORMATION

5 MHz	5 MHz	5 MHz
40-Pin DIP	**44-Pin PLCC**	**44-Pin QFP**
Z86E1505PSC	Z86E1505VSC	Z86E1505FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Package

P = Plastic DIP
V = Plastic Leaded Chip Carrier
F = Quad Flat Pack

Speed

05 = 5 MHz

Environmental

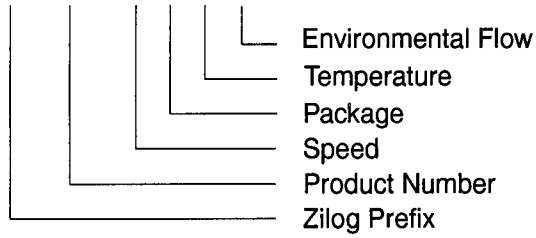
C = Plastic Standard

Temperature

S = 0°C to +70°C

Example:

Z 86E15 05 P S C is a Z86E15, 05 MHz, DIP, 0° to +70°C, Plastic Standard Flow



Development Projects:

Customer is cautioned that while reasonable efforts will be employed to meet performance objectives and milestone dates, development is subject to unanticipated problems and delays. No production release is authorized or committed until the Customer and Zilog have agreed upon a Customer Procurement Specification for this project.

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Low Margin:

Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

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