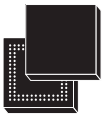
STA2416

Bluetooth® technology baseband transceiver with integrated Flash memory

Features

- Bluetooth® specification V1.1, V1.2 compliant
- Software compatible with STLC2416
- 2-layer class-4 PCB compatible
  - Point-to-point, point-to-multi-point (up to 7 slaves) and scatternet capability
- Asynchronous connection-less (ACL) logical transport link
- Synchronous connection oriented (SCO) links: 2 simultaneous SCO channels
- Supports pitch-period error concealment (PPEC)
  - Improves speech quality in the vicinity of interference
  - Improves coexistence with WLAN
  - Works at receiver, no Bluetooth implication
- Adaptive frequency hopping (AFH): hopping kernel, channel assessment as master and as slave
- Faster connection: interlaced scan for page and inquiry scan, first FHS without random backoff, RSSI used to limit range
- Extended SCO (eSCO) links
- Standard BlueRF bus interface
- QoS flush
- Clock support
  - System clock input: 13 MHz (±20 ppm if shared with Bluetooth® RF chipset
  - LPO clock input at 3.2 and 32 kHz or via the embedded 32 kHz crystal oscillator cell
- ARM7TDMI® 32-bit CPU
- Memory
  - Integrated 4-Mbit Flash

LFBGA120
(10x10x1.4 mm)



  - 64-KByte on-chip RAM
  - 4-KByte on-chip boot ROM
- Low power architecture with sleep mode
- Hardware support for packet types
  - ACL: DM1, 3, 5 and DH1, 3, 5
  - SCO: HV1, 3 and DV
  - eSCO: EV3, 5
- Communication interfaces
  - Synchronous serial interface, supporting up to 32-bit data
  - Two enhanced 16550 UARTs with 128-byte FIFO depth
  - 12 Mbit/s USB interface
  - Fast master I^2C bus interface
  - Multi slot PCM interface
  - 15 programmable GPIOs
  - 2 external interrupts and various interrupt possibilities through other interfaces
- 32 kHz clock out
- Efficient support for WLAN coexistence
- Ciphering support for up to 128-bit key
- Receiver signal strength indication (RSSI) support for power-controlled links
- Separate control for external power amplifier (PA) for class-1 power support
- Software support: low level (up to HCI) stack or embedded stack with profiles
  - Support of UART and USB HCI transport layers.

Table 1. Device summary

Order code	Package	Packaging
STA2416	LFBGA120 (10x10x1.4mm)	Tube

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1 Application features

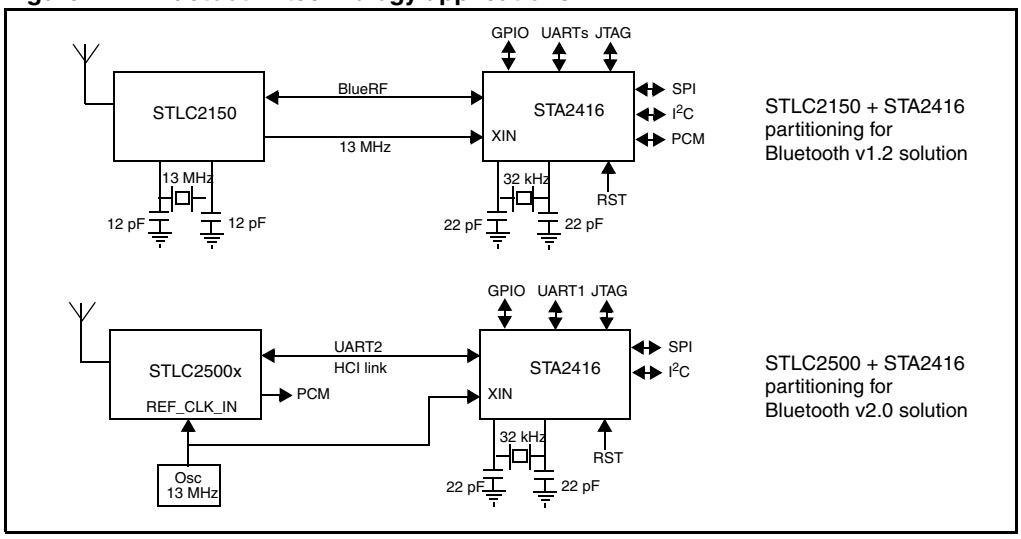
Typical applications in which the STA2416 can be used are:

- serial or audio cable replacement (SPP or A2DP profile)
- portable computers, PDA
- handheld data transfer devices
- computer peripherals
- other devices that require wireless communication using Bluetooth® technology
- software host for ST single chip STLC2500x
- audio applications include:
  - wireless audio
  - Bluetooth® extensions for cradles and home-audio systems
  - wireless speakers for, for example, TV, STB and LCDPDP displays
  - indoor multi-room audio diffusion with remote speaker sets
  - headsets and headphones
  - wireless transmitters.

When used in Bluetooth® applications the STA2416 can support two different partitionings.

- Bluetooth® v1.2 (basic rate): STLC2150 + STA2416. A dedicated customer framework SDK (CFW) can be provided by STM to customers needing to develop their own code.
- Bluetooth® v2.0 (enhanced data rate): STLC2500x + STA2416. In this case please refer to the CFWLite SDK.

Figure 1. Bluetooth® technology applications



Both CFW and CFWLite are provided by STM free of charge and include all the required software drivers to easily operate with the device I/O peripherals, a proprietary multi-tasking RTOS, all required Bluetooth® lower layers to communicate with the RF/HCI front-end and a complete offering of APIs to access and control device functions. STM provides support for full Bluetooth stack integration as well as complete and pre-configured solutions for both audio and SPP applications. Contact your STM representative for more information.

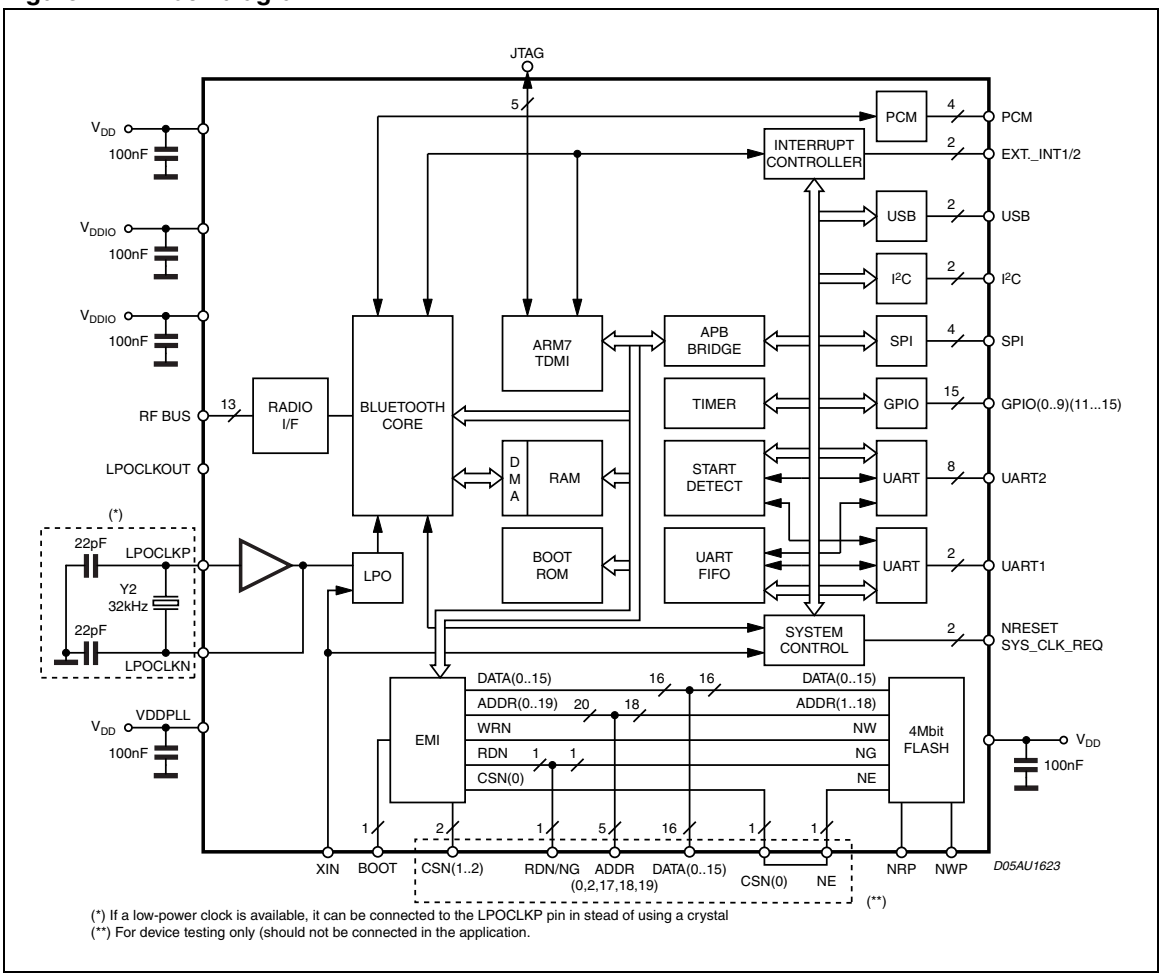
2 Description

The STA2416 from STMicroelectronics is a Bluetooth® technology baseband controller with integrated 4-Mbit Flash memory. Together with a Bluetooth radio this product offers a compact and complete solution for short-range wireless connectivity. It incorporates all the lower layer functions of the Bluetooth protocol.

The microcontroller allows the support of all data packets of Bluetooth® transmission in addition to voice. The embedded controller can be used to run the Bluetooth protocol and application layers if required. The software is located in the integrated Flash memory.

2.1 Block diagram

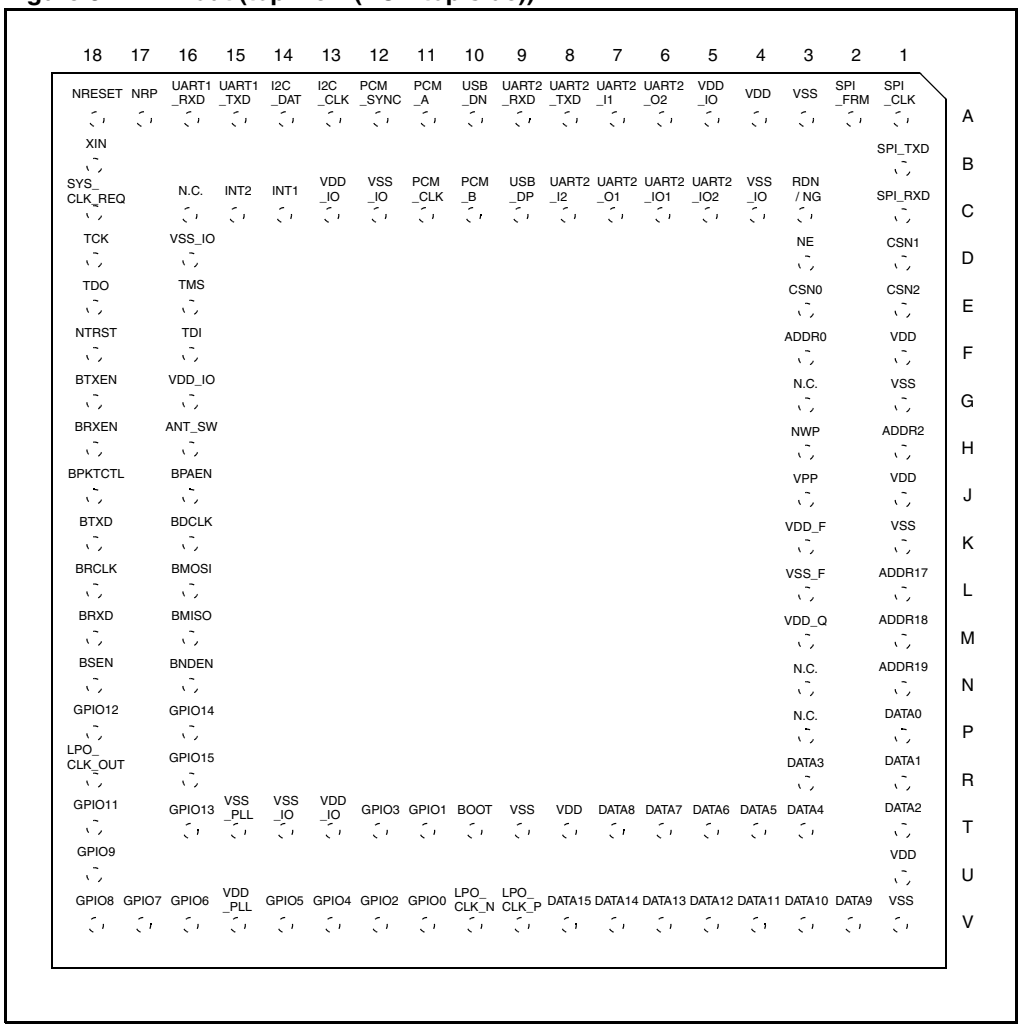
Figure 2. Block diagram



(*) If a low-power clock is available, it can be connected to the LPOCLKP pin in stead of using a crystal
(**) For device testing only (should not be connected in the application.

2.2 Pin description

Figure 3. Pin out (top view (PCB top side))



2.3 Pin description and assignment

Table 2 shows the pin list of the STA2416. There are 91 functional pins of which 25 are used for device testing only (should not be connected in the application) and 24 supply pins. The column headed PU/PD shows the pads which implement an optional internal weak pull-up or pull-down to set the logical level of the pin if left unconnected.

The pads are grouped according to two different power supply values, as shown in the column headed VDD:

- V1 for nominal 3.3 V (2.7 - 3.6 V range)
- V2 for nominal 1.8 V (1.55 - 1.95 V range)

Finally the column headed DIR describes the pin directions:

- I for inputs
- O for outputs
- I/O for input/outputs
- O/T for 3-state outputs

Table 2. Pin list

Name	Pin #	Description	DIR	PU/PD	VDD	PAD
Clock and test pins						
XIN	B18	System clock	I		V1	CMOS, 3.3V TTL compatible, schmitt trigger
NRESET	A18	Reset	I			
NRP	A17	Flash memory reset	I		V2	
NWP	H3	Flash memory write protect	I		V2	CMOS 1.8V
SYS_CLK_REQ	C18	System clock request	I/O		V1	CMOS, 3.3V TTL compatible, 2mA, 3-state, slew rate control
LPO_CLK_P	V9	Low-power mode oscillator + (slow clock input)	I		V2	
LPO_CLK_N	V10	Low-power mode oscillator -	O			
LPO_CLK_OUT	R18	32 MHz clock out	O		V1	
INT1	C14	External interrupt used also as external walk-up	I	(1)	V1	CMOS, 3.3V TTL compatible, schmitt trigger
INT2	C15	Second external interrupt	I	(1)		
BOOT	T10	Select external boot from EMI or internal from ROM	I	(1)	V2	CMOS 1.8V

Table 2. Pin list (continued)

Name	Pin #	Description	DIR	PU/ PD	VDD	PAD
SPI interface						
SPI_FRM	A2	Synchronous serial interface frame sync	I/O		V1	CMOS, 3.3V TTL compatible, 2mA, 3-state, slew rate control, schmitt trigger
SPI_CLK	A1	Synchronous serial interface clock	I/O			
SPI_TXD	B1	Synchronous serial interface transmit data	O/t		V1	CMOS, 3.3V TTL compatible, 2mA, slew rate control
SPI_RXD	C1	Synchronous serial interface receive data	I	(1)	V1	CMOS, 3.3V TTL compatible, schmitt trigger
UART interface						
UART1_TXD	A15	UART1 transmit data	O/t		V1	CMOS, 3.3V TTL compatible, 2mA, slew rate control
UART1_RXD	A16	UART1 receive data	I	(2)	V1	CMOS, 3.3V TTL compatible, schmitt trigger
UART2_O1	C7	UART2 modem output	O		V1	CMOS, 3.3V TTL compatible, 2mA, slew rate control
UART2_O2	A6	UART2 modem output	O/t		V1	CMOS, 3.3V TTL compatible, 2mA, slew rate control
UART2_I1	A7	UART2 modem input	I	(2)	V1	CMOS, 3.3V TTL compatible
UART2_I2	C8	UART2 modem input	I	(2)	V1	
UART2_IO1	C6	UART2 modem input/output	I/O	(2)	V1	CMOS, 3.3V TTL compatible, 2mA, 3-state, slew rate control
UART2_IO2	C5	UART2 modem input/output	I/O	(2)	V1	
UART2_TXD	A8	UART2 transmit data	O/t		V1	CMOS, 3.3V TTL compatible, 2mA, slew rate control
UART2_RXD	A9	UART2 receive data	I	(2)	V1	CMOS, 3.3V TTL compatible
I^2C interface						
I2C_DAT	A14	I^2C data pin	I/O	(3)	V1	CMOS, 3.3V TTL compatible, 2mA, 3-state, slew rate control
I2C_CLK	A13	I^2C clock pin	I/O	(3)	V1	
USB interface						
USB_DN	A10	USB - pin (Needs a series resistor of 27 Ω ±5%)	I/O	(1)	V1	
USB_DP	C9	USB + pin (Needs a series resistor of 27 Ω ±5%)	I/O	(1)	V1	

Table 2. Pin list (continued)

Name	Pin #	Description	DIR	PU/ PD	VDD	PAD
GPIO interface						
GPIO0	V11	GPIO port 0	I/O	PU	V1	CMOS, 3.3V TTL compatible, 4mA, 3-state, slew rate control
GPIO1	T11	GPIO port 1	I/O	PU		
GPIO2	V12	GPIO port 2	I/O	PU		
GPIO3	T12	GPIO port 3	I/O	PU	V1	CMOS, 3.3V TTL compatible, 4mA, 3-state, slew rate control, schmitt trigger
GPIO4	V13	GPO port 4	I/O	PU	V1	CMOS, 3.3V TTL compatible, 4mA, 3-state, slew rate control
GPIO5	V14	GPO port 5	I/O	PU		
GPIO6	V16	GPO port 6	I/O	PU		
GPIO7	V17	GPO port 7	I/O	PU		
GPIO8	V18	GPO port 8	I/O	PU	V1	CMOS, 3.3V TTL compatible, 2mA, 3-state, slew rate control
GPIO9	U18	GPO port 9	I/O	PU		
GPIO11	T18	GPO port 11	I/O	PU		
GPIO12	P18	GPO port 12	I/O	PU		
GPIO13	T16	GPO port 13	I/O	PU		
GPIO14	P16	GPO port 14	I/O	PU		
GPIO15	R16	GPO port 15	I/O	PU		
JTAG interface						
NTRST	F18	JTAG pin	I	PD	V1	CMOS, 3.3V TTL compatible
TCK	D18	JTAG pin	I	(1)	V1	CMOS, 3.3V TTL compatible, schmitt trigger
TMS	E16	JTAG pin	I	PU	V1	CMOS, 3.3V TTL compatible
TDI	F16	JTAG pin	I	PU		
TDO	E18	JTAG pin (should be left open)	O/T		V1	CMOS, 3.3V TTL compatible, 2mA, slew rate control
PCM interface						
PCM_A	A11	PCM data	I/O	PD	V1	CMOS, 3.3V TTL compatible, 2mA, 3-state, slew rate control
PCM_B	C10	PCM data	I/O	PD		
PCM_SYNC	A12	PCM 8 kHz sync	I/O	PD		
PCM_CLK	C11	PCM clock	I/O	PD	V1	CMOS, 3.3V TTL compatible, 2mA, 3-state, slew rate control, schmitt trigger

Table 2. Pin list (continued)

Name	Pin #	Description	DIR	PU/ PD	VDD	PAD
Radio interface						
BRCLK	L18	Transmit clock	I	(1)	V1	CMOS, 3.3V TTL compatible, schmitt trigger
BRXD	M18	Receive data	I			
BMISO	M16	RF serial interface input data	I	(1)	V1	CMOS, 3.3V TTL compatible
BNDEN	N16	RF serial interface control	O		V1	CMOS, 3.3V TTL compatible, 2mA, slew rate control
BMOSI	L16	RF serial interface output data	O			
BDCLK	K16	RF serial interface clock	O			
BTXD	K18	Transmit data	O			
BSEN	N18	Synthesizer on	O			
BPAEN	J16	Open PLL	O			
BRXEN	H18	Receive on	O			
BTXEN	G18	Transmit on	O			
BPKTCTL	J18	Packet on	O			
ANT_SW	H16	Antenna switch	O		V1	CMOS, 3.3V TTL compatible, 8mA, slew rate control
Power supply						
VSS_PLL	T15	PLL ground				
VDD_PLL	V15	1.8V supply for PLL				
VDD	A4	1.8V digital supply				
VDD	F1	1.8V digital supply				
VDD	J1	1.8V digital supply				
VDD	U1	1.8V digital supply				
VDD	T8	1.8V digital supply				
VDD_F	K3	1.8V digital supply for Flash memory				
VDD_Q	M3	1.8V I/O supply for Flash memory				
VPP	J3	12V fast program supply for Flash memory				
VDD_IO	C13	3.3V I/O supply				
VDD_IO	A5	3.3V I/O supply				
VDD_IO	T13	3.3V I/O supply				
VDD_IO	G16	3.3V I/O supply				

Table 2. Pin list (continued)

Name	Pin #	Description	DIR	PU/ PD	VDD	PAD
VSS	A3	Digital ground				
VSS	G1	Digital ground				
VSS	K1	Digital ground				
VSS	V1	Digital ground				
VSS	T9	Digital ground				
VSS_F	L3	Digital ground for Flash memory				
VSS_IO	C12	I/O ground				
VSS_IO	C4	I/O ground				
VSS_IO	T14	I/O ground				
VSS_IO	D16	I/O ground				
To be connected together on the PCB						
NE	D3	Flash memory enable	I			
CSN0	E3	External chip select bank 0	O			
Test interface only (do NOT connect)						
RDN / NG	C3	External read	O		V2	CMOS 1.8V, 4mA, slew rate control
CSN1	D1	External chip select bank 1	O			
CSN2	E1	External chip select bank 2	O			
ADDR0	F3	External address bit 0	O			
ADDR2	H1	External address bit 2	O			
ADDR17	L1	External address bit 17	O			
ADDR18	M1	External address bit 18	O			
ADDR19	N1	External address bit 19	O			
DATA0	P1	External data bit 0	I/O	PD		
DATA1	R1	External data bit 1	I/O	PD		
DATA2	T1	External data bit 2	I/O	PD		
DATA3	R3	External data bit 3	I/O	PD		
DATA4	T3	External data bit 4	I/O	PD		
DATA5	T4	External data bit 5	I/O	PD		
DATA6	T5	External data bit 6	I/O	PD		
DATA7	T6	External data bit 7	I/O	PD		
DATA8	T7	External data bit 8	I/O	PD		
DATA9	V2	External data bit 9	I/O	PD		
DATA10	V3	External data bit 10	I/O	PD		
DATA11	V4	External data bit 11	I/O	PD		

Table 2. Pin list (continued)

Name	Pin #	Description	DIR	PU/ PD	VDD	PAD
DATA12	V5	External data bit 12	I/O	PD	V2	CMOS 1.8V, 4mA, slew rate control
DATA13	V6	External data bit 13	I/O	PD		
DATA14	V7	External data bit 14	I/O	PD		
DATA15	V8	External data bit 15	I/O	PD		
Not connected						
N.C.	C16, G3, N3, P3	Not connected				

1. Must be strapped to VSS_IO if not used
2. Must be strapped to VDD_IO if not used
3. Must have a 10 kΩ pull-up

3 Quick reference data

3.1 Absolute maximum ratings

Operation of the device beyond these maximum ratings is not guaranteed.

Sustained exposure to these limits will adversely affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Conditions	Min	Max	Unit
V_{DD}	Supply voltage baseband core	V_{SS} - 0.5	2.5	V
V_{DDF}	Supply voltage Flash	V_{SS} - 0.5	2.5	V
V_{PP}	Fast Program Voltage	V_{SS} - 0.5	13	V
V_{DDIO}	Supply voltage baseband I/O		4	V
V_{DDQ}	Supply voltage Flash I/O	V_{SS} - 0.5	2.5	V
V_{IN}	Input voltage on any digital pin (excluding Flash input pins)	V_{SS} - 0.5	V_{DDIO} + 0.3	V
T_{stg}	Storage temperature	-55	+150	°C
T_{lead}	Lead temperature < 10s		+240	°C

3.2 Operating ranges

Operating ranges define the limits for functional operation and parametric characteristics of the device. Operation outside these limits is not implied.

Table 4. Operating ranges

Symbol	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage baseband core and EMI pads	1.55	1.8	1.95	V
V_{DDF}	Supply voltage for Flash memory	1.55	1.8	1.95	V
V_{DDIO}	Supply voltage for digital I/O	2.7	3.3	3.6	V
V_{DDQ}	Supply voltage for Flash memory I/Os ($V_{DDQ} \leq V_{DDF}$)	1.55	1.8	1.95	V
T_{amb}	Operating ambient temperature	-40		+85	°C

3.3 I/O specifications

The I/O voltage depends on the interface. The voltage is typically 1.8 V for the interface to the Flash memory and typically 3.3 V for all the other interfaces. These I/Os comply with the EIA/JEDEC standard JESD8-B.

3.3.1 Specifications for 3.3-V I/Os

Table 5. LVTTL DC input specification ($3V < V_{DDIO} < 3.6V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{il}	Low level input voltage				0.8	V
V_{ih}	High level input voltage		2			V
V_{hyst}	Schmitt trigger hysteresis		0.4			V

Table 6. LVTTL DC output specification ($3V < V_{DDIO} < 3.6V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ol}	Low level output voltage	I_{ol} = X mA (1)			0.15	V
V_{oh}	High level output voltage	I_{oh} =-X mA (1)	V_{DDIO} - 0.15			V

1. X is the source/sink current under worst-case conditions according to the drive capability, see *Table 2 on page 10* for the value of X.

3.3.2 Specifications for 1.8-V I/Os

Table 7. DC input specification ($1.55V < V_{DD} < 1.95V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{il}	Low level input voltage				0.35 * V_{DD}	V
V_{ih}	High level input voltage		0.65 * V_{DD}			V
V_{hyst}	Schmitt trigger hysteresis		0.2	0.3	0.5	V

Table 8. DC output specification ($1.55V < V_{DD} < 1.95V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ol}	Low level output voltage	I_{ol} = X mA (1)			0.15	V
V_{oh}	High level output voltage	I_{oh} =-X mA (1)	V_{DD} - 0.15			V

1. X is the source/sink current under worst-case conditions according to the drive capability, see *Table 2 on page 10* for the value of X.

3.4 Current consumption

Table 9. Typical power consumption (V_{DD} = V_{DDF} = V_{DDPLL} = 1.8V, V_{DDIO} = 3.3V)

STA2416 state	Core		IO	Unit
	Slave	Master		
Standby (no low-power mode)	5.10	5.10	0.13	mA
Standby (low-power mode enabled)	0.94	0.94	0.13	mA
ACL connection (no transmission)	7.60	6.99	0.13	mA
ACL connection (data transmission)	7.90	7.20	0.13	mA
SCO connection (no codec connected)	8.70	7.90	0.14	mA
Inquiry and Page scan (low-power mode enabled)	127	n.a.	5	µA
Low-power mode (32 kHz crystal)	20	20	0	µA

4 Functional description

4.1 Baseband

- WLAN coexistence. See also *Section 5.12: Bluetooth®, WLAN coexisting in collocated scenario*.

4.1.1 Baseband 1.1 features

The baseband is based on Ericsson® Technology Licensing Baseband Core (EBC) and it is compliant with the Bluetooth® wireless technology specification 1.1:

- point-to-multipoint (up to 7 slaves).
- asynchronous connection-less (ACL) link support giving data rates up to 721 kbit/s.
- synchronous connection oriented (SCO) link with support for 2 voice channels over the air interface.
- flexible voice format to host and over the air (CVSD, PCM 13/16 bits, A-law, µ-law).
- hardware support for packet types: DM1, 3, 5; DH1, 3, 5; HV1, 3; DV.
- Scatternet capabilities (master in one piconet and slave in the other one; slave in two piconets). All Scatternet v.1.1 errata supported.
- ciphering support up to 128 bits key.
- paging modes R0, R1, R2.
- channel quality driven data rate.
- full Bluetooth® software stack available.
- low-level link controller.

4.1.2 Baseband 1.2 features

The baseband part is also compliant with the Bluetooth® specification 1.2:

- extended SCO (eSCO) links: supports EV3 and EV5 packets. See also *Section 5.6: V1.2 detailed functions - extended SCO on page 23*.
- adaptive frequency hopping (AFH): hopping kernel, channel assessment as Master and as Slave. See also *Section 5.7: V1.2 detailed functions - adaptive frequency hopping on page 24*.
- faster connection: interlaced scan for page and inquiry scan, answer FHS at first reception, RSSI used to limit range. See also *Section 5.8: V1.2 detailed functions - faster connection on page 24*.
- QoS flush. See also *Section 5.9: V1.2 detailed functions - quality of service on page 25*.
- synchronization: the local and the master BT clock are available via HCI commands for synchronization of parallel applications on different slaves.
- L2CAP flow and error control.
- LMP improvements.
- LMP SCO handling.
- parameter ranges update.

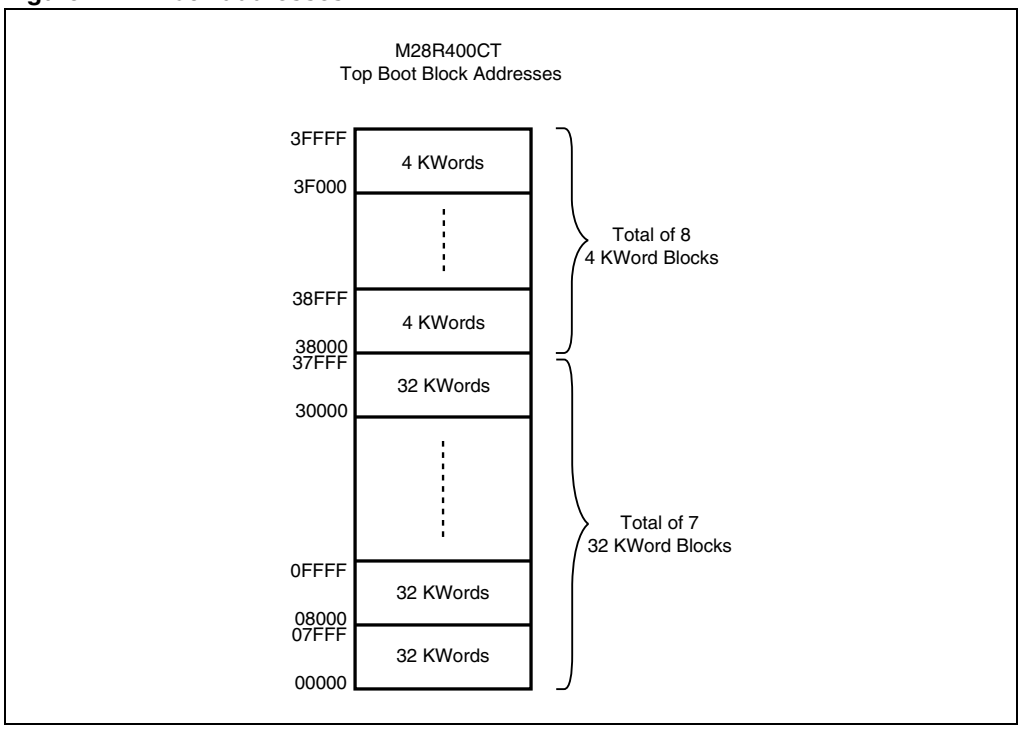
4.2 Integrated Flash memory

Features:

- 4-Mbit size
- eight parameter blocks of 4 Kword (top configuration)
- seven main blocks of 32 Kword
- 120 ns access time.

See the datasheet for the standalone product M28R400CT for detailed information.

Figure 4. Block addresses



4.2.1 Flash signals description

Write protect (NWP)

Write protect is an input that gives an additional hardware protection for each block. When pin NWP is ≤ 0.4 V the lock-down is enabled and the protection status of the Flash blocks cannot be changed. When NWP is ≥ (V_{DDQ} - 0.4 V), the lock-down is disabled and the Flash memory blocks can be locked or unlocked.

Reset (NRP)

The reset input provides a hardware reset of the memory. When NRP is ≤ 0.4 V, the memory is in reset mode where the outputs are high impedance and the current consumption is minimized. After a reset all blocks are in the locked state. When NRP is ≥ (V_{DDQ} - 0.4 V), the device is in normal operation. On exiting the reset mode the device enters the read array mode, but a negative transition of chip enable (CSN0, NE) or a change of the address is required to ensure valid data outputs.

VDD_F supply voltage (V_{DDF})

VDD_F provides the power supply to the internal core of the Flash memory device. It is the main power supply for all operations (read, program and erase)

VDD_Q supply voltage (V_{DDQ})

Pin VDD_Q provides the power supply to the I/O pins and enables all outputs to be powered independently from VDD_F. Pin VDD_Q can be tied to VDD_F or can use separate supply.

VPP program supply voltage (V_{PP})

VPP is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin. The supply voltage V_{DDF} and the program supply voltage V_{PP} can be applied in any order.

If pin VPP is kept within a low voltage range (0 V to 3.6 V) then pin VPP is seen as a control input. In this case a voltage lower than 1 V gives protection against program or block erase, while 1.65 V < V_{pp} < 3.6 V enables these functions. Pin VPP is sampled only at the beginning of a program or block erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PP} is in the range 11.4 V to 12.6 V, then pin VPP acts as a power supply pin. In this condition V_{PP} must be stable until the program/erase algorithm has terminated.

VSS_F Flash memory ground (V_{SSF})

V_{SSF}, the voltage on pin VSS_F, is the reference for all voltage measurements.

Address inputs, data I/Os, control signals

The address inputs (ADDR0-ADDR17), data I/Os (DATA0-DATA15), chip enable (CSN0), output enable (RDN / NG) and write enable (NWP) are internally connected to and controlled by the Bluetooth® technology baseband controller.

5 General specification

5.1 System clock

The STA2416 works with a single 13 MHz clock provided on pin XIN. For proper Bluetooth® wireless operation this clock must have a tolerance of ±20 ppm or better.

5.1.1 Slow clock

The slow clock is used by the baseband as reference clock during the low-power modes. The slow clock requires an accuracy of ±250 ppm (overall).

Several options are foreseen in order to adjust the STA2416 behavior according to the features of the radio used.

- If the system clock is not provided at all times (power consumption saving) and no slow clock is provided by the system, a 32 kHz crystal must be used by the STA2416 (default mode).
- If the system clock is not provided at all times (power consumption saving) and the system provides a slow clock at 32 kHz or 3.2 kHz, this signal is simply connected to the STA2416 (LPO_CLK_P).
- If the system clock is provided at all times, the STA2416 generates from the reference clock an internal 32 kHz clock. This mode is not an optimized mode for power consumption.

5.2 Boot procedure

The boot code instructions are the first that ARM7TDMI® executes after a hardware reset. All the internal device registers are set to their default value.

There are two types of boot:

- Flash memory boot

  When boot pin is set to ‘1’ (connected to VDD), the STA2416 boots on its Flash.
- UART download boot from ROM

  When boot pin is set to ‘0’ (connected to GND), the STA2416 boots on its internal ROM (needed to download the new firmware in the Flash memory). When booting on the internal ROM, the STA2416 will monitor the UART interface for approximately 1.4 second. If there is no request for code downloading during this period, the ROM jumps to Flash.

In order to reliably download code the STA2416 must run with a system clock of 13 MHz. At other frequencies the download may fail.

5.3 Clock detection

The STA2416 has an automatic slow-clock frequency detection (32kHz, 3.2kHz or none).

5.4 Master reset

When the device reset is held active (NRESET is low) then UART1_TXD and UART2_TXD are set to input state. When the NRESET returns high, the device starts to boot.

Note: The device should be held in active reset for minimum 20 ms in order to guarantee a complete reset of the device.

5.5 Interrupts/wake-up

All GPIOs can be used both as external interrupt source and as wake-up source. In addition the chip can be woken-up by USB, UART1_RXD, UART2_RXD, INT1, INT2.

5.6 V1.2 detailed functions - extended SCO

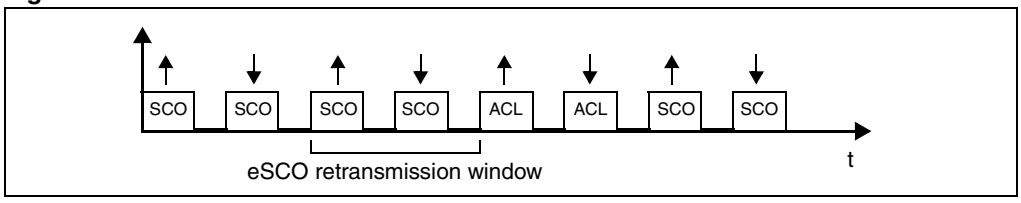
User perspective - extended SCO

This function gives improved voice quality since it enables the possibility to retransmit lost or corrupted voice packets in both directions.

Technical perspective - extended SCO

eSCO incorporates CRC, negotiable data rate, negotiable retransmission window and multi-slot packets. Retransmission of lost or corrupted packets during the retransmission window guarantees on-time delivery.

Figure 5. eSCO



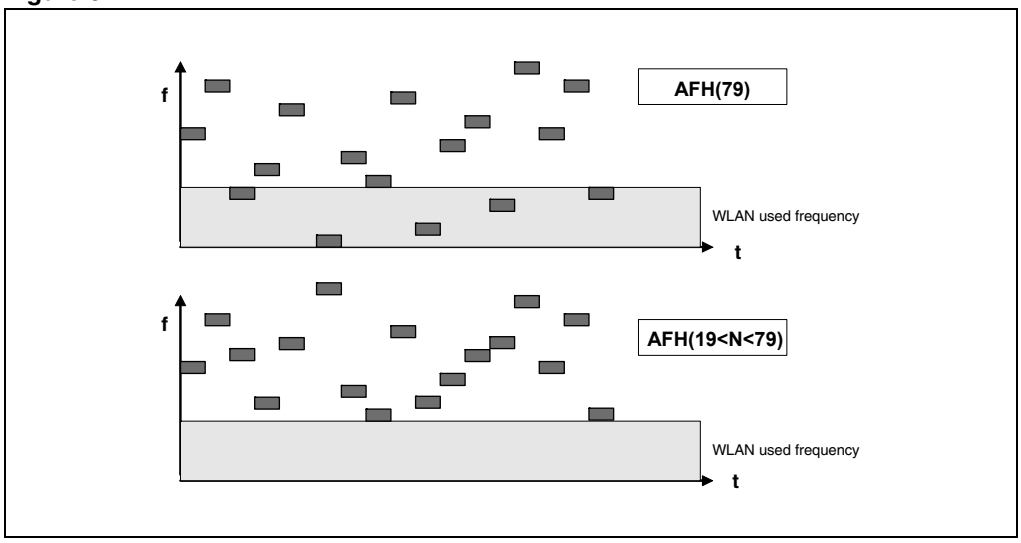
5.7 V1.2 detailed functions - adaptive frequency hopping

User perspective - adaptive frequency hopping

In the Bluetooth® specification 1.1 the Bluetooth wireless devices hop in the 2.4 GHz band over 79 channels. Since WLAN 802.11 has become popular, there are specification improvements in the 1.2-SIG spec for Bluetooth technology where the Bluetooth units can avoid the jammed bands and thereby provide an improved co-existence with WLAN.

Technical perspective - adaptive frequency hopping

Figure 6. AFH



First the master and/or the slaves identify the jammed channels. The master decides on the channel distribution and informs the involved slaves. The master and the slaves, at a predefined instant, switch to the new channel distribution scheme.

No longer are jammed channels re-inserted into the channel distribution scheme. AFH uses the same hop frequency for transmission as for reception

5.8 V1.2 detailed functions - faster connection

User perspective - faster connection

This feature gives the user about 65% faster connection on average when enabled compared to Bluetooth® specification 1.1 connection procedure.

Technical perspective - faster connection

The faster Inquiry function is based on a removed/shortened random back off and also a new interlaced inquiry scan scheme.

The faster page function is based on interlaced page scan.

5.9 V1.2 detailed functions - quality of service

User perspective - quality of service

Small changes to the BT1.1 spec regarding quality of service (QoS) makes a large difference by allowing all QoS parameters to be communicated over HCI to the link manager that enables efficient bandwidth management. Below is a short list of user perspectives.

- **Flush time-out:** enables time-bounded traffic such as video streaming to become more robust when the channel degrades. It sets the maximum delay of an L2CAP frame. It does not enable multiple streams in one piconet, or heavy data transfer at the same time.
- **Simple latency control:** allows the host to set the poll interval. It provides enough support for HID devices mixed with other traffic in the piconet.

5.10 Low-power modes

To save power, two low-power modes are supported. Depending on the Bluetooth® and the host activity, the STA2416 autonomously decides to use Sleep mode or Deep Sleep mode.

Table 10. Low-power modes

Low power mode	Description
Sleep mode	The STA2416: – accepts HCI commands from the host – supports page- and inquiry scans – supports Bluetooth® links that are in Sniff, Hold or Park – can transfer data over Bluetooth links – the system clock is still active in part of the design
Deep sleep mode(1)	The STA2416: – does not accept HCI commands from the host – keeps track of page- and inquiry scan activities – switches between sleep and active mode when it is time to scan – supports Bluetooth® links that are in Sniff, Hold or Park – does not transfer data over Bluetooth links – the system clock is not active in any part of the design

1. Deep Sleep mode is not compatible with a USB transport layer

5.10.1 Sniff or park

The STA2416 is in active mode with a Bluetooth® connection, once the connection is concluded the SNIFF or the PARK is programmed. Once one of these two states is entered the STA2416 goes in Sleep mode. After that, the host may decide to place the STA2416 in Deep Sleep mode by putting the UART link in low-power mode. The Deep Sleep mode allows smaller power consumption. When the STA2416 needs to send or receive a packet (for example, at T_{SNIFF} or at the beacon instant) it will require the clock and it will go in active mode for the needed transmission/reception. Immediately afterwards it will go back to the Deep Sleep mode. If some HCI transmission is needed, the UART link will be reactivated, using one of the two ways explained in 7.5, and the STA2416 will move from the Deep Sleep mode to the Sleep mode.

5.10.2 Inquiry/page scan

When only inquiry scan or page scan is enabled, the STA2416 will go in Sleep mode or Deep Sleep mode outside the receiver activity. The selection between Sleep mode and Deep Sleep mode depend on the UART activity like in SNIFF or PARK.

5.10.3 No connection

If the host places the UART in low power and there is no activity, then the STA2416 can be placed in Deep Sleep mode.

5.10.4 Active link

When there is an active link (SCO or ACL), the STA2416 cannot go in Deep Sleep mode whatever the UART state is. But the STA2416 baseband is made such that whenever it is possible, depending on the scheduled activity (number of link, type of link, amount of data exchanged), it goes in Sleep mode.

5.11 Software initiated low-power mode

A wide set of wake-up mechanisms is supported.

5.12 Bluetooth®, WLAN coexisting in collocated scenario

The coexistence interface uses four GPIO pins, when enabled.

Bluetooth® wireless and WLAN 802.11 b/g technologies occupy the same 2.4-GHz ISM band. STA2416 implements a set of mechanisms to avoid interference in a collocated scenario.

The STA2416 supports five different algorithms in order to provide efficient and flexible simultaneous function between the two technologies in collocated scenarios.

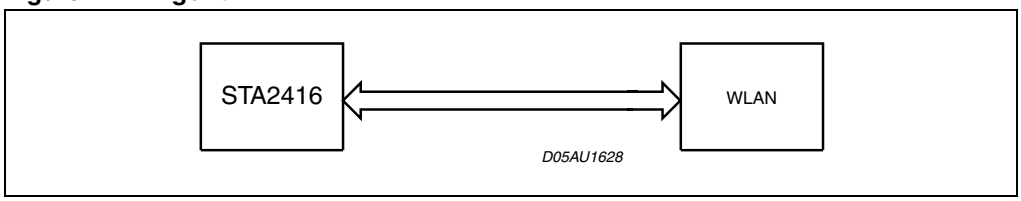
- **Algorithm 1:** PTA (packet traffic arbitration) based coexistence algorithm defined in accordance with the IEEE 802.15.2 recommended practice.
- **Algorithm 2:** the WLAN is the master and it indicates to the STA2416 when not to operate in case of simultaneous use of the air interface.
- **Algorithm 3:** the STA2416 is the master and it indicates to the WLAN chip when not to operate in case of simultaneous use of the air interface.
- **Algorithm 4:** two-wire mechanism.
- **Algorithm 5:** alternating wireless medium access (AWMA), defined in accordance with the WLAN 802.11 b/g technologies.

The algorithm is selected via HCI command. The default algorithm is algorithm 1.

5.12.1 Algorithm 1: packet traffic arbitration (PTA)

Algorithm 1 is based on a bus connection between the STA2416 and the WLAN chip.

Figure 7. Algorithm 1: PTA



By using this coexistence interface it's possible to dynamically allocate bandwidth to the two devices when simultaneous operations are required while the full bandwidth can be allocated to one of them in case the other one does not require activity. The algorithm involves a priority mechanism, which allows preserving the quality of certain types of link. A typical application would be to guarantee optimal quality to the Bluetooth® voice communication while an intensive WLAN communication is ongoing.

Several algorithms have been implemented in order to provide a maximum of flexibility and efficiency for the priority handling. Those algorithms can be activated via specific HCI commands.

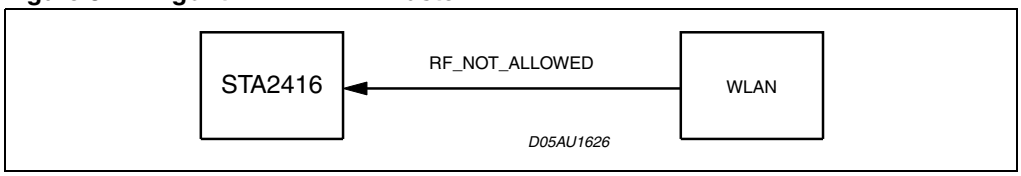
The combination of a time division multiplexing techniques to share the bandwidth in case of simultaneous operations and of the priority mechanism avoid the interference due to packet collision and it allows the maximization of the 2.4-GHz ISM bandwidth usage for both devices while preserving the quality of some critical types of link.

5.12.2 Algorithm 2: WLAN master

In case the STA2416 has to cooperate, in a collocated scenario, with a WLAN chip not supporting a PTA based algorithm, it's possible to put in place a simpler mechanism.

The interface is reduced to 1 line.

Figure 8. Algorithm 2: WLAN master



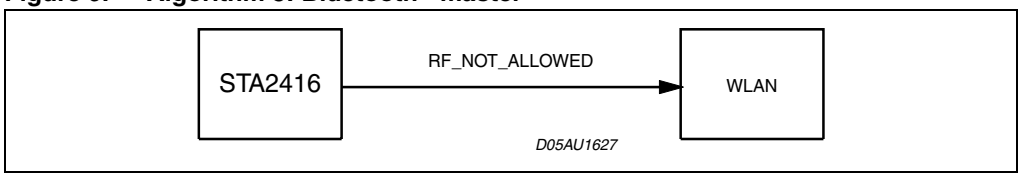
When the WLAN has to operate, it alerts HIGH the RF_NOT_ALLOWED signal and the STA2416 will not operate while this signals stays HIGH.

This mechanism permits to avoid packet collision in order to make an efficient use of the bandwidth but cannot provide guaranteed quality over the Bluetooth® links.

5.12.3 Algorithm 3: Bluetooth® master

This algorithm represents the symmetrical case of *Section 5.12.2: Algorithm 2: WLAN master*. Also in this case the interface is reduced to 1 line.

Figure 9. Algorithm 3: Bluetooth® master



When the STA2416 has to operate it puts the RF_NOT_ALLOWED signal HIGH. The WLAN will not operate while this signals stays HIGH.

This mechanism is used to avoid packet collision in order to make efficient use of the bandwidth. It provides high quality for all Bluetooth® links but cannot provide guaranteed quality over the WLAN links.

5.12.4 Algorithm 4: two-wire mechanism

Based on algorithms 2 and 3, the host decides, on a case-by-case basis, whether WLAN or Bluetooth® is master.

5.12.5 Algorithm 5: alternating wireless medium access (AWMA)

AWMA utilizes a portion of the WLAN beacon interval for Bluetooth® operations. From a timing perspective, the medium assignment alternates between usage following WLAN procedures and usage following Bluetooth procedures.

The timing synchronization between the WLAN and the STA2416 is done by the hardware signal MEDIUM_FREE.

Table 11. WLAN hardware signal assignment

WLAN	Scenario 1: PTA	Scenario 2: WLAN master	Scenario 3: BT master	Scenario 4: 2-wire	Scenario 5: AWMA
WLAN 1	TX_ CONFIRM	BT_RF_NOT_ ALLOWED	Not used	BT_RF_NOT_ ALLOWED	MEDIUM_FREE
WLAN 2	TX_ REQUEST	Not used	WLAN_RF_ NOT_ ALLOWED	WLAN_RF_ NOT_ ALLOWED	Not used
WLAN 3	STATUS	Not used	Not used	Not used	Not used
WLAN 4	OPTIONAL_ SIGNAL	Not used	Not used	Not used	Not used

6 Interfaces

6.1 UART interface

The chip contains two enhanced (128 byte transmit FIFO and 128 byte receive FIFO, sleep mode, 127 Rx and 128 Tx interrupt thresholds) UARTs named UART1 and UART2 compatible with the standard M16550 UART.

For UART1, only Rx and Tx signals are available (used for debug purposes).

UART2 features:

- standard HCI UART transport layer:
  - all HCI commands as described in the Bluetooth® specification 1.1
  - ST specific HCI command (check STA2416 Software Interface document for more information)
- RXD, TXD, CTS, RTS on permanent external pins
- 128-byte FIFOs, for transmit and for receive
- default configuration: 57.600 kbit/s
- specific HCI command to change to the baud rates given in *Table 12*

Table 12. List of supported baud rates

-	57.600 kbit/s (default)	4800 bit/s
921.6 kbit/s	38.4 kbit/s	2400 bit/s
460.8 kbit/s	28.8 kbit/s	1800 bit/s
230.4 kbit/s	19.2 kbit/s	1200 bit/s
153.6 kbit/s	14.4 kbit/s	900 bit/s
115.2 kbit/s	9600 bit/s	600 bit/s
76.8 kbit/s	7200 bit/s	300 bit/s

6.2 Synchronous serial interface

The synchronous serial interface (SSI) (or the synchronous peripheral interface (SPI)) is a flexible module supporting full-duplex and half-duplex synchronous communications with external devices in master and slave mode. It enables a microcontroller unit to communicate with peripheral devices or allows inter-processor communications in a multiple-master environment. This Interface is compatible with the Motorola SPI standard, with the Texas Instruments Synchronous Serial Frame format and with National Semiconductor Microwire standard.

Special extensions are implemented to support the Agilent® SPI interface for optical mouse applications and the 32-bit data SPI for stereo codec applications.

Some applications examples are given in *Section 6.8 on page 33*.

6.2.1 Feature description: Agilent® mode

One application is a combination of a Bluetooth® device with an Agilent® optical mouse sensor to build a Bluetooth Mouse. The Agilent chip has an SPI interface with one bi-directional data port.

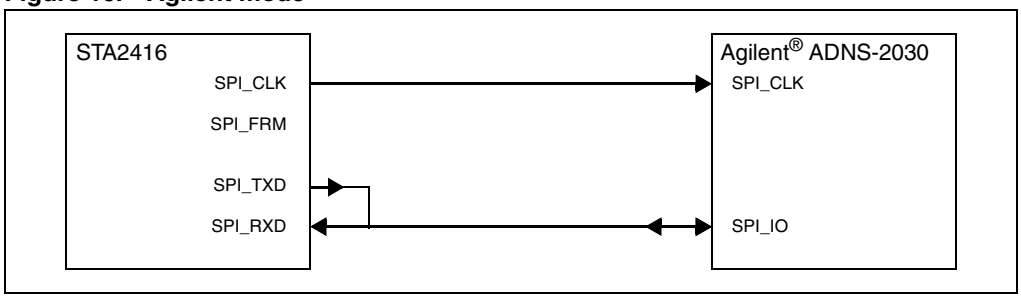
When SPI_IO from ADNS_2030 is driving, SPI_RXD should be active, while SPI_TXD is set as a 3-state high impedance input.

For a read operation, the Bluetooth® SPI_TXD is put in high impedance state after the reception of the address.

Note that this feature works independently of the SPI mode, supporting other combinations.

In this case, the devices are connected as described in *Figure 10*.

Figure 10. Agilent mode



6.2.2 Feature description: 32-bit SPI

One application is a Bluetooth® technology stereo headset. In this application, the audio samples are received from the emitter through the air using the Bluetooth baseband with ACL packets. The samples are decoded by the embedded ARM CPU (the samples were encode for compression in SBC codec) and then sent to a stereo codec though the SPI interface.

To support this application, the data size is 32 bits. The 32-bit support is implemented for both transmit and receive.

6.3 I^2C Interface

Used to access I^2C peripherals.

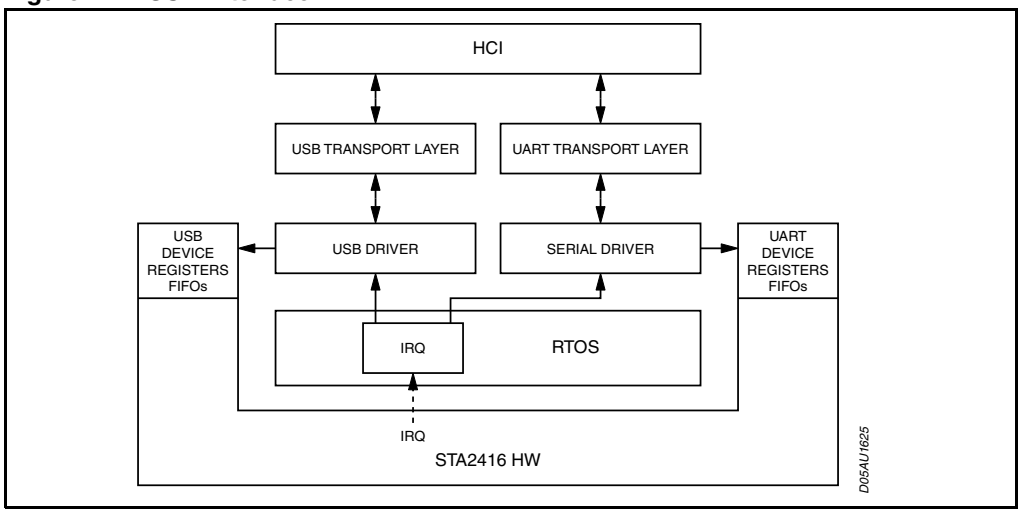
The interface is a fast master I^2C. It has full control of the interface at all times. I^2C slave function is not supported.

6.4 USB interface

The USB interface is compliant with the USB-2.0 full-speed specification. Maximum throughput on the USB interface is 12 Mbit/s.

Figure 11 gives an overview of the main components needed for supporting the USB interface, as specified in the Bluetooth® core specification. For clarity, the serial interface (including the UART transport layer) is also shown.

Figure 11. USB interface



The USB device registers and FIFOs are memory mapped. The USB driver will use these registers to access the USB interface. The equivalent exists for the HCI communication over UART.

For transmission to the host, the USB and Serial Drivers interface with the hardware via a set of registers and FIFOs, while in the other direction, the hardware may trigger the drivers through a set of interrupts (identified by the RTOS, and directed to the appropriate driver routines).

6.5 JTAG interface

The JTAG interface is compliant with the JTAG IEEE Standard 1149.1. Its allows both the boundary scan of the digital pins and the debug of the ARM7TDMI® application when connected with the standard ARM7® development tools.

6.6 RF interface

The STA2416 radio interface is compatible to BlueRF (unidirectional RxMode2 for data and unidirectional serial interface for control).

6.7 PCM voice interface

The voice interface is a direct PCM interface to connect to a standard codec (for example, STA529) including internal decimator and interpolator filters. The data can be linear PCM (13 to 16-bit), µ-law (8-bit) or A-law (8-bit). By default the codec interface is configured as master. The encoding on the air interface is programmable to be CVSD, A-law or µ-law.

The PCM block is able to manage the PCM bus with up to three timeslots.

In master mode, PCM clock and data can operate at 2 MHz or at 2.048 MHz to allow interfacing of standard codecs.

The four signals of the PCM interface are:

- PCM_CLK: PCM clock
- PCM_SYNC: PCM 8 kHz sync
- PCM_A: PCM data
- PCM_B: PCM data.

Directions of PCM_A and PCM_B are software configurable.

Three additional PCM_SYNC signals can be provided via the GPIOs. See *Chapter 9 on page 36* for more details.

Figure 12. PCM (A-law, µ-law) standard mode

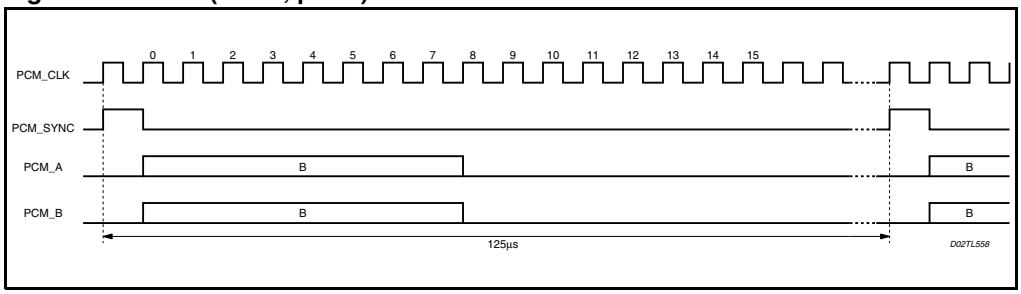


Figure 13. Linear mode

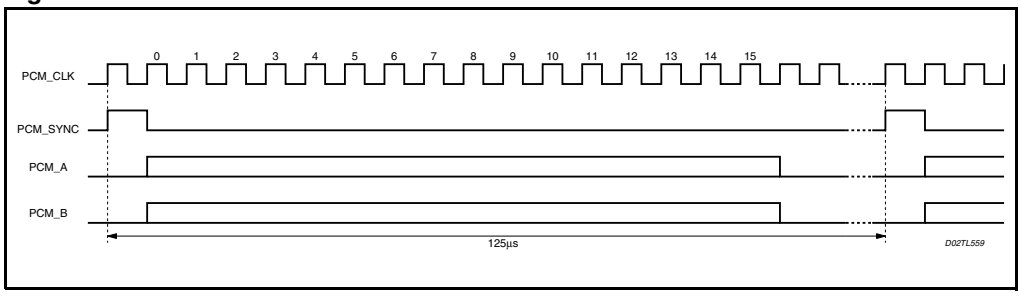
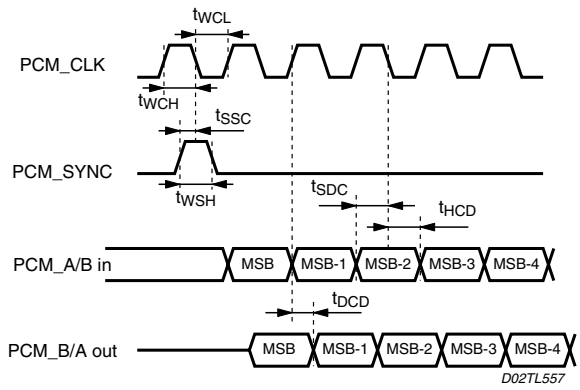


Table 13. PCM interface timing

Symbol	Description	Min	Typ	Max	Unit
F_{pcm_clk}	Frequency of PCM_CLK (master)		2048		kHz
F_{pcm_sync}	Frequency of PCM_SYNC		8		kHz
t_{WCH}	High period of PCM_CLK	200			ns
t_{WCL}	Low period of PCM_CLK	200			ns
t_{WSH}	High period of PCM_SYNC	200			ns
t_{SSC}	Setup time, PCM_SYNC high to PCM_CLK low	100			ns
t_{SDC}	Setup time, PCM_A/B input valid to PCM_CLK low	100			ns
t_{HCD}	Hold time, PCM_CLK low to PCM_A/B input invalid	100			ns
t_{DCD}	Delay time, PCM_CLK high to PCM_A/B output valid			150	ns

Figure 14. PCM interface timing



6.8 Applications examples

Figure 15. Bluetooth® technology v1.2 application example

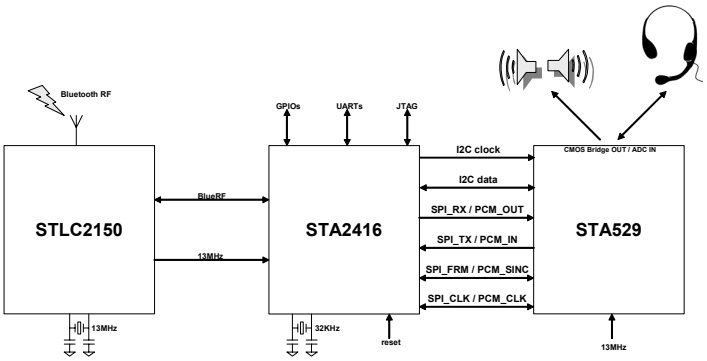
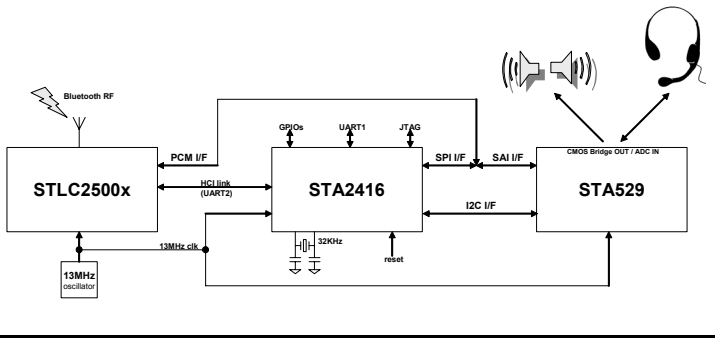


Figure 16. Bluetooth® technology v2.0 application example



7 HCI-UART transport layer

The UART transport layer has been specified by the Bluetooth® SIG, and allows HCI-level communication between a host controller (STA2416) and a host (for example, PC), via a serial line.

The objective of this HCI-UART transport layer is to make it possible to use the Bluetooth® HCI over a serial interface between two UARTs on the same PCB. The HCI-UART transport layer assumes that the UART communication is free from line errors.

7.1 UART settings

The HCI-UART transport layer uses the following settings for RS232:

Baud rate:	Configurable (default baud rate: 57.600 kbit/s)
Number of data bits:	8
Parity bit:	no parity
Stop bit:	1 stop bit
Flow control:	RTS/CTS
Flow-off response time:	3 ms

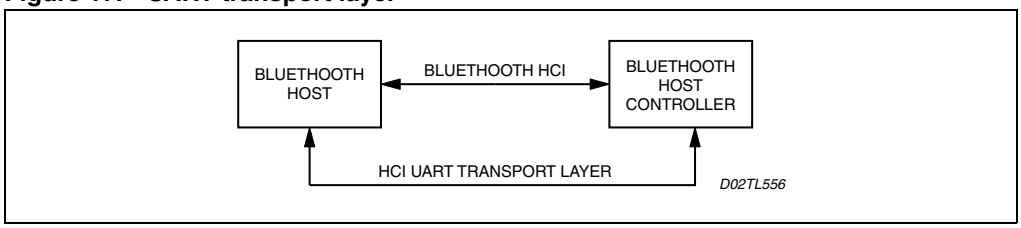
Flow control with RTS/CTS is used to prevent temporary UART buffer overrun. It should not be used for flow control of HCI, since HCI has its own flow control mechanisms for HCI commands, HCI events and HCI data.

If CTS is 1, then the host/host controller is allowed to send.

If CTS is 0, then the host/host controller is not allowed to send.

The flow-off response time defines the maximum time from setting RTS low until the byte flow actually stops. The signals should be connected in a null-modem fashion; that is, the local TXD should be connected to the remote RXD and the local RTS should be connected to the remote CTS and vice versa.

Figure 17. UART transport layer



8 HCI-USB transport layer

The USB transport layer has been specified by the Bluetooth® SIG, and allows HCI-level communication between a host controller (STA2416) and a host (for example, PC), via a USB interface. The USB transport layer is completely implemented in software. It accepts HCI messages from the HCI layer, prepares it for transmission over a USB bus, and sends it to the USB driver. It reassembles the HCI messages from USB data received from the USB driver, and sends these messages to the HCI layer. The transport layer does not interpret the contents (payload) of the HCI messages; it examines only the header.

9 Class-1 power support

The chip can control an external power amplifier (PA). Several signals are duplicated on GPIOs for this purpose in order to avoid digital/analogue noise loops in the radio.

A software controlled register enables the alternative functions of GPIO[15:11, 9:6] to generate the signals for driving an external PA in a Bluetooth® technology class-1 power application.

Each bit enables a dedicated signal on a GPIO pin, as described in *Table 14*.

Table 14. GPIOs alternative functions

Involved GPIO	Description
GPIO0	No dedicated function
GPIO1	WLAN 1
GPIO2	WLAN 2
GPIO3	WLAN 3
GPIO4	WLAN 4
GPIO5	Can be used for plug/unplug emulation in the case of USB connectivity
GPIO6	Power Class 1 RX_ON
GPIO7	Power Class 1 NOT_RXON
GPIO8	Power Class 1 PA0 or PCM sync 1
GPIO9	Power Class 1 PA1 or PCM sync 2
GPIO11	Power Class 1 PA3
GPIO12	Power Class 1 PA4
GPIO13	Power Class 1 PA5
GPIO14	Power Class 1 PA6
GPIO15	Power Class 1 PA7

The signal BRXEN is the same as the RX_ON (GPIO6) output pin. The signal NOT_RXON is the inverted signal, provided in order to save components on the application board.

PA7 to PA0 are the power amplifier control lines. They are managed, on a connection basis, by the baseband core. The power level programmed for a certain Bluetooth® technology connection is managed by the firmware, as specified in the Bluetooth SIG specification.

The WLAN signals, as described in *Section 5.12: Bluetooth®, WLAN coexisting in collocated scenario on page 26*, can be enabled on GIPIO pins

The WXTRA PCM sync signals, as described in *Section 6.7: PCM voice interface on page 31*, can be flexibly configured on GPIO pins to connect multiple codecs.

10 Package information

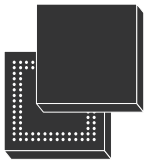
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: www.st.com.

Figure 18. LFBGA120 (10x10x1.4mm) mechanical data and package dimensions

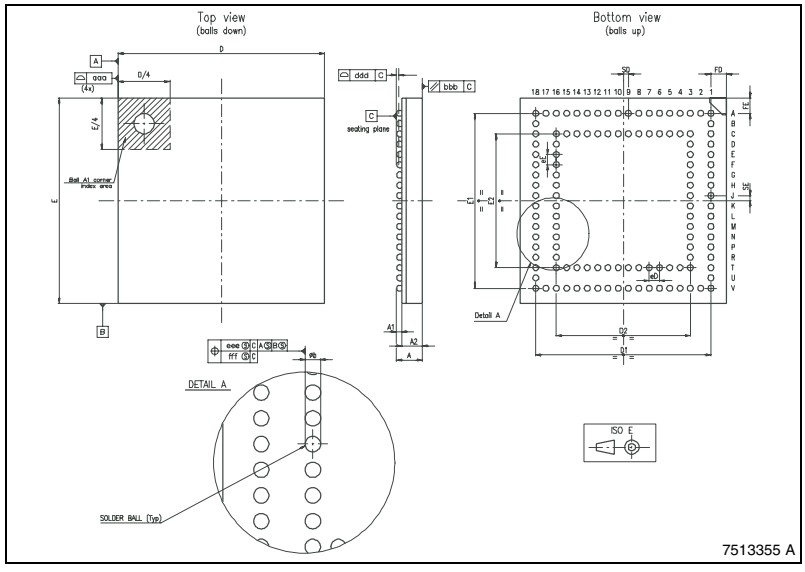
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.40			0.055
A1	0.20			0.008		
A2		1			0.039	
b	0.25	0.30	0.35	0.010	0.012	0.014
D	9.90	10.00	10.10	0.390	0.394	0.398
D1		8.50			0.335	
D2		6.50			0.256	
E	9.90	10.00	10.10	0.390	0.394	0.398
E1		8.50			0.335	
E2		6.50			0.256	
eD	0.50 basic			0.020 basic		
eE	0.50 basic			0.020 basic		
FD		0.75			0.029	
FE		0.75			0.029	
mD	18					
mE	18					
n	120 balls					
SE	0.25 basic			0.0098 basic		
SD	0.25 basic			0.0098 basic		
Tolerance						
aaa	0.15			0.006		
bbb	0.10			0.0039		
ddd	0.08			0.0031		
eee	0.15			0.006		
fff	0.05			0.002		

OUTLINE AND MECHANICAL DATA



Body: 10 x 10 x 1.4mm

LFBGA120
Low Fine Ball Grid Array



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12 Revision history

Table 15. Document revision history

Date	Revision	Changes
20-Dec-2006	1	Initial release.
18-Feb-2008	2	General updates Updated various references to system clock frequency New applications sections *on page 7* and *on page 33* Added sentence for downloading code at 13 MHz in *Section 5.2 on page 22*.

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