STA1050

CD-Audio one-chip

DATA BRIEF

Features

- CD-R, CD-RW playback
- CLV (1x, 2x, 4x) & CAV mode (6x)
- 3.3V supply / 1.8V supply / 3.3V capable and 5V tolerant I/O
- Low power consumption at top speed (tbd)
- Power down mode
- Power On Reset / Brownout controller
- 33.8688MHz external quartz/resonator
- LQFP128 package
- Temperature range -40/+85°C

Embedded ST7 Micro-controller

- 8-bit MCU with 4-stage pipeline
- 8.4672MHz clock with option up to 11.2896MHz
- 56Kbyte internal ROM (4Mb eFlash for debug)
- 4Kbytes internal RAM
- I^2C master/slave interface (400 kHz) + 1 CRQ line

Analogue Front-end Part

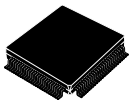
- A, B, C, D, E, F voltage inputs
- Automatic gain and offset control for diode signals
- ALPC circuit for laser control with integrated Power MOS
- 8-bit 2channels general purpose ADC

Digital Servo

- Automatic fine gain/balance/offset adjustment for tracking and focus
- Embedded 16bit servo DSP (33.8688MHz) with programmable sampling rate
- 1.7Kx32 DSP program RAM
- 256x16 DSP coefficient RAM
- 256x16 DSP data RAM
- PDM actuator controls (Focus/Tracking/Spindle/Sledge)
- Embedded Stepping Sledge motor controller
- CLV & CAV spindle control
- Defect generator logic

Acquisition

- Digital Interpolator & Equalizer



LQFP128

- Full range adjustment-free digital PLL
- EFM Demodulation and Synchronisation
- Q subcode & CD Text Decoder

Error Correction

- CIRC, capable of dual C1 and quadruple C2 erasure corrections
- jitter absorbing capacity ±24 frames

Schock-Proof controller

- Up to 64Mbit External SDRAM interface
- 4/8/16 bit data bus interface
- ADPCM (4:1) lossy compression for extended shock proof capability

Digital Interfaces

- I^2S + EIAJ CP-340 output interface with slave mode capability (external clock)
- C2PO output
- SPDIF transmitter (IEC958)
- Soft audio mute/fade/attenuation
- De-emphasis filter
- I2S input for audio DAC if external audio processing (i.e. MP3 decoder) (or 3GPIOs)
- 8 dedicated GPIOs
- MLB interface for direct MOST

Audio Features

- Digital Equalizer for bass/tremble control
- Built-in stereo DAC with 96 dB SNR
- De-emphasis filter built-in

Development Environment

- On Chip ST7 Emulation (2 dedicated pins)
- C language compiler for ST7, Macro assembler, Linker, archiver, functional simulator
- Windows debugger

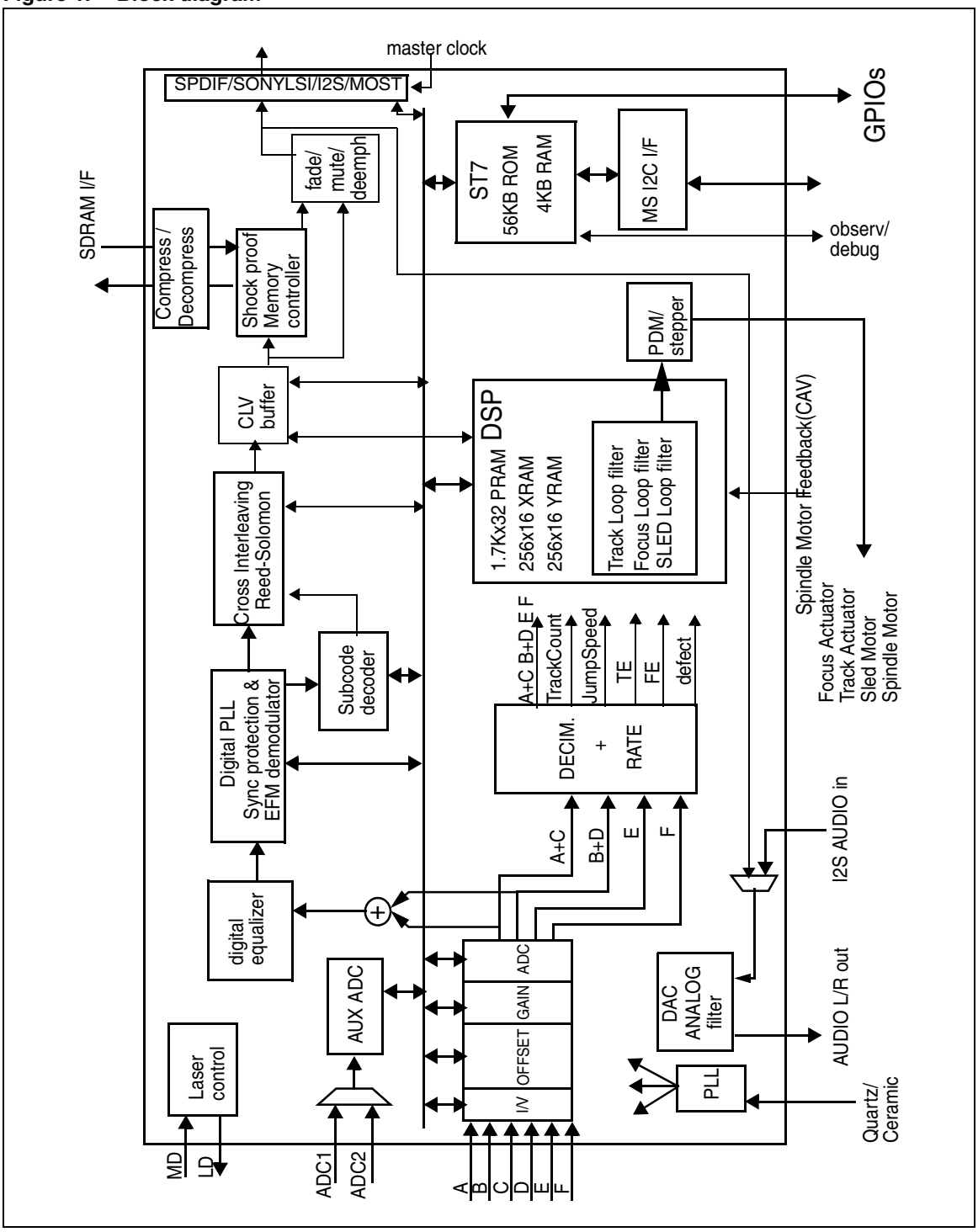
Order code

Part number	Package	Packing
STA1050	LQFP128	Tube

Contents

1 Block diagram

Figure 1. Block diagram



2 Pin function description

Table 1. Pin List- LQFP128

N°	Name	Description	Pin Type
1	DRD15/FLASH_D7	SDRAM Data 15 or FLASH Data 7	bidir, 3.3V, 2mA
2	DRD0/GPC0	SDRAM Data 0 or ST7 GPIO PC0	bidir, 3.3V, 2mA
3	VDDPAD5	3.3V	Vdd
4	VDDPAD1	3.3V	Vdd
5	RESETN	Hardware reset input (pull-up)	in, 3.3V
6	TESTEN	Test enable signal (Active low)	in, 3.3V
7	I2C_SDA/GPB5	I2C I/F data or ST7 GPIO PB5	i2c dedicated
8	I2C_SCL/GPB4	I2C I/F clock or ST7 GPIO PB4	i2c dedicated
9	I2C_CRQ	I2C CRQ lime or ST7 GPIO PA0	i2c dedicated
10	#nc	to be connected to ground on PCB	
11	#nc	to be connected to ground on PCB	
12	PLL_VSS18P	PLL Digital&Analog ground	Vss
13	PLL_VDDA33P	PLL 3.3 Analog power supply	Vdd
14	#nc	to be connected to ground on PCB	
15	PLL_XTI	Crystal input	analog in
16	PLL_XTO	Crystal output	analog out
17	#nc	to be connected to ground on PCB	
18	PLL_VDDA18P	PLL 1.8V Analog power supply	Vdd
19	PLL_VDD18P	PLL 1.8V Digital power supply	Vdd
20	FE_VSSA33S	Ground for servo channels	Vss
21	FE_A	OPU “A” input	analog in
22	FE_C	OPU “C” input	analog in
23	FE_B	OPU “B” input	analog in
24	FE_D	OPU “D” input	analog in
25	FE_E	OPU “E” input	analog in
26	FE_F	OPU “F” input	analog in
27	FE_VDDA33S	3.3V Analog for servo channels/ 3.3V for AFE pad ring (decoupling cap to Vssa)	Vdd
28	FE_VDDPAD1	3.3V for AFE pad ring	Vdd
29	FE_ADCIN1	General purpose ADC input 1	analog in
30	FE_ADCIN2	General purpose ADC input 2	analog in
31	FE_VREF_ADC	General purpose ADC Vtop reference output	analog out
32	FE_VREF_OUT	External Vref Pickup (decoupling cap 1nF)	analog out

Table 1. Pin List- LQFP128 (continued)

N°	Name	Description	Pin Type
33	FE_VDDA33R	Analog 3.3V for Bandgap	Vdd
34	FE_CEXT	external cap for bandgap (1nF)	analog
35	FE_REXT	external res for bandgap (25kOhm)	analog
36	FE_VSSA33R	Analog Ground Bandgap	Vss
37	FE_MD_LAS	Laser driver input from monitor diode	analog in
38	FE_CAP_LAS	Laser driver compensation cap (30nF)	analog
39	FE_LD_LAS	First Laser driver output	analog out
40	FE_LD1_LAS	Second Laser driver output	analog out
41	FE_VDDPAD2	3.3V for AFE pad ring	Vdd
42	FE_VDDA33T	Analog 3.3V for test buffer	Vdd
43	FE_TESTP	Test Buffer Positive Output	analog out
44	FE_TESTN	Test Buffer Negative Output	analog out
45	FE_VSSA33T	Analog Ground Test Buffer	Vss
46	FE_VDDA18AD	Analog 1.8V ADC	Vdd
47	FE_VSSA18AD	Analog ground ADC	Vss
48	#nc	to be connected to ground on PCB	
49	FFSR	Focusing actuator control signal output - PDM	bidir, 3.3V, 2mA
50	#nc	to be connected to ground on PCB	
51	REFFSR	Clock (50% duty cycle) for Actuator PDM reference	bidir, 3.3V, 2mA
52	SPDL	Spindle motor control signal output - PDM	bidir, 3.3V, 2mA
53	SLED1	SLED motor control signal output1 (stepping/DC) - PDM	bidir, 3.3V, 2mA
54	SLED2	SLED motor control signal output2 (stepping) -PDM	bidir, 3.3V, 2mA
55	ICC1/GPB6	Serial interface TX or ST7 GPIO PB6	bidir, 3.3V, 2mA
56	ICC2/GPB7	Serial interface RX or ST7 GPIO PB7	bidir, 3.3V, 2mA
57	VDD_TOP	Core VDD 1.8V	Vdd
58	TFSR	Tracking actuator control signal output - PDM	bidir, 3.3V, 2mA
59	VSS_TOP	Core VSS Ground	Vss
60	VSSPAD1	Pad Ring ground	Vss
61	VDDPAD2	3.3V for Digital Pad Ring	Vdd
62	VDDPAD3	3.3V for Digital Pad Ring	Vdd
63	ICD_N	On-Chip-Emulator enable	in, 3.3V
64	DRD4/FLASH_OE	SDRAM Data 4 or FLASH Output Enable	bidir, 3.3V, 2mA
65	GPB0/CAV	ST7 GPIO PB0 or CAV feedback input	bidir, 3.3V, 2mA
66	GPA7	ST7 GPIO PA7 (external interrupt)	bidir, 3.3V, 2mA
67	GPA6	ST7 GPIO PA6	bidir, 3.3V, 2mA

Table 1. Pin List- LQFP128 (continued)

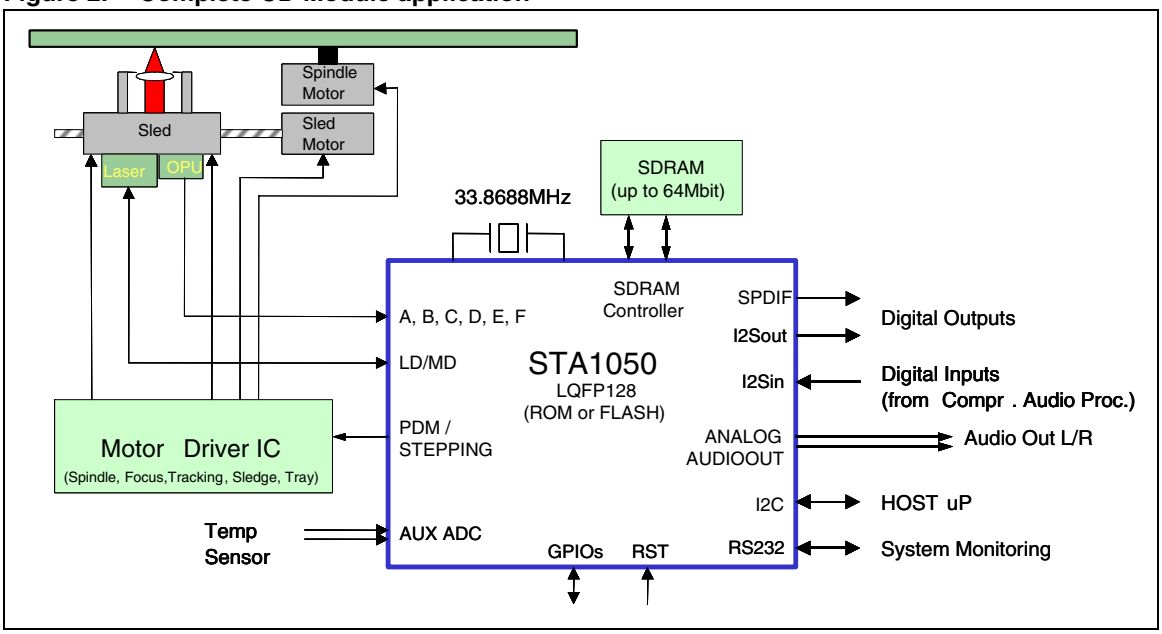
N°	Name	Description	Pin Type
68	GPA5	ST7 GPIO PA5	bidir, 3.3V, 2mA
69	GPA4	ST7 GPIO PA4	bidir, 3.3V, 2mA
70	GPA3	ST7 GPIO PA3	bidir, 3.3V, 2mA
71	GPA2/ICCDATA	ST7 GPIO PA2 or ICC data for ST7 emulator	bidir, 3.3V, 2mA
72	GPA1/ICCCLK	ST7 GPIO PA1 or ICC clock for ST7 emulator	bidir, 3.3V, 2mA
73	VSS_TOP	Core VSS Ground	Vss
74	VSSPAD2	Pad Ring ground	Vss
75	VDD_TOP	Core VDD 1.8V	Vdd
76	MEMSEL0	Memory Select (ROM,FLASH)	in, 3.3V, pull-down
77	SPDIF	SPDIF Digital output	bidir, 3.3V, 2mA
78	VDDPAD4	3.3V for Digital Pad Ring	Vdd
79	C2PO	EIAJ CP-340 I/F C2PO	bidir, 3.3V, 2mA
80	SDI/MLBDATA/GPB3	I2S serial data input or MLB data line or ST7 GPIO PB3	bidir, 3.3V, 2mA
81	WSIN/MLBSIG/GPB2	I2S Word select input or MLB sig line or ST7 GPIO PB2	bidir, 3.3V, 2mA
82	SCKIN/MLBCLK/GPB1	I2S Clk input or MLB clock line or ST7 GPIO PB1	bidir, 3.3V, 2mA
83	LRCK/WSO	EIAJ CP-340 I/F L/R signal or I2S Word Select output	bidir, 3.3V, 2mA
84	MDAT/SDO	EIAJ CP-340 I/F dataout or I2S Data output	bidir, 3.3V, 2mA
85	BCLK/SCKO	EIAJ CP-340 I/F clk output or I2S Clock output	bidir, 3.3V, 2mA
86	VSSPAD3	Pad Ring ground	Vss
87	DRD5/FLASH_CE	SDRAM Data 5 or FLASH Chip Enable	bidir, 3.3V, 2mA
88	DRD7/FLASH_RSTN	SDRAM Data 7 or FLASH Reset	out, 3.3V, 2mA
89	DRD6/FLASH_RYBY	SDRAM Data 6 or FLASH Ready Busy	out, 3.3V, 2mA
90	DRD8/FLASHD0	SDRAM Data 8 or FLASH Data 0	bidir, 3.3V, 2mA
91	#nc	to be connected to ground on PCB	
92	ADAC_VDDA	3.3V Audio DAC	Vdd
93	OUTR	Right channel analog output	analog out
94	VMC	Common Mode input for audio DAC	analog in
95	OUTL	Left channel analog output	analog out
96	ADAC_VSSA	Audio DAC ground	Vss
97	DRCLK	SDRAM CLK	out, 3.3V, 2mA
98	DRD3/GPC3	SDRAM Data 3 or ST7 GPIO PC3	bidir, 3.3V, 2mA
99	DRA0/FLASHA0	SDRAM Address 0 or Flash Address 0	out, 3.3V, 2mA
100	VSSPAD4	Pad Ring ground	Vss
101	DRCAS/FLASHA15	SDRAM Col address sel or Flash Address 15	out, 3.3V, 2mA
102	DRRAS/FLASHA14	SDRAM Row address sel or Flash Address 14	out, 3.3V, 2mA

Table 1. Pin List- LQFP128 (continued)

N°	Name	Description	Pin Type
103	DRD14/FLASHD6	SDRAM Data 14 or Flash Data 6	bidir, 3.3V, 2mA
104	DRBA1/FLASHA13	SDRAM Bank sel address 1 or Flash Address 13	out, 3.3V, 2mA
105	DRBA0/FLASHA12	SDRAM Bank sel address 0 or Flash Address 12	out, 3.3V, 2mA
106	DRA11/FLASHA11	SDRAM Address 11 or Flash Address 11	out, 3.3V, 2mA
107	DRD13/FLASHD5	SDRAM Data 13 or Flash Data 5	bidir, 3.3V, 2mA
108	DRA10/FLASHA10	SDRAM Address 10 or Flash Address 10	out, 3.3V, 2mA
109	DRA9/FLASHA9	SDRAM Address 9 or Flash Address 9	out, 3.3V, 2mA
110	DRD12/FLASHD4	SDRAM Data 12 or Flash Data 4	bidir, 3.3V, 2mA
111	DRWR/FLASHA16	SDRAM Write control or Flash Address 16	out, 3.3V, 2mA
112	VDDPAD6	3.3V for Digital Pad Ring	Vdd
113	DRD11/FLASHD3	SDRAM Data 11 or Flash Data 3	bidir, 3.3V, 2mA
114	DRD2/GPC2	SDRAM Data 2 or ST7 GPIO PC2	bidir, 3.3V, 2mA
115	DRA8/FLASHA8	SDRAM Address 8 or Flash Address 8	out, 3.3V, 2mA
116	DRA7/FLASHA7	SDRAM Address 7 or Flash Address 7	out, 3.3V, 2mA
117	DRA6/FLASHA6	SDRAM Address 6 or Flash Address 6	out, 3.3V, 2mA
118	DRD10/FLASHD2	SDRAM Data 10 or Flash Data 2	bidir, 3.3V, 2mA
119	DRA5/FLASHA5	SDRAM Address 5 or Flash Address 5	out, 3.3V, 2mA
120	DRA4/FLASHA4	SDRAM Address 4 or Flash Address 4	out, 3.3V, 2mA
121	DRD9/FLASHD1	SDRAM Data 9 or Flash Data 1	bidir, 3.3V, 2mA
122	DRA3/FLASHA3	SDRAM Address 3 or Flash Address 3	out, 3.3V, 2mA
123	DRA2/FLASHA2	SDRAM Address 2 or Flash Address 2	out, 3.3V, 2mA
124	DRD1/GPC1	SDRAM Data 1 or ST7 GPIO PC1	bidir, 3.3V, 2mA
125	DRCLKE/FLASH_WEN	SDRAM CLK enable or Flash Write Enable	out, 3.3V, 2mA
126	VSSPAD5	Pad Ring ground	Vss
127	DRA1/FLASHA1	SDRAM Address 1 or Flash Address 1	out, 3.3V, 2mA
128	APAD16	Flash Address 17	in, 3.3V

3 System description

Figure 2. Complete CD Module application



STA1050 is an high integration, high performance chip which integrates most required components for CD module application. The only external components needed are:

- a ceramic oscillator with a nominal frequency of 33.8688 MHz. All frequencies needed in STA1050 are internally synthesised thanks to a PLL.
- a motor driver IC to drive focus, tracking, spindle, sledge and tray motors
- a SDRAM to implement shock-proof handling (if needed)

STA1050 includes an embedded 8-bit CPU (ST7) running from an internal ROM (or Flash for debug) Program memory.

The laser diode is driven directly using an embedded power PMOS.

2 analog inputs and 8GPIOs are available to monitor sensors and switches or to control auxiliary circuitry.

An embedded Audio DAC generates a stereo audio output. This DAC can use as input a digital stream received by the I2Sin interface from an external source, for example a compressed audio processor.

Several digital outputs are available: SPDIF, I2S, EIAJ and a MLB (Media Local Bus) interface which allows STA1050 to be directly interfaced to current and future MOST networks.

4 Package information

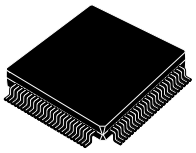
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

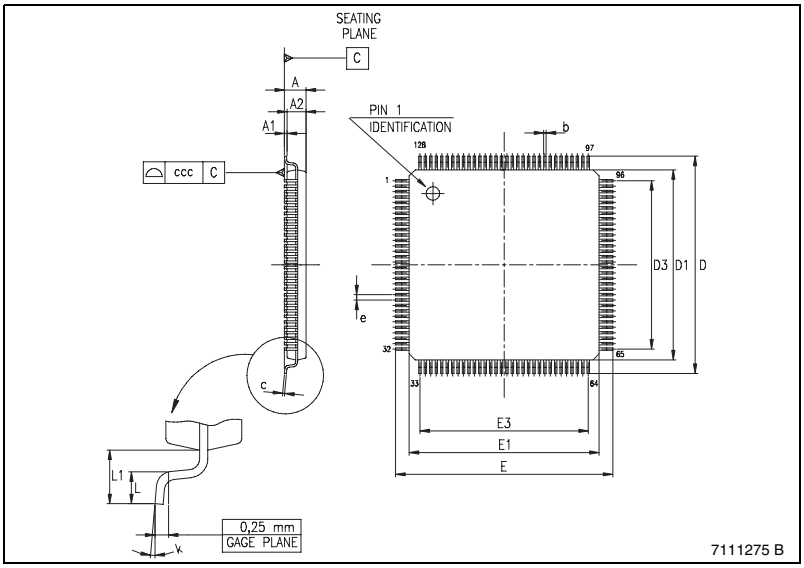
Figure 3. LQFP128 (14x14x1.4mm) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.600			0.063
A1	0.050		0.150	0.002		0.006
A2	1.350	1.400	1.450	0.053	0.055	0.057
b	0.130	0.180	0.230	0.005	0.007	0.009
c	0.090		0.200	0.003		0.008
D	15.800	16.000	16.200	0.622	0.630	0.638
D1	13.800	14.000	14.200	0.543	0.551	0.559
D3		12.400			0.488	
e		0.400			0.016	
E	15.800	16.000	16.200	0.622	0.630	0.638
E1	13.800	14.000	14.200	0.543	0.551	0.559
E3		12.400			0.488	
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.000			0.0393	
K	0° (min.), 3.5° (typ.), 7°(max.)					
ccc			0.080			0.003

OUTLINE AND MECHANICAL DATA



LQFP128
(14 x 14 x 1.40mm)



5 Revision history

Table 2. Document revision history

Date	Revision	Changes
21-Nov-2006	1	Initial release.

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