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ML675050

ARM7TDMI based Micro-controller (for IC card Reader/Writer)

GENERAL DESCRIPTION

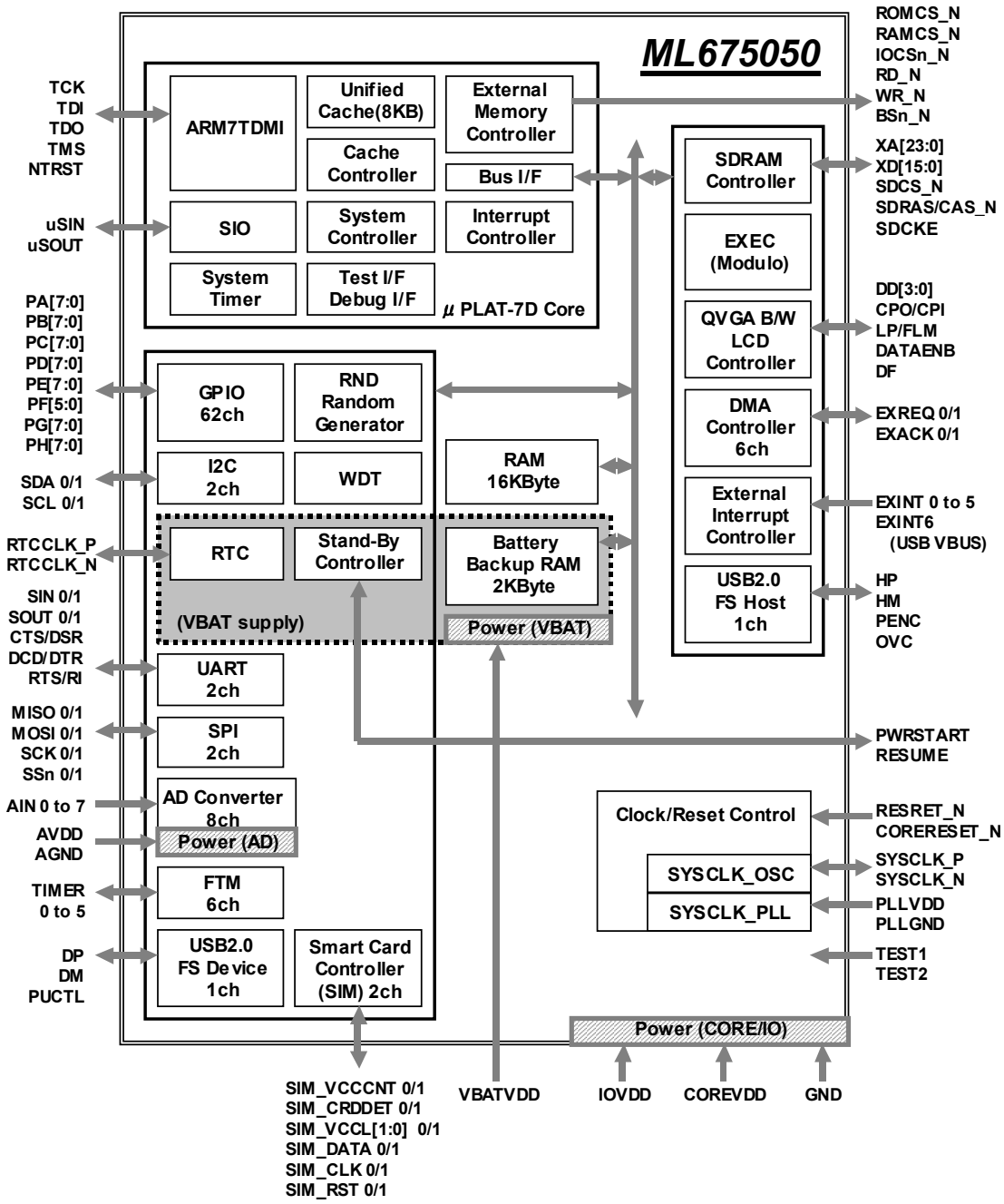
The ML675050 is a ARM7TDMITM based MCU optimized for IC card reader/writers, which supports ISO-7816 T=0 / T=1 protocol complying IC card interface, a variety of serial interfaces, QVGA B/W STN LCD controller and USB2.0 FS hostand device controller.

The ML675050 also includes a Modulo Calculation Accelerator for Encryption / Decryption, which enables RSA encryption/decryption much faster than software based solution under the same conditions. A Battery Backup RAM is also integrated for safely storing crypto-key data. Therefore ML675050 is an ideal MCU for IC card reader/writer based applications.

FEATURES

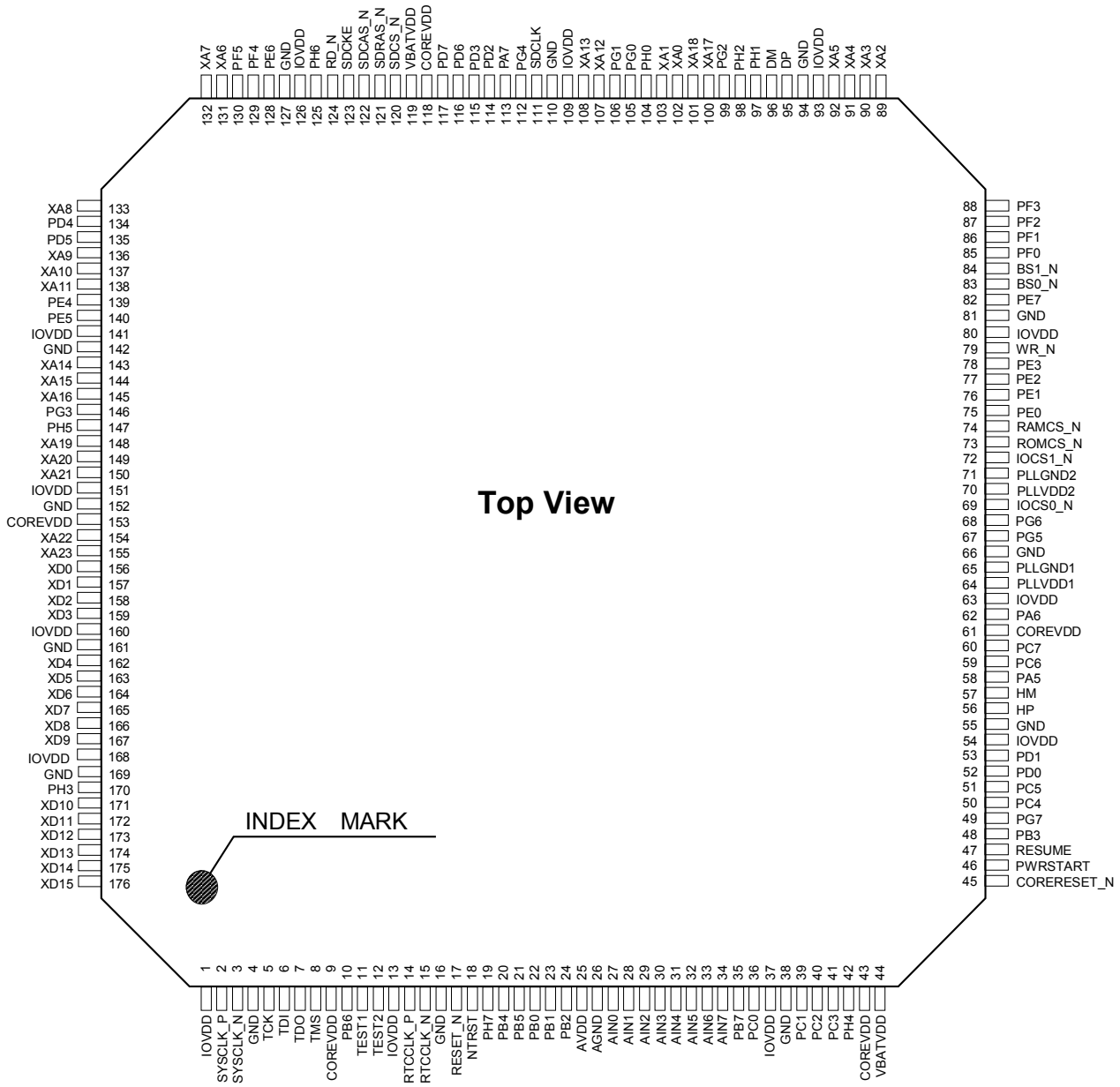
• CPU	32-bit RISC CPU (ARM7TDMI)
• CPU Platform	μ PLAT-7D® (with 8KB Unified Cache memory)
• Internal Memory	16Kbyte RAM and 2Kbyte Battery Backup RAM
• External Memory	ROM(FLASH), SRAM, SDRAM, I/O devices(memory-mapped I/O)
• Interrupt (Internal LSI)	38 sources, Seven levels of interrupt priorities can be set for each interrupt source.
• Interrupt (External LSI)	7 sources(with 1 source being FIQ), Seven levels of interrupt priorities can be set for each interrupt source.
• DMA Controller	6 channels, transfer request source can be assigned for each channel.
• LCD Controller	QVGA(320x240 pixcels) Monochrome 1bpp STN with Built-in buffer (10KByte)
• Modulo calculation Accelerator	Installed hardware that supports multi-bit lengths (512,768,1024 bits) Can be extended to support more than 1024 bits by software Modulo exponential calculation: Within 20 ms (for 1024-bit, 64MHz) Within 80 ms (for 2048-bit, 64MHz)
• Ramdom Number Generator	8-bit random number generator
• Smart Card Interface(SIM)	2-ch ISO UART, each having a built-in 48-Byte FIFO Supports asynchronous protocols T=0 and T=1 conform to ISO7816
• Watchdog timer	16-bit x 1-ch timer, Maximum overflow time is 6.71 sec. Interrupts or resets are generated according to settings.
• Analog-to-Digital Converter	12-bit x 8-ch sequential conversion type, Max. 400K samples/sec.
• System timer	16-bit x 1-ch Auto-Reload timer
• Flexible timer	16-bit x 6-ch, Operable in each of Auto-Reload/Compeare-Out/Pulse-Width-Modulation/Capture
• Real time clock(RTC)	1-ch, generate 1 second from 32.768 kHz, Built-in 100 year counter.
• USB2.0 Full-Speed Host	1-ch Full-Speed Host interface, compliant with USB2.0 and OpenHCI 1.0a, supports four types of transfer.
• USB2.0 Full-Speed Device	1-ch Full-Speed Device interface, compliant with USB2.0, support four types of transfer.
• Serial interface	I2C x 2-ch, SPI x 2-ch, UART x 2-ch, and SIO x 1-ch
• JTAG interface	Connectable to JTAG ICE
• Oscillator	2 Oscillators, for Main clock (8 or 16 MHz) and for RTC (32.768KHz)
• Power management	Stand-by (Turns power off) and Clock stop (CPU halt/STOP)
• Operating frequency	Max. 64MHz (use internal PLL)
• Operating temperature(ambient)	-40C to +85C
• Package(QFP)	176-pin plastic LQFP(LQFP176-P2424-0.50-ZK)
• Package(BGA)	176-pin plastic LFBGA(P-LFBGA176-1313-0.80-2)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW) (1/2)

176-Pin LQFP (LQFP176-P-2424-0.50-ZK)



PIN CONFIGURATION (TOP VIEW) (2/2)

176-Pin LFBGA (P-LFBGA176-1313-0.80-2)

PF3	XA3	XA4	XA0	DP	DM	PG1	SDCLK	PG4	PD2	PD3	PD7	SDCKE	PF5	XA7	15
PF1	PF2	XA5	PH1	PH2	XA17	PH0	XA12	XA13	SDCS_N	RD_N	SDCAS_N	PF4	XA6	PD4	14
BS0_N	PF0	PE7	XA2	PG2	XA18	XA1	PG0	PA7	PD6	SDRAS_N	PH6	PE6	XA8	XA9	13
WR_N	BS1_N	PE3	IOVDD	GND	IOVDD	GND	COREVDD	VBATVDD	IOVDD	GND	IOVDD	PD5	XA10	XA11	12
PE1	PE0	PE2	GND								GND	XA14	PE5	PE4	11
ROMCS_N	PLLVDD2	RAMCS_N	IOVDD								GND	PG3	XA15	XA16	10
IOCS0_N	PLLGND2	IOCS1_N	IOVDD								IOVDD	PH5	XA19	XA21	9
PG5	PG6	PLLGND1	GND								COREVDD	XA23	XA20	XA22	8
HM	PLLVDD1	PC6	COREVDD								IOVDD	XD1	XD3	XD0	7
HP	PA5	PD1	GND								GND	XD5	XD6	XD2	6
PA6	PD0	PC5	IOVDD								IOVDD	GND	XD9	XD4	5
PC4	PC7	PG7	VBATVDD	COREVDD	IOVDD	GND	GND	IOVDD	COREVDD	GND	IOVDD	XD8	XD7	PH3	4
PB3	PWRSTART	PH4	PB7	AIN3	AIN5	AIN1	PB2	PB0	RESET_N	TEST1	TDI	XD13	XD11	XD10	3
RESUME	PC3	PC1	AIN6	PC0	AIN2	AVDD	AGND	NTRST	TEST2	PB4	TCK	TMS	XD14	XD12	2
CORERESET_N	PC2	AIN7	AIN4	AIN0	PB1	PB5	PH7	RTCCLK_N	RTCCLK_P	PB6	TDO	SYSCLK_N	SYSCLK_P	XD15 ○	1
R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

ML675050

176-PIN LFBGA

BOTTOM VIEW

0.8 mm pitch

LIST OF PINS (FUNCTION LIST) (1/6)

Pin		Primary Function			Secondary Function			Tertiary Function		
QFP	BGA	Symbol	I/O	Description	Symbol	I/O	Description	Symbol	I/O	Description
1	D4	IOVDD	VDD	I/O power						
2	B1	SYSCLK_P	I	Ocillation (main)						
3	C1	SYSCLK_N	O							
4	E4	GND	GND	GND						
5	D2	TCK	I	JTAG TCK	PA0	IO	GPIO A bit0			
6	D3	TDI	I	JTAG TDI	PA1	IO	GPIO A bit1			
7	D1	TDO	O	JTAG TDO	PA2	IO	GPIO A bit2			
8	C2	TMS	I	JTAG TMS	PA3	IO	GPIO A bit3			
9	F4	COREVDD	VDD	CORE power						
10	E1	PB6	IO	GPIO B bit6	SDA1(note)	IO	I2C1 Data	EXINT2	I	INT input 2
11	E3	TEST1	I	test mode						
12	F2	TEST2	I	test mode						
13	G4	IOVDD	VDD	I/O power						
14	F1	RTCCLK_P	I	Oscillation (RTC)						
15	G1	RTCCLK_N	O							
16	H4	GND	GND	GND						
17	F3	RESET_N	I	Reset input						
18	G2	NTRST	I	JTAG Reset input	PA4	IO	GPIO A bit4			
19	H1	PH7	IO	GPIO H bit7	TIMER5	IO	Timer bit5	uSOUT	O	SIO Tx
20	E2	PB4	IO	GPIO B bit4	SDA0(note)	IO	I2C0 Data			
21	J1	PB5	IO	GPIO B bit5	SCL0(note)	IO	I2C0 Clock			
22	G3	PB0	IO	GPIO B bit0	TIMER0	IO	Timer bit0	EXREQ0	I	DMA req. 0
23	K1	PB1	IO	GPIO B bit1	TIMER1	IO	Timer bit1	EXACK0	O	DMA ack. 0
24	H3	PB2	IO	GPIO B bit2	TIMER2	IO	Timer bit2	EXINT0	I	INT input 0
25	J2	AVDD	A-VDD	AD Converter Power						
26	H2	AGND	A-GND	AD converter GND						
27	L1	AIN0	I	Analog in 0						
28	J3	AIN1	I	Analog in 1						
29	K2	AIN2	I	Analog in 2						
30	L3	AIN3	I	Analog in 3						
31	M1	AIN4	I	Analog in 4						
32	K3	AIN5	I	Analog in 5						
33	M2	AIN6	I	Analog in 6						
34	N1	AIN7	I	Analog in 7						
35	M3	PB7	IO	GPIO B bit7	SCL1(note)	IO	I2C1 Clock	EXINT3	I	INT input 3
36	L2	PC0	IO	GPIO C bit0	DD0	O	LCD Data 0			
37	K4	IOVDD	VDD	I/O power						
38	J4	GND	GND	GND						
39	N2	PC1	IO	GPIO C bit1	DD1	O	LCD Data 1			
40	P1	PC2	IO	GPIO C bit2	DD2	O	LCD Data 2			
41	P2	PC3	IO	GPIO C bit3	DD3	O	LCD Data 3			

(note) : This pin operates as NMOS Open drain in output mode

LIST OF PINS (FUNCTION LIST) (2/6)

Pin		Primary Function			Secondary Function			Tertiary Function		
QFP	BGA	Symbol	I/O	Description	Symbol	I/O	Description	Symbol	I/O	Description
42	N3	PH4	IO	GPIO H bit4	SIM_VCCL10	O	SIM1 Voltage Control 0			
43	L4	COREVDD	VDD	CORE power						
44	M4	VBATVDD	VDD	BAT power						
45	R1	CORE RESET_N	I	CORE reset						
46	P3	PWR START	O	Regulator control						
47	R2	RESUME	I	Resume from Stand-by						
48	R3	PB3	IO	GPIO B bit3	TIMER3	IO	Timer bit3	EXINT1	I	INT input 1
49	N4	PG7	IO	GPIO G bit7	TIMER4	IO	Timer bit4	uSIN	I	SIO Rx
50	R4	PC4	IO	GPIO C bit4	CPO	O	LCD Clock Input			
51	N5	PC5	IO	GPIO C bit5	LP	O	LCD Line Synchronous Pulse			
52	P5	PD0	IO	GPIO D bit0	MISO0	IO	SPI0 MISO			
53	N6	PD1	IO	GPIO D bit1	MOSI0	IO	SPI0 MOSI			
54	D5	IOVDD	VDD	I/O power						
55	C5	GND	GND	GND						
56	R6	HP	IO	USBhost D+						
57	R7	HM	IO	USBhost D-						
58	P6	PA5	IO	GPIO A bit5	DATAENB	O	LCD Data Enable			
59	N7	PC6	IO	GPIO C bit6	FLM	O	LCD Frame Synchronous Pulse			
60	P4	PC7	IO	GPIO C bit7	DF	O	LCD AC Conversion			
61	M7	COREVDD	VDD	CORE power						
62	R5	PA6	IO	GPIO A bit6	CPI	I	LCD Clock Output			
63	M5	IOVDD	VDD	I/O power						
64	P7	PLLVDD1	PLL-VDD	PLL power 1						
65	N8	PLLGND1	PLL-GND	PLL GND 1						
66	D6	GND	GND	GND						
67	R8	PG5	IO	GPIO G bit5	SIM_VCCL01	O	SIM0 Voltage Control 1			
68	P8	PG6	IO	GPIO G bit6	SIM_CRDDET0	I	SIM0 Card Detect			
69	R9	IOCS0_N	O	Ext. I/O 0 Chip Select						
70	P10	PLLVDD2	PLL-VDD	PLL power 2						
71	P9	PLLGND2	PLL-GND	PLL GND 2						

LIST OF PINS (FUNCTION LIST) (3/6)

Pin		Primary Function			Secondary Function			Tertiary Function		
QFP	BGA	Symbol	I/O	Description	Symbol	I/O	Description	Symbol	I/O	Description
72	N9	IOCS1_N	O	Ext. I/O 1 Chip Select						
73	R10	ROMCS_N	O	Ext. ROM Chip Select						
74	N10	RAMCS_N	O	Ext. RAM Chip Select						
75	P11	PE0	IO	GPIO E bit0	SIN0	I	UART0 Rx			
76	R11	PE1	IO	GPIO E bit1	SOUT0	O	UART0 Tx			
77	N11	PE2	IO	GPIO E bit2	CTS	I	UART0 CTS	EXINT0	I	INT input 0
78	N12	PE3	IO	GPIO E bit3	RTS	O	UART0 RTS	EXINT1	I	INT input 1
79	R12	WR_N	O	Ext. Write pulse						
80	D7	IOVDD	VDD	I/O power						
81	M6	GND	GND	GND						
82	N13	PE7	IO	GPIO E bit7	DCD	I	UART0 DCD	EXINT5	I	INT input 5
83	R13	BS0_N	O	Ext. Byte Select 0						
84	P12	BS1_N	O	Ext. Byte Select 1						
85	P13	PF0	IO	GPIO F bit0	SIN1	I	UART1 Rx	EXREQ1	I	DMA req. 0
86	R14	PF1	IO	GPIO F bit1	SOUT1	I	UART1 Tx	EXACK1	I	DMA ack. 0
87	P14	PF2	IO	GPIO F bit2	PENC	O	USB Host Power Control			
88	R15	PF3	IO	GPIO F bit3	OVC	I	USBHost Over Voltage signnal			
89	M13	XA2	O	Ext. Address 2						
90	P15	XA3	O	Ext. Address 3						
91	N15	XA4	O	Ext. Address 4						
92	N14	XA5	O	Ext. Address 5						
93	D9	IOVDD	VDD	I/O power						
94	M8	GND	GND	GND						
95	L15	DP	IO	USBdev D+						
96	K15	DM	IO	USBdev D−						
97	M14	PH1	IO	GPIO H bit1	SIM_CLK1	O	SIM1 Clock			
98	L14	PH2	IO	GPIO H bit2	SIM_RST1	O	SIM1 Reset			
99	L13	PG2	IO	GPIO G bit2	SIM_RST0	O	SIM0 Reset			
100	K14	XA17	O	Ext. Address 17						
101	K13	XA18	O	Ext. Address 18						

LIST OF PINS (FUNCTION LIST) (4/6)

Pin		Primary Function			Secondary Function			Tertiary Function		
QFP	BGA	Symbol	I/O	Description	Symbol	I/O	Description	Symbol	I/O	Description
102	M15	XA0	O	Ext. Address 0						
103	J13	XA1	O	Ext. Address 1						
104	J14	PH0	IO	GPIO H bit0	SIM_DATA1	IO	SIM1 Data			
105	H13	PG0	IO	GPIO G bit0	SIM_DATA0	IO	SIM0 Data			
106	J15	PG1	IO	GPIO G bit1	SIM_CLK0	O	SIM0 Clock			
107	H14	XA12	O	Ext. Address 12						
108	G14	XA13	O	Ext. Address 13						
109	M9	IOVDD	VDD	I/O Power						
110	D10	GND	GND	GND						
111	H15	SDCLK	O	Ext. SDRAM CLK						
112	G15	PG4	IO	GPIO G bit4	SIM_VCCL 00	O	SIM0 Voltage Control 0			
113	G13	PA7	IO	GPIO A bit7						
114	F15	PD2	IO	GPIO D bit2	SCK0	IO	SPI0 Clock			
115	E15	PD3	IO	GPIO D bit3	SSn0	IO	SPI0 Slave Select			
116	F13	PD6	IO	GPIO D bit6	SCK1	IO	SPI1 Clock	EXINT4	I	INT input 4
117	D15	PD7	IO	GPIO D bit7	SSn1	IO	SPI1 Slave Select	EXINT5	I	INT input 5
118	D8	COREVDD	VDD	CORE power						
119	G12	VBATVDD	VDD	BAT power						
120	F14	SDCS_N	O	Ext. SDRAM Chip Select						
121	E13	SDRAS_N	O	Ext. SDRAM RAS						
122	D14	SDCAS_N	O	Ext. SDRAM CAS						
123	C15	SDCKE	O	Ext. SDRAM CKE						
124	E14	RD_N	O	Ext. Read Enable						
125	D13	PH6	IO	GPIO H bit6	SIM_ CRDDET1	I	SIM1 Card Detect			
126	M10	IOVDD	VDD	I/O power						
127	D11	GND	GND	GND						
128	C13	PE6	IO	GPIO E bit6	RI	I	UART0 RI	EXINT4	I	INT input 4
129	C14	PF4	IO	GPIO F bit4	PUCTL	O	USBdevice Pull-up Control			
130	B15	PF5	IO	GPIO F bit5	EXINT6	I	INT input 6 for USBdevice VBUS			

LIST OF PINS (FUNCTION LIST) (5/6)

Pin		Primary Function			Secondary Function			Tertiary Function		
QFP	BGA	Symbol	I/O	Description	Symbol	I/O	Description	Symbol	I/O	Description
131	B14	XA6	O	Ext. Address 6						
132	A15	XA7	O	Ext. Address 7						
133	B13	XA8	O	Ext. Address 8						
134	A14	PD4	IO	GPIO D bit4	MISO1	IO	SPI1 MISO			
135	C12	PD5	IO	GPIO D bit5	MOSI1	IO	SPI1 MOSI			
136	A13	XA9	O	Ext. Address 9						
137	B12	XA10	O	Ext. Address 10						
138	A12	XA11	O	Ext. Address 11						
139	A11	PE4	IO	GPIO E bit4	DSR	I	UART0 DSR	EXINT2	I	INT input 2
140	B11	PE5	IO	GPIO E bit5	DTR	O	UART0 DTR	EXINT3	I	INT input 3
141	D12	IOVDD	VDD	I/O power						
142	M11	GND	GND	GND						
143	C11	XA14	O	Ext. Address 14						
144	B10	XA15	O	Ext. Address 15						
145	A10	XA16	O	Ext. Address 16						
146	C10	PG3	IO	GPIO G bit3	SIM_ VCCCNT0	O	SIM0 Power Control			
147	C9	PH5	IO	GPIO H bit5	SIM_ VCCL11	O	SIM1 Voltage Control1			
148	B9	XA19	O	Ext. Address 19						
149	B8	XA20	O	Ext. Address 20						
150	A9	XA21	O	Ext. Address 21						
151	F12	IOVDD	VDD	I/O power						
152	E12	GND	GND	GND						
153	H12	COREVDD	VDD	CORE power						
154	A8	XA22	O	Ext. Address 22						
155	C8	XA23	O	Ext. Address 23						
156	A7	XD0	IO	Ext. Data 0						
157	C7	XD1	IO	Ext. Data 1						
158	A6	XD2	IO	Ext. Data 2						
159	B7	XD3	IO	Ext. Data 3						
160	K12	IOVDD	VDD	I/O power						
161	J12	GND	GND	GND						

LIST OF PINS (FUNCTION LIST) (6/6)

Pin		Primary Function			Secondary Function			Tertiary Function		
QFP	BGA	Symbol	I/O	Description	Symbol	I/O	Description	Symbol	I/O	Description
162	A5	XD4	IO	Ext. Data 4						
163	C6	XD5	IO	Ext. Data 5						
164	B6	XD6	IO	Ext. Data 6						
165	B4	XD7	IO	Ext. Data 7						
166	C4	XD8	IO	Ext. Data 8						
167	B5	XD9	IO	Ext. Data 9						
168	M12	IOVDD	VDD	I/O power						
169	L12	GND	GND	GND						
170	A4	PH3	IO	GPIO H bit3	SIM_ VCCCNT1	O	SIM1 Power Control			
171	A3	XD10	IO	Ext. Data 10						
172	B3	XD11	IO	Ext. Data 11						
173	A2	XD12	IO	Ext. Data 12						
174	C3	XD13	IO	Ext. Data 13						
175	B2	XD14	IO	Ext. Data 14						
176	A1	XD15	IO	Ext. Data 15						

LIST OF PINS (PROPERTY LIST) (1/4)

QFP	BGA	Symbol	Internal Pull-up/Pull-down	Shmitt Trigger (Hysteresis)	Buffer type [mA]	5V tolerant
1	D4	IOVDD	–	–	–	–
2	B1	SYSCLK_P	–	–	–	–
3	C1	SYSCLK_N	–	–	–	–
4	E4	GND	–	–	–	–
5	D2	TCK	Internal Pull-up	○	2	–
6	D3	TDI	Internal Pull-up	–	2	–
7	D1	TDO	–	–	2	–
8	C2	TMS	Internal Pull-up	–	2	–
9	F4	COREVDD	–	–	–	–
10	E1	PB6	–	○	4	○
11	E3	TEST1	–	○	–	–
12	F2	TEST2	–	○	–	–
13	G4	IOVDD	–	–	–	–
14	F1	RTCCLK_P	–	–	–	–
15	G1	RTCCLK_N	–	–	–	–
16	H4	GND	–	–	–	–
17	F3	RESET_N	–	○	–	–
18	G2	NTRST	Internal Pull-up	○	2	–
19	H1	PH7	–	–	4	–
20	E2	PB4	–	○	4	○
21	J1	PB5	–	○	4	○
22	G3	PB0	–	○	4	–
23	K1	PB1	–	–	4	–
24	H3	PB2	–	○	4	–
25	J2	AVDD	–	–	–	–
26	H2	AGND	–	–	–	–
27	L1	AIN0	–	–	–	–
28	J3	AIN1	–	–	–	–
29	K2	AIN2	–	–	–	–
30	L3	AIN3	–	–	–	–
31	M1	AIN4	–	–	–	–
32	K3	AIN5	–	–	–	–
33	M2	AIN6	–	–	–	–
34	N1	AIN7	–	–	–	–
35	M3	PB7	–	○	4	○
36	L2	PC0	–	–	4	–
37	K4	IOVDD	–	–	–	–
38	J4	GND	–	–	–	–
39	N2	PC1	–	–	4	–
40	P1	PC2	–	–	4	–
41	P2	PC3	–	–	4	–
42	N3	PH4	–	–	4	–
43	L4	COREVDD	–	–	–	–
44	M4	VBATVDD	–	–	–	–
45	R1	CORERESET_N	–	○	–	–
46	P3	PWRSTART	–	–	4	–
47	R2	RESUME	–	○	–	–
48	R3	PB3	–	○	4	–

LIST OF PINS (PROPERTY LIST) (2/4)

QFP	BGA	Symbol	Internal Pull-up/Pull-down	Shmitt Trigger (Hysteresis)	Buffer type [mA]	5V tolerant
49	N4	PG7	–	–	4	–
50	R4	PC4	–	–	4	–
51	N5	PC5	–	–	4	–
52	P5	PD0	–	–	4	–
53	N6	PD1	–	–	4	–
54	D5	IOVDD	–	–	–	–
55	C5	GND	–	–	–	–
56	R6	HP	–	–	–	–
57	R7	HM	–	–	–	–
58	P6	PA5	–	–	4	–
59	N7	PC6	–	–	4	–
60	P4	PC7	–	–	4	–
61	M7	COREVDD	–	–	–	–
62	R5	PA6	–	○	4	–
63	M5	IOVDD	–	–	–	–
64	P7	PLLVDD1	–	–	–	–
65	N8	PLLGND1	–	–	–	–
66	D6	GND	–	–	–	–
67	R8	PG5	–	–	4	–
68	P8	PG6	–	–	4	–
69	R9	IOCS0_N	–	–	6	–
70	P10	PLLVDD2	–	–	–	–
71	P9	PLLGND2	–	–	–	–
72	N9	IOCS1_N	–	–	6	–
73	R10	ROMCS_N	–	–	6	–
74	N10	RAMCS_N	–	–	6	–
75	P11	PE0	–	○	4	–
76	R11	PE1	–	–	4	–
77	N11	PE2	–	○	4	–
78	N12	PE3	–	○	4	–
79	R12	WR_N	–	–	6	–
80	D7	IOVDD	–	–	–	–
81	M6	GND	–	–	–	–
82	N13	PE7	–	○	4	–
83	R13	BS0_N	–	–	6	–
84	P12	BS1_N	–	–	6	–
85	P13	PF0	–	○	4	–
86	R14	PF1	–	–	4	–
87	P14	PF2	–	–	4	–
88	R15	PF3	–	–	4	–
89	M13	XA2	–	–	6	–
90	P15	XA3	–	–	6	–
91	N15	XA4	–	–	6	–
92	N14	XA5	–	–	6	–
93	D9	IOVDD	–	–	–	–
94	M8	GND	–	–	–	–
95	L15	DP	–	–	–	–

LIST OF PINS (PROPERTY LIST) (3/4)

QFP	BGA	Symbol	Internal Pull-up/Pull-down	Shmitt Trigger (Hysteresis)	Buffer type [mA]	5V tolerant
96	K15	DM	–	–	–	–
97	M14	PH1	–	–	4	–
98	L14	PH2	–	–	4	–
99	L13	PG2	–	–	4	–
100	K14	XA17	–	–	6	–
101	K13	XA18	–	–	6	–
102	M15	XA0	–	–	6	–
103	J13	XA1	–	–	6	–
104	J14	PH0	–	–	4	–
105	H13	PG0	–	–	4	–
106	J15	PG1	–	–	4	–
107	H14	XA12	–	–	6	–
108	G14	XA13	–	–	6	–
109	M9	IOVDD	–	–	–	–
110	D10	GND	–	–	–	–
111	H15	SDCLK	–	–	6	–
112	G15	PG4	–	–	4	–
113	G13	PA7	–	○	4	–
114	F15	PD2	–	○	4	–
115	E15	PD3	–	○	4	–
116	F13	PD6	–	○	4	–
117	D15	PD7	–	○	4	–
118	D8	COREVDD	–	–	–	–
119	G12	VBATVDD	–	–	–	–
120	F14	SDCS_N	–	–	6	–
121	E13	SDRAS_N	–	–	6	–
122	D14	SDCAS_N	–	–	6	–
123	C15	SDCKE	–	–	6	–
124	E14	RD_N	–	–	6	–
125	D13	PH6	–	–	4	–
126	M10	IOVDD	–	–	–	–
127	D11	GND	–	–	–	–
128	C13	PE6	–	○	4	–
129	C14	PF4	–	–	4	–
130	B15	PF5	–	○	4	○
131	B14	XA6	–	–	6	–
132	A15	XA7	–	–	6	–
133	B13	XA8	–	–	6	–
134	A14	PD4	–	–	4	–
135	C12	PD5	–	–	4	–
136	A13	XA9	–	–	6	–
137	B12	XA10	–	–	6	–
138	A12	XA11	–	–	6	–
139	A11	PE4	–	○	4	–
140	B11	PE5	–	○	4	–
141	D12	IOVDD	–	–	–	–
142	M11	GND	–	–	–	–
143	C11	XA14	–	–	6	–

LIST OF PINS (PROPERTY LIST) (4/4)

QFP	BGA	Symbol	Internal Pull-up/Pull-down	Shmitt Trigger (Hysteresis)	Buffer type [mA]	5V tolerant
144	B10	XA15	–	–	6	–
145	A10	XA16	–	–	6	–
146	C10	PG3	–	–	4	–
147	C9	PH5	–	–	4	–
148	B9	XA19	–	–	6	–
149	B8	XA20	–	–	6	–
150	A9	XA21	–	–	6	–
151	F12	IOVDD	–	–	–	–
152	E12	GND	–	–	–	–
153	H12	COREVDD	–	–	–	–
154	A8	XA22	–	–	6	–
155	C8	XA23	–	–	6	–
156	A7	XD0	Internal Pull-down	–	6	–
157	C7	XD1	Internal Pull-down	–	6	–
158	A6	XD2	Internal Pull-down	–	6	–
159	B7	XD3	Internal Pull-down	–	6	–
160	K12	IOVDD	–	–	–	–
161	J12	GND	–	–	–	–
162	A5	XD4	Internal Pull-down	–	6	–
163	C6	XD5	Internal Pull-down	–	6	–
164	B6	XD6	Internal Pull-down	–	6	–
165	B4	XD7	Internal Pull-down	–	6	–
166	C4	XD8	Internal Pull-down	–	6	–
167	B5	XD9	Internal Pull-down	–	6	–
168	M12	IOVDD	–	–	–	–
169	L12	GND	–	–	4	–
170	A4	PH3	–	–	–	–
171	A3	XD10	Internal Pull-down	–	6	–
172	B3	XD11	Internal Pull-down	–	6	–
173	A2	XD12	Internal Pull-down	–	6	–
174	C3	XD13	Internal Pull-down	–	6	–
175	B2	XD14	Internal Pull-down	–	6	–
176	A1	XD15	Internal Pull-down	–	6	–

PIN DISCRIPTION (CLOCK, RESET, DEBUG SIGNALS)

Pin name	Discript in FUNCTION LIST	IO	Discript in detail (Inside the parentheses the QFP pin number is shown)	Primary/ Secondary/ Tertiary	Logic
Clock/Reset					
RESET_N	Reset input	I	Reset input Do not assert after resume from stand-by mode. (17)	Primary	Negative
CORERESET_N	CORE reset	I	Core reset input Assert after resume from stand-by mode. (45)	Primary	Negative
PWRSTART	Regulator control	O	Regulator(VDDCORE) enable output. Negate after stand-by mode. (46)	Primary	Positive
RESUME	Resume from Stand-by	I	Resume request Input for return from standby. (47)	Primary	Positive/ Negative
SYSCLK_P	Osclation (Main)	I	Crystal connection or external clock input. Connect a crystal(8MHz, 16MHz), if used, to SYSCLK_P and SYSCLK_N. It is also possible to input a direct clock (8MHz, 16MHz). (2)	Primary	-
SYSCLK_N		O	Crystal connection. When not using a crystal, leave this pin unconnected. (3)	Primary	-
RTCCLK_P	Osclation (RTC)	I	Crystal connection or external clock input. Connect a crystal(32.768KHz), if used, to RTCCLK_P and RTCCLK_N. It is also possible to input a direct clock(32.768KHz). (14)	Primary	-
RTCCLK_N		O	Crystal connection. When not using a crystal, leave this pin unconnected. (15)	Primary	-
Debugging support (JTAG)					
TCK	JTAG TCK	I	Debugging pin. Normally connect to ground level. (5)	Primary	Positive
TDI	JTAG TDI	I	Debugging pin. Normally drive at High level. (6)	Primary	Positive
TDO	JTAG TDO	O	Debugging pin. Normally leave open. (7)	Primary	Positive
TMS	JTAG TMS	I	Debugging pin. Normally drive at High level. (8)	Primary	Positive
NTRST	JTAG Reset input	I	Debugging pin. Normally connect to ground level. (18)	Primary	Negative

PIN DISCRIPTION (GENERAL I/O SIGNALS)

Pin name	Discript in FUNCTION LIST	IO	Discript in detail (Inside the parentheses the QFP pin number is shown)	Primary/ Secondary/ Tertiary	Logic
General-purpose I/O ports (PA～PH) Total 62bits					
PA[7:0]	GPIO A	IO	General Purpose I/O port A (PA[7:5] are primary, PA[4:0] are secondary) (5, 6, 7, 8, 18, 58, 62, 113)	Primary/ Secondary	Positive
PB[7:0]	GPIO B	IO	General Purpose I/O port B (10, 20, 21, 22, 23, 24, 35, 48)	Primary	Positive
PC[7:0]	GPIO C	IO	General Purpose I/O port C (36, 39, 40, 41, 50, 51, 59, 60)	Primary	Positive
PD[7:0]	GPIO D	IO	General Purpose I/O port D (52, 53, 114, 115, 116, 117, 134, 135)	Primary	Positive
PE[7:0]	GPIO E	IO	General Purpose I/O port E (75, 76, 77, 78, 82, 128, 139, 140)	Primary	Positive
PF[5:0]	GPIO F	IO	General Purpose I/O port F (85, 86, 87, 88, 129, 130)	Primary	Positive
PG[7:0]	GPIO G	IO	General Purpose I/O port G (49, 67, 68, 99, 105, 106, 112, 146)	Primary	Positive
PH[7:0]	GPIO H	IO	General Purpose I/O port H (19, 42, 97, 98, 104, 125, 147, 170)	Primary	Positive

PIN DISCRIPTION (EXTERNAL BUS SIGNALS)

Pin name	Discript in FUNCTION LIST	IO	Discript in detail (Inside the parentheses the QFP pin number is shown)	Primary/ Secondary/ Tertiary	Logic
External Bus and control signals (for ROM, SRAM, SDRAM, I/O)					
XA[23:0]	Ext. Address	O	Address bus to external RAM, external ROM, external I/O banks and external SDRAM. (89, 90, 91, 92, 100, 101, 102, 103, 107, 108, 131, 132, 133, 136, 137, 138, 143, 144, 145, 148, 149, 150, 154, 155)	Primary	Positive
XD[15:0]	Ext. Data	IO	Data bus to external RAM, external ROM, external I/O banks and external SDRAM. (156, 157, 158, 159, 162, 163, 164, 165, 166,167, 171, 172, 173, 174, 175, 176)	Primary	Positive
ROMCS_N	Ext. ROM Chip Select	O	ROM bank chip enable. (73)	Primary	Negative /
RAMCS_N	Ext. RAM Chip Select	O	SRAM bank chip enable. (74)	Primary	Negative
IOCS0_N	Ext. I/O 0 Chip Select	O	I/O chip enable 0. (69)	Primary	Negative
IOCS1_N	Ext. I/O 1 Chip Select	O	I/O chip enable 1. (72)	Primary	Negative
SDCS_N	Ext. SDRAM Chip Select	O	SDRAM chip enable. (120)	Primary	Negative
RD_N	Ext. Read Enable	O	Read enable/Output enable (124)	Primary	Negative
WR_N	Ext. Write pulse	O	Write pulse/Write enable (79)	Primary	Negative
BS0_N BS1_N	Ext. Byte Select	O	Byte select BS1_N is for MSB, BS0_N is for LSB. (83, 84)	Primary	Negative
SDCLK	Ext. SDRAM CLK	O	SDRAM clock (Same as operating frequency, Max. 64MHz) (111)	Primary	-
SDRAS_N	Ext. SDRAM RAS	O	Raw address strobe for SDRAM (121)	Primary	Negative
SDCAS_N	Ext. SDRAM CAS	O	Column address strobe for SDRAM (122)	Primary	Negative
SDCKE	Ext. SDRAM CKE	O	Clock enable for SDRAM (123)	Primary	-

PIN DISCRIPTION (REQUEST (DMA/INTERRUPT) SIGNALS)

Pin name	Discript in FUNCTION LIST	IO	Discript in detail (Inside the parentheses the QFP pin number is shown)	Primary/ Secondary/ Tertiary	Logic
Interrupt request signals					
EXINT0	INT input 0	I	External interrupt 0 input signal. (24, 77)	Tertiary	Positive/ Negative
EXINT1	INT input 1	I	External interrupt 1 input signal. (48, 78)	Tertiary	Positive/ Negative
EXINT2	INT input 2	I	External interrupt 2 input signal. (10, 139)	Tertiary	Positive/ Negative
EXINT3	INT input 3	I	External interrupt 3 input signal. (35, 140)	Tertiary	Positive/ Negative
EXINT4	INT input 4	I	External interrupt 4 input signal. (116, 128)	Tertiary	Positive/ Negative
EXINT5	INT input 5	I	External interrupt 5 input signal. (82, 117)	Tertiary	Positive/ Negative
EXINT6	INT input 6 for USBdevice VBUS	I	External interrupt 6 input signal (for USB device VBUS). (130)	Secondary	Positive/ Negative
DMA control signals					
EXREQ0	DMA req. 0	I	Ch 0 DMA request signal, used when DMA controller configured for DREQ type (22)	Tertiary	Positive
EXACK0	DMA ack. 0	O	Ch 0 DREQ signal clear request. The DMA device responds to this output by negating DREQ. (23)	Tertiary	Positive
EXREQ1	DMA req. 1	I	Ch 1 DMA request signal, used when DMA controller configured for DREQ type (85)	Tertiary	Positive
EXACK1	DMA ack. 1	O	Ch 1 DREQ signal clear request. The DMA device responds to this output by negating DREQ. (86)	Tertiary	Positive

PIN DISCRIPTION (SERIAL INTERFACE (UART/SIO/I2C) SIGNALS)

Pin name	Discript in FUNCTION LIST	IO	Discript in detail (Inside the parentheses the QFP pin number is shown)	Primary/ Secondary/ Tertiary	Logic
UARTsignals (2ch installed : ch0, ch1) ch0 : The combination of SIN0, SOUT0, CTS, DSR, DCD, DTR, RTS, RI. ch1 : The combination of SIN1, SOUT1.					
SIN0 SIN1	UART Rx	I	SIO receive signal (SIN0:75, SIN1:85)	Secondary	Positive
SOUT0 SOUT1	UART Tx	O	SIO transmit signal (SOUT0:76, SOUT1:86)	Secondary	Positive
CTS	UART CTS	I	Clear To Send (77) Indicates that modem or data set is ready to transfer data. Bit 4 in modem status register reflects this input.	Secondary	Negative
DSR	UART DSR	I	Data Set Ready (139) Indicates that modem or data set is ready to establish a communication link with UART. Bit5 in modem status register refrects this input.	Secondary	Negative
DCD	UART DCD	I	Data Carrier Detect (82) Indicates that modem or data set has detected data carrier signal. Bit7 in modem status register reflects this input.	Secondary	Negative
DTR	UART DTR	O	Data Terminal Ready (140) Indicates that UART is ready to establish a communicationslink with modem or data set. Bit0 in modem control register controls this output.	Secondary	Negative
RTS	UART RTS	O	Request To Send (78) Indicates that UART is ready to transfer data to modem or data set. Bit1 in modem control register controls this output	Secondary	Negative
RI	UART RI	I	Ring Indicator (128))) Indicates that modem or data set has received telephone ring indicator. Bit6 in modem status register refrects this input.	Secondary	Negative
SIO signals					
uSIN	SIO Rx	I	SIO receive signal (49)	Tertiary	Positive
uSOUT	SIO Tx	O	SIO transmit signal (19)	Tertiary	Positive
I2C signals (2ch installed : ch0, ch1) ch0 : The combination of SDA0, SCL0. ch1 : The combination of SDA1, SCL1.					
SDA0 SDA1	I2C Data	IO	I2C Data. This pin operates as NMOS Open drain. Connect pull-up resistor. (SDA0:20, SDA1:10)	Secondary	Positive
SCL0 SCL1	I2C Clock	IO	I2C Clock. This pin operates as NMOS Open drain. Connect pull-up resistor. (SCL0:21, SCL1:35)	Secondary	-

PIN DISCRIPTION (SERIAL INTERFACE (SPI/USB/SIM) SIGNALS)

Pin name	Discript in FUNCTION LIST	IO	Discript in detail (Inside the parentheses the QFP pin number is shown)	Primary/ Secondary/ Tertiary	Logic
SPI signals (2ch installed : ch0, ch1) ch0 : The combination of MISO0, MSOI0, SCLK0, SSn0. ch1 : The combination of MISO1, MSOI1, SCLK1, SSn1.					
MISO0 MISO1	SPI MISO	IO	Master serial input/slave serial output signals (MISO0:52, MISO1:134)	Secondary	Positive
MOSI0 MOSI1	SPI MOSI	IO	Master serial output/slave serial input signals (MOSI0:53, MOSI1:135)	Secondary	Positive
SCK0 SCK1	SPI Clock	IO	Baud rate clocks (SCK0:114, SCK1:116)	Secondary	-
SSn0 SSn1	SPI Slave Select	IO	Slave select signals (SSn0:115, SSn1:117)	Secondary	Negative
USB signals					
HP	USB Host D+	IO	USB host interface I/O pin D+. (56))	Primary	-
HM	USB Host D−	IO	USB host interface I/O pin D-. (57)	Primary	-
PENC	USB Host Power Control	O	Output pin for USB host interface power supply control (ON/OFF). ‘L’ : ON, ‘H’ : OFF (87)	Secondary	Negative
OVC	USB Host Over Voltage Signal	I	Input pin for notifying a USB host interface power supply abnormality (overcurrent, etc.). "L": Abnormal, "H": Normal (88)	Secondary	Negative
DP	USB Dev D+	IO	USB device interface I/O pin D+. (95)	Secondary	-
DM	USB Dev D−	IO	USB device interface I/O pin D- (96)	Secondary	-
PUCTL	USB Dev Pull−up Control	O	USB device interface Pull-up Pull-down control signal (129)	Secondary	-
Smart card interface (SIM) signals (2ch installed : ch0, ch1) ch0 : The combination of SIM_DATA0, SIM_CLK0, SIM_RST0, SIM_VCCL00, SIM_VCCL01, SIM_VCCCNT0, SIM_CRDDET0. ch1 : The combination of SIM_DATA1, SIM_CLK1, SIM_RST1, SIM_VCCL10, SIM_VCCL11, SIM_VCCCNT1, SIM_CRDDET1.					
SIM_DATA0 SIM_DATA1	SIM Data	IO	SIM Serial data. 【SIM_DATA0:105, SIM_DATA1:104)	Secondary	Positive
SIM_CLK0 SIM_CLK1	SIM Clock	O	SIM Clock. (SIM_CLK0:106, SIM_CLK1:97)	Secondary	-
SIM_RST0 SIM_RST1	SIM Reset	O	SIM Reset. (SIM_RST0:99, SIM_RST1:98)	Secondary	Negative
SIM_VCCL00 SIM_VCCL10	SIM Voltage Control 0	O	SIM Power supply voltage control 0. (SIM_VCCL00:112, SIM_VCCL10:42)	Secondary	Positive
SIM_VCCL01 SIM_VCCL11	SIM Voltage Control 1	O	SIM Power supply voltage control 1. (SIM_VCCL01:67, SIM_VCCL11:147)	Secondary	Positive
SIM_VCCCNT0 SIM_VCCCNT1	SIM Power Control	O	SIM External power supply regulator control. (SIM_VCCCNT0:146, SIM_VCCCNT1:170)	Secondary	Positive
SIM_CRDDET0 SIM_CRDDET1	SIM Card Detect	I	SIM Card detection (H=Detected / L=Empty). (SIM_CRDDET0:68, SIM_CRDDET1:125)	Secondary	Positive

PIN DISCRIPTION (TIMER, LCD CONTROL, AD CONVERTER SIGNALS)

Pin name	Discript in FUNCTION LIST	IO	Discript in detail (Inside the parentheses the QFP pin number is shown)	Primary/ Secondary/ Tertiary	Logic
Timer signals					
TIMER0 TIMER1	Timer	IO	Flexible timer 0/1 input output signals. Capture input, compare output, and timer clock input are available. (TIMER0:22, TIMER1:23)	Secondary	Positive
TIMER2 TIMER3 TIMER4 TIMER5	Timer	IO	Flexible timer 2/3/4 input output signals. Capture input, compare output are available. (TIMER2:24, TIMER3:48, TIMER4:49, TIMER5:19)	Secondary	Positive
LCD Control signals					
DD[3:0]	LCD Data	O	LCD Display data output. (41, 40, 39, 36)	Secondary	Positive
CPO	LCD Pannel Clock Output	O	LCD Pannel clock output. (50)	Secondary	Positive
LP	LCD Line Synchronous Pulse	O	LCD Line Synchronous Pulse. (51)	Secondary	Positive
FLM	LCD Frame Synchronous Pulse	O	LCD Frame Synchronous Pulse. (59)	Secondary	Positive
DATAENB	LCD Data Enable	O	LCD Data Enable signal. This signal is asserted during available data output. (58)	Secondary	Positive
DF	LCD DF Conversiton	O	LCD signal convert switch. Switch signal to convert LCD drive waveform into AC (60)	Secondary	Positive
CPI	LCD Pannel Clock Input	I	LCD Pannel clock intput. (62)	Secondary	-
Analog to Digital Converter signals					
AIN0 AIN1 AIN2 AIN3 AIN4 AIN5 AIN6 AIN7	Analog in	I	Analog input for analog to digital converter (AIN0:27, AIN1:28, AIN2:29, AIN3:30 AIN4:31, AIN5:32, AIN6:33, AIN7:34)	Primary	–

PIN DISCRIPTION (MODE SIGNALS AND POWERS)

Pin name	Discript in FUNCTION LIST	IO	Discript in detail (Inside the parentheses the QFP pin number is shown)	Primary/ Secondary/ Tertiary	Logic
Mode configuration signals					
TEST1	Test mode	I	Test mode. Normally connect to ground level. (11)	Primary	Positive
TEST2	Test mode	I	Test mode. Normally connect to ground level. (12)	Primary	Positive
Power supplies					
COREVDD	Core power		Core power supply. (9, 43, 61, 118, 153)		
IOVDD	I/O power		I/O power supply. (1, 13, 37, 54, 63, 80, 93, 109, 126, 141, 151, 160, 168)		
VBATVDD	BAT power		VBAT (Battery Backup) power supply. (44, 119)		
AVDD	AD Converter power		Analog to digital converter power supply. (25)		
PLLVDD1 PLLVDD2	PLL power		PLL power supply. (PLLVDD1:64, PLLVDD2:70)		
GND	GND		GND for core and I/O. (4, 16, 38, 55, 66, 81, 94, 110, 127, 142, 152, 161, 169)		
AGND	AD Converter GND		GND for Analog to digiatal converter. (26)		
PLLGND1 PLLGND2	PLL GND		GND for PLL. (PLLGND1:65, PLLGND2:71)		

DISCRIPT OF FUNCTIONS (1/5)

CPU
- 32-bit RISC CPU (ARM7TDMI)
- Built-in 8-Kbyte unified cache
- Little-endian format
- Maximum operating frequency of 64 MHz
- Instruction structure: Enables mixed execution of high-density 32-bit long instructions and the subset of them, i.e., 16-bit long instructions of high object efficiency.
- General-purpose registers: 32 bits x 31 registers
- Built-in barrel shifter (operations of ALU and barrel shift can be executed by a single instruction)
- Built-in debug function (JTAG interface)

Internal memory
- 16-Kbyte RAM: AHB connection
- 2-Kbyte battery backup RAM: AHB connection

External memory controller
- Setting of programmable access timing for each space
- ROM (FLASH) access function
  Supports 1-bank x 16-Mbyte ROM space
  Supports 16-bit devices only
  Supports flash memories
  Supports page access
- SRAM access function
  1-bank x 16-Mbyte SRAM space
  Supports 8- and 16-bit devices
  Supports asynchronous SRAMs
- External I/O access function
  2-bank I/O space
  Supports 8- and 16-bit devices
  OE/WE pulse and data OFF timing can be set
- SDRAM access function
  Maximum SDRAM capacity: 64 Mbytes (16-bit configuration)
  Supports 16-bit devices
  Supports CBR auto-refresh and self-refresh
  Operates at the same clock as a 64 MHz CPU

Interrupt controller
- LSI internal interrupt : 38 sources
- LSI external interrupt: 7 sources (with 1 source being FIQ)
- Seven levels of interrupt priorities can be set for each interrupt source.

DISCRIPT OF FUNCTIONS (2/5)

DMA controller
- 6ch (dual configuration of 4ch + 2ch)
- A DMA transfer request source can be assigned for each channel.
- Fixed mode or round robin mode can be selected for the priority order of channels.
- Cycle still mode or burst mode can be selected as the bus right request method.
- Two types of DMA transfer requests are supported: software request and external request.
- Maximum number of transfers: 65,536 transfers
- Data transfer size: 8/16/32 bits
- Transfer request source: I2C, UART, SPI, SIM card interface, USB 2.0 FS/LS host, modulo calculation accelerator

Modulo calculation accelerator
- Installed hardware that supports multi-bit length (512,768,1024 bits)
- Can be extended to support more than 1024 bits by software
- Modulo multiply calculation: Within 12 ms (at 1024-bit, 64 MHz operation)
  Modulo exponential calculation: Within 20 ms (at 1024-bit, 64 MHz operation)
  Modulo exponential calculation: Within 80 ms (at 2048-bit, 64 MHz operation)
- Supports DMAC

Random number generator
- Built-in 8-bit random number generator

LCD controller
- 320 x 240 pixels maximum
- Monochrome STN (with 2 levels of grayscale: 1bpp)
- Built-in VRAM (10 Kbytes for 1 frame)

Smart card interface
- Built-in 2-channel ISO UART
- Built-in 48-byte FIFO on each channel
- Provided with an internal parity error counter for receive mode and transmit mode in automatic retransmission
- Supports asynchronous protocols T=0 and T=1 that conform to ISO7816
- Built-in hardware functions: error detection code generation and error detection
- Supports DMAC

Watchdog timer
- Built-in 16-bit timer
- Maximum overflow time is 8.3875 seconds (when operating at 32 MHz APB clock)
- Watchdog timer mode provided
- Interrupts or resets are generated according to settings.
- Starting/stopping a watchdog timer
- Clearing a watchdog occurrence factor
- The watchdog timer cycle can be changed during watchdog timer operation.

DISCRIPT OF FUNCTIONS (3/5)

A/D converter
- 12-bit sequential conversion type x 8ch
- Sample hold function
- Conversion time: 25 ms (400ksample/s max.)
- Enables sequential A/D conversion (one-time/continuous) from the minimum channel to the maximum channel selected arbitrarily.

USB 2.0 FS/LS host
- Compliant with Universal Serial Bus (USB) 2.0 and OpenHCI (Open Host Controller Interface) 1.0a
- Supports four types of data transfer: Control transfer, bulk transfer, interrupt transfer, and isochronous transfer
- Built-in 4-Kbyte RAM
- Supports DMA transfer and PIO transfer
  Number of channels: 1
  DMA transfer mode: Single transfer mode, burst transfer mode
- Supports one USB port (Full-speed (12 Mbps) and Low-speed (1.5 Mbps) supported)
- Supports SOF and CRC5/16 generation function
- Enables 32-/16-/8-bit access to data transfer FIFO (Fixed to 32-bit access in the case of DMA transfer)

USB 2.0 FS device
- Compliant with Universal Serial Bus (USB) 2.0
- Supports four types of data transfer: Control transfer, bulk transfer, interrupt transfer, and isochronous transfer
- Supports one USB port (Full-speed (12 Mbps) supported)
- Supports five or six endpoints
- Supports SOF generation and CRC5/16 generation function
- Enables 32-/16-/8-bit access to data transfer FIFO

I2C bus controller
- Philips I2C bus specification Ver 2.1 compliant controller ´ 2ch
- Supports multi-master mode.
- Data transfer modes
  Standard mode (100 kHz)
  Fast mode (400 kHz)
- 7-bit/10-bit address compatible
- Clocks are stopped to synchronize data between master and slave.
- Supports DMA transfer.

DISCRIPT OF FUNCTIONS (4/5)

System timer
- 16-bit auto-reload timer: ´ 1ch

Flexible timer
- 16-bit timer x 6ch
- Operation mode
  Operable in each of the modes, Auto Reload Timer (ART)/Compare Out (CMO)/
  Pulse Width Modulation (PWM)/Capture (CAP)
  Timer 0 and 1 also support external timer clock inputs

RTC
- Generates 1 second from external 32.768 kHz
- Support Year/Month/Date/Hour/Minute/Second/Day of the week
- 30 seconds correct by software
- Interrupt in cycles for alarm
- Start/Stop function for measuring time
- 24 hours/12 hours format are selectable
- Automatic correcting the Leap-years equation
- Built-in 100-year counter

GPIO
- Built-in GPIO of a total of 62 bits
- Input or output can be specified for each bit. Every bit can be configured as interrupt input.
- Interrupt function (level/edge and positive logic/negative logic can be set, and this function is also supported even when no clock is operating.)

SIO
- Full-duplex start-stop synchronization method
- Built-in baud rate generator
- Maximum buad rate 0.5 Mbps

UART
- Two channels of serial communication function with FIFO
- Serial communication with 16-byte FIFO
- Flow control by hardware (one channel only)
- Supports DMA transfer.
- 921.6 kbps max.

SPI
- Built-in two channel of full duplex serial peripheral interface
- The master or slave mode can be selected.
- Built-in 16-byte or 16-word (16-bit) FIFO on the transmitting side and receiving side
- 8 bits (byte) or 16 bits (word) can be selected as the transfer size.
- Supports DMA transfer.
- Built-in baud rate generator
- 16 Mbps max. (APBCLK divided by 2)

DISCRIPT OF FUNCTIONS (5/5)

Clock
- Main clock oscillator (8/16 MHz)
- RTC clock oscillator (32.768 kHz for clocking function)

Boundary scan
- JTAG boundary scan test executable

Power management
- Power saving mode
  - · CPU halt mode: Stops only the CPU clock.
  - · STOP mode: Stops all the clocks of the chip except RTC.
  - · Standby mode: Turns power off, except for RTC and backup RAM

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Digital power supply (COREVDD) voltage (CORE)	V_{DDCORE}	—(*1)	–0.3 to +2.0	V
Digital power supply (IOVDD) voltage (I/O)	V_{DDIO}	—(*1)	–0.3 to +4.6	
Input voltage (normal buffer)	V_I	—(*1)	–0.3 to V_{DDIO}+0.3	
Output voltage (normal buffer)	V_O	—(*1)	–0.3 to V_{DDIO}+0.3	
PLL section power supply (PLLVDD) voltage	V_{DDPLL}	—(*1)	–0.3 to +2.0	
VBAT section power supply (VBATVDD) voltage	V_{BAT}	—(*1)	–0.3 to +2.0	
ADC analog power supply (AVDD) voltage	V_{DDA}	—(*1)	–0.3 to +4.6	
Analog input voltage	V_{AI}	—(*1)	–0.3 to V_{DDA}	
Allowable input current	I_I	—(*1)	–10 to +10	mA
Allowable output current (2mA buffer)	I_O	—(*1)	–8 to +8	
Allowable output current (4mA buffer)			–16 to +16	
Allowable output current (6mA buffer)			–24 to +24	
Power dissipation	P_D	Ta = 85°C 176pin LQFP package	1203	mW
		Ta = 85°C 176pin LFBGA package	670	
Storage temperature	T_{STG}	—	–50 to +150	°C

*1: GND = 0V, PLLGND = 0V, AGND = 0V, Ta = 25°C

Recommended Operating Conditions

(GND = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital power supply (COREVDD) voltage (CORE)	V_{DDCORE}	—	1.35	1.5	1.65	V
Digital power supply (IOVDD)voltage (I/O)	V_{DDIO}	—	2.7 (*1)	3.3	3.6	
PLL section power supply (PLLVDD) voltage	V_{DDPLL}	—	1.35	1.5	1.65	
VBAT section power supply (VBATVDD) voltage	V_{BAT}	—	1.35	1.5	1.65	
ADC analog power supply (AVDD) voltage	V_{DDA}	—	2.7	3.3	3.6	
CPU Operating frequency(*2)	f_{cpu}	—	0.032	—	64	MHz
Ambient temperature	Ta	—	–40	25	85	°C

*1: When using USB2.0 FS/LS host or USB2.0 FS device, use the minimum value of V_{DDIO} in more than 3.0V.

*2: The minimum value of the CPU operating frequency is specified for each function, as shown below.

I^2C : To operate I^2C, the CPU operating frequency must be 19.2 MHz or more if the I^2C bus speed is 100 kbps, and 25.6 MHz or more if 400 kbps.

ADC : To operate ADC, the CPU operating frequency must be 3.2 MHz or more.

SPI : To operate SPI, the CPU operating frequency must be four times more of the SPI serial clock frequency.

LCDC : To operate LCDC, the AHB_CLK frequency must be higher than CPI frequency.

ELECTRICAL CHARACTERISTICS (DC CHARACTERISTICS)

(1) Core Section and I/O Section (1/2)

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDIO} = 2.7 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH1}	Normal pins	2.0	—	V_{DDIO} + 0.3	V
	V_{IH2}	5 V tolerant pins	2.0	—	5.5	
"L" input voltage	V_{IL1}	Normal pins	–0.3	—	0.8	
	V_{IL2}	5 V tolerant pins	–0.3	—	0.8	
TTL Schmitt trigger input threshold voltage	$V_{t-,+}$ ΔV_t	V_{DDIO} = 2.7 to 3.0 V $V_{t+} - V_{t-}$	0.6 0.25	— —	2.4 —	
	$V_{t-,+}$ ΔV_t	V_{DDIO} = 3.0 to 3.6 V $V_{t+} - V_{t-}$	0.7 0.25	— —	2.4 —	
I^2C Schmitt trigger input threshold voltage	$V_{IICt-,+}$ ΔV_{IICt}	V_{DDIO} = 2.7 V $V_{t+} - V_{t-}$	0.81 0.135	— —	1.89 —	
	$V_{IICt-,+}$ ΔV_{IICt}	V_{DDIO} = 3.0 V $V_{t+} - V_{t-}$	0.9 0.15	— —	2.1 —	
	$V_{IICt-,+}$ ΔV_{IICt}	V_{DDIO} = 3.6 V $V_{t+} - V_{t-}$	1.08 0.18	— —	2.52 —	
"H" output voltage	V_{OH}	V_{DDIO} = 2.7 to 3.0 V Normal pins, 5 V tolerant pins	2.2(*1)	—	—	
		V_{DDIO} = 3.0 to 3.6 V Normal pins, 5 V tolerant pins	2.4(*1)	—	—	
"L" output voltage	V_{OL}	V_{DDIO} = 2.7 to 3.0 V Normal pins, 5 V tolerant pins	—	—	0.45(*2)	
		V_{DDIO} = 3.0 to 3.6 V Normal pins, 5 V tolerant pins	—	—	0.4(*2)	
"H" input current	I_{IH1}	$V_I = V_{DDIO}$ Normal pins	—	—	10	uA
	I_{IH2}	$V_I = V_{DDIO}$ to 5.5 V 5 V tolerant pins	—	—	10	
	I_{IH3}	$V_I = V_{DDIO}$ 50kΩ pull-down pins	10	—	200	
"L" input current	I_{IL1}	V_I = 0 V Normal pins	–10	—	—	
	I_{IL2}	V_I = 0 V 5 V tolerant pins	–10	—	—	
	I_{IL3}	V_I = V 50kΩ pull-up pins	–200	—	–10	

*1: Avoid using "H" output voltage in lower than this voltage value.
*2: Avoid using "L" output voltage in lower than this voltage value.

ELECTRICAL CHARACTERISTICS (DC CHARACTERISTICS)

(1) Core Section and I/O Section (2/2)

	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
current consumption (run mode)	I/O section	I_{DDOIO}	When a 30 pF external capacitor is connected (including the oscillator circuit)	—	50(*1)	—	mA
	ADC section	I_{DDOAD}		—	1(*1)	3(*2)	
	Core section	$I_{DDOCore}$		—	40(*1)	115(*2)	
	PLL1	$I_{DDOPLL1}$	PLL1: 128 MHz output	—	0.1(*1)	1(*2)	
	PLL2	$I_{DDOPLL2}$	PLL2: 192 MHz output	—	0.1(*1)	1(*2)	
	VBAT section	$I_{DDOVBAT}$		—	0.7(*1)	3(*2)	
current consumption (HALT mode)	I/O section	I_{DDOIO_H}	When a 30 pF external capacitor is connected	—	50(*1)	—	
	ADC section	I_{DDOAD_H}		—	1(*1)	3(*2)	
	Core section	$I_{DDOCore\_H}$		—	26(*1)	75(*2)	
	PLL1	$I_{DDOPLL1\_H}$	PLL1: 128 MHz output	—	0.1(*1)	1(*2)	
	PLL2	$I_{DDOPLL2\_H}$	PLL2: 192 MHz output	—	0.1(*1)	1(*2)	
	VBAT section	$I_{DDOVBAT\_H}$		—	0.7(*1)	3(*2)	
current consumption (STOP mode)	I/O section	I_{DDOIO}		—	1(*1)	10(*2)	uA
	ADC section	I_{DDOAD}		—	1(*1)	10(*2)	
	Core section	$I_{DDOCore}$		—	49(*1)	6900(*2)	
	PLL1	$I_{DDOPLL1}$		—	1(*1)	8.3(*2)	
	PLL2	$I_{DDOPLL2}$		—	1(*1)	8.3(*2)	
	VBAT section	$I_{DDOVBAT}$		—	3(*1)	490(*2)	
current consumption (standby mode)	I/O section	I_{DDOIO_ST}	V_{BAT} = 1.65 V, V_{DDIO} = 3.6 V Ta = 25 °C	—	—	1	
			V_{BAT} = 1.65 V, V_{DDIO} = 3.6 V Ta = 85 °C	—	—	10	
	VBAT section	$I_{DDOVBAT\_ST}$	V_{BAT} = 1.65 V, V_{DDIO} = 3.6 V Ta = 25 °C	—	3	30	
			V_{BAT} = 1.65 V, V_{DDIO} = 3.6 V Ta = 85 °C	—	—	490	

*1: V_{DDCORE}=V_{BAT}=V_{DDPLL1}=V_{DDPLL2}=1.50V, V_{DDIO}=V_{DDAD}=3.3V, Ta=25°C
*2: V_{DDCORE}=V_{BAT}=V_{DDPLL1}=V_{DDPLL2}=1.65V, V_{DDIO}=V_{DDAD}=3.6V, Ta=85°C

ELECTRICAL CHARACTERISTICS (DC CHARACTERISTICS)

(2) Analog to Digital Converter Characteristics

(V_{DDCORE} = 1.35 to 1.65 V, V_{DDA} = 2.7 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
operating clock frequency	f_{cin}	—	0.8	—	10.0	MHz
sampling clock frequency	f_{cs}	—	32	—	400	KHz
Resolution	n	—	—	—	12	bit
Differential linearity error	DNL	Analog input source impedance Ri ≤ 1 kΩ	—	±1.0	±4.0	LSB
Linearity error	INL		—	±1.0	±6.0	
Zero scale error	Ezs		—	±1.0	±8.0	
Full scale error	Efs		—	±1.0	±8.0	
Analog Input leakage current	I_{IA}	—	–1.0	0	1.0	uA
Conversion time	tconv	Analog input source impedance Ri ≤ 1 kΩ	2.5	—	31.25	uS
Throughput rate	f_{ath}		32	—	400	kHz

- Definition of Terms

(1) Resolution:
Minimum input analog value recognized. For 10-bit resolution, this is (VREF – Aground) ÷ 1024.

(2) Linearity error:
Difference between the theoretical and actual conversion characteristics.
(Note that it does not include quantization error.)
The theoretical conversion characteristic divides the voltage range between VREF and AGND into 1024 equal steps.

(3) Differential linearity error:
Difference between the theoretical and actual input voltage change producing a 1-bit change in the digital output anywhere within the conversion range.
This is an indicator of conversion characteristic smoothness.
The theoretical value is (VREF – Aground) ÷ 1024.

(4) Zero scale error:
Difference between the theoretical and actual conversion characteristics at the point where the digital output switches from “0x000” to “0x001.”

(5) Full scale error:
Difference between the theoretical and actual conversion characteristics at the point where the digital output switches from “0x3FE” to “0x3FF.”

ELECTRICAL CHARACTERISTICS (DC CHARACTERISTICS)

(3) USB Port Section (Full-Speed/Low-Speed Common)

(V_{DDIO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Target pins
Differential input sensitivity	VDI	|(D+) – (D–)|	0.2	—	—	V	D+, D–
Differential common mode range	VCM	VDI included	0.8	—	2.5		
Single-ended receiver threshold	VSE		0.8	—	2.0		
"H" output voltage	VOH	15 kΩ to GND	2.8	—	3.6		
"L" output voltage	VOL	1.5 kΩ to 3.6 V	—	—	0.3		
Output leakage current	ILO	V_O = 0 to V_{DD_io}	–10	—	10	uA	

(4) USB Port Section (Full-Speed)

(V_{DDIO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Measuring condition	Min.	Typ.	Max.	Unit	Target pins
Rise time(*1)	tR	CL = 50 pF	4	—	20	ns	D+, D–
Fall time(*1)	tF	CL = 50 pF	4	—	20		
Output signal crossover voltage	VCRS		1.3	—	2	V	
Driver output resistance(*2)	ZDRV	When being driven in a steady state	28	—	44	Ω	
Data rate	tDRATE	Average bit rate (12 Mbps ±0.25%)	11.97	—	12.03	Mbps	

*1: tR and tF are the intervals on the transition between the 10% and 90% points of an amplitude.
*2: ZDRV is a value that contains external serial resistance (22Ω ± 5%).

(5) USB Port Section (Low-Speed)

(V_{DDIO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Target pins
Rise time(*1)	tR	CL = 150 pF	75	—	300	ns	D+, D–
Fall time(*1)	tF	CL = 150 pF	75	—	300	ns	
Output signal crossover voltage	VCRS		1.3	—	2	V	
Data rate	tDRATE	Average bit rate (1.5 Mbps ±0.25%)	1.4775	—	1.5225	Mbps	

*1: tR and tF are the intervals on the transition between the 10% and 90% points of an amplitude.

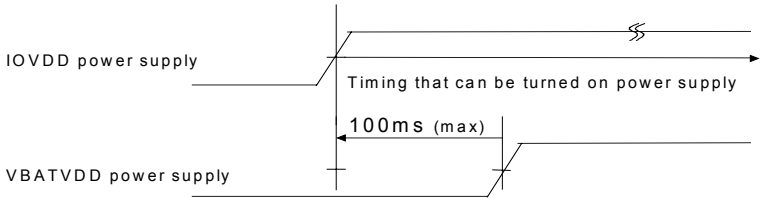
ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

[Caution]
There is no specification for rise and fall of input and output signals; however, avoid waveforms containing ripples.

(1) Restriction on the Order of Applying Power

- The IOVDD power supply can be turned on 100ms before turning on the VBATVDD power supply.
- There is no restriction on the order of turning on powers for COREVDD, VBATVDD, IOVDD, power for A/D and power for PLL, except the above restriction on IOVDD and VBATVDD.
- After the VBATVDD power supply is turned on, turn on each power supply (powers for COREVDD, VBATVDD, IOVDD, power for A/D and power for PLL) within one second.
- After the IOVDD power supply is turned on, the pin state is undefined till COREVDD power supply is turned on.

- VBATVDD Power-IOVDD Power Apply timimg



(2) Restriction on the Order of Applying Power

- Turn off the 3V power supplies, IOVDD and AVDD, first.
- There are no restrictions on the sequence of turning off power supplies, IOVDD and AVDD and on the sequence of turning off the other power supplies.

(3) Current Rise/Fall Time

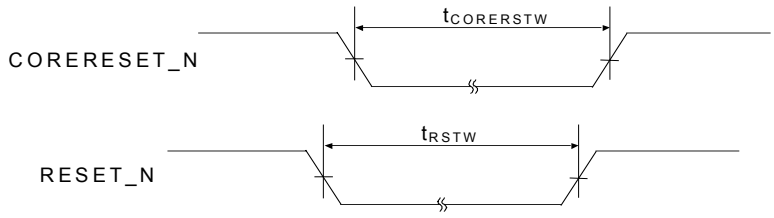
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage rise time (COREVDD, PLLVDD, VBATVDD)	t_{RV1}	0→1.35 V	—	—	100	ms
Power supply voltage rise time (IOVDD, AVDD)	t_{RV2}	0→2.7 V	—	—	100	ms
Power supply voltage fall time (COREVDD, PLLVDD, VBATVDD)	t_{FV1}	1.35→0 V	—	—	100	ms
Power supply voltage fall time (IOVDD, AVDD)	t_{FV2}	2.7 →0 V	—	—	100	ms

ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(4) Reset Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Core reset pulse width	$t_{CORERSTW}$	—	10	—	—	µs
Reset pulse width	t_{RSTW}	—	10	—	—	µs

- Reset timing

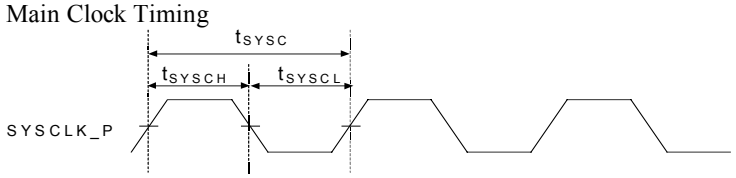


ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(5) Main Clock Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Main clock (SYSCLK_P) frequency	f_{SYSC}	—	8	—	16	MHz
Main clock (SYSCLK_P) cycle	t_{SYSC}	—	62.5	—	125	ns
Main clock (SYSCLK_P) "H" pulse	t_{SYSCH}	—	20	—	—	ns
Main clock (SYSCLK_P) "L" pulse	t_{SYSCL}	—	20	—	—	ns

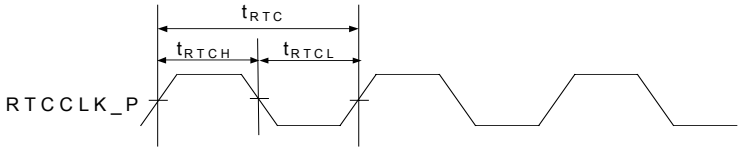
- Main Clock Timing



(6) RTC Clock Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RTC clock (RTCCLK_P) frequency	f_{RTC}	—		32.768		kHz
RTC clock (RTCCLK_P) cycle	t_{RTC}	—		30.517		µs
RTC clock (RTCCLK_P) "H" pulse width	t_{RTCH}	—	10	—	—	µs
RTC clock (RTCCLK_P) "L" pulse width	t_{RTCL}	—	10	—	—	µs

- RTC clock timing

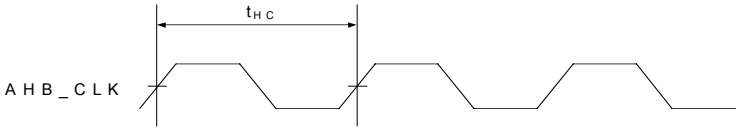


ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(7) AHB_CLK Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AHB_CLK frequency	f_{HC}		—	—	64	MHz
AHB_CLK cycle	t_{HC}		15.625	—	—	ns

- AHB_CLK Timing

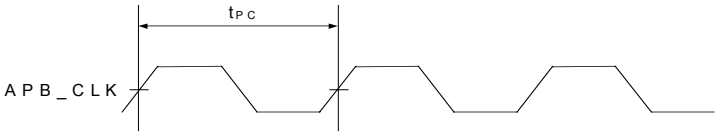


(8) APB_CLK Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
APB_CLK frequency	f_{PC}	(*1)	—	—	32	MHz
APB_CLK cycle	t_{PC}	(*2)	31.25	—	—	ns

Notes
*1: Any of $f_{PC} = f_{HC}/2$, $f_{HC}/4$ or $f_{HC}/8$
*2: Any of $t_{PC} = t_{HC} \times 2$, $t_{HC} \times 4$, or $t_{HC} \times 8$

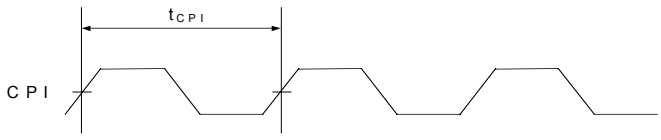
- APB_CLK Timing



(9) CPI (LCDC clock) Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CPI frequency	F_{CPI}	$F_{CPI} \le f_{HC}$	—	—	20	MHz
CPI cycle	t_{CPI}		50	—	—	ns

- CPI Timing



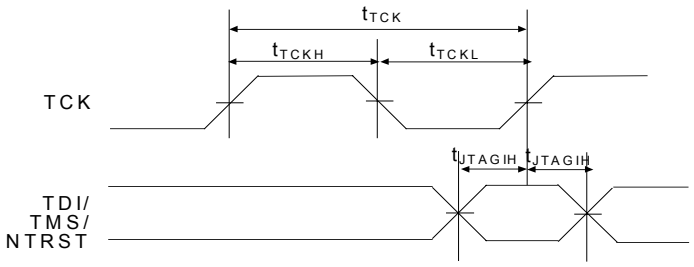
ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(10) JTAG Access Timing

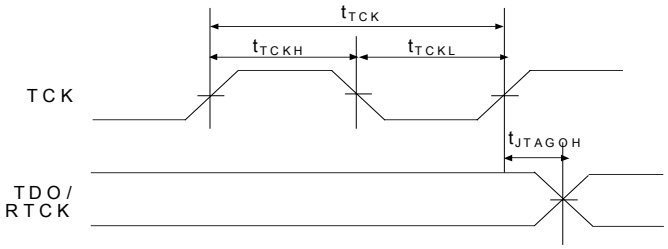
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TCK frequency	f_{TCK}	CL = 30pF	—	—	20	MHz
TCK cycle	t_{TCK}		50	—	—	
TCK "H" pulse width	t_{TCKH}		20	—	—	ns
TCK "L" pulse width	t_{TCKL}		20	—	—	
TDI, TMS, NTRST input setup time	t_{JTAGIS}		10	—	—	
TDI, TMS, NTRST input hold time	t_{JTAGIH}		10	—	—	
TDO, RTCK output hold time	t_{JTAGOH}		10	—	—	

Notes:
*: When operating JTAG, also operate the clock to CPU along with TCK.

- JTAG Input Timing



- JTAG Output Timing



ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

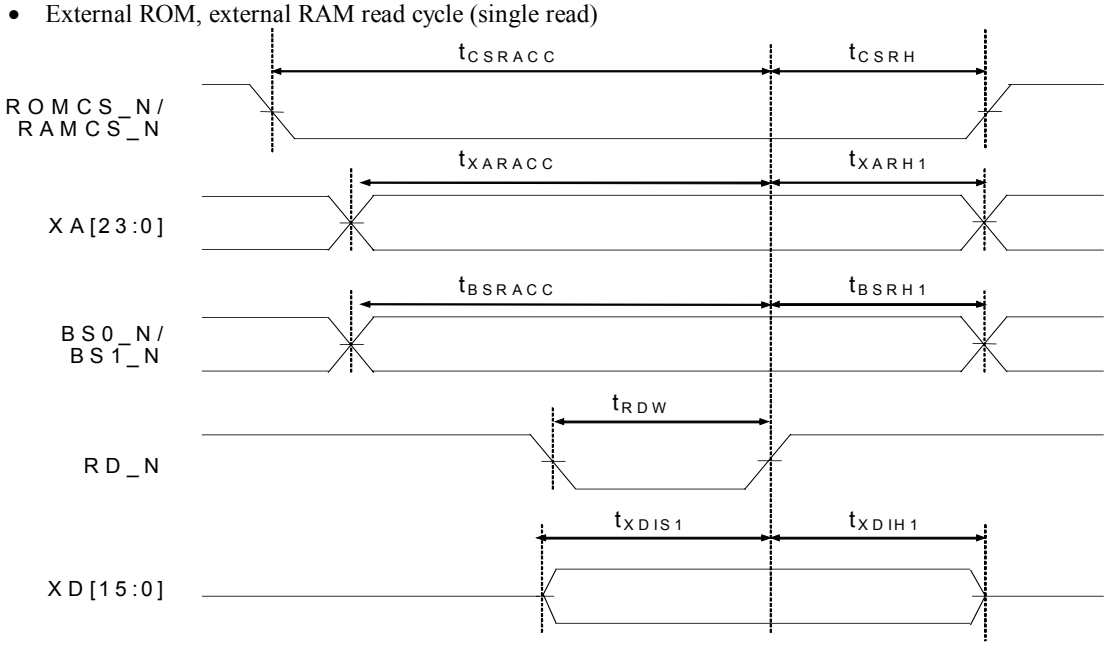
(11) External ROM, SRAM Timing (1/5)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
ROMCS_N, RAMCS_N Read access time (ROM/SRAM)	t_{CSRACC}	CL = 30 pF	$(n_{R1}+n_{R2})\ t_{HC} - 3$	—	$(n_{R1}+n_{R2})\ t_{HC} + 3$	ns	The RD_N/WR_N pulse width and the read off time when accessing SRAM/ROM are the parameters that can be set by the ROMAC/ RAMAC register. See Table below for details. n_{R1} = Address setup n_{R2} = RD_N, WR_N pulse width n_{R3} = Data off time n_{R4} = Burst timing t_{HC} = AHB_CLK cycle
ROMCS_N, RAMCS_N Write access time (ROM/SRAM)	t_{CSWACC}		$(n_{R1}+n_{R2})\ t_{HC} - 3$	—	$(n_{R1}+n_{R2})\ t_{HC} + 3$		
ROMCS_N, RAMCS_N Page mode access time (ROM/SRAM)	t_{CSPACC}		$(n_{R1}+n_{R2}+3*n_{R4})\ t_{HC} - 3$	—	$(n_{R1}+n_{R2}+3*n_{R4})\ t_{HC} + 3$		
XA[23:0] Read access time (ROM/SRAM)	t_{XARACC}		$(n_{R1}+n_{R2})\ t_{HC} - 6$	—	$(n_{R1}+n_{R2})\ t_{HC} + 6$		
XA[23:0] Write access time (ROM/SRAM)	t_{XAWACC}		$(n_{R1}+n_{R2})\ t_{HC} - 6$	—	$(n_{R1}+n_{R2})\ t_{HC} + 6$		
XA[23:0] Page mode access time (ROM/SRAM)	t_{XAPACC}		$n_{R4}t_{HC} - 6$	—	$n_{R4}t_{HC} + 6$		
BS0_N, BS1_N Read access time (ROM/SRAM)	t_{BSRACC}		$n_{R4}t_{HC} - 6$	—	$n_{R4}t_{HC} + 6$		
BS0_N, BS1_N Write access time (ROM/SRAM)	t_{BSWACC}		$n_{R4}t_{HC} - 6$	—	$n_{R4}t_{HC} + 6$		
BS0_N, BS1_N Page mode access time (ROM/SRAM)	t_{BSPACC}		$n_{R4}t_{HC} - 6$	—	$n_{R4}t_{HC} + 6$		
RD_N pulse width (ROM/SRAM)	t_{RDW}		$n_{R2}t_{HC}$ - 4	—	$n_{R2}t_{HC} + 4$		
RD_N pulse width (ROM/SRAM: Page mode)	t_{PRDW}		$(n_{R2}+3*n_{R4})\ t_{HC} - 4$	—	$(n_{R2}+3*n_{R4})\ t_{HC} + 4$		
WR_N pulse width (ROM/SRAM)	t_{WRW}		$n_{R2}t_{HC} - 4$	—	$n_{R2}t_{HC} + 4$		
ROMCS_N, RAMCS_N output hold time (ROM/SRAM : Read)	t_{CSRH}		$t_{HC} - 3$	—	—		
ROMCS_N, RAMCS_N output hold time (ROM/SRAM : Write)	t_{CSWH}		$t_{HC} - 3$	—	—		
XA[23:0] output hold time 1 (ROM/SRAM : Read)	t_{XARH1}		3	—	—		
XA[23:0] output hold time 2 (ROM/SRAM : Read)	t_{XARH2}		$t_{HC} - 3$	—	—		
XA[23:0] output hold time (ROM/SRAM : Write)	t_{XAWH}		$t_{HC} - 3$	—	—		
BS0_N, BS1_N output hold time 1 (ROM/SRAM : Read)	t_{BSRH1}		3	—	—		
BS0_N, BS1_N output hold time 2 (ROM/SRAM : Read)	t_{BSRH2}		$t_{HC} - 3$	—	—		
BS0_N, BS1_N output hold time (ROM/SRAM : Write)	t_{BSWH}		$t_{HC} - 3$	—	—		
XD[15:0] input setup time 1 (ROM/SRAM)	t_{XDIS1}		15.5	—	—		
XD[15:0] input setup time 2 (ROM/SRAM)	t_{XDIS2}		15.5	—	—		
XD[15:0] input hold time 1 (ROM/SRAM)	t_{XDIH1}		0	—	—		
XD[15:0] input hold time 2 (ROM/SRAM)	t_{XDIH2}		0	—	—		
XD[15:0] output setup time (ROM/SRAM)	t_{XDOS}		$n_{R2}t_{HC} - 6$	—	—		
XD[15:0] output hold time (ROM/SRAM)	t_{XDOH}		$t_{HC} - 6$	—	—		

ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(11) External ROM, SRAM Timing (2/5)

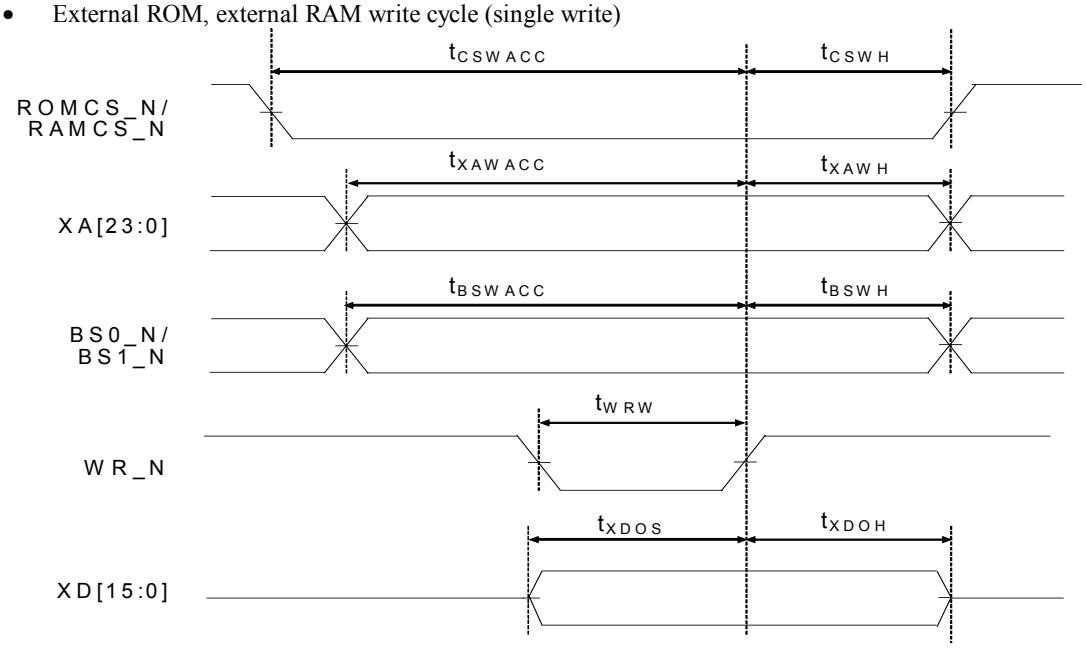
- External ROM, external RAM read cycle (single read)



ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(11) External ROM, SRAM Timing (3/5)

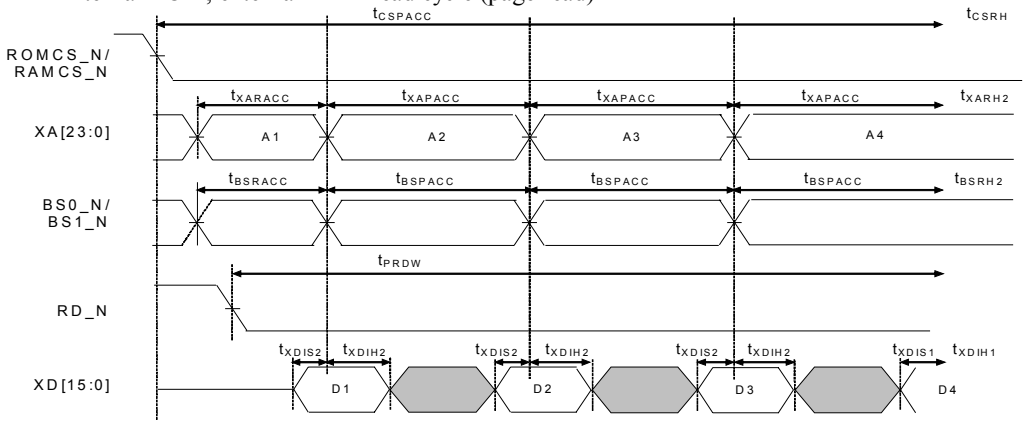
- External ROM, external RAM write cycle (single write)



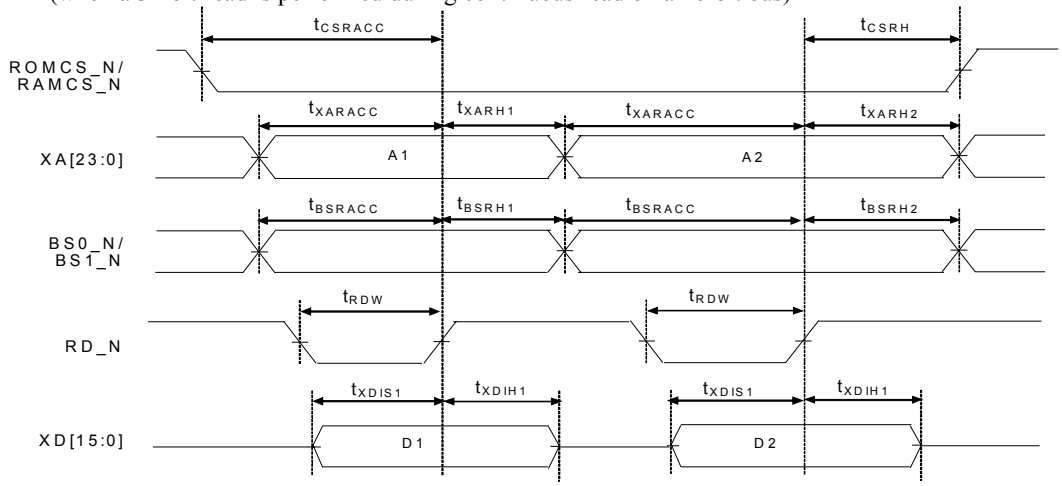
ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(11) External ROM, SRAM Timing (4/5)

- External ROM, external RAM read cycle (page read)



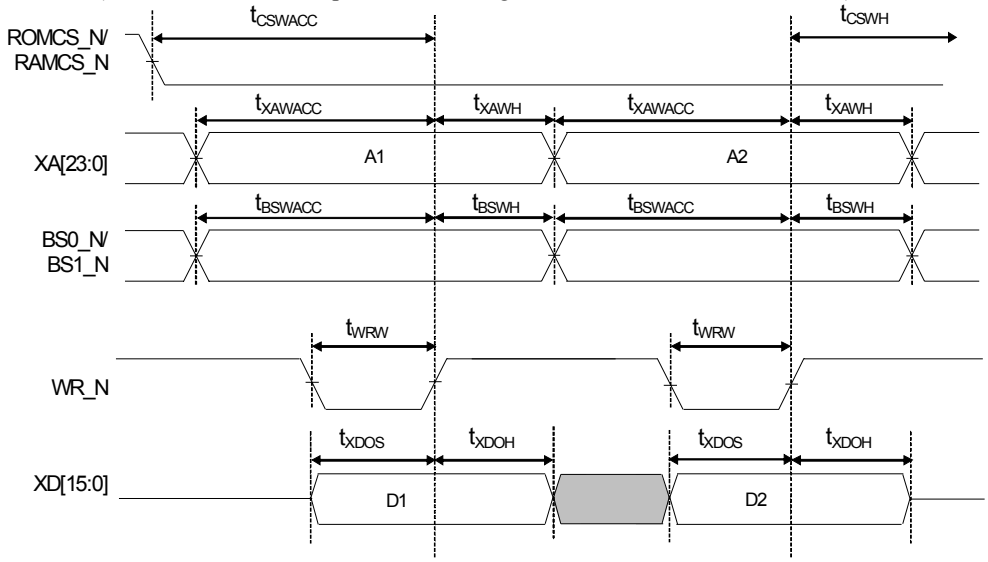
- External ROM, external RAM read cycle
  (when a 32-bit read is performed during continuous read on a 16-bit bus)



ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(11) External ROM, SRAM Timing (5/5)

- External ROM, external RAM write cycle
  (when a 32-bit write is performed during continuous write on a 16-bit bus)



ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(12) ROMAC register and timing parameters that can be set

(Please see ML675050 User's manual when refer to the ROMAC register in detail)
The following timing parameters can be set:

- Address setup
- RD_N, WR_N pulse width
- Data off timing (period for waiting the ROM output floating delay time from RD_N deassert)
- Burst timing (period from confirming the address in the page to sampling valid data)

The timing that can be set depends on memory to be connected. It is necessary to perform optimum setting according to the bus speed.

ROMTYPE[2:0]: Setting of Timing Parameters (values in the table indicate AHB_CLK count)

ROMTYPE [2:0]	Address setup	RD_N/WR_N pulse width	Data off timing	Burst timing	Remarks
000	1	1	1	1	Setting when using a high-speed ROM
001	1	2	2	2	
010	1	3	3	3	
011	1	5	3	3	
100	2	8	4	5	
101	2	10	5	6	
110	2	13	6	7	Setting when using a low-speed ROM
111	2	16	7	9	

*1: Data off timing will be three cycles when accessing from the DMAC.
For ROMAC, see Section 8.4.2, "ROM Access Control Register."
For RAMAC, see Section 8.4.3, "SRAM Access Control Register."

(13) RAMAC register and timing parameters that can be set

(Please see ML675050 User's manual when refer to the RAMAC register in detail)
The following timing parameters can be set:

- Address setup
- RD_N, WR_N pulse width
- Data off timing (period for waiting the SRAM output floating delay time from RD_N deassert)
- Burst timing (period from confirming the address in the page to sampling valid data)

RAMTYPE[2:0]: Setting of Timing Parameters (Values in the table indicate AHB_CLK count)

RAMTYPE [2:0]	Address setup	RD_N/WR_N pulse width	Data off timing(*1)	Burst timing	Remarks
000	1	1	1	1	Setting when using a high-speed SRAM
001	1	2	2	2	
010	1	3	3	3	
011	1	5	3	3	
100	2	8	4	5	
101	2	10	5	6	
110	2	13	6	7	Setting when using a low-speed SRAM
111	2	16	7	9	

ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(14) SDRAM Access Timing (1/5)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
SDCS_N delay time (SDRAM)	t_{SDCSD}	CL = 30 pF	$0.5t_{SDC} - 4$	—	$0.5t_{SDC} + 4$	ns	The tRCD, tRAS, tRP and tDPL when accessing SDRAM are the parameters that can be set by the DRPC register. See Table below for details.
SDCKE delay time (SDRAM)	t_{SDCSD}		$0.5t_{SDC} - 3$	—	$0.5t_{SDC} + 3$		
BS0_N, BS1_N delay time (SDRAM)	t_{DQMD}		$0.5t_{SDC} - 6$	—	$0.5t_{SDC} + 6$		
SDRAS_N delay time (SDRAM)	t_{SDRASD}		$0.5t_{SDC} - 3$	—	$0.5t_{SDC} + 3$		n_{SD1} = tRCD
SDCAS_N delay time (SDRAM)	t_{SDCASD}		$0.5t_{SDC} - 3$	—	$0.5t_{SDC} + 3$		n_{SD2} = tRAS
SDRAS_N-SDCAS_N Minimum delay time (SDRAM)	t_{SDRCD}	—	$n_{SD1}t_{SDC}$	—	—		n_{SD3}= tRP
SDRAS_N active time (SDRAM)	t_{SDRAS}		$n_{SD2}t_{SDC}$	—	—		
SDRAS_N precharge time (SDRAM)	t_{SDRP}		$n_{SD3}t_{SDC}$	—	—		
WR_N delay time (SDRAM)	t_{SDWED}	CL = 30 pF	$0.5t_{SDC} - 3$	—	$0.5t_{SDC} + 3$		
XD[15:0] input setup time (SDRAM)	t_{SDXDIS}		8(*1)	—	—		
XD[31:0] input hold time (SDRAM)	t_{SDXDIH}		1(*2)	—	—		
XA[23:0] delay time (SDRAM)	t_{SDXAD}		$0.5t_{SDC} - 6$	—	$0.5t_{SDC} + 6$		
XD[15:0] output delay time (SDRAM)	t_{SDXDOD}		$0.5t_{SDC} - 6$	—	$0.5t_{SDC} + 6$		
XD[15:0] output hold time (SDRAM)	t_{SDXDOH}		$0.5t_{SDC} - 3$	—			
XD[15:0] output enable time (SDRAM)	t_{SDXDOE}		$0.5t_{SDC} - 6$	—	$0.5t_{SDC} + 6$		
XD[15:0] output disable time (SDRAM)	$t_{SDXDODE}$		$0.5t_{SDC} - 3$	—			

Notes:

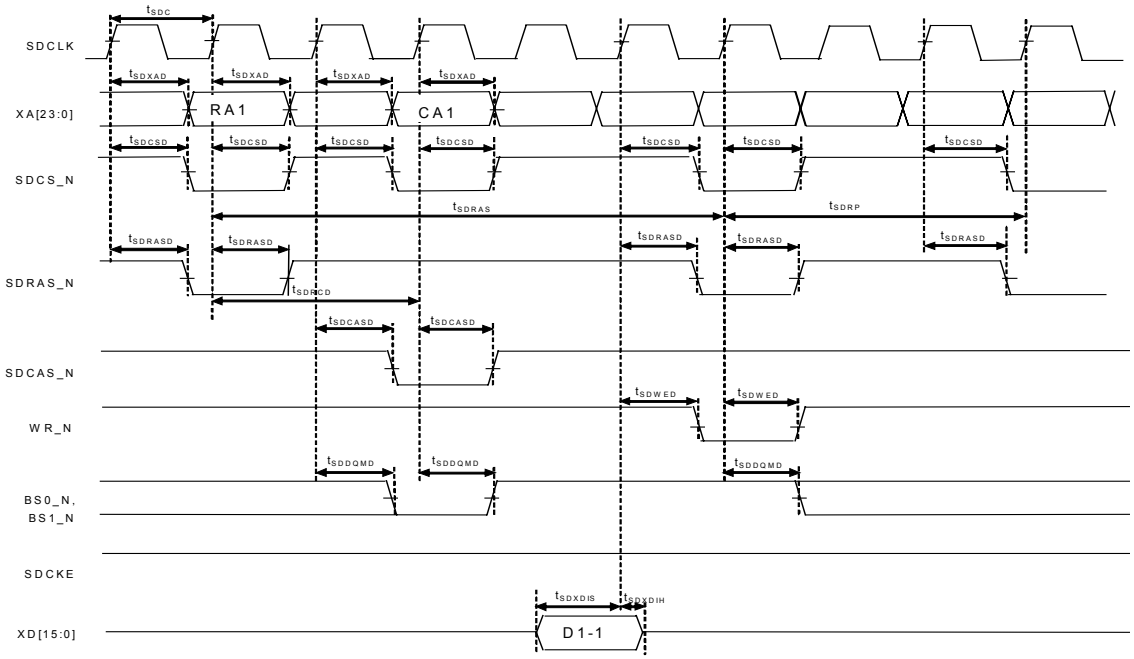
*1: Because the output delay of SDCLK increases at a rate of 0.3 ns/10 pF, the output setup time increases accordingly.

*2: The actual value will be a negative value due to external load, but input so as to guarantee minimum hold time 0.

ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(14) SDRAM Access Timing (2/5)

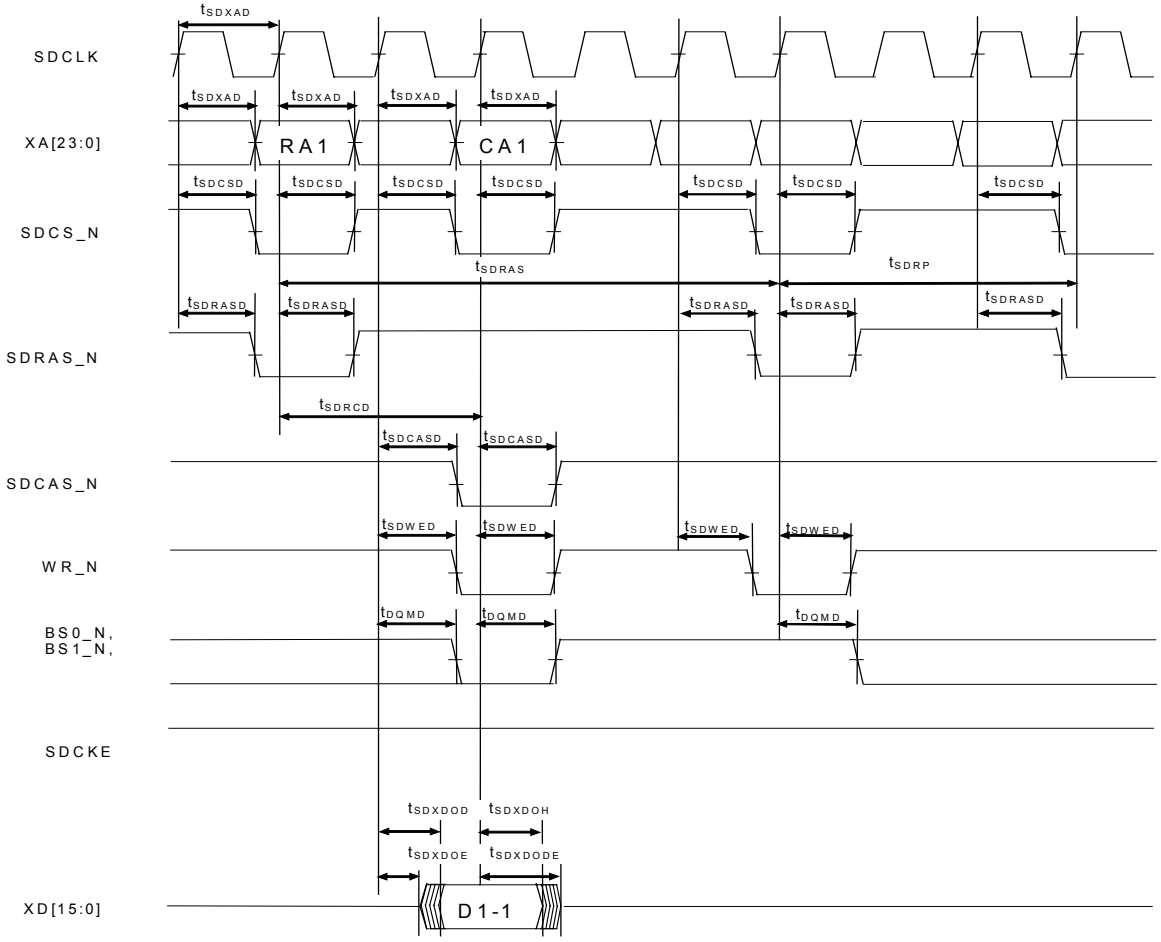
- SDRAM read cycle (16-bit bus width SDRAM; Byte/half-word access)



ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(14) SDRAM Access Timing (3/5)

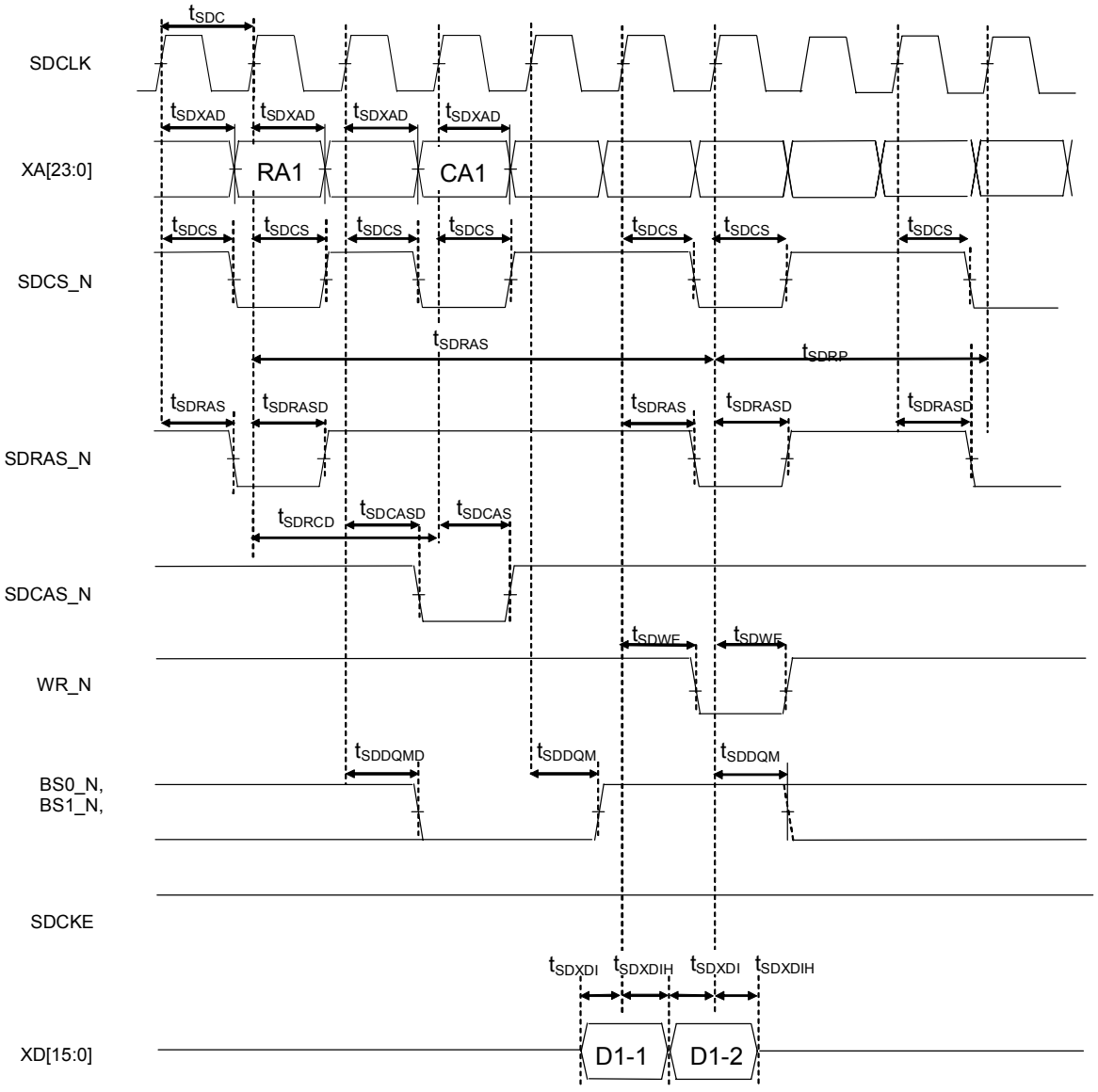
- SDRAM write cycle (16-bit bus width SDRAM; Byte/half-word access)



ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(14) SDRAM Access Timing (4/5)

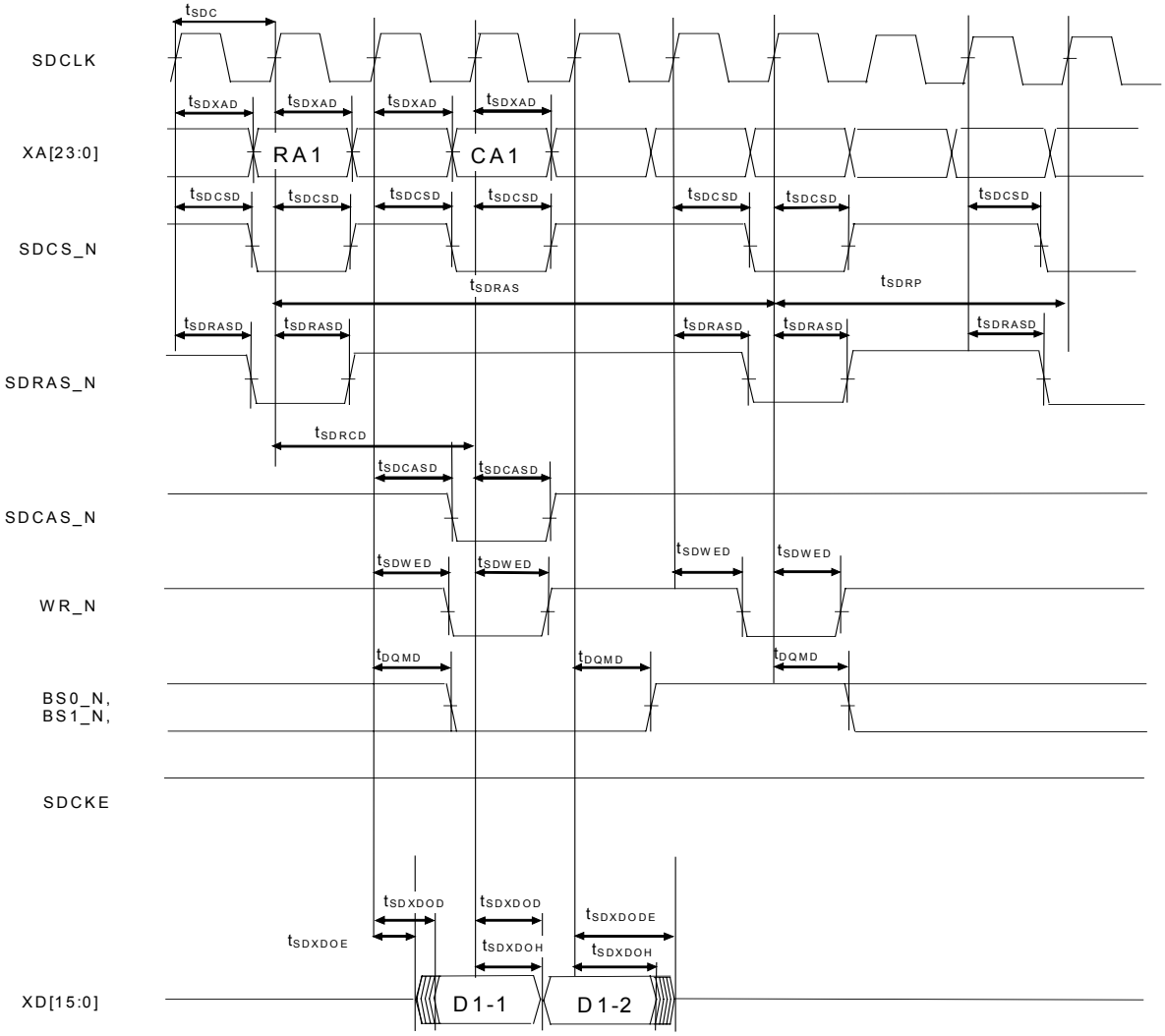
- SDRAM read cycle (16-bit bus width SDRAM; word access)



ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(14) SDRAM Access Timing (5/5)

- SDRAM write cycle (16-bit bus width SDRAM; word access)



ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(15) DRPC register setting and parameters (tRCD, tRAS, tRP, tDPL)

(Please see ML675050 User's manual when refer to the DPRC register in detail)
DRAM SPEC: DRAM characteristics parameter setting

SDRAM DRAM SPEC [3:0]	tRCD	tRAS	tRP	tDPL	
0000	1	2	1	1	High-speed DRAM Low frequency
0001	1	3	1	1	
0010	2	3	2	1	
0011	2	4	2	1	
0100	2	4	2	2	
0101	2	5	2	1	
0110	2	5	2	2	
0111	2	5	3	1	
1000	3	5	3	2	
1001	3	6	3	2	Low-speed DRAM High frequency
1010 : 1111	Reserved				If set to this value, operation is not guaranteed. : If set to this value, operation is not guaranteed.

Note: For DRPC, see Section 11.6.3, "DRAM Characteristics Parameter Control Register."

ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(16) External IO0,1 Timing (1/3)

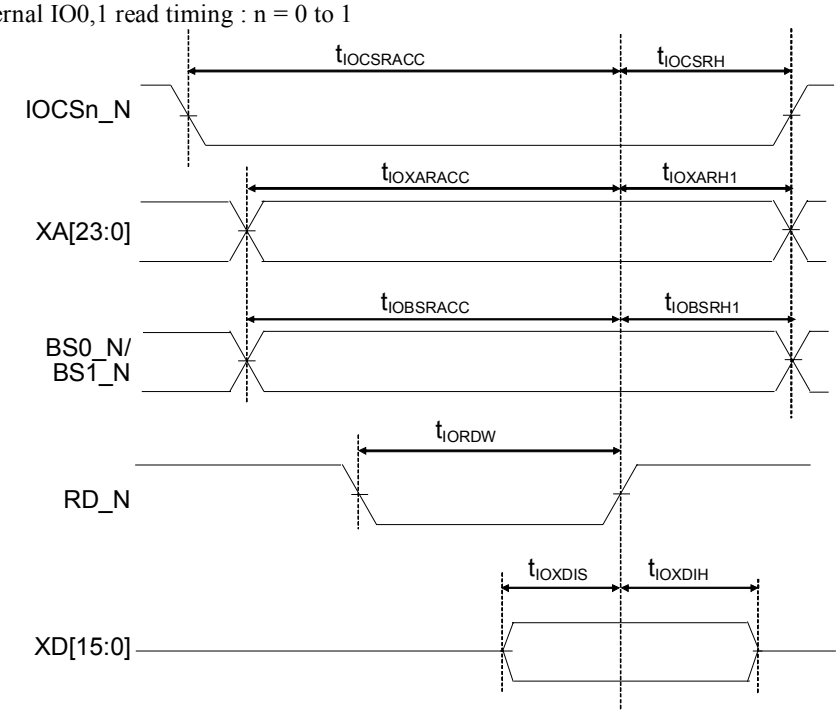
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
IOCSn_N read access time (IO0/IO1)	$t_{IOCSRACC}$	CL = 30 pF	$(n_1+n_2)t_{HC}$-3	—	$(n_1+n_2)t_{HC}$+4	ns	*: The address setup, RD_N/WR_N pulse width, and data off time when IO0 and IO1 are accessed are the parameters that can be set by the IOAC register. For more details, see the upper table on page 29-26. *: Address hold time is fixed by a combination of the type of read access, data size at the time of read access, and IO bus width. For more details, see the lower table on page 29-26. *: XWAIT is not used. n_1 = Address setup n_2 = Access pulse width n_3 = Address hold time t_{HC} = AHB_CLK period
IOCSn_N write access time (IO0/IO1)	$t_{IOCSWACC}$		(n_1+n_2+1) t_{HC}-3	—	(n_1+n_2+1) t_{HC}+4		
XA[23:0] read access time (IO0/IO1)	$t_{IOXARACC}$		$(n_1+n_2)t_{HC}$-4	—	$(n_1+n_2)t_{HC}$+3		
XA[23:0] write access time (IO0/IO1)	$t_{IOXAWACC}$		(n_1+n_2+1) t_{HC}-5	—	(n_1+n_2+1) t_{HC}+3		
BS0_N, BS1_N read access tim (IO0/IO1)	$t_{IOBSRACC}$		$(n_1+n_2)t_{HC}$-4	—	$(n_1+n_2)t_{HC}$+3		
BS0_N, BS1_N write access time (IO0/IO1)	$t_{IOBSWACC}$		(n_1+n_2+1) t_{HC}-5	—	(n_1+n_2+1) t_{HC}+3		
RD_N pulse width (IO0/IO1)	t_{IORDW}		n_2t_{HC} - 4	—	n_2t_{HC} + 4		
WR_N pulse width (IO0/IO1)	t_{IOWRW}		n_2t_{HC} - 4	—	n_2t_{HC} + 4		
IOCSn_N output hold time (IO0/IO1 : Read)	t_{IOCSRH}		t_{HC} - 3	—	—		
IOCSn_N output hold time (IO0/IO1 : Write)	t_{IOCSWH}		t_{HC} - 3	—	—		
XA[23:0] output hold time 1 (IO0/IO1 : Read)	$t_{IOXARH1}$		n_3t_{HC} - 3	—	—		
XA[23:0] output hold time 2 (IO0/IO1 : Read)	$t_{IOXARH2}$		t_{HC} - 3	—	—		
XA[23:0] output hold time (IO0/IO1 : Write)	t_{IOXAWH}		t_{HC} - 3	—	—		
BS0_N, BS1_N output hold time 1 (IO0/IO1 : Read)	$t_{IOBSRH1}$		n_3t_{HC} - 3	—	—		
BS0_N, BS1_N output hold time 2 (IO0/IO1 : Read)	$t_{IOBSRH2}$		t_{HC} - 3	—	—		
BS0_N, BS1_N output hold time (IO0/IO1 : Write)	t_{IOBSWH}		t_{HC} - 3	—	—		
XD[15:0] input setup time (IO0/IO1)	t_{IODIS}		15.5	—	—		
XD[15:0] input hold time (IO0/IO1)	t_{IODIH}		0	—	—		
XD[15:0] output setup time (IO0/IO1)	t_{IODOS}		$(n_1+n_2)t_{HC}$ - 7	—	—		
XD[15:0] output hold time (IO0/IO1)	t_{IODOH}		t_{HC} - 3	—	—		

Note: n = 0 to 1.

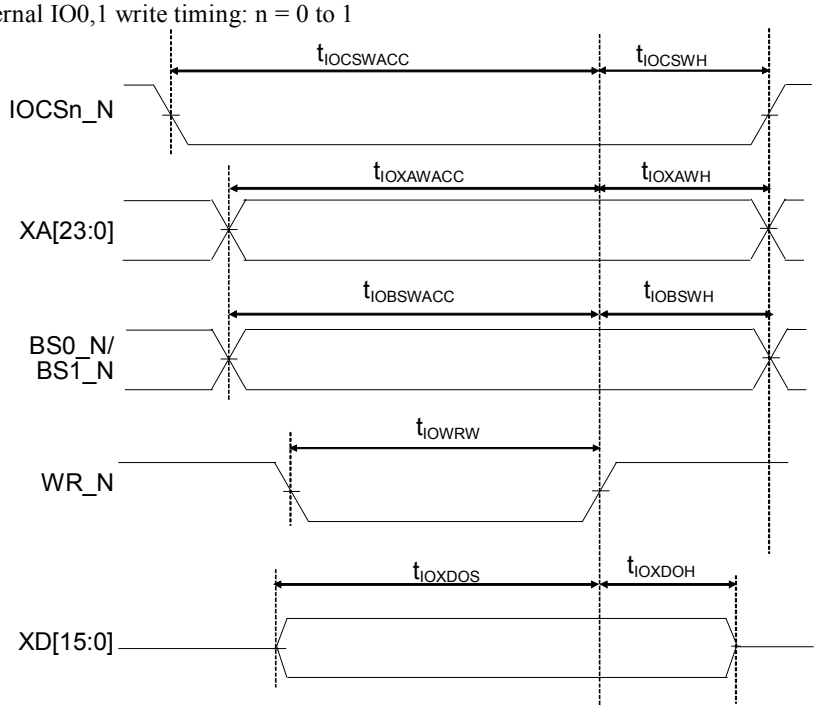
ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(16) External IO0,1 Timing (2/3)

- External IO0,1 read timing : n = 0 to 1



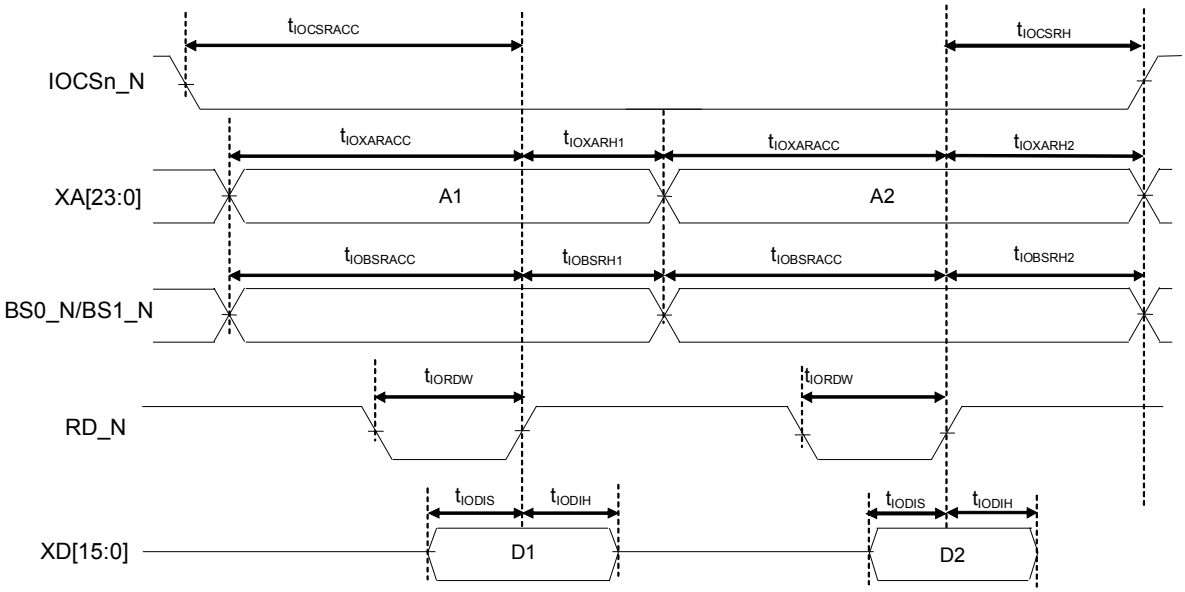
- External IO0,1 write timing: n = 0 to 1



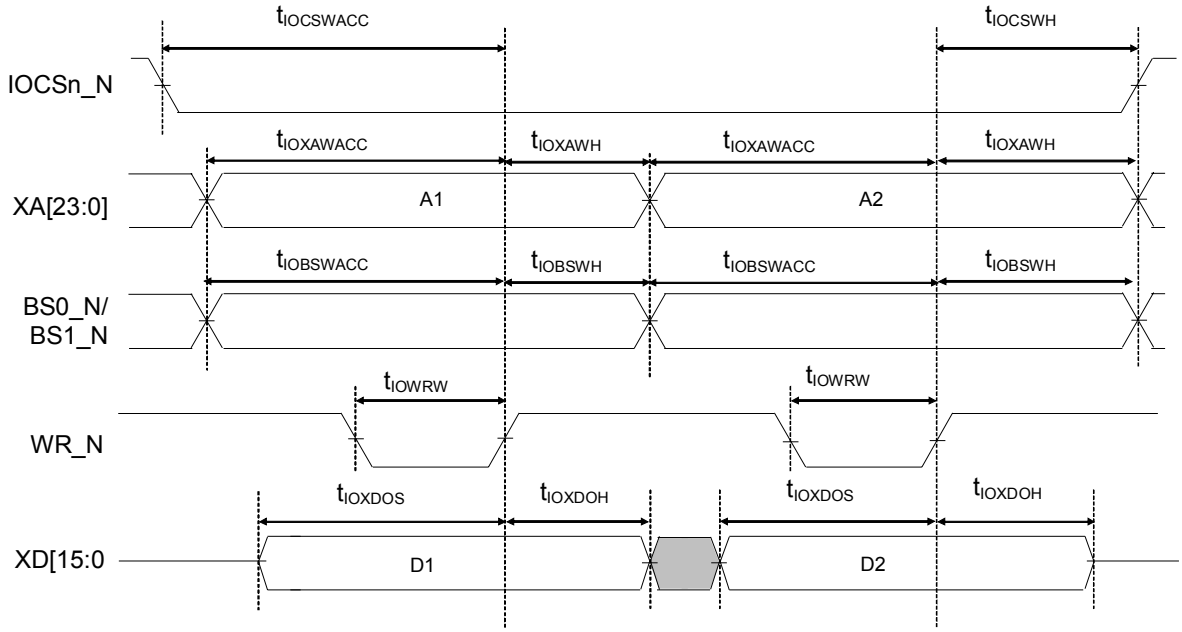
ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(16) External IO0,1 Timing (3/3)

- External I/O continuous read cycle (when a 32-bit read is performed on a 16-bit bus): n = 0 to 1



- External I/O continuous write cycle (when a 32-bit write is performed on a 16-bit bus): n = 0 to 1



ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(17) IOAC register and timing parameters that can be set

(Please see ML675050 User's manual when refer to the IOAC register in detail)
The following timing parameters can be set:

- Address setup
- RD_N/WR_N pulse width
- Data off timing (period for waiting the I/O output floating delay time from RD_N deassert)

IOTYPE[2:0]: Setting of Timing Parameters (Values in the table indicate AHB_CLK count)

IO TYPE[2:0]	Address setup	RD_N/WR_N pulse width	Data off timing
000	1	1	1
001	1	4	3
010	1	6	4
011	2	8	5
100	2	12	7
101	2	16	8
110	3	20	9
111	4	24	11

Note: For IOAC, see Section 8.4.4, "IO Access Control Register."

(18) Address hold time

Address hold time is fixed by a combination of the type of read access, data size at the time of read access, and IO bus width.

Access master	Type of access	Data size at the time of read access (bit)	IO bus width (bit)	Address hold time (AHB_CLK)
ARM processor	—	8/16	16	1
		8	8	1
		16	8	0
AHB master	SINGLE/INCR	8/16	16	1
		8	8	1
		16	8	0
	INCR4/8/16, WRAP4/8/16	8/16	8/16	0

ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(19) I²C Access Timing

Standard Mode

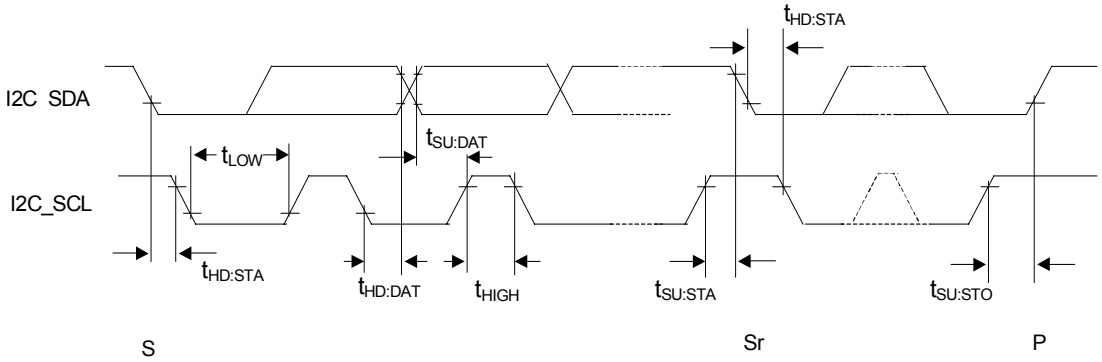
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
I2C_SCL clock frequency	f_{SCL}	CL=400pF	—		100	kHz
I2C_SCL clock "L" period	t_{LOW}		4.7		—	us
I2C_SCL clock "H" period	t_{HIGH}		4.0		—	us
(Repetitive) "START" condition hold time After this period, the first clock pulse is generated.	$t_{HD:STA}$		4.0		—	us
Repetitive "START" condition setup time	$t_{SU:STA}$		4.7		—	us
Data hold time	$t_{HD:DAT}$		5.0		—	us
Data setup time	$t_{SU:DAT}$		250		—	us
"STOP" condition setup time	$t_{SU:STO}$		4.0		—	us

Fast Mode

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
I2C_SCL clock frequency	f_{SCL}	CL=400pF	—		400	kHz
I2C_SCL clock "L" period	f_{LOW}		1.3		—	us
I2C_SCL clock "H" period	f_{HIGH}		0.6		—	us
(Repetitive) "START" condition hold time. After this period, the first clock pulse is generated.	$t_{HD:STA}$		0.6		—	us
Repetitive "START" condition setup time	$t_{SU:STA}$		0.6		—	us
Data hold time	$t_{HD:DAT}$		—		—	us
Data setup time	$t_{SU:DAT}$		400(*1)		—	us
"STOP" condition setup time	$t_{SU:STO}$		0.6		—	us

*1: Although a fast-mode I²C bus device can be utilized in the standard I²C bus system, the required condition "tSU: DAT ≥ 250 ns" should be satisfied. This means that the device is in the state in which it does not extend the "L" period of the I2C_SCL signal.
If a certain device does not extend the "L" period of the I2C_SCL signal, it should output the next data to the I2C_SDA line 1250 ns (for the next data bit in the standard mode, according to the I²C Bus specification) before the I2C_SCL line is released (1250 ns = trmax + $t_{SU: DAT}$ = 1000 + 250).

- I²C cycle



ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(20) SPI Access Timing (1/4)

Master Mode Timing Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Serial clock cycle time	t_{sck}	—	$2 \times t_{PC}$(*3)	—	$2046 \times t_{PC}$	ns
Serial clock "H"/"L" time	t_{wsck}	—	$1 \times t_{PC}$(*3)	—	$1023 \times t_{PC}$	ns
Data delay time (output)	t_{dd}	—	—	—	25	ns
Data setup time (input)	t_{sd}	CL=30pF	—	—	25(*1)	ns
Data hold time (input)	t_{hd}	—	0(*2)	—	—	ns
SSN-SCK lead time	t_{lead}	—	$0.5 \times t_{sck}$	—	$1.5 \times t_{sck}$	ns
SCK-SSN time lag	t_{lag}	—	$0.5 \times t_{sck}$	—	$1.5 \times t_{sck}$	ns
SSN "H" minimum guaranteed time	t_{wssh}	—	$1 \times t_{sck}$	—	$511 \times t_{sck}$	ns
SPI bus input-outputrise time/fall time	t_r, t_f	—	—	—	25	ns

*1: Because the output delay of SCK increases at a rate of 0.4 ns/10 pF, the data setup time increases accordingly.

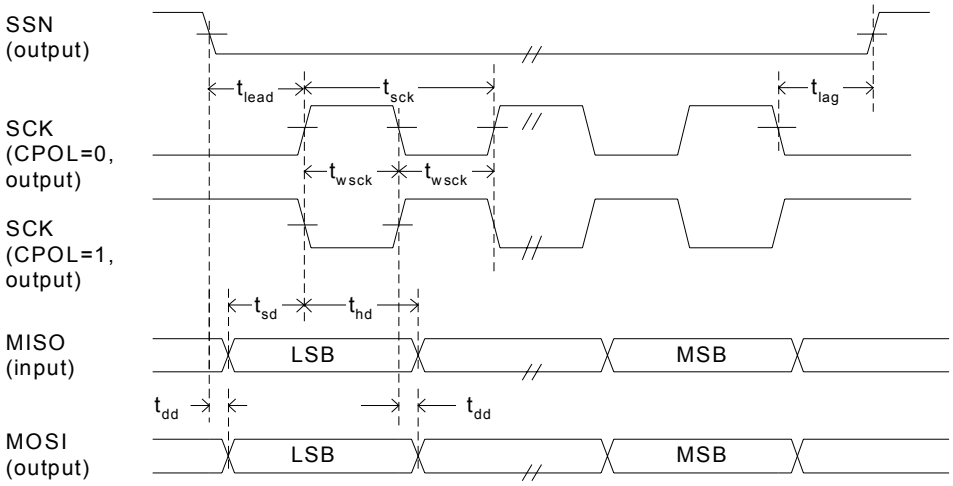
*2: The actual value will be a negative value due to external load, but input so as to guarantee data hold time 0.

*3: t_{PC} is the cycle time of APB_CLK.

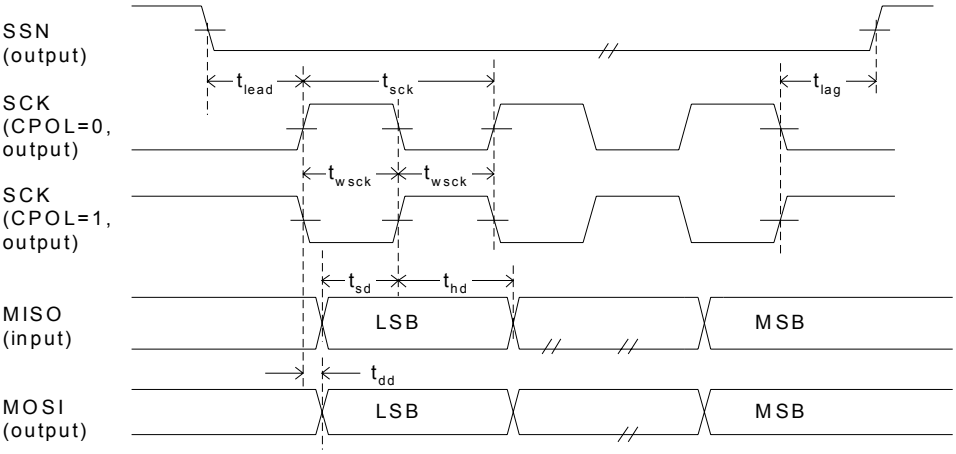
ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(20) SPI Access Timing (2/4)

- SPI master mode timing (CPHA = 0)



- SPI master mode timing (CPHA = 1)



Note: For CPHA and CPOL, please see Section 24.4.1, “SPI Control Register.” of ML675050 User’s manual

ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(20) SPI Access Timing (3/4)

Slave Mode Timing Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Serial clock cycle time	t_{sck}	—	$2 \times t_{PC}$ (*2)	—	—	ns
Serial clock "H"/"L" time	t_{wsck}	—	$1 \times t_{PC}$ (*2)	—	—	ns
Data delay time (output)	t_{dd}	—	—	—	25 (*1)	ns
Data setup time (input)	t_{sd}	—	—	—	25	ns
Data hold time (input)	t_{hd}	—	25	—	—	ns
SSN-SCK lead time	t_{lead}	—	25	—	—	ns
SCK-SSN time lag	t_{lag}	—	25	—	—	ns
Slave data disable time	t_{dis}	—	—	—	25	ns
SPI bus input-output rise time/fall time	t_r, t_f	—	—	—	25	ns

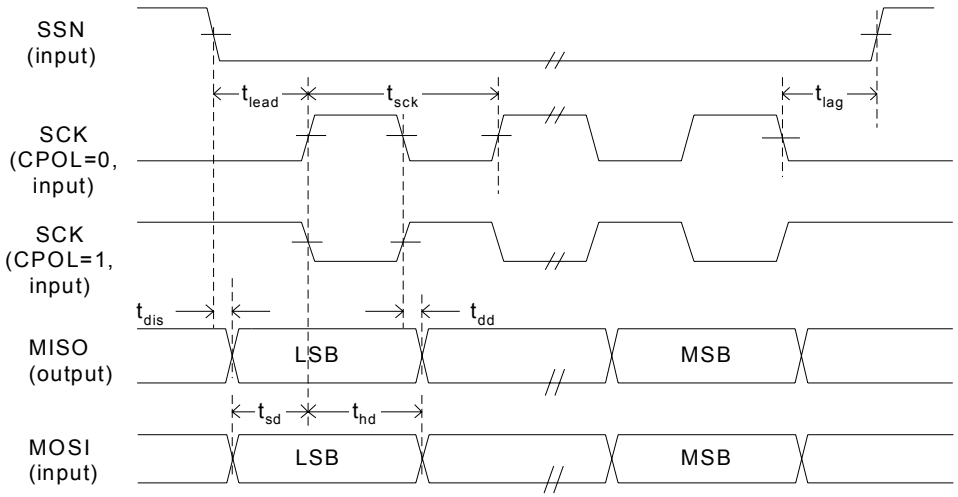
*1: The output delay increases at a rate of 0.4 ns/10 pF.

*2: t_{PC} is the cycle time of APB_CLK.

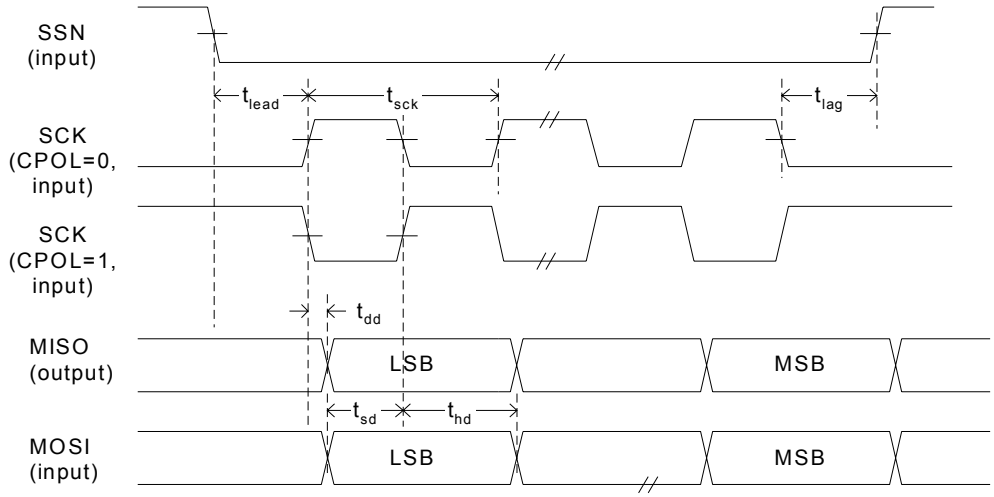
ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(20) SPI Access Timing (4/4)

- SPI slave mode timing (CPHA = 0)



- SPI slave mode timing (CPHA = 1)



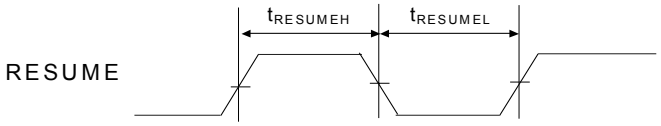
Note: For CPHA and CPOL, please see Section 24.4.1, “SPI Control Register.” of ML675050 User’s manual

ELECTRICAL CHARACTERISTICS (AC CHARACTERISTICS)

(21) Resume Access Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RESUME "H" period	t_{resH}	—	10	—	—	ns
RESUME "L" period	t_{resL}	—	10	—	—	ns

- Resume Access Timing

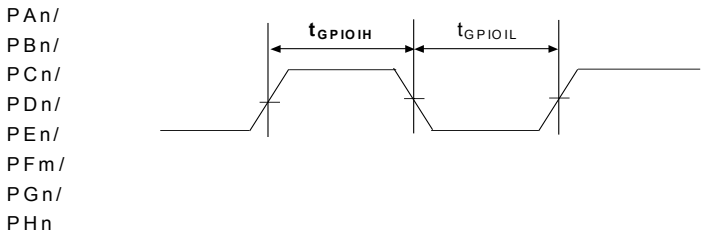


(22) GPIO0 to 7 (PA, PB, PC, PD, PE, PF, PG, PH) Access Timing

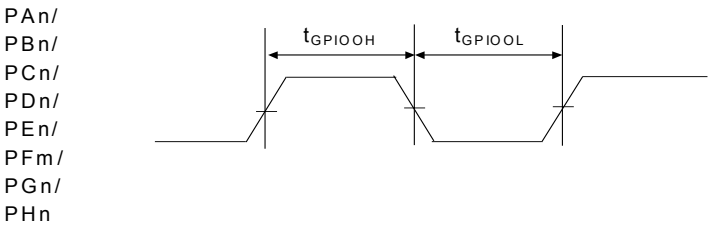
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PAn, PBn, PCn, PDn, PEn, PFm, PGn, PHn input "H" period	t_{GPIOIH}	—	10	—	—	ns
PAn, PBn, PCn, PDn, PEn, PFm, PGn, PHn input "L" period	t_{GPIOIL}	—	10	—	—	ns
PAn, PBn, PCn, PDn, PEn, PFm, PGn, PHn output "H" period	t_{GPIOOH}	APB_CLK : A case of cpu continuous access a register of GPIO in 32MHz.	62.5	—	—	ns
PAn, PBn, PCn, PDn, PEn, PFm, PGn, PHn output "L" period	t_{GPIOOL}		62.5	—	—	ns

*1: n = 0 to 7, m = 0 to 5

- PA, PB, PC, PD, PE, PF, PG, PH input timing (n = 0 to 7, m = 0 to 5)



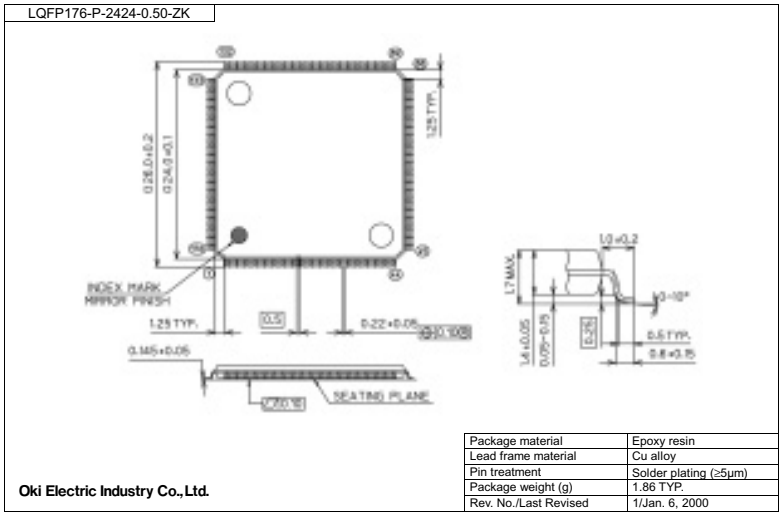
- PA, PB, PC, PD, PE, PF, PG, PH output timing (n = 0 to 7 m = 0 to 5)



PACKAGE DIMENSIONS

(1) 176pin LQFP(LQFP176-P-2424-0.50-ZK)

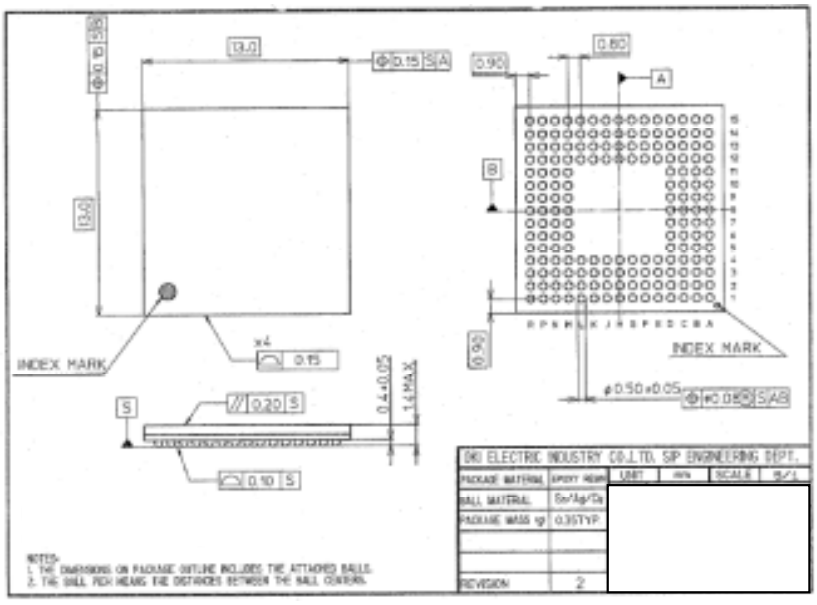
(Unit: mm)



Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	1.86 TYP.
Rev. No./Last Revised	1/Jan. 6, 2000

(2) 176pin LFBGA(P-LFBGA176-1313-0.80-2)

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL675050-01	Nov. 10, 2006	–	–	Final edition 1
FEDL675050-02	Mar. 1, 2007	24	24	SIM interface descript correction

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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