DATA SHEET

OKI ARM-BASED MICROCONTROLLER PRODUCTS

ML674000
32-Bit ARM®-Based General Purpose Microcontroller

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Oki Semiconductor

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32-Bit ARM®-Based General-Purpose Microcontroller

DESCRIPTION

Oki's ML674000 standard microcontroller (MCU) is a member of an extensive and growing family of ARM® architecture 32-bit MCUs for general-purpose applications that require 32-bit CPU performance and low cost afforded by MCU integrated features.

Oki Semiconductor's ML674000 MCU provides a host of useful peripherals such as 8KB of on-board SRAM, timers, watchdog timer, pulse-width modulators, AD converter, UART's, GPIO connectivity capability, and external memory controller. These integrated features make it ideal for embedded applications where low costs and low power consumption are key.

Oki's ML674K series MCUs are capable of executing both the 32-bit ARM instruction set for high-performance applications as well as the 16-bit Thumb® instruction set for power-efficient applications. With an ARM7TDMI® core operating at 33 MHz maximum frequency, ARM Thumb™ capabilities, and robust feature sets, the ML674K series MCUs are suitable for an array of applications including high performance industrial controllers and instrumentation, telecom, PC peripherals, security/surveillance, test equipment, and a variety of consumer electronics devices.

The ARM7TDMI® Advantage

Oki Semiconductor's ML67 Family of low-cost ARM-based MCUs offers system designers a bridge from 8- and 16-bit proprietary MCU architectures to ARM's higher-performance, affordable, widely-accepted industry standard architecture and its industry-wide support infrastructure. The ARM industry infrastructure offers system developers many advantages including software compatibility, many ready-to-use software applications, and a large choice among hardware and software development tools. These ARM-based advantages allow Oki's customers to better leverage engineering resources, lower development costs, minimize project risks, and reduce their product time to market. In addition, migration of a design with an Oki standard MCU to an Oki custom solution is easily facilitated with its award-winning µPLAT™ product development architecture.

FEATURES

- ARM7TDMI 32-bit RISC CPU
- 32-bit mode (ARM) and/or 16-bit mode (Thumb)
- Built-in external memory controller supports glue-less connectivity to memory (including SDRAM and EDO DRAM) and I/O
- 8 KB built in zero-wait-state SRAM
- 24 interrupt sources
- DMA: 2 channels with external access
- Timers: 7 x 16-bit timers
- Watch-Dog Timer: dual stage 16 bit
- PWM: 2 x 16-bit channels
- Serial Interfaces: SIO, UART
- GPIO: 32 bits
- AD Converter: 8 x 10-bit channels
- Available in 128 TQPF and 144 LFBGA packages

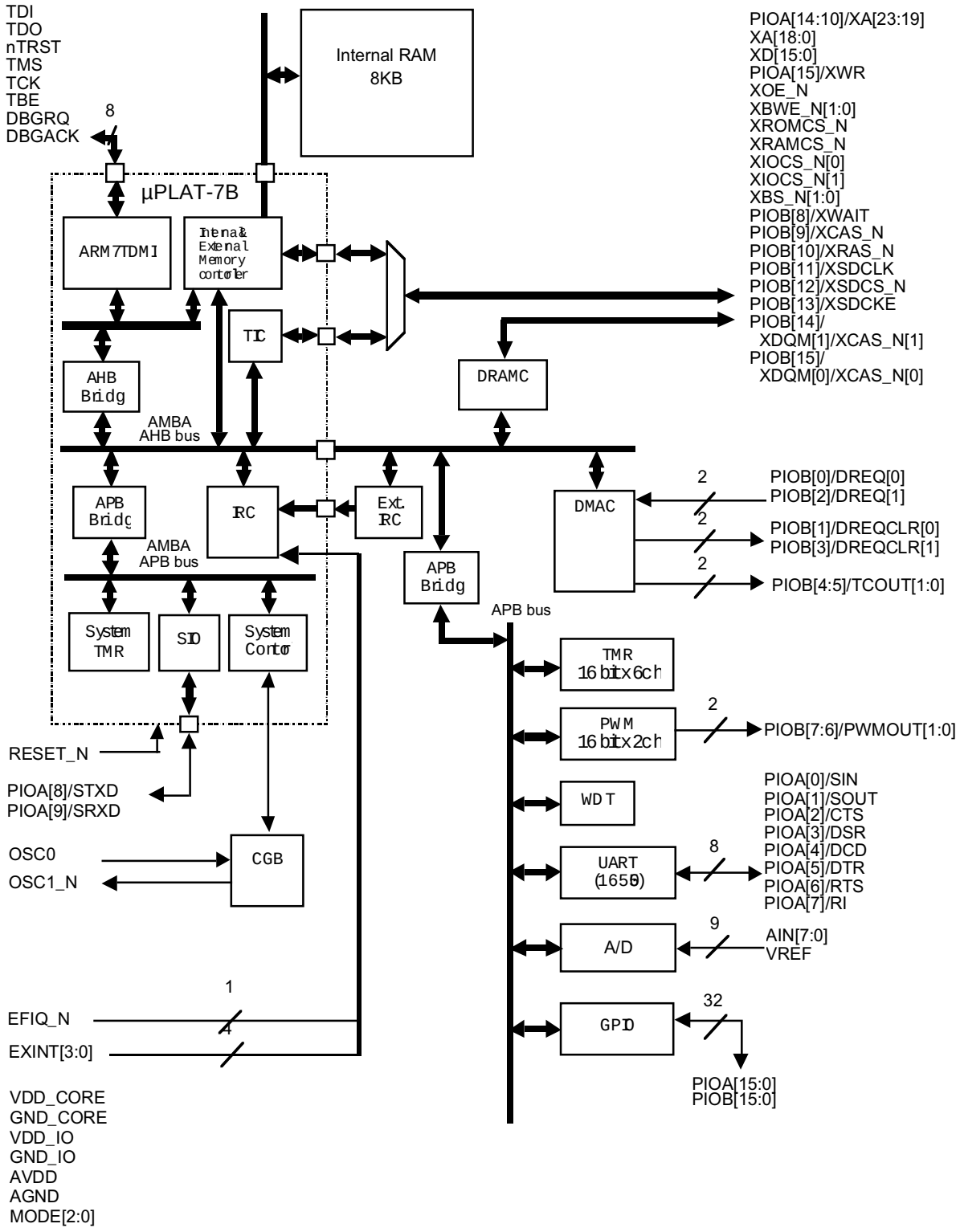
APPLICATIONS

- Flexible solution for various cost-effective, power-sensitive embedded real-time control applications
- Security / Surveillance, Telecom, Industrial Control, Electronic Peripherals, and Consumers Electronics embedded application

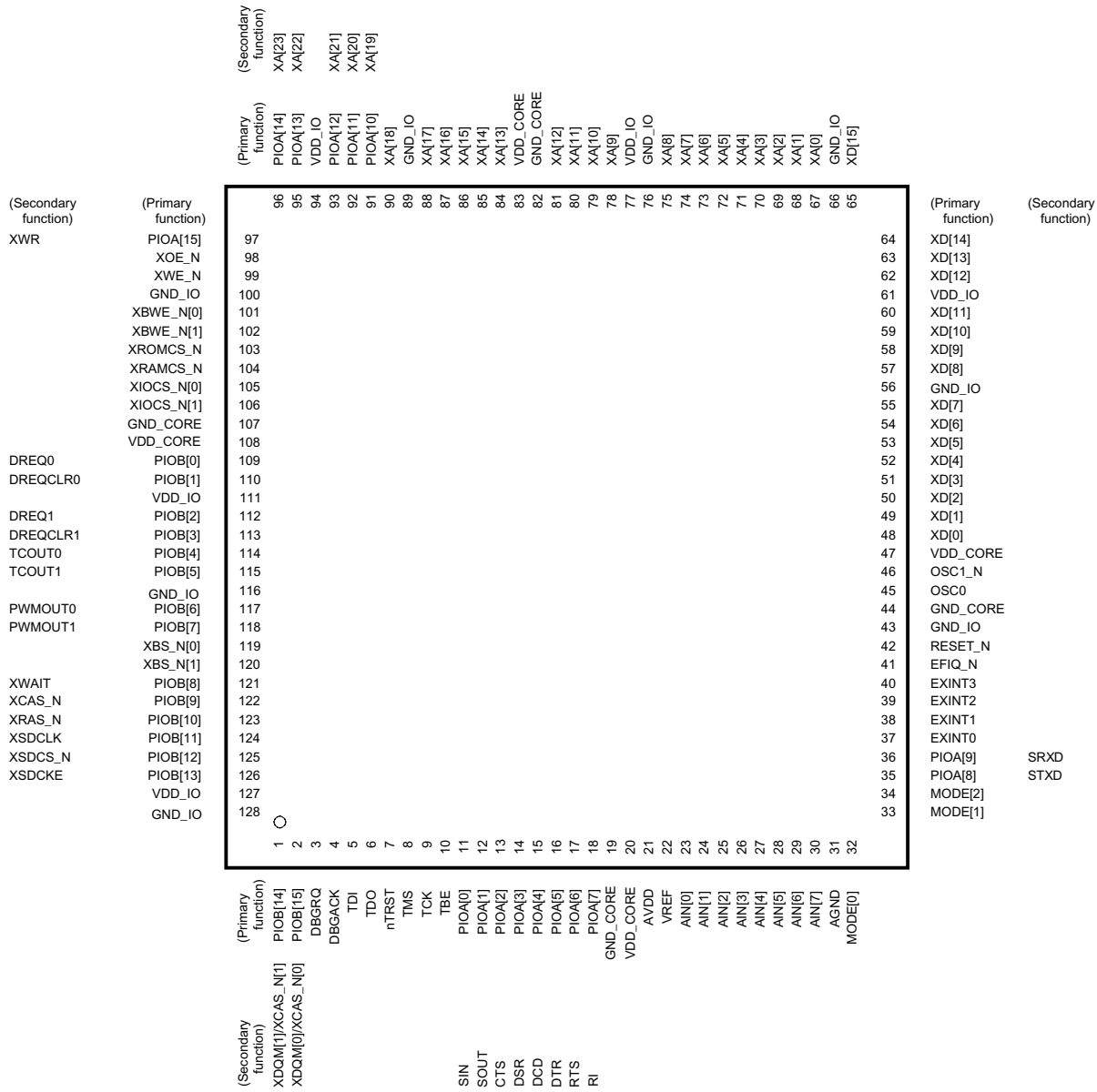
SPECIFICATION OVERVIEW

CPU	32-bit RISC (ARM7TDMI) 32-bit mode (ARM instructions) and/or 16-bit mode (Thumb instructions) General purpose registers : 31 x 32 bits Barrel shifter and multiplier (32 bit x 8 bit) Little endian On-chip debug and in-circuit-emulation (ICE)
Internal memory	8 KB of SRAM; 32-bit single clock access
External memory controller	Glueless connectivity to the following: ROM (Flash): up to 16 MBytes SRAM: up to 16 MBytes DRAM: up to 64 MBytes (SDRAM and EDO DRAM support) External IO devices: up to 16 MBytes x 2 banks (with wait control by external signal). Programmable wait setting by each bank.
Interrupt controller	24 sources: 19 internal and 5 external (IRQ: 4, FIQ: 1) 8 level priority, inidividually maskable
DMA controller	2 channels; Supports dual address mode transfers, burst mode and cycle steel
Timers	7 channels: 16-bit auto reload for application 1 channel: 16 bit watchdog timer
Serial I/O interface	1 channel UART with Tx and Rx signals only
UART	1 channel: asynchronous with 16-Byte FIFO
GPIO	2 channels x 16 bits
PWM	2 channels x 16 bits
A to D converter	8 channels x 10 bits
Power down mechanism	Standby and Halt (halting of clock to each block is configurable independently) Clock ratio (selectable 1/1, 1/2, 1/4, 1/8, 1/16 input clock frequency)
JTAG interface	Porivdes access to the on-chip ICE (In Circuit Emulation)
Power supply voltage	Core: 2.25 V to 2.75 V, I/O section: 3.0 V to 3.6 V
Operating frequency	33 MHz (Maximum)
Operating temp (ambient)	–40°C to +85°C
Package	128-pin plastic TQFP (TQFP128-P-1414-0.40-K) 144-pin plastic LFBGA (P-LFBGA144-1111-0.80)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



128-Pin Plastic TQFP

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	NC	NC	NC	PIOA[12]/ XA[21]	XA[18]	XA[16]	GND_ CORE	XA[8]	XA[5]	XA[2]	GND_IO	XD[15]	NC	13
12	PIOA[15]/ XWR	PIOA[14]/ XA[23]	VDD_IO	GND_IO	XA[15]	XA[14]	XA[10]	GND_IO	XA[7]	XA[4]	XA[1]	NC	XD[14]	12
11	XOE_N	GND_IO	NC	PIOA[11]/ XA[20]	PIOA[10]/ XA[19]	VDD_ CORE	XA[12]	XA[9]	XA[3]	XA[0]	NC	VDD_IO	XD[13]	11
10	XBWE_ N[0]	XROM CS_N	XWE_N	PIOA[13]/ XA[22]	XA[17]	XA[13]	XA[11]	VDD_IO	XA[6]	XD[12]	XD[10]	GND_IO	XD[11]	10
9	XRAM CS_N	XIOCS_ N[1]	XBWE_ N[1]	XIOCS_ N[0]						XD[7]	XD[9]	XD[5]	XD[8]	9
8	GND_ CORE	VDD_ CORE	PIOB[1]/ DREQCLR0	PIOB[0]/ DREQ0						XD[3]	XD[2]	XD[4]	XD[6]	8
7	PIOB[4]/ TCOUT0	VDD_IO	PIOB[3]/ DREQCLR1	PIOB[2]/ DREQ1						XD[0]	XD[1]	NC	NC	7
6	XBS_N[0]	PIOB[6]/ PWMOUT0	PIOB[5]/ TCOUT1	GND_IO						NC	VDD_ CORE	OSC1_N	OSC0	6
5	PIOB[9]/ XCAS_N	PIOB[7]/ PWMOUT 1	PIOB[10]/ XRAS_N	XBS_N[1]						GND_IO	EXINT3	GND_ CORE	RESET_N	5
4	PIOB[12]/ XSDCS_N	PIOB[8]/ XWAIT	PIOB[11]/ XSDCLK	VDD_IO	TCK	PIOA[2]/ CTS	PIOA[5]/ DTR	VDD_ CORE	AIN[0]	AIN[7]	EXINT0	EFIQ_N	EXINT2	4
3	NC	PIOB[13]/ XSDCKE	NC	DBGRQ	TDO	PIOA[3]/ DSR	PIOA[6]/ RTS	GND_ CORE	AIN[3]	AIN[4]	PIOA[8]/ STXD	EXINT1	PIOA[9]/ SRXD	3
2	NC	GND_IO	DBGACK	nTRST	TBE	PIOA[1]/ SOUT	PIOA[4]/ DCD	NC	AVDD	AIN[1]	AIN[6]	NC	MODE[2]	2
1	NC	PIOB[14]/ XDQM[1]/ XCAS_N[1]	PIOB[15]/ XDQM[0]/ XCAS_N[0]	TDI	TMS	PIOA[0]/ SIN	PIOA[7]/ RI	VREF	AIN[2]	AIN[5]	AGND	MODE[0]	MODE[1]	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Note: NC pins should remain unconnected.

144-Pin Plastic LFBGA

LIST OF PINS

Pin Number		Primary Function			Secondary Function		
TQFP	LFBGA	Pin Name	I/O	Function	Pin Name	I/O	Function
1	B1	PIOB[14]	I/O	General-purpose port (with interrupt function)	XDQM[1]/ XCAS_N[1]	O	I/O mask/CAS (MSB)
2	C1	PIOB[15]	I/O	General-purpose port (with interrupt function)	XDQM[0]/ XCAS_N[0]	O	I/O mask/CAS (LSB)
3	D3	DBGRQ	I	Debugging input signal	—	—	
4	C2	DBGACK	O	Debugging output signal	—	—	
5	D1	TDI	I	JTAG data input	—	—	
6	E3	TDO	O	JTAG data output	—	—	
7	D2	nTRST	I	JTAG reset	—	—	
8	E1	TMS	I	JTAG mode select	—	—	
9	E4	TCK	I	JTAG clock	—	—	
10	E2	TBE	I	Test input signal	—	—	
11	F1	PIOA[0]	I/O	General-purpose port (with interrupt function)	SIN	I	UART Serial Data In
12	F2	PIOA[1]	I/O	General-purpose port (with interrupt function)	SOUT	O	UART Serial Data Out
13	F4	PIOA[2]	I/O	General-purpose port (with interrupt function)	CTS	I	UART Clear To Send
14	F3	PIOA[3]	I/O	General-purpose port (with interrupt function)	DSR	I	UART Set Ready
15	G2	PIOA[4]	I/O	General-purpose port (with interrupt function)	DCD	I	UART Carrier Detect
16	G4	PIOA[5]	I/O	General-purpose port (with interrupt function)	DTR	O	UART Data Terminal Ready
17	G3	PIOA[6]	I/O	General-purpose port (with interrupt function)	RTS	O	UART Request To Send
18	G1	PIOA[7]	I/O	General-purpose port (with interrupt function)	RI	I	UART Ring Indicator
19	H3	GND_CORE	GND	Core ground	—	—	
20	H4	VDD_CORE	VDD	Core power supply	—	—	
21	J2	AVDD	VDD	Analog-to-digital converter power supply	—	—	
22	H1	VREF	I	Analog-to-digital converter reference voltage	—	—	
23	J4	AIN[0]	I	Analog-to-digital converter analog input	—	—	
24	K2	AIN[1]	I	Analog-to-digital converter analog input	—	—	
25	J1	AIN[2]	I	Analog-to-digital converter analog input	—	—	
26	J3	AIN[3]	I	Analog-to-digital converter analog input	—	—	
27	K3	AIN[4]	I	Analog-to-digital converter analog input	—	—	
28	K1	AIN[5]	I	Analog-to-digital converter analog input	—	—	
29	L2	AIN[6]	I	Analog-to-digital converter analog input	—	—	
30	K4	AIN[7]	I	Analog-to-digital converter analog input	—	—	
31	L1	AGND	GND	GND for A/D converter	—	—	
32	M1	MODE[0]	I	Mode setting	—	—	
33	N1	MODE[1]	I	Mode setting	—	—	
34	N2	MODE[2]	I	Mode setting	—	—	

Pin Number		Primary Function			Secondary Function		
TQFP	LFBGA	Pin Name	I/O	Function	Pin Name	I/O	Function
35	L3	PIOA[8]	I/O	General-purpose port (with interrupt function)	STXD	O	SIO transmit data output
36	N3	PIOA[9]	I/O	General-purpose port (with interrupt function)	SRXD	I	SIO receive data input
37	L4	EXINT0	I	Interrupt input	—	—	
38	M3	EXINT1	I	Interrupt input	—	—	
39	N4	EXINT2	I	Interrupt input	—	—	
40	L5	EXINT3	I	Interrupt input	—	—	
41	M4	EFIQ_N	I	FIQ input	—	—	
42	N5	RESET_N	I	Reset input	—	—	
43	K5	GND_IO	GND	I/O ground	—	—	
44	M5	GND_CORE	GND	Core ground	—	—	
45	N6	OSC0	I	Oscillator input	—	—	
46	M6	OSC1_N	O	Oscillator output	—	—	
47	L6	VDD_CORE	VDD	Core power supply	—	—	
48	K7	XD[0]	I/O	External data bus	—	—	
49	L7	XD[1]	I/O	External data bus	—	—	
50	L8	XD[2]	I/O	External data bus	—	—	
51	K8	XD[3]	I/O	External data bus	—	—	
52	M8	XD[4]	I/O	External data bus	—	—	
53	M9	XD[5]	I/O	External data bus	—	—	
54	N8	XD[6]	I/O	External data bus	—	—	
55	K9	XD[7]	I/O	External data bus	—	—	
56	M10	GND_IO	GND	I/O ground	—	—	
57	N9	XD[8]	I/O	External data bus	—	—	
58	L9	XD[9]	I/O	External data bus	—	—	
59	L10	XD[10]	I/O	External data bus	—	—	
60	N10	XD[11]	I/O	External data bus	—	—	
61	M11	VDD_IO	VDD	I/O power supply	—	—	
62	K10	XD[12]	I/O	External data bus	—	—	
63	N11	XD[13]	I/O	External data bus	—	—	
64	N12	XD[14]	I/O	External data bus	—	—	
65	M13	XD[15]	I/O	External data bus	—	—	
66	L13	GND_IO	GND	I/O ground	—	—	
67	K11	XA[0]	O	External address output	—	—	
68	L12	XA[1]	O	External address output	—	—	
69	K13	XA[2]	O	External address output	—	—	
70	J11	XA[3]	O	External address output	—	—	
71	K12	XA[4]	O	External address output	—	—	
72	J13	XA[5]	O	External address output	—	—	
73	J10	XA[6]	O	External address output	—	—	
74	J12	XA[7]	O	External address output	—	—	
75	H13	XA[8]	O	External address output	—	—	

Pin Number		Primary Function			Secondary Function		
TQFP	LFBGA	Pin Name	I/O	Function	Pin Name	I/O	Function
76	H12	GND_IO	GND	I/O ground	—	—	
77	H10	VDD_IO	VDD	I/O power supply	—	—	
78	H11	XA[9]	O	External address output	—	—	
79	G12	XA[10]	O	External address output	—	—	
80	G10	XA[11]	O	External address output	—	—	
81	G11	XA[12]	O	External address output	—	—	
82	G13	GND_CORE	GND	Core ground	—	—	
83	F11	VDD_CORE	VDD	Core power supply	—	—	
84	F10	XA[13]	O	External address output	—	—	
85	F12	XA[14]	O	External address output	—	—	
86	E12	XA[15]	O	External address output	—	—	
87	F13	XA[16]	O	External address output	—	—	
88	E10	XA[17]	O	External address output	—	—	
89	D12	GND_IO	GND	I/O ground	—	—	
90	E13	XA[18]	O	External address output	—	—	
91	E11	PIOA[10]	I/O	General-purpose port (with interrupt function)	XA[19]	O	External address output
92	D11	PIOA[11]	I/O	General-purpose port (with interrupt function)	XA[20]	O	External address output
93	D13	PIOA[12]	I/O	General-purpose port (with interrupt function)	XA[21]	O	External address output
94	C12	VDD_IO	VDD	I/O power supply	—	—	
95	D10	PIOA[13]	I/O	General-purpose port (with interrupt function)	XA[22]	O	External address output
96	B12	PIOA[14]	I/O	General-purpose port (with interrupt function)	XA[23]	O	External address output
97	A12	PIOA[15]	I/O	General-purpose port (with interrupt function)	XWR	O	External bus data transfer direction
98	A11	XOE_N	O	Output enable (except SDRAM)	—	—	
99	C10	XWE_N	O	Write enable	—	—	
100	B11	GND_IO	GND	I/O ground	—	—	
101	A10	XBWE_N[0]	O	Write enable (LSB)			
102	C9	XBWE_N[1]	O	Write enable (MSB)	—	—	
103	B10	XROMCS_N	O	External ROM chip select	—	—	
104	A9	XRAMCS_N	O	External RAM chip select	—	—	
105	D9	XIOCS_N[0]	O	I/O bank 0 chip select	—	—	
106	B9	XIOCS_N[1]	O	I/O bank 1 chip select	—	—	
107	A8	GND_CORE	GND	Core ground	—	—	
108	B8	VDD_CORE	VDD	Core power supply	—	—	
109	D8	PIOB[0]	I/O	General-purpose port (with interrupt function)	DREQ0	I	DMA request signal (Ch 0)
110	C8	PIOB[1]	I/O	General-purpose port (with interrupt function)	DREQCLR0	O	DREQ clear signal (Ch 0)
111	B7	VDD_IO	VDD	I/O power supply	—	—	

Pin Number		Primary Function			Secondary Function		
TQFP	LFBGA	Pin Name	I/O	Function	Pin Name	I/O	Function
112	D7	PIOB[2]	I/O	General-purpose port (with interrupt function)	DREQ1	I	DMA request signal (Ch 1)
113	C7	PIOB[3]	I/O	General-purpose port (with interrupt function)	DREQCLR1	O	DREQ clear signal (Ch 1)
114	A7	PIOB[4]	I/O	General-purpose port (with interrupt function)	TCOUT0	O	DMA Termination Signal (CH 0)
115	C6	PIOB[5]	I/O	General-purpose port (with interrupt function)	TCOUT1	O	DMA Termination Signal (CH 1)
116	D6	GND_IO	GND	I/O ground	—	—	
117	B6	PIOB[6]	I/O	General-purpose port (with interrupt function)	PWMOUT0	O	PWM output (Ch 0)
118	B5	PIOB[7]	I/O	General-purpose port (with interrupt function)	PWMOUT1	O	PWM output (Ch 1)
119	A6	XBS_N[0]	O	External bus byte select (LSB)	—	—	
120	D5	XBS_N[1]	O	External bus byte select (MSB)	—	—	
121	B4	PIOB[8]	I/O	General-purpose port (with interrupt function)	XWAIT	I	WAIT input for IO bank 0
122	A5	PIOB[9]	I/O	General-purpose port (with interrupt function)	XCAS_N	O	Column address strobe (SDRAM)
123	C5	PIOB[10]	I/O	General-purpose port (with interrupt function)	XRAS_N	O	Row address strobe (SDRAM/EDO)
124	C4	PIOB[11]	I/O	General-purpose port (with interrupt function)	XSDCLK	O	SDRAM clock
125	A4	PIOB[12]	I/O	General-purpose port (with interrupt function)	XSDCS_N	O	SDRAM chip select
126	B3	PIOB[13]	I/O	General-purpose port (with interrupt function)	XSDCKE	O	Clock enable (SDRAM)
127	D4	VDD_IO	VDD	I/O power supply	—	—	
128	B2	GND_IO	GND	I/O ground	—	—	

Note: A1, C3, H2, M2, K6, M7, N7, M12, N13, L11, C13, B13, A13, C11, A3, A2 pins of LFBGA packaged version are NC pins. These pins must remain unconnected.

PIN DESCRIPTION

Pin Name	I/O	Description	Primary/ Secondary	Logic
System				
RESET_N	I	Reset input	—	Negative
OSC0	I	Crystal oscillator connection or external clock input. Connect a crystal oscillator (16 MHz to 33 MHz), if used, to OSC0 and OSC1_N.	—	
OSC1_N	O	Crystal oscillator connection. Leave this pin unconnected if using external clock input.	—	
TBE	I	Test pin. Drive at High level.	—	Negative
Debugging support				
DBGRQ	I	Debugging pin. Normally connect to ground.	—	Positive
DBGACK	O	Debugging pin. Normally leave open.	—	Positive
TCK	I	Debugging pin. Normally connect to ground.	—	—
TMS	I	Debugging pin. Normally drive at High level.	—	Positive
nTRST	I	Debugging pin. Normally connect to ground.	—	Negative
TDI	I	Debugging pin. Normally drive at High level.	—	Positive
TDO	O	Debugging pin. Normally leave open.	—	Positive
General-purpose I/O ports				
PIOA[15:0]	I/O	General-purpose port. Not available for use as port pins when secondary functions are in use.	Primary	Positive
PIOB[15:0]	I/O	General-purpose port. Not available for use as port pins when secondary functions are in use. Note that enabling DRAM controller with MODE[2:0] inputs permanently configures PIOB[15:9] for their secondary functions, making them unavailable for use as port pins.	Primary	Positive

Pin Name	I/O	Description	Primary/ Secondary	Logic
External bus				
XA[23:19]	O	Address bus to external RAM, external ROM, external I/O banks, and external DRAM. After a reset, these pins are configured for their primary function (PIOA[14:10]).	Secondary	Positive
XA[18:0]	O	Address bus to external RAM, external ROM, external I/O banks, and external DRAM	—	Positive
XD[15:0]	I/O	Data bus to external RAM, external ROM, external I/O banks, and external DRAM	—	Positive
External bus control signals				
XROMCS_N	O	ROM bank chip select	—	Negative
XRAMCS_N	O	SRAM bank chip select	—	Negative
XIOCS_N[0]	O	I/O bank 0 chip select	—	Negative
XIOCS_N[1]	O	I/O bank 1 chip select	—	Negative
XOE_N	O	Output enable/read enable	—	Negative
XWE_N	O	Write enable	—	Negative
XBS_N[1:0]	O	Byte select: XBS_N[1] for MSB; XBS_N[0] for LSB	—	Negative
XBWE_N[0]	O	LSB write enable	—	Negative
XBWE_N[1]	O	MSB write enable	—	Negative
XWR	O	Data transfer direction for external bus, used when connecting to Motorola I/O devices. This represents the secondary function of pin PIOA[15], produced by setting bit 7 in the port control (GPCTL) register to "1."	Secondary	—
XWAIT	I	External I/O bank 0 WAIT signal. This input permits access to devices slower than register settings.	Secondary	Positive
External bus control signals (DRAM)				
XRAS_N	O	Row address strobe. Used for both EDO DRAM and SDRAM.	Secondary	Negative
XCAS_N	O	Column address strobe signal (SDRAM)	Secondary	Negative
XSDCLK	O	SDRAM clock (same frequency as internal system clock)	Secondary	—
XSDCKE	O	Clock enable (SDRAM)	Secondary	—
XSDCS_N	O	Chip select (SDRAM)	Secondary	Negative
XDQM[1]/ XCAS_N[1]	O	Connected to SDRAM: DQM (MSB) Connected to EDO DRAM: column address strobe signal (MSB)	Secondary	Positive/ Negative
XDQM[0]/ XCAS_N[0]	O	Connected to SDRAM: DQM (LSB) Connected to EDO DRAM: column address strobe signal (LSB)	Secondary	Positive/ Negative

Pin Name	I/O	Description	Primary/ Secondary	Logic
DMA control signals				
DREQ0	I	Ch 0 DMA request signal, used when DMA controller configured for DREQ type	Secondary	Positive
DREQCLR0	O	Ch 0 DREQ signal clear request. The DMA device responds to this output by negating DREQ.	Secondary	Positive
TCOUT0	O	Indicates to Ch 0 DMA device that last transfer has started	Secondary	Positive
DREQ1	I	Ch 1 DMA request signal, used when DMA controller configured for DREQ type	Secondary	Positive
DREQCLR1	O	Ch 1 DREQ signal clear request. The DMA device responds to this output by negating DREQ.	Secondary	Positive
TCOUT1	O	Indicates to Ch 1 DMA device that last transfer has started	Secondary	Positive
Serial IO Interface				
STXD	O	SIO transmit signal	Secondary	Positive
SRXD	I	SIO receive signal	Secondary	Positive
UART				
SIN	I	Serial data input	Secondary	Positive
SOUT	O	Serial data output	Secondary	Positive
CTS	I	Clear To Send. Indicates that modem or data set is ready to transfer data. Bit 4 in modem status register reflects this input.	Secondary	Negative
DSR	I	Data Set Ready. Indicates that modem or data set is ready to establish a communications link with UART. Bit 5 in modem status register reflects this input.	Secondary	Negative
DCD	I	Data Carrier Detect. Indicates that modem or data set has detected data carrier signal. Bit 7 in modem status register reflects this input.	Secondary	Negative
DTR	O	Data Terminal Ready. Indicates that UART is ready to establish a communications link with modem or data set. Bit 0 in modem control register controls this output.	Secondary	Negative
RTS	O	Request To Send. Indicates that UART is ready to transfer data to modem or data set. Bit 1 in modem control register controls this output.	Secondary	Negative
RI	I	Ring Indicator. Indicates that modem or data set has received telephone ring indicator. Bit 6 in modem status register reflects this input.	Secondary	Negative

Pin Name	I/O	Description	Primary/ Secondary	Logic
PWM signals				
PWMOUT0	O	Ch 0 PWM output	Secondary	Positive
PWMOUT1	O	Ch 1 PWM output	Secondary	Positive
Analog-to-digital converter				
AIN[0]	I	Ch 0 analog input	—	
AIN[1]	I	Ch 1 analog input	—	
AIN[2]	I	Ch 2 analog input	—	
AIN[3]	I	Ch 3 analog input	—	
AIN[4]	I	Ch 4 analog input	—	
AIN[5]	I	Ch 5 analog input	—	
AIN[6]	I	Ch 6 analog input	—	
AIN[7]	I	Ch 7 analog input	—	
VREF	I	Analog-to-digital converter convert reference voltage	—	
AVDD		Analog-to-digital converter power supply	—	
AGND		Analog-to-digital converter ground	—	
Interrupt signals				
EXINT3 EXINT2 EXINT1 EXINT0	I	External interrupt input signals	—	Positive/ Negative
EFIQ_N	I	External fast interrupt input signal. Interrupt controller connects this to CPU FIQ input.	—	Negative
Mode				
MODE[2:0]	I	Operating mode control signals	—	
Power supplies				
VDD_CORE	—	Core power supply	—	
VDD_IO	—	I/O power supply	—	
GND_CORE	—	Core ground	—	
GND_IO	—	I/O ground	—	

FUNCTIONAL DESCRIPTION

CPU

CPU core:	ARM7TDMI
Operating frequency:	1 MHz to 33 MHz
Instructions:	ARM instruction (32-bit length) and Thumb instruction (16-bit length) can be mixed.
General register bank:	31 x 32 bits
Built-in barrel shifter:	ALU and barrel shift operations can be executed by one instruction.
Multiplier:	32 bits x 8 bits (Modified Booth's Algorithm)
Built-in debug function:	JTAG interface, break point register

Built-in Memory

RAM: 8 KB (2K x 32 bits)
Connected to processor bus (read: 1 cycle access, write: 2 cycle access)

Interrupt Controller

Fast interrupt input (FIQ) and interrupt input (IRQ) are used as interrupt input signals of ARM core. The interrupt controller controls these interrupt signals to the ARM core.

(1) Interrupt sources of ML674000
FIQ: 1 source, external source (external pin: EFIQ_N)
IRQ: 23 sources, internal sources: 19, external sources: 4 (external pins: EXINT[3:0])
(2) Interrupt priority level
Priority can be set in 8 levels for each source.
(3) External interrupt pin input
Level sense: Interrupt signal level is selected.
Edge sense: Rising or falling is selected.
(4) External fast interrupt pin input
Edge sense: Falling edge is detected.

Timer

7 channels of 16-bit reload timers are used. Of these, 1 channel is used as system timer for the OS.
The timers of the other 6 channels are used in application software.

(1) System timer: 1 channel
16-bit auto reload timer: Used as system timer for OS
(This timer is incorporated in µPLAT-7B.)
Interval mode
(2) Application timer: 6 channels
16-bit auto reload timer
One shot, interval mode
Clock can be set for each channel

WDT

This MCU contains a Watch Dog Timer that can function as an interval timer.

(1) 16-bit timer
(2) Watch dog timer or interval timer mode can be selected
(3) Interrupt or reset generation
- Watchdog timer mode: generates reset or interrupt when the timer overflows.
- Interval timer mode: generates interrupt when the timer reaches an overflow condition.
(4) Maximum period: 200 msec or longer

PWM

This MCU contains two PWM (Pulse Width Modulation) channels which can change duty cycle within a certain fixed period. The PWM output resolution is 16 bits for each channel.

Serial Interface

This MCU contains two channels of serial interface.

(1) UART without FIFO: 1 channel
This serial interface is incorporated in µPLAT-7B.
(2) UART with 16-byte FIFO: 1 channel
This is ACE (Asynchronous Communication Element) equivalent in function to 16550A. It has 16-byte FIFO in both sending and receiving.

GPIO

This MCU contains two 16-bit parallel ports.

(1) Input or output can be selected for each bit.
(2) Interrupt can be used for all 16 bits of each channel, and both GPIO channels can be used as an interrupt input.
(3) Interrupt mask and interrupt mode (level) can be set for all bits.
(4) Configured as inputs immediately after reset.

AD Converter

This is a successive approximation type AD converter.

(1) 10 bits x 8 channels
(2) Sample and hold function
(3) Scan mode and select mode are supported
(4) Interrupt is generated after completion of conversion.
(5) Conversion time: 5 µs (min).

DMAC

This MCU contains a two channel direct memory access controller which transfers data between memory and memory, between I/O and memory, and between I/O and I/O.

(1) Number of channels: 2 channels
(2) Channel priority level: Fixed mode
Channel priority level is always fixed (channel 0 > 1).
Round-robin
Priority level of the channel requested for transfer is kept lowest.
(3) Maximum number of transfers: 65,536 times (64K times)
(4) Data transfer size: Byte (8 bits), half-word (16 bits), word (32 bits)
(5) Bus request system: Cycle steal mode: Bus request signal is asserted for each DMA transfer cycle.
Burst mode: Bus request signal is asserted until all transfers of transfer cycles are complete.
(6) DMA transfer request: Software request: By setting the software transfer request bit within DMAC, the CPU starts DMA transfer.
External request: DMA transfer is started by external request allocated to each channel.
(7) Interrupt request: Interrupt request is generated in CPU after the end of DMA transfers for the set number of transfer cycles or after occurrence of error.
Interrupt request signal is output separately for each channel.
Interrupt request signal output can be masked for each channel.

External Memory Controller

Controls access of externally connected devices such as ROM (FLASH), SRAM, SDRAM (EDO DRAM), and IO devices.

(1) ROM (FLASH) access function
Supports 16-bit device
Supports FLASH memory: Byte write (can be written only by IF equivalent to SRAM).
Access timing setting
(2) SRAM access function
Supports 16-bit device
Supports asynchronous SRAM
Access timing setting
(3) DRAM access function
Supports 16-bit device
Supports EDO/SDRAM: Simultaneous connections to EDO-DRAM and SDRAM are not supported.
Access timing setting
(4) External IO access function
Supports 8-bit/16-bit device
Supports 2 banks independently
Supports external wait input: XWAIT (IO bank 0 only)
Access timing setting (for each bank)

Power Management

HALT and STANDBY functions are supported as power save functions.

(1) HALT mode
HALT object
CPU, internal RAM, AHB bus control
HALT mode setting: Set by the system control register.
HALT mode cancelling: Reset, interrupt
(2) STANDBY mode
Stops the clock of entire MCU.
STANDBY mode setting: Specified by the system control register.
STANDBY mode cancelling: Reset, external interrupt (other than FIQ)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Conditions	Rating	Unit
Digital power supply voltage (core)	V_{DD_CORE}	GND = AGND = 0 V Ta = 25°C	–0.3 to +3.6	V
Digital power supply voltage (I/O)	V_{DD_IO}		–0.3 to +4.6	
Input voltage	V_I		–0.3 to V_{DD_IO}+0.3	
Output voltage	V_O		–0.3 to V_{DD_IO}+0.3	
Analog power supply voltage	AV_{DD}		–0.3 to V_{DD_IO}+0.3	
Analog reference voltage	V_{REF}		–0.3 to V_{DD_IO}+0.3 and –0.3 to AV_{DD} +0.3	
Analog input voltage	V_{AI}		–0.3 to V_{REF}	
Input current	I_I		–10 to +10	mA
High level output current	I_{OH}		+10	
Low level output current [1]	I_{OL}		–20	
Low level output current [2]			–30	
Power dissipation	P_D	Ta = 85°C per package	530	mW
Storage temperature	T_{STG}	—	–50 to +150	°C

Notes

1. All output pins except XA[15:0]
2. XA[15:0]

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Item	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Digital power supply voltage (core)	V_{DD_CORE}	$V_{DD\_IO} \geq V_{DD\_CORE}$	2.25	2.5	2.75	V
Digital power supply voltage (I/O)	V_{DD_IO}		3.0	3.3	3.6	
Analog power supply voltage	AV_{DD}	$A_{VDD} = V_{DD\_IO}$	3.0	3.3	3.6	
Analog reference voltage	V_{REF}	$V_{REF} = A_{VDD} = V_{DD\_IO}$	3.0	3.3	3.6	
Storage hold voltage	V_{DDH}	f_{OSC} = 0 Hz	2.25	—	3.6	
Operating frequency	f_{OSC}	V_{DD_CORE} = 2.25 to 2.75 V_{DD_IO} = 3.0 to 3.6 [1]	1	—	33.333	MHz
Ambient temperature	Ta	—	–40	25	+85	°C

Note

1. Oscillator frequencies between 16 MHz and 33 MHz. Minimum of 2.56 MHz for external SDRAM. Minimum of 6.4 MHz for external EDO DRAM. Minimum of 2 MHz for analog-to-digital converter.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD_CORE} = 2.25 to 2.75 V, V_{DD_IO} = 3.0 to 3.6 V, Ta = –40 to +85°C)

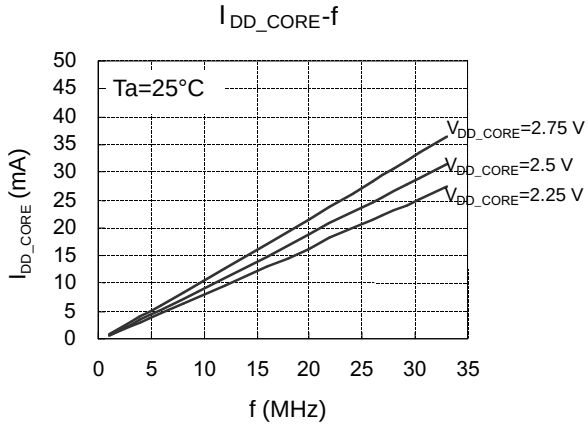
Item	Symbol	Conditions	Minimum	Typical	Maximum	Unit
High level input voltage	V_{IH}	—	2.0	—	V_{DD_IO}+0.3	V
Low level input voltage	V_{IL}		–0.3	—	0.8	
Schmitt input buffer threshold voltage	V_{T+}		—	1.6	2.1	
	$V_{T\_}$		0.7	1.1	—	
	V_{HYS}		0.4	0.5	—	
High level output voltage	V_{OH}	I_{OH} = –100 µA	V_{DD}–0.2	—	—	
		I_{OH} = –4 mA	2.4	—	—	
Low level output voltage	V_{OL}	I_{OL} = 100 µA	—	—	0.2	
Low level output voltage [1]		I_{OL} = 4 mA	—	—	0.4	
Low level output voltage [2]		I_{OL} = 6 mA	—	—	0.4	
Input leak current [3]	I_{IH}/I_{IL}	V_I = 0 V/V_{DD_IO}	–10	—	10	µA
Input leak current [4]		V_I = 0 V Pull-up resistance of 50 kΩ	10	66	200	
Output leak current	I_{LO}	V_O = 0 V/V_{DD_IO}	–10	—	10	
Input pin capacitance	C_I	—	—	6	—	pF
Output pin capacitance	C_O	—	—	9	—	
I/O pin capacitance	C_{IO}	—	—	10	—	
Analog reference power supply current	I_{REF}	Analog-to-digital converter operative [5]	—	320	650	µA
		Analog-to-digital converter stopped	—	1	2	
Current consumption (STANDBY)	I_{DDS_CORE}	Ta = 25°C [6]	—	3	45	µA
	I_{DDS_IO}		—	1	5	
Current consumption (HALT) [7]	I_{DDH_CORE}	f_{OSC} = 16 MHz C_L = 50 pF	—	8	15	mA
	I_{DDH_IO}		—	2	5	
Current consumption (RUN)	I_{DD_CORE}		—	15	25	mA
	I_{DD_IO}		—	18	30	

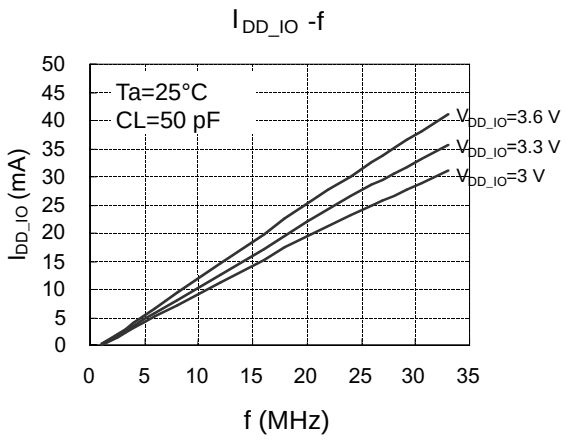
Notes

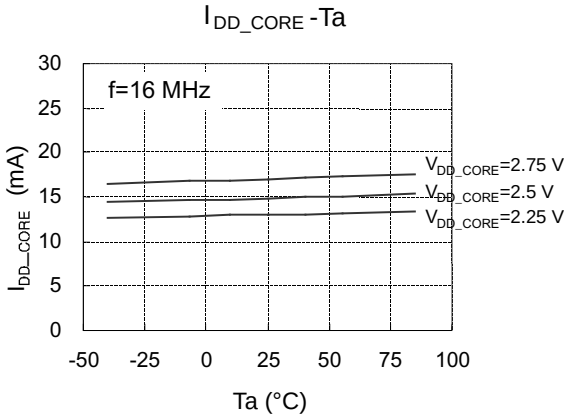
1. All output pins except XA[15:0]
2. XA[15:0]
3. All input pins except RESET_N
4. RESET_N pin, with 50 k_ pull-up resistance
5. Analog-Digital Converter operation ratio is 20%
6. V_{DD_IO} or 0 V for input ports; no load for other pins
7. DRAM function stop by MODE pin setting

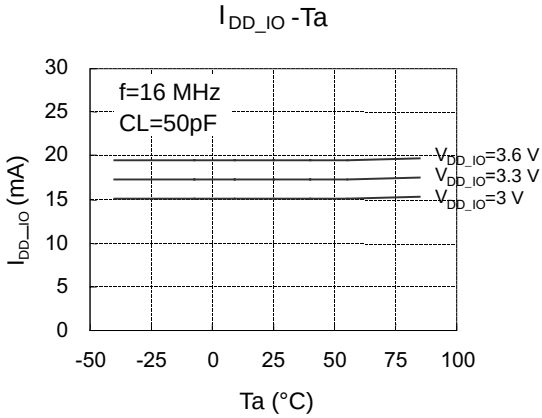
Power Consumption

The values in the following charts are measured values in the operating conditions indicated.
The samples were taken during normal operation in ARM mode with all peripheral clocks activated. Instructions were being executed from external memory.









Analog-to-Digital Converter Characteristics

(V_{DD_CORE} = 2.50 V, V_{DD_IO} = 3.3 V, Ta = 25°C)

Item	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Resolution	n	—	—	—	10	bit
Linearity error	E_L	Analog input source impedance Ri ≤ 1kΩ	—	±3	—	LSB
Differential linearity error	E_D		—	±3	—	
Zero scale error	E_{ZS}		—	±3	—	
Full scale error	E_{FS}		—	±3	—	
Conversion time	t_{CONV}	—	5	—	—	µs
Throughput		—	10	—	200	kHz

Note: VDD_IO and AVDD should be supplied separately.

- Definition of Terms

(1) Resolution: Minimum input analog value recognized. For 10-bit resolution, this is (VREF – Aground) ÷ 1024.

(2) Linearity error: Difference between the theoretical and actual conversion characteristics. (Note that it does not include quantization error.) The theoretical conversion characteristic divides the voltage range between VREF and AGND into 1024 equal steps.

(3) Differential linearity error: Difference between the theoretical and actual input voltage change producing a 1-bit change in the digital output anywhere within the conversion range. This is an indicator of conversion characteristic smoothness. The theoretical value is (VREF – Aground) ÷ 1024.

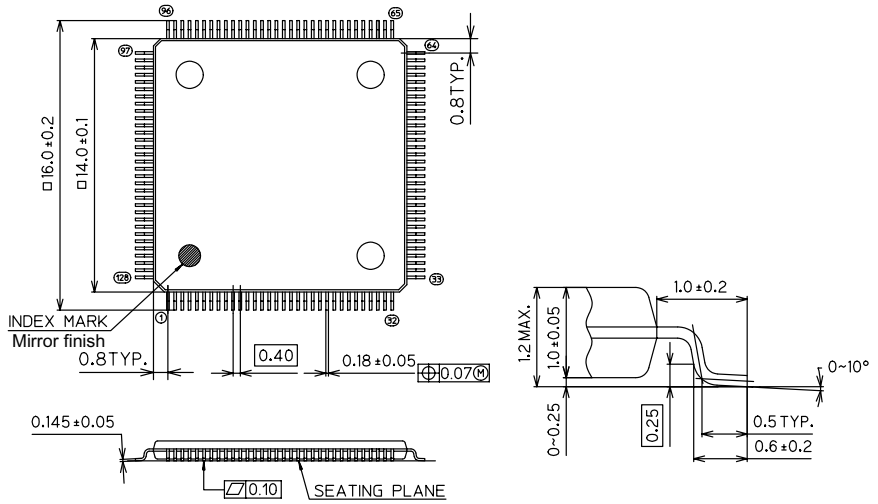
(4) Zero scale error: Difference between the theoretical and actual conversion characteristics at the point where the digital output switches from “0x000” to “0x001.”

(5) Full scale error: Difference between the theoretical and actual conversion characteristics at the point where the digital output switches from “0x3FE” to “0x3FF.”

PACKAGE DIMENSIONS

(Unit : mm)

TQFP128-P-1414-0.40-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	1/Nov. 18, 1999

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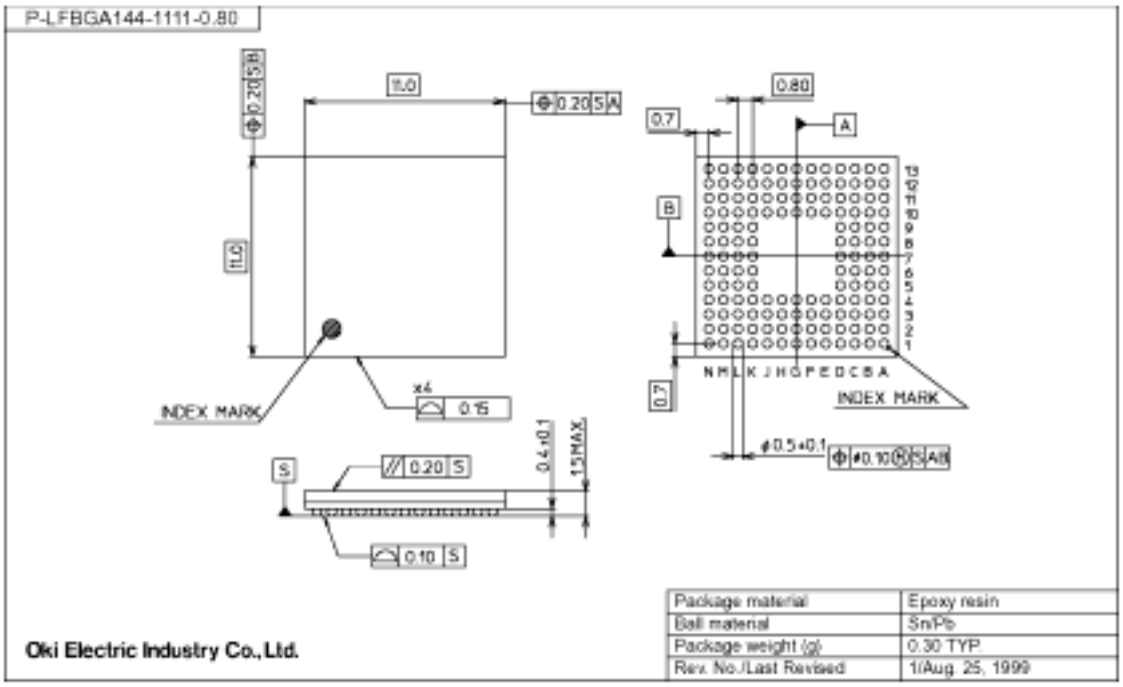

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact an Oki sales person for the product name, package name, pin number, package code, and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL674000-01	Oct., 2001	–	–	Preliminary edition 1
PEDL674000-02	May 17, 2002	–	–	Preliminary edition 2
		1	1	Feature Table rewritten.
		2-13	2-12	Pin names are changed.
		14-16	13-15	Description rewritten.
		17	16-37	Electrical characteristics added.
FEDL674000-01	Aug. 8, 2002	–	–	Final edition 1
		1	1	Number of interrupt sources corrected.
		8	8	TBE signal description corrected.
		8	8	Pin numbers of XA[23:19] and XA[18:0] corrected.
		15-36	15-50	Description rewritten.
FEDL674000-02	Nov. 8, 2002	–	–	Final edition 2
		1	1 to 2	Description changed. Add 144-pin LFBGA package.
		–	5	Add Pin layout for LFBGA package.
		4 to 7	6 to 9	Change table of pin list.(Add LFBGA description and correct some descriptions.)
		8 to 11	10 to 13	Change table of pin description. (Correct some descriptions.)
		12 to 14	14 to 16	Description changed.
		18 to 50	–	Description of AC characteristics Deleted. Please refer to User's Manual.
		51	21	The values of Zero scale error and Full scale error of Analog-to-Digital converter are corrected.
		–	23	Add Package Dimensions for LFBGA package.
FEDL674000-02.1 320307-003	Dec. 20, 2002	1	1	Description enhancement, addition of Features and Applications sections
		1	2	Enhancement and name change of Specification Overview section
		–	–	Miscellaneous non-technical or typographical enhancements.

Notes:

The information contained herein can change without notice owing to product and/or technical improvements.

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