Poly Phase Multifunction Energy Metering IC with Neutral Current Measurement

Preliminary Technical Data

ADE7854

FEATURES

Highly accurate; supports EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-22 and IEC 62053-23
Compatible with 3-phase, 3 or 4 wire (delta or wye) and other 3-phase services
Supplies total active / apparent energy on each phase and on the overall system
Less than 0.1% error in active energy over a dynamic range of 1000 to 1 at 25°C
Less than 0.2% error in active energy over a dynamic range of 3000 to 1 at 25°C
Supports current transformer and di/dt current sensors
Less than 0.1% error in voltage and current rms over a dynamic range of 1000 to 1 at 25°C
Supplies sampled waveform data on all 3 phases
Selectable No-load threshold level for total active powers and for apparent powers
Phase angle measurements in both current and voltage channels with max 0.3° error
Wide supply voltage operation 2.4 to 3.7V
Reference 1.2 V (drift 10 ppm/°C typ) with external overdrive capability
Single 3.3 V supply
40-Lead Frame Chip Scale (LFCSP) Lead Free Package
Operating temperature -40° to 85°C
Flexible I²C, SPI®, HSDC serial interfaces

GENERAL DESCRIPTION

The ADE7854[1] is a high accuracy, 3-phase electrical energy measurement IC with serial interfaces and three flexible pulse outputs. The ADE7854 incorporates second-order Σ-Δ ADCs, a digital integrator, reference circuitry, and all the signal processing required to perform total active and apparent energy measurement and rms calculations. A fixed function digital signal processor (DSP) executes this signal processing.

The ADE7854 is suitable to measure active and apparent energy in various 3-phase configurations, such as WYE or DELTA services, with both three and four wires. The ADE7854 provides system calibration features for each phase, that is, rms offset correction, phase calibration, and gain calibration. The CF1, CF2 and CF3 logic outputs provide a wide choice of power information: total active power, total apparent power or sum of current rms values.

[1] U.S. Pattents pending.

The ADE7854 has waveform sample registers that allow access to all ADC outputs. The device also incorporates power quality measurements such as short duration low or high voltage detections, short duration high current variations, line voltage period measurement and angles between phase voltages and currents. Two serial interfaces can be used to communicate with the ADE7854 : SPI or I²C while a dedicated high speed interface, HSDC (High Speed Data Capture) port, can be used in conjunction with I²C to provide access to the ADC outputs and real time power information. The ADE7854 has also two interrupt request pins, $\overline{IRQ0}$ and $\overline{IRQ1}$, to indicate that an enabled interrupt event has occurred.

The ADE7854 is available in 40-lead LFCSP lead free package.

Rev. PrC

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

FUNCTIONAL BLOCK DIAGRAM

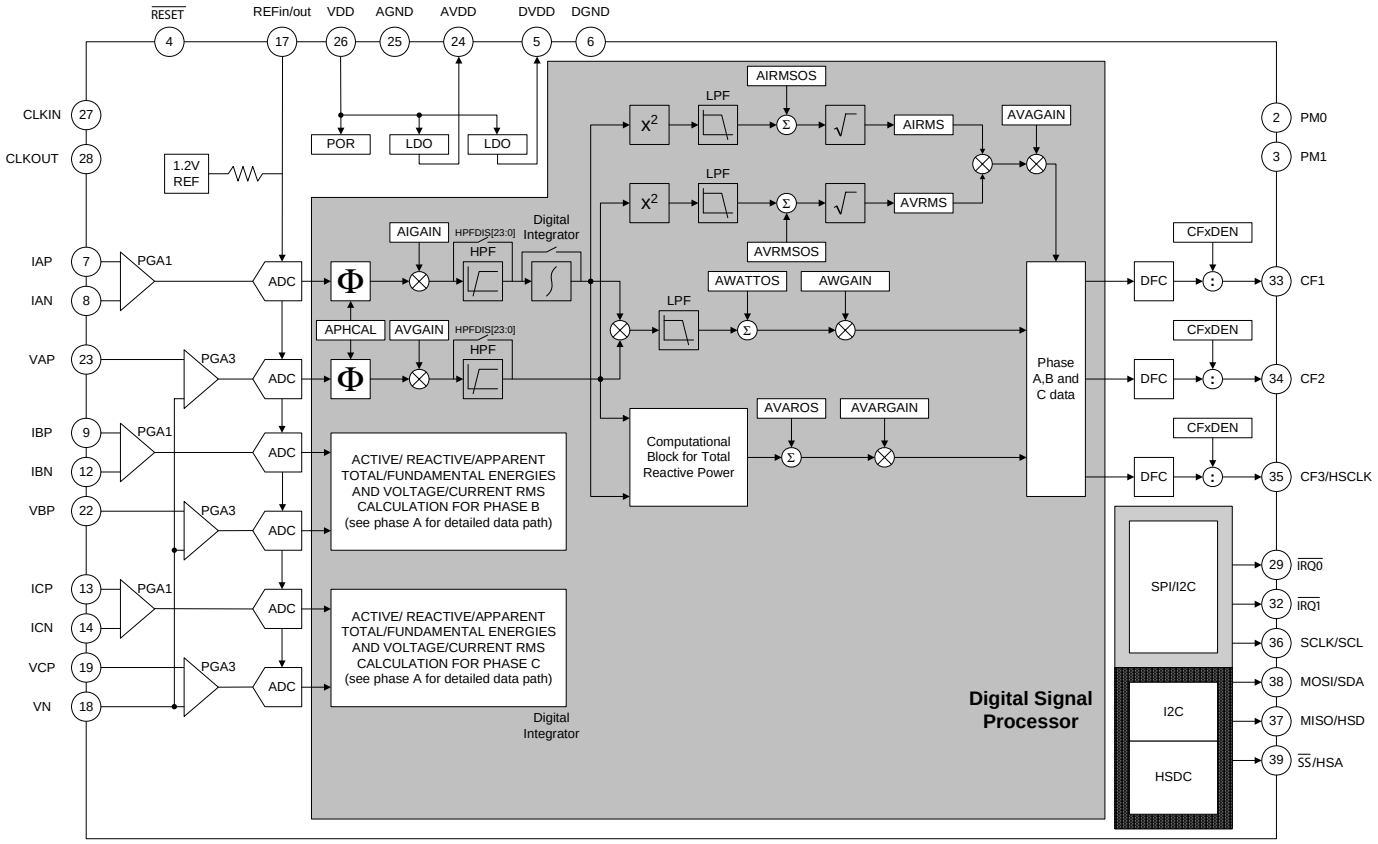

Figure 1. ADE7854 Functional Block Diagram

SPECIFICATIONS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 1.

Parameter[1, 2]	Specification	Unit	Test Conditions/Comments
ACCURACY			
ACTIVE ENERGY MEASUREMENT			
Total Active Energy Measurement Error (per Phase)	0.1	% typ	Over a dynamic range of 1000 to 1, PGA=1
	0.2	% typ	Over a dynamic range of 3000 to 1, PGA=1
Phase Error Between Channels	±0.05	°max	Line frequency = 45 Hz to 65 Hz, HPF on
PF = 0.8 Capacitive	±0.05	°max	Phase lead 37°
PF = 0.5 Inductive			Phase lag 60°
AC Power Supply Rejection			
Output Frequency Variation	0.01	% typ	TBD Conditions
DC Power Supply Rejection			
Output Frequency Variation	0.01	% typ	TBD Conditions
Total Active Energy Measurement Bandwidth	4	kHz typ	
RMS MEASUREMENTS			
IRMS and VRMS Measurement Bandwidth	4	kHz typ	
IRMS and VRMS Measurement Error (PSM0 mode[3])	0.1	% typ	Over a dynamic range of 1000:1, PGA=1
ANALOG INPUTS			
Maximum Signal Levels	±500	mV peak, Max	Differential inputs: IAP-IAN, IBP-IBN, ICP-ICN, INP-INN Single ended inputs: VAP-VN, VBP-VN, VCP-VN
Input Impedance (DC)	400	kΩ min	
ADC Offset Error	±25	mV max	Uncalibrated error, see the Terminology section
Gain Error	±4	% typ	External 1.2 V reference
WAVEFORM SAMPLING			Sampling CLKIN/2048, 16.384 MHz/2048 = 8 kSPS
Current and Voltage Channels			See Waveform Sampling Mode chapter
Signal-to-Noise Ratio	55	dB typ	
Signal-to-Noise Plus Distortion	62	dB typ	
Bandwidth (−3 dB)	4	kHz	
TIME INTERVAL BETWEEN PHASES			
Measurement error	0.3	deg typ	Line frequency = 45 Hz to 65 Hz, HPF on
CF1, CF2, CF3 PULSE OUTPUTS			
Maximum Output Frequency	8	KHz	
Duty Cycle	50	%	If CF1, CF2 or CF3 frequency >6.25Hz
Active Low Pulse Width	80	Msec	If CF1, CF2 or CF3 frequency <6.25Hz
Jitter	0.04	% typ	For CF1, CF2 or CF3 frequency of 1Hz
REFERENCE INPUT			
$REF_{IN/OUT}$ Input Voltage Range	1.3	V max	1.2 V + 8%
	1.1	V min	1.2 V − 8%
Input Capacitance	10	pF max	
ON-CHIP REFERENCE (PSM0 modes)			Nominal 1.2 V at $REF_{IN/OUT}$ pin
Reference Error	±0.9	mV max	
Output Impedance	4	kΩ min	
Temperature Coefficient	10	ppm/°C typ	
	50	ppm/°C max	
CLKIN			All specifications CLKIN of 16.384 MHz
Input Clock Frequency	16.384	MHz max	
Crystal equivalent series resistance	30	KΩ min	

Parameter[1, 2]	Specification	Unit	Test Conditions/Comments
	50	KΩ max	
CLKIN input capacitance	12	pF typ	
CLKOUT output capacitance	12	pF typ	
LOGIC INPUTS—MOSI/SDA, SCLK/SCL, CLKIN and $\overline{SS}$			
Input High Voltage, V_{INH}	2.4	V min	VDD = 3.3 V ± 10%
Input Low Voltage, V_{INL}	0.8	V max	VDD = 3.3 V ± 10%
Input Current, I_{IN}	±3	µA max	Typical 10 nA, V_{IN} = 0 V to VDD
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS— $\overline{IRQ0}$, $\overline{IRQ1}$, MISO/HSDATA, HSCLK and CLKOUT			DVDD = 3.3 V ± 10%
Output High Voltage, V_{OH}	3.0	V min	I_{SOURCE} = 800 µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 2 mA
CF1, CF2, CF3			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 500 µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 2 mA
POWER SUPPLY in PSM0 mode			For specified performance
VDD	3.0	V min	3.3 V – 10%
	3.6	V max	3.3 V + 10%
I_{DD}	TBD	mA typ.	
POWER SUPPLY in PSM3 modes			For specified performance
VDD	2.4	V min	
	3.7	V max	
I_{DD} in PSM3 mode	TBD	µA typ.	

[1] See the Typical Performance Characteristics.
[2] See the Terminology section for a definition of the parameters.
[3] See Power Management chapter for details on various power modes of the ADE7854

TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz , T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 2. I²C Compatible Interface Timing Parameter

Parameter	Symbol	Standard mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition.	$t_{HD;STA}$	4.0		0.6		µs
LOW period of SCL clock	t_{LOW}	4.7		1.3		µs
HIGH period of SCL clock	t_{HIGH}	4.0		0.6		µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7		0.6		µs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data setup time	$t_{SU;DAT}$	250		100		ns
Rise time of both SDA and SCL signals	t_r		1000	20	300	ns
Fall time of both SDA and SCL signals	t_f		300	20	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0		0.6		µs
Bus free time between a STOP and START condition	t_{BUF}	4.7		1.3		µs
Pulse width of suppressed spikes	t_{SP}	na			50	ns

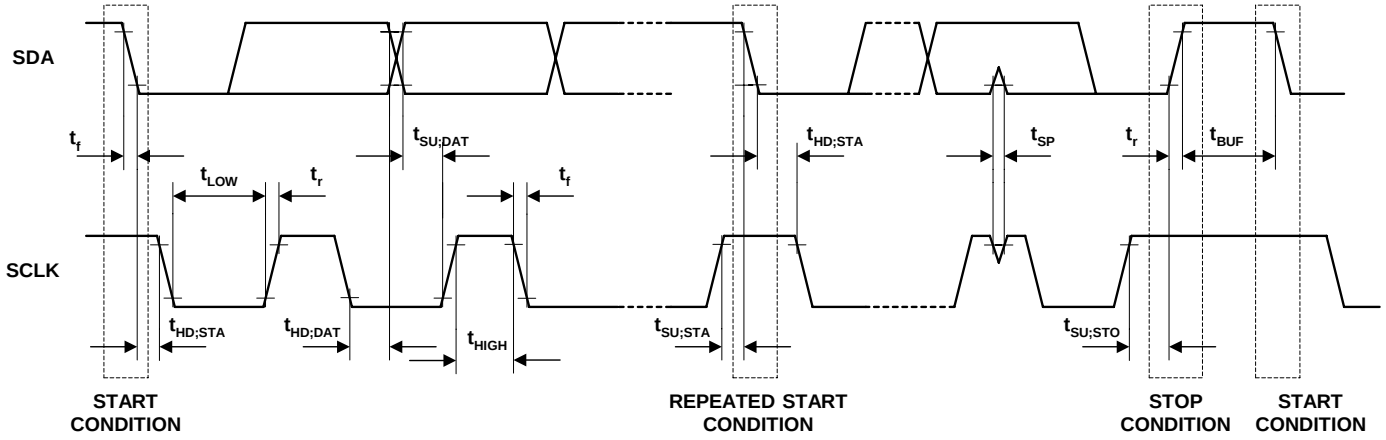

Figure 2. I²C Compatible Interface Timing

Table 3. SPI INTERFACE TIMING Parameter

Parameter	Symbol	Min	Max	Unit
$\overline{SS}$ to SCLK edge	t_{SS}	50		ns
SCLK period		400		ns
SCLK low pulse width	t_{SL}	175		ns
SCLK high pulse width	t_{SH}	175		ns
Data output valid after SCLK edge	t_{DAV}	5	40	ns
Data input setup time before SCLK edge	t_{DSU}	20		ns
Data input hold time after SCLK edge	t_{DHD}	5		ns
Data output fall time	t_{DF}		20	ns
Data output rise time	t_{DR}		20	ns
SCLK rise time	t_{SR}		20	ns
SCLK fall time	t_{SF}		20	ns
MISO disable after $\overline{SS}$ rising edge	t_{DIS}	5	40	ns
$\overline{SS}$ high after SCLK edge	t_{SFS}	0		ns

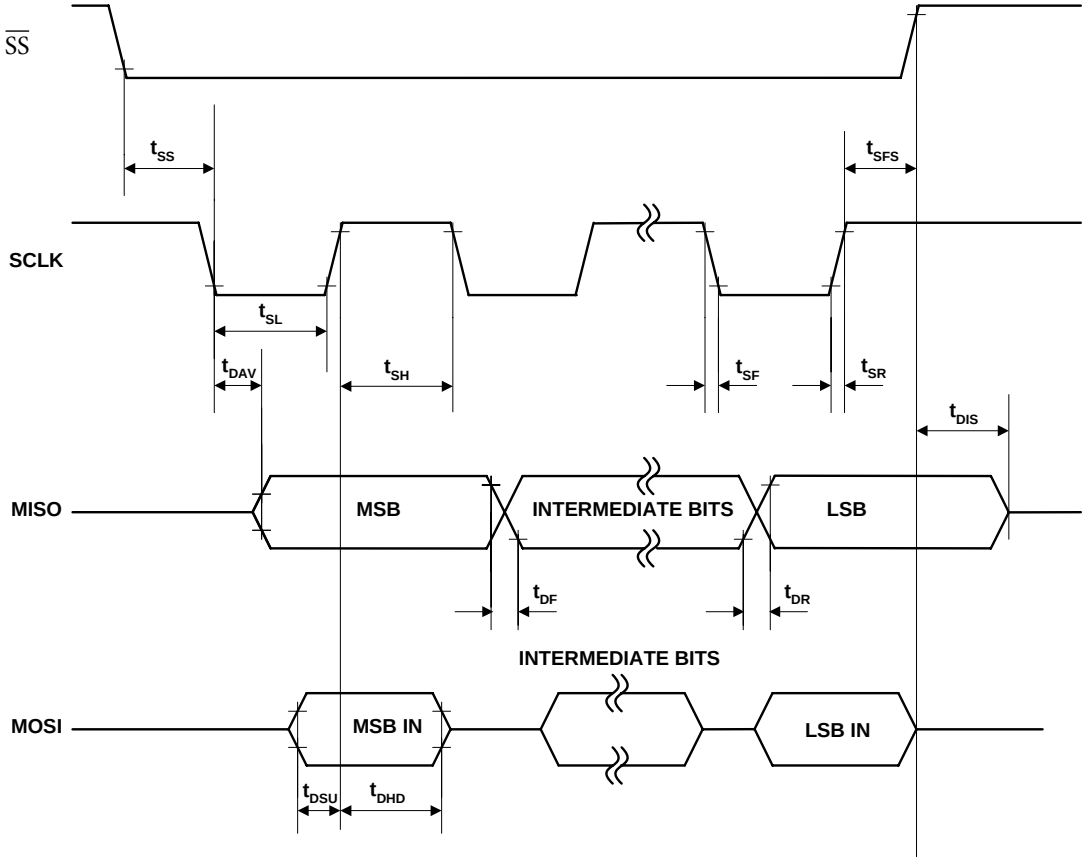

Figure 3. SPI Interface Timing

Table 4. HSDC INTERFACE TIMING Parameter

Parameter	Symbol	Min	Max	Unit
HSA to SCLK edge	t_{SS}	0		ns
HSCLK period		125		
HSCLK low pulse width	t_{SL}	50		ns
HSCLK high pulse width	t_{SH}	50		ns
Data output valid after HSCLK edge	t_{DAV}	5	40	ns
Data output fall time	t_{DF}		20	ns
Data output rise time	t_{DR}		20	ns
HSCLK rise time	t_{SR}		10	ns
HSCLK fall time	t_{SF}		10	ns
HSD disable after HAS rising edge	t_{DIS}	40		ns
HSA high after HSCLK edge	t_{SFS}	0		ns

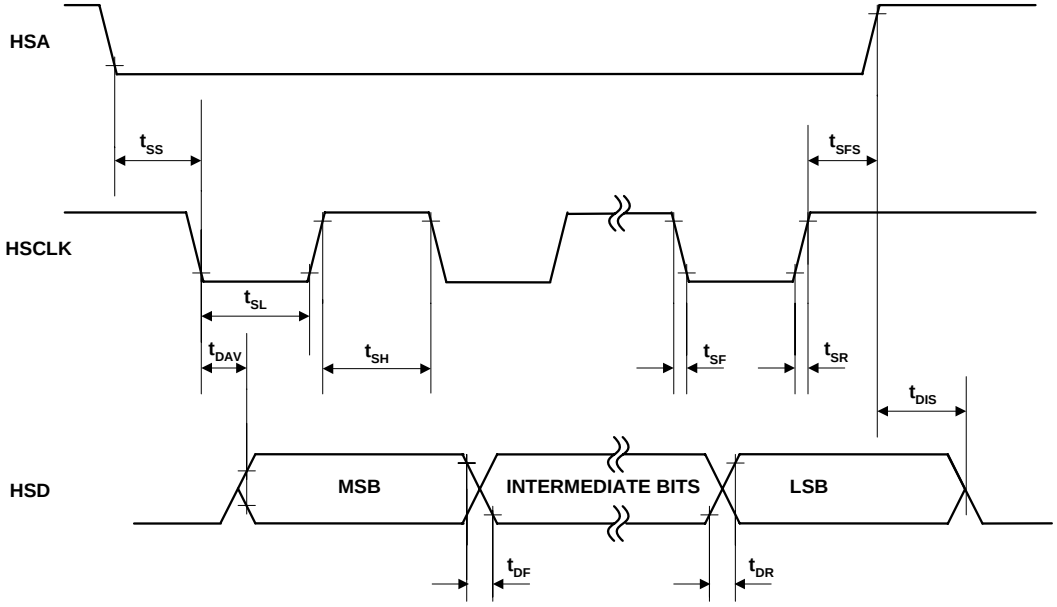

Figure 4. HSDC Interface Timing

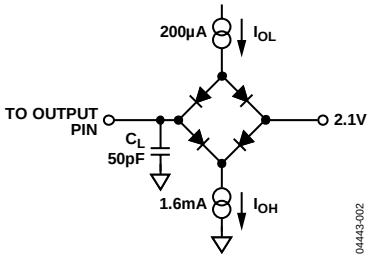

Figure 5. Load Circuit for Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5. Absolute Maximum Ratings

Parameter	Rating
VDD to AGND	–0.3 V to +3.7 V
VDD to DGND	–0.3 V to +3.7 V
Analog Input Voltage to AGND, IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, VCP, VN	–2 V to +2 V
Reference Input Voltage to AGND	–0.3 V to VDD + 0.3 V
Digital Input Voltage to DGND	–0.3 V to VDD + 0.3 V
Digital Output Voltage to DGND	–0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	TBD°C
32-Lead LQFP, Power Dissipation	TBD mW
θ_{JA} Thermal Impedance	TBD°C/W
Lead Temperature, Soldering	
Vapor Phase (TBD sec)	TBD°C
Infrared (TBD sec)	TBD°C
32-Lead LFCSP, Power Dissipation	TBD mW
θ_{JA} Thermal Impedance	TBD°C/W
Lead Temperature, Soldering	
Vapor Phase (TBD sec)	TBD°C
Infrared (TBD sec)	TBD°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

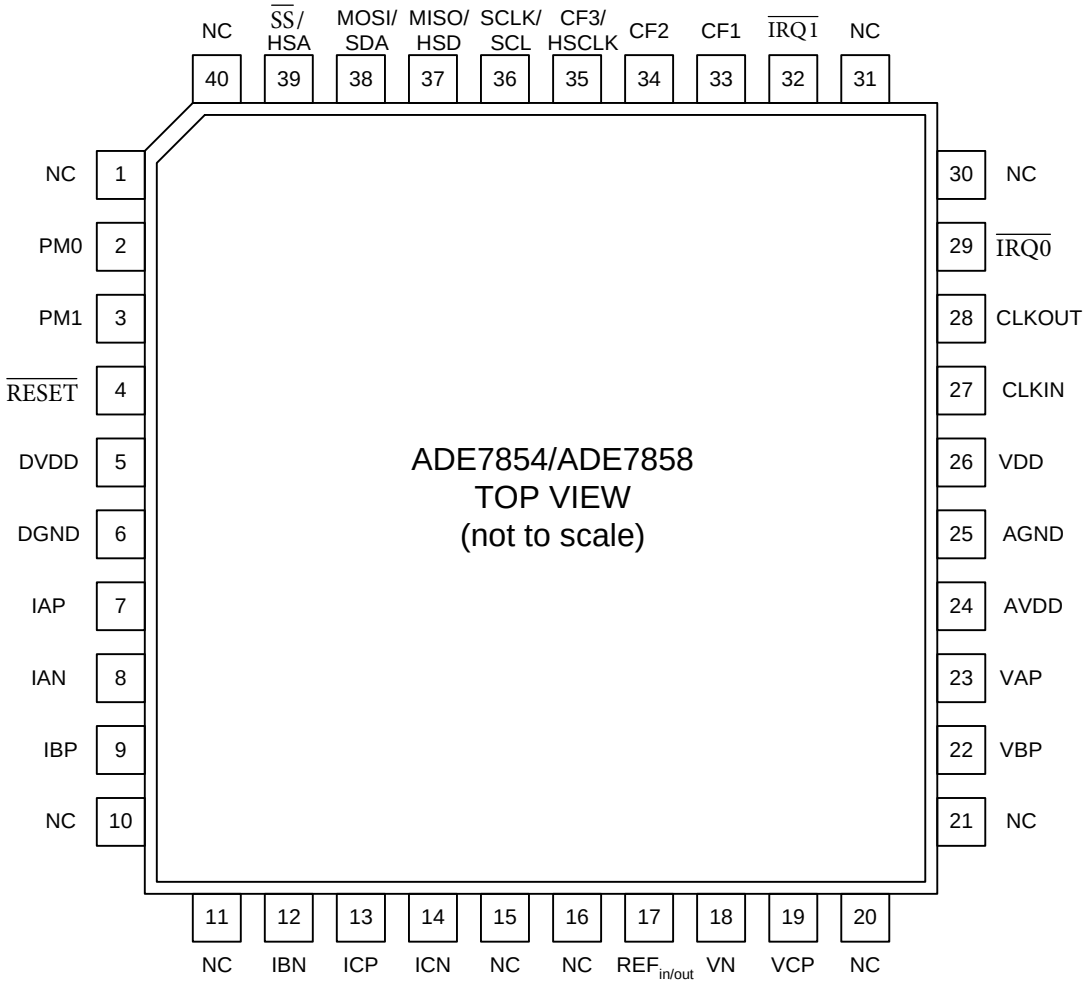

Figure 6. ADE7854 Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1,10,11,20,21,30,31,40	NC	These pins are not connected internally.
2	PM0	Power Mode pin 0. This pin should be set to VDD via a 10kΩ pull-up resistor for proper operation of the ADE7854.
3	PM1	Power Mode pin 1. This pin defines the power mode of the ADE7854 as described in Table 7.
4	$\overline{\text{RESET}}$	Reset Input, active low.
5	DVDD	This pin provides access to the on-chip 2.5V digital LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor.
6	DGND	This provides the ground reference for the digital circuitry in the ADE7854.
7,8, 9,12, 13,14	IAP, IAN, IBP, IBN, ICP, ICN	Analog Inputs for Current Channel. This channel is used with the current transducers and is referenced in this document as the current channel. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel has an internal PGA for IA, IB and IC.
15,16	NC	These pins should be connected to AGND.
17	$\text{REF}_{\text{IN/OUT}}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V ± 0.075% and a maximum temperature coefficient of 50 ppm/°C. An external reference source with 1.2V ± 8% can also be connected at this pin. In either case, this pin should be decoupled to AGND with a 10 µF ceramic capacitor. After reset, the on-

		chip reference is enabled.
18, 19, 22, 23	VN, VCP, VBP, VAP	Analog Inputs for the Voltage Channel. This channel is used with the voltage transducer and is referenced as the voltage channel in this document. These inputs are single-ended voltage inputs with the maximum signal level of ±0.5 V with respect to VN for specified operation. This channel has also an internal PGA.
24	AVDD	This pin provides access to the on-chip 2.5V analog LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor.
25	AGND	This pin provides the ground reference for the analog circuitry in the ADE7854. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, for example, antialiasing filters, current, and voltage transducers.
26	VDD	This pin provides the supply voltage for the ADE7854. In PSM0 (normal power mode) the supply voltage should be maintained at 3.3 V ± 10% for specified operation. In PSM3 (sleep mode), when the ADE7854 is supplied from a battery, the supply voltage should be maintained between 2.4 and 3.7V. This pin should be decoupled to DGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
27	CLKIN	Master Clock for the ADE7854. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7854. The clock frequency for specified operation is 16.384 MHz. Ceramic load capacitors of a few tens of picofarad should be used with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for the load capacitance requirements.
28	CLKOUT	A crystal can be connected across this pin and CLKIN as previously described to provide a clock source for the ADE7854. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used.
29, 32	$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$	Interrupt Request Outputs. These are active low logic outputs. See the Interrupts section for a detailed presentation of the events that may trigger interrupts.
33,34,35	CF1,CF2,CF3/HSCLK	Calibration Frequency (CF) Logic Outputs. Provide power information based on CF1SEL, CF2SEL, CF3SEL bits in CFMODE register. These outputs are used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the respectively CF1DEN, CF2DEN, CF3DEN registers (see the ENERGY to FREQUENCY CONVERSION section). CF3 is multiplexed with the serial clock output of HSDC port.
36	SCLK/SCL	Serial Clock Input for SPI port / Serial Clock Input for I^2C port. All serial data transfers are synchronized to this clock (see the Serial Interfaces section). This pin has a Schmidt-trigger input for use with a clock source that has a slow edge transition time, for example, opto-isolator outputs.
37	MISO/HSD	Data Out for SPI port / Data Out for HSDC port
38	MOSI/SDA	Data In for SPI port / Data Out for I^2C port
39	$\overline{\text{SS}}$ /HSA	Slave Select for SPI port / HSDC port active

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7854 is defined by

$$Measurement\ Error = \frac{Energy\ Registered\ by\ ADE7858/7854 - True\ Energy}{True\ Energy} \times 100\% \quad (1)$$

Phase Error Between Channels

The high-pass filter (HPF) and digital integrator introduce a slight phase mismatch between the current and the voltage channel. The all-digital design ensures that the phase matching between the current channels and voltage channels in all three phases is within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range of 40 Hz to 1 kHz. This internal phase mismatch can be combined with the external phase error (from current sensor or component tolerance) and calibrated with the phase calibration registers.

Power Supply Rejection (PSR)

This quantifies the ADE7854 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (TBD mV rms/TBD Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading—see the Measurement Error definition.

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied ±10%. Any error introduced is again expressed as a percentage of the reading.

ADC Offset Error

This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND that the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection (see the Typical Performance Characteristics section). However, the offset is removed from the current and voltage channels by a HPF and the power calculation is not affected by this offset.

Gain Error

The gain error in the ADCs of the ADE7854 is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADC section and the Voltage Channel ADC section). The difference is expressed as a percentage of the ideal code.

Gain Error Match

The gain error match is defined as the gain error (minus the offset) obtained when switching between a gain of 1, 2, 4, 8 or 16. It is expressed as a percentage of the output ADC code obtained under a gain of 1.

CF Jitter

The period of pulses at one of CF1, CF2 or CF3 pins is continuously measured. The maximum, minimum and average values of 4 consecutive pulses are computed:

$$MAX = \max(Period_0, Period_1, Period_2, Period_3)$$

$$MIN = \min(Period_0, Period_1, Period_2, Period_3)$$

$$AVG = \frac{Period_0 + Period_1 + Period_2 + Period_3}{4}$$

The CF jitter is then computed as

$$CF_{jitter} = \frac{MAX - MIN}{AVG} \cdot 100[\%]$$

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

TEST CIRCUITS

TBD

Figure 7. Test Circuit for Integrator Off

TBD

Figure 8. Test Circuit for Integrator On

POWER MANAGEMENT

The ADE7854 has two modes of operation, determined by the state of PM1 pin (see Table 7). This pin provides a complete control of ADE7854 operation and could easily be connected to an external microprocessor I/O. PM1 pin has internal pull up resistors. Table 8 presents all characteristics of the power modes.

Table 9 presents actions that are recommended before and after setting a new power mode.

Table 7. ADE7854 Power Supply Modes

Power Supply Modes	PM1
PSM0 – normal power mode	0
PSM3 – sleep mode	1

PSM0 – Normal Power Mode

In this mode, the ADE7854 is fully functional. The PM1 pin is set to low for the ADE7854 to enter this mode.

If the ADE7854 is in PSM3 mode and is switched into PSM0 mode, then all control registers take the default values. The ADE7854 signals the end of the transition period by triggering $\overline{\text{IRQ1}}$ interrupt pin low and setting bit 15 (RSTDONE) in STATUS1[31:0] register to 1. This bit is 0 during the transition period and becomes 1 when the transition is finished. The status bit is cleared and $\overline{\text{IRQ1}}$ pin is set back high by writing STATUS1[31:0] register with the corresponding bit set to 1. The bit 15 (RSTDONE) in interrupt mask register does not have any functionality attached even if $\overline{\text{IRQ1}}$ pin goes low when bit 15 (RSTDONE) in STATUS1[31:0] is set to 1. This makes RSTDONE interrupt unmaskable.

PSM3 – Sleep Mode

In this mode, the ADE7854 has most of its internal circuits turned off. The current consumption is the lowest. The I^2C, HSDC or SPI ports are not functional during this mode. The pins $\overline{\text{RESET}}$, SCLK/SCL, MOSI/SDA and $\overline{SS}$ /HAS should be set high.

Power Up Procedure

The ADE7854 contains an on-chip power supply monitor that supervises the power supply VDD. At power up, until VDD reaches 2V ± 10%, the chip is in an inactive state. As VDD crosses this threshold, the power supply monitor keeps the chip in this inactive state for 26msec more, allowing VDD to achieve 3.3V-10%, the minimum recommended supply voltage. As PM1 pin has an internal pull up resistor and the external microprocessor keeps it high, the ADE7854 always powers up in sleep mode PSM3. Then, an external circuit (i.e. microprocessor) sets PM1 pin to low level, allowing the ADE7854 to enter normal mode PSM0. The passage from PSM3 mode in which most of the internal circuitry is turned off to PSM0 mode in which all functionality is enabled is done in less than 40msec. See Figure 9 for details.

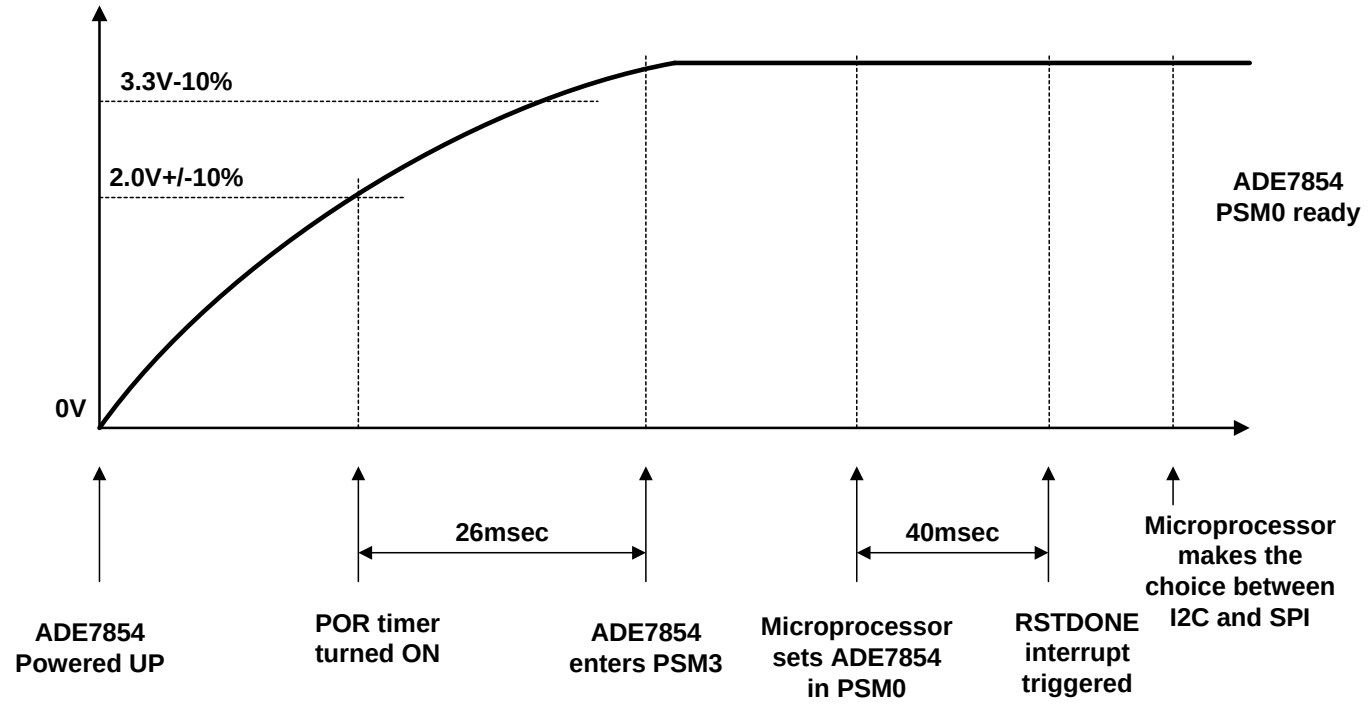

Figure 9. ADE7854 power up procedure

As the ADE7854 enters PSM0 mode, the I²C port is the active serial port. If the SPI port is used, then the $\overline{SS}$ pin must be toggled three times high to low. This action selects the ADE7854 into using the SPI port for further use. If I²C is the active serial port, bit 1 (I2C_LOCK) of CONFIG2[7:0] must be set to 1 to lock it in. From this moment on, the ADE7854 ignores spurious togglings of the $\overline{SS}$ pin and an eventual switch into using SPI port is no longer possible. If SPI is the active serial port, any write to CONFIG2[7:0] registers locks the port. From this moment on, a switch into using I²C port is no longer possible.

Only a power down or setting $\overline{RESET}$ pin low resets back the ADE7854 to use the I²C port. Once locked, the serial port choice is maintained when the ADE7854 changes between PSM0 and PSM3 power modes.

Immediately after entering PSM0, the ADE7854 sets all registers to their default values, including LPOILVL[7:0] and CONFIG2[7:0]. The ADE7854 signals the end of the transition period by triggering $\overline{IRQ1}$ interrupt pin low and setting bit 15 (RSTDONE) in STATUS1[31:0] register to 1. This bit is 0 during the transition period and becomes 1 when the transition ends. The status bit is cleared and $\overline{IRQ1}$ pin is set back high by writing STATUS1[31:0] register with the corresponding bit set to 1. As the RSTDONE is an unmaskable interrupt, bit 15 (RSTDONE) in STATUS1[31:0] register has to be cancelled in order for the $\overline{IRQ1}$ pin to turn back high. It is recommended to wait until $\overline{IRQ1}$ pin goes low before accessing STATUS1[31:0] register to test the state of RSTDONE bit. As a good programming practice, it is also recommended at this point to cancel all other status flags in STATUS1[31:0] and STATUS0[31:0] registers by writing the corresponding bits with 1.

Initially, the DSP is in idle mode, which means it does not execute any instruction. This is the moment to initialize all ADE7854 registers and then write 0x0001 into the RUN[15:0] register to start the DSP (see Digital Signal Processor chapter for details on the RUN[15:0] register).

If the supply voltage VDD becomes lower than 2V ± 10%, the ADE7854 goes into inactive state, which means no measurements are executed.

Hardware Reset

The ADE7854 has a RESET pin. If the ADE7854 is in PSM0 mode and RESET pin is set low, then the ADE7854 enters in hardware reset state. The ADE7854 has to be in PSM0 mode for hardware reset to be considered. Setting RESET pin low while the ADE7854 is in PSM3 mode does not have any effect.

If the ADE7854 is in PSM0 mode and RESET pin is toggled from high to low and then back high, all the registers are set to their default values, including LPOILVL[7:0] and CONFIG2[7:0]. The ADE7854 signals the end of the transition period by triggering $\overline{IRQ1}$ interrupt pin low and setting bit 15 (RSTDONE) in STATUS1[31:0] register to 1. This bit is 0 during the transition period and becomes 1 when the transition ends. The status bit is cleared and $\overline{IRQ1}$ pin is set back high by writing STATUS1[31:0] register with the corresponding bit set to 1.

After a hardware reset, the DSP is in idle mode, which means it does not execute any instruction. As the I²C port is the default serial port of the ADE7854, it becomes active after a reset state. If SPI is the port used by the external microprocessor, the procedure to enable it has to be repeated immediately after $\overline{RESET}$ pin is toggled back high. See Serial Interfaces chapter for details.

At this point, it is recommended to initialize all ADE7854 registers and then write 0x0001 into the RUN[15:0] register to start the DSP (see Digital Signal Processor chapter for details on RUN[15:0] register).

Software Reset Functionality

Bit 7 (SWRST) in CONFIG[15:0] register manages the software reset functionality in PSM0 mode. The default value of this bit is 0. If this bit is set to 1, then the ADE7854 enters a software reset state. In this state, almost all internal registers are set to their default value. In addition, the choice of what serial port I²C or SPI is in use remains unchanged if the lock in procedure has been previously executed (See Serial Interfaces chapter for details). The registers that maintain their values despite SWRST bit being set to 1 are LPOILVL[7:0] and CONFIG2[7:0]. When the software reset ends, bit 7 (SWRST) in CONFIG[15:0] is cleared to 0, the $\overline{IRQ1}$ interrupt pin is set low and bit 15 (RSTDONE) in STATUS1[31:0] register is set to 1. This bit is 0 during the transition period and becomes 1 when the transition ends. The status bit is cleared and $\overline{IRQ1}$ pin is set back high by writing STATUS1[31:0] register with the corresponding bit set to 1.

After a software reset ended, the DSP is in idle mode, which means it does not execute any instruction. It is recommended to initialize all the ADE7854 registers and then write 0x0001 into the RUN[15:0] register to start the DSP (see Digital Signal Processor chapter for details on the RUN[15:0] register).

Software reset functionality is not available in PSM3 mode.

Table 8: ADE7854 Power modes and related characteristics

Power Mode		Registers	LPOILVL, CONFIG2	I²C/SPI	Functionality
PSM0	**State after hardware reset**	Set to default	Set to default	I²C enabled	All circuits are active. DSP is in idle mode

Power Mode		Registers	LPOILVL, CONFIG2	I²C/SPI	Functionality
	State after software reset	Set to default	Unchanged	Active serial port unchanged if lock in procedure has been previously executed	All circuits are active. DSP is in idle mode
PSM3		Not available	Values set during PSM0 unchanged	Disabled	Internal circuits shut down Serial ports not available

Table 9. Recommended actions when changing power modes

Initial Power Mode	Recommended actions before setting next power mode	Next Power Mode	
		PSM0	**PSM3**
PSM0	-stop DSP by setting RUN[15:0]=0x0000 -disable HSDC by clearing bit 6 (HSDEN) to 0 in CONFIG[15:0] register -mask interrupts by setting in MASK0[31:0]=0x0 and MASK1[31:0]=0x0 -erase interrupt status flags in STATUS0[31:0] and STATUS1[31:0] registers		-no action necessary
PSM3	-no action necessary	-wait until $\overline{\text{IRQ1}}$ pin triggered low -poll STATUS1[31:0] register until bit 15 (RSTDONE) set to 1	

THEORY OF OPERATION

ANALOG INPUTS

The ADE7854 has seven analog inputs forming current and voltage channels. The current channels consist of three pairs of fully differential voltage inputs: IAP and IAN, IBP and IBN, ICP and ICN. These voltage input pairs have a maximum differential signal of ±0.5 V. The maximum common mode signal allowed on the inputs is ±25 mV. Figure 10 presents a schematic of the current channels inputs and their relation to the maximum common mode voltage.

All inputs have a programmable gain amplifier (PGA) with possible gain selection of 1, 2, 4, 8 or 16. The gain of IA, IB and IC inputs is set in PGA1 bits of GAIN[15:0] register. See Table 33 for details on GAIN[15:0] register.

The voltage channel has three single-ended voltage inputs: VAP, VBP, and VCP. These single-ended voltage inputs have a maximum input voltage of ±0.5 V with respect to VN. In addition, the maximum signal level on analog inputs for VxP and VN is ±0.5 V with respect to AGND. The maximum common mode signal allowed on the inputs is ±25 mV. Figure 12 presents a schematic of the voltage channels inputs and their relation to the maximum common mode voltage.

All inputs have a programmable gain with possible gain selection of 1, 2, 4, 8, or 16. The setting is done using PGA3 bits in GAIN[15:0] register – see Table 33.

Figure 11 shows how the gain selection from GAIN[15:0] register works in both current and voltage channels.

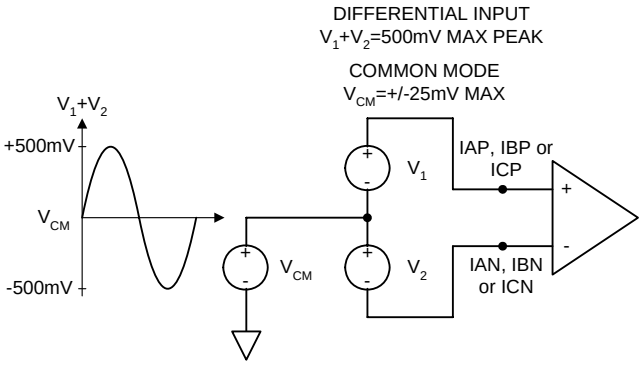

Figure 10. Maximum input level, current channels, Gain=1

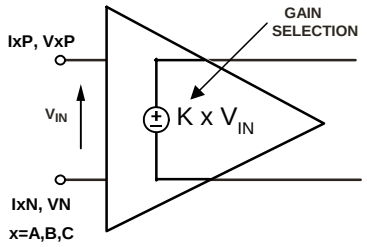

Figure 11.PGA in current and voltage channels

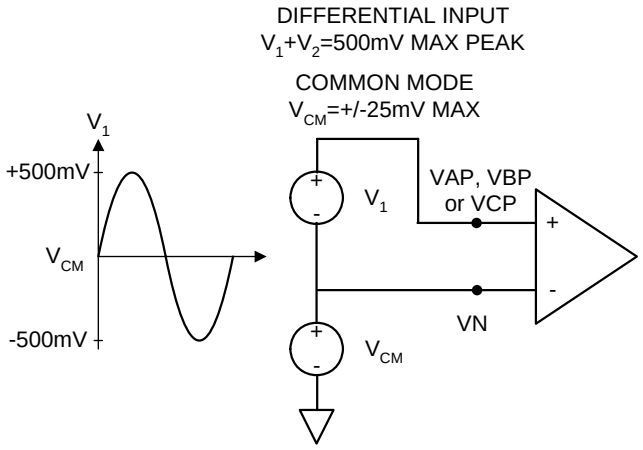

Figure 12. Maximum input level, voltage channels, Gain=1

ANALOG TO DIGITAL CONVERSION

The ADE7854 has six sigma-delta Analog to Digital Converters (ADC). In PSM0 mode, all ADCs are active. In PSM3 mode, the ADCs are powered down to minimize power consumption.

For simplicity, the block diagram in Figure 13 shows a first-order Σ-Δ ADC. The converter is made up of the Σ-Δ modulator and the digital low-pass filter.

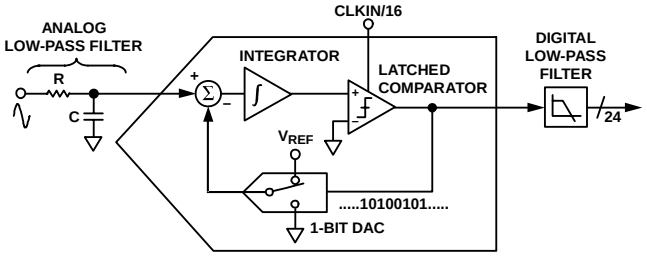

Figure 13. First-Order Σ-Δ ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7854, the sampling clock is equal to 1.024MHz (CLKIN/16). The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and therefore the bit stream) can approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged is a meaningful result obtained. This averaging is carried out in the second part of the ADC, the digital low-pass filter. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is oversampling. Oversampling means that the signal is sampled at a rate (frequency), which is many times higher than the bandwidth of interest. For example, the sampling rate in the

ADE7854 is 1.024MHz and the band of interest is 40 Hz to 4 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered — see Figure 14. However, oversampling alone is not efficient enough to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling ratio of 4 is required just to increase the SNR by only 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass-type response for the quantization noise. This is the second technique used to achieve high resolution. The result is that most of the noise is at the higher frequencies where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 14.

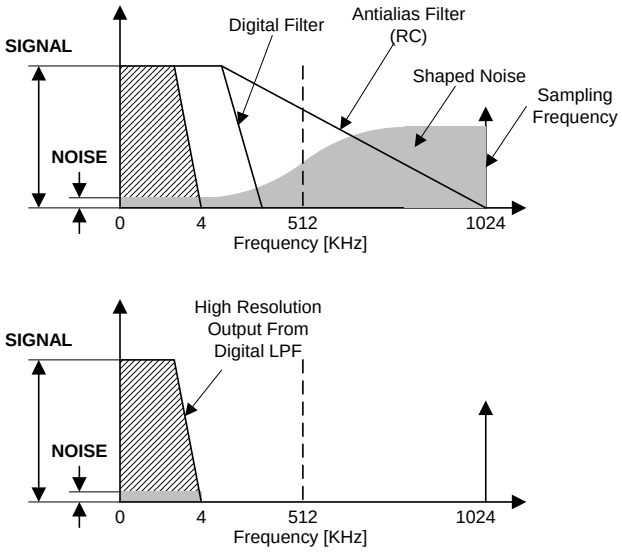

Figure 14. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

Antialiasing Filter

Figure 13 also shows an analog low-pass filter (RC) on the input to the ADC. This filter is placed outside the ADE7854 and its role is to prevent aliasing. Aliasing is an artifact of all sampled systems and is illustrated in Figure 15. Aliasing means that frequency components in the input signal to the ADC, which are higher than half the sampling rate of the ADC, appear in the sampled signal at a frequency below half the sampling rate. Frequency components (arrows shown in black) above half the sampling frequency (also know as the Nyquist frequency, i.e., 512 kHz) are imaged or folded back down below 512 kHz. This happens with all ADCs regardless of the architecture. In the example shown, only frequencies near the sampling frequency, i.e., 1.024MHz, move into the band of interest for metering, i.e., 40 Hz to 4 kHz. To attenuate the high frequency (near 1.024MHz) noise and prevent the distortion of the band of interest, a LPF (low-pass filter) has to be introduced. For conventional current sensors, it is recommended to use one RC filter with a corner frequency of 5KHz in order for the attenuation to be sufficiently high at the sampling frequency of 1.024MHz. The 20 dB per decade attenuation of this filter is usually sufficient to eliminate the effects of aliasing for conventional current sensors. However, for a di/dt sensor such as a Rogowski coil, the sensor has a 20 dB per decade gain. This neutralizes 20 dB per decade attenuation produced by the LPF. Therefore, when using a di/dt sensor, care should be taken to offset the 20 dB per decade gain. One simple approach is to cascade one more RC filter, so a –40 dB per decade attenuation is produced.

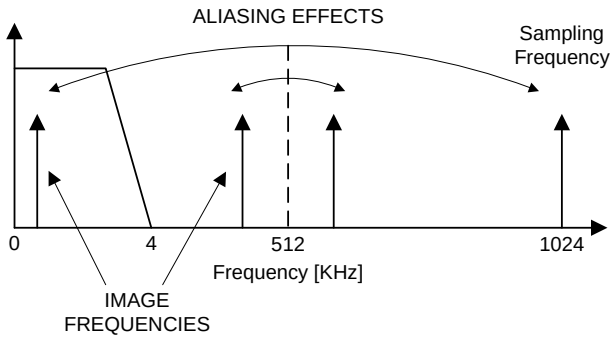

Figure 15. Aliasing effects at ADE7854

ADC Transfer Function

All ADCs in the ADE7854 are designed to produce the same 24-bit signed output code for the same input signal level. With a full-scale input signal of 0.5 V and an internal reference of 1.2 V, the ADC output code is nominally 5,928,256 (0x5A7540). The code from the ADC may vary between 0x800000 (-8,388,608) and 0x7FFFFF (+8,388,607); this is equivalent to an input signal level of ±0.707V. However, for specified performance, it is recommended not to exceed the nominal range of ±0.5V. The ADC performance is guaranteed only for input signals lower than ±0.5V.

CURRENT CHANNEL ADC

Figure 19 shows the ADC and signal processing path for the input IA of the current channels (same for IB and IC). The ADC outputs are signed twos complement 24-bit data-words and are available at a rate of 8 kSPS (thousand samples per second). With the specified full-scale analog input signal of ±0.5V, the ADC produces its maximum output code value. This diagram shows a full-scale voltage signal being applied to the differential inputs IAP and IAN. The ADC output swings between –5,928,256 (0xA58AC0) and+5,928,256 (0x5A7540).

Current Waveform Gain Registers

There is a multiplier in the signal path of each phase current. The current waveform can be changed by ±100% by writing a correspondent twos complement number to the 24-bit signed current waveform gain registers (AIGAIN[23:0], BIGAIN[23:0] and CIGAIN[23:0]). For example, if 0x400000 is written to those registers, the ADC output is scaled up by 50%. To scale the input by -50%, write 0xC00000 to the registers. Equation (1)

describes mathematically the function of the current waveform gain registers.

$$\text{Current waveform} = \text{ADC Output} \times \left(1 + \frac{\text{Content of Current Gain Register}}{2^{23}}\right) \quad (1)$$

Changing the content of AIGAIN[23:0], BIGAIN[23:0] or CIGAIN[23:0] affects all calculations based on its current; that is, it affects the corresponding phase active/reactive/apparent energy and current rms calculation. In addition, waveform samples are also scaled accordingly.

Note that the serial ports of the ADE7854 work on 32, 16 or 8-bit words and the DSP works on 28 bits. The 24-bit AIGAIN, BIGAIN and CIGAIN registers are accessed as 32-bit registers with 4 most significant bits padded with 0s and sign extended to 28 bits. See Figure 16 for details.

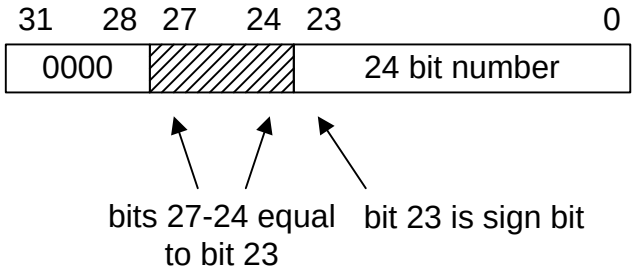

Figure 16. 24-bit xIGAIN (x=A,B,C) are transmitted as 32-bit words

Current Channel HPF

The ADC outputs can contain a dc offset. This offset may create errors in power and rms calculations. High Pass Filters (HPF) are placed in the signal path of the phase currents and of the phase voltages. If enabled, the HPF eliminates any dc offset on the current channel. All filters are implemented in the DSP and by default they are all enabled: 24-bit register HPFDIS[23:0] is cleared to 0x00000000. All filters are disabled by setting HPHDIS[23:0] to any non zero value.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words. The HPFDIS register is accessed as a 32-bit register with 8 most significant bits padded with 0s. See Figure 17 for details.

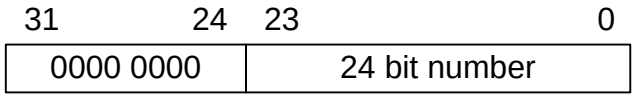

Figure 17. 24-bit HPFDIS register is transmitted as 32-bit word

Current Channel Sampling

The waveform samples of the current channel are taken at the output of HPF and stored into IAWV, IBWV, ICWV 24-bit signed registers at a rate of 8kSPS. All power and rms calculations remain uninterrupted during this process. Bit 17 (DREADY) in STATUS0[31:0] register is set when IAWV, IBWV and ICWV registers are available to be read using I^2C or SPI serial ports. Setting bit 17 (DREADY) in MASK0[31:0] register enables an interrupt to be set when the DREADY flag is set. See Digital Signal Processor chapter for more details on bit DREADY.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words. When IAWV, IBWV, ICWV 24-bit signed registers are read from the ADE7854, they are transmitted signed extended to 32 bits. See Figure 18 for details.

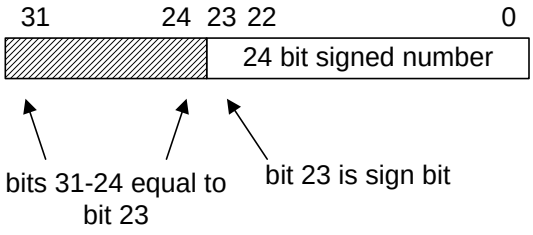

Figure 18. 24-bit IxWV (x=A, B, C) are transmitted as 32-bit signed words

The ADE7854 contains a High Speed Data Capture (HSDC) port that is specially designed to provide fast access to the waveform sample registers. See HSDC Interface section for more details.

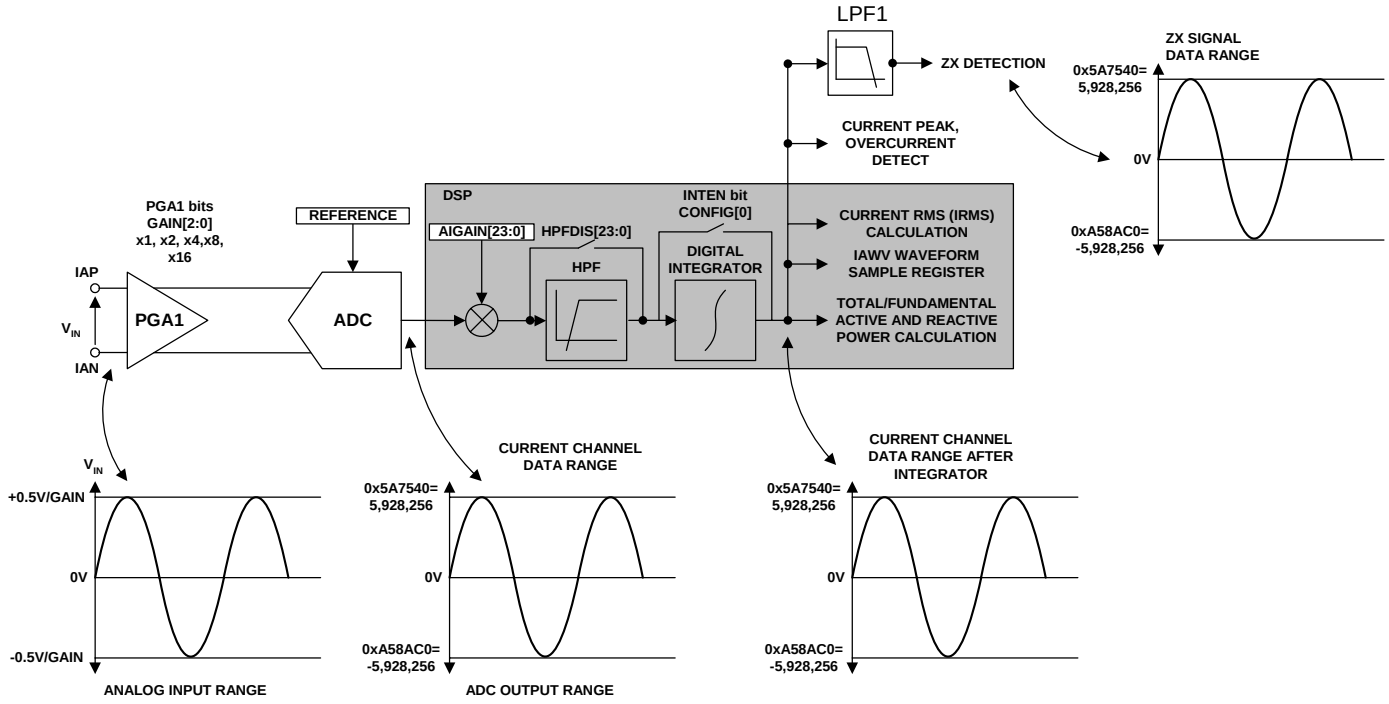

Figure 19. Current Channel Signal Path

di/dt CURENT SENSOR AND DIGITAL INTEGRATOR

The di/dt sensor detects changes in the magnetic field caused by the ac current. Figure 20 shows the principle of a di/dt current sensor.

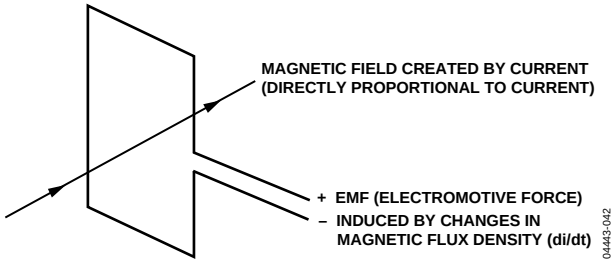

Figure 20. Principle of a di/dt Current Sensor

The flux density of a magnetic field induced by a current is directly proportional to the magnitude of the current. The changes in the magnetic flux density passing through a conductor loop generate an electromotive force (EMF) between the two ends of the loop. The EMF is a voltage signal that is proportional to the di/dt of the current. The voltage output from the di/dt current sensor is determined by the mutual inductance between the current carrying conductor and the di/dt sensor.

Due to the di/dt sensor, the current signal needs to be filtered before it can be used for power measurement. On each phase current data path, there is a built-in digital integrator to recover the current signal from the di/dt sensor. The digital integrator is disabled by default when the ADE7854 is powered up and after reset. Setting bit 0 (INTEN) of the CONFIG[15:0] register turns on the integrator. Figure 21 to Figure 24 show the magnitude and phase response of the digital integrator.

TBD

Figure 21. Combined Gain Response of the Digital Integrator

TBD

Figure 22. Combined Phase Response of the Digital Integrator

TBD

Figure 23. Combined Gain Response of the Digital Integrator (40 Hz to 70 Hz)

TBD

Figure 24. Combined Phase Response of the Digital Integrator (40 Hz to 70 Hz)

Note that the integrator has a −20 dB/dec attenuation and approximately −90° phase shift. When combined with a di/dt sensor, the resulting magnitude and phase response should be a flat gain over the frequency band of interest. However, the di/dt sensor has a 20 dB/dec gain associated with it and generates significant high frequency noise. An antialiasing filter of at least the second order is needed to avoid that the noise alias back in the band of interest when the ADC is sampling (see the Antialiasing Filter section).

DICOEFF[23:0] 24-bit signed register is used in the digital integrator algorithm. At power up or after a reset, its value is 0x000000. Before turning on the integrator, this register must be initialized with 0xFF8000. DICOEFF[23:0] is not used when the integrator is turned off and can be left at 0x000000 in this case.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words. Similar to the registers presented in Figure 16, DICOEFF[23:0] 24-bit signed register is accessed as a

32-bit register with 4 most significant bits padded with 0s and sign extended to 28 bits.

When the digital integrator is switched off, the ADE7854 can be used directly with a conventional current sensor, such as a current transformer (CT).

VOLTAGE CHANNEL ADC

Figure 25 shows the ADC and signal processing chain for the input VA in the voltage channel. The VB and VC channels have similar processing chains. The ADC outputs are signed twos complement 24-bit words and are available at a rate of 8 kSPS. With the specified full-scale analog input signal of ±0.5 V, the ADC produces its maximum output code value. This diagram shows a full-scale voltage signal being applied to the differential inputs VA and VN. The ADC output swings between −5,928,256 (0xA558AC0) and +5,928,256 (0x5A7540).

Voltage Waveform Gain Registers

There is a multiplier in the signal path of each phase voltage. The voltage waveform can be changed by ±100% by writing a correspondent twos complement number to the 24-bit signed current waveform gain registers (AVGAIN[23:0], BVGAIN[23:0] and CVGAIN[23:0]). For example, if 0x400000 is written to those registers, the ADC output is scaled up by 50%. To scale the input by -50%, write 0xC00000 to the registers. Equation (7) describes mathematically the function of the current waveform gain registers.

$$\text{Voltage waveform} = \text{ADC Output} \times \left(1 + \frac{\text{Content of Voltage Gain Register}}{2^{23}}\right) \quad (2)$$

Changing the content of AVGAIN[23:0], BVGAIN[23:0] and CVGAIN[23:0] affects all calculations based on its voltage; that is, it affects the corresponding phase active/reactive/apparent energy and voltage rms calculation. In addition, waveform samples are also scaled accordingly.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words and the DSP works on 28 bits. As presented in Figure 16, AVGAIN, BVGAIN and CVGAIN registers are accessed as 32-bit registers with 4 most significant bits padded with 0s and sign extended to 28 bits.

Voltage Channel HPF

As seen in Current Channel HPF section, the ADC outputs can contain a dc offset that can create errors in power and rms calculations. High Pass Filters (HPF) are placed in the signal path of the phase voltages, similar to the ones in the current channels. HPFDIS[23:0] register may enable or disable the filters. See Current Channel HPF section for more details.

Voltage Channel Sampling

The waveform samples of the current channel are taken at the output of HPF and stored into VAWV, VBWV and VCWV 24-bit signed registers at a rate of 8kSPS. All power and rms calculations remain uninterrupted during this process. Bit 17 (DREADY) in STATUS0[31:0] register is set when VAWV, VBWV and VCWV registers are available to be read using I^2C or SPI serial ports. Setting bit 17 (DREADY) in MASK0[31:0] register enables an interrupt to be set when the DREADY flag is set. See Digital Signal Processor chapter for more details on bit DREADY.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words. Similar to registers presented in Figure 18, VAWV, VBWV and VCWV 24-bit signed registers are transmitted signed extended to 32 bits.

The ADE7854 contains a High Speed Data Capture (HSDC) port that is specially designed to provide fast access to the waveform sample registers. See HSDC Interface section for more details.

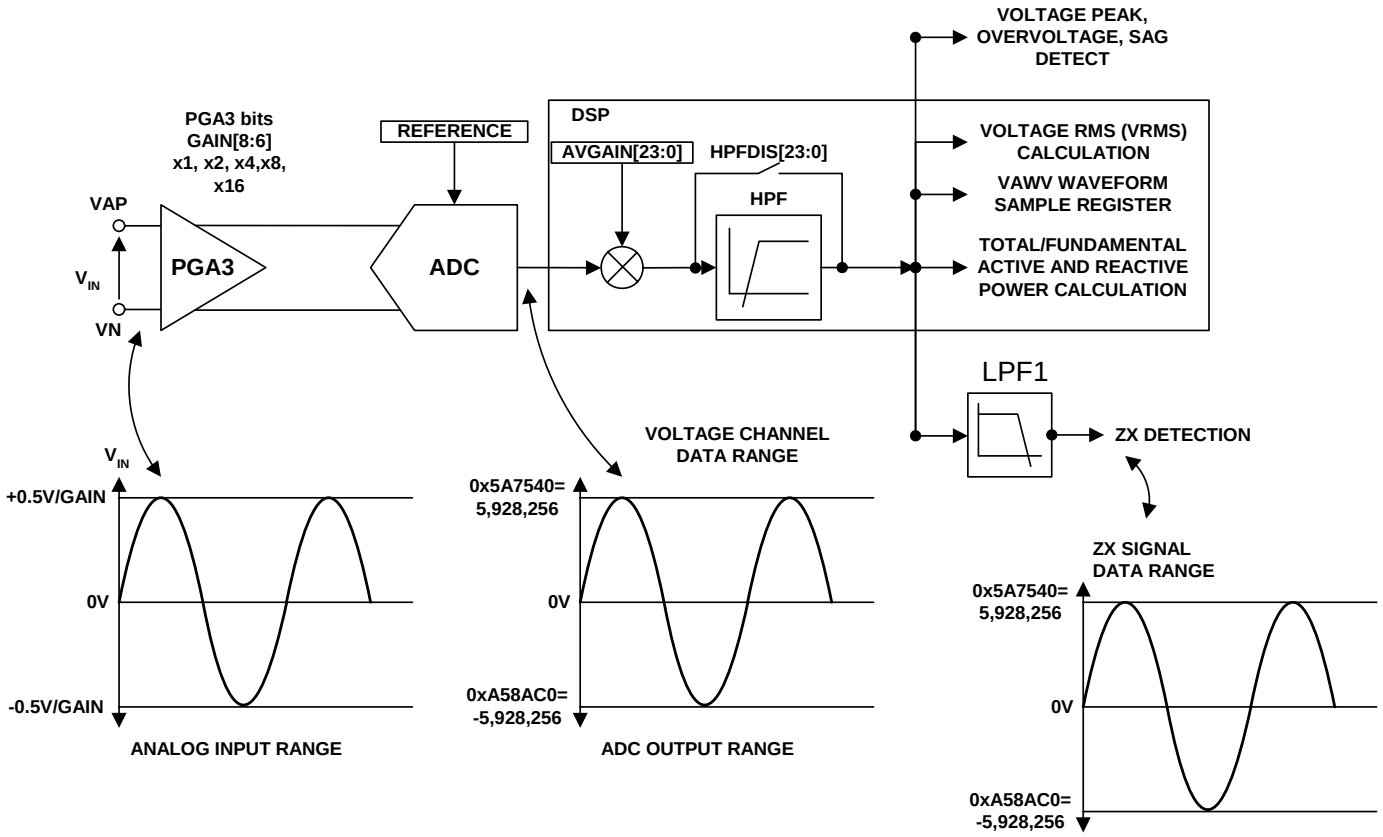

Figure 25. Voltage Channel Data Path

CHANGING PHASE VOLTAGE DATA PATH

The ADE7854 may direct one phase voltage input to the computational data path of another phase. For example, phase A voltage may be introduced in the phase B computational data path, which means all powers computed by the ADE7854 in phase B are based on phase A voltage and phase B current.

Bits 9-8 (VTOIA[1:0]) of CONFIG[15:0] register manage the phase A voltage measured at VA pin. If VTOIA[1:0]=00 (default value), the voltage is directed to phase A computational data path, if VTOIA[1:0]=01, the voltage is directed to phase B path and if VTOIA[1:0]=10, the voltage is directed to phase C path. If VTOIA[1:0]=11, the ADE7854 behave as if VTOIA[1:0]=00.

Bits 11-10 (VTOIB[1:0]) of CONFIG[15:0] register manage the phase B voltage measured at VB pin. If VTOIB[1:0]=00 (default value), the voltage is directed to phase B computational data path, if VTOIB[1:0]=01, the voltage is directed to phase C path and if VTOIB[1:0]=10, the voltage is directed to phase A path. If VTOIB[1:0]=11, the ADE7854 behave as if VTOIB[1:0]=00.

Bits 13-12 (VTOIC[1:0]) of CONFIG[15:0] register manage the phase C voltage measured at VC pin. If VTOIC[1:0]=00 (default value), the voltage is directed to phase C computational data path, if VTOIC[1:0]=01, the voltage is directed to phase A path and if VTOIC[1:0]=10, the voltage is directed to phase B path. If VTOIC[1:0]=11, the ADE7854 behaves as if VTOIC[1:0]=00.

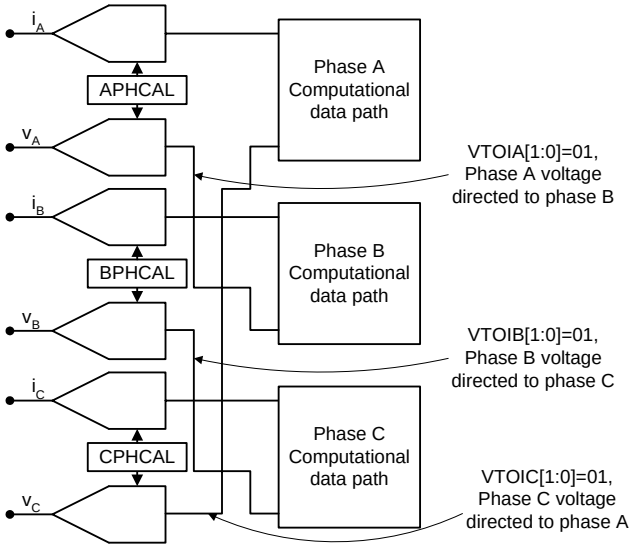

Figure 26.Phase voltages used in different data paths

Figure 26 presents the case in which phase A voltage is used in the phase B data path, phase B voltage is used in phase C data path and phase C voltage is used in phase A data path.

POWER QUALITY MEASUREMENTS

Zero Crossing Detection

The ADE7854 has a zero-crossing (ZX) detection circuit on the current and voltage channels. Zero crossing events are used as a

time base for various power quality measurements and in the calibration process.

A zero-crossing is generated from the output of LPF1. The low pass filter is intended to eliminate all harmonics of 50Hz and 60Hz systems and help identify the zero crossing events on the fundamental components of both current and voltage channels. The digital filter has a pole at 80Hz and is clocked at 256KHz. As a result, there is a phase lag between the analog input signal (one of IA, IB, IC, VA, VB and VC) and the output of LPF1. The error in ZX detection is 0.07° for 50Hz systems (0.085° for 60Hz systems). The phase lag response of LPF1 results in a time delay of approximately 31.4° or 1.74msec (@ 50 Hz) between its input and output. The overall delay between the zero crossing on the analog inputs and ZX detection obtained after LPF1 is around 39.6° or 2.2 msec (@ 50 Hz). The ADC and HPF introduce the additional delay. The LPF1 cannot be disabled to assure a good resolution of the ZX detection. Figure 27 shows how the zero-crossing signal is detected.

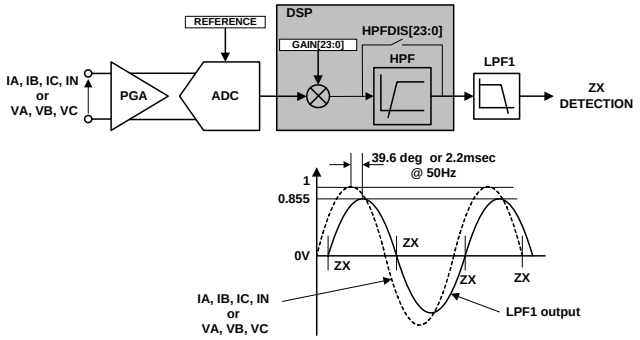

Figure 27. Zero-Crossing Detection on Voltage and Current channels

In order to provide further protection from noise, input signals to the voltage channel with amplitude lower than 10% of full scale do not generate zero crossing events at all. The current channel ZX detection circuit is active for all input signals independent of their amplitude.

The ADE7854 contains six zero crossing detection circuits, one for each phase voltage and current channel. Each circuit drives one flag in STATUS1[31:0] register. If circuit placed in phase A voltage channel detects one zero crossing event, then bit 9 (ZXVA) in STATUS1[31:0] register is set to 1. Similarly, phase B voltage circuit drives bit 10 (ZXVB), phase C voltage circuit drives bit 11 (ZXVC) and circuits placed in the current channel drive bit 12 (ZXIA), bit 13 (ZXIB) and bit 14 (ZXIC). If a ZX detection bit is set in the MASK1[31:0] register, the $\overline{\text{IRQ1}}$ interrupt pin is driven low and the corresponding status flag is set to 1. The status bit is cleared and $\overline{\text{IRQ1}}$ pin is set back high by writing STATUS1 register with the status bit set to 1.

Zero-Crossing Timeout

Every zero-crossing detection circuit has an associated timeout register. This register is loaded with the value written into 16-bit ZXTOUT register and is decremented (1 LSB) every 62.5 µs (16KHz clock). The register is reset to ZXTOUT value every time a zero crossing is detected. The default value of this register is 0xFFFF. If the timeout register decrements to 0 before a zero crossing is detected, then one of bits 8-3 of STATUS1[31:0] register is set to 1. Bit 3 (ZXTOVA), bit 4 (ZXTOVB) and bit 5 (ZXTOVC) refer to phases A, B and C of the voltage channel, bit 6 (ZXTOIA), bit 7 (ZXTOIB), bit 8 (ZXTOIC) refer to phases A, B and C of the current channel. If a ZXTOUT bit is set in the MASK1[31:0] register, the $\overline{\text{IRQ1}}$ interrupt pin is driven low when the corresponding status bit is set to 1. The status bit is cleared and $\overline{\text{IRQ1}}$ pin is set back high by writing STATUS1 register with the status bit set to 1.

The resolution of ZXTOUT register is 62.5 µs (16KHz clock) per LSB. Thus, the maximum time-out period for an interrupt is 4.096seconds: 2^{16}/16KHz.

Figure 28 shows the mechanism of the zero-crossing timeout detection when the voltage or the current signal stays at a fixed dc level for more than 62.5 x ZXTOUT µs.

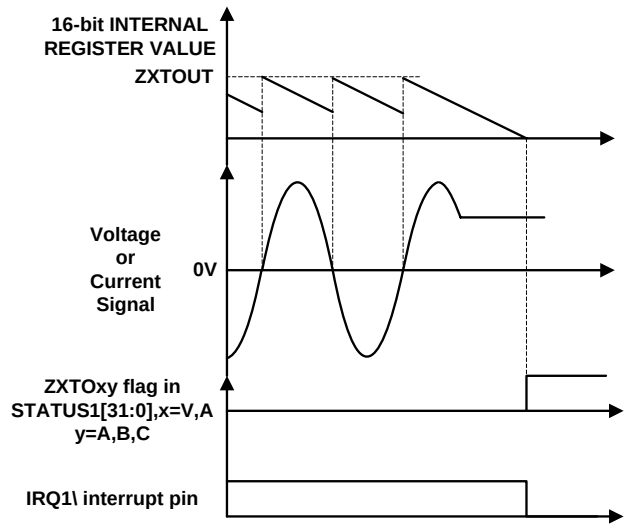

Figure 28. Zero-Crossing Timeout Detection

Phase Sequence Detection

The ADE7854 has an on-chip phase sequence error detection circuit. This detection works on phase voltages and considers only the zero crossings determined by their negative to positive transitions. The regular succession of these zero crossing events is phase A followed by phase B followed by phase C (see Figure 30). If the sequence of zero crossing events is instead phase A, followed by phase C followed by phase B, then bit 19 (SEQERR) in STATUS1[31:0] register is set. If bit 19 (SEQERR) in MASK1[31:0] register is set to 1 and a phase sequence error event is triggered, then $\overline{\text{IRQ1}}$ interrupt pin is driven low. The status bit is cleared and $\overline{\text{IRQ1}}$ pin is set back high by writing STATUS1 register with the status bit SEQERR set to 1.

The phase sequence error detection circuit is functional only when the ADE7854 is connected in a 3 phase 4 wire 3 voltage sensors configuration (bits 5,4 CONSEL in ACCMODE[7:0] set to 00). In all other configurations, only two voltage sensors are

used and therefore it is not recommended to use the detection circuit. In these cases, the time intervals between phase voltages should be used to analyze the phase sequence (see Time Interval Between Phases section for details).

Figure 29 presents the case in which phase A voltage is not followed by phase B voltage, but by phase C voltage. Every time a negative to positive zero crossing occurs, bit 19 (SEQERR) in STATUS1[31:0] register is set to 1 because such zero crossings on phase C, B or A cannot come after zero crossings from phase A, C or respectively B zero crossings.

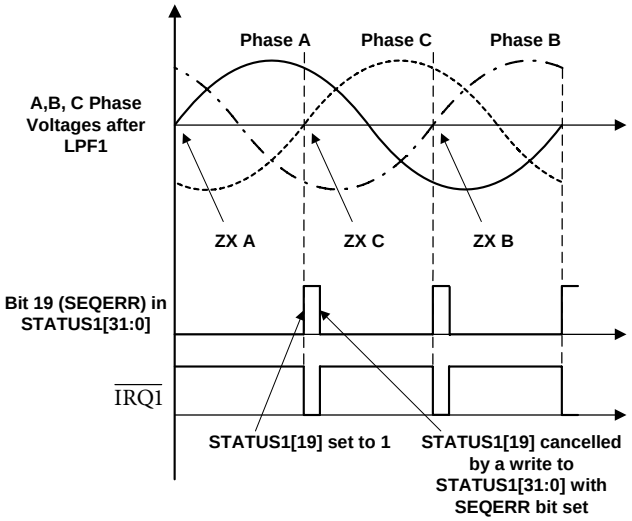

Figure 29. SEQERR bit set to 1 when phase A voltage is followed by phase C voltage

Once a phase sequence error has been detected, the time measurement between various phase voltages (see Time Interval Between Phases section) may help to identify which phase voltage should be considered with another phase current in the computational data path. The bits 9-8 (VTOIA[1:0]), 11-10 (VTOIB[1:0]) and 13-12 (VTOIC[1:0]) in CONFIG[15:0] register may be used to direct one phase voltage to the data path of another phase. See Changing Phase voltage data path section for details.

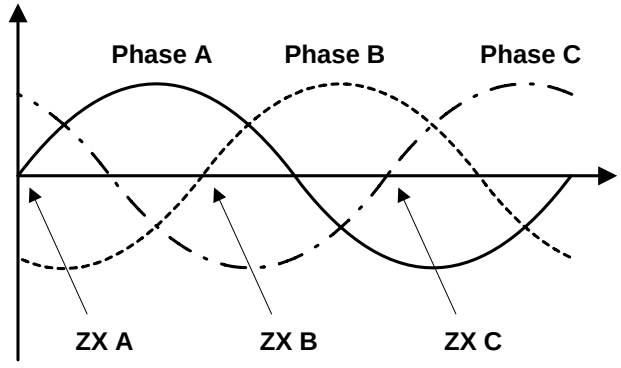

Figure 30. Phase Sequence Detection

Time Interval Between Phases

The ADE7854 has the capability to measure the time delay between phase voltages, between phase currents or between voltages and currents of the same phase. The negative to positive transitions identified by the zero crossing detection circuit are used as start and stop measuring points. Only one set of such measurements are available at one time, based on bits 10,9 (ANGLESEL[1:0]) in COMPMODE[15:0] register.

When ANGLESEL[1:0] bits are set to 00, the default value, then the delays between voltages and currents on the same phase are measured. The delay between phase A voltage and phase A current is stored in the 16-bit unsigned ANGLE0[15:0] register (See Figure 31). In a similar way, the delays between voltages and currents on phase B and C are stored in ANGLE1[15:0] and ANGLE2[15:0] registers respectively.

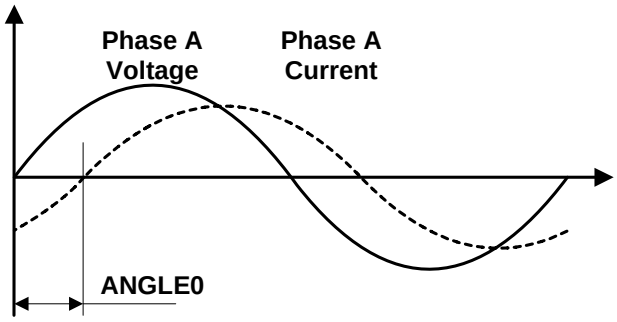

Figure 31.Delay between phase A voltage and current is stored in ANGLE0[15:0]

When ANGLESEL[1:0] bits are set to 01, the delays between phase voltages are measured. The delay between phase A voltage and phase C voltage is stored into ANGLE0[15:0]. The delay between phase B voltage and phase C voltage is stored in ANGLE1[15:0] register and the delay between phase A voltage and phase B voltage is stored into ANGLE2[15:0] register (see Figure 32).

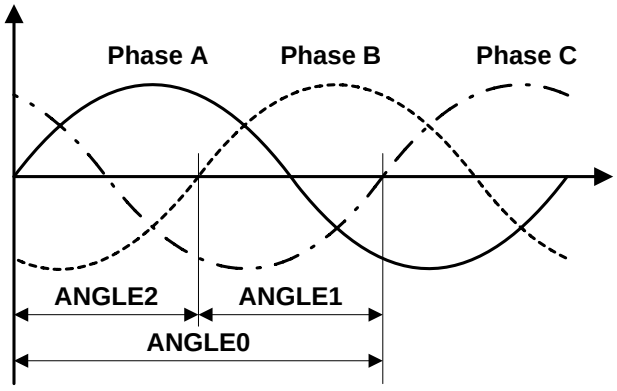

Figure 32. Delays between phase voltages(currents)

When ANGLESEL[1:0] bits are set to 10, the delays between phase currents are measured. Similar to delays between phase voltages, the delay between phase A and phase C currents is

stored into ANGLE0[15:0] register, the delay between phase B and phase C currents is stored into ANGLE1[15:0] register and the delay between phase A and phase B currents is stored into ANGLE2[15:0] register (see Figure 32).

The ANGLE0, ANGLE1 and ANGLE2 registers are 16-bit unsigned registers with 1LSB corresponding to 3.9µs (256 KHz clock), which means a resolution of 0.07° (360°x 50Hz/256KHz) for 50Hz systems and 0.084° (360°x 60Hz/256KHz) for 60Hz systems. The delays between phase voltages or phase currents are used to characterize how balanced the load is. The delays between phase voltages and currents are used to compute the power factor on each phase (see expression (3) below).

$$\cos\varphi_x = \cos\left[ANGLEx \cdot \frac{360° \cdot f_{Line}}{256KHz} \right] \quad (3)$$

where x=A, B or C and $f_{Line}$is 50Hz or 60Hz.

Period Measurement

The ADE7854 provides the period measurement of the line in the voltage channel. Bits 1,0 (PERSEL[1:0]) in MMODE[7:0] register select the phase voltage used for this measurement. The PERIOD register is a 16-bit unsigned register and is updated every line period. Because of LPF1 filter (see Figure 27), a settling time of 30-40msec is associated with this filter before the measurement is stable.

The period measurement has a resolution of 3.9 µs/LSB (256 KHz clock), which represents 0.0195% (50Hz/256KHz) when the line frequency is 50 Hz. The value of the period register for 50Hz networks is approximately 5,120 (256KHz/50Hz). The length of the register enables the measurement of line frequencies as low as 3.9 Hz (256KHz/2^{16}). The period register is stable at ±1 LSB when the line is established and the measurement does not change.

The following expressions may be used to compute the line period and frequency using PERIOD[15:0] register:

$$T_L = \frac{PERIOD[15:0]}{256E3}[\text{sec}] \quad (4)$$

$$f_L = \frac{256E3}{PERIOD[15:0]}[Hz] \quad (5)$$

Phase Voltage Sag Detection

The ADE7854 can be programmed to detect when the absolute value of any phase voltage drops below a certain peak value for a number of half line cycles. The phase where this event took place is identified in bits 14,13,12 (VSPHASE[2:0]) of PHSTATUS[15:0] register. This condition is illustrated in Figure 33.

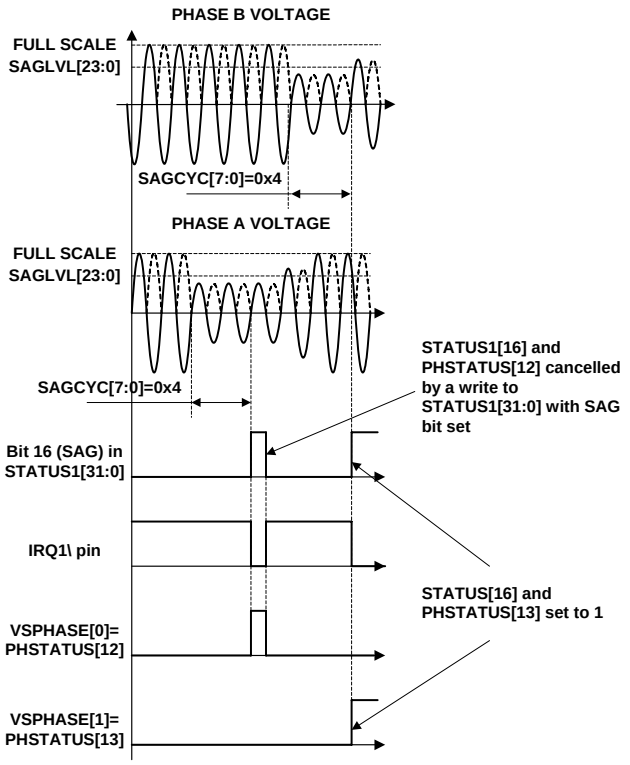

Figure 33. ADE7854 Sag Detection

Figure 33 shows phase A voltage falling below a threshold that is set in the sag level register (SAGLVL[23:0]) for four half line cycles (SAGCYC=4). When bit 16 (SAG) in STATUS1[31:0] register is set to 1 to indicate the condition, bit VSPHASE[0] in PHSTATUS[15:0] register also is set to 1 because the event happened on phase A. Bit 16 (SAG) in STATUS1[31:0] register and all bits 14,13,12 (VSPHASE[2:0]) of PHSTATUS[15:0] register (not only VSPHASE[0] bit) are erased by writing STATUS1[31:0] register with SAG bit set to 1. The SAGCYC[7:0] register represents the number of half line cycles the phase voltage must remain below the level indicated in SAGLVL register in order to trigger a sag condition. 0 is not valid a valid number for SAGCYC. For example, when the sag cycle (SAGCYC[7:0]) contains 0x07, the SAG flag in STATUS1[31:0] register is set at the end of the seventh half line cycle for which the line voltage falls below the threshold. If bit 16 (SAG) in MASK1[31:0] is set, $\overline{\text{IRQ1}}$ interrupt pin is driven low in case of a sag event in the same moment the status bit 16 (SAG) in STATUS1[31:0] register is set to 1. The SAG status bit in STATUS1[31:0] register and all bits 14,13,12 (VSPHASE[2:0]) of PHSTATUS[15:0] register are cleared and $\overline{\text{IRQ1}}$ pin is set back high by writing STATUS1[31:0] register with the status bit set to 1.

When the phase B voltage falls below the threshold indicated into SAGLVL[23:0] register for two line cycles, bit VSPHASE[1] in PHSTATUS[15:0] register is set to 1 and bit VSPHASE[0] is cleared to 0. In the same moment, bit 16 (SAG) in STATUS1[31:0] register is set to 1 to indicate the condition.

Note that the internal zero-crossing counter is always active. By setting SAGLVL[23:0] register, the first sag detection result is, therefore, not done across a full SAGCYC period. Writing to the SAGCYC[7:0] register when the SAGLVL[23:0] is already initialized resets the zero-crossing counter, thus ensuring that the first sag detection result is obtained across a full SAGCYC period.

The recommended procedure to manage sag events is the following:

-enable SAG interrupts in MASK1[31:0] register by setting bit 16 (SAG) to 1.

-when a sag event happens, the $\overline{\text{IRQ1}}$ interrupt pin goes low.

-STATUS1[31:0] register is read with bit 16 (SAG) set to 1.

-PHSTATUS[15:0] is read, identifying on which phase or phases a sag event happened.

-STATUS1[31:0] register is written with bit 16 (SAG) set to 1. In this moment, bit SAG is erased and also all bits 14,13,12 (VSPHASE[2:0]) of PHSTATUS[15:0] register.

Sag Level Set

The content of the sag level register SAGLVL[23:0] is compared to the absolute value of the output from HPF. Writing 5,928,256 (0x5A7540) to SAGLVL register, puts the sag detection level at full scale – see Voltage Channel ADC Chapter, so the sag event is triggered continuously. Writing 0x00 or 0x01 puts the sag detection level at 0, so the sag event is never triggered.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words. Similar to the register presented in Figure 17, SAGLVL register is accessed as 32-bit registers with 8 most significant bits padded with 0s.

Peak Detection

The ADE7854 records the maximum absolute values reached by the voltage and current channels over a certain number of half line cycles and stores them into the less significant 24 bits of VPEAK[31:0] and IPEAK[31:0] 32-bit registers. PEAKCYC[7:0] register contains the number of half line cycles used as a time base for the measurement. It uses the zero crossing points identified by the zero crossing detection circuit. Bits 4, 3, 2 (PEAKSEL[2:0]) in MMODE[7:0] register select on which phases the peak measurement is done. Bit 2 selects phase A, bit 3 selects phase B and bit 4 selects phase C. Selecting more than one phase to monitor the peak values decreases proportionally the measurement period indicated in PEAKCYC[7:0] register because zero crossings from more phases are involved in the process. When a new peak value is determined, one of bits 26, 25, 24 (IPPHASE[2:0] or VPPHASE[2:0]) in IPEAK[31:0] and VPEAK[31:0]registers is set to 1 identifying the phase that triggered the peak detection event. For example, if a peak value has been identified on phase A current, bit 24 (IPPHASE[0]) in IPEAK[31:0] register is set to 1. If next time a new peak value is measured on phase B, then bit 24 (IPPHASE[0]) of IPEAK[31:0] is cleared to 0 and bit 25 (IPPHASE[1]) of IPEAK[31:0] is set to 1. Figure 34 presents the composition of IPEAK and VPEAK registers.

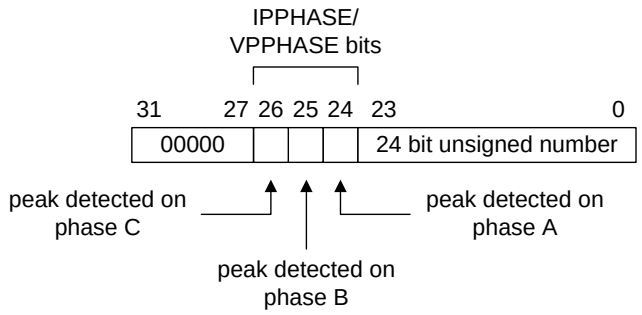

Figure 34.Composition of IPEAK[31:0] and VPEAK[31:0] registers

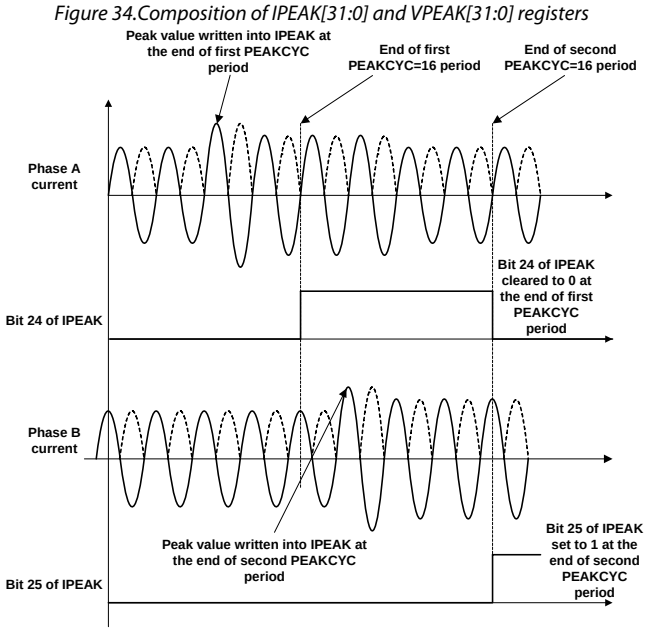

Figure 35. ADE7854 Peak Level Detection

Figure 35 shows how the ADE7854 records the peak value on the current channel when measurements on phases A and B are enabled (bits PEAKSEL[2:0] in MMODE[7:0] are 011). PEAKCYC[7:0] is set to 16, meaning that the peak measurement cycle is 4 line periods. The maximum absolute value of phase A is the greatest during the first 4 line periods (PEAKCYC=16), so the maximum absolute value is written into the less significant 24 bits of IPEAK[31:0] register and bit 24 (IPPHASE[0]) of IPEAK[31:0] register is set to 1 at the end of the period. This bit remains 1 for the duration of the second PEAKCYC period of 4 line cycles. The maximum absolute value of phase B is the greatest during the second PEAKCYC period, so the maximum absolute value is written into the less significant 24 bits of IPEAK register and bit 25 (IPPHASE[1]) in IPEAK register is set to 1 at the end of the period.

At the end of the peak detection period in the current channel, bit 23 (PKI) in STATUS1[31:0] register is set to 1. If bit 23 (PKI) in MASK1[31:0] register is set, then $\overline{\text{IRQ1}}$ interrupt pin is driven low at the end of PEAKCYC period and the status bit 23 (PKI) in STATUS1[31:0] is set to 1. In a similar way, at the end of the

peak detection period in the voltage channel, bit 24 (PKV) in STATUS1[31:0] register is set to 1. If bit 24 (PKV) in MASK1[31:0] register is set, then $\overline{\text{IRQ1}}$ interrupt pin is driven low at the end of PEAKCYC period and the status bit 24 (PKV) in STATUS1[31:0] is set to 1. To find the phase that triggered the interrupt, one of IPEAK[31:0] or VPEAK[31:0] registers is read immediately after reading STATUS1[31:0]. Then the status bits are cleared and $\overline{\text{IRQ1}}$ pin is set back high by writing STATUS1[31:0] register with the status bit set to 1.

Note that the internal zero-crossing counter is always active. By setting bits 4, 3, 2 (PEAKSEL[2:0]) in MMODE[7:0] register, the first peak detection result is, therefore, not done across a full PEAKCYC period. Writing to the PEAKCYC[7:0] register when the PEAKSEL[2:0] bits are set resets the zero-crossing counter, thus ensuring that the first peak detection result is obtained across a full PEAKCYC period.

Overvoltage and Overcurrent Detection

The ADE7854 detects when the instantaneous absolute value measured on the voltage and current channels becomes greater than thresholds set in OVLVL[23:0] and OILVL[23:0] 24-bit unsigned registers. If bit 18 (OV) in MASK1[31:0] register is set, $\overline{\text{IRQ1}}$ interrupt pin is driven low in case of an overvoltage event. There are two status flags set when $\overline{\text{IRQ1}}$ interrupt pin is driven low: bit 18 (OV) in STATUS1[31:0] register and one of bits 11, 10, 9 (OVPHASE[2:0]) in PHSTATUS[15:0] register identifying the phase that generated the overvoltage. The status bit 18 (OV) in STATUS1[31:0] register and all bits 11, 10, 9 (OVPHASE[2:0]) in PHSTATUS[15:0] register are cleared and $\overline{\text{IRQ1}}$ pin is set back high by writing STATUS1[31:0] register with the status bit set to 1. Figure 36 presents overvoltage detection in phase A voltage. Whenever the absolute instantaneous value of the voltage goes above the threshold from OVLVL[23:0] register, bit 18 (OV) in STATUS1[31:0] and bit 9 (OVPHASE[0]) in PHSTATUS[15:0] registers are set to 1. The bit 18 (OV) of STATUS1[31:0] register and bit 9 (OVPHASE[0]) in PHSTATUS[15:0] register are cancelled when STATUS1 register is written with bit 18 (OV) set to 1.

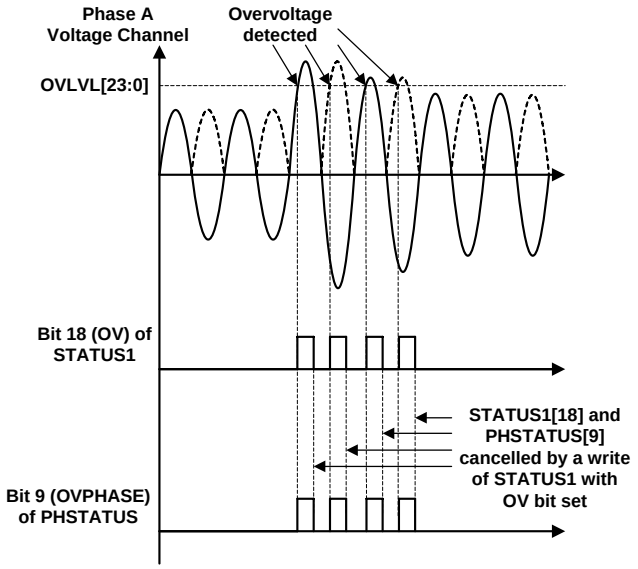

Figure 36. ADE7854 Overvoltage Detection

The recommended procedure to manage overvoltage events is the following:

-enable OV interrupts in MASK1[31:0] register by setting bit 18 (OV) to 1.

-when an overvoltage event happens, the $\overline{\text{IRQ1}}$ interrupt pin goes low.

-STATUS1[31:0] register is read with bit 18 (OV) set to 1.

-PHSTATUS[15:0] is read, identifying on which phase or phases an overvoltage event happened.

-STATUS1[31:0] register is written with bit 18 (OV) set to 1. In this moment, bit OV is erased and also all bits 11, 10, 9 (OVPHASE[2:0]) of PHSTATUS[15:0] register.

In case of an overcurrent event, if bit 17 (OI) in MASK1[31:0] register is set, $\overline{\text{IRQ1}}$ interrupt pin is driven low. In the same moment, bit 17 (OI) in STATUS1[31:0] register and one of bits 5,4,3 (OIPHASE[2:0]) in PHSTATUS[15:0] register identifying the phase that generated the interrupt are set. To find the phase that triggered the interrupt, PHSTATUS[15:0] register is read immediately after reading STATUS1[31:0]. Then the status bit 17 (OI) in STATUS1[31:0] register and bits 5,4,3 (OIPHASE[2:0]) in PHSTATUS[15:0] register are cleared and $\overline{\text{IRQ1}}$ pin is set back high by writing STATUS1[31:0] register with the status bit set to 1. The process is similar with the overvoltage detection.

Overvoltage and Overcurrent Level Set

The content of the overvoltage OVLVL[23:0] and overcurrent OILVL[23:0] 24-bit unsigned registers is compared to the absolute value of the voltage and current channels. The maximum value of these registers is the maximum value of the HPF outputs: +5,928,256 (0x5A7540). When OVLVL or OILVL are equal to this value, the overvoltage or overcurrent

conditions will never be detected. Writing 0x0 to these registers signifies the overvoltage or overcurrent conditions are continuously detected and the corresponding interrupts are triggered permanently.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words. Similar to the register presented in Figure 17, OILVL and OVLVL registers are accessed as 32-bit registers with 8 most significant bits padded with 0s.

PHASE COMPENSATION

As seen in Current Channel ADC and Voltage Channel ADC chapters, the data path for both current and voltages is the same. The phase error between current and voltage signals introduced by the ADE7854 is negligible. However, the ADE7854 must work with transducers that may have inherent phase errors. For example, a current transformer (CT) with a phase error of 0.1° to 3° is not uncommon. These phase errors can vary from part to part, and they must be corrected to perform accurate power calculations.

The errors associated with phase mismatch are particularly noticeable at low power factors. The ADE7854 provides a means of digitally calibrating these small phase errors. The ADE7854 allows a small time delay or time advance to be introduced into the signal processing chain to compensate for the small phase errors.

The phase calibration registers (APHCAL[9:0], BPHCAL[9:0], and CPHCAL[9:0]) are 10-bit registers that can vary the time advance in the voltage channel signal path from +61.5 µs to −374.0 µs, respectively. Negative values written to the PHCAL registers represent a time advance, and positive values represent a time delay. One LSB is equivalent to 0.976 µs of time delay or time advance (clock rate of 1.024MHz). With a line frequency of 60 Hz, this gives a phase resolution of 0.0211° (360° × 60 Hz/1.024 MHz) at the fundamental. This corresponds to a total correction range of −8.079° to +1.329° at 60 Hz. At 50Hz, the correction range is -6.732° to +1.107° and the resolution is 0.0176°(360° × 50 Hz/1.024 MHz) .

Given a phase error of x degrees measured using the phase voltage as the reference, then the corresponding LSBs are computed dividing x by the phase resolution (0.0211°/LSB for 60Hz, 0.0176°/LSB for 50Hz). Only results between -383 and +63 are acceptable. Numbers outside this range are not accepted. If the result is negative, the absolute value is written into PHCAL registers. If the result is positive, 512 is added to it before writing the result into PHCAL.

$$yPHCAL = \begin{cases} \left| \dfrac{x}{phase\_resolution} \right|, x \le 0 \\ \dfrac{x}{phase\_resolution} + 512, x > 0 \end{cases} \quad (6)$$

Figure 38 illustrates how the phase compensation is used to remove x=-1° phase lead in IA of the current channel from the external current transducer (equivalent of 55.5µs for 50Hz systems). To cancel the lead (1°) in the current channel of Phase A, a phase lead must be introduced into the corresponding voltage channel. Using expression (3), APHCAL is 57, rounded up from 56.8. The phase lead is achieved by introducing a time delay of 55.73 µs into the phase A current.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words. As presented in Figure 37, APHCAL, BPHCAL and CPHCAL 10-bit registers are accessed as a 16-bit registers with 6 most significant bits padded with 0s.

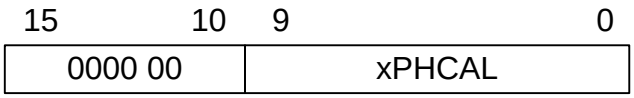

Figure 37. xPHCAL registers (x=A,B,C) are communicated as 16-bit registers

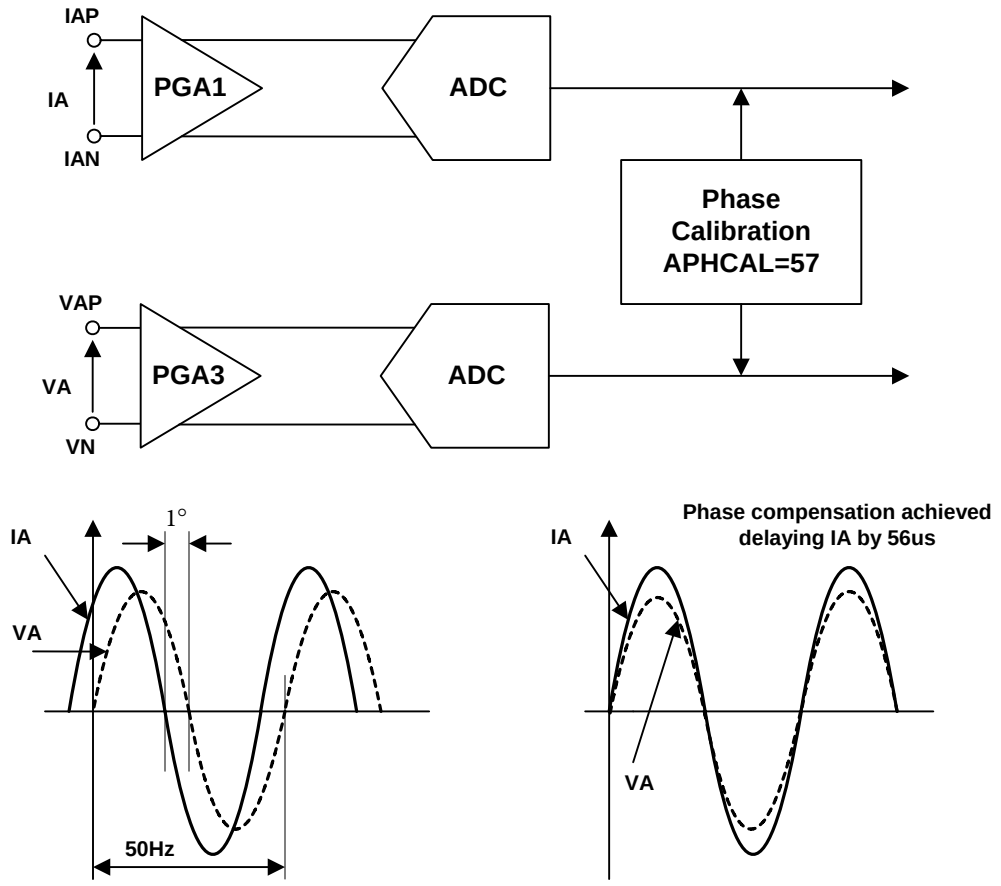

Figure 38. Phase Calibration on Voltage Channels

REFERENCE CIRCUIT

The nominal reference voltage at the $REF_{IN/OUT}$ pin is 1.2±1% V. This is the reference voltage used for the ADCs in the ADE7854. The $REF_{IN/OUT}$ pin can be overdriven by an external source, for example, an external 1.2 V reference. The voltage of the ADE7854 reference drifts slightly with temperature; see the Specifications section for the temperature coefficient specification (in ppm/°C). The value of the temperature drift varies from part to part. Because the reference is used for all ADCs, any x% drift in the reference results in a 2x% deviation of the meter accuracy. The reference drift resulting from temperature changes is usually very small and typically much smaller than the drift of other components on a meter. Alternatively, the meter can be calibrated at multiple temperatures.

If bit 0 (EXTREFEN) in CONFIG2[7:0] register is cleared to 0 (the default value), the ADE7854 use the internal voltage reference. If the bit is set to 1, then the external voltage reference is used. CONFIG2 register should be set during PSM0 mode. Its value is maintained during the other power mode PSM3.

DIGITAL SIGNAL PROCESSOR

The ADE7854 contains an internal Digital Signal Processor (DSP) that computes all powers and rms values. It contains various memories: program memory ROM, program memory RAM, data memory RAM.

The program used for the power and rms computations is stored in the program memory ROM and the processor executes it every 8KHz. The end of the computations is signaled by setting bit 17 (DREADY) to 1 in STATUS0[31:0] register. An interrupt attached to this flag may be enabled by setting bit 17 (DREADY) in MASK0[31:0] register. If enabled, the $\overline{IRQ0}$ pin is set low and status bit DREADY is set to 1 at the end of the computations. The status bit is cleared and $\overline{IRQ0}$ pin is set back high by writing STATUS0[31:0] register with bit 17 (DREADY) set to 1.

The registers used by the DSP are located in the data memory RAM, at addresses between 0x4000 and 0x43FF. The width of this memory is 28 bits.

As seen in Power Up Procedure section, at power up or after a hardware or software reset, the DSP is in idle mode. No instruction is being executed. All the registers located in the data memory RAM are initialized at 0, their default values. The register RUN[15:0] used to start and stop the DSP is cleared to

0x0000. The RUN[15:0] register needs to be written with 0x0001 in order for the DSP to start code execution. It is recommended to first initialize all ADE7854 registers located into the data memory RAM with their desired values and then write RUN[15:0] register with 0x0001. In this way, the DSP starts the computations from a desired configuration.

There is no obvious reason to stop the DSP if the ADE7854 is maintained in PSM0 normal mode. All ADE7854 registers including ones located in the data memory RAM can be modified without stopping the DSP. However, to stop the DSP, 0x0000 has to be written into the register RUN[15:0]. To start the DSP again, one of the following procedures must be followed:

- if ADE7854 registers located in the data memory RAM have not been modified, write 0x0001 into register RUN[15:0] to start the DSP.

-if ADE7854 registers located in the data memory RAM have to be modified, first execute a software or a hardware reset, initialize all ADE7854 registers at desired values and then write 0x0001 into register RUN[15:0] to start the DSP.

As mentioned in Power Management chapter, when the ADE7854 switches out of PSM0 power mode into PSM3 sleep mode, it is recommended to stop the DSP by writing 0x0000 into RUN[15:0] register (see Table 9 for recommended actions when changing power modes).

ROOT MEAN SQUARE MEASUREMENT

Root mean square (rms) is a measurement of the magnitude of an ac signal. Its definition can be both practical and mathematical. Defined practically, the rms value assigned to an ac signal is the amount of dc required to produce an equivalent amount of power in the load. Mathematically, the rms value of a continuous signal f(t) is defined as

$$FRMS = \sqrt{\frac{1}{T}\int_0^T f^2(t)\mathrm{dt}} \quad (7)$$

For time sampling signals, rms calculation involves squaring the signal, taking the average, and obtaining the square root.

$$FRMS = \sqrt{\frac{1}{N}\sum_{n=1}^{N} f^2[n]} \quad (8)$$

The expression (8) implies that for signals containing harmonics, the rms calculation contains the contribution of all harmonics, not only the fundamental.

The first method is to low-pass filter the square of the input signal (LPF3) and take the square root of the result (see Figure 40).

$$f(t) = \sum_{k=1}^{\infty} F_k \sqrt{2}\sin(k\omega t + \gamma_k) \quad (9)$$

Then

$$f^2(t) = \sum_{k=1}^{\infty} F_k^2 - \sum_{k=1}^{\infty} F_k^2 \cos(2k\omega t + \gamma_k) + 2\sum_{\substack{k,m=1 \\ k\neq m}}^{\infty} 2\cdot F_k \cdot F_m \sin(k\omega t + \gamma_k)\cdot\sin(m\omega t + \gamma_m) \quad (10)$$

After the LPF3 and the execution of the square root, the rms value of f(t) is obtained:

$$F = \sqrt{\sum_{k=1}^{\infty} F_k^2} \quad (11)$$

The rms calculation based on this method is simultaneously processed on all six analog input channels. Each result is available in 24-bit registers AIRMS, BIRMS, CIRMS, AVRMS, BVRMS and CVRMS.

Current RMS Calculation

This chapter presents the first approach to compute the rms values of all phase and neutral currents.

Figure 40 shows the detail of the signal processing chain for the rms calculation on one of the phases of the current channel. The current channel rms value is processed from the samples used in the current channel. The current rms values are signed 24-bit values and they are stored into AIRMS[23:0], BIRMS[23:0] and CIRMS[23:0]. The update rate of the current rms measurement is 8KHz.

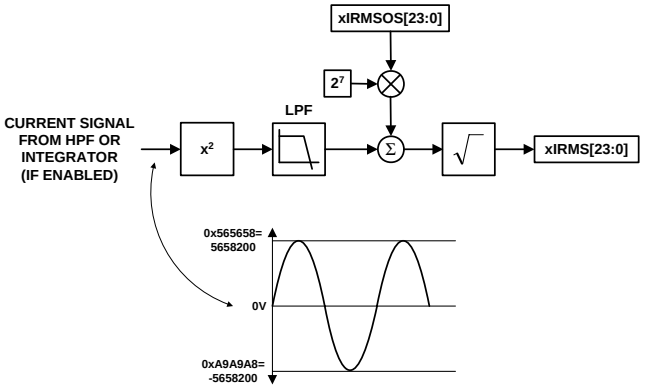

Figure 40. Current RMS Signal Processing

With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code that is approximately ±5,928,256. The equivalent rms value of a full-scale sinusoidal signal is 4,191,910(0x3FF6A6), independent of the line frequency. If the integrator is enabled, that is when bit 0 (INTEN) in CONFIG[15:0] register is set to 1, the equivalent rms value of a full-scale sinusoidal signal at 50Hz is 4,191,910(0x3FF6A6) and at 60Hz is 3,493,258(0x354D8A).

The accuracy of the current rms is typically 0.1% error from the full-scale input down to 1/1000 of the full-scale input. Additionally, this measurement has a bandwidth of 4 kHz. It is recommended

to read the rms registers synchronous to the voltage zero crossings to ensure stability. The $\overline{\text{IRQ1}}$ interrupt can be used to indicate when a zero crossing has occurred (see the Interrupts section).

Table 10 shows the settling time for the IRMS measurement, which is the time it takes for the rms register to reflect the value at the input to the current channel.

Table 10. Settling Time for IRMS Measurement

	50Hz Input signals	60Hz Input signals
Integrator Off	530msec	530msec
Integrator On	550msec	500msec

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words. Similar to the register presented in Figure 17, AIRMS, BIRMS and CIRMS 24-bit signed registers are accessed as 32-bit registers with 8 most significant bits padded with 0s.

Current RMS Offset Compensation

The ADE7854 incorporates a current rms offset compensation register for each phase: AIRMSOS[23:0], BIRMSOS[23:0] and CIRMSOS[23:0]. These are 24-bit signed registers and are used to remove offsets in the current rms calculations. An offset can exist in the rms calculation due to input noises that are integrated in the dc component of $I^2(t)$. One LSB of the current rms offset compensation register is equivalent to 128 LSBs of the square of the current rms register. Assuming that the maximum value from the current rms calculation is 4,191,400 with full-scale ac inputs (50 Hz), one LSB of the current rms offset represents 0.00036% of the rms measurement at 60 dB down from full scale. Calibration of the offset should be done at low current and values at zero input should be ignored.

$$IRMS = \sqrt{IRMS_0^2 + IRMSOS \cdot 128} \qquad (12)$$

where $IRMS_0$ is the rms measurement without offset correction.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words and the DSP works on 28 bits. Similar to registers presented in Figure 16, AIRMSOS, BIRMSOS and CIRMSOS 24-bit signed registers are accessed as 32-bit registers with 4 most significant bits padded with 0s and sign extended to 28 bits.

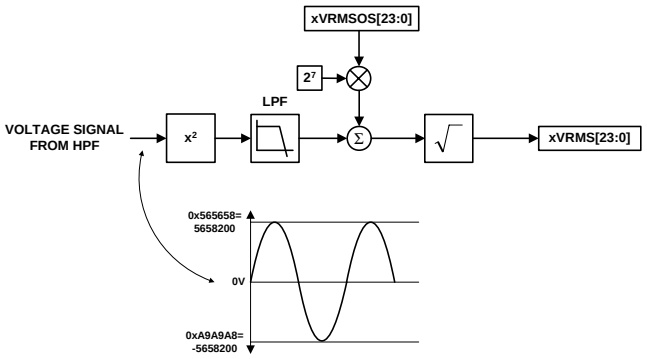

Figure 41. Voltage RMS Signal Processing

Voltage Channel RMS Calculation

Figure 41 shows the detail of the signal processing chain for the rms calculation on one of the phases of the voltage channel. The voltage channel rms value is processed from the samples used in the voltage channel. The voltage rms values are signed 24-bit values and they are stored into the registers AVRMS[23:0], BVRMS[23:0] and CVRMS[23:0]. The update rate of the current rms measurement is 8KHz.

With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code that is approximately ±5,928,256. The equivalent rms value of a full-scale sinusoidal signal at 4,191,910 (0x3FF6A6), independent of the line frequency.

The accuracy of the voltage rms is typically 0.1% error from the full-scale input down to 1/1000 of the full-scale input. Additionally, this measurement has a bandwidth of 4 kHz. It is recommended to read the rms registers synchronous to the voltage zero crossings to ensure stability. The $\overline{\text{IRQ1}}$ interrupt can be used to indicate when a zero crossing has occurred (see the Interrupts section).

Table 11 shows the settling time for the VRMS measurement, which is the time it takes for the rms register to reflect the value at the input to the voltage channel.

Table 11. Settling Time for VRMS Measurement

50Hz Input signals	60Hz Input signals
530 ms	530 ms

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words. Similar to the register presented in Figure 17, AVRMS, BVRMS and CVRMS 24-bit signed registers are accessed as 32-bit registers with 8 most significant bits padded with 0s.

Voltage RMS Offset Compensation

The ADE7854 incorporates a voltage rms offset compensation for each phase AVRMSOS[23:0], BVRMSOS[23:0], and CVRMSOS[23:0]. These are 24-bit signed registers used to remove offsets in the voltage rms calculations. An offset can exist in the rms calculation due to input noises that are integrated in the dc component of $V^2(t)$. One LSB of the voltage rms offset compensation register is equivalent to 128 LSBs of the square of the voltage rms register. Assuming that the maximum value from the voltage rms calculation is 4,191,400 with full-scale ac inputs (50 Hz), one LSB of the current rms offset represents 0.00036% of the rms measurement at 60 dB down from full scale. Calibration of the offset should be done at low current and values at zero input should be ignored.

$$VRMS = \sqrt{VRMS_0^2 + VRMSOS \cdot 128} \qquad (13)$$

where $VRMS_0$ is the rms measurement without offset correction.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words and the DSP works on 28 bits. Similar to registers presented in Figure 16, AVRMSOS, BVRMSOS and CVRMSOS 24-bit registers are accessed as 32-bit registers with 4 most significant bits padded with 0s and sign extended to 28 bits.

ACTIVE POWER CALCULATION

The ADE7854 computes the total active power. Total active power considers in its calculation all fundamental and harmonic components of the voltages and currents.

Total Active Power Calculation

Electrical power is defined as the rate of energy flow from source to load. It is given by the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. If an ac system is supplied by a voltage v(t) and consumes the current i(t) and each of them contains harmonics, then:

$$v(t) = \sum_{k=1}^{\infty} V_k \sqrt{2} \sin(k\omega t + \varphi_k) \quad (14)$$

$$i(t) = \sum_{k=1}^{\infty} I_k \sqrt{2} \sin(k\omega t + \gamma_k)$$

where V_k, I_k = rms voltage and current of each harmonic, φ_k, γ_k =phase delays of each harmonic.

The instantaneous power in an ac system is:

$$p(t) = v(t) \cdot i(t) = \sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k) - \sum_{k=1}^{\infty} V_k I_k \cos(2k\omega t + \varphi_k - \gamma_k) + \\ + \sum_{\substack{k,m=1 \\ k \neq m}}^{\infty} V_k I_m \{\cos[(k-m)\omega t + \varphi_k - \gamma_m] - \cos[(k+m)\omega t + \varphi_k + \gamma_m]\} \quad (15)$$

The average power over an integral number of line cycles (n) is given by the expression in expression (16).

$$P = \frac{1}{nT} \int_0^{nT} p(t)dt = \sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k) \quad (16)$$

where: T is the line cycle period.
P is referred to as the total active or total real power. Note that the total active power is equal to the dc component of the instantaneous power signal $p(t)$ in (15), that is, $\sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k)$. This is the expression used to calculate the total active power in the ADE7854 for each phase.

Figure 42 shows how the ADE7854 computes the total active power on each phase. First, it multiplies the current and voltage signals in each phase. Then, extracts the dc component of the instantaneous power signal in each phase (A, B and C) using LPF2, the low pass filter.

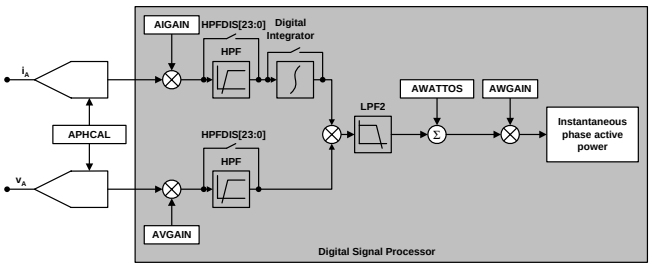

Figure 42. Total Active Power Data Path

If the phase currents and voltages contain only the fundamental component, are in phase (that is $\varphi_1 = \gamma_1 = 0$) and they correspond to full scale ADC inputs, then multiplying them results in an instantaneous power signal that has a dc component $V_1 \cdot I_1$ and a sinusoidal component $V_1 \cdot I_1 \cos(2\omega t)$. Figure 43 shows the corresponding waveforms.

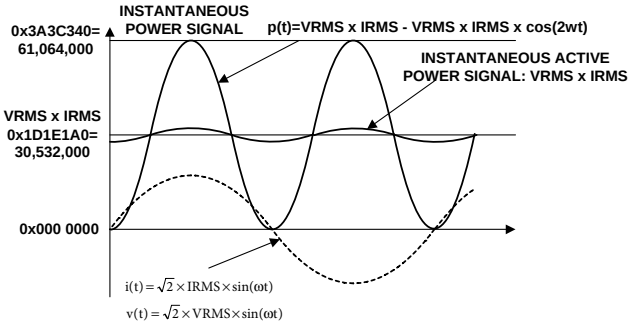

Figure 43. Active Power Calculation

Because LPF2 does not have an ideal brick wall frequency response (see Figure 44), the active power signal has some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Because the ripple is sinusoidal in nature, it is removed when the active power signal is integrated over time to calculate the energy.

TBD

Figure 44. Frequency Response of the LPF Used to Filter Instantaneous Power in Each Phase

The ADE7854 stores the instantaneous total phase active powers into AWATT[23:0], BWATT[23:0] and CWATT[23:0] registers. Their expression is:

$$xWATT = \sum_{k=1}^{\infty} \frac{U_k}{U_{FS}} \cdot \frac{I_k}{I_{FS}} \cdot \cos(\varphi_k - \gamma_k) \cdot PMAX \cdot \frac{1}{2^4} \quad (17)$$

where: x=A, B, C,

U_{FS}, I_{FS} are the rms values of the phase voltage and current when the ADC inputs are at full scale.

PMAX=33,516,139 is the instantaneous power computed when the ADC inputs are at full scale and in phase.

The xWATT[23:0], x=A,B,C waveform registers may be accessed using various serial ports. See Waveform Sampling Mode chapter for more details.

Active Power Gain Calibration

Note that the average active power result from the LPF2 output in each phase can be scaled by ±100% by writing to the phase's watt gain 24-bit register (AWGAIN[23:0], BWGAIN[23:0], CWGAIN[23:0]). xWGAIN, x=A,B,C registers are placed in each phase of the total active power data path. The watt gain registers are twos complement, signed registers and have a resolution of 2^{-23}/LSB. Equation (18) describes mathematically the function of the watt gain registers.

$$\text{Average Power Data} = \text{LPF2 Output} \times \left(1 + \frac{\text{Watt Gain } \textit{Register}}{2^{23}}\right) \quad (18)$$

The output is scaled by −50% by writing 0xC00000 to the watt gain registers and increased by +50% by writing 0x400000 to them. These registers can be used to calibrate the active power (or energy) calculation in the ADE7854 for each phase.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words and the DSP works on 28 bits. Similar to registers presented in Figure 16, AWGAIN, BWGAIN, CWGAIN 24-bit signed registers are accessed as 32-bit registers with 4 most significant bits padded with 0s and sign extended to 28 bits.

Active Power Offset Calibration

The ADE7854 also incorporates a watt offset 24-bit register on each phase and on each active power. AWATTOS[23:0], BWATTOS[23:0], and CWATTOS[23:0] registers compensate the offsets in the total active power calculations. These are signed twos complement, 24-bit registers that are used to remove offsets in the active power calculations. An offset can exist in the power calculation due to crosstalk between channels on the PCB or in the chip itself. The offset calibration allows the contents of the active power register to be maintained at 0 when no power is being consumed. One LSB in the active power offset register is equivalent to 1 LSB in the active power multiplier output. With full scale current and voltage inputs, the LPF2 output is PMAX=33,516,139. At -80dB down from the full scale (active power scaled down 10^4 times), one LSB of the active power offset register represents 0.032% of PMAX.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words and the DSP works on 28 bits. Similar to registers presented in Figure 16, AWATTOS, BWATTOS, CWATTOS 24-bit signed registers are accessed as 32-bit registers with 4 most significant bits padded with 0s and sign extended to 28 bits.

Sign of Active Power Calculation

Note that the average active power is a signed calculation. If the phase difference between the current and voltage waveform is more than 90°, the average power becomes negative. Negative power indicates that energy is being injected back on the grid. The ADE7854 has a sign detection circuitry for total active power calculations. As will be seen in the Active Energy Calculation section, the active energy accumulation is performed in two stages. Every time a sign change is detected in the energy accumulation at the end of the first stage, that is after the energy accumulated into the 48 bit accumulator reaches WTHR[47:0] threshold, a dedicated interrupt is triggered. The sign of each phase active power may be read in PHSIGN[15:0] register.

Bits 8, 7, 6 (REVAPC, REVAPB and respectively REVAPA) in STATUS0[31:0] are set when a sign change occurs in the total active power.

Bits 2, 1, 0 (CWSIGN, BWSIGN and respectively AWSIGN) in PHSIGN[15:0] register are set simultaneously with REVAPC, REVAPB and REVAPA bits. They indicate the sign of the power. When they are 0, the total active power is positive. When they are 1, the total active power is negative.

Interrupts attached to the bits 8, 7, 6 (REVAPC, REVAPB and respectively REVAPA) in STATUS0[31:0] register may be enabled by setting bits 8,7,6 in MASK0[31:0] register. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever a change of sign occurs. To find the phase that triggered the interrupt, PHSIGN[15:0] register is read immediately after reading STATUS0[31:0]. Then the status bit is cleared and $\overline{\text{IRQ0}}$ pin is set back high by writing STATUS0 register with the corresponding bit set to 1.

Active Energy Calculation

As previously stated, power is defined as the rate of energy flow. This relationship can be expressed mathematically as

$$Power = \frac{d\textit{Energy}}{dt} \quad (19)$$

Conversely, *Energy* is given as the integral of power.

$$\textit{Energy} = \int p(t)dt \quad (20)$$

Total active energy accumulation is signed. Negative energy is subtracted from the active energy contents.

The ADE7854 achieves the integration of the active power signal in two stages (see Figure 45). The process is identical for both total and fundamental active powers. The first stage is done inside the DSP: every 125µsec (8KHz frequency), the instantaneous phase total or fundamental active power is accumulated into an internal 56-bit register. When a threshold is reached, a pulse is generated at processor port and the threshold is subtracted from the internal register. The sign of the energy in this moment is considered the sign of the active power (see Sign of Active Power Calculation section for details). The second stage is done outside the DSP and consists in accumulating the pulses generated by the processor into internal 32-bit accumulation registers. The content of these registers is transferred to watt-hr registers xWATTHR[31:0], x=A,B,C when these registers are accessed. AWATTHR[31:0],

BWATTHR[31:0] and CWATTHR[31:0] represent the phase total active powers.

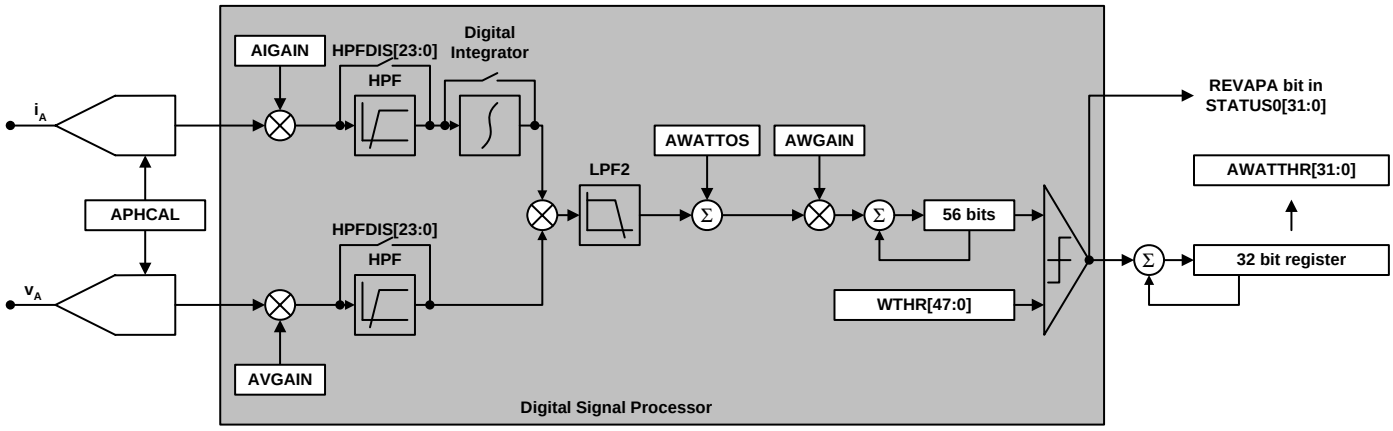

Figure 45. ADE7854 Total Active Energy Accumulation

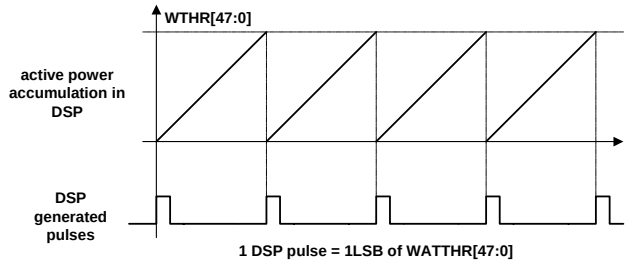

Figure 46. Active Power Accumulation inside DSP

Figure 46 explains this process. The WTHR[47:0] 48-bit signed register contains the threshold. It is introduced by the user and is common for both total and fundamental phase active powers. Its value depends on how much energy is assigned to 1LSB of watt-hour registers. Let's suppose a derivative of wh [10^n wh], n an integer, is desired as 1LSB of WATTHR. Then WTHR is computed using the following expression:

$$WTHR = \frac{PMAX \cdot f_s \cdot 3600 \cdot 10^n}{U_{FS} \cdot I_{FS}} \quad (21)$$

where:

PMAX=33,516,139=0x1FF6A6B is the instantaneous power computed when the ADC inputs are at full scale.

f_s=8KHz is the frequency with which the DSP computes the instantaneous power.

U_{FS}, I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.

The maximum value that may be written on WTHR[47:0] is 2^{47}-1. The minimum value is 0x0, but it is recommended to write a number equal or greater than PMAX. Negative numbers should never be used.

The WTHR[47:0] is a 48-bit register. As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words. As presented in Figure 47, WTHR register is accessed as two 32-bit registers (WTHR1[31:0] and WTHR0[31:0]), each having 8 most significant bits padded with 0s.

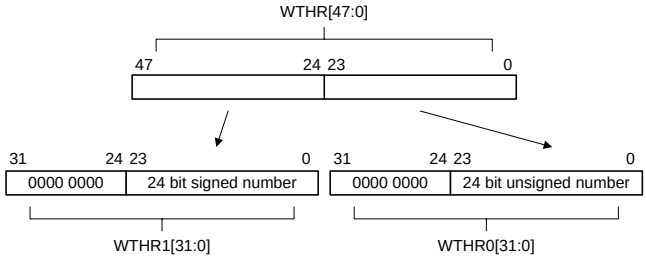

Figure 47. WTHR[47:0] is communicated as two 32-bit registers

This discrete time accumulation or summation is equivalent to integration in continuous time following the description in expression (22).

$$Energy = \int p(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} p(nT) \times T \right\} \quad (22)$$

where:

n is the discrete time sample number.
T is the sample period.

In the ADE7854, the total phase active powers are accumulated in AWATTHR[31:0], BWATTHR[31:0] and CWATTHR[31:0] 32-bit signed registers. The active energy register content can roll over to full-scale negative (0x80000000) and continue increasing in value when the active power is positive. Conversely, if the active power is negative, the energy register would underflow to full-scale positive (0x7FFFFFFF) and continue decreasing in value.

Bit 0 (AEHF) in STATUS0[31:0] register is set when bit 30 of one of xWATTHR, x=A, B, C registers changes, signifying one of these registers is half full. If the active power is positive, the watt-hr register becomes half full when it increments from 0x3FFF FFFF to 0x4000 0000. If the active power is negative, the watt-hr register becomes half full when it decrements from 0xC000 0000 to 0xBFFF FFFF.

Setting bit 0 in MASK0[31:0] register enables the AEHF interrupts. If enabled, the $\overline{IRQ0}$ pin is set low and the status bit is set to 1 whenever one of the energy registers xWATTHR (for AEHF interrupt), x=A, B, C becomes half full. The status bit is cleared and $\overline{IRQ0}$ pin is set to logic high by writing STATUS0 register with the corresponding bit set to 1.

Setting bit 6 (RSTREAD) of LCYMODE[7:0] register enables a read-with-reset for all watt-hr accumulation registers, that is, the registers are reset to 0 after a read operation.

Integration Time Under Steady Load

The discrete time sample period (T) for the accumulation register is 125µs (1/8KHz). With full-scale sinusoidal signals on the analog inputs and the watt gain registers set to 0x00000, the average word value from each LPF2 is PMAX=33,516,139=0x1FF6A6B. If the WTHR[47:0] threshold is set at PMAX level, this means the DSP generates a pulse that is added at watt-hr registers every 125 µs.

The maximum value that can be stored in the watt-hr accumulation register before it overflows is $2^{31} - 1$ or 0x7FFFFFFF. The integration time is calculated as

$$\text{Time} = 0x7FFF,FFFF \times 125\mu s = 74h33\,\text{min}\,55s \quad (23)$$

Energy Accumulation Modes

The active power accumulated in each watt-hr accumulation 32-bit register (AWATTHR, BWATTHR, CWATTHR) depends on the configuration of bits 5, 4 (CONSEL) in ACCMODE[7:0] register. The different configurations are described in Table 12.

Table 12. Inputs to Watt-Hr Accumulation Registers

CONSEL	AWATTHR	BWATTHR	CWATTHR
00	VA × IA	VB × IB	VC × IC
01	VA × IA	0	VC × IC
10	VA × IA	VB × IB VB = –VA – VC	VC × IC
11	VA × IA	VB × IB VB = –VA	VC × IC

Depending on the poly-phase meter service, the appropriate formula should be chosen to calculate the active energy. The American ANSI C12.10 Standard defines the different configurations of the meter. Table 13 describes which mode should be chosen in these different configurations.

Table 13. Meter Form Configuration

ANSI Meter Form		CONSEL
5S/13S	3-Wire Delta	01
6S/14S	4-Wire Wye	10
8S/15S	4-Wire Delta	11
9S/16S	4-Wire Wye	00

Bits 1, 0 (WATTACC[1:0]) in ACCMODE[7:0] register determine how CF frequency output may be generated function of the total and fundamental active powers. While the watt-hr accumulation registers accumulate the active power in a signed format, the frequency output may be generated in signed mode or in absolute mode, function of WATTACC[1:0]. See ENERGY to FREQUENCY CONVERSION chapter for details.

Line Cycle Active Energy Accumulation Mode

In line cycle energy accumulation mode, the energy accumulation is synchronized to the voltage channel zero crossings so that active energy is accumulated over an integral number of half line cycles. The advantage of summing the active energy over an integer number of line cycles is that the sinusoidal component in the active energy is reduced to 0. This eliminates any ripple in the energy calculation and allows the energy to be accumulated accurately over a shorter time. By using the line cycle energy accumulation mode, the energy calibration can be greatly simplified, and the time required to calibrate the meter can be significantly reduced. In line cycle energy accumulation mode, the ADE7854 transfers the active energy accumulated in the 32-bit internal accumulation registers into xWATHHR[31:0], x=A,B,C registers after an integral number of line cycles, as shown in Figure 48. The number of half line cycles is specified in the LINECYC[15:0] register.

The line cycle energy accumulation mode is activated by setting bit 0 (LWATT) in the LCYCMODE[7:0] register. The energy accumulation over an integer number of half line cycles is written to the watt-hr accumulation registers after LINECYC[15:0] number of half line cycles are detected. When using the line cycle accumulation mode, the bit 6 (RSTREAD) of the LCYCMODE[7:0] register should be set to Logic 0 because the read with reset of watt-hr registers is not available in this mode.

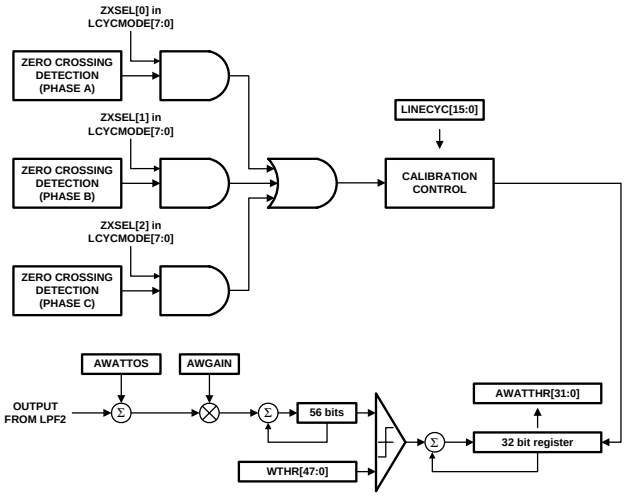

Figure 48. ADE7854 Line Cycle Active Energy Accumulation Mode

Phase A, Phase B, and Phase C zero crossings are, respectively, included when counting the number of half-line cycles by setting bits 5, 4, 3 (ZXSEL) in the LCYCMODE[7:0] register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Only one phase should be selected at a time for inclusion in the zero crossings count during line accumulation.

The number of zero crossings is specified by the LINECYC[15:0] 16-bit unsigned register. The ADE7854 can accumulate active power for up to 65535 combined zero crossings. Note that the internal zero-crossing counter is always active. By setting bit 0 (LWATT) in LCYCMODE[7:0] register, the first energy accumulation result is, therefore, incorrect. Writing to the LINECYC[15:0] register when the LWATT bit is set resets the zero-crossing counter, thus ensuring that the first energy accumulation result is accurate.

At the end of an energy calibration cycle, the bit 5 (LENERGY) in the STATUS0[31:0]register is set. If the corresponding mask bit in the MASK0[31:0] interrupt mask register is enabled, the $\overline{\text{IRQ0}}$ pin also goes active low. The status bit is cleared and $\overline{\text{IRQ0}}$ pin is set back high by writing STATUS0 register with the corresponding bit set to 1.

Because the active power is integrated on an integer number of half-line cycles in this mode, the sinusoidal components are reduced to 0, eliminating any ripple in the energy calculation. Therefore, total energy accumulated using the line-cycle accumulation mode is

$$e = \int_{t}^{t+nT} p(t)dt = nT \sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k) \quad (24)$$

where *nT* is the accumulation time.

Note that line cycle active energy accumulation uses the same signal path as the active energy accumulation. The LSB size of these two methods is equivalent.

APPARENT POWER CALCULATION

Apparent power is defined as the maximum power that can be delivered to a load. One way to obtain the apparent power is by multiplying the voltage rms value by the current rms value:

$$S = VRMS \times IRMS \quad (25)$$

where *S* is the apparent power and *VRMS* and *IRMS* are the rms voltage and current, respectively. It is also called the arithmetic apparent power.

The ADE7854 computes the arithmetic apparent power on each phase. Figure 49 illustrates the signal processing in each phase for the calculation of the apparent power in the ADE7854. As VRMS and IRMS contain all harmonic information, the apparent power computed by the ADE7854 is a total apparent power.

The ADE7854 stores the instantaneous phase apparent powers into AVA[23:0], BVA[23:0] and CVA[23:0] registers. Their expression is:

$$xVA = \frac{U}{U_{FS}} \cdot \frac{I}{I_{FS}} \cdot PMAX \cdot \frac{1}{2^4} \quad (26)$$

where:

x=A,B,C

U, I are the rms values of the phase voltage and current.

U_{FS},I_{FS} are the rms values of the phase voltage and current when the ADC inputs are at full scale.

PMAX=33,516,139 is the instantaneous power computed when the ADC inputs are at full scale and in phase.

The xVA[23:0], x=A,B,C waveform registers may be accessed using various serial ports. See Waveform Sampling Mode chapter for more details.

The ADE7854 may compute the apparent power in an alternative way by multiplying the phase rms current by an rms voltage introduced externally. See Apparent Power Calculation using VNOM section for details.

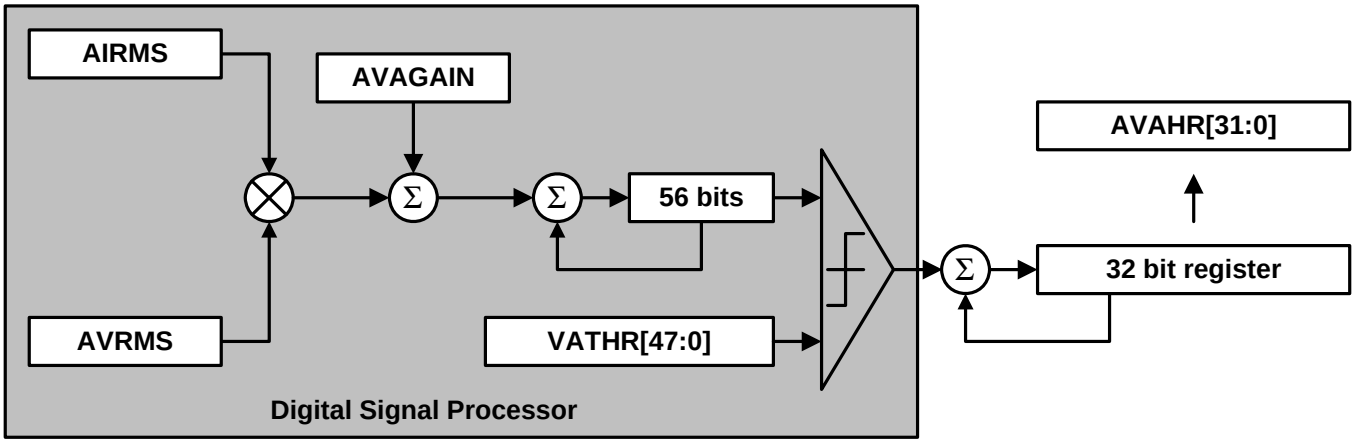

Figure 49. Apparent Power data flow and Apparent Energy Accumulation

Apparent Power Gain Calibration

The average apparent power result in each phase can be scaled by ±100% by writing to the phase's VAGAIN 24-bit register (AVAGAIN[23:0], BVAGAIN[23:0] or CVAG AIN[23:0]). The VAGAIN registers are twos complement, signed registers and have a resolution of 2^{-23}/LSB. The function of the VA gain registers is expressed mathematically as

Average Apparent Power =

$$VRMS \times IRMS \times \left(1 + \frac{\text{VAGAIN Register}}{2^{23}}\right) \quad (27)$$

The output is scaled by –50% by writing 0xC00000 to the VA gain registers and increased by +50% by writing 0x400000 to them. These registers can be used to calibrate the apparent power (or energy) calculation in the ADE7854 for each phase.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words and the DSP works on 28 bits. Similar to registers presented in Figure 16, AVAGAIN, BVAGAIN, CVAGAIN 24-bit registers are accessed as 32-bit registers with 4 most significant bits padded with 0s and sign extended to 28 bits.

Apparent Power Offset Calibration

Each rms measurement includes an offset compensation register to calibrate and eliminate the dc component in the rms value (see the Root Mean Square Measurement section). The voltage and current rms values are then multiplied together in the apparent power signal processing. As no additional offsets are created in the multiplication of the rms values, there is no specific offset compensation in the apparent power signal processing. The offset compensation of the apparent power measurement in each phase should be done by calibrating each individual rms measurement.

Apparent Power Calculation using VNOM

The ADE7854 may compute the apparent power multiplying the phase rms current by an rms voltage introduced externally in VNOM[23:0] 24-bit unsigned register. When one of bits 13, 12, 11 (VNOMCEN, VNOMBEN, VNOMAEN) in COMPMODE[15:0] register is set to 1, the apparent power in the corresponding phase (phase x for VNOMxEN, x=A,B,C) is computed in this way. When bits VNOMxEN are cleared to 0, the default value, then the arithmetic apparent power is computed.

VNOM[23:0] register contains a number determined by U, the desired rms voltage and U_{FS}, the rms value of the phase voltage when the ADC inputs are at full scale:

$$VNOM = \frac{U}{U_{FS}} \cdot 4{,}191{,}400 \quad (28)$$

Usually U is the nominal phase rms voltage.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words. Similar to the register presented in Figure 17, VNOM 24-bit register is accessed as a 32-bit register with 8 most significant bits padded with 0s.

Apparent Energy Calculation

Apparent energy is defined as the integral of apparent power.

$$ApparentEnergy = \int s(t)dt \quad (29)$$

Similar to active and reactive powers, the ADE7854 achieves the integration of the apparent power signal in two stages (see Figure 49). The first stage is done inside the DSP: every 125µsec (8KHz frequency), the instantaneous phase apparent power is accumulated into an internal 56-bit register. When a threshold is reached, a pulse is generated at processor port and the threshold is subtracted from the internal register. The second stage is done outside the DSP and consists in accumulating the pulses generated by the processor into internal 32-bit accumulation registers. The content of these registers is transferred to va-hr registers xVAHR[31:0], x=A, B, C when these registers are accessed.

Figure 46 from the Active Energy Calculation section explains this process. The VATHR[47:0] 48-bit register contains the threshold. Its value depends on how much energy is assigned to 1LSB of VA-hour registers. Let's suppose a derivative of VAh [10^n VAh], n an integer, is desired as 1LSB of VAHR. Then VATHR may be computed using the following expression:

$$VATHR = \frac{PMAX \cdot f_s \cdot 3600 \cdot 10^n}{U_{FS} \cdot I_{FS}}$$

where:

PMAX=33,516,139=0x1FF6A6B, the instantaneous power computed when the ADC inputs are at full scale.

f_s=8KHz is the frequency with which the DSP computes the instantaneous power.

U_{FS}, I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.

The VATHR[47:0] is a 48-bit register. As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words. Similar to the WTHR[47:0] register presented in Figure 47, VATHR[47:0] is accessed as two 32-bit registers (VATHR1[31:0] and VATHR0[31:0]), each having 8 most significant bits padded with 0s.

This discrete time accumulation or summation is equivalent to integration in continuous time following the description in expression (30).

$$ApparentEnergy = \int s(t)dt = \lim_{T \to 0}\left\{\sum_{n=0}^{\infty} s(nT) \times T\right\} \quad (30)$$

where:

n is the discrete time sample number.
T is the sample period.

In the ADE7854, the phase apparent powers are accumulated in AVAHR[31:0], BVAHR[31:0] and CVAHR[31:0] 32-bit signed registers. The apparent energy register content can roll over to full-scale negative (0x80000000) and continue increasing in value when the apparent power is positive. Conversely, if because of offset compensation in rms data path, the apparent power is negative, the energy register would under flow to full-scale positive (0x7FFFFFFF) and continue decreasing in value.

Bit 4 (VAEHF) in STATUS0[31:0] register is set when bit 30 of one of xVAHR, x=A,B,C registers changes, signifying one of these registers is half full. As the apparent power is always positive and xVAHR, x=A,B,C registers are signed, the VA-hr registers become half full when they increment from 0x3FFFFFFF to 0x4000 0000. Interrupts attached to bit VAEHF in STATUS0[31:0] register may be enabled by setting bit 4 in MASK0[31:0] register. If enabled, the $\overline{IRQ0}$ pin is set low and the status bit is set to 1 whenever one of the energy registers xVAHR, x=A,B,C becomes half full. The status bit is cleared and $\overline{IRQ0}$ pin is set back high by writing STATUS0 register with the corresponding bit set to 1.

Setting bit 6 (RSTREAD) of LCYMODE[7:0] register enables a read-with-reset for all va-hr accumulation registers, that is, the registers are reset to 0 after a read operation.

Integration Time Under Steady Load

The discrete time sample period (T) for the accumulation register is 125µs (1/8 KHz). With full-scale pure sinusoidal signals on the analog inputs, the average word value representing the apparent power is PMAX. If the VATHR threshold is set at PMAX level, this means the DSP generates a pulse that is added at VA-hr registers every 125 µs.

The maximum value that can be stored in the va-hr accumulation register before it overflows is $2^{31} - 1$ or 0x7FFFFFFF. The integration time is calculated as

$$\text{Time} = 0x7FFF,FFFF \times 125\mu s = 74h33\,\text{min}\,55s \quad (31)$$

Energy Accumulation Mode

The apparent power accumulated in each VA-hr accumulation register (AVAHR[31:0], BVAHR[31:0] or CVAHR[31:0]) depends on the configuration of bits 5,4 (CONSEL) in the ACCMODE[7:0] register. The different configurations are described in Table 14.

Table 14. Inputs to VA-Hr Accumulation Registers

CONSEL[1,0]	AVAHR	BVAHR	CVAHR
00	AVRMS × AIRMS	BVRMS × BIRMS	CVRMS × CIRMS
01	AVRMS × AIRMS	0	CVRMS × CIRMS
10	AVRMS × AIRMS	BVRMS × BIRMS VB=-VA-VC	CVRMS × CIRMS
11	AVRMS × AIRMS	BVRMS × BIRMS VB=-VA	CVRMS × CIRMS

Line Cycle Apparent Energy Accumulation Mode

As mentioned in Line Cycle Active Energy Accumulation Mode section, in line cycle energy accumulation mode, the energy accumulation can be synchronized to the voltage channel zero crossings so that apparent energy can be accumulated over an integral number of half line cycles. In this mode, the ADE7854 transfers the apparent energy accumulated in the 32-bit internal accumulation registers into xVAHR[31:0], x=A,B,C registers after an integral number of line cycles, as shown in Figure 50. The number of half line cycles is specified in the LINECYC[15:0] register.

The line cycle apparent energy accumulation mode is activated by setting bit 2 (LVA) in the LCYCMODE[7:0] register. The apparent energy accumulated over an integer number of zero crossings is written to the VA-hr accumulation registers after the LINECYC number of zero crossings is detected. When using the line cycle accumulation mode, bit 6 (RSTREAD) of the LCYCMODE[7:0] register should be set to Logic 0 because the read with reset of VA-hr registers is not available in this mode.

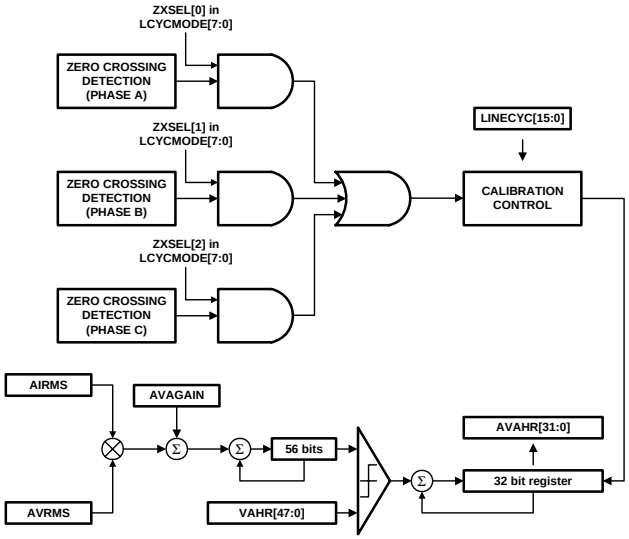

Figure 50. ADE7854 Line Cycle Apparent Energy Accumulation Mode

Phase A, Phase B, and Phase C zero crossings are, respectively, included when counting the number of half-line cycles by setting bits 5,4,3 (ZXSEL) in the LCYCMODE[7:0] register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Only one phase should be selected at a time for inclusion in the zero crossings count during calibration.

For details on setting LINECYC[15:0] register and the interrupt LENERGY associated with the line cycle accumulation mode, see Line Cycle Active Energy Accumulation Mode section.

WAVEFORM SAMPLING MODE

The waveform samples of the current and voltage waveform, the active and apparent power multiplier outputs are stored every 125µsec (8KHz rate) into 24-bit signed registers that may be accessed through various serial ports of the ADE7854. Table 15 presents the list of the registers and their description.

Table 15. Waveform registers list

Register	Description	Register	Description
IAWV	Phase A current	AWATT	Phase A active power
IBWV	Phase B current	BWATT	Phase B active

Register	Description	Register	Description
			power
ICWV	Phase C current	CWATT	Phase C active power
VAWV	Phase A voltage	AVA	Phase A apparent power
VBWV	Phase B voltage	BVA	Phase B apparent power
VCWV	Phase C voltage	CVA	Phase C apparent power

The bit 17 (DREADY) in STATUS0[31:0] register can be used to signal when the registers mentioned in Table 15 may be read using I²C or SPI serial ports. An interrupt attached to the flag may be enabled by setting bit 17 (DREADY) in MASK0[31:0] register. See Digital Signal Processor chapter for more details on bit DREADY.

The ADE7854 contains a High Speed Data Capture (HSDC) port that is specially designed to provide fast access to the waveform sample registers. See HSDC Interface section for more details.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words. All registers listed in Table 15 are transmitted signed extended from 24 to 32 bits (see Figure 18).

ENERGY TO FREQUENCY CONVERSION

The ADE7854 provides 3 frequency output pins: CF1, CF2 and CF3.

CF3 pin is multiplexed with HSCLK pin of HSDC interface. When HSDC is enabled, the CF3 functionality is disabled at the pin. CF1 and CF2 pins are always available. After initial calibration at manufacturing, the manufacturer or end customer verifies the energy meter calibration. One convenient way to verify the meter calibration is to provide an output frequency proportional to the active, reactive or apparent powers under steady load conditions. This output frequency can provide a simple, single-wire, optically isolated interface to external calibration equipment. Figure 51 illustrates the energy-to-frequency conversion in the ADE7854.

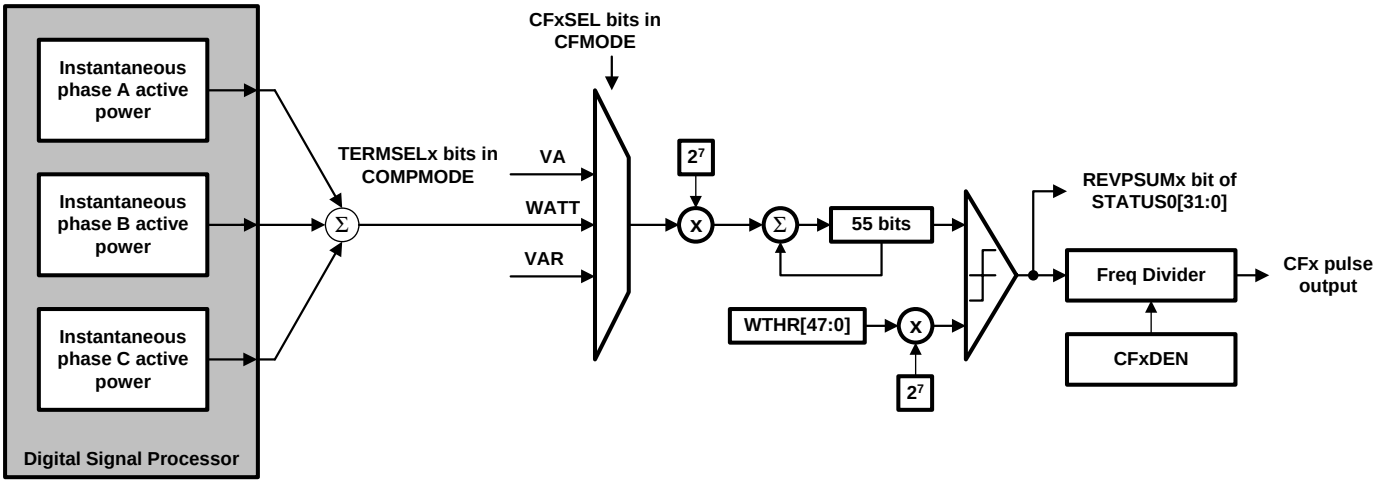

Figure 51. ADE7854 Energy to Frequency Conversion

The DSP computes the instantaneous values of all phase powers: total active, fundamental active, total reactive, fundamental reactive and apparent. The process in which the energy is sign accumulated in various hr registers (watt-hr, var-hr and VA-hr) has already been described in Energy Calculation chapters. In the energy to frequency conversion process, the instantaneous powers are used to generate signals at frequency output pins CF1, CF2 and CF3.

One digital to frequency converter is used for every CF pin. Every converter sums certain phase powers and generates a signal proportional to the sum. Two sets of bits decide what powers are converted.

First, bits 2, 1, 0 (TERMSEL1[2:0]), 5, 4, 3 (TERMSEL2[2:0]) and 8, 7, 6 (TERMSEL3[2:0]) of COMPMODE[15:0] register decide which phases or which combination of phases are added. TERMSEL1 bits refer to CF1 pin, TERMSEL2 bits refer to CF2 pin and TERMSEL3 bits refer to CF3 pin. TERMSELx[0] bits, x=1, 2, 3 manage phase A. When set to 1, phase A power is included in the sum of powers at CFx converter. When cleared to 0, phase A power is not included. TERMSELx[1] bits manage phase B, TERMSELx[2] bits manage phase C. Setting all TERMSELx bits to 1 means all 3 phase powers are added at CFx converter. Clearing all TERMSELx bits to 0 means no phase power is added and no CF pulse is generated.

Second, bits 2, 1, 0 (CF1SEL[2:0]), 5, 4, 3 (CF2SEL[2:0]) and 8, 7, 6 (CF3SEL[2:0]) in CFMODE[15:0] register decide what type power is used at the inputs of CF1, CF2 and respective CF3 converters. Table 16 shows the values that CFxSEL may have: total active or apparent powers.

By default, TERMSELx bits are all 1 and CF1SEL bits are 000, CF2SEL bits are 001 and CF3SEL bits are 010. This means that by default, the CF1 digital to frequency converter produces signals proportional to the sum of all 3 phase total active powers and CF3 produces signals proportional to apparent powers. CF2 digital to frequency converter does not produce a signal as its default setting is reserved.

Table 16. CFxSEL, x=1,2,3 bits description

CFxSEL	Description	Registers latched when CFxLATCH=1
000	CFx signal proportional to the sum of total phase active powers	AWATTHR, BWATTHR, CWATTHR
001	Reserved	
010	CFx signal proportional to the sum of phase apparent powers	AVAHR, BVAHR, CVAHR
011-111	Reserved	

Similar to the energy accumulation process, the energy to frequency conversion is done in two stages. In the first stage, the instantaneous phase powers obtained from the DSP at 8KHz rate are shifted left 7 bits and then accumulated into a 55 bit register at 1MHz rate. When a threshold is reached, a pulse is generated and the threshold is subtracted from the internal register. The sign of the energy in this moment is considered the sign of the sum of phase powers (see Sign of sum of phase powers in CFx data path section for details). The threshold is the same threshold used in various active and appearent energy accumulators in DSP, WTHR[47:0] or VATHR[47:0], but this time it is shifted left 7 bits. The advantage of accumulating the instantaneous powers at 1MHz rate is that the ripple at CFx pins is greatly diminished. The second stage consists in a frequency divider by CFxDEN[15:0], x=1,2,3, 16-bit unsigned registers. The values of CFxDEN depend on the meter constant (MC), measured in impulses/kwh and how much energy is assigned to 1LSB of various energy registers: WATT-hr and VA-hr. Let's suppose a derivative of wh, [10^n wh], n a positive or negative integer, is desired as 1LSB of WATTHR. Then CFxDEN is:

$$\text{CFxDEN} = \frac{10^3}{\text{MC[imp/kwh]} \cdot 10^n} \qquad (32)$$

The derivative of wh must be chosen in such a way to obtain a CFxDEN greater than 1. Fractional results cannot be accommodated by the frequency converter, so the result of the division has to be rounded to the nearest integer. If CFxDEN is set equal to 0, then the ADE7854 considers it as equal to 1.

The pulse output for all digital to frequency converters stays low for 80ms if the pulse period is larger than 160ms (6.25Hz). If the pulse period is smaller than 160ms, the duty cycle of the pulse output is 50%. The pulse output is active low and should be preferably connected to an LED as shown in Figure 52.

Bits 11, 10, 9 (CF3DIS , CF2DIS and CF1DIS) of CFMODE[15:0] register decide if the frequency converter output is generated at CF3, CF2 or CF1 pins. When bit CFxDIS, x=1, 2, 3 is set to 1, the default value, the CFx pin is disabled and the pin stays high. When bit CFxDIS is cleared to 0, the correspondent CFx pin output generates an active low signal.

Bits 16, 15, 14 (CF3, CF2, CF1) in interrupt mask register MASK0[31:0] manage CF3, CF2 and CF1 related interrupts. When CFx, x=1, 2, 3 bits are set, whenever a high to low transition at corresponding frequency converter output occurs, an interrupt $\overline{\text{IRQ0}}$ is triggered and a status bit in STATUS0[31:0] register is set to 1. The interrupt is available even if the CFx output is not enabled by CFxDIS bits in CFMODE[15:0].

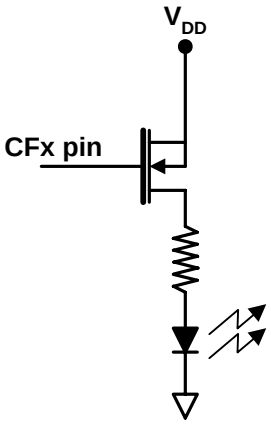

Figure 52. CF pin recommended connection

Synchronizing energy registers with CFx outputs

The ADE7854 contains a feature that allows synchronizing the content of phase energy accumulation registers with the generation of a CFx pulse. When a high to low transition at one frequency converter output occurs, the content of all internal phase energy registers that relate to the power being output at CFx pin is latched into hr registers and then is reset to 0. See Table 16 for the list of registers that are latched based on CFxSEL[2:0] bits in CFMODE[15:0] register. All 3 phase registers are latched independent of TERMSELx bits of COMPMODE[15:0] register. The process is shown in Figure 53 for CF1SEL[2:0]=010 (apparent powers contribute at CF1 pin) and CFCYC=2.

CFCYC[7:0] 8-bit unsigned register contains the number of high to low transitions at frequency converter output between two consecutive latches. Writing a new value into CFCYC[7:0] register during a high to low transition at any CFx pin should be avoided.

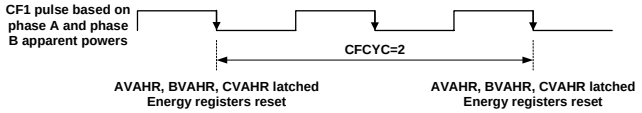

Figure 53.Synchronizing AVAHR and BVAHR with CF1

Bits 14, 13, 12 (CF3LATCH, CF2LATCH and CF1LATCH) of CFMODE[15:0] register enable this process when set to 1. When cleared to 0, the default state, no latch occurs. The process is available even if the CFx output is not enabled by CFxDIS bits in CFMODE[15:0].

CF outputs for various accumulation modes

The bits 1, 0 (WATTACC[1:0]) in ACCMODE[7:0] register determine the accumulation modes of the total active powers when signals proportional to the total active powers are chosen at CFx pins (bits CFxSEL[2:0], x=1,2,3 in CFMODE[15:0] register are equal to 000 or to 011). When WATTACC[1:0]=00, the default value, the active powers are sign accumulated before entering the energy to frequency converter. Figure 54 presents the way signed active power accumulation works. Note that in this mode, the CF pulses are perfectly synchronized with the active energy accumulated in watt-hr registers because the powers are sign accumulated in both data paths.

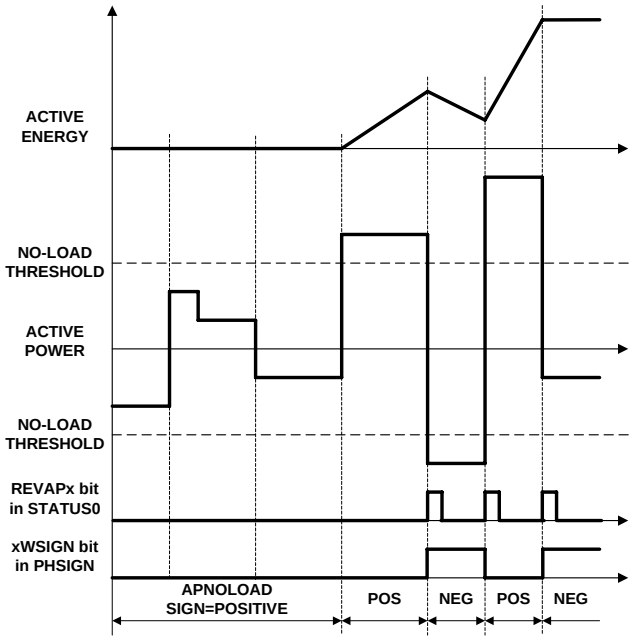

Figure 54. Active power signed accumulation mode

When WATTACC[1:0]=11, the active powers are accumulated in absolute mode. When the powers are negative, they change sign and are accumulated together with the positive power. Figure 55 presents the way absolute active power accumulation works. Note that in this mode, the watt-hr registers continue to accumulate active powers in signed mode, even if the CF pulses are generated based on the absolute accumulation mode.

Sign of sum of phase powers in CFx data path

The ADE7854 has a sign detection circuitry for the sum of phase powers that are used in CFx, x=1, 2, 3 data path. As seen in the beginning of ENERGY to FREQUENCY CONVERSION chapter, the energy accumulation in CFx data path is executed in two stages. Every time a sign change is detected in the energy accumulation at the end of the first stage, that is after the energy accumulated into the 55 bit accumulator reaches one of WTHR[47:0] or VATHR[47:0] thresholds, a dedicated interrupt may be triggered synchronously with the corresponding CF pulse. The sign of each sum may be read in PHSIGN[15:0] register.

Bits 18, 13, 9 (REVPSUM3, REVPSUM2, and respectively REVPSUM1) of STATUS0[31:0] register are set to 1 when a sign change of the sum of powers in CF3, CF2 or CF1 data paths occurs. To correlate these events with the pulses generated at CFx pins, after a sign change occurs, bits REVPSUM3, REVPSUM2 and REVPSUM1 are set in the same moment in which a high to low transition at CF3, CF2 and respectively CF1 pin occurs.

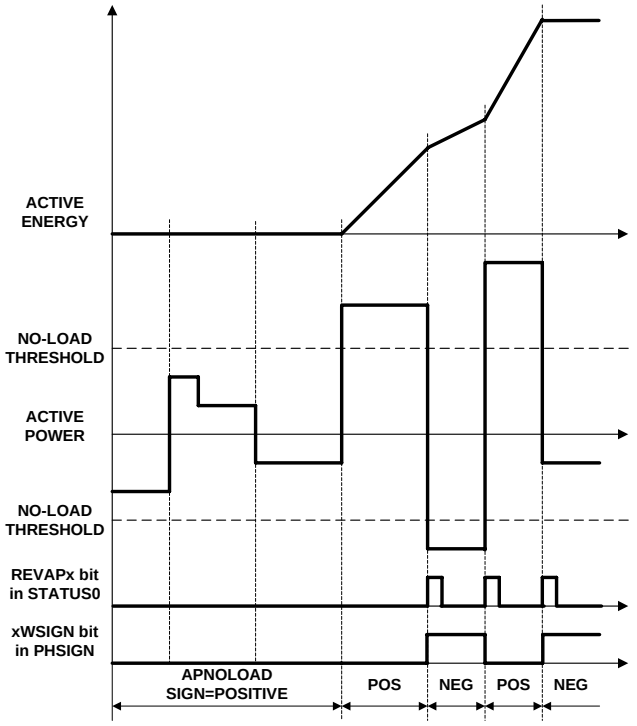

Figure 55. Active power absolute accumulation mode

Bits 8, 7, 3 (SUM3SIGN, SUM2SIGN and respectively SUM1SIGN) of PHSIGN[15:0] register are set in the same moment with bits REVPSUM3, REVPSUM2 and REVPSUM1 and indicate the sign of the sum of phase powers. When cleared to 0, the sum is positive. When set to 1, the sum is negative.

Interrupts attached to the bits 18, 13, 9 (REVPSUM3, REVPSUM2, and respectively REVPSUM1) in STATUS0[31:0] register may be enabled by setting bits 18, 13 , 9 in MASK0[31:0] register. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever a change of sign occurs. To find the phase that triggered the interrupt, PHSIGN[15:0] register is read immediately after reading STATUS0[31:0]. Then the status bit is cleared and $\overline{\text{IRQ0}}$ pin is set back high by writing STATUS0 register with the corresponding bit set to 1.

NO-LOAD CONDITION

The no-load condition is defined in metering equipment standards as occurring when the voltage is applied to the meter and no current flows in the current circuit. To eliminate any creep effects in the meter, the ADE7854 contains two separate no-load detection circuits: one related to the total active powers, and one related to the apparent powers.

No-load detection based on total active power

This no-load condition is triggered when the absolute values of phase total active powers are less than or equal to a threshold indicated in APNOLOAD[23:0] signed 24-bit register. In this case, the total active energy on that phase is not accumulated and no CF pulses are generated based on it. APNOLOAD[24:0] represents the positive no-load level of total active power relative to PMAX, the maximum total active power obtained when full scale voltages and currents are provided at ADC inputs. The expression used to compute APNOLOAD[23:0] signed 24-bit value is:

$$APNOLOAD = \frac{U_n}{U_{FS}} \cdot \frac{I_{noload}}{I_{FS}} \cdot PMAX \qquad (33)$$

where: PMAX=33,516,139=0x1FF6A6B, the instantaneous power computed when the ADC inputs are at full scale

U_{FS}, I_{FS}, the rms values of phase voltages and currents when the ADC inputs are at full scale.

U_n, the nominal rms value of phase voltage.

I_{noload}, the minimum rms value of phase current the meter starts measuring.

When APNOLOAD is set to negative values, the no-load detection circuit is disabled. Note that to ensure the good functionality of this no-load circuit, the 24-bit VARNOLOAD register placed at address 0x43B2 must be set at 0x800000.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words and the DSP works on 28 bits. APNOLOAD and VARNOLOAD 24-bit signed registers are accessed as 32-bit registers with 4 most significant bits padded with 0s and sign extended to 28 bits. See Figure 16 for details.

Bit 0 (NLOAD) in STATUS1[31:0] register is set when this no-load condition in one of the three phases is triggered. Bits 2, 1, 0 (NLPHASE[2:0]) in PHNOLOAD[15:0] register indicate the state of all phases relative to no-load condition and are set simultaneously with bit NLOAD in STATUS1[31:0]. NLPHASE[0] indicates the state of phase A , NLPHASE[1] the state of phase B, NLPHASE[2] the state of phase C. When bit NLPHASE[x], x=0, 1, 2 is cleared to 0, it means the phase is out of no-load condition. When set to 1, it means the phase is in no-load condition.

An interrupt attached to the bit 0 (NLOAD) in STATUS1[31:0] may be enabled by setting bit 0 in MASK1[31:0] register. If enabled, the $\overline{IRQ1}$ pin is set low and the status bit is set to 1 whenever one of three phases enters or exits this no-load condition. To find the phase that triggered the interrupt, PHNOLOAD[15:0] register is read immediately after reading STATUS1[31:0]. Then the status bit is cleared and $\overline{IRQ1}$ pin is set back high by writing STATUS1 register with the corresponding bit set to 1.

No-load detection based on apparent power

This no-load condition is triggered when the absolute value of phase apparent power is less than or equal to the threshold indicated in VANOLOAD[23:0] 24-bit signed register. In this case, the apparent energy of that phase is not accumulated and no CF pulses are generated based on this energy. VANOLOAD represents the positive no-load level of apparent power relative to PMAX, the maximum apparent power obtained when full scale voltages and currents are provided at ADC inputs. The expression used to compute VANOLOAD[23:0] signed 24-bit value is:

$$VANOLOAD = \frac{U_n}{U_{FS}} \cdot \frac{I_{noload}}{I_{FS}} \cdot PMAX$$

where: PMAX=33,516,139=0x1FF6A6B, the instantaneous apparent power computed when the ADC inputs are at full scale

U_{FS}, I_{FS}, the rms values of phase voltages and currents when the ADC inputs are at full scale.

U_n, the nominal rms value of phase voltage.

I_{noload}, the minimum rms value of phase current the meter starts measuring.

When VANOLOAD[23:0] is set to negative values, the no load detection circuit is disabled.

As previously stated, the serial ports of the ADE7854 work on 32, 16 or 8-bit words and the DSP works on 28 bits. Similar to registers presented inFigure 16, VANOLOAD 24-bit signed register is accessed as a 32-bit registers with 4 most significant bits padded with 0s and sign extended to 28 bits.

Bit 2 (VANLOAD) in STATUS1[31:0] register is set when this no-load condition in one of the three phases is triggered. Bits 8, 7, 6 (VANLPHASE[2:0]) in PHNOLOAD[15:0] register indicate the state of all phases relative to no-load condition and are set simultaneously with bit VANLOAD in STATUS1[31:0]. VANLPHASE[0] indicates the state of phase A , VANLPHASE[1] the state of phase B, VANLPHASE[2] the state of phase C. When bit VANLPHASE[x], x=0, 1, 2 is cleared to 0, it means the phase is out of no-load condition. When set to 1, it means the phase is in no-load condition.

An interrupt attached to the bit 2 (VANLOAD) in STATUS1[31:0] may be enabled by setting bit 2 in MASK1[31:0] register. If enabled, the $\overline{IRQ1}$ pin is set low and the status bit is set to 1 whenever one of three phases enters or exits this no-load condition. To find the phase that triggered the interrupt, PHNOLOAD[15:0] register is read immediately after reading STATUS1[31:0]. Then the status bit is cleared and

$\overline{IRQ1}$ pin is set back high by writing STATUS1 register with the corresponding bit set to 1.

CHECKSUM REGISTER

The ADE7854 has a checksum 32-bit register CHECKSUM[31:0] that ensures certain very important configuration registers maintain their desired value during normal power mode PSM0.

The registers covered by this register are MASK0[31:0], MASK1[31:0], COMPMODE[15:0], GAIN[15:0], CFMODE[15:0], CF1DEN[15:0], CF2DEN[15:0], CF3DEN[15:0], CONFIG[15:0], MMODE[7:0], ACCMODE[7:0], LCYCMODE[7:0], HSDC_CFG[7:0] and other six 8-bit reserved internal registers that always have default values. The ADE7854 computes the cyclic redundancy check (CRC) based on the IEEE802.3 standard. The registers are introduced one by one into a linear feedback shift register (LFSR) based generator starting with the less significant bit (as presented in Figure 56). The 32-bit result is written in CHECKSUM[31:0] register. After power up or a hardware/software reset, the CRC is computed on the default values of the registers. The result is 0x2689B124.

Figure 57 presents how LFSR works. Bits a_0, a_1,…, a_{255} represent the bits from the list of registers presented above. a_0 is the less significant bit of the first internal register to enter LFSR, a_{255} is the most significant bit of MASK0[31:0] register, the last register to enter LFSR. The equations that govern LFSR are presented below:

$b_i(0)$ =1, i=0, 1, 2,…, 31, the initial state of the bits that form the CRC. b_0 is the less significant bit, b_{31} is the most significant.

g_i, i=0, 1, 2,…, 31 are the coefficients of the generating polynomial defined by IEEE802.3 standard:

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1 \quad (34)$$

$$g_0 = g_1 = g_2 = g_4 = g_5 = g_7 = 1$$
$$g_8 = g_{10} = g_{11} = g_{12} = g_{16} = g_{22} = g_{26} = 1 \quad (35)$$

All the other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \oplus b_{31}(j-1) \quad (36)$$

$$b_0(j) = FB(j) \cdot g_0 \quad (37)$$

$$b_i(j) = FB(j) \cdot g_i \oplus b_{i-1}(j-1), i = 1,2,3,...,31 \quad (38)$$

The operations $\oplus$ and $\cdot$ represent the logic XOR and AND. The equations *(36)*, *(37)* and *(38)* have to be repeated for j=1, 2,…, 256. The value written into CHECKSUM[31:0] register contains the bits $b_i(256)$,i=0, 1,…, 31. The value of the CRC after the bits from the reserved internal register have passed through LFSR is 0x3A7ABC72. It is obtained at step j=48.

Two different approaches may be followed in using the CHECKSUM register. One is to compute the CRC based on the relations (34) - *(38)* and then compare the value against the CHECKSUM register. Another is to periodically read the CHECKSUM[31:0] register. If two consecutive readings differ, then it may be safely assumed that one of the registers has changed value and therefore, the ADE7854 has changed configuration. The recommended response is to initiate a hardware/software reset that sets the values of all registers to the default, including the reserved ones, and then reinitialize the configuration registers.

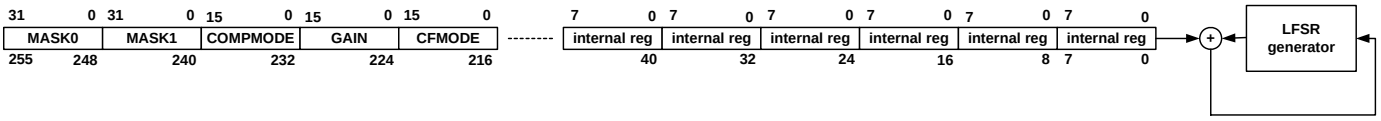

Figure 56. CHECKSUM[31:0] register calculation

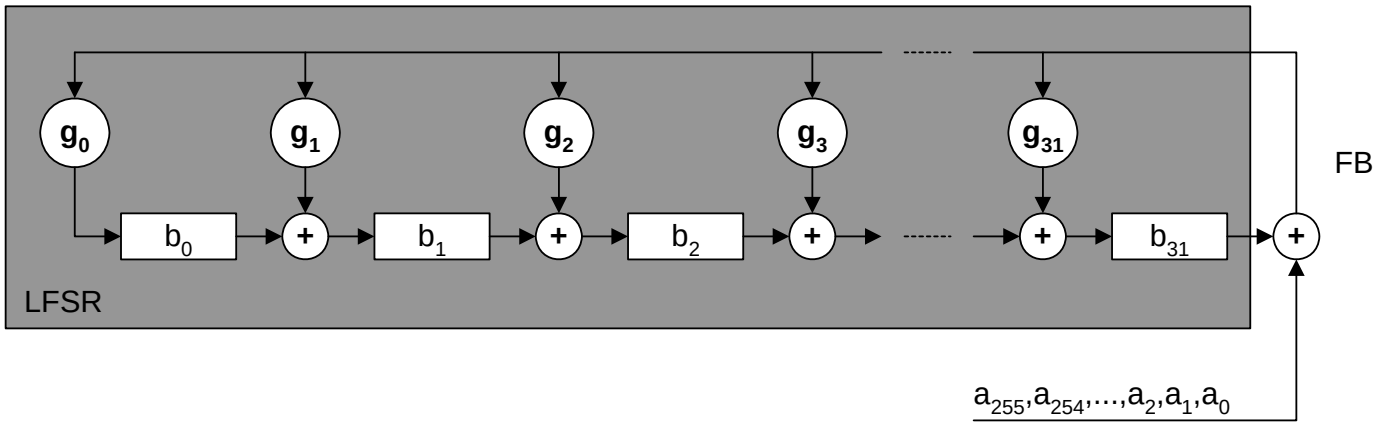

Figure 57.LFSR generator used in CHECKSUM[31:0] register calculation

INTERRUPTS

The ADE7854 has two interrupt pins, $\overline{IRQ0}$ and $\overline{IRQ1}$. Each of them is managed by a 32-bit interrupt mask register, MASK0[31:0], respective MASK1[31:0]. To enable an interrupt, a bit in MASKx[31:0] register has to be set to 1. To disable it, the bit has to be cleared to 0. Two 32-bit status registers, STATUS0[31:0] and STATUS1[31:0] are associated with the interrupts. When an interrupt event occurs in the ADE7854, the corresponding flag in the interrupt status register is set to a Logic 1 (see Table 26 and Table 27). If the mask bit for this interrupt in the interrupt mask register is Logic 1, then the $\overline{IRQx}$ logic output goes active low. The flag bits in the interrupt status register are set irrespective of the state of the mask bits. To determine the source of the interrupt, the MCU should perform a read of corresponding STATUSx register and identify which bit is 1. To erase the flag in the status register, STATUSx should be written back with the flag set to 1. Practically, after an interrupt pin goes low, the status register is read and the source of the interrupt is identified. Then, the status register is written back without any change to cancel the status flag. The $\overline{IRQx}$ pin remains low until the status flag is cancelled.

By default, all interrupts are disabled. RSTDONE interrupt is an exception. This interrupt can never be masked (disabled) and therefore bit 15 (RSTDONE) in MASK1[31:0] register does not have any functionality. $\overline{IRQ1}$ pin always goes low and bit 15 (RSTDONE) in STATUS1[31:0] is set to 1 whenever a power up or a hardware/software reset process ends. To cancel the status flag, STATUS1[31:0] register has to be written with bit 15(RSTDONE) set to 1.

Certain interrupts are used in conjunction with other status registers: bits 0 (NLOAD) and 2 (VANLOAD) in MASK1[31:0] work in conjunction with status bits in PHNOLAD[15:0]. Bits 16, (SAG), 17 (OI) and 18 (OV) in MASK1[31:0] work with status bits in PHSTATUS[15:0]. Bits 23 (PKI) and 24 (PKV) in MASK1[31:0] work with status bits in IPEAK[31:0] and respectively, VPEAK[31:0]. Bits 6, 7, 8 (REVAPx, x=A, B, C) and 9, 13, 18 (REVPSUMx) in MASK0[31:0] work with status bits in PHSIGN[15:0]. When STATUSx[31:0] register is read and one of these bits is set to 1, the status register associated with the bit is immediately read to identify the phase that triggered the interrupt and only then STATUSx[31:0] is written back with the bit set to 1 to cancel the status flag.

Using the Interrupts with an MCU

Figure 58 shows a timing diagram that illustrates a suggested implementation of the ADE7854 interrupt management using an MCU. At time t_1, $\overline{IRQx}$ pin goes active low indicating that one or more interrupt events have occurred in the ADE7854. The $\overline{IRQx}$ pin should be tied to a negative-edge-triggered external interrupt on the MCU. On detection of the negative edge, the MCU should be configured to start executing its interrupt service routine (ISR). On entering the ISR, all interrupts should be disabled using the global interrupt mask bit. At this point, the MCU external interrupt flag can be cleared to capture interrupt events that occur during the current ISR. When the MCU interrupt flag is cleared, a read from STATUSx, the interrupt status register is carried out. The interrupt status register content is used to determine the source of the interrupt(s) and hence the appropriate action to be taken. Then, the same STATUSx content is written back into the ADE7854 to clear the status flag(s) and reset $\overline{IRQx}$ line to logic high (t_2). If a subsequent interrupt event occurs during the ISR (t_3) that event is recorded by the MCU external interrupt flag being set again.

On returning from the ISR, the global interrupt mask bit is cleared (same instruction cycle) and the external interrupt flag uses the MCU to jump to its ISR once again. This ensures that the MCU does not miss any external interrupts.

Figure 59 shows a recommended timing diagram when status bits in STATUSx registers work in conjunction with bits in other registers. Same as above, when $\overline{IRQx}$ pin goes active low, STATUSx register is read and if one of these bits is 1, then a second status register is read immediately to identify the phase that triggered the interrupt. The name PHx in the figure denotes one of PHSTATUS, IPEAK, VPEAK or PHSIGN registers. Then STATUSx register is afterwards written back to clear the status flag(s).

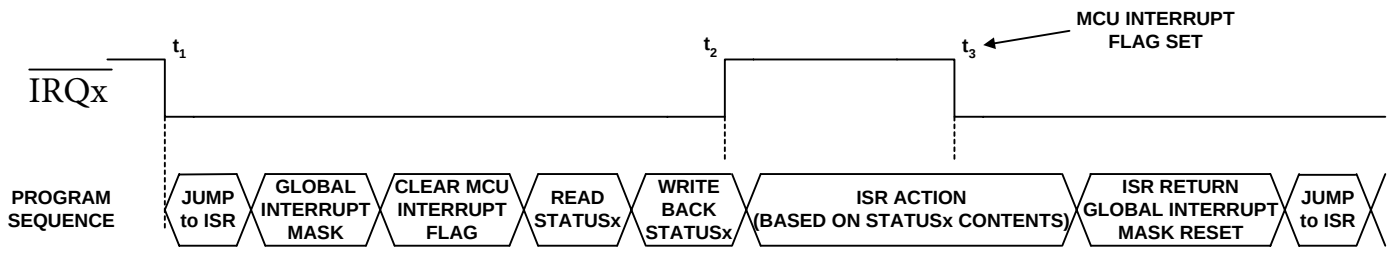

Figure 58. ADE7854 interrupt management

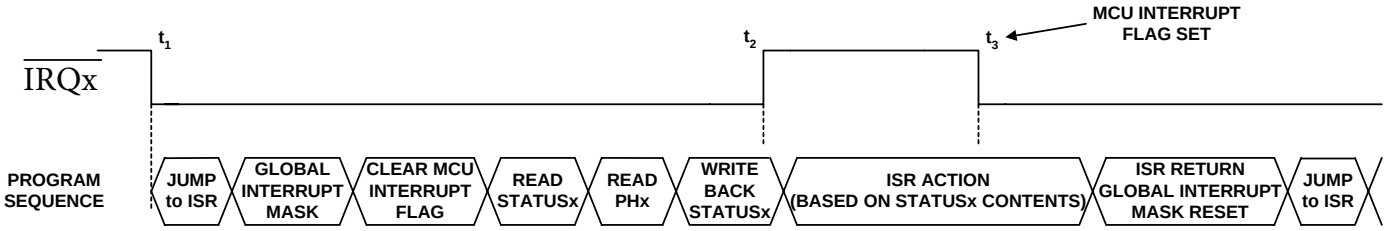

Figure 59. ADE7854 interrupt management when PHSTATUS, IPEAK, VPEAK or PHSIGN registers are involved

SERIAL INTERFACES

The ADE7854 has three serial port interfaces: one fully licensed I²C interface, one Serial Peripheral Interface (SPI) and one High Speed Data Capture Port (HSDC). As the SPI pins are multiplexed with some of the pins of I²C and HSDC ports, the ADE7854 accepts two configurations: one using SPI port only and one using I²C port in conjunction with HSDC port.

Serial interface choice

After reset, the HSDC port is always disabled. The choice between I²C and SPI port is done by manipulating the $\overline{SS}$ pin after power up or after a hardware reset. If $\overline{SS}$ pin is kept high, then ADE7854 will use the I²C port until a new hardware reset is executed. If $\overline{SS}$ pin is toggled high low 3 times after power up or after a hardware reset, then the ADE7854 will use the SPI port until a new hardware reset is executed. This manipulation of the $\overline{SS}$ pin can be accomplished in two ways: one way is to use the $\overline{SS}$ pin of the master device (i.e. the microcontroller) as a regular I/O pin and toggle it 3 times. Another way is to execute 3 SPI write operations to a location in the address space that is not allocated to a specific ADE7854 register (for example 0xEBFF). These writes allow the $\overline{SS}$ pin to toggle 3 times. See SPI Write Operation section for details on the write protocol involved.

After the serial port choice is done, it needs to be locked, so the active port remains in use until a hardware reset is executed in PSM0 normal mode or until a power down. If I²C is the active serial port, bit 1 (I2C_LOCK) of CONFIG2[7:0] must be set to 1 to lock it in. From this moment on, the ADE7854 ignores spurious togglings of the $\overline{SS}$ pin and an eventual switch into using SPI port is no longer possible. If SPI is the active serial port, any write to CONFIG2[7:0] register locks the port. From this moment on, a switch into using I²C port is no longer possible.

Once locked, the serial port choice is maintained when the ADE7854 changes between PSM0 and PSM3 power modes.

The functionality of the ADE7854 is accessible via several on-chip registers. The contents of these registers can be updated or read using the I²C or SPI interfaces. HSDC port provides the state of up to 13 registers representing instantaneous values of phase voltages and currents, neutral current, active and apparent powers.

I²C Compatible Interface

The ADE7854 supports a fully licensed I²C interface. The I²C interface is implemented as a full hardware slave. SDA is the data I/O pin, and SCL is the serial clock. These two pins are shared with the MOSI and SCLK pins of the on-chip SPI interface. The maximum serial clock frequency supported by this interface is 400KHz.

The two pins used for data transfer, SDA and SCL are configured in a Wired-AND format that allows arbitration in a multi-master system.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a START condition while the bus is idle. The master transmits the address of the slave device and the direction of the data transfer in the initial address transfer. If the slave acknowledges, then the data transfer is initiated. This continues until the master issues a STOP condition and the bus becomes idle.

I²C Write Operation

The write operation using I²C interface of the ADE7854 initiates when the master generates a START condition and consists in one byte representing the address of the ADE7854 followed by the 16-bit address of the target register and by the value of the register.

The most significant 7 bits of the address byte constitute the address of the ADE7854 and they are equal to b#0111000. Bit 0 of the address byte is READ/ $\overline{WRITE}$ bit. Because this is a write operation, it has to cleared to 0, so the first byte of the write operation is 0x70. After every byte is received, the ADE7854 generates an acknowledge. As registers may have 8, 16 or 32 bits, after the last bit of the register is transmitted and the ADE7854 acknowledges the transfer, the master generates a STOP condition. The addresses and the register content are sent with the most significant bit first. See Figure 60 for details of the I²C write operation.

I²C Read Operation

The read operation using the I²C interface of the ADE7854 is done in two stages. The first stage sets the pointer to the address of the register. The second stage reads the content of the register.

As seen in Figure 61, the first stage initiates when the master generates a START condition and consists in one byte representing the address of the ADE7854 followed by the 16-bit address of the target register. The ADE7854 acknowledges every

byte received. The address byte is similar to the address byte of a write operation and is equal to 0x70 (See I2C Write Operation section for details). After the last byte of the register address has been sent and it has been acknowledged by the ADE7854, the second stage begins with the master generating a new START condition followed by an address byte. The most significant 7 bits of this address byte constitute the address of the ADE7854 and they are equal to b#0111000. Bit 0 of the address byte is READ/ $\overline{\text{WRITE}}$ bit. Because this is a read operation, it has to be set to 1, so the first byte of the read operation is 0x71. After this byte is received, the ADE7854 generates an acknowledge. Then the ADE7854 sends the value of the register and after every 8 bits are received, the master generates an acknowledge. All the bytes are sent with the most significant bit first. As registers may have 8, 16 or 32 bits, after the last bit of the register is received , the master does not acknowledge the transfer, but does generate a STOP condition.

SPI Compatible Interface

The Serial Peripheral Interface (SPI) of the ADE7854 is always a slave of the communication and consists in four pins: SCLK, MOSI, MISO and $\overline{\text{SS}}$. The serial clock for a data transfer is applied at the SCLK logic input. This logic input has a Schmitt trigger input structure that allows slow rising (and falling) clock edges to be used. All data transfer operations are synchronized to the serial clock. Data is shifted into the ADE7854 at the MOSI logic input on the falling edge of SCLK. Data is shifted out of the ADE7854 at the MISO logic output on a rising edge of SCLK. The most significant bit of the word is shifted in and out first. The maximum serial clock frequency supported by this interface is 2.5MHz. MISO stays in high impedance when no data is transmitted from the ADE7854. Figure 62 presents details of the connection between ADE7854 SPI and a master device containing an SPI interface.

The $\overline{SS}$ logic input is the chip select input. This input is used when multiple devices share the serial bus. The $\overline{SS}$ input should be driven low for the entire data transfer operation. Bringing $\overline{SS}$ high during a data transfer operation aborts the transfer and places the serial bus in a high impedance state. A new transfer can then be initiated by bringing the $\overline{SS}$ logic input back low. However, because aborting a data transfer before completion leaves the accessed register in a state that cannot be guaranteed, every time a register is written, its value should be verified by reading it back.

The protocol is similar to the protocol used in I²C interface.

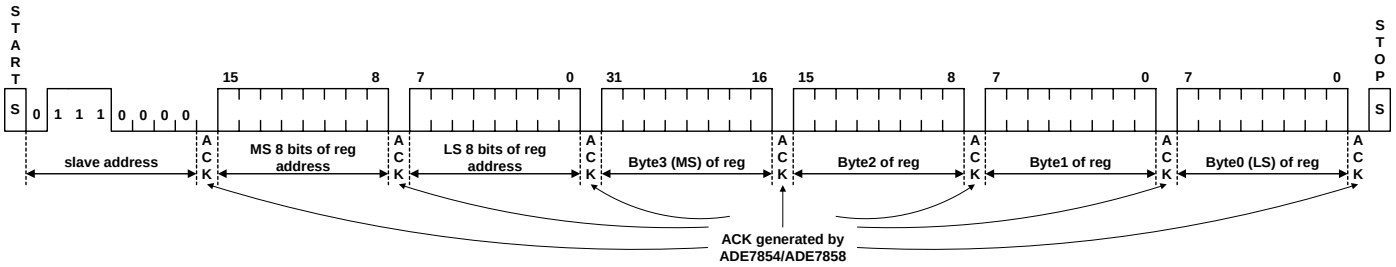

Figure 60. I²C Write Operation of a 32 bit register

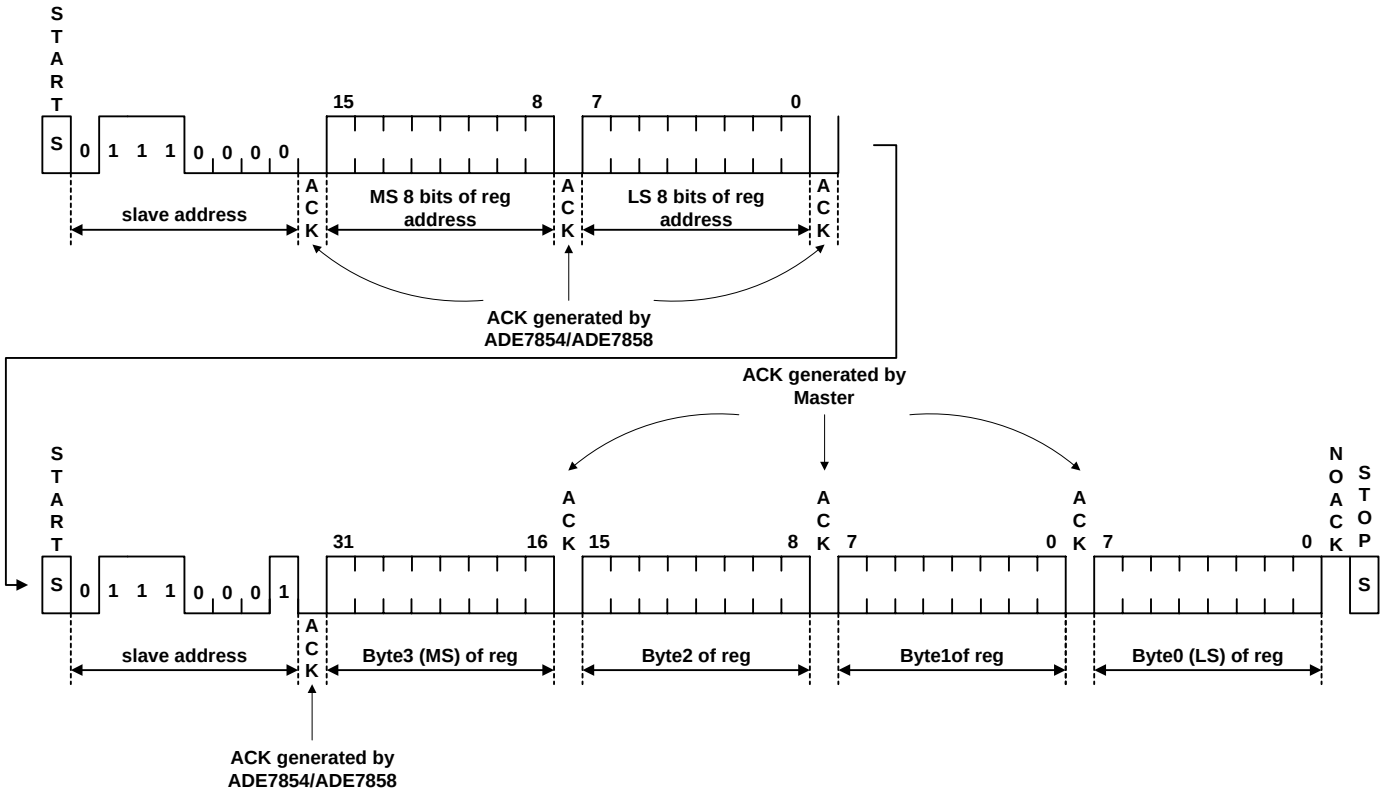

Figure 61. I²C Read Operation of a 32-bit register

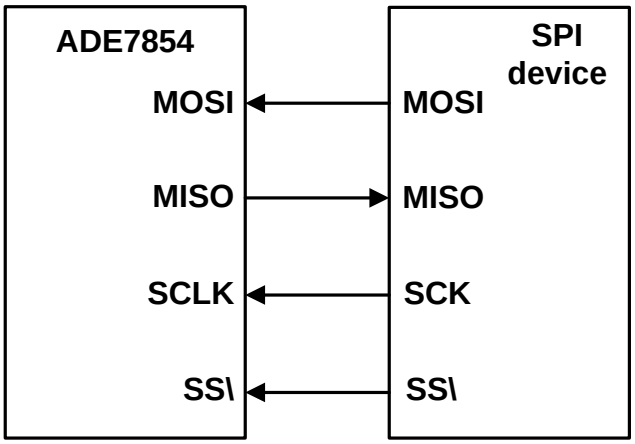

Figure 62. Connecting ADE7854 SPI with an SPI device

SPI Read Operation

The read operation using the SPI interface of the ADE7854 initiates when the master sets $\overline{SS}$ pin low and begins sending one byte representing the address of the ADE7854 on the MOSI line. The master sets data on the MOSI line starting with the first high to low transition of SCLK. The SPI of the ADE7854 samples data on the low to high transitions of SCLK. The most significant 7 bits of the address byte can have any value, but as a good programming practice, they should be different from b#0111000, the 7 bits used in the I²C protocol. Bit 0 (READ/ $\overline{WRITE}$) of the address byte must be 1 for a read operation. Next, the master sends the 16-bit address of the register that is read. After the ADE7854 receives the last bit of address of the register on a low to high transition of SCLK, it begins to transmit its content on the MISO line before the next SCLK high to low transition occurs, so the master can sample the data on this SCLK transition. After the master receives the last bit, it sets $\overline{SS}$ and SCLK lines high and the communication ends. The data lines MOSI and MISO go in high impedance state.

See Figure 63 for details of the SPI read operation.

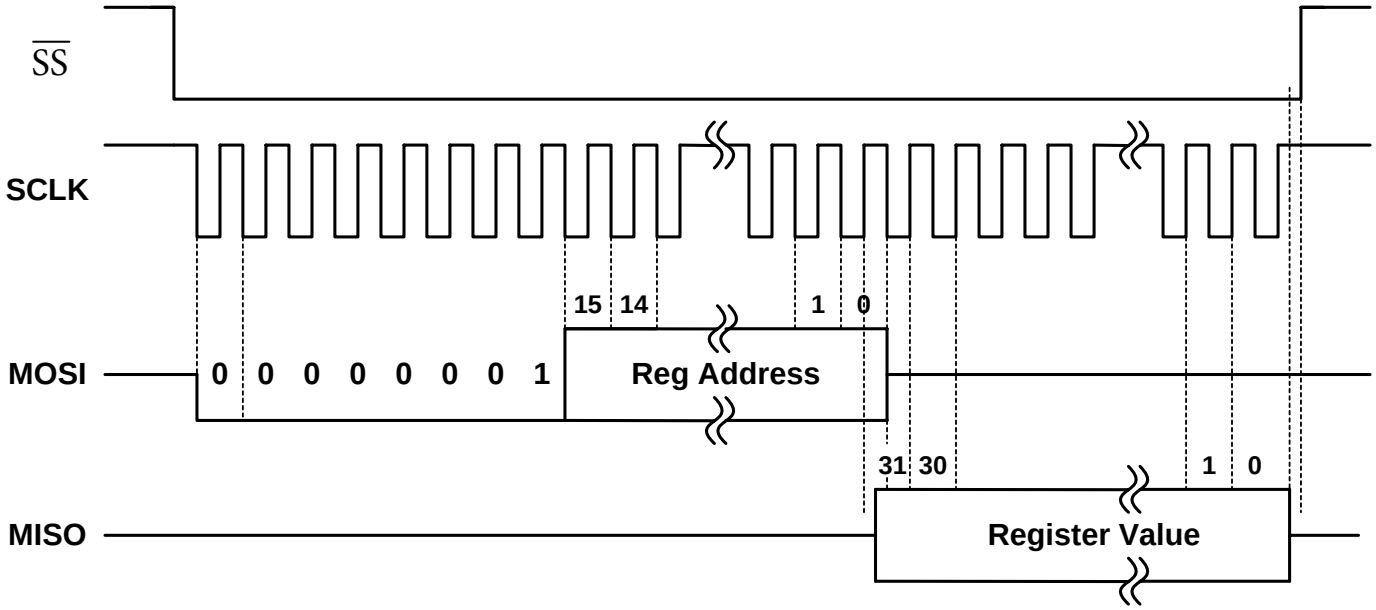

Figure 63. SPI read operation of a 32-bit register

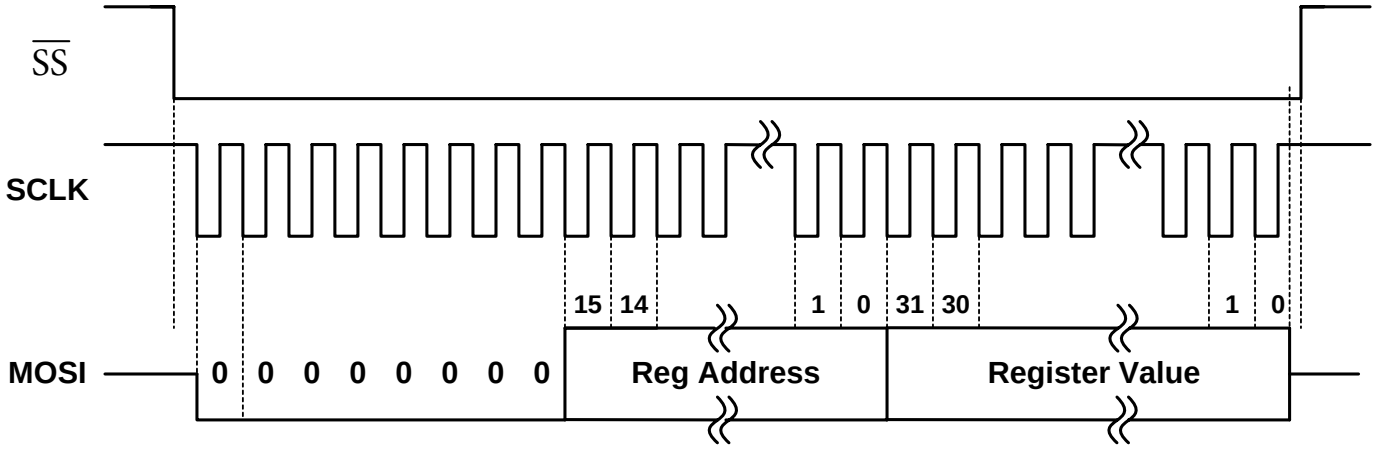

Figure 64. SPI Write operation of a 32-bit register

SPI Write Operation

The write operation using the SPI interface of the ADE7854 initiates when the master sets $\overline{SS}$ pin low and begins sending one byte representing the address of the ADE7854 on the MOSI line. The master sets data on the MOSI line starting with the first high to low transition of SCLK. The SPI of the ADE7854 samples data on the low to high transitions of SCLK. The most significant 7 bits of the address byte can have any value, but as a good programming practice, they should be different from b#0111000, the 7 bits used in the I²C protocol. Bit 0 (READ/ $\overline{WRITE}$) of the address byte must be 0 for a write operation. Next, the master sends the 16-bit address of the register that is written and the 32, 16 or 8-bit value of that register without losing any SCLK cycle. After the last bit is transmitted, the master sets $\overline{SS}$ and SCLK lines high at the end of SCLK cycle and the communication ends. The data lines MOSI and MISO go in high impedance state.

See Figure 64 for details of the SPI write operation.

HSDC Interface

The High Speed Data Capture (HSDC) interface is disabled after default. It can be used only if the ADE7854 are configured with I²C interface. The SPI interface cannot be used in conjunction with HSDC. Bit 6 (HSDCEN) in CONFIG[15:0] register activates HSDC when set to 1. If bit HSDCEN is cleared to 0, the default value, the HSDC interface is disabled. Setting bit HSDCEN to 1 when SPI is in usage does not have any effect.

HSDC is an interface that is used to send to an external device, usually a microprocessor or a DSP, up to thirteen 32-bit words. The words represent the instantaneous values of the phase currents and voltages, active and apparent powers. The registers being transmitted are: IAWV[23:0], IBWV[23:0], ICWV[23:0], VAWV[23:0], VBWV[23:0], VCWV[23:0], AWATT[23:0], BWATT[23:0], CWATT[23:0], AVA[23:0], BVA[23:0] and CVA[23:0]. All are 24-bit registers that are sign extended to 32-

bits (see Figure 18 for details). HSDC can be interfaced with SPI, SPORT (Serial Peripheral Port) or similar interfaces.

HSDC is always a master of the communication and consists in 3 pins: HSA, HSD and HSCLK. HSA represents the select signal. It stays active low when a word is transmitted and is usually connected to the select pin of the slave. HSD is used to send data to the slave and is usually connected to the data input pin of the slave. HSCLK is the serial clock line. It is generated by the ADE7854 and is usually connected to the serial clock input of the slave. Figure 65 and Figure 66 present details of connections between ADE7854 HSDC and slave devices containing SPI and SPORT interfaces.

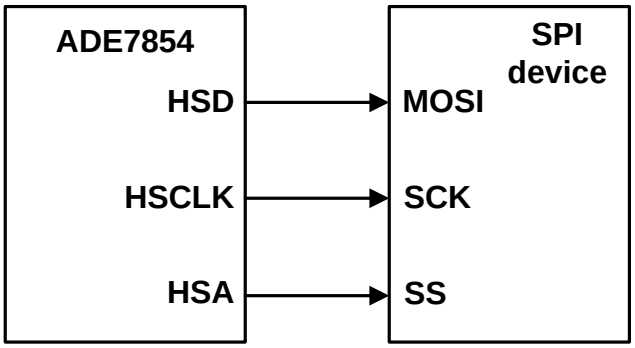

Figure 65. Connecting ADE7854 HSDC with an SPI

The HSDC communication is managed by the HSDC_CFG[7:0] register (see Table 17). It is recommended to set HSDC_CFG register to the desired value before enabling the port using bit 6 (HSDCEN) in CONFIG[15:0] register. In this way, the state of various pins belonging to HSDC port do not take levels inconsistent with the desired HSDC behaviour. After a hardware reset or after power up, the pins MISO/HSD and $\overline{SS}$ /HSA are set high.

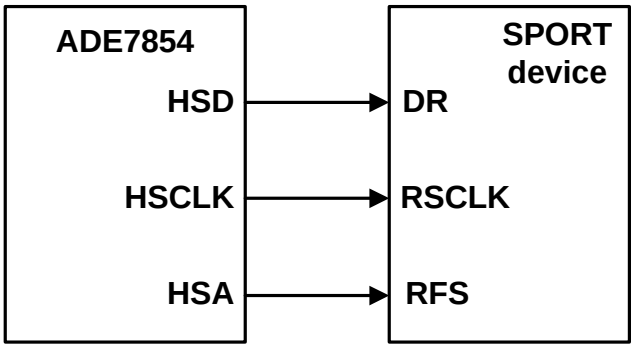

Figure 66. Connecting ADE7854 with a SPORT

Bit 0 (HCLK) in HSDC_CFG[7:0] register determines the serial clock frequency of the HSDC communication. When HCLK is 0, the default value, then the clock frequency is 8MHz. When HCLK is 1, the clock frequency is 4MHz. A bit of data is transmitted for every HSCLK high to low transition. The slave device that receives data from HSDC samples HSD line on the low to high transition of HSCLK.

The words may be transmitted as 32-bit packages or as 8-bit packages. When bit 1 (HSIZE) in HSDC_CFG[7:0] register is 0, the default value, the words are transmitted as 32-bit packages. When bit HSIZE is 1, the registers are transmitted as 8-bit packages. HSDC interface transmits the words with MSB first.

Table 17. HSDC_CFG register

Bit Location	Bit Mnemonic	Default Value	Description
0	HCLK	0	-0: HSCLK is 8MHz -1: HSCLK is 4MHz
1	HSIZE	0	-0: HSDC transmits the 32bit registers in 32bit packages, most significant bit first. -1: HSDC transmits the 32bit registers in 8bit packages, most significant bit first.
2	HGAP	0	-0: no gap is introduced between packages. -1: a gap of 7 HCLK cycles is introduced between packages.
4,3	HXFER[1:0]	00	-00=HSDC transmits 16 registers shown in Table 21. ADE7854 billable registers -01= HSDC transmits 6 instantaneous values of currents and voltages plus one 32-bit word always equal to 0 -10= HSDC transmits 6 instantaneous values of phase powers plus three 32-bit words always equal to 0 -11=reserved. If set, the ADE7854 behaves as if HXFER[1:0]=00.
5	HSAPOL	0	-0: HSACTIVE output pin is active LOW. -1: HSACTIVE output pin is active HIGH
7,6		00	Reserved. These bits do not manage any functionality.

Bit 2 (HGAP) introduces a gap of 7 HSCLK cycles between packages when is set to 1. When bit HGAP is cleared to 0, the default value, no gap is introduced between packages and the communication time is shortest. In this case, HSIZE does not have any influence on the communication and a bit is put on HSD line every HSCLK high to low transition.

Bits 4,3 (HXFER[1:0]) decide how many words are transmitted. When HXFER[1:0] is 00, the default value, then all sixteen words are transmitted. When HXFER[1:0] is 01, then only the words representing the instantaneous values of phase currents and phase voltages are transmitted in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV and one 32-bit word always equal to 0. When HXFER[1:0] is 01, then only the instantaneous values of phase powers are transmitted in the following order: AVA, BVA, CVA, AWATT, BWATT, CWATT, followed by three 32-bit words always equal to 0. The value 11

for HXFER[1:0] is reserved and writing it is equivalent to writing 00, the default value.

Bit 5 (HSAPOL) determines the polarity of HSA pin during the communication. When HSAPOL is 0, the default value, the HSA pin is active low during the communication. This means that HSA stays high when no communication is in progress. When the communication starts, HSA goes low and stays low until the communication ends. Then it goes back high. When HSAPOL is 1, the HSA pin is active high during the communication. This means that HSA stays low when no communication is in progress. When the communication starts, HSA goes high and stays high until the communication ends. Then it goes back low.

Bits 7, 6 of HSDC_CFG are reserved. Any value written into these bits does not have any consequence on HSDC behavior.

Figure 67 shows the HSDC transfer protocol for HGAP=0, HXFER[1:0]=00 and HSAPOL=0. Note that the HSDC interface sets a bit on HSD line every HSCLK high to low transition and the value of bit HSIZE is irrelevant.

Figure 68 shows the HSDC transfer protocol for HSIZE=0, HGAP=1, HXFER[1:0]=00 and HSAPOL=0. Note that HSDC interface introduces a 7 HSCLK cycles gap between every 32-bit word.

Figure 69 shows the HSDC transfer protocol for HSIZE=1, HGAP=1, HXFER[1:0]=00 and HSAPOL=0. Note that HSDC interface introduces a 7 HSCLK cycles gap between every 8-bit word.

Table 18 presents the time it takes to execute an HSDC data transfer for all HSDC_CFG[7:0] settings. For some settings, the transfer time is less than 125usec (8KHz), the waveform sample registers update rate. This means the HSDC port transmits data every sampling cycle. For settings in which the transfer time is greater than 125usec, the HSDC port transmits data only in the first of two consecutive 8KHz sampling cycles. This means it transmits registers at an effective rate of 4KHz.

Table 18. Communication times for various HSDC settings

HXFER[1:0]	HGAP	HSIZE	HCLK	Comm Time [µsec]
00	0	*	0	64
00	0	*	1	128
00	1	0	0	77.125
00	1	0	1	154.25
00	1	1	0	119.25
00	1	1	1	238.25
01	0	*	0	28
01	0	*	1	56
01	1	0	0	33.25
01	1	0	1	66.5
01	1	1	0	51.625
01	1	1	1	103.25
10	0	*	0	36
10	0	*	1	72
10	1	0	0	43
10	1	0	1	86
10	1	1	0	66.625
10	1	1	1	133.25

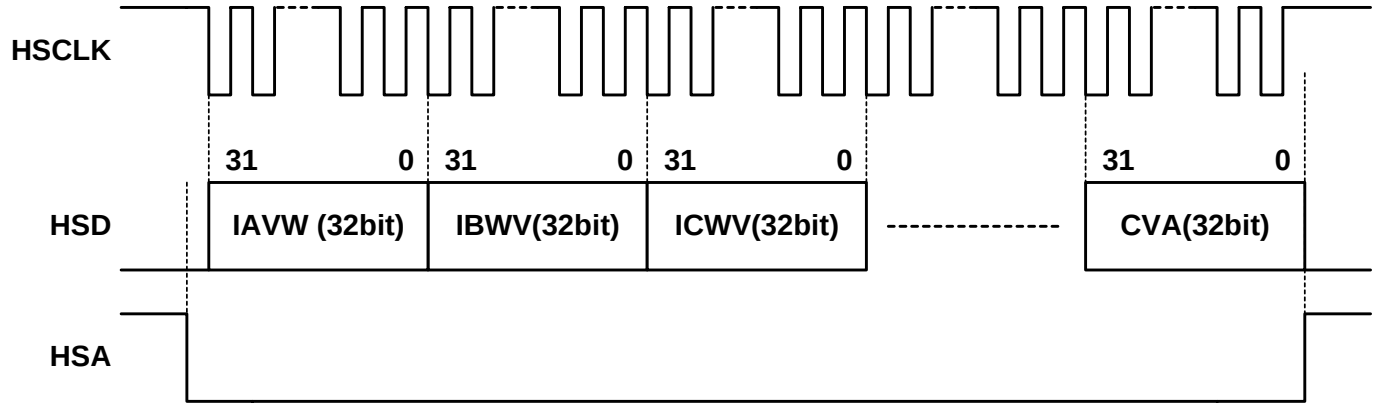

Figure 67. HSDC communication for HGAP=0, HXFER[1:0]=00 and HSAPOL=0. HSIZE is irrelevant

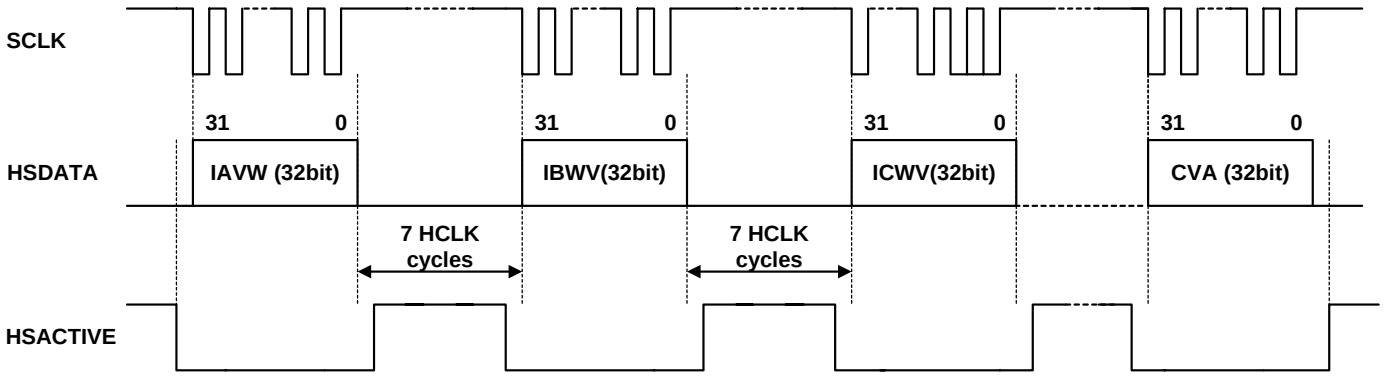

Figure 68. HSDC communication for HSIZE=0, HGAP=1, HXFER[1:0]=00 and HSAPOL=0

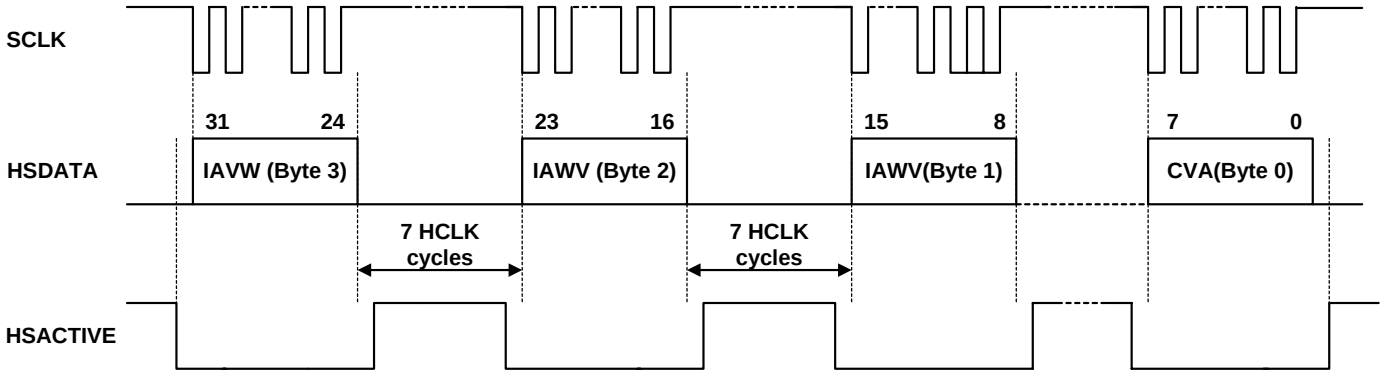

Figure 69. HSDC communication for HSIZE=1, HGAP=1, HXFER[1:0]=00 and HSAPOL=0

REGISTERS LIST

Table 19. ADE7854 Registers List located in DSP data memory RAM

Address	Name	R/W[1]	Bit Length	Bit Length during Comm[2]	Type[3]	Default Value	Description
0x4380	AIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A current gain adjust
0x4381	AVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A voltage gain adjust
0x4382	BIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B current gain adjust
0x4383	BVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B voltage gain adjust
0x4384	CIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C current gain adjust
0x4385	CVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C voltage gain adjust
0x4386	Reserved						This memory location should be kept at 0x000000 for proper operation
0x4387	AIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A current rms offset
0x4388	AVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A voltage rms offset
0x4389	BIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B current rms offset
0x438A	BVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B voltage rms offset
0x438B	CIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C current rms offset
0x438C	CVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C voltage rms offset
0x438D	reserved					0x000000	This memory location should be kept at 0x000000 for proper operation
0x438E	AVAGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A apparent power gain adjust
0x438F	BVAGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B apparent power gain adjust
0x4390	CVAGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C apparent power gain adjust
0x4391	AWGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A total active power gain adjust
0x4392	AWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase A total active power offset adjust
0x4393	BWGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B total active power gain adjust
0x4394	BWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase B total active power offset adjust
0x4395	CWGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C total active power gain adjust
0x4396	CWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase C total active power offset adjust
0x4397-0x43A8	reserved					0x000000	These memory locations should be kept at 0x000000 for proper operation
0x43A9	VATHR1	R/W	24	32 ZP	U	0x000000	Most significant 24 bits of VATHR[47:0] threshold used in phase apparent power data path.
0x43AA	VATHR0	R/W	24	32 ZP	U	0x000000	Less significant 24 bits of VATHR[47:0] threshold used in phase apparent power data path.
0x43AB	WTHR1	R/W	24	32 ZP	U	0x000000	Most significant 24 bits of WTHR[47:0] threshold used in phase total active power data path.
0x43AC	WTHR0	R/W	24	32 ZP	U	0x000000	Less significant 24 bits of WTHR[47:0] threshold used in phase total active power data path.
0x43AD-0x43AF	reserved					0x000000	This memory location should be kept at 0x000000 for proper operation
0x43B0	VANOLOAD	R/W	24	32 ZPSE	S	0x000000	No-load threshold in the apparent power data path
0x43B1	APNOLOAD	R/W	24	32 ZPSE	S	0x000000	No-load threshold in the total active power data path
0x43B2	VARNOLOAD	R/W	24	32 ZPSE	S	0x000000	This register must be set at 0x800000 to ensure the correct functionality of no-load detection circuit based on total active power (See No-load detection based on total active power section for details).
0x43B3-0x43B4	reserved					0x000000	This memory location should not be written for proper operation
0x43B5	DICOEFF	R/W	24	32ZPSE	S	0x0000000	Register used in the digital integrator algorithm. If the integrator is turned on, it must be set at 0xFF8000
0x43B6	HPFDIS	R/W	24	32 ZP	U	0x000000	Disables/enables the HPF in the current data path. (Table 23)

Address	Name	R/W[1]	Bit Length	Bit Length during Comm[2]	Type[3]	Default Value	Description
0x43B7-0x43BF	reserved					0x000000	These memory locations should be kept at 0x000000 for proper operation
0x43C0	AIRMS	R	24	32 ZP	S	NA	Phase A current rms value
0x43C1	AVRMS	R	24	32 ZP	S	NA	Phase A voltage rms value
0x43C2	BIRMS	R	24	32 ZP	S	NA	Phase B current rms value
0x43C3	BVRMS	R	24	32 ZP	S	NA	Phase B voltage rms value
0x43C4	CIRMS	R	24	32 ZP	S	NA	Phase C current rms value
0x43C5	CVRMS	R	24	32 ZP	S	NA	Phase C voltage rms value
0x43C6-0x43FF	reserved					0x000000	These memory locations should not be written for proper operation

[1] R=read
W=write
[2] 32 ZPSE=24-bit signed register that is transmitted as a 32-bit word with 4 most significant bits padded with 0s and sign extended to 28bits
32 ZP=28 or 24-bit signed or unsigned register that is transmitted as a 32-bit word with 4 or respectively 8 most significant bits padded with 0s
[3] U=unsigned register
S=signed register in two's complement format

Table 20. Internal DSP memory RAM registers

Address	Name	R/W[1]	Bit Length	Bit Length during Comm	Type[2]	Default Value	Description
0xE203	reserved	R/W	16	16	U	0x0000	This memory location should not be written for proper operation DSP stops execution.
0xE228	RUN	R/W	16	16	U	0x0000	RUN register starts and stops the DSP. See Digital Signal Processor chapter for more details.

[1] R=read
W=write
[2] U=unsigned register
S=signed register in two's complement format

Table 21. ADE7854 billable registers

Address	Name	R/W[1]	Bit Length	Bit Length during Comm	Type[2]	Default Value	Description
0xE400	AWATTHR	R	32	32	S	0x00000000	Phase A total active energy accumulation
0xE401	BWATTHR	R	32	32	S	0x00000000	Phase B total active energy accumulation
0xE402	CWATTHR	R	32	32	S	0x00000000	Phase C total active energy accumulation
0xE403-0xE40B	Reserved	R					
0xE40C	AVAHR	R	32	32	S	0x00000000	Phase A apparent energy accumulation
0xE40D	BVAHR	R	32	32	S	0x00000000	Phase B apparent energy accumulation
0xE40E	CVAHR	R	32	32	S	0x00000000	Phase C apparent energy accumulation

[1] R=read
W=write
[2] U=unsigned register
S=signed register in two's complement format

Table 22. Configuration and power quality registers

Address	Name	R/W[1]	Bit Length	Bit Length during comm[2]	Type[3]	Default Value	Description
0xE500	IPEAK	R	32	32	U	NA	Current peak register. (Figure 34 and Table 24)
0xE501	VPEAK	R	32	32	U	NA	Voltage peak register. (Figure 34 and Table 25)
0xE502	STATUS0	R	32	32	U	NA	Interrupt status register 0. (Table 26).
0xE503	STATUS1	R	32	32	U	NA	Interrupt status register 1. (Table 27).
0xE504-0xE506	Reserved	R					
0xE507	OILVL	R/W	24	32 ZP	U	0xFFFFFF	Overcurrent threshold
0xE508	OVLVL	R/W	24	32 ZP	U	0xFFFFFF	Overvoltage threshold
0xE509	SAGLVL	R/W	24	32 ZP	U	0x000000	Voltage sag level threshold
0xE50A	MASK0	R/W	32	32	U	0x00000000	Interrupt enable register 0. (Table 28).
0xE50B	MASK1	R/W	32	32	U	0x00000000	Interrupt enable register 1. (Table 29)
0xE50C	IAWV	R	24	32 SE	S	NA	Instantaneous value of phase A current
0xE50D	IBWV	R	24	32 SE	S	NA	Instantaneous value of phase B current
0xE50E	ICWV	R	24	32 SE	S	NA	Instantaneous value of phase C current
0xE50F	Reserved	R					
0xE510	VAWV	R	24	32 SE	S	NA	Instantaneous value of phase A voltage
0xE511	VBWV	R	24	32 SE	S	NA	Instantaneous value of phase B voltage
0xE512	VCWV	R	24	32 SE	S	NA	Instantaneous value of phase C voltage
0xE513	AWATT	R	24	32 SE	S	NA	Instantaneous value of phase A total active power
0xE514	BWATT	R	24	32 SE	S	NA	Instantaneous value of phase B total active power
0xE515	CWATT	R	24	32 SE	S	NA	Instantaneous value of phase B total active power
0xE516-0xE518	Reserved	R					
0xE519	AVA	R	24	32 SE	S	NA	Instantaneous value of phase A apparent power
0xE51A	BVA	R	24	32 SE	S	NA	Instantaneous value of phase Bapparent power
0xE51B	CVA	R	24	32 SE	S	NA	Instantaneous value of phase B apparent power
0xE51C-0xE51E	Reserved	R					
0xE51F	CHECKSUM	R	32	32	U	0x2689B124	Checksum verification. See Checksum Register section for details
0xE520	VNOM	R/W	24	32 ZP	S	0x000000	Nominal phase voltage rms used in the alternative computation of the apparent power
0xE521-0xE52E	reserved						These addresses should not be written for proper operation
0xE600	PHSTATUS	R	16	16	U	NA	Phase peak register. See Table 30 for details.
0xE601	ANGLE0	R	16	16	U	NA	Time delay 0. See Time Interval Between Phases section for details
0xE602	ANGLE1	R	16	16	U	NA	Time delay 1. See Time Interval Between Phases section for details
0xE603	ANGLE2	R	16	16	U	NA	Time delay 2. See Time Interval Between Phases section for details
0xE604-0xE606	reserved						These addresses should not be written for proper operation
0xE607	PERIOD	R	16	16	U	NA	Network line period
0xE608	PHNOLOAD	R	16	16	U	NA	Phase no-load register. (Table 31)
0xE609-0xE60B	reserved						These addresses should not be written for proper operation
0xE60C	LINECYC	R/W	16	16	U	0xFFFF	Line cycle accumulation mode count
0xE60D	ZXTOUT	R/W	16	16	U	0xFFFF	Zero crossing timeout count
0xE60E	COMPMODE	R/W	16	16	U	0x01FF	Computation mode register. (Table 32)
0xE60F	GAIN	R/W	16	16	U	0x0000	PGA gains at ADC inputs. (Table 33)
0xE610	CFMODE	R/W	16	16	U	0x0E88	CFx, x=1,2,3 configuration register. (Table 34)

Address	Name	R/W[1]	Bit Length	Bit Length during comm[2]	Type[3]	Default Value	Description
0xE611	CF1DEN	R/W	16	16	U	0x0000	CF1 denominator
0xE612	CF2DEN	R/W	16	16	U	0x0000	CF2 denominator
0xE613	CF3DEN	R/W	16	16	U	0x0000	CF3 denominator
0xE614	APHCAL	R/W	10	16 ZP	U	0x0000	Phase calibration of phase A. (Table 35).
0xE615	BPHCAL	R/W	10	16 ZP	U	0x0000	Phase calibration of phase B. (Table 35)
0xE616	CPHCAL	R/W	10	16 ZP	U	0x0000	Phase calibration of phase C. (Table 35)
0xE617	PHSIGN	R	16	16	U	NA	Power sign register. (Table 36)
0xE618	CONFIG	R/W	16	16	U	0x0000	ADE7854 configuration register. (Table 37)
0xE700	MMODE	R/W	8	8	U	0x16	Measurement mode register. (Table 38)
0xE701	ACCMODE	R/W	8	8	U	0x00	Accumulation mode register. (Table 39)
0xE702	LCYCMODE	R/W	8	8	U	0x78	Line accumulation mode behavior. (Table 40).
0xE703	PEAKCYC	R/W	8	8	U	0x00	Peak detection half line cycles
0xE704	SAGCYC	R/W	8	8	U	0x00	Sag detection half line cycles
0xE705	CFCYC	R/W	8	8	U	0x01	Number of CF pulses between two consecutive energy latches. See Synchronizing energy registers with CFx outputs section
0xE706	HSDC_CFG	R/W	8	8	U	0x00	HSDC configuration register.(Table 41)
0xEBFF	reserved						This address may be used in manipulating the $\overline{SS}$ pin when SPI is chosen as the active port. (See Serial Interfaces chapter for details)
0xEC00	Reserved						This address should not be written for proper operation
0xEC01	CONFIG2	R/W	8	8	U	0x00	Second configuration register. (Table 42)

[1] R=read
W=write
[2] 32 ZP=24 or 20-bit signed or unsigned register that is transmitted as a 32-bit word with 8 or respectively 12 most significant bits padded with 0s
32 SE=24-bit signed register that is transmitted as a 32-bit word sign extended to 32 bits
16 ZP=10-bit unsigned register that is transmitted as a 16-bit word with 6 most significant bits padded with 0s
[3] U=unsigned, S=signed

Table 23. HPFDIS register (address 0x43B6)

Bit Location	Bit Mnemonic	Default value	Description
23:0		00000000	When HPFDIS=0x00000000, then all high pass filters in voltage and current channels are enabled. When the register is set to any non zero value, all high pass filters are disabled.

Table 24. IPEAK register (address 0xE500)

Bit Location	Bit Mnemonic	Default value	Description
23-0	IPEAKVAL[23:0]	0	These bits contain the peak value determined in the current channel.
24	IPPHASE[0]	0	When this bit is set to 1, phase A current generated IPEAKVAL[23:0] value.
25	IPPHASE[1]	0	When this bit is set to 1, phase B current generated IPEAKVAL[23:0] value.
26	IPPHASE[2]	0	When this bit is set to 1, phase C current generated IPEAKVAL[23:0] value.
31-27		00000	These bits are always 0.

Table 25. VPEAK register (address 0xE501)

Bit Location	Bit Mnemonic	Default value	Description
23-0	VPEAKVAL[23:0]	0	These bits contain the peak value determined in the voltage channel.
24	VPPHASE[0]	0	When this bit is set to 1, phase A voltage generated VPEAKVAL[23:0] value.
25	VPPHASE[1]	0	When this bit is set to 1, phase B voltage generated VPEAKVAL[23:0] value.
26	VPPHASE[2]	0	When this bit is set to 1, phase C voltage generated VPEAKVAL[23:0] value.
31-27		00000	These bits are always 0.

Table 26. STATUS0 register (address 0xE502)

Bit Location	Bit Mnemonic	Default value	Description
0	AEHF	0	When this bit is set to 1, it indicates that bit 30 of any one of the total active energy registers AWATTHR, BWATTHR, CWATTHR has changed.
1-3	Reserved	000	These bits are always 0.
4	VAEHF	0	When this bit is set to 1, it indicates that bit 30 of any one of the apparent energy registers AVAHR, BVAHR, CVAHR has changed.
5	LENERGY	0	When this bit is set to 1, in line energy accumulation mode, it indicates the end of an integration over an integer number of half line cycles set in LINECYC[15:0] register.
6	REVAPA	0	When this bit is set to 1, it indicates that the phase A total active power has changed sign. The sign itself is indicated in bit 0 (AWSIGN) of PHSIGN[15:0] register (see Table 36).
7	REVAPB	0	When this bit is set to 1, it indicates that the phase B total active power has changed sign. The sign itself is indicated in bit 1 (BWSIGN) of PHSIGN[15:0] register (see Table 36).
8	REVAPC	0	When this bit is set to 1, it indicates that the phase C total active power has changed sign. The sign itself is indicated in bit 2 (CWSIGN) of PHSIGN[15:0] register (see Table 36).
9	REVPSUM1	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF1 data path has changed sign. The sign itself is indicated in bit 3 (SUM1SIGN) of PHSIGN[15:0] register (see Table 36).
10-12	Reserved	000	These bits are always 0.
13	REVPSUM2	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF2 data path has changed sign. The sign itself is indicated in bit 7 (SUM2SIGN) of PHSIGN[15:0] register (see Table 36).
14	CF1		When this bit is set to 1, it indicates a high to low transition has occurred at CF1 pin, that is an active low pulse has been generated. The bit is set even if the CF1 output is disabled by setting bit 9 (CF1DIS) to 1 in CFMODE[15:0] register. The type of the powers used at CF1 pin is determined by bits 2-0 (CF1SEL) in CFMODE[15:0] register (see Table 34).
15	CF2		When this bit is set to 1, it indicates a high to low transition has occurred at CF2 pin, that is an active low pulse has been generated. The bit is set even if the CF2 output is disabled by setting bit 10 (CF2DIS) to 1 in CFMODE[15:0] register. The type of the powers used at CF2 pin is determined by bits 5-3 (CF2SEL) in CFMODE[15:0] register (see Table 34).
16	CF3		When this bit is set to 1, it indicates a high to low transition has occurred at CF3 pin, that is an active low pulse has been generated. The bit is set even if the CF3 output is disabled by setting bit 11 (CF3DIS) to 1 in CFMODE[15:0] register. The type of the powers used at CF3 pin is determined by bits 8-6 (CF3SEL) in CFMODE[15:0] register (seeTable 34).
17	DREADY	0	When this bit is set to 1, it indicates that all periodical (at 8KHz rate) DSP computations have

Bit Location	Bit Mnemonic	Default value	Description
			finished.
18	REVPSUM3	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF3 data path has changed sign. The sign itself is indicated in bit 8 (SUM3SIGN) of PHSIGN[15:0] register (see Table 36).
31-19	Reserved	0 0000 0000 0000	These bits are always 0.

Table 27. STATUS1 register (address 0xE503)

Bit Location	Bit Mnemonic	Default value	Description
0	NLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no-load condition based on total active powers. The phase is indicated in bits 2-0 (NLPHASE) in PHNOLOAD[15:0] register (see Table 31).
1	Reserved	0	This bit is always 0.
2	VANLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no-load condition based on apparent power. The phase is indicated in bits 8-6 (VANLPHASE) in PHNOLOAD[15:0] register (see Table 31).
3	ZXTOVA	0	When this bit is set to 1, it indicates a zero crossing on phase A voltage is missing.
4	ZXTOVB	0	When this bit is set to 1, it indicates a zero crossing on phase B voltage is missing.
5	ZXTOVC	0	When this bit is set to 1, it indicates a zero crossing on phase C voltage is missing.
6	ZXTOIA	0	When this bit is set to 1, it indicates a zero crossing on phase A current is missing.
7	ZXTOIB	0	When this bit is set to 1, it indicates a zero crossing on phase B current is missing.
8	ZXTOIC	0	When this bit is set to 1, it indicates a zero crossing on phase C current is missing.
9	ZXVA	0	When this bit is set to 1, it indicates a zero crossing has been detected on phase A voltage.
10	ZXVB	0	When this bit is set to 1, it indicates a zero crossing has been detected on phase B voltage.
11	ZXVC	0	When this bit is set to 1, it indicates a zero crossing has been detected on phase C voltage.
12	ZXIA	0	When this bit is set to 1, it indicates a zero crossing has been detected on phase A current.
13	ZXIB	0	When this bit is set to 1, it indicates a zero crossing has been detected on phase B current.
14	ZXIC	0	When this bit is set to 1, it indicates a zero crossing has been detected on phase C current.
15	RSTDONE	1	In case of a software reset command, i.e. bit 7 (SWRST) set to 1 in CONFIG[15:0] register, or a transition from PSM3 to PSM0 or a hardware reset, this bit is set to 1 at the end of the transition process and after all registers changed value to default. $\overline{\text{IRQ1}}$ pin goes low to signal this moment because this interrupt cannot be disabled.
16	SAG	0	When this bit is set to 1, it indicates a SAG event has occurred on one of the phases indicated by bits 14-12 (VSPHASE) in PHSTATUS[15:0] register (see Table 30).
17	OI	0	When this bit is set to 1, it indicates an overcurrent event has occurred on one of the phases indicated by bits 5-3 (OIPHASE) in PHSTATUS[15:0] register (see Table 30).
18	OV	0	When this bit is set to 1, it indicates an overcurrent event has occurred on one of the phases indicated by bits 11-9 (OVPHASE) in PHSTATUS[15:0] register (see Table 30).
19	SEQERR	0	When this bit is set to 1, it indicates a negative to positive zero crossing on phase A voltage was not followed by a negative to positive zero crossing on phase B voltage, but by a negative to positive zero crossing on phase C voltage.
20	Reserved	0	
21	Reserved	1	
22	Reserved	0	
23	PKI	0	When this bit is set to 1, it indicates that the period used to detect the peak value in the current channel has ended. IPEAK[31:0] register contains the peak value and the phase where the peak has been detected (see Table 24).
24	PKV	0	When this bit is set to 1, it indicates that the period used to detect the peak value in the voltage channel has ended. VPEAK[31:0] register contains the peak value and the phase where the peak has been detected (see Table 25).
31:25	Reserved	000 0000	These bits are always 0.

Table 28. MASK0 register (address 0xE50A)

Bit Location	Bit Mnemonic	Default value	Description
0	AEHF	0	When this bit is set to 1, it enables an interrupt when bit 30 of any one of the total active energy registers AWATTHR, BWATTHR, CWATTHR changes.
1-3	Reserved	000	These bits do not manage any functionality.
4	VAEHF	0	When this bit is set to 1, it enables an interrupt when bit 30 of any one of the apparent energy registers AVAHR, BVAHR, CVAHR changes.
5	LENERGY	0	When this bit is set to 1, in line energy accumulation mode, it enables an interrupt at the end of an integration over an integer number of half line cycles set in LINECYC[15:0] register.
6	REVAPA	0	When this bit is set to 1, it enables an interrupt when the phase A active power register changes sign.
7	REVAPB	0	When this bit is set to 1, it enables an interrupt when the phase B active power changes sign.
8	REVAPC	0	When this bit is set to 1, it indicates that the phase C active power changes sign.
9	REVPSUM1	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF1 data path changes sign.
10-12	Reserved	000	These bits do not manage any functionality.
13	REVPSUM2	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF2 data path changes sign.
14	CF1		When this bit is set to 1, it enables an interrupt when a high to low transition occurs at CF1 pin, that is an active low pulse is generated. The interrupt may be enabled even if the CF1 output is disabled by setting bit 9 (CF1DIS) to 1 in CFMODE[15:0] register. The type of the powers used at CF1 pin is determined by bits 2-0 (CF1SEL) in CFMODE[15:0] register (see Table 34).
15	CF2		When this bit is set to 1, it enables an interrupt when a high to low transition occurs at CF2 pin, that is an active low pulse is generated. The interrupt may be enabled even if the CF2 output is disabled by setting bit 10 (CF2DIS) to 1 in CFMODE[15:0] register. The type of the powers used at CF2 pin is determined by bits 5-3 (CF2SEL) in CFMODE[15:0] register (see Table 34).
16	CF3		When this bit is set to 1, it enables an interrupt when a high to low transition occurs at CF3 pin, that is an active low pulse is generated. The interrupt may be enabled even if the CF3 output is disabled by setting bit 11 (CF3DIS) to 1 in CFMODE[15:0] register. The type of the powers used at CF3 pin is determined by bits 8-6 (CF3SEL) in CFMODE[15:0] register (seeTable 34).
17	DREADY	0	When this bit is set to 1, it enables an interrupt when all periodical (at 8KHz rate) DSP computations finish.
18	REVPSUM3	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF3 data path changes sign.
31-18	Reserved	00 0000 0000 0000	These bits do not manage any functionality.

Table 29. MASK1 register (address 0xE50B)

Bit Location	Bit Mnemonic	Default value	Description
0	NLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no-load condition based on total active and reactive powers.
1	Reserved	0	This bit does not manage any functionality.
2	VANLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no-load condition based on apparent power.
3	ZXTOVA	0	When this bit is set to 1, it enables an interrupt when a zero crossing on phase A voltage misses.
4	ZXTOVB	0	When this bit is set to 1, it enables an interrupt when a zero crossing on phase B voltage misses.
5	ZXTOVC	0	When this bit is set to 1, it enables an interrupt when a zero crossing on phase C voltage misses.
6	ZXTOIA	0	When this bit is set to 1, it enables an interrupt when a zero crossing on phase A current misses.
7	ZXTOIB	0	When this bit is set to 1, it enables an interrupt when a zero crossing on phase B current is missing.
8	ZXTOIC	0	When this bit is set to 1, it enables an interrupt when a zero crossing on phase C current is missing.
9	ZXVA	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on phase A voltage.
10	ZXVB	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on phase B voltage.
11	ZXVC	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on phase C voltage.
12	ZXIA	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on phase A current.

Bit Location	Bit Mnemonic	Default value	Description
13	ZXIB	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on phase B current.
14	ZXIC	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on phase C current.
15	RSTDONE	0	Because the RSTDONE interrupt cannot be disabled, this bit does not have any functionality attached. It can be set to 1 or cleared to 0 without having any effect.
16	SAG	0	When this bit is set to 1, it enables an interrupt when a SAG event occurs on one of the phases indicated by bits 14-12 (VSPHASE) in PHSTATUS[15:0] register (see Table 30).
17	OI	0	When this bit is set to 1, it enables an interrupt when an overcurrent event occurs on one of the phases indicated by bits 5-3 (OIPHASE) in PHSTATUS[15:0] register (see Table 30).
18	OV	0	When this bit is set to 1, it enables an interrupt when an overcurrent event occurs on one of the phases indicated by bits 11-9 (OVPHASE) in PHSTATUS[15:0] register (see Table 30).
19	SEQERR	0	When this bit is set to 1, it enables an interrupt when a negative to positive zero crossing on phase A voltage is not followed by a negative to positive zero crossing on phase B voltage, but by a negative to positive zero crossing on phase C voltage.
20-22	Reserved	000	These bits do not manage any functionality.
23	PKI	0	When this bit is set to 1, it enables an interrupt when the period used to detect the peak value in the current channel has ended.
24	PKV	0	When this bit is set to 1, it enables an interrupt when the period used to detect the peak value in the voltage channel has ended.
31:25		000 0000	These bits do not manage any functionality.

Table 30. PHSTATUS register (address 0xE600)

Bit Location	Bit Mnemonic	Default value	Description
2-0		000	These bits are always 0.
3	OIPHASE[0]	0	When this bit is set to 1, phase A current generated bit 17 (OI) in STATUS1[31:0]
4	OIPHASE[1]	0	When this bit is set to 1, phase B current generated bit 17 (OI) in STATUS1[31:0]
5	OIPHASE[1]	0	When this bit is set to 1, phase C current generated bit 17 (OI) in STATUS1[31:0]
8-6		000	These bits are always 0.
9	OVPHASE[0]	0	When this bit is set to 1, phase A voltage generated bit 18 (OV) in STATUS1[31:0]
10	OVPHASE[1]	0	When this bit is set to 1, phase B voltage generated bit 18 (OV) in STATUS1[31:0]
11	OVPHASE[2]	0	When this bit is set to 1, phase C voltage generated bit 18 (OV) in STATUS1[31:0]
12	VSPHASE[0]	0	When this bit is set to 1, phase A voltage generated bit 16 (SAG) in STATUS1[31:0]
13	VSPHASE[1]	0	When this bit is set to 1, phase B voltage generated 16 (SAG) in STATUS1[31:0]
14	VSPHASE[2]	0	When this bit is set to 1, phase C voltage generated 16 (SAG) in STATUS1[31:0]
15		0	This bit is always 0.

Table 31. PHNOLOAD register (address 0xE608)

Bit Location	Bit Mnemonic	Default value	Description
0	NLPHASE[0]	0	-0: phase A is out of no-load condition based on total active powers. -1: phase A is in no load condition based on total active powers. Bit set together with bit 0 (NLOAD) in STATUS1[31:0].
1	NLPHASE[1]	0	-0: phase B is out of no-load condition based on total active powers. -1: phase B is in no load condition based on total active powers. Bit set together with bit 0 (NLOAD) in STATUS1[31:0].
2	NLPHASE[2]	0	-0: phase C is out of no-load condition based on total active powers. -1: phase C is in no load condition based on total active powers. Bit set together with bit 0 (NLOAD) in STATUS1[31:0].
3-5	Reserved	000	These bits are always 0.
6	VANLPHASE[0]	0	-0: phase A is out of no-load condition based on apparent power. -1: phase A is in no load condition based on apparent power. Bit set together with bit 2 (VANLOAD) in STATUS1[31:0].
7	VANLPHASE[1]	0	-0: phase B is out of no-load condition based on apparent power. -1: phase B is in no load condition based on apparent power. Bit set together with bit 2 (VANLOAD) in STATUS1[31:0].
8	VANLPHASE[2]	0	-0: phase C is out of no-load condition based on apparent power. -1: phase C is in no load condition based on apparent power. Bit set together with bit 2

Bit Location	Bit Mnemonic	Default value	Description
			(VANLOAD) in STATUS1[31:0].
15-9	Reserved	000 0000	These bits are always 0.

Table 32. COMPMODE register (address 0xE60E)

Bit Location	Bit Mnemonic	Default value	Description
0	TERMSEL1[0]	1	Setting all TERMSEL1[2:0] to 1 signifies the sum of all 3 phases is included in CF1 output Phase A is included in CF1 outputs calculations
1	TERMSEL1[1]	1	Phase B is included in CF1 outputs calculations
2	TERMSEL1[2]	1	Phase C is included in CF1 outputs calculations
3	TERMSEL2[0]	1	Setting all TERMSEL2[2:0] to 1 signifies the sum of all 3 phases is included in CF2 output Phase A is included in CF2 outputs calculations
4	TERMSEL2[1]	1	Phase B is included in CF2 outputs calculations
5	TERMSEL2[2]	1	Phase C is included in CF2 outputs calculations
6	TERMSEL3[0]	1	Setting all TERMSEL3[2:0] to 1 signifies the sum of all 3 phases is included in CF3 output Phase A is included in CF3 outputs calculations
7	TERMSEL3[1]	1	Phase B is included in CF3 outputs calculations
8	TERMSEL3[2]	1	Phase C is included in CF3 outputs calculations
10,9	ANGLESEL[1:0]	00	-00:the angles between phase voltages and phase currents are measured -01: the angles between phase voltages are measured -10: the angles between phase currents are measured -11: no angles are measured
11	VNOMAEN	0	When this bit is 0, the apparent power on phase A is computed regularly. When this bit is 1, the apparent power on phase A is computed using VNOM[23:0] register instead of regular measured rms phase voltage.
12	VNOMBEN	0	When this bit is 0, the apparent power on phase B is computed regularly. When this bit is 1, the apparent power on phase B is computed using VNOM[23:0] register instead of regular measured rms phase voltage.
13	VNOMCEN	0	When this bit is 0, the apparent power on phase C is computed regularly. When this bit is 1, the apparent power on phase C is computed using VNOM[23:0] register instead of regular measured rms phase voltage.
14	SELFREQ	0	When the ADE7854 is connected to 50Hz networks, this bit should be cleared to 0 (default value). When the ADE7854 is connected to 60Hz networks, this bit should be set to 1.
15	Reserved	0	This bit does not manage any functionality.

Table 33: GAIN register (address 0xE60F)

Bit	Mnemonic	Default	Description
2 to 0	PGA1[2:0]	000	Phase currents gain selection -000: gain=1 -001: gain=2 -010: gain=4 -011: gain=8 -100: gain=16 -101, 110, 111: reserved. When set, the ADE7854 behaves like PGA1 [2:0]=000
5 to 3	Reserved	000	These bits do not manage any functionality.
8 to 6	PGA3[2:0]	000	Phase voltages gain selection -000: gain=1 -001: gain=2 -010: gain=4 -011: gain=8 -100: gain=16 -101, 110, 111: reserved. When set, the ADE7854 behaves like PGA3 [2:0]=000
15 to 9		000 0000	Reserved. These bits do not manage any functionality.

Table 34. CFMODE register (address 0xE610)

Bit Location	Bit Mnemonic	Default value	Description
2-0	CF1SEL[2:0]	000	-000: CF1 frequency proportional to the sum of total active powers on each phase identified by bits 2-0 (TERMSEL1) in COMPMODE[15:0] register. -001:if selected, CF1 pin is set low permanently. -010: CF1 frequency proportional to the sum of apparent powers on each phase identified by bits 2-0 (TERMSEL1) in COMPMODE[15:0] register. -011,100: if selected, CF1 pin is set low permanently. -101,110,111: reserved. When set, the ADE7854 behave like CF1SEL [2:0]=000.
5-3	CF2SEL[2:0]	000	-000: CF2 frequency proportional to the sum of total active powers on each phase identified by bits 5:3 (TERMSEL2) in COMPMODE[15:0] register. -001: if selected, CF2 pin is set low permanently. -010: CF2 frequency proportional to the sum of apparent powers on each phase identified by bits 5:3 (TERMSEL2) in COMPMODE[15:0] register. -011,100: if selected, CF2 pin is set low permanently. -100: if selected, CF2 pin is set low permanently. -101,110,111: reserved. When set, the ADE7854 behaves like CF2SEL [2:0]=000.
8-6	CF3SEL[2:0]	000	-000: CF3 frequency proportional to the sum of total active powers on each phase identified by bits 8:6 (TERMSEL3) in COMPMODE[15:0] register. -001: if selected, CF3 pin is set low permanently. -010: CF3 frequency proportional to the sum of apparent powers on each phase identified by bits 8:6 (TERMSEL3) in COMPMODE[15:0] register. -011,100: if selected, CF3 pin is set low permanently. -101,110,111: reserved. When set, the ADE7854 behaves like CF3SEL [2:0]=000.
9	CF1DIS	1	When this bit is set to 1, the CF1 output is disabled. The respective digital to frequency converter remains enabled even if CF1DIS=1. When set to 0, the CF1 output is enabled.
10	CF2DIS	1	When this bit is set to 1, the CF2 output is disabled. The respective digital to frequency converter remains enabled even if CF2DIS=1. When set to 0, the CF2 output is enabled.
11	CF3DIS	1	When this bit is set to 1, the CF3 output is disabled. The respective digital to frequency converter remains enabled even if CF3DIS=1. When set to 0, the CF3 output is enabled.
12	CF1LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF1 pulse is generated. See Synchronizing energy registers with CFx outputs section.
13	CF2LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF2 pulse is generated. See Synchronizing energy registers with CFx outputs section.
14	CF3LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF3 pulse is generated. See Synchronizing energy registers with CFx outputs section.
15	Reserved	0	This bit does not manage any functionality.

Table 35. APHCAL, BPHCAL, CPHCAL registers (addresses 0xE614, 0xE615, 0xE616)

Bit Location	Bit Mnemonic	Default value	Description
4-0	XPHCAL[4:0]	00000	These bits introduce a delay equal to XPHCAL cycles, i.e. a number between 0 and 31
6-5	YPHCAL[1:0]	00	These bits introduce a delay equal to YPHCAL*32+XPHCAL. If current channel compensation (VPHCAL=0), YPHCAL can have any value between 0 and 3. If voltage channel compensation (VPHCAL=1), YPHCAL can be maximum 1 and any number above it is considered equal to 1.
8-7	ZPHCAL[1:0]	00	The number of cycles introduced as delay only for current channel is equal to ZPHCAL*128+ YPHCAL*32+XPHCAL. For current channel compensation, ZPHCAL can be maximum 2. ZPHCAL bits are always considered 0 for voltage channel compensation.
9	VPHCAL	0	-0: current channel compensation -1: voltage channel compensation
15-10	Reserved	000000	These bits do not manage any functionality.

Table 36. PHSIGN register (address 0xE617)

Bit Location	Bit Mnemonic	Default value	Description
0	AWSIGN	0	-0: if total active power on phase A is positive. -1: if total active power on phase A is negative.
1	BWSIGN	0	-0: if total active power on phase B is positive.

Bit Location	Bit Mnemonic	Default value	Description
			-1: if total active power on phase B is negative.
2	CWSIGN	0	-0: if total active power on phase C is positive. -1: if total active power identified on phase C is negative.
3	SUM1SIGN	0	-0: if the sum of all phase powers in the CF1 data path is positive. -1: if the sum of all phase powers in the CF1 data path is negative. Phase powers in the CF1 data path are identified by bits 2,1,0 (TERMSEL1) of COMPMODE[15:0] register and by bits 2,1,0 (CF1SEL) of CFMODE[15:0] register.
4-6	Reserved	000	These bits are always 0.
7	SUM2SIGN	0	-0: if the sum of all phase powers in the CF2 data path is positive. -1: if the sum of all phase powers in the CF2 data path is negative. Phase powers in the CF2 data path are identified by bits 5,4,3 (TERMSEL2) of COMPMODE[15:0] register and by bits 5,4,3 (CF2SEL) of CFMODE[15:0] register.
8	SUM3SIGN	0	-0: if the sum of all phase powers in the CF3 data path is positive. -1: if the sum of all phase powers in the CF3 data path is negative. Phase powers in the CF3 data path are identified by bits 8,7,6 (TERMSEL3) of COMPMODE[15:0] register and by bits 8,7,6 (CF3SEL) of CFMODE[15:0] register.
15-9	Reserved	000 0000	These bits are always 0.

Table 37. CONFIG register (address 0xE618)

Bit Location	Bit Mnemonic	Default value	Description
0	INTEN	0	Integrator Enable. When this bit is set to 1, the internal digital integrator is enabled for use in meters utilizing Rogowski Coils on all 3 phase and neutral current inputs. When this bit is cleared to 0, the internal digital integrator is disabled.
2,1	Reserved	000	These bits do not manage any functionality.
3	SWAP	0	When this bit is set to 1, the voltage channel outputs are swapped with the current channel outputs. Thus, the current channel information will be present in the voltage channel registers and vice versa.
4	MOD1SHORT	0	When this bit is set to 1, the voltage channel ADCs behave as if the voltage inputs were put to ground.
5	MOD2SHORT	0	When this bit is set to 1, the current channel ADCs behave as if the voltage inputs were put to ground.
6	HSDCEN	0	When this bit is set to 1, the HSDC serial port is enabled and HSCLK functionality is chosen at CF3/HSCLK pin. When this bit is cleared to 0, HSDC is disabled and CF3 functionality is chosen at CF3/HSCLK pin.
7	SWRST	0	When this bit is set to 1, a software reset is initiated.
9,8	VTOIA[1:0]	00	These bits decide what phase voltage is considered together with phase A current in the power path: 00=phase A voltage 01=phase B voltage 10=phase C voltage 11=reserved. When set, the ADE7854 behaves like VTOIA [1:0]=00
11,10	VTOIB[1:0]	00	These bits decide what phase voltage is considered together with phase B current in the power path: 00=phase B voltage 01=phase C voltage 10=phase A voltage 11=reserved. When set, the ADE7854 behaves like VTOIB [1:0]=00
13,12	VTOIC[1:0]	00	These bits decide what phase voltage is considered together with phase C current in the power path: 00=phase C voltage 01=phase A voltage 10=phase B voltage 11=reserved. When set, the ADE7854 behaves like VTOIC [1:0]=00
14,15	Reserved	0	These bits do not manage any functionality.

Table 38. MMODE register (address 0xE700)

Bit Location	Bit Mnemonic	Default value	Description
1,0	PERSEL[1:0]	00	-00: Phase A selected as source of the voltage line period measurement -01: Phase B selected as source of the voltage line period measurement -10: Phase C selected as source of the voltage line period measurement -11:Reserved. When set, the ADE7854 behaves like PERSEL[1:0]=00
2	PEAKSEL[0]	1	PEAKSEL[2:0] bits can all be set to 1 simultaneously to allow peak detection on all 3 phases simultaneously. If more than one PEAKSEL[2:0] bits are set to 1, then the peak measurement period indicated in PEAKCYC[7:0] register decreases accordingly because zero crossings are detected on more than one phase. When this bit is set to 1, phase A is selected for the voltage and current peak registers
3	PEAKSEL[1]	1	When this bit is set to 1, phase B is selected for the voltage and current peak registers
4	PEAKSEL[2]	1	When this bit is set to 1, phase C is selected for the voltage and current peak registers
7-5		000	Reserved. These bits do not manage any functionality.

Table 39. ACCMODE Register (Address 0xE701)

Bit Location	Bit Mnemonic	Default value	Description
1,0	WATTACC[1:0]	00	-00: signed accumulation mode of the total active powers -01: reserved. When set, the ADE7854 behaves like WATTACC[1:0]=00 -10: reserved. When set, the ADE7854 behaves like WATTACC[1:0]=00 -11: absolute accumulation mode of the total active powers
3,2	Reserved	00	These bits do not manage any functionality
5,4	CONSEL[1:0]	00	These bits are used to select the inputs to the energy accumulation registers: -00: 3 phase 4 wires with 3 voltage sensors -01: 3 phase 3 wires delta connection -10: 3 phase 4 wires with 2 voltage sensors -11: 3 phase 4 wires delta connection
6-7	Reserved	0	These bits should be kept at 00 for proper operation

Energy Registers	CONSEL[1:0]=00	CONSEL[1:0]=01	CONSEL[1:0]=10	CONSEL[1:0]=11
AWATTHR	VA x IA	VA x IA	VA x IA	VA x IA
BWATTHR	VB x IB	0	VB=-VA-VC VB x IB	VB=-VA VB x IB
CWATTHR	VC x IC	VC x IC	VC x IC	VC x IC
AVAHR	VA_{RMS} x IA_{RMS}	VA_{RMS} x IA_{RMS}	VA_{RMS} x IA_{RMS}	VA_{RMS} x IA_{RMS}
BVAHR	VB_{RMS} x IB_{RMS}	0	VB_{RMS} x IB_{RMS}	VB_{RMS} x IB_{RMS}
CVAHR	VC_{RMS} x IC_{RMS}	VC_{RMS} x IC_{RMS}	VC_{RMS} x IC_{RMS}	VC_{RMS} x IC_{RMS}

Table 40. LCYCMODE register (address 0xE702)

Bit Location	Bit Mnemonic	Default value	Description
0	LWATT	0	-0: the watt-hour accumulation registers (AWATTHR, BWATTHR, CWATTHR) are placed in regular accumulation mode. -1: the watt-hour accumulation registers (AWATTHR, BWATTHR, CWATTHR) are placed into line-cycle accumulation mode.
1	Reserved	0	This bit does not manage any functionality.
2	LVA	0	-0: the va-hour accumulation registers (AVAHR, BVAHR, CVAHR) are placed in regular accumulation mode. -1: the va-hour accumulation registers (AVAHR, BVAHR, CVAHR) are placed into line-cycle accumulation mode.
3	ZXSEL[0]	1	-0: phase A is not selected for zero crossings counts in the line cycle accumulation mode. -1: phase A is selected for zero crossings counts in the line cycle accumulation mode. If more than one phase is selected for zero crossing detection, the accumulation time is shorten accordingly
4	ZXSEL[1]	1	-0: phase B is not selected for zero crossings counts in the line cycle accumulation mode. -1: phase B is selected for zero crossings counts in the line cycle accumulation mode.
5	ZXSEL[2]	1	-0: phase C is not selected for zero crossings counts in the line cycle accumulation mode.

Bit Location	Bit Mnemonic	Default value	Description
			-1: phase C is selected for zero crossings counts in the line cycle accumulation mode.
6	RSTREAD	1	-0: Read-with-reset of all energy registers is disabled. This bit should be cleared to 0 when bits 2,1,0 (LWATT, LVAR, LVA) are set to 1. -1: Read-with-reset of all xWATTHR, xVARHR, xVAHR registers (x=A,B,C) is enabled. This means a read of those registers resets them to 0.
7	Reserved	0	This bit does not manage any functionality.

Table 41. HSDC_CFG register (address 0xE706)

Bit Location	Bit Mnemonic	Default value	Description
0	HCLK	0	-0: HSCLK is 8MHz -1: HSCLK is 4MHz
1	HSIZE	0	-0: HSDC transmits the 32bit registers in 32bit packages, most significant bit first. -1: HSDC transmits the 32bit registers in 8bit packages, most significant bit first.
2	HGAP	0	-0: no gap is introduced between packages. -1: a gap of 7 HCLK cycles is introduced between packages.
4,3	HXFER[1:0]	00	-00=HSDC transmits all 16 registers shown in Billable registers List -01= HSDC transmits 7 instantaneous values of currents and voltages -10= HSDC transmits 9 instantaneous values of phase powers -11=reserved. If set, the ADE7854 behaves as if HXFER[1:0]=00.
5	HSAPOL	0	-0: HSACTIVE output pin is active LOW. -1: HSACTIVE output pin is active HIGH
7,6	Reserved	00	These bits do not manage any functionality.

Table 42. CONFIG2 register (address 0xEC01)

Bit Location	Bit Mnemonic	Default value	Description
0	EXTREFEN	0	When this bit is 0, signifies the internal voltage reference is used in the ADCs. When this bit is 1, an external reference is connected to the pin 17 REF in/out
1	I2C_LOCK	0	When this bit is 0, the $\overline{SS}$ /HSA pin can be toggled 3 times to activate the SPI port. If I^2C is the active serial port, this bit must be set to 1 to lock it in. From this moment on, spurious togglings of the $\overline{SS}$ pin and an eventual switch into using SPI port is no longer possible. If SPI is the active serial port, any write to CONFIG2[7:0] register locks the port. From this moment on, a switch into using I^2C port is no longer possible. Once locked, the serial port choice is maintained when the ADE7854 changes between PSM0 and PSM3 power modes.
7-2	Reserved	00000	These bits do not manage any functionality.

OUTLINE DIMENSIONS

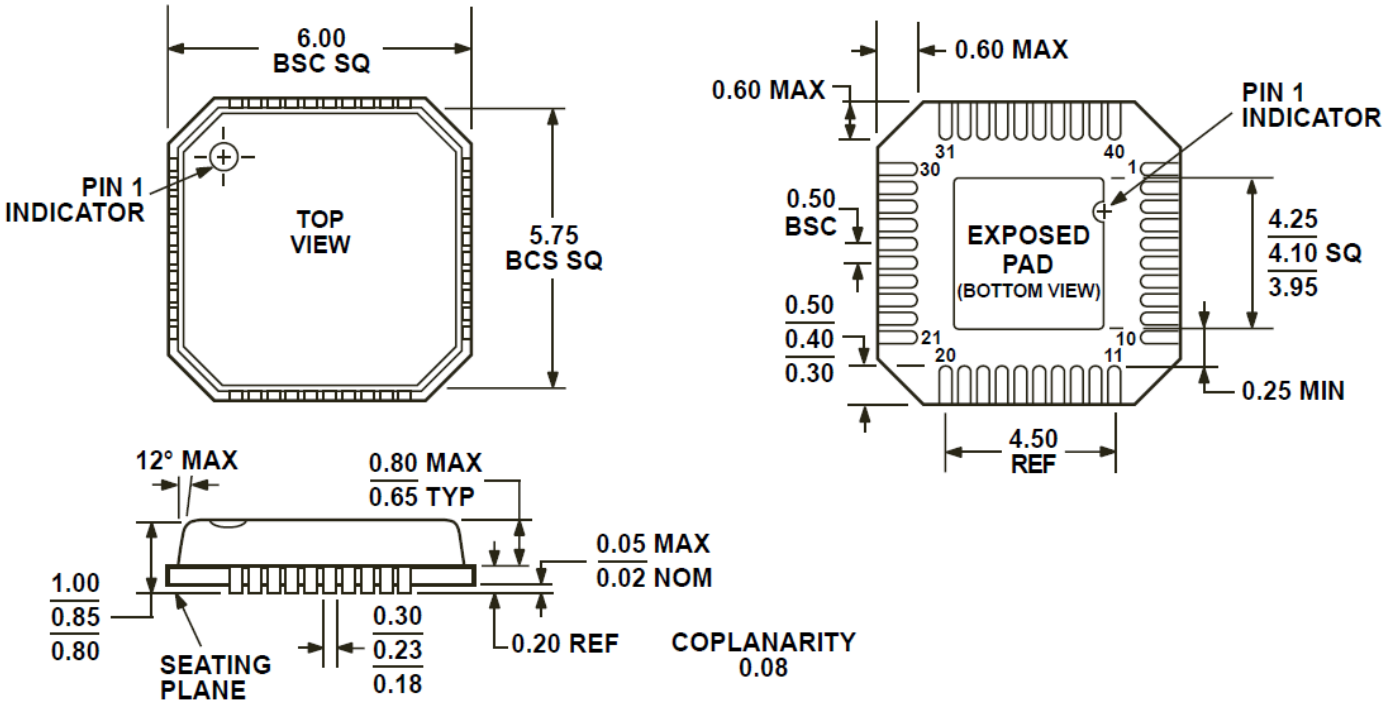

Figure 70. 40LFCSP (6 x 6 mm), CP-40-1
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADE7854ACPZ	–40°C to +85°C	40-Lead LFCSP	CP-40-1
ADE7854ACPZ-RL	–40°C to +85°C	40-Lead LFCSP, Reel	CP-40-1
EVAL-ADE7854EBZ		ADE7854 evaluation board	

NOTES

NOTES

PR08017-0-2/09(PrC)