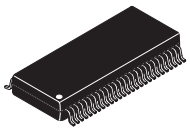
Integrated Quad Half-Bridge, Triple High-Side and EC Glass Driver with Embedded MCU and LIN for High End Mirror

908E622

QUAD HALF-BRIDGE, TRIPLE HIGH-SIDE SWITCH AND EC GLASS CIRCUITRY WITH EMBEDDED MCU AND LIN



DWB SUFFIX
98ARL10519D
54-TERMINAL SOICW-EP

The 908E622 is an integrated single-package solution that includes a high-performance HC08 microcontroller with a *SMARTMOS*™ analog control IC. The HC08 includes flash memory, a timer, enhanced serial communications interface (ESCI), an analog-to-digital converter (ADC), serial peripheral interface (SPI) (only internal), and an internal clock generator module. The analog control die provides four half-bridge and three high-side outputs with diagnostic functions, an EC glass driver circuit, a Hall-Effect sensor input, analog inputs, voltage regulator, window watchdog, and local interconnect network (LIN) physical layer.

The single-package solution, together with LIN, provides optimal application performance adjustments and space-saving PCB design. It is well suited for the control of automotive high-end mirrors.

Features

- High-Performance M68HC908EY16 Core
- 16 K Bytes of On-Chip Flash Memory, 512 Bytes of RAM
- Internal Clock Generator Module (ICG)
- Two 16-Bit, 2-Channel Timers
- 10-Bit Analog-to-Digital Converter (ADC)
- LIN Physical Layer Interface
- Autonomous MCU Watchdog / MCU Supervision
- One Analog Input with Switchable Current Source
- Four Low RDS(ON) Half-Bridge Outputs
- Three Low RDS(ON) High-Side Outputs
- EC glass driver circuitry
- Wake-Up Input
- One 2/3-Pin Hall-Effect Sensor Input
- 12 Microcontroller I/Os

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MM908E622ACDWB/R2	-40°C to 85°C	54 SOICW-EP

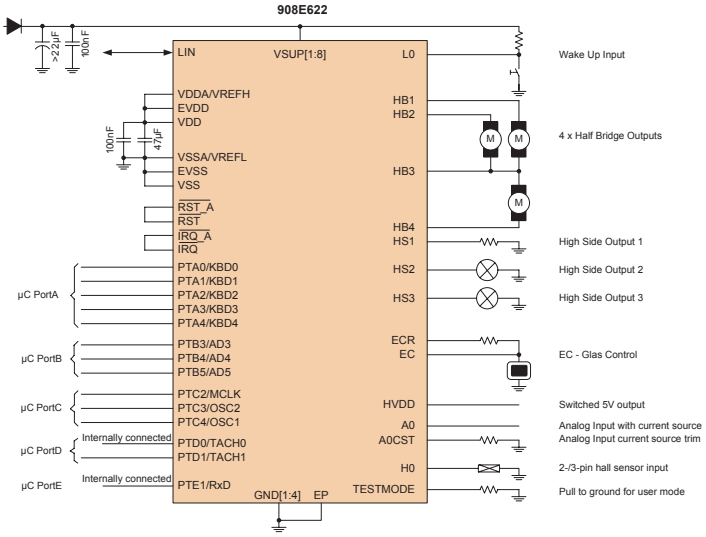


Figure 1. 908E622 Simplified Application Diagram

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

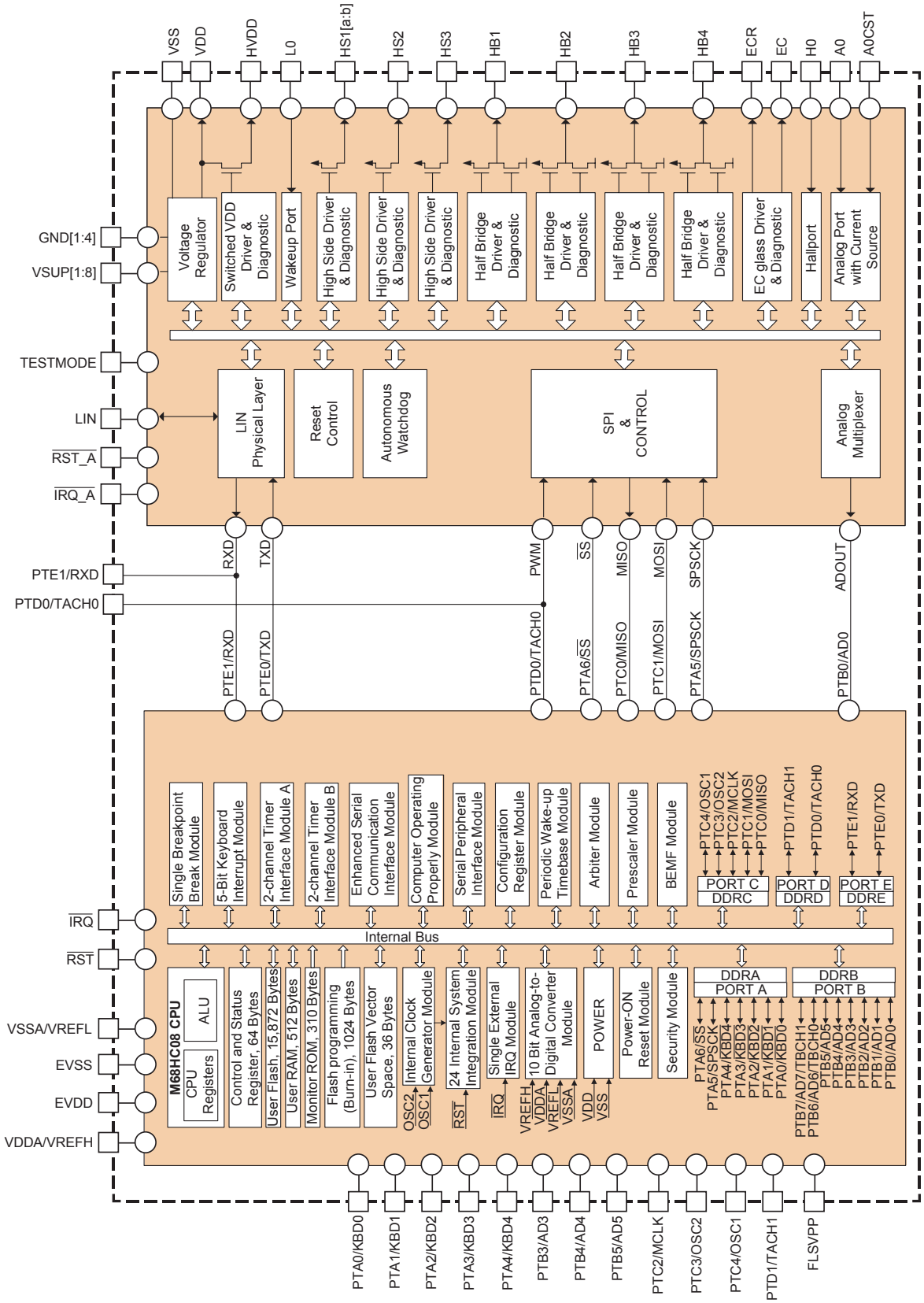


Figure 2. 908E622 Simplified Internal Block Diagram

TERMINAL CONNECTIONS

Transparent Top View of Package

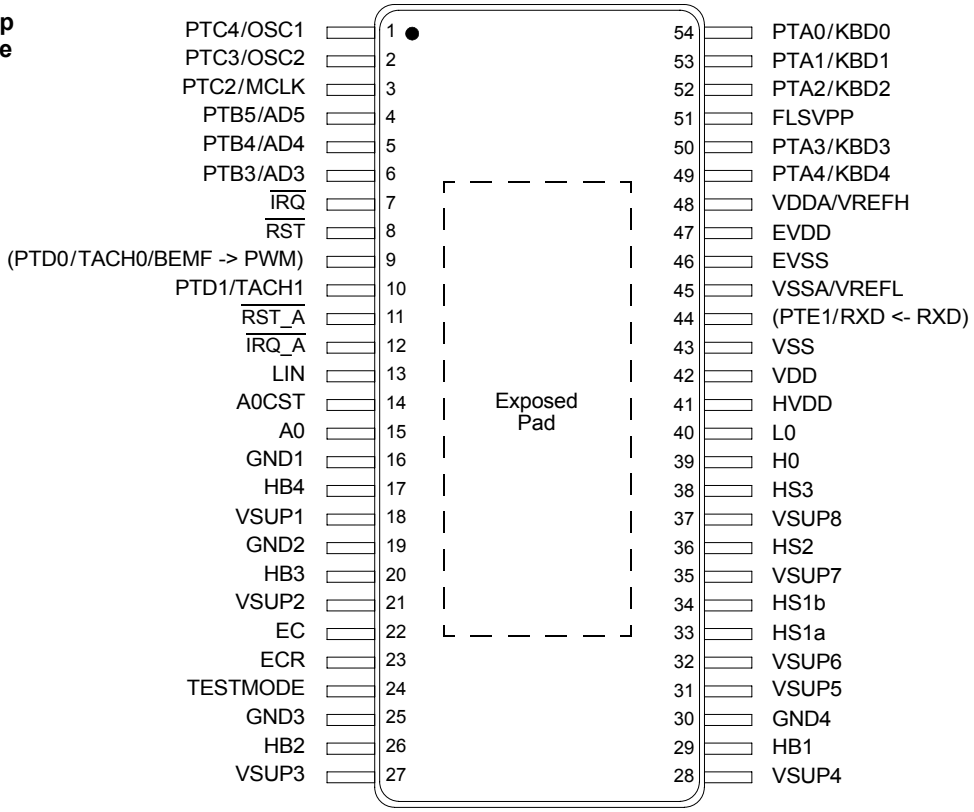


Figure 3. Terminal Connections

Table 1. Terminal Definitions

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 21.

Die	Terminal	Terminal Name	Formal Name	Definition
MCU	1 2 3	PTC4/OSC1 PTC3/OSC2 PTC2/MCLK	Port C I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
MCU	4 5 6	PTB5/AD5 PTB4/AD4 PTB3/AD3	Port B I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
MCU	7	$\overline{\text{IRQ}}$	External Interrupt Input	This terminal is an asynchronous external interrupt input terminal.
MCU	8	$\overline{\text{RST}}$	External Reset	This terminal is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.
MCU / Analog	9	(PTD0/TACH0/BEMF -> PWM)	PWM signal	This terminal is the PWM signal test terminal. It internally connects the MCU PTD0/TACH0 terminal with the Analog die PWM input. Note: Do not connect in the application.
MCU	10	PTD1/TACH1	Port D I/Os	This terminal is a special-function, bidirectional I/O port terminal that is shared with other functional modules in the MCU.
MCU / Analog	44	(PTE1/RXD <- RXD)	LIN Transceiver Output	This terminal is the LIN Transceiver output test terminal. It internally connects the MCU PTE1/RXD terminal with the Analog die LIN transceiver output terminal RXD. Note: Do not connect in the application.

Table 1. Terminal Definitions (continued)

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 21.

Die	Terminal	Terminal Name	Formal Name	Definition
MCU	45 48	VSSA/VREFL VDDA/VREFH	ADC Supply and Reference Terminals	These terminals are the power supply and voltage reference terminals for the analog-to-digital converter (ADC).
MCU	46 47	EVSS EVDD	MCU Power Supply Terminals	These terminals are the ground and power supply terminals, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Terminal	For test purposes only. Do not connect in the application.
Analog	11	$\overline{\text{RST\_A}}$	Internal Reset	This terminal is the bidirectional reset terminal of the analog die.
Analog	12	$\overline{\text{IRQ\_A}}$	Internal Interrupt Output	This terminal is the interrupt output terminal of the analog die indicating errors or wake-up events.
Analog	13	LIN	LIN Bus	This terminal represents the single-wire bus transmitter and receiver.
Analog	14	A0CST	Analog Input Trim Terminal	This is the Analog Input Trim Terminal for the A0 input. This is to connect a known fixed resistor value to trim the current source measurement.
Analog	15	A0	Analog Input Terminal	This terminal is an analog input port with selectable source values.
Analog	16 19 25 30	GND1 GND2 GND3 GND4	Power Ground Terminals	These terminals are device power ground connections.
Analog	29 26 20 17	HB1 HB2 HB3 HB4	Half-Bridge Outputs	This device includes power MOSFETs configured as four half-bridge driver outputs. These outputs may be configured for DC motor drivers, or as high-side and low-side switches. Note: The HB3 and HB4 have a lower $R_{DS(ON)}$ then HB1 and HB2.
Analog	18 21 27 28 31 32 35	VSUP1 VSUP2 VSUP3 VSUP4 VSUP5 VSUP6 VSUP7	Power Supply Terminals	These terminals are device power supply terminals.
Analog	22 23	EC ECR	EC Glass Terminal EC Ballast Resistor Terminal	These are the Electrochrome Circuitry Terminals. The EC Terminal has to be connected to the EC Glass and the ECR Terminal has to be connected to the external ballast resistor.
Analog	24	TESTMODE	TESTMODE Input	Terminal for test purpose only. In application this terminal needs to be tied GND.
Analog	34 35	HS1a HS1b	High-Side HS1 Output	This output terminal is a low $R_{DS(ON)}$ high-side switch.
Analog	36 38	HS2 HS3	High-Side HS2 Output High-Side HS3 Output	These output terminals are low $R_{DS(ON)}$ high-side switches.
Analog	39	H0	Hall-Effect Sensor / General Purpose Input	This terminal provides an input for a Hall-effect sensor or general purpose input.
Analog	40	L0	Wake-up Input	This terminal provides an high voltage input, which is wake-up capable.

Table 1. Terminal Definitions (continued)

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 21.

Die	Terminal	Terminal Name	Formal Name	Definition
Analog	41	HVDD	Switchable V_{DD} Output	This terminal is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; e.g. potentiometers.
Analog	42	VDD	Voltage Regulator Output	The +5.0 V voltage regulator output terminal is intended to supply the embedded microcontroller.
Analog	43	VSS	Voltage Regulator Ground	Ground terminal for the connection of all non-power ground connections (microcontroller and sensors).
–	EP	Exposed Pad	Exposed Pad	The exposed pad terminal on the bottom side of the package conducts heat from the chip to the PCB board.

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any terminal may cause permanent damage to the device.

Rating	Symbol	Value	Unit
Electrical Ratings			
Supply Voltage Analog Chip Supply Voltage under Normal Operation (Steady-State) Analog Chip Supply Voltage under Transient Conditions (1) MCU Chip Supply Voltage	 $V_{SUP(SS)}$ $V_{SUP(PK)}$ V_{DD}	 -0.3 to 28 -0.3 to 40 -0.3 to 5.5	V
Input Terminal Voltage Analog Chip Microcontroller Chip	 $V_{IN(ANALOG)}$ $V_{IN(MCU)}$	 -0.3 to 5.5 V_{SS}-0.3 to V_{DD}+0.3	V
Maximum Microcontroller Current per Terminal All Terminals except VDD, VSS, PTA0:PTA4 PTA0:PTA4	 $I_{PIN(1)}$ $I_{PIN(2)}$	 ±15 ±25	mA
Maximum Microcontroller VSS Output Current	I_{MVSS}	100	mA
Maximum Microcontroller VDD Input Current	I_{MVDD}	100	mA
LIN Supply Voltage Normal Operation (Steady-State) Transient Input Voltage (per ISO7637 Specification) and with External Components (Figure 4, page 18)	 $V_{BUS(SS)}$ $V_{BUS(PK)}$	 -18 to 40 -150 to 100	V
ESD Voltage Human Body Model (2) H0 terminal Human Body Model (2) all other terminals Machine Model (3) Charge Device Model (4)	 V_{ESD1-1} V_{ESD1-2} V_{ESD2} V_{ESD3}	 ±1000 ±2000 ±200 ±750	V

Notes

1. Transient capability for pulses with a time of t < 0.5 sec.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
3. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
4. ESD3 testing is performed in accordance with Charge Device Model, Robotic (C_{ZAP} = 4.0 pF).

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any terminal may cause permanent damage to the device.

Rating	Symbol	Value	Unit
Thermal Ratings			
Operating Ambient Temperature (5)	T_A	-40 to 85	°C
Operating Junction Temperature (6)	T_J	-40 to 125	°C
Storage Temperature	T_{STG}	-40 to 150	°C
Peak Package Reflow Temperature During Solder Mounting (7)	T_{SOLDER}	245	°C

Notes

5. The limiting factor is junction temperature; taking into account the power dissipation, thermal resistance, and heat sinking.
6. The temperature of analog and MCU die is strongly linked via the package, but can differ in dynamic load conditions, usually because of higher power dissipation on the analog die. The analog die temperature must not exceed 150°C under these conditions.
7. Terminal soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage Range					
Nominal Operating Voltage	V_{SUP1}	9.0	—	16	V
Extended Operating Voltage (LIN only 8..18V)(9)	V_{SUP2}	7.5	—	20	V
Supply Current Range					
Normal Mode (9) V_{SUP} = 12 V, Analog Chip in Normal Mode (PSON=1), MCU Operating Using Internal Oscillator at 32 MHz (8.0 MHz Bus Frequency), SPI, ESCI, ADC Enabled	I_{RUN}	—	25	—	mA
Stop Mode (9), (10) V_{SUP} = 12 V, Voltage Regulator with limited current capability	I_{STOP}	—	40	50	µA
Sleep Mode (9), (10) V_{SUP} = 12 V, Voltage Regulator off	I_{SLEEP}	—	12	20	µA
Digital Interface Ratings (Analog Die)					
Output terminals $\overline{RST\_A}$, $\overline{IRQ\_A}$, RXD (MISO probe only)					V
Low-state Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	–	–	0.4	
High-state Output Voltage (I_{OUT} = 250 uA)	V_{OH}	3.85	–	–	
Output terminal RXD - Capacitance (11)	C_{OUT}	–	4.0	–	pF
Input terminals $\overline{RST\_A}$, PWM ($\overline{SS}$, MOSI, TXD probe only)					V
Input Logic Low Voltage	V_{IL}	–	–	1.5	
Input Logic High Voltage	V_{IH}	3.5	–	–	
Input terminals - Capacitance (11)	C_{IN}	–	4.0	–	pF
Terminals $\overline{IRQ\_A}$, $\overline{RST\_A}$ - Pullup Resistor	$R_{PULLUP1}$	–	10	–	kOhm
Terminals $\overline{SS}$ - Pullup Resistor	$R_{PULLUP2}$	–	100	–	kOhm
Terminals MOSI, SPSCK, PWM - Pull-down Resistor	$R_{PULLDOWN}$	–	100	–	kOhm
Terminal TXD - PULLup Current Source	I_{PULLUP}	–	35	–	µA

Notes

8. Device is fully functional, but some of the parameters might be out of spec.
9. Total current measured at GND terminals.
10. Stop and Sleep mode current will increase if V_{SUP} exceeds 15 V.
11. This parameter is guaranteed by process monitoring but is not production tested.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
System Resets and Interrupts					
Low Voltage Reset (LVR)					
Threshold	V_{LVRON}	3.8	4.2	4.65	V
Hysteresis	V_{LVR_HYS}	50	–	300	mV
Low Voltage Interrupt (LVI)					V
Threshold	V_{LVION}	6.0	–	7.5	
Hysteresis	V_{LVI_HYS}	0.3	–	0.8	
High Voltage Interrupt (HVI)					V
Threshold	V_{HVION}	20	–	24	
Hysteresis	V_{HVI_HYS}	0.5	–	1.5	
High Temperature Interrupt (HTI) (12)					°C
Threshold T_J	T_{ION}	125	–	150	
Hysteresis	T_{IH}	5.0	–	10.0	
High Temperature Reset (HTR) (12)					°C
Threshold T_J	T_{RON}	155	–	180	
Hysteresis	T_{IH}	5.0	–	10.0	
Voltage Regulator (13)					
Normal Mode Output Voltage (14)					V
I_{OUT} = 60 mA, 7.5V < V_{SUP} < 20V	V_{DDRUN1}	4.75	5.0	5.25	
I_{OUT} = 60 mA, V_{SUP} < 7.5V and V_{SUP} > 20V	V_{DDRUN2}	4.75	5.0	5.25	
Normal Mode Total Output Current	I_{OUTRUN}	–	120	150	mA
Load Regulation - I_{OUT} = 60 mA, V_{SUP} = 9V, T_J = 125°C	V_{LR}	–	–	100	mV
STOP Mode Output Voltage (14)	V_{DDSTOP}	4.75	5.0	5.25	V
STOP Mode Total Output Current	$I_{OUTSTOP}$	150	500	850	uA

Notes

12. This parameter is guaranteed by process monitoring but is not production tested.
13. Specification with external low ESR ceramic capacitor 1.0 µF< C < 4.7 µF and 200 mΩ ≤ ESR ≤ 10 Ω. Its not recommended to use capacitor values above 4.7 µF
14. When switching from Normal to Stop mode or from Stop mode to Normal mode, the output voltage can vary within the output voltage specification.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN Physical Layer					
LIN Transceiver Output Voltage					V
Recessive State, TXD HIGH, I_{OUT} = 1.0 µA	V_{LIN_REC}	V_{SUP}-1	—	—	
Dominant State, TXD LOW, 500 Ω External Pullup Resistor	V_{LIN_DOM}	—	—	1.4	
Normal Mode Pullup Resistor to VSUP	R_{PU}	20	30	47	kΩ
Stop, Sleep Mode Pullup Current Source	I_{PU}	—	20	—	µA
Output Current Shutdown Threshold	I_{BLIM}	100	230	280	mA
Output Current Shutdown Timing	I_{BLS}	5.0	–	40	µs
Leakage Current to GND					
V_{SUP} Disconnected, V_{BUS} at 18V	I_{BUS}	–	1.0	10	µA
Recessive state, 8V ≤ V_{SUP} ≤ 18V, 8V ≤ V_{BUS} ≤ 18V, V_{BUS} ≥ V_{SUP}	$I_{BUS-PAS-REC}$	0.0	3.0	20	µA
GND Disconnected, V_{GND} = V_{SUP}, V_{BUS} at -18V	$I_{BUS-NOGND}$	-1.0	–	1.0	mA
LIN Receiver					VSUP
Receiver Threshold Dominant	V_{BUS_DOM}	–	–	0.4	
Receiver Threshold Recessive	V_{BUS_REC}	0.6	–	–	
Receiver Threshold Center	V_{BUS_CNT}	0.475	0.5	0.525	
Receiver Threshold Hysteresis	V_{BUS_HYS}	–	–	0.175	

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
High-Side Output HS1					
Switch On Resistance T_J = 25°C, I_{LOAD} = 1.0 A	$R_{DS(ON)-HS1}$	–	185	225	mΩ
Overcurrent Shutdown	I_{HSOC1}	6.0	–	9.0	A
Overcurrent Shutdown blanking time (15)	t_{OCB}	–	4-8	–	µs
Current to Voltage Ratio (16) V_{ADOUT} [V] / I_{HS} [A], (measured and trimmed I_{HS} = 2 A)	$CR_{RATIOHS1}$	0.84	1.2	1.56	V/A
High-Side Switching Frequency (15)	f_{PWMHS}	–	–	25	kHz
High-Side Free-Wheeling Diode Forward Voltage T_J = 25°C, I_{LOAD} = 1 A	V_{HSF}	–	0.9	–	V
Leakage Current	I_{LeakHS}	–	<0.2	10	µA
High-Side Outputs HS2 and HS3(17)					
Switch On Resistance T_J = 25°C, I_{LOAD} = 1.0 A	$R_{DS(ON)-HS23}$	–	440	500	mΩ
Overcurrent Shutdown	I_{HSOC23}	3.6	–	5.6	A
Overcurrent Shutdown blanking time (15)	t_{OCB}	–	4-8	–	µs
Current to Voltage Ratio (16) V_{ADOUT} [V] / I_{HS} [A], (measured and trimmed I_{HS} = 2 A)	$CR_{RATIOHS23}$	1.16	1.66	2.16	V/A
High-Side Switching Frequency (15)	f_{PWMHS}	–	–	25	kHz
High-Side Free-Wheeling Diode Forward Voltage T_J = 25°C, I_{LOAD} = 1 A	V_{HSF}	–	0.9	–	V
Leakage Current	I_{LeakHS}	–	<0.2	10	µA

Notes

15. This parameter is guaranteed by process monitoring but is not production tested.
16. This parameter is guaranteed only if correct trimming was applied.
17. The high-side HS3 can be only used for resistive loads.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Half-Bridge Outputs HB1 and HB2					
Switch On Resistance	$R_{DS(ON)-HB12}$				mΩ
High-Side, T_J = 25°C, I_{LOAD} = 1.0 A		–	750	900	
Low-Side, T_J = 25°C, I_{LOAD} = 1.0 A		–	750	900	
Overcurrent Shutdown	I_{HBOC12}				A
High-Side		1.0	–	1.5	
Low-Side		1.0	–	1.5	
Overcurrent Shutdown blanking time (18)	t_{OCB}	–	4-8	–	µs
Switching Frequency (18)	f_{PWM}	–	–	25	kHz
Free-Wheeling Diode Forward Voltage					V
High-Side, T_J = 25°C, I_{LOAD} = 1.0 A	V_{HSF}	–	0.9	–	
Low-Side, T_J = 25°C, I_{LOAD} = 1.0 A	V_{LSF}	–	0.9	–	
Leakage Current	I_{LeakHB}	–	<0.2	10	µA
Low-Side Current to Voltage Ratio (19)	$CR_{RATIOHB12}$				V/A
V_{ADOUT} [V] / I_{HB} [A], CSA = 1, (measured and trimmed I_{HS} = 200 mA)		17.5	25.0	32.5	
V_{ADOUT} [V] / I_{HB} [A], CSA = 0, (measured and trimmed I_{HS} = 500 mA)		3.5	5.0	6.5	
Half-Bridge Outputs HB3 and HB4					
Switch On Resistance	$R_{DS(ON)-HB34}$				mΩ
High-Side, T_J = 25°C, I_{LOAD} = 1.0 A		–	275	325	
Low-Side, T_J = 25°C, I_{LOAD} = 1.0 A		–	275	325	
Overcurrent Shutdown	I_{HBOC34}				A
High-Side		4.8	–	7.2	
Low-Side		4.8	–	7.2	
Overcurrent Shutdown blanking time (18)	t_{OCB}	–	4-8	–	µs
Switching Frequency (18)	f_{PWM}	–	–	25	kHz
Free-Wheeling Diode Forward Voltage					V
High-Side, T_J = 25°C, I_{LOAD} = 1.0 A	V_{HSF}	–	0.9	–	
Low-Side, T_J = 25°C, I_{LOAD} = 1.0 A	V_{LSF}	–	0.9	–	
Leakage Current	I_{LeakHB}	–	<0.2	10	µA
Low-Side Current to Voltage Ratio (19)	$CR_{RATIOHB34}$				V/A
V_{ADOUT} [V] / I_{HB} [A], CSA = 1, (measured and trimmed I_{HS} = 500 mA)		3.5	5.0	6.5	
V_{ADOUT} [V] / I_{HB} [A], CSA = 0, (measured and trimmed I_{HS} = 2 A)		0.7	1.0	1.3	

Notes

18. This parameter is guaranteed by process monitoring but is not production tested.
19. This parameter is guaranteed only if correct trimming was applied

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
EC Outputs EC and ECR					
Switch On Resistance					
T1 measured on ECR Terminal, T_J = 25°C, I_{LOAD} = 100 mA	$R_{DS(ON)T1}$	–	1.0	1.2	Ω
T2 measured on EC Terminal, T_J = 25°C, I_{LOAD} = 100 mA	$R_{DS(ON)T2}$	–	400	600	mΩ
Overcurrent Shutdown					A
T1 (short to GND)	I_{T1OC}	0.6	–	1.0	
T2 (short to VSUP)	I_{T2OC}	0.6	–	1.0	
Open Load Detection (Bit ECOLT is set) set @min output load	R_{OC}	–	10	–	kΩ
DAC resolution (from 0V to 1.4V)	EC_{DACRES}	–	6.0	–	Bit
Regulated Output Voltage (@ I = 1mA)	VEC_{REG}	0.18	–	1.4	V
Switchable V_{DD} Output HVDD					
Overcurrent Shutdown	I_{HVDDOC}	25	35	50	mA
Overcurrent Shutdown Blanking Time (20)	$t_{HVDDOCB}$				µs
HVDDT1:0 = 00		–	950	–	
HVDDT1:0 = 01		–	536	–	
HVDDT1:0 = 10		–	234	–	
HVDDT1:0 = 11		–	78	–	
Overcurrent Flag Delay (20)	$t_{HVDDOCFD}$	–	0.5	–	ms
Drop-Out Voltage @ I_{LOAD} = 20 mA	$V_{HVDDDROP}$	–	110	300	mV
V_{SUP} Down Scaler (21)					
Voltage Ratio ($RATIO_{VSUP}$ = V_{SUP} / V_{ADOUT})	$RATIO_{VSUP}$	4.75	5.0	5.25	–
Internal Die Temperature Sensor (21)					
Voltage / Temperature Slope (20)	S_{TtoV}	–	26	–	mV/°C
Output Voltage @25°C	V_{T25}	1.7	1.9	2.1	V

Notes

20. This parameter is guaranteed by process monitoring but is not production tested.
21. This parameter is guaranteed only if correct trimming was applied

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Hall-Effect Sensor Input H0 - General Purpose Input Mode (H0MS = 0)					
Input Voltage Low Threshold	V_{LT}	–	–	1.5	V
Input Voltage High Threshold	V_{HT}	3.5	–	–	V
Input Voltage Hysteresis	V_{HH}	100	–	500	mV
Pullup resistor	R_{PH}	7.0	10	13	kΩ
Hall-Effect Sensor Input H0 - 2pin Hall Sensor Input Mode (H0MS = 1)					
Output Voltage V_{SUP} < 17V V_{SUP} >17V	 V_{HALL1} V_{HALL2}	 – –	 V_{SUP}-1.2 –	 – 15.8	V
Output Drop @ I_{OUT} = 15mA	V_{H0D}	–	–	2.5	V
Sense Current Threshold	I_{HSCT}	6.0	7.9	10	mA
Sense Current Hysteresis	I_{HSCH}	800	1100	1650	µA
Sense Current Limitation	V_{HSCLIM}	20	40	70	mA
Analog Input A0, A0CST					
Current Source A0, A0CST (22) (23) CSSEL1:0 = 00 CSSEL1:0 = 01 CSSEL1:0 = 10 CSSEL1:0 = 11	 I_{CS1} I_{CS2} I_{CS3} I_{CS4}	 – – – –	 40 120 320 800	 – – – –	µA
Wake-Up Input L0					
Input Voltage Threshold Low	V_{LT}	–	–	1.5	V
Input Voltage Threshold High	V_{HT}	3.5	–	–	V
Input Voltage Hysteresis	V_{LH}	0.5	–	–	V
Input Current	I_N	-10	–	10	µA
Wake-Up Filter Time (24)	t_{WUP}	–	20	–	µs

Notes

22. This parameter is guaranteed only if correct trimming was applied
23. The current values are optimized to read a NTC temperature sensor, e.g. EPCOS type B57861 (R25 = 3000Ω, R/T characteristic 8016)
24. This parameter is guaranteed by process monitoring but is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN Physical Layer					
Driver Characteristics for Normal Slew Rate (25), (26)					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	50	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	50	µs
Duty Cycle 1: D1 = $t_{Bus\_rec(min)}$ / (2 x t_{BIT}), t_{BIT} = 50 µs, V_{SUP} = 7.0V..18V	D1	0.396	–	–	
Duty Cycle 2: D2 = $t_{Bus\_rec(max)}$ / (2 x t_{BIT}), t_{BIT} = 50 µs, V_{SUP} = 7.6V..18V	D2	–	–	0.581	
Driver Characteristics for Slow Slew Rate (25), (27)					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	100	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	100	µs
Duty Cycle 3: D3 = $t_{Bus\_rec(min)}$ / (2 x t_{BIT}), t_{BIT} = 96 µs, V_{SUP} = 7.0V..18V	D3	0.417	–	–	
Duty Cycle4: D4 = $t_{Bus\_rec(max)}$ / (2 x t_{BIT}), t_{BIT} = 96 µs, V_{SUP} = 7.6V..18V	D4	–	–	0.590	
Driver Characteristics for Fast Slew Rate					
LIN High Slew Rate (Programming Mode)	SR_{FAST}	—	20	—	V/µs
Receiver Characteristics and Wake-Up Timings					
Receiver Dominant Propagation Delay (28)	t_{RL}	—	3.5	6.0	µs
Receiver Recessive Propagation Delay (28)	t_{RH}	—	3.5	6.0	µs
Receiver Propagation Delay Symmetry	t_{R-SYM}	-2.0	—	2.0	µs
Bus Wake-Up Deglitcher	t_{PROPWL}	30	50	150	µs
Bus Wake-Up Event Reported (29)	t_{WAKE}	—	20	—	µs

Notes

25. V_{SUP} from 7.0 V to 18 V, bus load R0 and C0 1.0 nF/1.0 kΩ, 6.8 nF/660 Ω, 10 nF/500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter.
26. See Figure 6, page 18.
27. See Figure 7, page 19.
28. Measured between LIN signal threshold V_{IL} or V_{IH} and 50% of RXD signal.
29. t_{WAKE} is typically 2 internal clock cycles after LIN rising edge detected. See Figure 9 and Figure 8, page 19. In Sleep mode the V_{DD} rise time is strongly dependent upon the decoupling capacitor at VDD terminal.

Table 4. Dynamic Electrical Characteristics (continued)

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI Interface Timing					
SPI Operating Recommended Frequency (30)	f_{SPIOP}	0.25	—	4.0	MHz
State Machine					
Reset Low-Level Duration after VDD High	t_{RST}	0.8	1.25	1.94	ms
Normal Request Time-out	$t_{NORMREQ}$	51	80	124	ms
Window Watchdog Timer (31)					
Watchdog Period (WDP1:0 = 00)	t_{WD80}	52	80	124	ms
Watchdog Period (WDP1:0 = 01)	t_{WD40}	26	40	62	ms
Watchdog Period (WDP1:0 = 10)	t_{WD20}	13	20	31	ms
Watchdog Period (WDP1:0 = 11)	t_{WD10}	6.5	10	15.5	ms

Notes

30. This parameter is guaranteed by process monitoring but is not production tested.
31. This parameter is guaranteed only if correct trimming was applied. Additionally See Watchdog Period Range Value (AWD Trim) on page 51

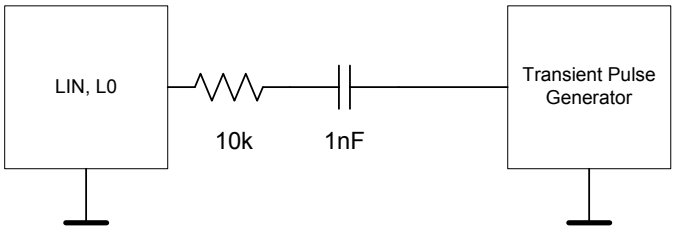
MICROCONTROLLER PARAMETRICS

Table 5. Microcontroller

For a detailed microcontroller description, refer to the MC68HC908EY16 datasheet.

Module	Description
Core	High Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz
Timer	Two 16-Bit Timers with 2 Channels (TIM A and TIM B)
Flash	16 K Bytes
RAM	512 Bytes
ADC	10-Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud-Rate Adjustment
ICG	Internal Clock Generation Module

TIMING DIAGRAMS



Note: Waveform in accordance to ISO7637 part 1, test pulses 1, 2, 3a and 3b.

Figure 4. Test Circuit for Transient Test Pulses

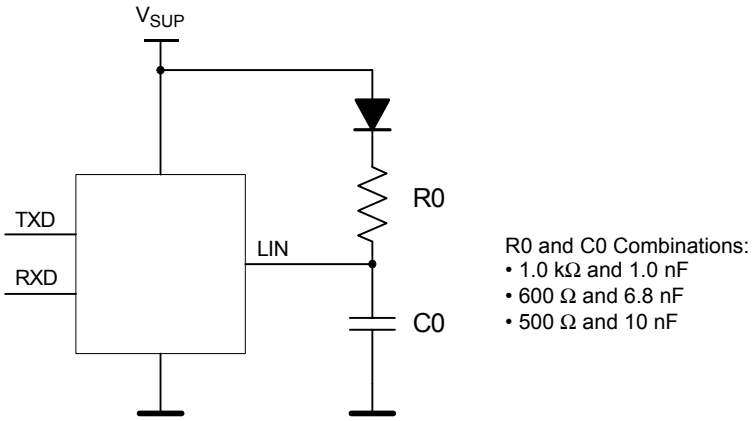


Figure 5. Test Circuit for LIN Timing Measurements

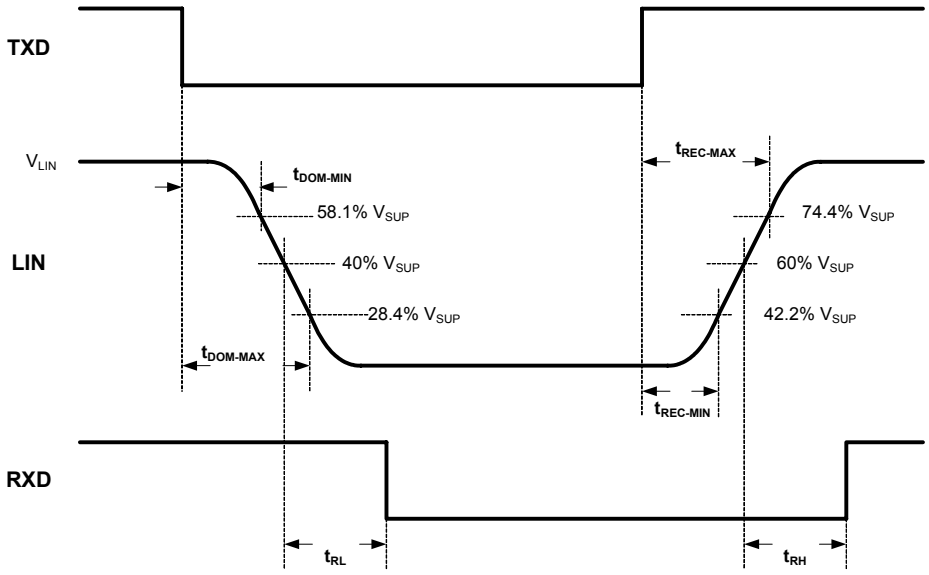


Figure 6. LIN Timing Measurements for Normal Slew Rate

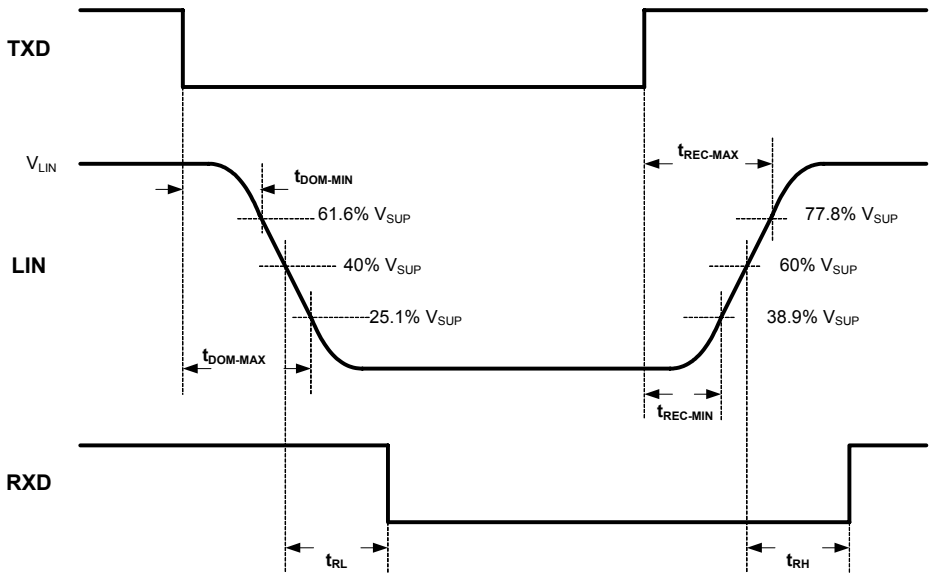


Figure 7. LIN Timing Measurements for Slow Slew Rate

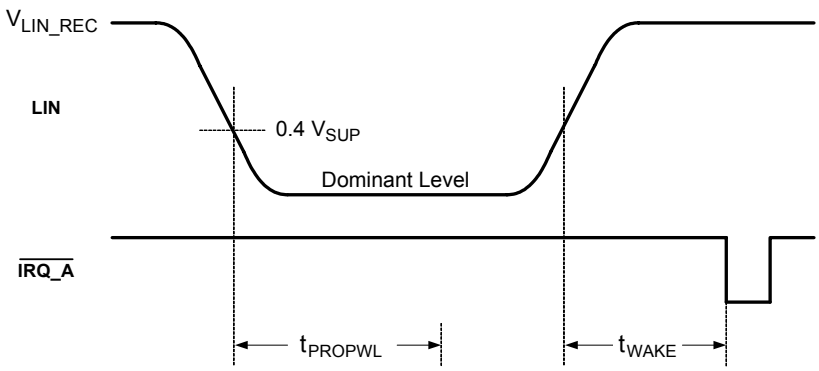


Figure 8. Wake-Up Stop Mode Timing

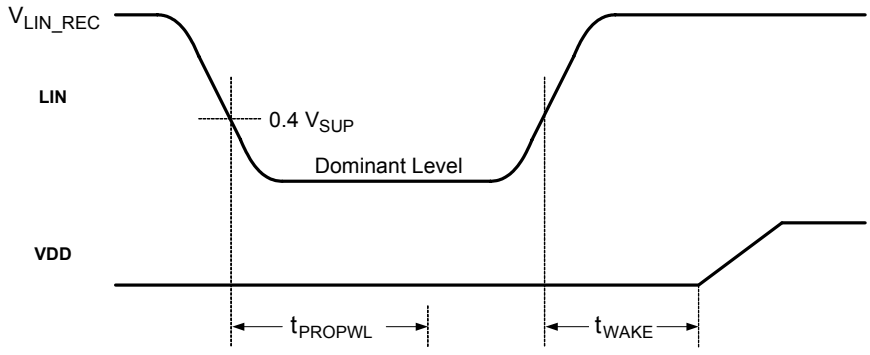


Figure 9. Wake-Up Sleep Mode Timing

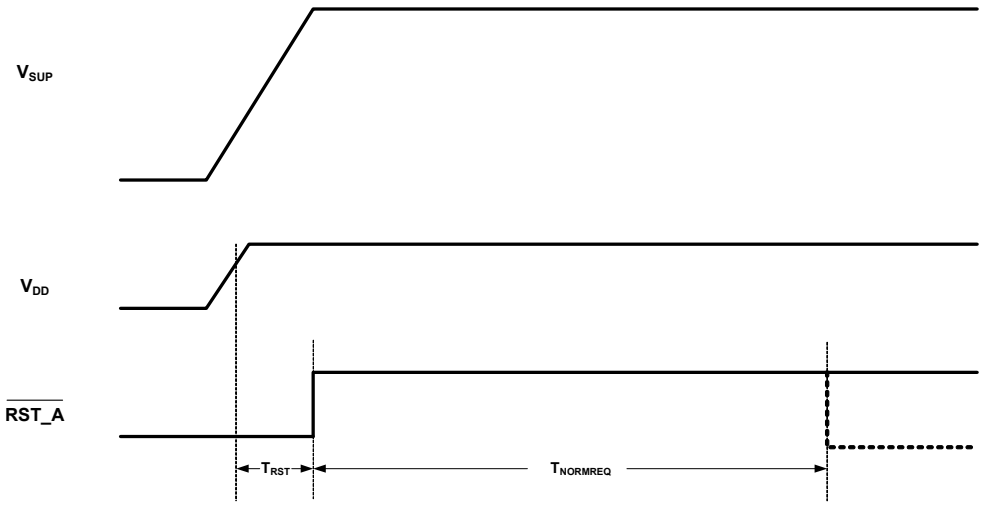


Figure 10. Power On Reset and Normal Request Time-out Timing

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 908E622 was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E622 is well suited to perform complete mirror control via a three-wire LIN bus.

This device combines an HC908EY16 MCU core with flash memory together with a *SmartMOS* IC chip. The *SmartMOS* IC chip combines power and control in one chip. Power switches are provided on the *SmartMOS* IC configured as half-bridge outputs and three high-side switches. Other ports are also provided, which include a circuitry for EC-glass control, one Hall-effect sensor input port, one analog input port with a switched current source, one wake-up terminal, and a selectable HVDD terminal. An internal voltage regulator provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with three-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

FUNCTIONAL TERMINAL DESCRIPTION

See Figure 2, 908E622 Simplified Internal Block Diagram, page 2, for a graphic representation of the various terminals referred to in the following paragraphs. Also, see the terminal diagram on page 3 for a depiction of the terminal locations on the package.

PORT A I/O TERMINALS

These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt terminals, KBD0:KBD4.

The PTA5/SPSCK terminal is not accessible in this device and is internally connected to the SPI clock terminal of the analog die.

The PTA6/$\overline{SS}$ terminal is not accessible in this device and is internally connected to the SPI slave select input of the analog die.

For details refer to the 68HC908EY16 datasheet.

PORT B I/O TERMINALS

These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU. All terminals are shared with the ADC module.

PTB0/AD0 is internally connected to the ADOUT terminal of the analog die, allowing diagnostic measurements to be calculated; e.g., current recopy, V_{SUP}, etc.

The PTB1/AD1, PTB2/AD2, PTB6/AD6/TBCH0, PTB7/AD7/TBCH1 terminals are not accessible in this device.

For details refer to the 68HC908EY16 datasheet.

PORT C I/O TERMINALS

These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device and are internally connected to the MISO and MOSI SPI terminals of the analog die.

For details refer to the 68HC908EY16 datasheet.

PORT D I/O TERMINALS

PTD0/TACH0/BEMF and PTD1/TACH1 are special-function, bidirectional I/O port terminals that can also be programmed to be timer terminals.

PTD0/TACH0 terminal is internally connected to the PWM input of the analog die and only accessible for test purposes (can not be used in the application).

For details refer to the 68HC908EY16 datasheet.

PORT E I/O TERMINAL

PTE0/TXD and PTE1/RXD are special-function, bidirectional I/O port terminals that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD terminal of the analog die. The connection for the receiver must be done externally.

PTE1/RXD is internally connected to the RXD terminal of the analog die and only accessible for test purposes (can not be used in the application).

For details refer to the 68HC908EY16 datasheet.

EXTERNAL INTERRUPT TERMINAL ($\overline{IRQ}$)

The $\overline{IRQ}$ terminal is an asynchronous external interrupt terminal. This terminal contains an internal pullup resistor that is always activated, even when the $\overline{IRQ}$ terminal is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

EXTERNAL RESET TERMINAL ($\overline{RST}$)

A logic [0] on the $\overline{RST}$ terminal forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven LOW when any internal reset source is asserted.

This terminal contains an internal pullup resistor that is always activated, even when the reset terminal is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

POWER SUPPLY TERMINALS (VSUP1:VSUP8)

VSUP1:VSUP8 are device power supply terminals. The nominal input voltage is designed for operation from 12 V systems. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high-side output drivers, multiple VSUP terminals are provided.

All VSUP terminals must be connected to get full chip functionality.

POWER GROUND TERMINALS (GND1:GND4)

GND1:GND4 are device power ground connections. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high-side output drivers, multiple terminals are provided.

GND1 and GND2 terminals must be connected to get full chip functionality.

HALF-BRIDGE OUTPUT TERMINALS (HB1:HB4)

The 908E622 device includes power MOSFETs configured as four half-bridge driver outputs. The HB3:HB4 have a lower $R_{DS(ON)}$, to run higher currents (e.g. fold motor), than the HB1:B2 outputs.

The HB1:HB4 outputs are short-circuit and overtemperature protected, and they feature current recopy. Over current protection is done on both high-side and low-side FET's. The current recopy are done on the low-side MOSFETs.

HIGH-SIDE OUTPUT TERMINALS (HS1:HS3)

The HS output terminals are a low $R_{DS(ON)}$ high-side switches. Each HS switch is protected against overtemperature and overcurrent. The output is capable of limiting the inrush current with an automatic PWM or feature a real PWM capability using the PWM input.

The HS1 has a lower $R_{DS(ON)}$, to run higher currents (e.g. heater), than the HS2 and HS3 outputs.

For the HS1 two terminals (HS1a:HS1b) are necessary for the current capability and have to be connected externally.

Important: The HS3 can be only used to drive resistive loads.

EC GLASS TERMINALS (ECR, EC)

These terminals are used to drive the electrochrome function on EC glass mirrors. The ECR terminal is used to connect an external ballast resistor. The EC terminal provides the mirror with an regulated output voltage up to 1.4V. The output voltage can be selected by an integrated DA converter.

HALL-EFFECT SENSOR INPUT TERMINAL (H0)

The Hall-effect sensor input terminal H0 provides an input for Hall-effect sensors (2pin or 3pin) or a switch.

ANALOG INPUT TERMINALS (A0, A0CST)

These terminals are analog inputs with selectable current source values. The A0CST is intent to trim the A0 input.

WAKE-UP INPUT TERMINAL (L0)

This terminal is 40V rated input. It can be used as wake-up source for a system wake-up. The input is falling or rising edge sensitive.

Important: If unused this terminal should be connected to VSUP or GND to avoid parasitic transitions. In Low Power Mode this could lead to random wake-up events.

SWITCHABLE V_{DD} OUTPUT TERMINAL (HVDD)

The HVDD terminal is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; e.g., 3-terminal Hall-effect sensors or potentiometers. The output is short-circuit protected.

LIN BUS TERMINAL (LIN)

The LIN terminal represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

+5.0 V VOLTAGE REGULATOR OUTPUT TERMINAL (VDD)

The VDD terminal is needed to place an external capacitor to stabilize the regulated output voltage. The VDD terminal is intended to supply the embedded microcontroller.

Important The VDD terminal should not be used to supply other loads; use the HVDD terminal for this purpose. The VDD, EVDD and VDDA/VREFH terminals must be connected together.

VOLTAGE REGULATOR GROUND TERMINAL (VSS)

The VSS terminal is the ground terminal for the connection of all non-power ground connections (microcontroller and sensors). **Important** VSS, EVSS and VSSA/VREFL terminals must be connected together.

RESET TERMINAL ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the bidirectional reset terminal of the analog die. It is an open drain with pullup resistor and must be connected to the $\overline{\text{RST}}$ terminal of the MCU.

INTERRUPT TERMINAL ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output terminal of the analog die indicating errors or wake-up events. It is an open drain with pullup resistor and must be connected to the $\overline{\text{IRQ}}$ terminal of the MCU.

ADC SUPPLY/REFERENCE TERMINALS (VDDA/ VREFH AND VSSA/VREFL)

VDDA and VSSA are the power supply terminals for the analog-to-digital converter (ADC).

VREFH and VREFL are the reference voltage terminals for the ADC.

The supply and reference signals are internally connected.

It is recommended that a high quality ceramic decoupling capacitor be placed between these terminals.

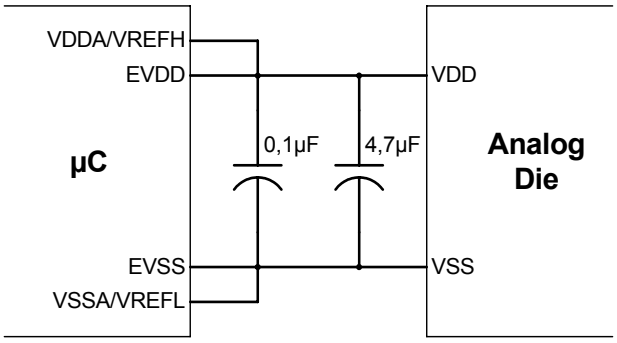
For details refer to the 68HC908EY16 datasheet.

MCU POWER SUPPLY TERMINALS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground terminals. The MCU operates from a single power supply.

Fast signal transitions on MCU terminals place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details refer to the 68HC908EY16 datasheet.



TEST MODE TERMINAL (TESTMODE)

This terminal is for test purpose only. In the application this terminal has to be forced to GND.

For Programming/Test this terminal has to be forced to VDD to bring the analog die into Test mode. In Test mode the Reset Time-out (80ms) is disabled and the LIN receiver is disabled

NOTE: After detecting a RESET (internal or external) the PSON bit needs to be set within 80ms. If not the device will automatically enter sleep mode.

MCU TEST TERMINAL (FLSVPP)

This terminal is for test purposes only. This terminal should be either left open (not connected) or can be connected to GND.

EXPOSED PAD TERMINAL

The exposed pad terminal on the bottom side of the package conducts heat from the chip to the PCB board. For thermal performance the pad must be soldered to the PCB board. It is recommended that the pad be connected to the ground potential.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

908E622 ANALOG DIE MODES OF OPERATION

The 908E622 offers three operating modes: Normal (Run), Stop, and Sleep. In Normal mode the device is active and is operating under normal application conditions. The Stop and Sleep modes are low power modes with wake-up capabilities. The different modes can be selected by the STOP and SLEEP bits in the System Control Register.

Figure 11 describes how transitions are done between the different operating modes and Table 6, page 26, gives an overview of the operating modes.

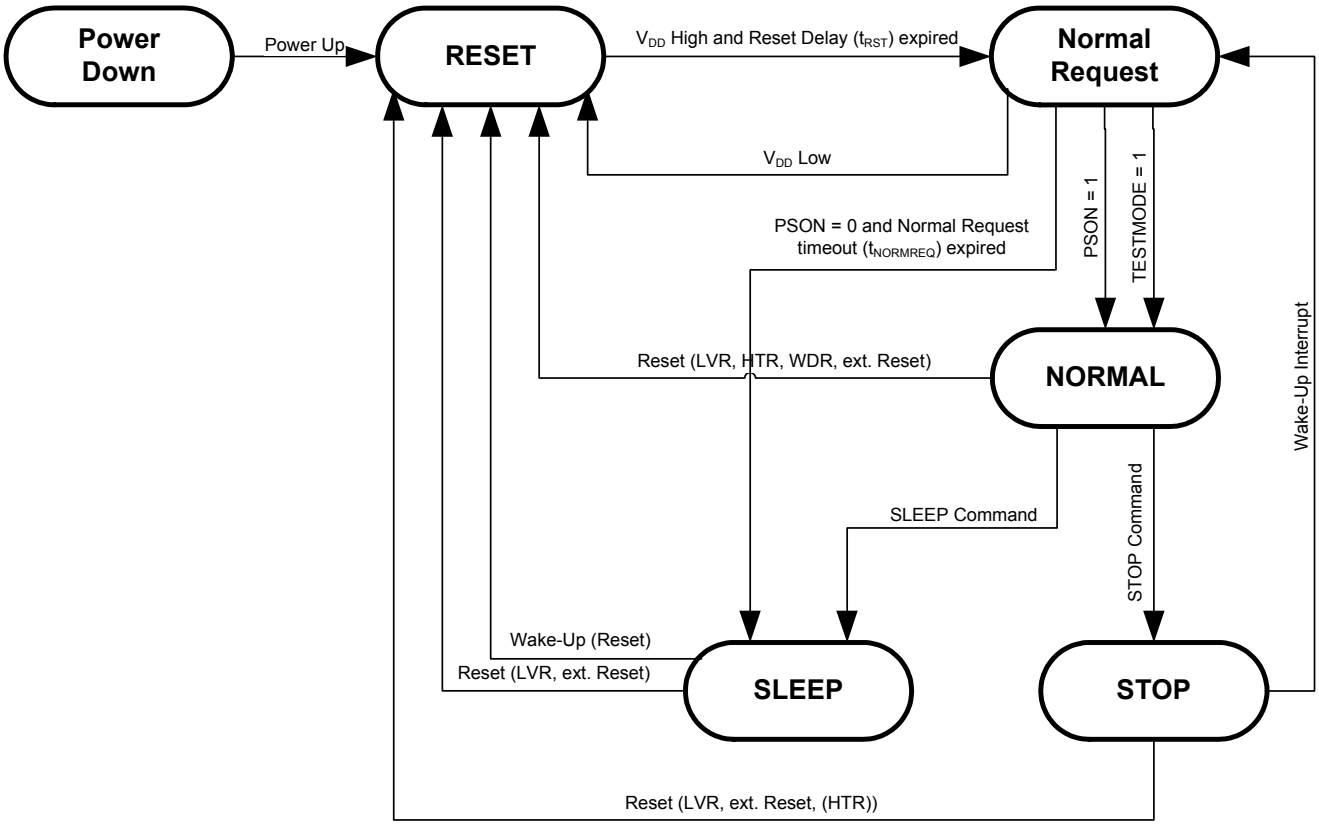


Figure 11. Operating Modes and Transitions

Normal Mode

This Mode is normal operating mode of the device, all functions and power stages are active and can be enabled/ disabled. The voltage regulator provides the +5V V_{DD} to the MCU.

After a reset (e.g. Power On Reset, Wake-Up from Sleep) the MCU has to set the PSON bit in the System Control Register within 80ms typical ($t_{NORMREQ}$), this is to ensure the MCU has started up and is operating correctly. If the PSON bit is not set within the required time frame the device is entering SLEEP mode to reduce power consumption (fail safe).

This MCU monitoring can be disabled e.g. for programming by applying V_{DD} on the TESTMODE terminal.

Stop Mode

In Stop mode the voltage regulator still supplies the MCU with V_{DD} (limited current capability). To enter the Stop mode the STOP bit in the System Control Register has to be set and the MCU has to be stopped also (see 908EY16 datasheet for details).

Wake-up from this mode is possible by LIN bus activity or the wake-up input L0 and is maskable with the LINIE and/or L0IE bits in the Interrupt Mask Register. The analog die is generating an interrupt on $\overline{\text{IRQ\_A}}$ terminal to wake-up the MCU. The wake-up / interrupt source can be evaluated with the L0IF and LINIF bits in the Interrupt Flag Register.

Stop mode has a higher current consumption than Sleep mode, but allows a quicker wake-up. Additionally the wake-

up sources can be selected (maskable) which is not possible in Sleep mode.

Figure 12 show the procedure to enter the Stop mode and how the system is waking up.

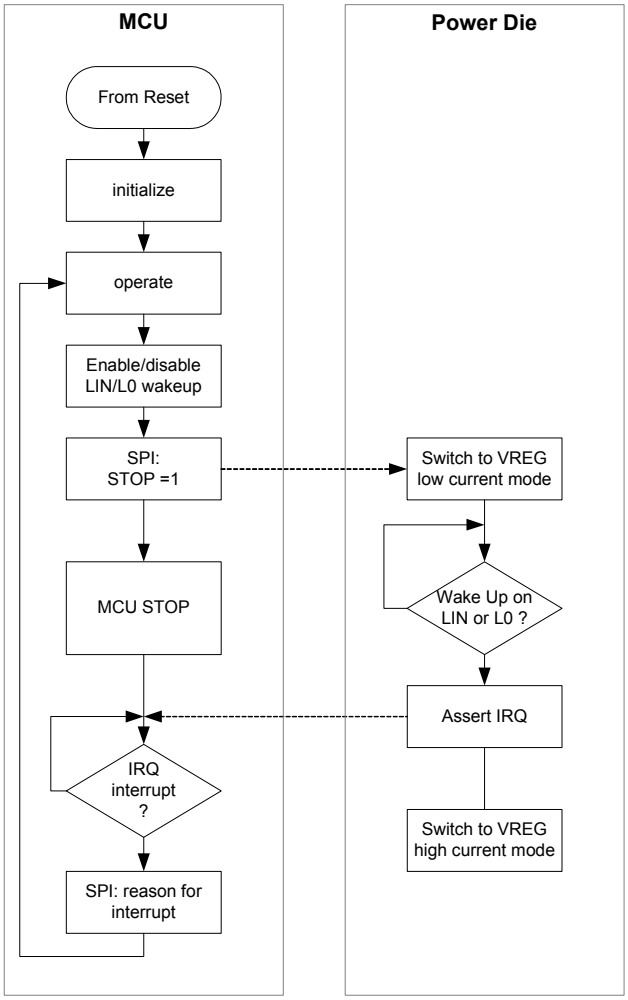


Figure 12. STOP mode Wake-up Procedure

Sleep Mode

In Sleep mode the voltage regulator is turned off and the MCU is not supplied (V_{DD} = 0 V) also the $\overline{RST\_A}$ terminal is pulled low.

To enter the Sleep mode the Sleep bit in the System Control Register has to be set.

Wake-up from this mode is possible by LIN bus activity or the wake-up input L0 and is not maskable. The wake-up behaves like a power on reset. The wake-up / reset source can be evaluated by the L0WF and/or LINWF bits in the Reset Status Register.

Sleep mode has a lower current consumption than Stop mode, but requires a longer time to wake-up. The wake-up sources can not be selected (not maskable).

Figure 13 show the procedure to enter the Sleep mode and how a wake-up is performed.

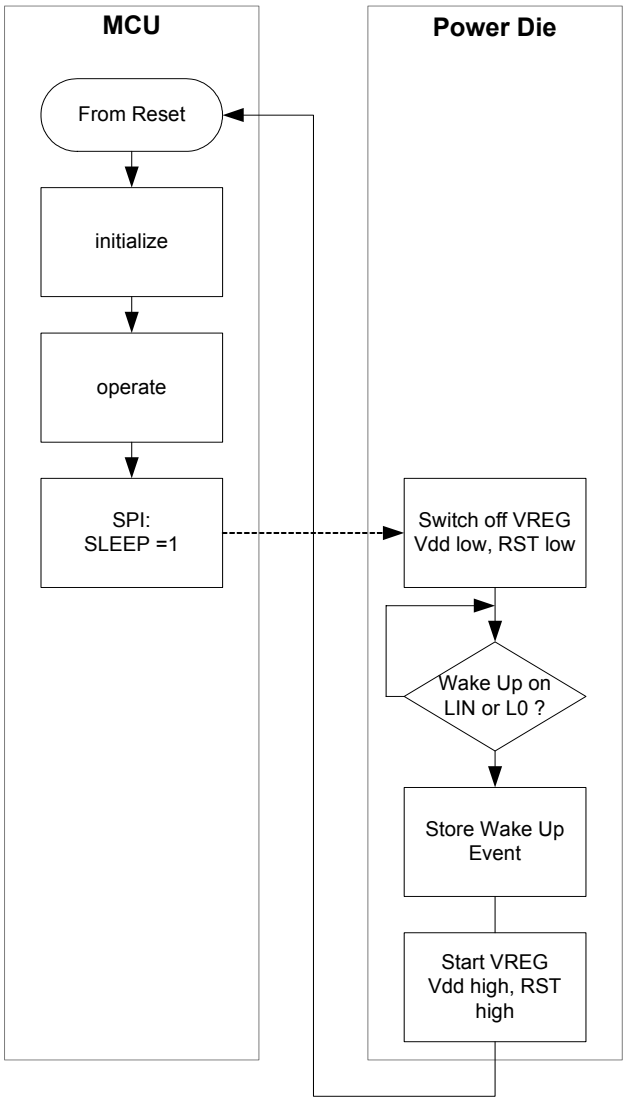


Figure 13. SLEEP mode Wake-up Procedure

Table 6 summarized the Operating modes.

Table 6. Operating Modes Overview

Device Mode	Voltage Regulator	Wake-Up Capabilities	$\overline{\text{RST\_A}}$ Output	MCU monitoring/ Watchdog Function	Power Stages	LIN Interface
Reset	V_{DD} ON	N/A	LOW	Disabled	Disabled	Disabled
Normal Request	V_{DD} ON	N/A	HIGH	$t_{NORMREQ}$ (80 ms typical) time out to set PSON bit in System Control Register	Disabled	Disabled
Normal (Run)	V_{DD} ON	N/A	HIGH	Window Watchdog active if enabled	Enabled	Enabled
Stop	V_{DD} ON with limited current capability	LIN wake-up, L0 state change (SPI PSON=1)(1)	HIGH	Disabled	Disabled	Recessive state with wake-up capability
Sleep	V_{DD} OFF	LIN wake-up L0 state change	LOW	Disabled	Disabled	Recessive state with wake-up capability

Notes
1. The SPI is still active in Stop mode. However, due to the limited current capability of the voltage regulator in Stop mode, the PSON bit has to be set before the increased current caused from a running MCU causes an LVR.

OPERATING MODES OF THE MCU

For a detailed description of the operating modes of the MCU, refer to the MC68HC908EY16 datasheet.

INTERRUPTS

The 908E622 has seven different interrupt sources. An interrupt pulse on the $\overline{\text{IRQ\_A}}$ terminal is generated to report an event or fault to the MCU. All interrupts are maskable and can be enabled/disabled via the SPI (Interrupt Mask Register). After reset all interrupts are automatically disabled.

Low Voltage Interrupt

Low voltage interrupt (LVI) is related to external supply voltage VSUP. If this voltage falls below the LVI threshold, it will set the LVIF bit in the Interrupt Flag Register. In case the low voltage interrupt is enabled (LVIE = 1), an interrupt will be initiated.

During Sleep and Stop mode the low voltage interrupt circuitry is disabled.

High Voltage Interrupt

The High voltage Interrupt (HVI) is related to the external supply voltage VSUP. If this voltage rises above the HVI threshold it will set the HVIF bit in the Interrupt Flag Register. In case the High voltage Interrupt is enabled (HVIE = 1), an interrupt will be initiated.

During Stop and Sleep mode the HVI circuitry is disabled.

High Temperature Interrupt

The high temperature interrupt (HTI) is generated by the on chip temperature sensors. If the chip temperature is above the HTI threshold the HTIF bit in the Interrupt Flag Register will be set. In case the high temperature interrupt is enabled (HTIE = 1), an interrupt will be initiated.

During Stop and Sleep mode the HTI circuitry is disabled.

LIN Interrupt

The LIN Interrupt is related to the Stop mode. If the LIN interrupt is enabled (LINIE = 1) in Stop mode an interrupt is asserted, if a rising edge is detected and the bus was dominant longer than T_{propWL}. After the wake-up / interrupt the LINIF is indicating the reason for the wake-up / interrupt.

Power Stage Fail Interrupt

The power stage fail flag indicates an error condition on any of the power stages (see Figure 14, page 27).

In case the power stage fail interrupt is enabled (PSFIE = 1), an interrupt will be initiated if:

During Stop and Sleep mode the PSFI circuitry is disabled.

HO Input Interrupt

The H0 interrupt flag H0IF is set in run mode by a state change of the H0F flag (rising or falling edge on the enabled

input). The interrupt function is available if the input is selected as General Purpose or as 2pin Hallsensor input. The interrupt is maskable with the H0IE bit in the Interrupt Mask Register.

During Stop and Sleep mode the H0I circuitry is disabled.

L0 input Interrupt

The L0 interrupt flag L0IF is set in run mode by a state change of the L0F flag (rising or falling edge). The interrupt is maskable with the L0IE bit in the interrupt mask register.

INTERRUPT FLAG REGISTER (IFR)

Register Name and Address: IFR - $0A

	Bit7	6	5	4	3	2	1	Bit0
Read	L0IF	H0IF	LINIF	0	HTIF	LVIF	HVIF	PSFIF
Write								
Reset	0	0	0	0	0	0	0	0

L0IF - L0 Input Flag Bit

This read/write flag is set on a falling or rising edge at the L0 input. Clear L0IF by writing a logic [1] to L0IF.
Reset clears the L0IF bit. Writing a logic [0] to L0IF has no effect.

1 = rising or falling edge on L0 input detected
0 = no state change on L0 input detected

H0IF - H0 Input Flag Bit

This read/write flag is set on a falling or rising edge at the H0 input. Clear H0IF by writing a logic [1] to H0IF.
Reset clears the H0IF bit. Writing a logic [0] to H0IF has no effect.

1 = state change on the hallflags detected
0 = no state change on the hallflags detected

LINIF - LIN Flag Bit

This read/write flag is set if a rising edge is detected and the bus was dominant longer than TpropWL. Clear LINIF by writing a logic [1] to LINIF. Reset clears the LINIF bit. Writing a logic [0] to LINIF has no effect.

1 = LIN bus interrupt has occurred
0 = not LIN bus interrupt occurred since last clear

HTIF - High Temperature Flag Bit

This read/write flag is set on high temperature condition. Clear HTIF by writing a logic [1] to HTIF. If high temperature condition is still present while writing a logical one to HTIF, the writing has no effect. Therefore, a high temperature interrupt cannot be lost due to inadvertent clearing of HTIF.
Reset clears the HTIF bit. Writing a logic [0] to HTIF has no effect.

1 = high temperature condition has occurred
0 = high temperature condition has not occurred

LVIF - Low Voltage Flag Bit

This read/write flag is set on low voltage condition. Clear LVIF by writing a logic [1] to LVIF. If low voltage condition is still present while writing a logical one to LVIF, the writing has no effect. Therefore, a low voltage interrupt cannot be lost due to inadvertent clearing of LVIF.
Reset clears the LVIF bit. Writing a logic [0] to LVIF has no effect.

1 = low voltage condition has occurred
0 = low voltage condition has not occurred

HVIF - High Voltage Flag Bit

This read/write flag is set on high voltage condition. Clear HVIF by writing a logic [1] to HVIF. If high voltage condition is still present while writing a logical one to HVIF, the writing has no effect. Therefore, a high voltage interrupt cannot be lost due to inadvertent clearing of HVIF.
Reset clears the HVIF bit. Writing a logic [0] to HVIF has no effect.

1 = high voltage condition has occurred
0 = high voltage condition has not occurred

PSFIF - Power Stage Fail Bit

This read-only flag is set on a fail condition on one of the power outputs (HBx, HSx, HVDD, EC, H0). Reset clears the PSFIF bit. Clear this flag, by writing a logic [1] to the appropriate fail flag.

1 = power stage fail condition has occurred
0 = power stage fail condition has not occurred

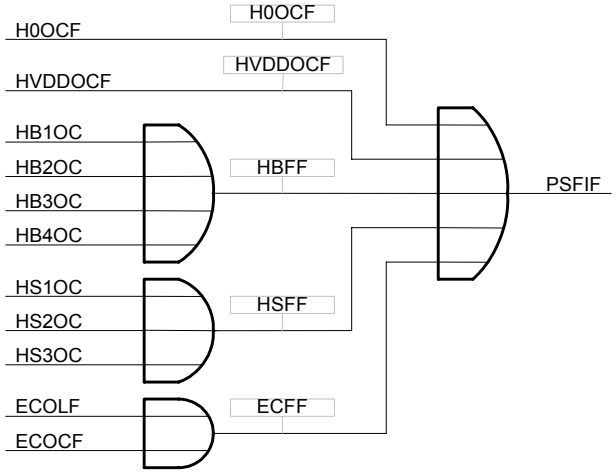


Figure 14. Principal Implementation of the PSFIF

INTERRUPT MASK REGISTER (IMR)

Register Name and Address: IMR - $09

	Bit7	6	5	4	3	2	1	Bit0
Read Write	L0IE	H0IE	LINIE	HTRD	HTIE	LVIE	HVIE	PSFIE
Reset	0	0	0	0	0	0	0	0

L0IE - L0 Input Interrupt Enable Bit

This read/write bit enables CPU interrupts by the L0 flag, L0IF. Reset clears the L0IE bit.

1 = interrupt requests from L0IF flag enabled
0 = interrupt requests from L0IF flag disabled

H0IE - H0 Input Interrupt Enable Bit

This read/write bit enables CPU interrupts by the Hallport flag, H0IF. Reset clears the H0IE bit.

1 = interrupt requests from H0IF flag enabled
0 = interrupt requests from H0IF flag disabled

LINIE - LIN line Interrupt Enable Bit

This read/write bit enables CPU interrupts by the LIN flag, LINIF. Reset clears the LINIE bit.

1 = interrupt requests from LINIF flag enabled
0 = interrupt requests from LINIF flag disabled

HTRD - High Temperature Reset Disable Bit

This read/write bit disables the high temperature reset function. Reset clears the HTRD bit.

1 = high temperature reset is disabled
0 = high temperature reset is enabled

Note: Disabling of the high temperature reset can lead to a destruction of the part in cases of high temperature. This bit was foreseen for test purposes only!!!!!

HTIE - High Temperature Interrupt Enable Bit

This read/write bit enables CPU interrupts by the high temperature flag, HTIF. Reset clears the HTIE bit.

1 = interrupt requests from HTIF flag enabled
0 = interrupt requests from HTIF flag disabled

LVIE - Low Voltage Interrupt Enable Bit

This read/write bit enables CPU interrupts by the low voltage flag, LVIF.Reset clears the LVIE bit.

1 = interrupt requests from LVIF flag enabled
0 = interrupt requests from LVIF flag disabled

HVIE - High Voltage Interrupt Enable Bit

This read/write bit enables CPU interrupts by the high voltage flag, HVIF.Reset clears the HVIE bit.

1 = interrupt requests from HVIF flag enabled
0 = interrupt requests from HVIF flag disabled

PSFIE - Power Stage Fail Interrupt Enable Bit

This read/write bit enables CPU interrupts by power stage fail flag, PSFIF. Reset clears the PSFIE bit.

1 = interrupt requests from PSFIF flag enabled
0 = interrupt requests from PSFIF flag disabled

RESETS

The 908E622 has four internal and one external reset source.

Each internal reset event will cause a reset pin low for t_{RST} (1.25 ms typical), after the reset event is gone.

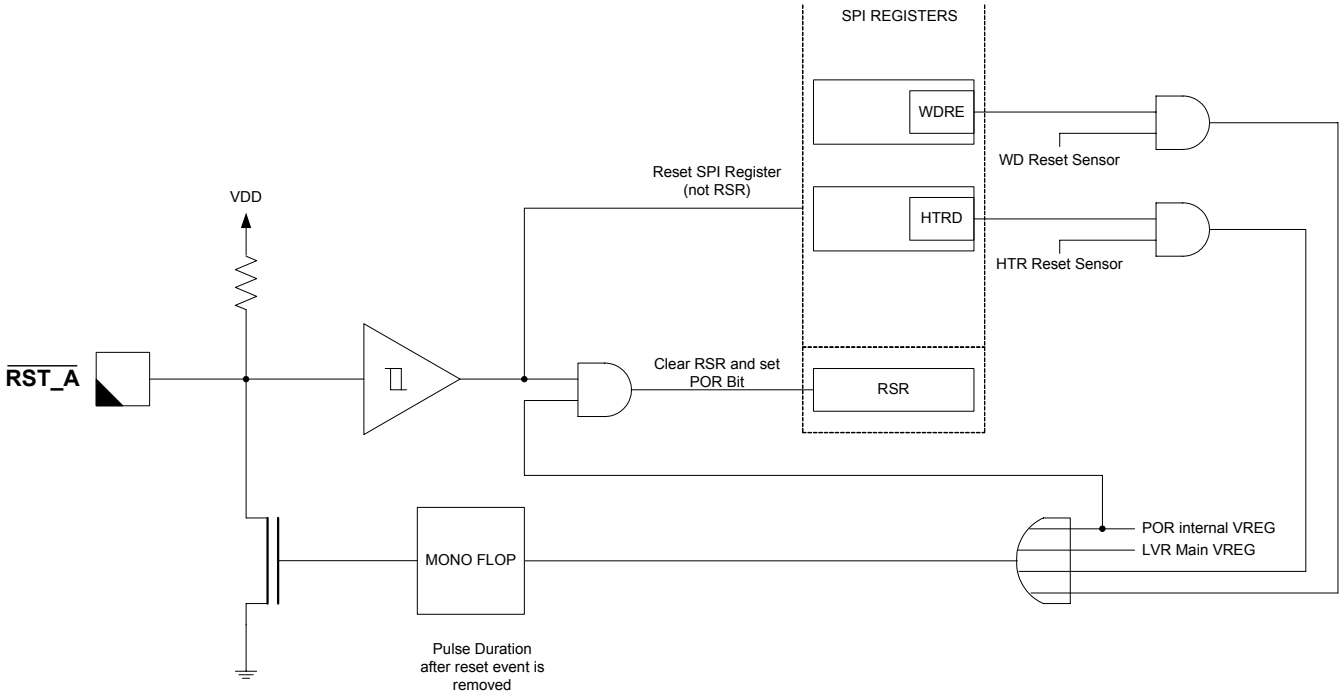


Figure 15. Internal Reset Routing

RESET SOURCE

High Temperature Reset

The device is protected against high temperature. When the chip temperature exceeds a certain temperature, a reset (HTR) is generated. The reset is flagged by bit HTR in the Interrupt Flag Register. A HTR event will reset all registers in the SPI excluding the RSR.

The HTR can be disabled by bit HTRD in the Interrupt Mask register.

Note: Disabling the high temperature reset can lead to destruction of the part in cases of high temperature. This bit was foreseen for test purposes only!

Watchdog Reset

The WatchDog module generates a reset, because of a watchdog time-out or wrong watchdog timer reset. Reset is flagged by bit WDR in the Reset Status Register. A Watchdog reset event will reset all registers in the SPI excluding the RSR.

Main VREG Low Voltage Reset

The LVR is related to the Main VDD. In case the voltage falls below a certain threshold, it will pull down the $\overline{\text{RST\_A}}$ terminal. Reset is flagged by bit LVR in the Reset Status Register. A LVR event will reset all register in the SPI excluding the RSR.

Power On Reset

The POR is related to the internal 5V supply. In case the device detects a power on the POR bit in the Reset Status Register (RSR) is set. A power on reset will reset all register in the SPI including the RSR and set the POR bit.

The Power On Reset circuitry will force the $\overline{\text{RST\_A}}$ terminal low for $t_{\overline{RST}}$ after the V_{DD} has reached its nominal value (above LVR Threshold). Also see Figure 10, page 20).

Reset terminal / external Reset

An external reset can be applied by pulling down the $\overline{\text{RST\_A}}$ terminal. The reset event is flagged by bit PINR in the reset status register.

Reset Status Register

This register contains five flags that shows the source of the last reset. A power-on reset sets the POR bit and clears all other bits in the Reset Status Register. All bits can be cleared by writing a one to the corresponding bit. Uncleared bits remain set as long as they are not cleared by a power-on reset or by software.

In addition the register includes two flags which will indicate the source of a wake-up from Sleep mode: Either LIN bus activity or an event on the L0 wake-up input terminal.

Register Name and Address: RSR - $0D

	Bit7	6	5	4	3	2	1	Bit0
Read	POR	PINR	WDR	HTR	LVR	0	LINWF	LOWF
Write								
POR	1	0	0	0	0	0	0	0

POR— Power On Reset bit

This read/write bit is set after power on. Bit is cleared by writing a logic “1” to this location.

1 = Reset due to power on
0 = no power on reset

PINR— Reset forced from external Reset terminal bit

This read/write bit is set after an reset was forced on the external reset RST_A terminal. Bit is cleared by writing an logic “1” to this location.

1 = reset source is external reset terminal
0 = no external reset

WDR— Watch Dog Reset bit

This read/write flag is set due to watchdog time-out or wrong watchdog timer reset. Clear WDR by writing a logic “1” to WDR.

1 = reset source is watchdog
0 = no watchdog reset

HTR— High Temperature Reset bit

This read/write bit is set if the chip temperature exceeds a certain value. Bit is cleared by writing a logic “1” to this location.

1 = reset due to high temperature condition
0 = no high temperature reset

LVR— Low Voltage Reset bit

This read/write bit is set if the external VDD voltage coming from the main voltage regulator falls below a certain value. Bit is cleared by writing a logic “1” to this location.

1 = reset due to low voltage condition
0 = no low voltage reset

LINWF— LIN Wake-Up Flag

This read/write bit is set if a bus activity was the case of an wake-up. Bit is cleared by writing a logic “1” to this location.

1 = Wake-up due to bus activity
0 = no wake-up due to bus activity

L0WF— L0 Wake-Up Flag

This read/write bit is set if a event on the L0 terminal caused an wake-up. Bit is cleared by writing a logic “1” to this location.

1 = Wake-Up due to L0 terminal
0 = no Wake-Up due to L0 terminal

ANALOG DIE INPUTS/OUTPUTS

LIN PHYSICAL LAYER

The LIN bus terminal provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification.

The LIN driver is a low-side MOSFET with internal current limitation and thermal shutdown. An internal pullup resistor with a serial diode structure is integrated, so no external pullup components are required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slew rate controls is guaranteed.

The slew rate can be selected for optimized operation at 10 and 20kBit/s as well as high baud rates for test and programming. The slew rate can be adapted with 2 bits SRS[1:0] in the System Control Register. The initial slew rate is optimized for 20kBit/s.

The LIN terminal offers high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

The LIN transmitter circuitry is enabled by setting the PSON bit in the System Control Register (SYSCTL).

If the transmitter works in the current limitation region, the LINCL bit in the System Status Register (SYSSTAT) is set and the LIN transceiver is disabled after a certain time.

For improved performance and safe behavior in case of LIN bus short to Ground or LIN bus leakage during low power mode the internal pull-up resistor on the LIN terminal is disconnected from VSUP and a small current source keeps the LIN bus at recessive level. In case of a LIN bus short to GND, this feature will reduce the current consumption in STOP and SLEEP modes.

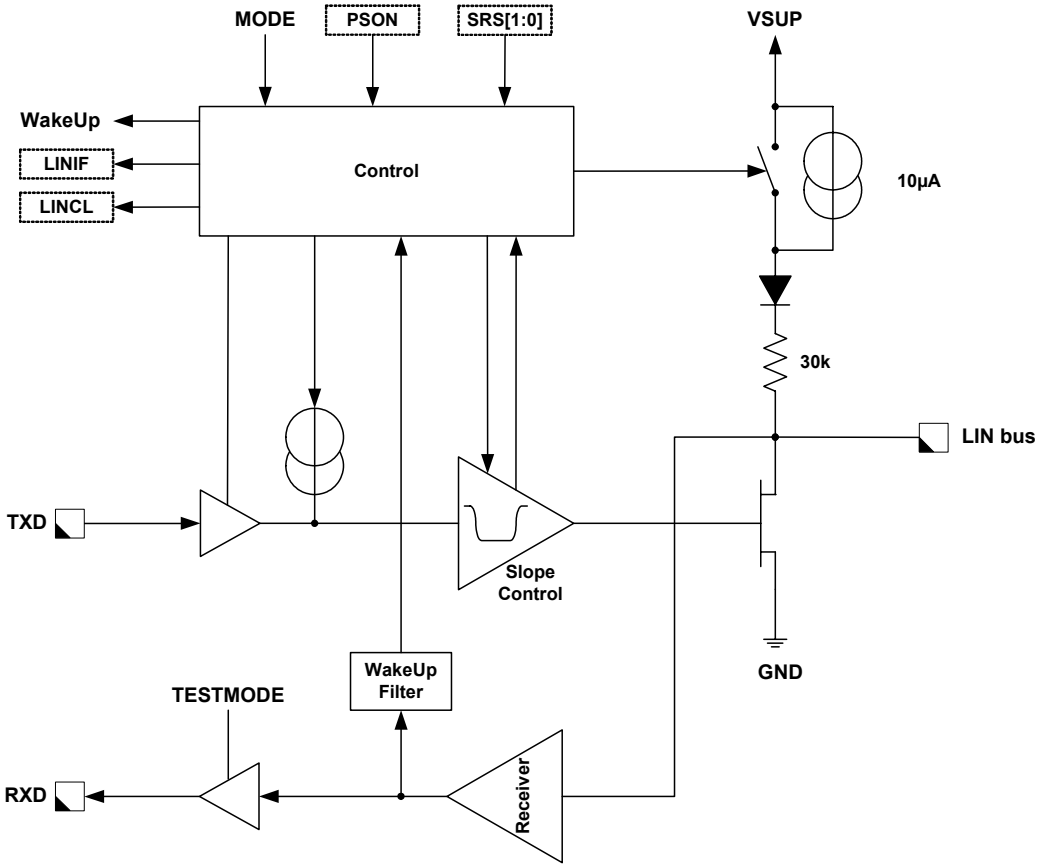


Figure 16. LIN Interface

TXD Terminal

The TXD terminal is the MCU interface to control the state of the LIN transmitter (see Figure 2, page 2). When TXD is LOW, the LIN terminal is low (dominant state). When TXD is HIGH, the LIN output MOSFET is turned off (recessive state). The TXD terminal has an internal pullup current source in order to set the LIN bus to recessive state in the event, for instance, the microcontroller could not control it during system power-up or power-down.

RXD Terminal

The RXD transceiver terminal is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive state) is reported by a high level on RXD, LIN LOW (dominant state) by a low level on RXD.

STOP Mode and Wake-up Feature

During STOP mode operation the transmitter of the physical layer is disabled and the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN terminal in recessive state. The receiver is still active and able to detect wake-up events on the LIN bus line.

If the LIN interrupt is enabled (LINIE bit in the Interrupt Mask register is set), a dominant level longer than T_{propWL} followed by an rising edge will set the LINIF flag and generate an interrupt which causes a system wake-up (see Figure 8, page 19)

SLEEP Mode and Wake-up Feature

During SLEEP mode operation the transmitter of the physical layer is disabled and the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN terminal in recessive state. The receiver is still active to be able to detect wake-up events on the LIN bus line.

A dominant level longer than T_{propWL} followed by an rising edge will generate a system wake-up (reset) and set the LINWF flag in the Reset Status register (RSR). Also see Figure 9, page 19).

A0 INPUT AND ANALOG MULTIPLEXER

A0 - Analog Input

Input A0 is an analog input used for reading switches or as analog inputs for potentiometers, NTC, etc.

A0 is internally connected to the analog multiplexer. This terminal offers a switchable current source. To read the Analog Input the terminal has to be selected with the SS[3:0] bits in the A0MUCTL register.

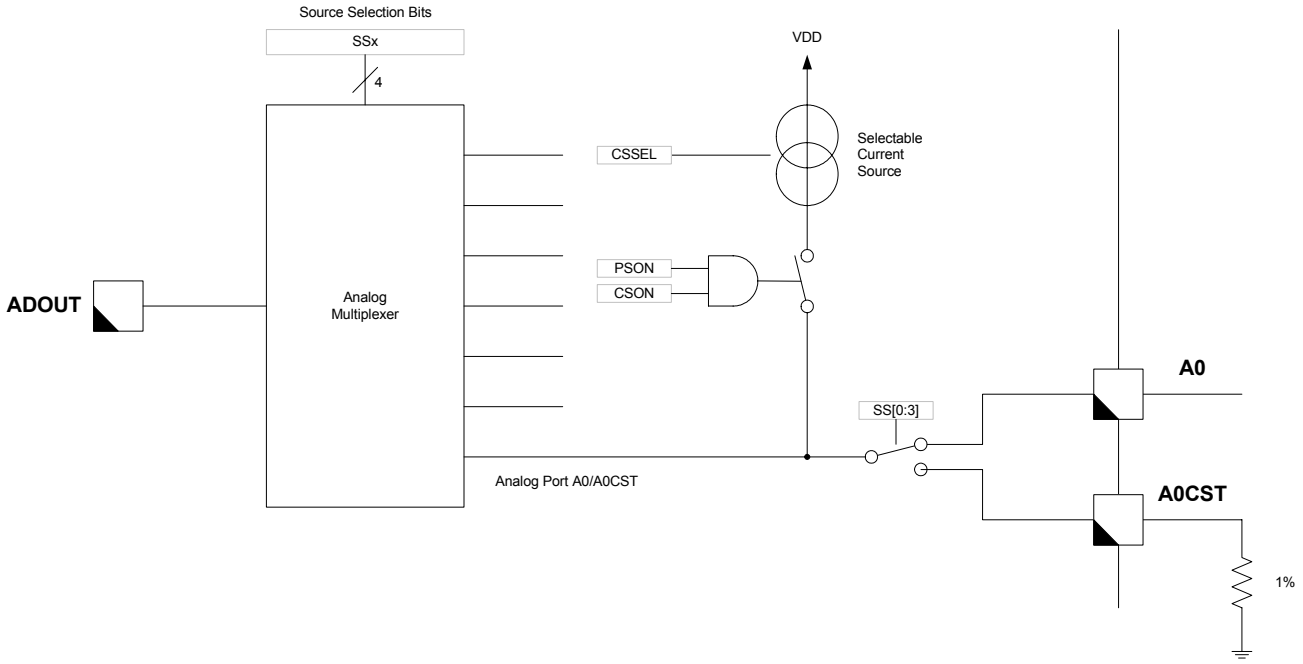


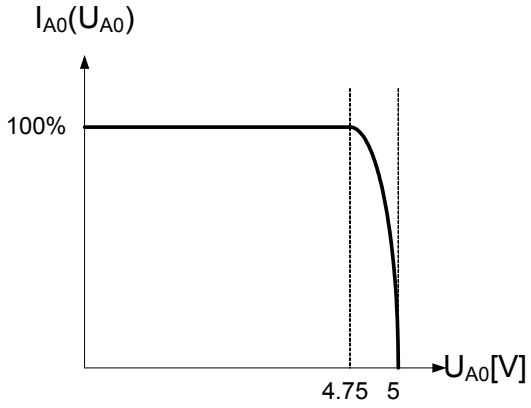
Figure 17. Analog Input and Multiplexer

A0 Current Source

The terminal A0 provides a switchable current source, to be able to read in switches, NTC, etc. without the need of an additional supply line for the sensor. The overall enable of this feature is done by setting the PSON bit in the System Control register. In addition the terminal has to be selected with the SS[3:0] bits. The current source can be enabled with Bit CSON and adjusted with the bits CSSEL[1:0].

With the CSSEL[1:0] bit's four different current values can be selected (40, 120, 320 and 800µA). This function is ceased during STOP and SLEEP mode operation.

The current source is derived from the Vdd voltage and is constant up to an output voltage of ~4.75V.



To calibrate the current sources an extra terminal (A0CST) is foreseen. On this terminal an accurate resistor can to be connected. Switching the current sources to this resistor allows the user to measure the current and use the measured value for calculating the current on A0.

Analog Multiplexer / ADOUT terminal

The ADOUT terminal is the analog output interface to the Analog-to-digital converter of the MCU. To be able to have different sources for the MCU with one single signal an

analog multiplexer is integrated in the analog die. This multiplexer has twelve different sources, which can be selected with the SS[3:0] bits in the A0MUCTL register.

Half-bridge (HB1:HB4) Current Recopy

The multiplexer is connected to the four current sense circuits on the low side FET of the half bridges. This sense circuits offers a voltage proportional to the current through the MOSFET. The resolution is depending on bit CSA in the A0 and Multiplexer control register (A0MUCTL).

High-side (HS1:HS3) Current Recopy

The multiplexer is connected to the three high-side switches. This sense circuits offers a voltage proportional to the current through the transistor.

Analog Input A0 and A0CST

A0 and A0CST are directly connected to the analog multiplexer. It offers the possibility to read analog values from the periphery.

Temperature Sensor

The analog die includes an on chip temperature sensor. This sensor offers a voltage which is proportional to the actual mean chip junction temperature.

VSUP prescaler

The VSUP prescaler offers a possibility to measure the external supply voltage. The output of this voltage is VSUP / RATIOVSUP.

EC Output

The EC output is directly connected to the multiplexer to be able to read the actual voltage on the EC terminal.

A0 and Multiplexer Control Register (A0MUCTL)

Register Name and Address: A0MUCTL - $08

	Bit7	6	5	4	3	2	1	Bit0
Read Write	CSON	CSSEL 1	CSSEL 0	CSA	SS3	SS2	SS1	SS0
Reset	0	0	0	0	0	0	0	0

CSON — Current Source on/off

This read/write bit enables the current source for the A0 or A0CST inputs
Reset clears CSON bit.
1 = Current Source enabled
0 = Current Source disabled

CSSEL[1:0] — Current Source Select Bits

These read/write bits select the current source values for A0 or A0CST input.
Reset clears CSSEL[1:0] bits.

Table 7. A0 Current Source Level Selection Bits

CSSEL1	CSSEL0	Current Source Enable (typ.)
0	0	40µA
0	1	120µA
1	0	320µA
1	1	800µA

CSA — H-Bridges Current Sense Amplification Select Bit

This read/write bit selects the current sense amplification of the H-Bridges HB1:HB4 current recopy.
Reset clears the CSA bit.
1 = low current sense amplification
0 = high current sense amplification

SS[3:0] — Analog Source Input Select Bits

These read/write bits selects the analog input source for the ADOUT terminal.
Reset clears the SS[3:0] bits

Table 8. Analog Multiplexer Configuration Bits.

SS3	SS2	SS1	SS0	Channel
0	0	0	0	current recopy HB1
0	0	0	1	current recopy HB2
0	0	1	0	current recopy HB3
0	0	1	1	current recopy HB4
0	1	0	0	current recopy HS1
0	1	0	1	current recopy HS2
0	1	1	0	current recopy HS3
0	1	1	1	not used
1	0	0	0	Chip temperature
1	0	0	1	VSUP prescaler
1	0	1	0	Terminal A0
1	0	1	1	Terminal A0CST
1	1	0	0	Terminal EC
1	1	0	1	not used
1	1	1	0	not used
1	1	1	1	not used

Hall-Effect Sensor Input Terminal H0

The H0 terminal can be configured as general purpose input (H0MS = 0) or as hall-effect sensor input (H0MS = 1) to be able to read 3pin / 2pin hall sensors or switches.

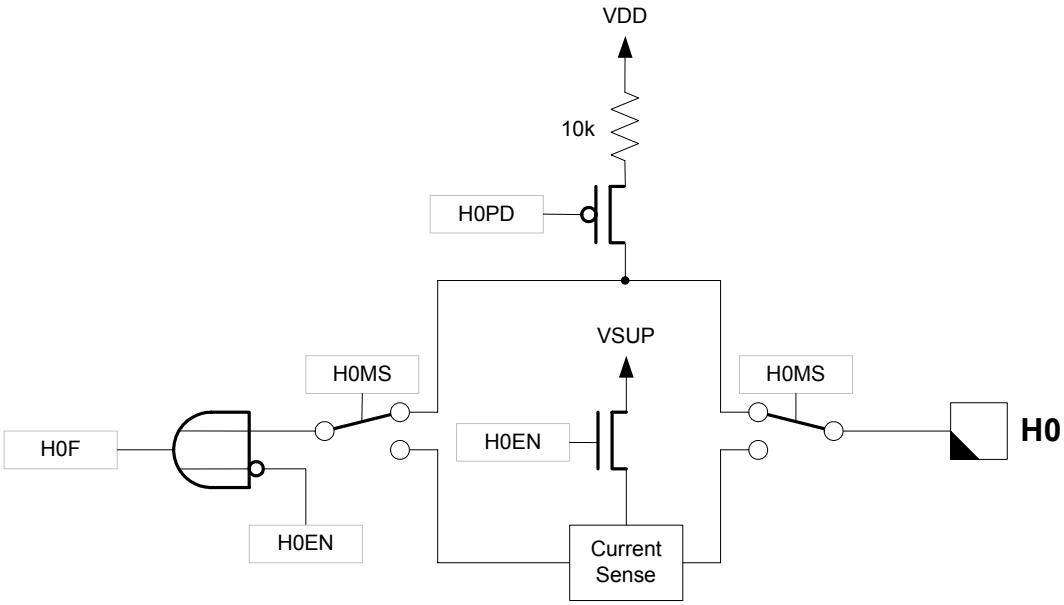


Figure 18. General purpose / hall-effect sensor input (H0)

Current Coded Hallsensor Input

H0 is selected as “2 pin hallsensor input”, if the corresponding H0MS bit in the H0/L0 Status and Control Register (HLSCTL) is set. In this mode the terminal current to GND is monitored by a special sense circuitry. Setting bit H0EN in the H0/L0 Status and Control Register switches the output to VSUP and enable the sense circuitry. The result of the sense operation is given by the H0F flag. The flag is low if the sensed current is higher than the sense current threshold I_{HSCT}. In this configuration the HO terminal is protected (current limitation) against short circuit to GND.

After switching on the hallport (H0EN = “1”) the hallsensor needs some time to stabilize the output. In RUN mode the software has to take care about waiting for a few µs (40) before sensing the hallflags.

The hallport output current is sensed. In case of an overcurrent (short to GND) the hallport overcurrent flag (H0OCF) is set and the current is limited. For proper operation of the current limitation an external capacitor (>100nF) close to the H0 terminal is required.

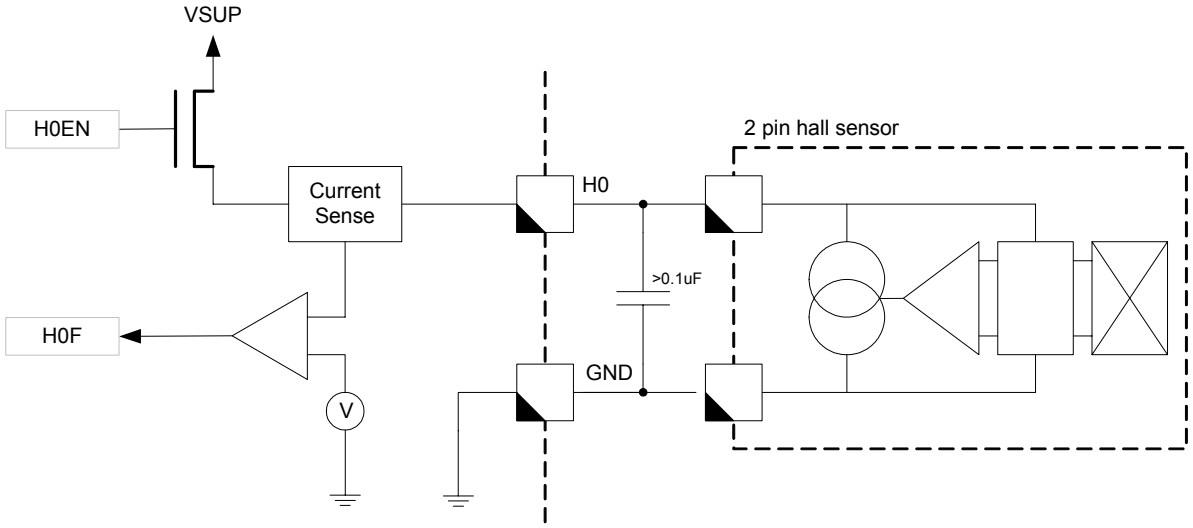


Figure 19. H0 used as 2-pin hallsensor input

General Purpose Input

H0 is selected as general purpose input, if the H0MS bit in the H0/L0 Status and Control Register (HLSCTL) is cleared. In this mode the input is usable as standard 5V input. The H0 input has a selectable internal pull-up resistors. The pull-up can be switched off with the H0PD bit in the H0/L0 Status and Control Register (HLSCTL). After reset the internal pull-up is enabled.

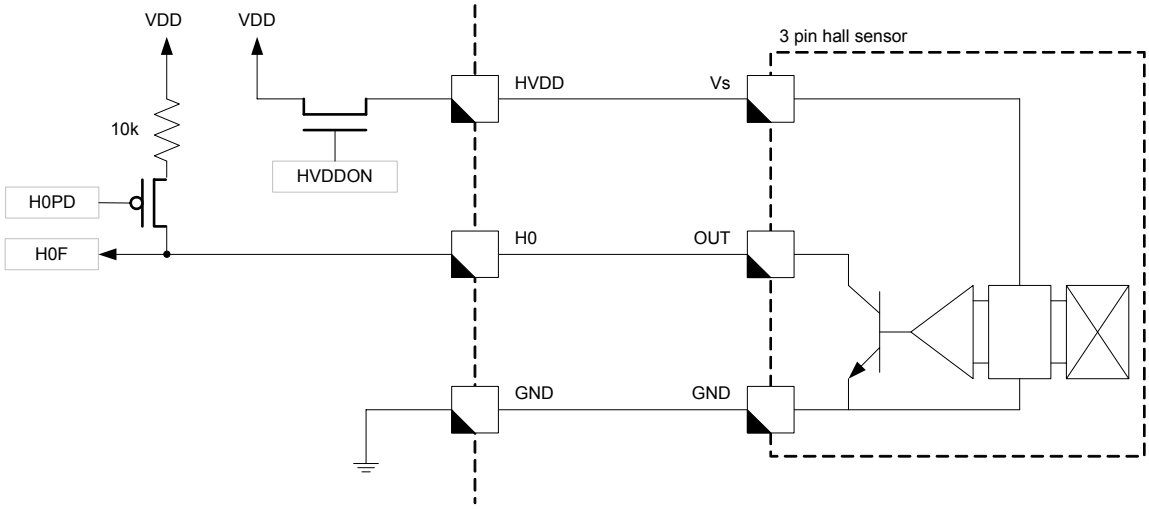


Figure 20. H0 used as 3 pin hall-effect sensor input

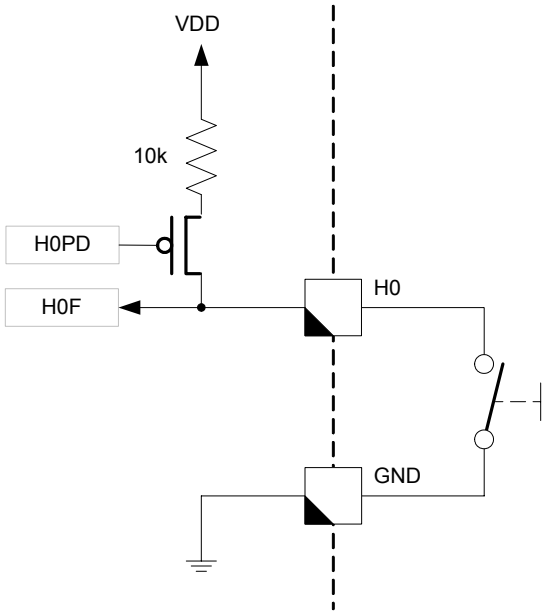


Figure 21. H0 used to read in standard switches

H0 Interrupt

The interrupt functionality on this terminal is just available in RUN mode. H0 interrupt flag H0IF is set in run mode by a state change of the H0 flag (rising or falling edge on the enabled input). The interrupt function is available if the input is selected as General Purpose or as 2pin Hallsensor input. The interrupt can be masked with the H0IE bit in the interrupt mask register.

Wake-up input L0

The device provides one wake-up capable input for reading VSUP or VDD related signals.

RUN mode

The actual input state is reflected in bit L0F of the H0/L0 Status and Control register (HLSCTL).

The L0 terminal offers an interrupt capability on rising and falling edge. The interrupt can be enabled with the L0IE bit in the Interrupt Mask register.

STOP/SLEEP mode

During STOP and SLEEP mode the terminal can be used to wake-up the device.

Before entering the STOP or SLEEP mode the actual state of the input is stored. If the state is changing during in the STOP or SLEEP mode a wake-up is initiated.

H0 / L0 Status and Control Register (HLSCTL)

Register Name and Address: HLSCTL - $07

	Bit7	6	5	4	3	2	1	Bit0
Read	L0F	0	0	H0OCF	H0F	H0EN	H0PD	H0MS
Write								
Reset	0	0	0	0	0	0	0	0

L0F — L0 Flag Bit

This read only flag reflects the state of the L0 input
1 = L0 input high
0 = L0 input low

H0OCF — H0 Overcurrent Flag Bit

This read/write flag is set at overcurrent condition on H0 during 2pin hallsensor mode. Clear H0OCF by writing a logic [1] to H0OCF.
Reset clears the H0OCF bit.
1 = overcurrent condition on H0 terminal has occurred
0 = no overcurrent condition on H0 terminal has occurred

H0F — H0 Flag Bit

This read only flag reflects the state of the H0 input
1 = Hallport sensed high / current below threshold detected

0 = Hallport sensed low / current above threshold detected

H0EN — H0 Input 2pin Hall-effect sensor Enable Bit

This read/write bit enables the 2pin hall-effect sensor sense circuitry.
Reset clears H0EN bit.

1 = Hallport H0 is switched on and sensed
0 = Hallport H0 disabled

H0PD — Hallport Pull-up Disable Bit

This read/write bit disables the H0 Pull-up resistor.
Reset clears H0PD bit.

1 = Hallport Pull-up resistor on H0 disabled
0 = Hallport Pull-up resistor on H0 enabled

H0MS — H0 Mode Select

These read/write bits select the mode of the H0 input
Reset clears H0MS bit.

1 = H0 is 2-pin hallsensor input
0 = H0 is general purpose input

Half-Bridge Outputs

Outputs HB1:HB4 provide four low-resistive half-bridge output stages. The half-bridges can be used in H-Bridge, high-side or low-side configurations.

Reset clears all bits in the H-Bridge Output Register (HBOUT) owing to the fact that all half-bridge outputs are switched off.

HB1:HB4 output features

- Short circuit (overcurrent) protection on high-side and low-side MOSFETs
- Current recopy feature (low-side MOSFET)
- Overtemperature protection
- Overvoltage and undervoltage protection
- Active clamp on low-side MOSFET

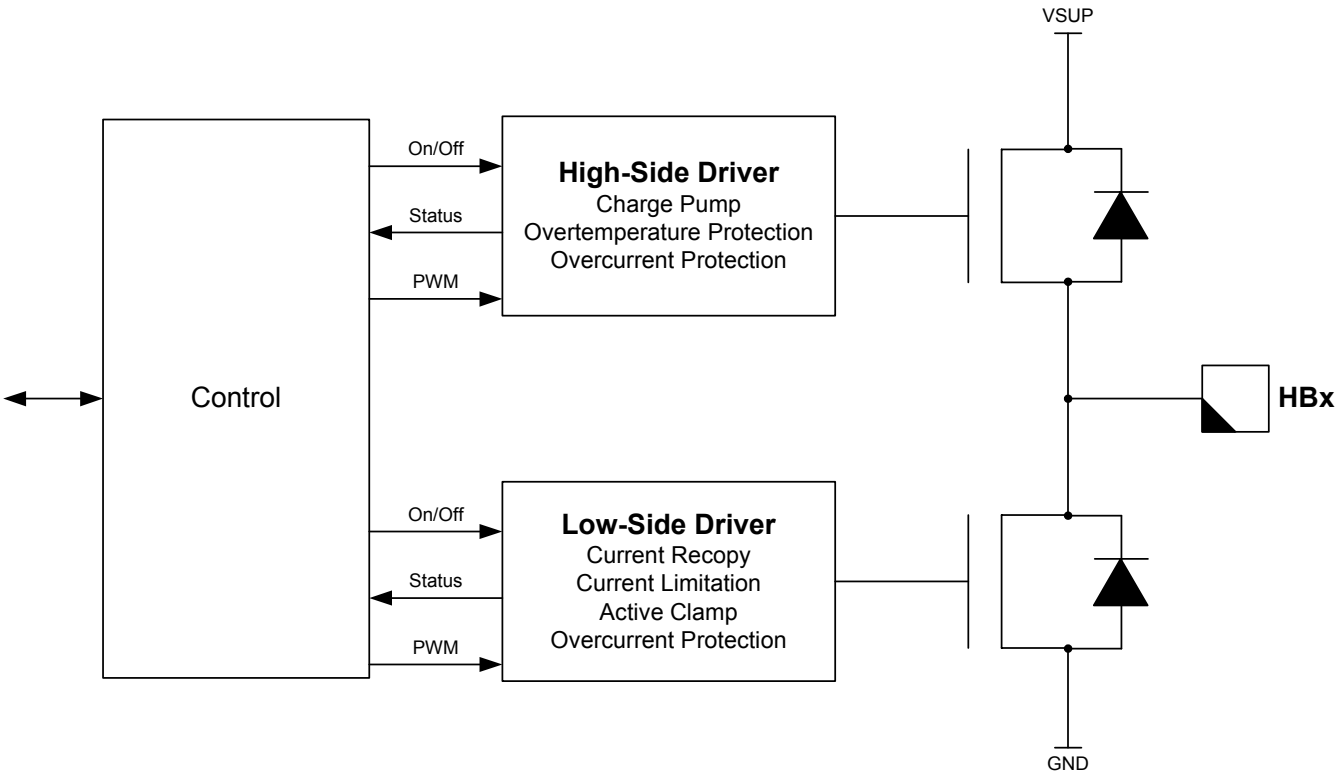


Figure 22. Half-Bridge Push-Pull Output Driver

Half-Bridge Control

Each output MOSFET can be controlled individually. The general enable of the circuitry is done by setting PSON in the System Control Register (SYSCTL). The HBx_L and HBx_H bits form one half bridge. It is not possible to switch on both MOSFETs in one half-bridge at the same time. If both bits are set, the high-side MOSFET is in PWM mode.

To avoid both MOSFETs (high-side and low-side) of one half-bridge being on at the same time, a break-before-make circuit exists. Switching the high-side MOSFET on is inhibited as long as the potential between gate and V_{SS} is not below a certain threshold. Switching the low-side MOSFET on is blocked as long as the potential between gate and source of the high-side MOSFET did not fall below a certain threshold.

HALF-BRIDGE OUTPUT REGISTER (HBOUT)

Register Name and Address: HBOUT - $01

	Bit7	6	5	4	3	2	1	Bit0
Read Write	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
Reset	0	0	0	0	0	0	0	0

HBx_H, HBx_L — Half Bridge Output Switches

These read/write bits select the output of each half-bridge output according to the following table.
Reset clears all HBx_H, HBx_L bits.

Table 9. Half-Bridge Configuration

HBx_H	HBx_L	Mode
0	0	Low-side and high-side MOSFET off
0	1	High-side MOSFET off, low-side MOSFET on
1	0	High-side MOSFET on, low-side MOSFET off
1	1	High-side MOSFET in PWM mode

Half-Bridge PWM mode

The PWM mode is selected by setting both HBxL and HBxH of one Half-bridge to “1”. In this mode the high-side MOSFET is controlled by the incoming PWM signal on the PWM terminal (see Figure 2, page 2).

If the incoming signal is high, the high-side MOSFET is switched on.

If the incoming signal is low, the high-side MOSFET is switched off.

With the current recirculation mode control bit CRM in the Half-Bridge Status and Control Register (HBSCTL) the recirculation behavior in PWM mode can be controlled. If CRM is set the corresponding low-side MOSFET is switched on if the PWM controlled high-side MOSFET is off.

Half-Bridge Current Recopy

Each low-side MOSFET has an additional sense output to allow a current recopy feature. These sense sources are internally amplified and switched to the Analog Multiplexer.

The factor for the Current Sense amplification can be selected via bit CSA in the A0MUCTL register (see page 32)

CSA = “1”: low resolution selected

CSA = “0”: high resolution selected

Half-Bridge Overtemperature Protection

The outputs are protected against overtemperature conditions. Each power output comprises two different temperature thresholds.

The first threshold is the high temperature interrupt (HTI). If the temperature reaches this threshold the HTIF bit in the Interrupt Flag Register (IFR) is set and an interrupt will be initiated if HTIE bit in the Interrupt Mask register is set. In addition this interrupt can be used to automatically turn off the power stages. This shutdown can be enabled/disabled by Bits HTIS0-1 in the System Control Register (SYSCTL).

The high temperature interrupts flag (HTIF) is cleared (and the outputs reenabled) by writing a “1” to the HTIF flag in the Interrupt Flag Register (IFR) or by a reset. Clearing this flag has no effect as long as a high temperature condition is present.

If the HTI shutdown is disabled, a second threshold high temperature reset (HTR) will be used to turn off all power stages (HB (all Fet’s), HS, HVDD, EC, H0) in order to protect the device.

Half-Bridge Overcurrent Protection

The Half-Bridges are protected against short to GND, VSUP and load shorts. The overcurrent protection is implemented on each HB. If a overcurrent condition on the high-side MOSFET occurs the high-side MOSFET is automatically switched off. An overcurrent condition on the low-side MOSFET will automatically turn off the low-side MOSFET. In both cases the corresponding HBxOCF flag in the Half-Bridge Status and Control Register (HBSCTL) is set.

The overcurrent status flag is cleared (and the corresponding Half-Bridge MOSFETs reenabled) by writing a “1” to the HBxOCF in the Half-Bridge Status and Control Register (HBSCTL) or by a reset.

Half-Bridge Overvoltage/Undervoltage Protection

The half-bridge outputs are protected against undervoltage and overvoltage conditions. This protection is done by the low and high voltage interrupt circuitry. If one of this flags (LVIF, HVIF) is set, the outputs are automatically disabled if the VIS bit in the System Control Register (SYSCTL) is cleared.

The overvoltage and undervoltage status flags are cleared (and the outputs reenabled) by writing a “1” to the LVIF / HVIF flags in the Interrupt Flag Register (IFR) or by a reset. Clearing this flag has no effect as long as the high voltage or low voltage condition is still present.

Half-Bridge Status and Control Register (HBSCTL)

Register Name and Address: HBSCTL - $03

	Bit7	6	5	4	3	2	1	Bit0
Read	CRM	0	0	0	HB4 OCF	HB3 OCF	HB2 OCF	HB1 OCF
Write								
Reset	0	0	0	0	0	0	0	0

CRM — Current Recirculation Mode bit

This read/write bit selects the recirculation mode during PWM.
Reset clears the CRM bit.

1 = recirculation via switched on low-side MOSFET
0 = recirculation via low-side free wheeling diode

HBxOCF — Half Bridges Overcurrent Flag Bit

This read/write bit indicates that an overcurrent condition on either the LS or the HS FET on HBx has occurred.

Clear HBxOCF and enable Half Bridge by writing a logic [1] to HBxOCF. Writing a logic [0] to HBxOCF has no effect. Reset clears the HBxOCF bit.

1 = overcurrent condition on HBx occurred
0 = no overcurrent condition on HBx

High-Side Drivers

The high-side outputs are low resistive high-side switches, targeted for driving lamps. The high-sides are protected against overtemperature, overcurrent and overvoltage/ undervoltage.

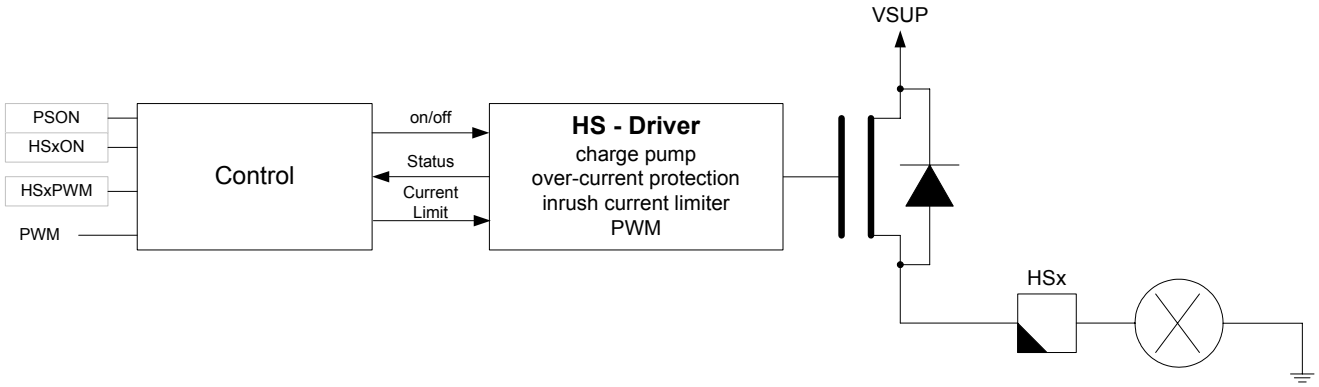


Figure 23. HS circuitry

HIGH-SIDE OPERATING MODES

The High-sides outputs are enabled if the PSON bit in the System Control Register (SYSCTL) is set.

Each high-side output is permanently switched on, if the HSxON bit in the High-Side Output Register (HSOUT) is set.

PWM control of the output is enabled, if the HSxPWM bit High-Side Output Register (HSOUT) is set. In this operating mode the high-side MOSFET is on, if the input PWM signal (PWM terminal) is high.

The below table shows the behavior of the high-side MOSFETs depending on the HSONx and PWMHSx bits.

Table 10. High-Side Configuration Bits

HSxPWM	HSxON	Mode
0	0	High-side MOSFET off
0	1	High-side MOSFET on, in case of overcurrent the overcurrent flag (HSxOCF) is set and the High-side MOSFET is turned off
1	0	In this mode the PWM duty cycle is either controlled by the PWM input signal or in case the overcurrent shutdown value is reached by the part itself. Without reaching the overcurrent shutdown, the high-side driver is directly driven from the PWM input signal. If the Input signal is high the output is on, if low the output is off (PWM control). If the current reaches the overcurrent shutdown value, the high-side will be automatically turned off, with the next rising edge of the PWM input signal the output will turn on again (current limitation). The HSxOCF bit will be set, software has to distinguish between an inrush current and a real short on the output.
1	1	High-side MOSFET is switched on and the inrush current limitation is enabled, means the high side will start automatically with an current limitation around the overcurrent shutdown threshold. (PWM signal must be applied, see Figure 24) If the high-side enters current limitation the HSxOCF bit is set, but the output is not disabled. The software needs to take care about distinguish between an inrush current and a real short on the output.

High-Side Overvoltage / Undervoltage Protection

The outputs are protected against under- / overvoltage conditions. This protection is done by the low and high voltage interrupt circuitry. If an over- under voltage condition is detected (LVIF / HVIF) and Bit VIS in the High-Side Status Register is cleared, the output is disabled.

The over- / undervoltage status flags are cleared (and the output reenabled) by writing a logic [1] to the LVIF / HVIF flags in the Interrupt Flag Register or by reset. Clearing this flag has no effect as long as a high or low voltage condition is present.

HIGH-SIDE OVERTEMPERATURE PROTECTION

The outputs are protected against over temperature conditions.

Each power output comprises two different temperature thresholds.

The first threshold is the high temperature interrupt (HTI), if the temperature reach this threshold the HTI bit in the interrupt flag register is set and an interrupt will be generated if HTIE bit in the interrupt mask register is set. In addition this interrupt can be used to automatically turn off the power stages (all high-sides, on Half bridges just the high-side FET's). This shutdown can be enabled/disabled by Bit HTIS0.

The high temperature interrupts flag (HTIE) is cleared (and the outputs reenabled) by writing a logic [1] to the HTIF flag in the Interrupt Status Register or by reset. Clearing this flag has no effect as long as a high temperature condition is present.

If the HTIS shutdown is disabled, a second threshold (HTR) will be used to turn off all power stages (HB (all Fet's), HS, HVDD, EC, H0) in order to protect the device.

High-Side Overcurrent Protection

The HS outputs are protected against overcurrent. When the overcurrent limit is reached, the output will be automatically switched off and the overcurrent flag is set.

Due to the high inrush current of bulbs a special feature was implemented to avoid a overcurrent shutdown during this inrush current. If a PWM frequency will be supplied to the PWM input during the switch on of a bulb, the inrush current will be limited to the overcurrent shutdown limit. This means, if the current reaches the overcurrent shutdown, the high-side will be switched off, but each rising edge on the PWM input will enable the driver again. The duty cycle supplied by the MCU has no influence on the switch-on time of the high-side driver.

In order to distinguish between a shutdown due to an inrush current or a real shutdown, the software has to check if the overcurrent status flag (HSxOCF) in the High-Side Status register is set beyond a certain period of time.

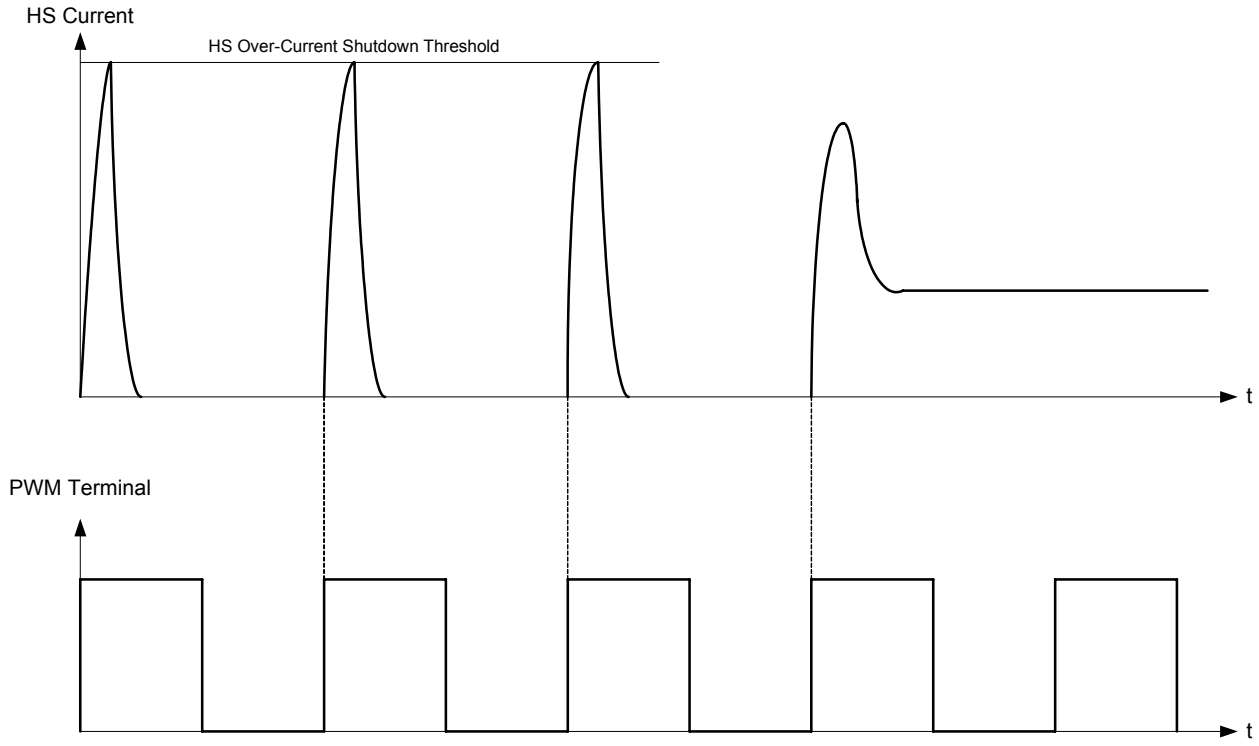


Figure 24. Inrush Current Limitation on HS Outputs

High-Side Current Recopy

Each High-Side has an additional sense output to allow a current recopy feature. This sense source is internally connected to a shunt resistor. The drop voltage is amplified and switched to the Analog Multiplexer.

Switchable HVDD Outputs

The HVDD terminal is a switchable 5V output terminal. It can be used for driving external circuitry which requires a 5V voltage. The output is enabled with bit PSON in the System Control register and can be switched on / off with bit HVDD_ON in the High-Side Out register. Low or high voltage conditions (LVIF / HVIF) will have no influence on this circuitry.

HVDD Over Temperature Protection

The output is protected against over temperature conditions.

HVDD Over Current Protection

The HVDD output is protected against overcurrent. In case the current reach the overcurrent limit, the output current will be limited and the HVDDOCF overcurrent flag in the System Status register is set.

High-Side Out Register (HSOUT)

Register Name and Address: HSOUT - $02

	Bit7	6	5	4	3	2	1	Bit0
Read	HVDD ON	0	HS3P WM	HS2P WM	HS1P WM	HS3O N	HS2O N	HS1O N
Write								
Reset	0	0	0	0	0	0	0	0

HVDD-ON — HVDD On Bit

This read/write bit enables the HVDD output.
Reset clears HVDDON bit.

1 = HVDD enabled
0 = HVDD disabled

HSxON — High-Side on/off Bits

These read/write bits turn on the High-Side Fet's permanently
Reset clears the HSxON bits.

1 = High-Side x is turned on
0 = High-Side x is turned off

HSxPWM — High-Side PWM on/off Bits

These read/write bits enable the PWM control of the High-Side Fet's.
Reset clears the HSxPWM bits.

1 = High-Side x is controlled by PWM input signal
0 = High-Side x is not controlled by PWM input signal

High-Side Status Register (HSSTAT)

Register Name and Address: HSSTAT - $04

	Bit7	6	5	4	3	2	1	Bit0
Read	HVDD OCF	0	0	0	0	HS3O CF	HS2O CF	HS1O CF
Write								
Reset	0	0	0	0	0	0	0	0

HSxOCF — High-Side Overcurrent Flag Bit

This read/write flag is set by an overcurrent condition at the high-side drivers x.
Clear HSxOCF and enable the HS Driver by writing a logic [1] to HSxOCF. Writing a logic [0] to HSxOCF has no effect.
Reset clears the HSxOCF bit.

1 = overcurrent condition on high-side drivers has occurred
0 = no overcurrent condition on high-side drivers has occurred

HVDDOCF — HVDD Output Overcurrent Flag Bit

This read/write flag is set by an overcurrent condition at HVDD terminal. Clear HVDDOCF and enable the output by writing a logic [1] to the HVDDOCF Flag. Writing a logic [0] to HVDDOCF has no effect.
Reset clears the HVDDOCF bit.

1 = overcurrent condition on VDD output has occurred
0 = no overcurrent condition on VDD output has occurred

Electrochrome Circuitry

The EC glass is controlled by two transistors. T1 is switching on/off the EC glass and T2 is controlling the EC output voltage given by the 6Bit DA Converter.

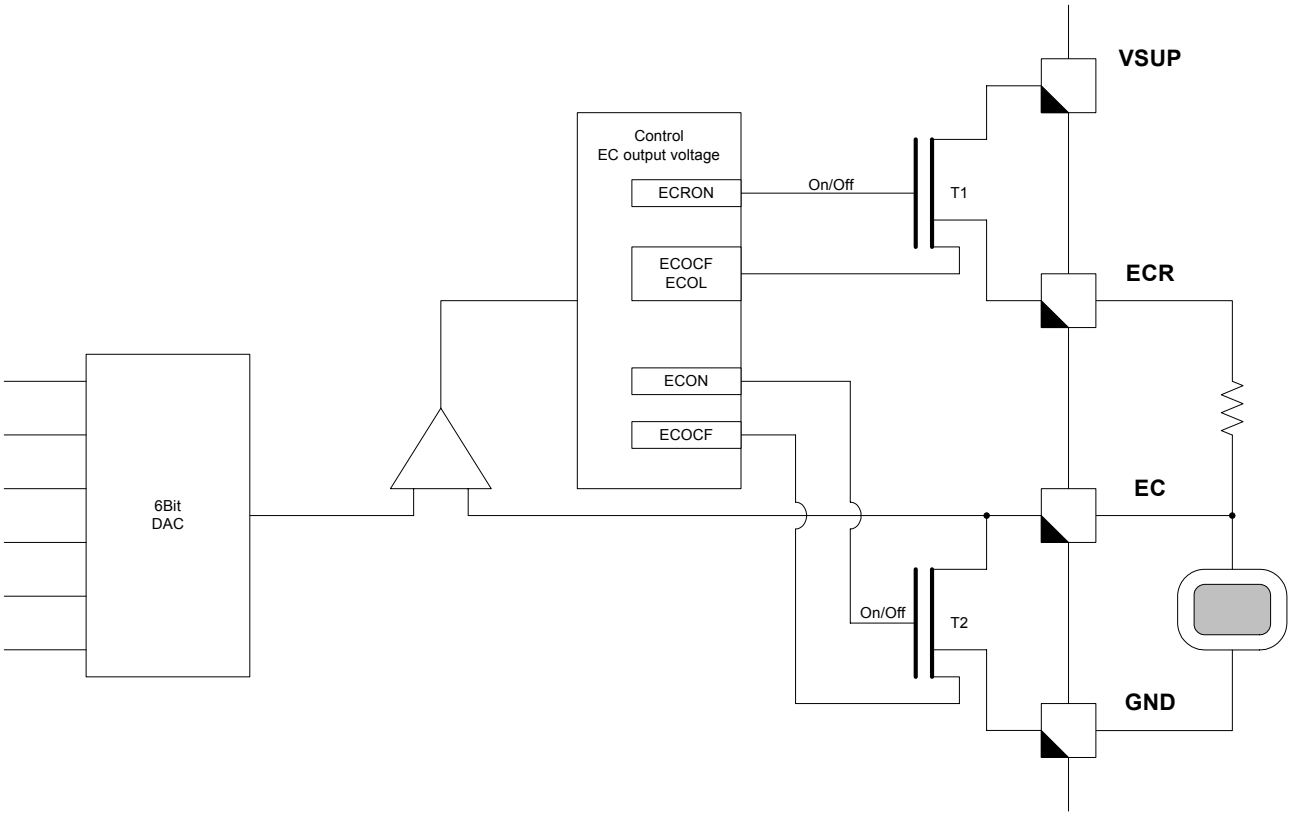


Figure 25. EC Circuitry

EC Open Load Detection

Open Load can be detected by setting ECOLT. A small current source is sourcing a current of typical 200uA on the EC terminal and the voltage on the terminal is measured. In case the voltage is above typical 2V (typical 10K threshold) the ECOLF bit in the EC Status and Control Register ECSCTL is set indicating the open load condition.

If the Open load circuitry is activated (ECOLT=1) the EC glass is disabled.

EC Short Circuit Protection

The EC output is protected against shorts to VSUP. In case of an short circuit the ECOCF in the EC Status and Control Register (ECSCTL) is set and the EC circuitry is disabled.

The EC output is protected against shorts to GND. In case of an short circuit the ECOCF in the EC Status and Control Register (ECSCTL) is set and the EC circuitry is disabled.

EC Digital to Analog Converter

The EC output and therefore the voltage on the EC glass is controlled. The EC glass circuitry has a 6 bit D/A converter to control the output voltage between 0 and 1,4V.

EC D/A Converter Control Register (ECDACC)

Register Name and Address: ECDACC - $06

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	ECDA5	ECDA4	ECDA3	ECDA2	ECDA1	ECDA0
Write								
Reset	0	0	0	0	0	0	0	0

ECDAx — Digital to Analog Bits

These read/write bits set the output voltage on the EC terminal.

EC Status and Control Register (ECSCTL)

Register Name and Address: ECSCTL - $05

	Bit7	6	5	4	3	2	1	Bit0
Read	ECON	ECOLT	ECRON	0	0	0	ECOCF	ECOLF
Write								
Reset	0	0	0	0	0	0	0	0

ECON — Electrochrome Circuitry enable Bit

This read/write bit enables transistor T2 of the electrochrome circuitry.
Reset clears the ECON bit.

1 = T2 EC circuitry enabled
0 = T2 EC circuitry disabled

ECOLT — Electrochrome Circuitry Open Load Test Bit

This read/write bit enables the open load test for the electrochrome circuitry. If this bit is set the EC Glass functionality is ceased.
Reset clears the ECOLT bit.

1 = EC Open Load circuitry enabled
0 = EC Open Load circuitry disabled

ECRON — EC Resistor enable Bit

This read/write bit enables transistor T1 of the electrochrome circuitry.
Reset clears the ECRON bit.

1 = T1 EC circuitry enabled
0 = T1 EC circuitry disabled

Note: Controlling the output voltage on terminal EC is done by transistor T2 only. The enable of T1 will switch the VSUP voltage via the external EC resistor to the EC glass.

ECOCF — EC Output Overcurrent Flag Bit

This read/write flag is set on short circuit condition at the EC output (short to VSUP/ short to GND). Clear ECOCF and enable the EC circuitry by writing a logic [1] to ECOCF. Writing a logic [0] to ECOCF has no effect.
Reset clears the ECOCF bit.

1 = short circuit condition on EC output detected
0 = no short circuit condition on EC output detected

ECOLF — EC Open Load Flag Bit

This read/write flag is set on an open load condition of the EC output.
Clear ECOLF and disable the EC circuitry by writing a logic [1] to ECOLF. Writing a logic [0] to ECOLF has no effect.
Reset clears the ECOLF bit.

1 = open load condition on EC output detected
0 = no open load condition on EC output detected

System Control Register (SYSCTL)

Register Name and Address: SYSCTL - $00

	Bit7	6	5	4	3	2	1	Bit0
Read	PSON	0	0	HTIS1	HTIS0	VIS	SRS1	SRS0
Write		STOP	SLEEP					
Reset	0	0	0	0	0	0	0	0

PSON — Power Stages On Bit

This read/write bit enables the power stages (half bridges, high-sides, LIN transmitter, A0 Current Sources and HVDD output).
Reset clears the PSON bit.

1 = power stages enabled
0 = power stages disabled

STOP — Change to STOP Mode Bit

This write bit instructs the chip to enter Stop mode (See Operational Modes on page 24).
Reset or CPU interrupt requests clear the STOP bit.

1 = go to Stop mode
0 = not in stop mode

In order to safely Stop mode all other bits (Bit7-Bit2) have to be “0”. Otherwise the STOP command will not be executed.

SLEEP — Change to SLEEP Mode Bit

This write bit instructs the chip to enter Sleep mode (See Operational Modes on page 24).
Reset or CPU interrupt requests clear the SLEEP bit.

1 = go to Sleep mode
0 = not in sleep mode

In order to safely enter Sleep mode all other bits (Bit7-Bit2) have to be “0”. Otherwise the SLEEP command will not be executed.

HTIS0-1 — High Temperature Interrupt Shutdown Bits

This read/write bits selects the power stage behavior at High Temperature Interrupt (HTI).
Reset clears the HTIS0-1 bits.

The HTIS0 bit selects the behavior of the high-side HS1:3 and the high-side FET of the half-bridges HB1:4.

1 = automatic HTI shutdown of the high-side drivers disabled
0 = automatic HTI shutdown of the high-side drivers enabled

The HTIS1 bit selects the behavior of the low-side drivers of the half-bridges HB1:4.

1 = automatic HTI shutdown of the low-side drivers disabled

0 = automatic HTI shutdown of the low-side drivers enabled

The user has to take care to protect the device against thermal destruction!

VIS — Over-/Undervoltage Interrupt Shutdown

This read/write bit selects the power stage behavior at LVI/HVI.
Reset clears the VIS bit.
1 = automatic LVI/HVI shutdown disabled
0 = automatic LVI/HVI shutdown enabled

SRS0-1 — LIN Slew rate Select Bits

These read/write bits enable the user to select the appropriate LIN slew rate for different Baudrate configurations.
Reset clears the SRS1:0 bits.

Table 11. LIN Slew Rate Selection Bits

SRS1	SRS0	Slew rate
0	0	Initial Slew Rate (20kBaud)
0	1	High Speed II (8x)
1	0	Slow Slew Rate (10kBaud)
1	1	High Speed I (4x)

The high speed slew rates are used, for example, for programming via the LIN and are not intended for use in the application.

System Status Register (SYSSTAT)

Register Name and Address: SYSSTAT - $0C

	Bit7	6	5	4	3	2	1	Bit0
Read	LINCL	HTIF	VF	H0F	HVDDF	HSF	HBF	ECF
Write								
Reset	0	0	0	0	0	0	0	0

LINCL — LIN Current Limitation Bit

This read only bit is set if the LIN transmitter operates in current limitation region. Due to excessive power dissipation in the transmitter, the driver will be automatically turned off after a certain time.
1 = transmitter operating in current limitation region
0 = transmitter not operating in current limitation region

HTIF— Overtemperature Status Bit

This read only bit is a copy of the HTIF bit in the Interrupt Flag register
1 = overtemperature condition
0 = no overtemperature condition

VF — Voltage Failure Bit

This read only bit indicates that the supply voltage was out of the allowed range. The bit is set if either the LVIF or the HVIF in the Interrupt Flag register is set.
1 = low/high voltage condition detected
0 = no voltage failure condition detected

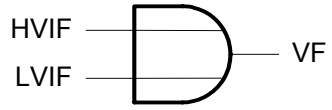


Figure 26. VF flag generation

H0F — H0 Failure Bit

This read only bit is a copy of the H0OCF bit in the H0/L0 Status and Control Register (HLSCTL)
1 = overcurrent detected on H0
0 = no overcurrent on H0

HVDDF— HVDD Failure Bit

This read only bit is a copy of the HVDDOCF bit in the High-Side Status register
1 = HVDD terminal fail
0 = HVDD normal operating

HSF— HS1:3 Failure Bit

This read only bit is set if a fail condition on one of the high-side outputs is present
1 = HS1:3 terminal fail
0 = HS1:3 normal operating

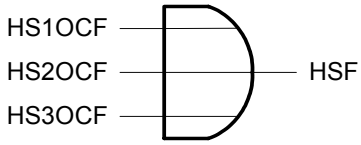


Figure 27. HSF flag generation

HBF— HB1:4 Failure Bit

This read only bit is set if a fail condition on one of the half bridge outputs is present.
1 = HB1:4 terminal overcurrent fail
0 = HB1:4 normal operating

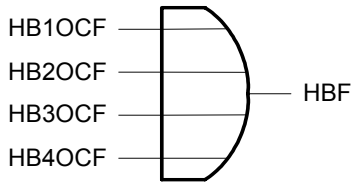


Figure 28. HBF flag generation

ECF— EC terminal Failure Bit

This read only bit is set if a fail condition on the electrochrome output is present

1 = EC terminal fail
0 = EC normal operating

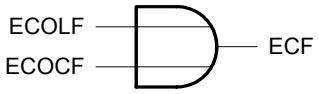


Figure 29. ECF flag generation

WINDOW WATCHDOG

The window watchdog is to supervise the device and to recover from e.g. code runaways or similar conditions.

The use of a window watchdog adds additional safety as the watchdog clear has not only to occur but to be done at a certain time frame / window.

Normal mode

The window watchdog function is just available in Normal mode and is ceased in Stop and Sleep mode. On setting the WDRE bit, the watchdog functionality is activated. Once this function is enabled it is not possible to disable it via software. Reset clears the WDRE bit.

To prevent a Watchdog reset, the Watchdog timer has to be cleared in the Window Open frame. This is done by writing a logic “1” to the WDRST bit in the Watchdog Control register (WDCTL). The actual reset of the watchdog counter occurs at the end of the corresponding SPI transmission with the rising edge of the $\overline{SS}$ signal.

If the watchdog is enabled, it will generate a system reset if the timer has reached its end value or if a watchdog reset (WDRST) has occurred in the closed window.

The watchdog period can be selected with 2 bits in the WDCTL, in order to get 10ms, 20ms, 40ms and 80ms period.

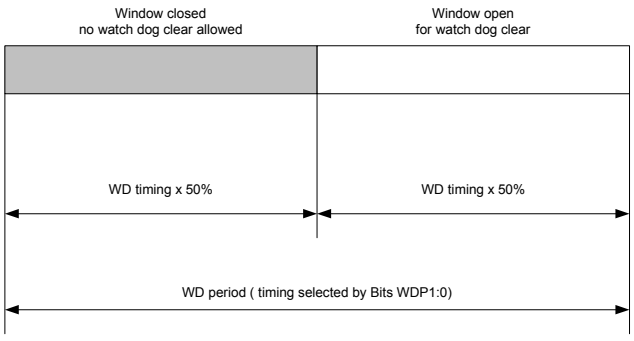


Figure 30. Window Watchdog Period

Stop mode

Operations of the watchdog function is ceased in stop mode (counter/oscillator stopped). After wake-up the watchdog timer **is automatically cleared** in order to give the MCU the full time to reset the watchdog.

Sleep mode

Operations of the watchdog function is ceased is sleep mode. Due to the reason that the main voltage regulator asserts an LVR reset the Watchdog functionality is disabled and the WDRE bit is cleared as soon as sleep mode is entered. To reenable this function bit WDRE has to be set after wake-up.

Watchdog Control Register (WDCTL)

Register Name and Address: WDCTL - $0B

	Bit7	6	5	4	3	2	1	Bit0
Read	WDRE	WDP1	WDP0	0	0	0	0	0
Write								WDRST
Reset	0	0	0	0	0	0	0	0

WDRE - Watchdog Reset Enable Bit

This read/write (write once) bit activates the watchdog The WDRE can only be set and can’t be cleared by software. Reset clears the WDRE bit.

1 = Watchdog enabled
0 = Watchdog disabled

WDP1:0 - Watchdog Period Select Bits

This read/write bit select the clock rate of the Watchdog. Reset clears the WDP1:0 bits.

Table 12. Watchdog Period Selection Bits

WDP1	WDP0	Mode
0	0	80ms window watchdog period
0	1	40ms window watchdog period
1	0	20ms window watchdog period
1	1	10ms window watchdog period

WDRST - Watchdog Reset Bit

This write only bit resets the Watchdog. Write a logic [1] to reset the watchdog timer.

1 = Reset WD and restart timer
0 = no effect

Voltage Regulator

The 908E622 contains a low power, low drop voltage regulator to provide internal power and external power for the MCU. The on-chip regulator consist of two elements, the main regulator and the low voltage reset circuit.

The V_{DD} regulator accepts an unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD terminal to provide the 5.0 V to the microcontroller.

Run mode

During RUN mode the main voltage regulator is on. It will provide a regulated supply to all digital sections.

STOP mode

During STOP mode, the Stop mode regulator will take care of suppling a regulated output voltage. The Stop mode regulator has a limited output current capability.

SLEEP mode

In Sleep mode the main voltage regulator external V_{DD} is turned off and the LVR circuitry will force the $\overline{\text{RST\_A}}$ terminal low.

LOGIC COMMANDS AND REGISTERS

908E622 SERIAL PHERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) creates the communication link between the MCU and the analog die.

The interface consists of four terminals

- MOSI - Master Out Slave In (internal pull-down)
- MISO - Master In Slave Out
- SPSCK - Serial Clock (internal pull-down)
- $\overline{SS}$ - Slave Select (internal pull-up)

A complete data transfer via the SPI, consists of 2 bytes. The master sends address and data, the slave returns system status and the data of the selected address.

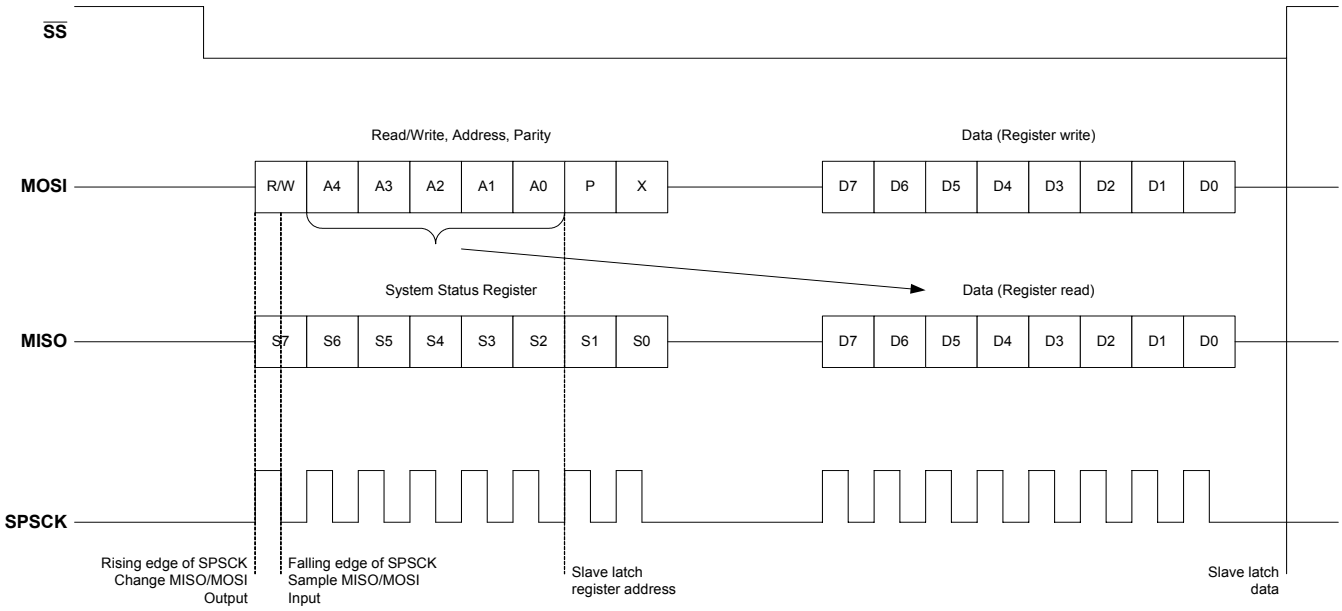


Figure 31. SPI Protocol

- During the inactive phase of $\overline{SS}$, the new data transfer will be prepared. The falling edge on the $\overline{SS}$ line, indicates the start of a new data transfer (framing) and puts MISO in the low impedance mode. The first valid data are moved to MISO with the rising edge of SPSCK.
- The MOSI, MISO will change data on a rising edge of SPSCK.
- The MOSI, MISO will be sampled on a falling edge of SPSCK.
- The data transfer is only valid, if exactly 16 sample clock edges are present in the active phase of $\overline{SS}$.
- After a write operation the transmitted data will be latched into the register, by the rising edge of $\overline{SS}$.
- Register read data is internally latched into the SPI, at the time when the parity bit is transferred
- $\overline{SS}$ high will force MISO to high impedance

Master Address Byte

A4 - A0

include the address of the desired register.

R/$\overline{W}$

includes the information if it is a read or a write operation.

- If R/$\overline{W}$ = 1 (read operation), second byte of master contains no valid information, slave just transmits back register data.
- If R/$\overline{W}$ = 0 (write operation), master sends data to be written in the second byte, slave sends concurrently contents of selected register prior to write operation, write data is latched in the *SmartMOS* registers on rising edge of $\overline{SS}$

Parity P

completes the total number of 1 bits of (R/W,A[4-0]) to an even number. e.g. (R/W,A[4-0]) = 100001 -> P0 = 0.

The parity bit is only evaluated during a write operations and ignored for read operations.

Bit X

not used

Master Data Byte

This byte includes data to be written or no valid data during a read operation.

Slave Status Byte

This byte includes always the contents of the system status register ($0C) independent if it is a write or read operation or which register was selected.

Slave Data Byte

This byte includes the contents of selected register, during write operation in includes the register content prior to write operation.

SPI REGISTER OVERVIEW

TABLE 13 SUMMARIZES THE SPI REGISTER ADDRESSES AND THE BIT NAMES OF EACH REGISTER.

Table 13. SPI Register Overview

Addr	Register Name	R/W	Bit							
			7	6	5	4	3	2	1	0
$00	System Control (SYSCTL)	R	PSON	0	0	HTIS1	HTIS0	VIS	SRS1	SRS0
		W		STOP	SLEEP					
$01	Half-Bridge Output (HBOUT)	R	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
		W								
$02	High-Side Output (HSOUT)	R	HVDDON	0	HS3PWM	HS2PWM	HS1PWM	HS3ON	HS2ON	HS1ON
		W								
$03	Half-Bridge Status and Control (HBSCTL)	R	CRM	0	0	0	HB4OCF	HB3OCF	HB2OCF	HB1OCF
		W								
$04	High-Side Status and Control (HSSCTL)	R	HVDDOCF	0	0	0	0	HS3OCF	HS2OCF	HS1OCF
		W								
$05	EC Status and Control (ECSCTL)	R	ECON	ECOLT	ECRON	0	0	0	ECOCF	ECOLF
		W								
$06	EC Digital to Analog Control (ECDACC)	R	0	0	ECDAC5	ECDAC4	ECDAC3	ECDAC2	ECDAC1	ECDAC0
		W								
$07	H0/L0 Status and Control (HLSCTL)	R	L0F	0	0	H0OCF	H0F	H0EN	H0PD	H0MS
		W								
$08	A0 and Multiplexer Control (A0MUCTL)	R	CSON	CSSEL1	CSSEL0	CSA	SS3	SS2	SS1	SS0
		W								
$09	Interrupt Mask (IMR)	R	L0IE	H0IE	LINIE	HTRD	HTIE	LVIE	HVIE	PSFIE
		W								
$0A	Interrupt Flag (IFR)	R	L0IF	H0IF	LINIF	0	HTIF	LVIF	HVIF	PSFIF
		W								
$0B	Watchdog Control (WDCTL)	R	WDRE	WDP1	WDP0	0	0	0	0	0
		W								WDRST
$0C	System Status (SYSSTAT)	R	LINCL	HTIF	VF	H0F	HVDDF	HSF	HBF	ECF
		W								
$0D	Reset Status (RSR)	R	POR	PINR	WDR	HTR	LVR	0	LINWF	L0WF
		W								
$0E	System Test (SYSTEST)	R	reserved							
		W								
$0F	System Trim 1 (SYSTRIM1)	R	HVDDT1	HVDDT0	reserved	reserved	itrim3	itrim2	itrim1	itrim0
		W								
$10	System Trim 2 (SYSTRIM2)	R	0	0	0	0	0	0	0	0
		W	CRHBHC1	CRHBHC0	CRHB5	CRHB4	CRHB3	CRHB2	CRHB1	CRHB0
$11	System Trim 3 (SYSTRIM3)	R	0	0	0	0	0	0	0	0
		W	CRHBHC3	CRHBHC2	CRHS5	CRHS4	CRHS3	CRHS2	CRHS1	CRHS0

FACTORY TRIMMING AND CALIBRATION

To enhance the ease-of-use of the 908E622, various parameters (e.g. ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the “empty” ($FF) state:

- $FD80:$FDDF Trim and Calibration Values
- $FFFE:$FFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

Trim Values

Below the usage of the trim values located in the flash memory is explained

Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller without using any external components. The untrimmed frequency of the low frequency base clock (IBASE), will vary as much as ±25 percent due to process, temperature, and voltage dependencies. To compensate this dependencies a ICG trim values is located at address $FDC2. After trimming the ICG is a range of typ. ±2% (±3% max.) at nominal conditions (filtered (100nF) and stabilized (4,7uF) V_{DD} = 5V, $T_{Ambient}$~25°C) and will vary over temperature and voltage (V_{DD}) as indicated in the 68HC908EY16 datasheet.

To trim the ICG this values has to be copied to the ICG Trim Register ICGTR at address $38 of the MCU.

Important The value has to copied after every reset.

Watchdog Period Range Value (AWD Trim)

The window watchdog supervises device recover from e.g. code runaways.

The application software has to clear the watchdog within the open window. Due to the high variation of the watchdog period - and therefore the reduced width of the watchdog window - a value is stored at address $FDCF. This value classifies the watchdog period into 3 ranges (Range 0, 1, 2). This allows the application software to select one out of three time intervals to clear the watchdog based on the stored value. The classification is done in a way that the application software can have up to ±19% variation of the of optimal clear interval, e.g. caused by ICG variation.

Effective Open Window

Having a variation in the watchdog period in conjunction with a 50% open window results in effective open window, which can be calculated by:

latest window open time: t_open = t_wd max / 2

earliest window closed time: t_closed = t_wd min

Optimal Clear Interval

The optimal clear interval - meaning the clear interval with the biggest possible variation to latest window open time and to the earliest window closed time can be calculated with the following formula:

t_opt = t_open + (t_open+t_closed) / 2

See Table 14 to select the optimal clear interval for the watchdog based on the Window No. and chosen period.

Table 14. Window Clear Interval

Window Range	Period Select bits	Watchdog Period t_wd			Effective Open Window			Optimal Clear Interval		
$FDCF	WDP1:0	min.	max.	Unit	t_open	t_closed	Unit	t_opt	Unit	max. variation
0	00	68	92	ms	46	68	ms	57	ms	±19.3%
	01	34	46		23	34		28.5		
	10	17	23		11.5	17		14.25		
	11	8.5	11.5		5.75	8.5		7.125		
1	00	92	124	ms	62	92	ms	77	ms	±19.5%
	01	46	62		31	46		38.5		
	10	23	31		15.5	23		19.25		
	11	11.5	15.5		7.75	11.5		9.625		
2	00	52	68	ms	34	52	ms	43	ms	±20.9%
	01	26	34		17	26		21.5		
	10	13	17		8.5	13		10.75		
	11	6.5	8.5		4.25	6.5		5.375		

Analog Die System Trim Values

For improved application performance and to ensure the outlined datasheet values the analog die needs to be trimmed. For this purpose 3 trim values are stored in the Flash memory at address $FDC4 - $FDC6. These values have to be copied into the analog die SPI registers:

- copy $FDC4 into SYSTRIM1 register $0F
- copy $FDC5 into SYSTRIM2 register $10
- copy $FDC6 into SYSTRIM3 register $11

Note: This values have to be copied to the respective SPI register after a reset to ensure proper trimming of the device.

System Test Register (SYSTEST)

Register Name and Address: SYSTEST - $0E

	Bit7	6	5	4	3	2	1	Bit0
Read Write	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0

Note: do not write to the reserved bits

The System Test Register is reserved for production testing and is not allowed to be written to.

System Trim Register 1 (SYSTRIM1)

Register Name and Address: IBIAS - $0F

	Bit7	6	5	4	3	2	1	Bit0
Read Write	HVDDT1	HVDDT0	0 reserved	0 reserved	ITRIM3	ITRIM2	ITRIM1	ITRIM0
Reset	0	0	0	0	0	0	0	0

Note: do not change (set) the reserved bits

HVDDT1:0 - HVDD Overcurrent Shutdown Delay Bits

These read/write bits allow to change the filter time (for capacitive load) for the HVDD over current detection. Reset clears the HVDDT1:0 bits an sets the delay to the maximum value.

Table 15. HVDD Overcurrent Shutdown Selection Bits

HVDDT1	HVDDT0	typical Delay
0	0	950us
0	1	536us
1	0	234us
1	1	78us

ITRIM3:0 - IRef Trim Bits

These write only bits are for trimming of the internal current references IRef (also A0, A0CST). The provided trim values have to be copied into these bits after every reset. Reset clears the ITRIM3:0 bits.

Table 16. IRef Trim Bits

itrim3	itrim2	itrim2	itrim0	Adjustment
0	0	0	0	0
0	0	0	1	2%
0	0	1	0	4%
0	0	1	1	8%
0	1	0	0	12%
0	1	0	1	-2%
0	1	1	0	-4%
0	1	1	1	-8%
1	0	0	0	-12%

System Trim Register 2 (SYSTRIM2)

Register Name and Address: IFBHBTRIM - $10

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	0	0	0	0
Write	CRHBHC1	CRHBHC0	CRHB5	CRHB4	CRHB3	CRHB2	CRHB1	CRHB0
Reset	0	0	0	0	0	0	0	0

CRHBHC1:0 - Current Recopy HB1:2 Trim Bits

These write only bits are for trimming of the current recopy of the half-bridge HB1 and HB2 (CSA=0). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHBHC1:0 bits.

Table 17. Current Recopy Trim for HB1:2 (CSA=0)

CRHBHC1	CRHBHC0	Adjustment
0	0	0
0	1	-10%

CRHBHC1	CRHBHC0	Adjustment
1	0	5%
1	1	10%

CRHB5:3 - Current Recopy HB3:4 Trim Bits

These write only bits are for trimming of the current recopy of the half-bridge HB3 and HB4 (CSA=1). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHB5:3 bits.

Table 18. Current Recopy Trim for HB3:4 (CSA=1)

CRHB5	CRHB4	CRHB3	Adjustment
0	0	0	0
0	0	1	-5%
0	1	0	-10%
0	1	1	-15%
1	0	0	reserved
1	0	1	5%
1	1	0	10%
1	1	1	15%

CRHB2:0 - Current Recopy HB1:2 Trim Bits

These write only bits are for trimming of the current recopy of the half-bridge HB1 and HB2 (CSA=1). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHB2:0 bits.

Table 19. Current Recopy Trim for HB1:2 (CSA=1)

CRHB2	CRHB1	CRHB0	Adjustment
0	0	0	0
0	0	1	-5%
0	1	0	-10%
0	1	1	-15%
1	0	0	reserved
1	0	1	5%
1	1	0	10%
1	1	1	15%

System Trim Register 3 (SYSTRIM3)

Register Name and Address: IFBHSTRIM - $11

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	0	0	0	0
Write	CRHBHC3	CRHBHC2	CRHS5	CRHS4	CRHS3	CRHS2	CRHS1	CRHS0
Reset	0	0	0	0	0	0	0	0

CRHBHC3:2 - Current Recopy HB3:4 Trim Bits

These write only bits are for trimming of the current recopy of the half-bridge HB3 and HB4 (CSA=0). The provided trim values have to be copied into these bits after every reset. Reset clears the CRHBHC3:2 bits.

Table 20. Current Recopy Trim for HB3:4 (CSA=0)

CRHBHC3	CRHBHC2	Adjustment
0	0	0
0	1	-10%
1	0	5%
1	1	10%

CRHS5:3 - Current Recopy HS2:3 Trim Bits

These write only bits are for trimming of the current recopy of the high-side HS2 and HS3. The provided trim values have to be copied into these bits after every reset. Reset clears the CRHS5:3 bits.

Table 21. Current Recopy Trim for HS2:3

CRHS5	CRHS4	CRHS3	Adjustment
0	0	0	0
0	0	1	-5%
0	1	0	-10%
0	1	1	-15%
1	0	0	reserved
1	0	1	5%
1	1	0	10%
1	1	1	15%

CRHS2:0 - Current Recopy HS1 Trim Bits

These write only bits are for trimming of the current recopy of the high-side HS1. The provided Trim values have to be copied into these bits after every reset. Reset clears the CRHS2:0 bits.

Current Recopy Trim for HS1

CRHS2	CRHS1	CRHS0	Adjustment
0	0	0	0
0	0	1	-5%
0	1	0	-10%
0	1	1	-15%
1	0	0	reserved
1	0	1	5%
1	1	0	10%
1	1	1	15%

TYPICAL APPLICATIONS

DEVELOPMENT SUPPORT

As the 908E622 has the MC68HC908EY16 MCU embedded, typically all the development tools available for the MCU also apply for this device. However, due to the additional analog die circuitry and the nominal +12V supply voltage, some additional items have to be considered:

- nominal 12V rather than 5V or 3V supply
- high voltage $V_{\overline{TST}}$ might be applied not only to $\overline{IRQ}$ terminal, but $\overline{IRQ\_A}$ terminal
- MCU monitoring (Normal request time-out) has to be disabled

For a detailed information on the MCU related development support see the MC68HC908EY16 datasheet - section development support.

The programming is principally possible at two stages in the manufacturing process - first on chip level, before the IC is soldered onto a pcb board, and second after the IC is soldered onto the pcb board.

Chip level programming

At the Chip level, the easiest way is to only power the MCU with +5V (see Figure 32), and not to provide the analog chip with VSUP. In this setup all the analog terminal should be left open (e.g. VSUP[1:8]) and interconnections between MCU and analog die have to be separated (e.g. $\overline{IRQ}$ - $\overline{IRQ\_A}$).

This mode is well described in the MC68HC908EY16 datasheet - section development support.

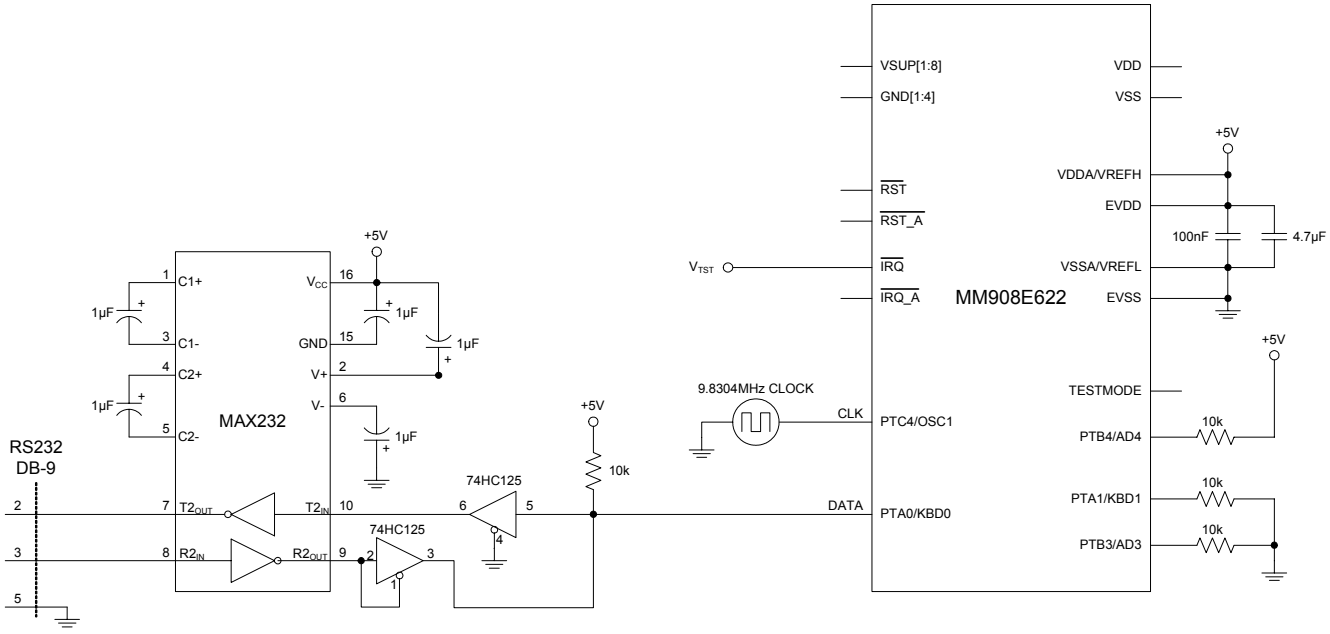


Figure 32. Normal Monitor Mode Circuit (MCU only)

Of course its also possible to supply the whole system with Vsup instead (12V) as described in Figure 33, page 56.

PCB level programming

If the IC is soldered onto the pcb board, its typically not possible to separately power the MCU with +5V. The whole system has to be powered up providing V_{SUP} (see Figure 33)..

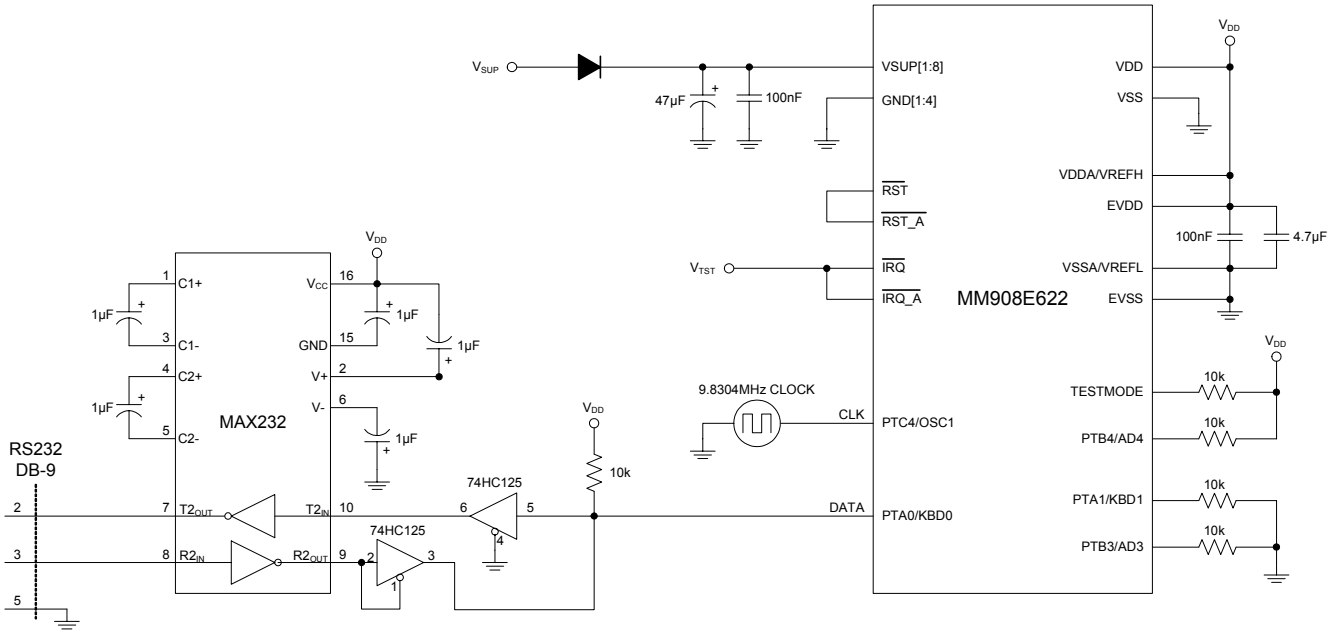


Figure 33. Normal Monitor Mode Circuit

Table 22 summarizes the possible configurations and the necessary setups.

Table 22. Monitor Mode Signal Requirements and Options

Mode	$\overline{IRQ}$	$\overline{RST}$	TESTMODE	Reset Vector	Serial Communication		Mode Selection		ICG	COP	Normal Request Time-out	Communication Speed		
					PTA0	PTA1	PTB3	PTB4				External Clock	Bus Frequency	Baud Rate
Normal Monitor	V_{TST}	V_{DD}	1	X	1	0	0	1	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
Forced Monitor	V_{DD}	V_{DD}	1	$FFFF (blank)	1	0	X	X	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
	GND								ON	disabled	disabled	—	Nominal 1.6MHz	Nominal 6300
User	V_{DD}	V_{DD}	0	not $FFFF (not blank)	X	X	X	X	ON	enabled	enabled	—	Nominal 1.6MHz	Nominal 6300

Notes

1. PTA0 must have a pullup resistor to V_{DD} in monitor mode
2. External clock is a 4.9152MHz, 9.8304MHz or 19.6608MHz canned oscillator on OCS1
3. Communication speed with external clock is depending on external clock value. Baud rate is bus frequency / 256
4. X = don't care
5. V_{TST} is a high voltage $V_{DD} + 3.5V \leq V_{TST} \leq V_{DD} + 4.5V$

EMC/EMI RECOMMENDATIONS

This paragraph gives some device specific recommendations to improve EMC/EMI performance. Further generic design recommendations can be e.g. found on the Freescale web site www.freescale.com.

VSUP terminals (VSUP[1:8])

Its recommended to place a high quality ceramic decoupling capacitor close to the VSUP terminals to improve EMC/EMI behavior.

LIN terminal

For DPI (Direct Power Injection) and ESD (Electrostatic Discharge) its recommended to place a high quality ceramic decoupling capacitor near the LIN terminal. An additional varistor will further increase the immunity against ESD. A ferrite in the LIN line will suppress some of the noise induced.

Voltage regulator output terminals (VDD and VSS)

Use a high quality ceramic decoupling capacitor to stabilize the regulated voltage.

MCU digital supply terminals (EVDD and EVSS)

Fast signal transitions on MCU terminals place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU. It is recommended that a high quality ceramic decoupling capacitor be placed between these terminals.

MCU analog supply terminals (VREFH/VDDA and VREFL/VSSA)

To avoid noise on the analog supply terminals, its important to take special care on the layout. The MCU digital and analog supplies should be tied to the same potential via separate traces and connected to the voltage regulator output.

Figure 34 and Figure 35 show the recommendations on schematics and layout level and Table 23 indicates recommended external components and layout considerations.

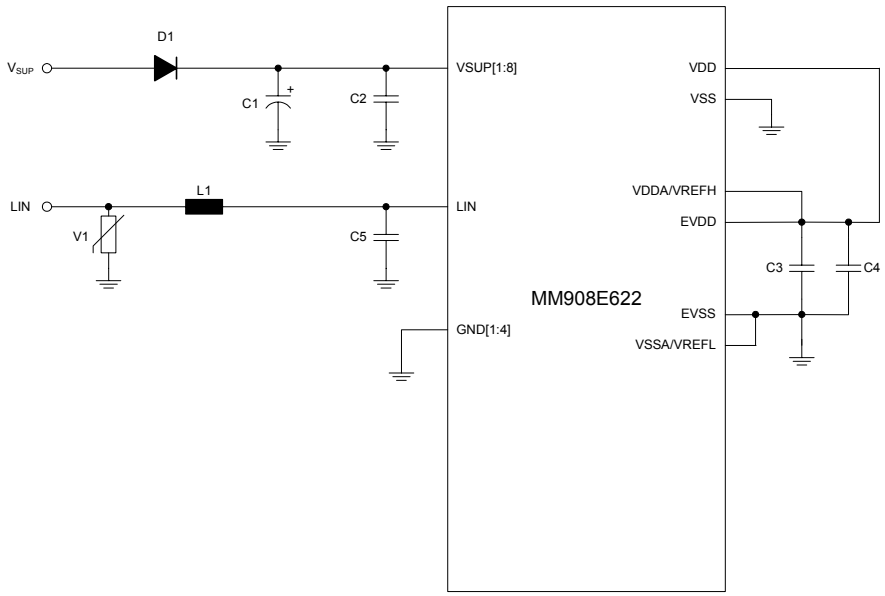


Figure 34. EMC/EMI recommendations

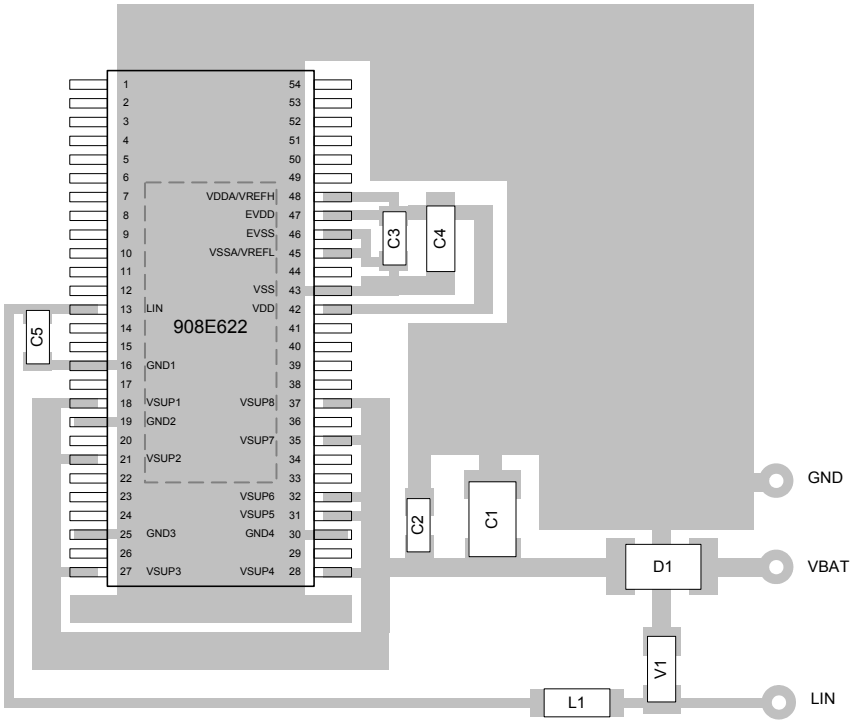


Figure 35. PCB Layout Recommendations

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Table 23. Component Value Recommendation

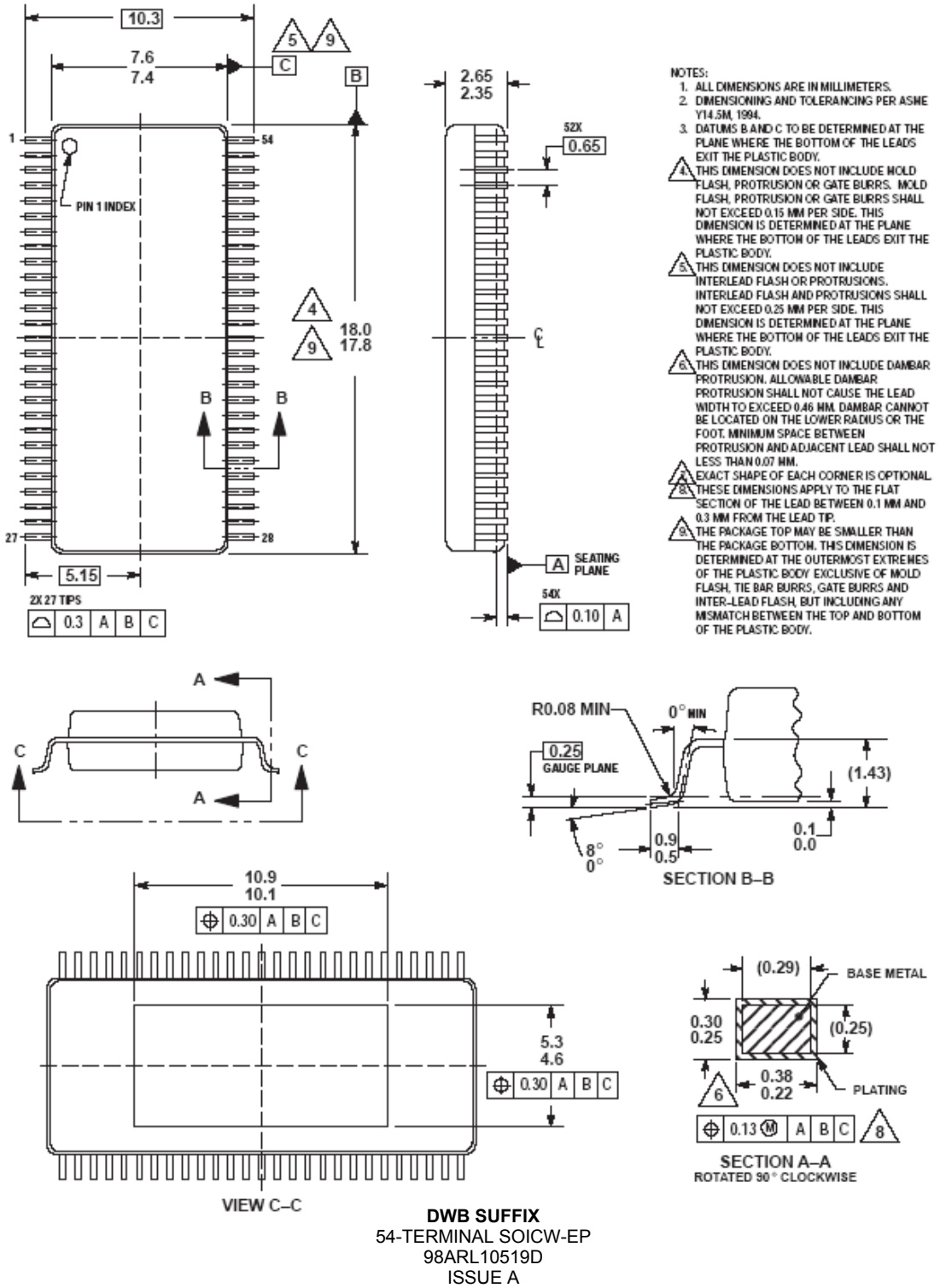
Component	Recommended Value[1]	Comments / Signal routing
D1		reverse battery protection
C1	Bulk Capacitor	
C2	100nF, SMD Ceramic, Low ESR	Close to VSUP terminals with good ground return
C3	100nF, SMD Ceramic, Low ESR	Close (<3mm) to digital supply terminals (EVDD, EVSS) with good ground return. The positive analog (VREFH/ VDDA) and the digital (EVDD) supply should be connected right at the C3.
C4	4,7uF, SMD Ceramic, Low ESR	Bulk Capacitor
C5	180pF, SMD Ceramic, Low ESR	Close (<5mm) to LIN terminal. Total Capacitance on LIN has to be below 220pF. (C_{total} = $C_{LIN-Terminal}$ + C5 + $C_{Varistor}$ ~ 10pF + 180pF + 15pF)
V1[2]	Varistor Type TDK AVR-M1608C270MBAAB	Optional (close to LIN connector)
L1[2]	SMD Ferrite Bead Type TDK MMZ2012Y202B	Optional, (close to LIN connector)

Notes

1. Freescale does not assume liability, endorse, or want components from external manufactures that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
2. Components are recommended to improve EMC and ESD performance.

PACKAGE DIMENSIONS

Important For the most current revision of the package, visit www.freescale.com and do a keyword search on the 98A drawing number: 98ARL10519D.



DWB SUFFIX
54-TERMINAL SOICW-EP
98ARL10519D
ISSUE A

908E622

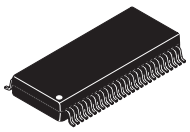
ADDITIONAL INFORMATION

THERMAL ADDENDUM

INTEGRATED QUAD H-BRIDGE, TRIPLE HIGH-SIDE AND EC GLASS DRIVER WITH EMBEDDED MCU AND LIN FOR MIRROR

908E622

54-TERMINAL SOICW-EP



DWB SUFFIX
98ARL105910
54-TERMINAL SOICW-EP

Note For package dimensions, refer to the 908E622 device datasheet.

Thermal Addendum

Introduction

This thermal addendum ia provided as a supplement to the MM908E622 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application and packaging information is provided in the data sheet.

Package and Thermal Considerations

This MM908E622 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

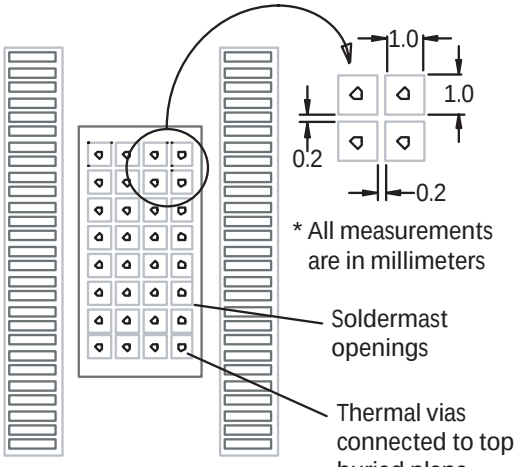
The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 24. Thermal Performance Comparison

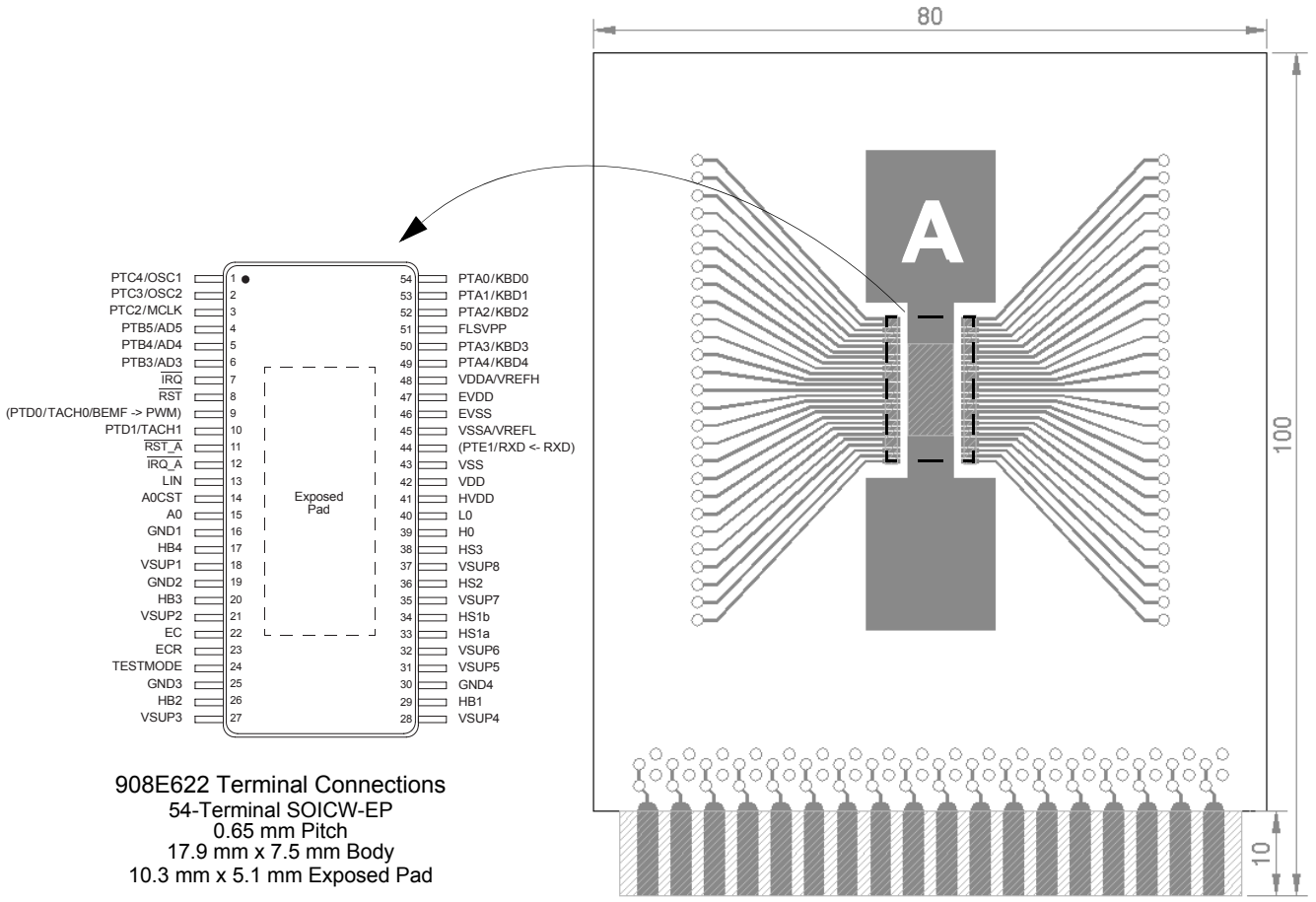
Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$ (1)(2)	23	20	24
$R_{\theta JBmn}$ (2)(3)	9.0	6.0	10
$R_{\theta JAmn}$ (1)(4)	52	47	52
$R_{\theta JCmn}$ (5)	1.0	0	2.0

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.



54 Terminal SOIC-EP
0.65 mm Pitch
17.9 mm x 7.5 mm Body
10.3 mm x 5.1 mm Exposed Pad

Figure 36. Thermal Land Pattern for Direct Thermal Attachment Per JEDEC JESD51-5



908E622 Terminal Connections
54-Terminal SOICW-EP
0.65 mm Pitch
17.9 mm x 7.5 mm Body
10.3 mm x 5.1 mm Exposed Pad

Figure 37. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area **A**:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 25. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$	0	53	48	53
	300	39	34	38
	600	35	30	34
$R_{\theta JSmn}$	0	21	16	20
	300	15	11	15
	600	14	9.0	13

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

$R_{\theta JSmn}$ is the thermal resistance between die junction and the reference location on the board surface near a center lead of the package. This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

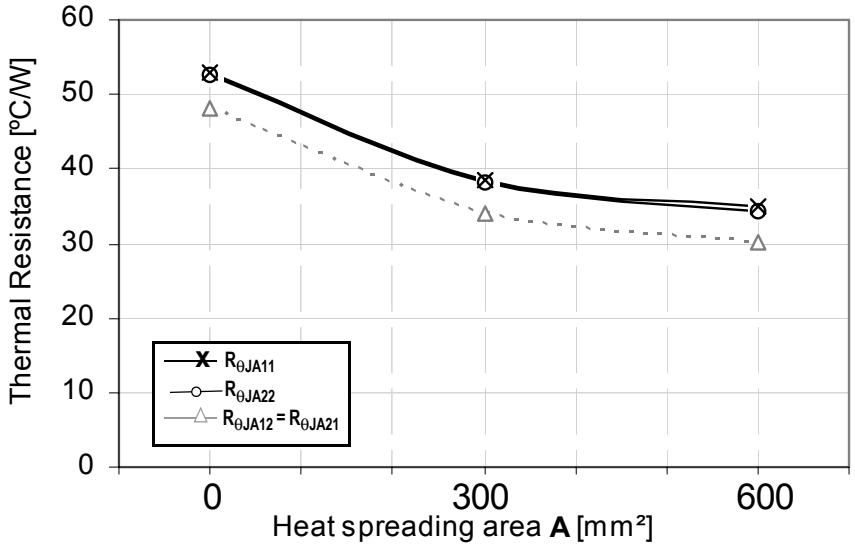


Figure 38. Device on Thermal Test Board $R_{\theta JA}$

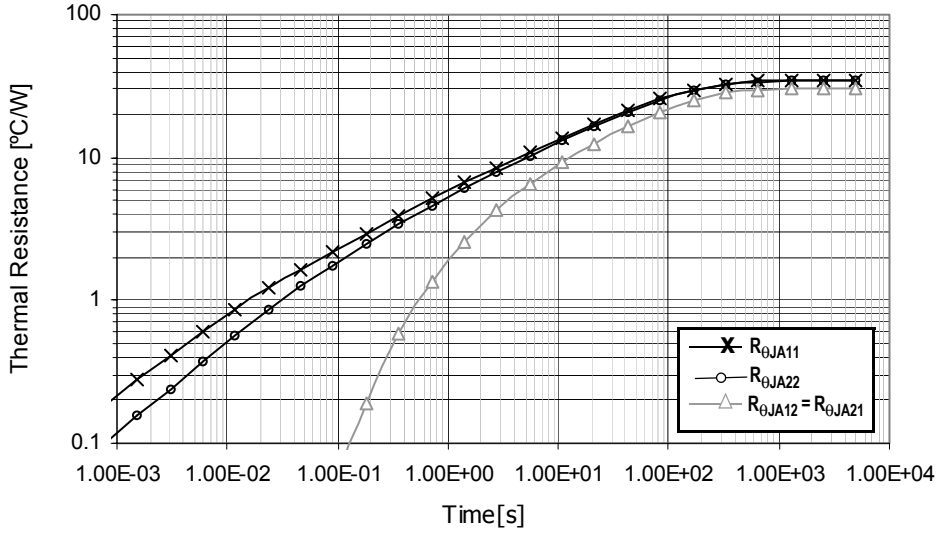


**Figure 39. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)**

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