January 7, 2011

PSoC® 3: CY8C34 Family Errata Silicon Revision ES2 (Datasheet Document Number: 001-53304 Rev. *H)

This document describes the preliminary errata for the PSoC 3: CY8C34 Family silicon revision ES2. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Compare this document to the device's datasheet for a complete functional description.

ES2 is marked on the package as part of the device number. See the examples below. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
CY8C3446AXI-099ES2
CY8C3446LTI-085ES2
CY8C3446LTI-075ES2

PSoC 3: CY8C34 Family Qualification Status

-40 °C to 85 °C Functionality.

Specifications only applicable when operating with ES2 silicon.

PSoC 3: CY8C34 Family Errata Summary

The following table defines the errata applicability to available PSoC 3: CY8C34 Family of devices.

Note Errata items in the table below are hyperlinked. Click on any item entry to jump to its description.

Items	Part Number	Silicon Revision	Fix Status
1. Electrical Specifications	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
2. Device Features	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
3. Device Function	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
4. Brown Out	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
5. Delta Sigma ADC Range	All ES2 Parts Affected	ES2	Fix Confirmed in ES2[1]
6. Delta Sigma ADC Output Count	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
7. Delta Sigma ADC End-of-Conversion	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
8. Delta Sigma ADC Gain	All ES2 Parts Affected	ES2	Fix Confirmed in ES2[1]
9. Delta Sigma ADC Routing	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
10. MHz Oscillator Reliability	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
11. MHz Oscillator Startup	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
12. MHz External Crystal Oscillator Voltage	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
13. WDT Does Not Work in Low Power Modes	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
14. WDT Cleared Once, Does Not Time Out	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
15. Comparator Wakeup	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
16. Comparator Enable	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
17. LVD and Comparator Interrupt Level	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
18. UDB Low Power Retention	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
19. Low Power Mode and JTAG/SWD	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
20. Power System Initialization	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon

[1] See full errata text for additional information and greater detail regarding fix status.

Items	Part Number	Silicon Revision	Fix Status
21. Sleep Request and IRQ	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
22. Analog Low Power Routing	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
23. SWD Clock	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
24. SWD ACK	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
25. SWO Pin	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
26. JTAG/SWD XRES Requirement	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
27. Configurable XRES Pin	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
28. 68-Pin QFN Boost Circuit	CY8C3446LTI-085ES2	ES2	Fix Confirmed in ES2[1]
29. Segment LCD Vddio Restriction	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
30. Analog Connectivity	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
31. Analog Routing	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
32. VIDAC0 Operation	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
33. VDAC Output	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
34. VDAC/IDAC Strobe	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
35. IDAC Current Consumption	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
36. IDAC and Analog Global Performance	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
37. SIO Increased Current Consumption	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
38. SIO Port Registers	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
39. I/O Pin Configuration	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
40. Interrupts	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
41. Fixed Function Timer Capture	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
42. Fixed Function Timer ISR	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
43. USB EP0 Transaction Failures	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
44. USB Bus Clock	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
45. USB Suspend	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
46. USBIO Used as GPIO	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
47. Power Mode: I2C Available	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
48. I2C Clocking	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
49. Reading ECC	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
50. Enabling ECC in Firmware	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
51. SPC Checksum Failure	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
52. DMA Intraspoke Bursts	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
53. CAN Conformance	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon
54. Opamp Buffering of VREF	All ES2 Parts Affected	ES2	Fix Confirmed in Production Silicon

[1] See full errata text for additional information and greater detail regarding fix status.

1. Electrical Specifications

■ PROBLEM DEFINITION

The listed parameters do not meet their electrical specifications. A quick summary is provided below.

- ESD human body model is below specification.
- Maximum current per VDDIO supply pin is below specification.
- Active power exceeds specification.
- Device wake from sleep time is approximately twice as long as datasheet specification.
- VBAT has a minimum voltage of 1.8 V.
- DelSig ADC input offset voltage exceeds specification when using level shift buffer.
- 1.024 V reference error exceeds 0.1%.
- IDAC linearity and error exceed specification.
- Mixers input offset voltages are double the datasheet specification.
- TIA bandwidth is decreased when VDDA is below 1.9 V.
- PGA gain error exceeds specification.
- Temperature sensor accuracy does not meet specification.
- LCD subsystem exceeds power specifications.
- Nonvolatile latches must be programmed at 1.8 V.
- IMO clock sources exceed frequency error tolerance.

- **PARAMETERS AFFECTED**

Module	Parameter and Description	Conditions	DC Specifications			ES2 Specifications Units	Units
			Min	Typ	Max		
Absolute Max DC Specifications, Table 11-1	ESD_{HBM}, Electro-Static Discharge Voltage	Human Body Model	750	–	–	500	V
	I_{vddio}. Current per VDDIO supply pin		–	–	100	20	mA
DC Specifications, Table 11-2	IDD, Execute from Flash, CPU at 3 MHz	T = -40 °C	–	–	–	–	mA
		T = 25 °C	–	0.8	–	1.13	mA
		T = 80 °C	–	–	–	–	mA
	IDD, Execute from Flash, CPU at 6 MHz	T = -40 °C	–	–	–	–	mA
		T = 25 °C	–	1.2	–	2.89	mA
		T = 80 °C	–	–	–	–	mA
	IDD, Execute from Flash, CPU at 12 MHz	T = -40 °C	–	–	–	–	mA
		T = 25 °C	–	2.0	–	5.46	mA
		T = 80 °C	–	–	–	–	mA
	IDD, Execute from Flash, CPU at 24 MHz	T = -40 °C	–	–	–	–	mA
		T = 25 °C	–	3.5	–	8.00	mA
		T = 80 °C	–	–	–	–	mA
	IDD, Execute from Flash, CPU at 50 MHz	T = -40 °C	–	–	–	–	mA
		T = 25 °C	–	6.6	–	12.48	mA
		T = 80 °C	–	–	–	–	mA
	IDD, Execute from Flash, CPU at 67 MHz	T = -40 °C	–	–	–	–	mA
		T = 25 °C	–	9.0	–	20.33	mA
		T = 80 °C	–	–	–	–	mA
AC Specifications, Table 11-3	Tsleep, Wakeup from sleep mode (non LVD interrupt)		–	–	12	Typical:20	µs
Inductive Boost Regulator DC Specifications, Table 11-6	VBat, Input Voltage	Includes Setup	0.5	–	5.5	Minimum: VBat > 1.8 V	V
12-bit Delta-sigma ADC DC Specifications, Table 11-19	Vos ADC, ADC Input offset voltage		–	–	±0.1	±0.5	mV
Voltage Reference Specifications, Table 11-22	VREF, Precision reference voltage	Initial Trimming	1.023 (-0.1%)	1.024	1.025 (+0.1%)	Min = 1.017 (-0.7%), Max = 1.033 (+0.9%)	V

Module	Parameter and Description	Conditions	DC Specifications			ES2 Specifications Units	Units
			Min	Typ	Max		
IDAC DC Specifications, Table 11-26	INL, Integral Non-Linearity	Sink Mode, range = 255 µA, Codes 8-255, Rload = 2.4kΩ, Cload = 15 pF	–	±1.2	±1.5	±3.0	LSB
		Source Mode, range = 255 µA, Codes 8-255, Rload = 2.4kΩ, Cload = 15 pF	–	±0.9	±1.0	±3.0	LSB
	DNL, Differential Non-Linearity	Sink Mode, range = 255 µA, Rload = 2.4kΩ, Cload = 15 pF	–	±0.3	±0.5	±1.6 (Non Monotonic)	LSB
		Source Mode, range = 255 µA, Rload = 2.4kΩ, Cload = 15 pF	–	±0.3	±0.5	±1.6 (Non Monotonic)	LSB
	Ezs, Zero Scale Error		–	0	±1	±2.5	LSB
	Eg, Gain Error		–	–	3.5	5	%
Mixer DC Specifications, Table 11-30	V_{OS}, Input Offset Voltage		–	–	10	20	mV
TIA AC Specifications, Table 11-33	BW, Input Bandwidth (-3dB)	R = 20K; –20 pF load	1600	–	–	<1800 for Vdda < 1.9 V, 1800 for Vdda ≥ 1.9 V	kHz
		R = 120K; –20 pF load	240	–	–	<330 for Vdda < 1.9 V, 330 for Vdda ≥ 1.9 V	kHz
		R = 1M; –20 pF load	25	–	–	<47 for Vdda < 1.9 V, 47 for Vdda ≥ 1.9 V	kHz
		R = 20K; –40 pF load	1500	–	–	<1500 for Vdda < 1.9 V, 1500 for Vdda ≥ 1.9 V	kHz
		R = 120K; –40 pF load	240	–	–	<300 for Vdda < 1.9 V, 300 for Vdda ≥ 1.9 V	kHz
		R = 1M; –40 pF load	25	–	–	<46 for Vdda < 1.9 V, 46 for Vdda ≥ 1.9 V	kHz
PGA DC Specifications, Table 11-34	Ge1, Gain Error at gain = 1	Vdda = 5 V	–	–	±0.15	±0.61	%
	Ge16, Gain Error at gain = 16	Vdda = 5 V	–	–	±2.5	±6.06	%
	Ge50, Gain Error at gain = 50	Vdda = 5 V	–	–	±5	±9	%
Temperature Sensor, Table 11-36	Temp Sensor Accuracy	Range: –40 to +85 °C	–	±5	–	±8	°C

Module	Parameter and Description	Conditions	DC Specifications			ES2 Specifications Units	Units
			Min	Typ	Max		
LCD Direct Drive DC Specifications, Table 11-37	Icc_{LCD} operating current	16x4 segment display at 50 Hz	–	19	–	63	µA
	Icc_{LCD}, LCD system operating current	Static; Vbias = 5 V, Number of LCD pins: 33 (32x1), Number of segments: 32	–	12	–	131	µA
	Icc_{LCD}, LCD system operating current	Static; Vbias = 3 V, Number of LCD pins: 33 (32x1), Number of segments: 32	–	10	–	111	µA
	Icc_{LCD}, LCD system operating current	¼ duty; Vbias = 5 V, Number of LCD pins: 36 (32x4), Number of segments: 128	–	24	–	188	µA
	Icc_{LCD}, LCD system operating current	¼ duty; Vbias = 3 V, Number of LCD pins: 36 (32x4), Number of segments: 128	–	21	–	165	µA
	Icc_{LCD}, operating current	1/16 duty; Vbias = 5 V, Number of LCD pins: 48 (32x16), Number of segments: 512	–	93	–	458	µA
	Icc_{LCD}, LCD system operating current	1/16 duty; Vbias = 3 V, Number of LCD pins: 48 (32x16), Number of segments: 512	–	83	–	419	µA
NVL DC Specifications, Table 11-55	Erase and program voltage	Vddd pin	1.71	–	5.5	1.71 Minimum, 1.89 Maximum	V
IMO AC Specifications, Table 11-74	F_{IMO} Frequency Stability, 24 MHz (Non USB Mode)		-4	–	4	±6	%
	F_{IMO} Frequency Stability, 24 MHz (USB Mode)	With oscillator locking to USB bus	-0.25	–	0.25	±6	%
	F_{IMO} Frequency Stability, F_{IMO} = 12 MHz		-3	–	3	±6	%
	F_{IMO}O Frequency Stability, F_{IMO} = 6 MHz		-2	–	2	±4	%
	F_{IMO} Frequency Stability, F_{IMO} = 3 MHz		-1	–	1	±4	%

- **TRIGGER CONDITION(S)**
  NA
- **SCOPE OF IMPACT**
  NA
- **WORKAROUND**
  The errata specifications for ES2 silicon are provided to assist in working around system design issues.
- **FIX STATUS**
  Silicon revision fix for all electrical specification errata confirmed in production silicon.

2. Device Features

- **PROBLEM DEFINITION**

  The following features are not available. They are disabled by default.
  Keep in their disabled state.

  - External Memory Interface (EMIF)
  - JTAG Boundary Scan
  - USB memory management mode: Mode 3 (automatic memory management with automatic DMA access) in USB. See the *PSoC 3: CY8C34 Family Datasheet* for details
  - Trace
  - Segment locking of configuration registers
  - Temperature sensor in ES2 silicon prior to date code 1005
  - External MHz Oscillator (not to be used for production)
  - I^2C Hardware Address Match
  - DMA Transaction Descriptor 0xFE

  - **PARAMETERS AFFECTED**

  NA

- **TRIGGER CONDITION(S)**

  NA

- **SCOPE OF IMPACT**

  NA

- **WORKAROUND**

  NA

- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

3. Device Function

- **PROBLEM DEFINITION**

  For the following functions, the hardware requires specific register settings and sequences to operate properly. APIs are provided that implement the specific code sequences required for this version of the silicon.

  - Delta Sigma ADC
  - USB
  - Clocking
  - EEPROM

- **PARAMETERS AFFECTED**

  NA

- **TRIGGER CONDITION(S)**

  NA

- **SCOPE OF IMPACT**

  NA

- **WORKAROUND**

  Use Cypress-generated APIs for listed functions instead of writing directly to the registers.

- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

4. Brown Out

- **PROBLEM DEFINITION**

  The brown out detection circuit on ES2 silicon does not function properly and is unable to guarantee brown out detection in both active and sleep power modes.

- **TRIGGER CONDITIONS**

  Vcca, Vccd, Vdda, Vddd voltage below 1.71 V.

- **SCOPE OF IMPACT**

  The device will reset on a brown out condition, but the brown out threshold may be too low to guarantee device function. Device state and data retention are not guaranteed which may result in improper code execution and device function.

- **WORKAROUND**

  There are several possible workarounds. These workarounds are not required for prototyping at room temperature (25 °C).

  1. Externally guarantee that all supply voltages do not fall below 1.8 V when regulated and 1.71 V when unregulated. If operating in sleep mode, use a Schottky diode to clamp Vdda to Vcca by connecting the diode cathode to Vdda
  2. Provide external voltage monitoring circuitry to reset the device in the event that Vdda or Vddd drop below 1.8 V when regulated and 1.71 V when unregulated. One possible implementation for regulated mode is to use a 2.2 V supervisor device. In unregulated mode, there is insufficient margin to use a voltage monitoring circuit to implement this workaround. If JTAG interface is enabled, the workaround will not reset the device and may not be used
  3. Use the Low Voltage Interrupt (LVI) setting LVI_A/D_SEL[3:0] = 0001b for 1.95 V or higher voltage to detect that the Vdda and Vddd supplies have dropped below the threshold. Ensure sufficient bulk capacitance to guarantee that the CPU can service the interrupt and perform a hardware reset. Hardware reset is performed by writing 0x00 to register RESET_IPOR_CR0 (0x46F0). In unregulated mode, there is insufficient margin to use the LVI 1.701 voltage detection level to implement this workaround

- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

5. Delta Sigma ADC Range

- **PROBLEM DEFINITION**

  When using the Delta Sigma ADC, the maximum useable input into the ADC is 90% of the reference value.

- **PARAMETERS AFFECTED**

  NA

- **TRIGGER CONDITIONS**

  Using the Delta Sigma ADC.

- **SCOPE OF IMPACT**

  An input into the ADC greater than 90% of the reference value results in increased noise, which produces inaccurate results.

- **WORKAROUND**

  There are two possible workarounds.

  1. If possible, increase external reference voltage so that the input voltage does not exceed 90% of reference value
  2. Attenuate the input signal so that it never exceeds 90% of the reference value

- **FIX STATUS**

  Silicon revision fix confirmed in ES2 with date code 1026 or later in conjunction with PSoC Creator Beta 5 release.

6. Delta Sigma ADC Output Count

- **PROBLEM DEFINITION**

  The Delta Sigma ADC outputs a count value symmetrical about 0, resulting in 2^n+1 counts rather than 2^n. If the result is truncated to n bits, the maximum count is the same as the minimum count. It is interpreted as the minimum count creating a discontinuity. For example, if you configure the ADC for an 8-bit result, you expect values between 0x80 and 0x7F (-128 to +127). Instead the range is 0x80 to 0x80 (-128 to -128).

- **PARAMETERS AFFECTED**

  NA

- **TRIGGER CONDITION(S)**

  NA

- **SCOPE OF IMPACT**

  All Delta Sigma ADC conversions.

- **WORKAROUND**

  Two workarounds are possible. The recommended workaround is to read and use at least one more bit of resolution from the ADC than the configured conversion requires. The extra bit ensures that the sign is properly accounted for. For 6 and 7 bit conversions read an int8 value, for 8 to 12 bit conversions read an int16 value. The second workaround is to ensure that the maximum count value is never reached by the ADC in the end application.

- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

7. Delta Sigma ADC End-of-Conversion

- **PROBLEM DEFINITION**

  End-of-Conversion (EOC) is signaled by a status register bit, decimator interrupt, decimator DMA, and DSI routable signal. The DSI routable signal does not work. The CPU can poll the status register bit or use the decimator interrupt or decimator DMA.

- **PARAMETERS AFFECTED**

  NA

- **TRIGGER CONDITION(S)**

  NA

- **SCOPE OF IMPACT**

  The ADC End-of-Conversion (EOC) output of the PSoC Creator component can only be used to route to one DMA channel. The EOC output cannot be used to route through the DSI routing to any other digital resources. The decimator DMA route bypasses the DSI routing avoiding this issue. The decimator interrupt integrated into the PSoC Creator component also bypasses the DSI routing. All other possible EOC connections require DSI routing.

- **WORKAROUND**

  The CPU can poll the EOC bit in the status register or use the decimator interrupt to signal the digital system using firmware and a control register.

- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

8. Delta Sigma ADC Gain

- **PROBLEM DEFINITION**
  Gain compensation trim values are not provided in the silicon. This results in gain errors when using the Delta Sigma ADC and a reduction in usable range.
- **TRIGGER CONDITION(S)**
  Using the Delta Sigma ADC.
- **SCOPE OF IMPACT**
  Gain errors of less than 1% are typically found. However, gain errors up to 2% are possible.
- **WORKAROUND**
  Manually calibrate the ADC using the ADC_SetGain() API provided in the DeltaSigma ADC component datasheet. A known external reference voltage is required to be provided in order to perform this calibration.
- **FIX STATUS**
  Silicon revision fix confirmed in ES2 with date code 1042 or later in conjunction with PSoC Creator Beta 5 release.

9. Delta Sigma ADC Routing

- **PROBLEM DEFINITION**
  The positive input mux to the Delta Sigma ADC does not include a connection to the AMUX Bus. The negative input mux incorrectly connects to the AMUX Bus. See the *PSoC 3: CY8C34 Family Technical Reference Manual* for details.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  NA
- **SCOPE OF IMPACT**
  The Delta Sigma ADC cannot be directly connected to the AMUX Bus for single-ended ADC conversions.
- **WORKAROUND**
  The positive input mux of the Delta Sigma ADC may be connected to a Global Mux Bus, which in turn may connect to the AMUX Bus through one of the other analog resource's input muxes. The use of another analog resource's mux for this routing connection may limit the use of that resource. PSoC® Creator™ software automatically works around this errata if hardware resources allow.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

10. MHz Oscillator Reliability

- **PROBLEM DEFINITION**
  The MHz oscillator contains a design weakness that causes it to function outside datasheet specifications if Vdda is greater than 1.8 V. This weakness is not immediately present on new devices. The issue manifests over a period of time ranging from a few months to several years. The exact time to failure varies from device to device. This applies only when prototyping. MHz oscillator is not to be used in production.
- **TRIGGER CONDITION(S)**
  Vdda greater then 1.8 V when the ECO MHz oscillator is enabled.
- **SCOPE OF IMPACT**
  The MHz oscillator failure mode ranges from increased current in low power modes of approximately 10 µA, up through complete non functionality of the ECO MHz oscillator. The exact failure mode varies from device to device.
- **WORKAROUND**
  None. MHz oscillator not to be used in production.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

11. MHz Oscillator Startup

- **PROBLEM DEFINITION**

  The MHz oscillator has reduced average gain; this results in startup failures in some devices with gain on the lower end of the distribution. This applies only when prototyping. MHz oscillator is not to be used in production.

- **TRIGGER CONDITION(S)**

  Starting the external MHz crystal.

- **SCOPE OF IMPACT**

  The oscillator is unable to start the external crystal. Additionally, the XERR bit in the MHz ECO register XMHZ_CSR[7] does not report error conditions correctly. If an error occurs the XERR bit will not reflect the error condition.

- **WORKAROUND**

  Two workarounds are available for startup issues. These workarounds apply only when prototyping. MHz oscillator is not to be used in production.

  1. Use a low ESR crystal in design. This is not guaranteed to correct startup issues in all cases
  2. Contact Cypress to request replacement samples

- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

12. MHz External Crystal Oscillator Voltage

- **PROBLEM DEFINITION**

  The MHz External Crystal Oscillator (MHz ECO) used to drive an external MHz crystal does not function when Vdda is below 2.0 V.

- **PARAMETERS AFFECTED**

  NA

- **TRIGGER CONDITION(S)**

  Vdda < 2.0 V with External Crystal Oscillator enable.

- **SCOPE OF IMPACT**

  This issue results in the MHz oscillator only functioning for Vdda > 2.0.

- **WORKAROUND**

  1. If possible run the device at Vdda ≥ 2.0 V
     a) Directly increase the Vdda supply to ≥ 2.0 V
     b) Use the Inductive Boost Pump to increase the Vdda supply to ≥ 2.0 V
  2. If MHz crystal accuracy is required with Vdda below 2.0 V an external crystal and oscillator can be used to route a digital clock into the device through the Digital Clock Source in PSoC Creator
  3. Use the IMO (and PLL if required) with 1% accuracy

- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

13. WDT Does Not Work in Low Power Modes

- **PROBLEM DEFINITION**
  The Watchdog Timer (WDT) does not work in low power modes (Sleep and Hibernate).
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  NA
- **SCOPE OF IMPACT**
  The WDT will not reset the device during low power modes. The device will stay in the low power mode and stop responding to all other stimulus if a WDT reset occurs in the low power mode.
- **WORKAROUND**
  1. Do not use the WDT and low power modes in the same application
  2. If low power modes and the WDT must be used in the same application, ensure that the device wakes from the low power mode and the WDT is serviced before a WDT reset can occur
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

14. WDT Cleared Once, Does Not Time Out

- **PROBLEM DEFINITION**
  If the Watchdog Timer (WDT) is cleared once, it does not time out.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  NA
- **SCOPE OF IMPACT**
  The WDT will not reset the device after it has been cleared.
- **WORKAROUND**
  After each watchdog clear operation performed by writing WDT_CR (0x4384); also immediately write a zero to WDT_CFG(0x4383).
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

15. Comparator Wakeup

- **PROBLEM DEFINITION**
  The device is unable to wake from sleep when trigged by a comparator.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Using the comparator to wake the chip from a sleep to an active state.
- **SCOPE OF IMPACT**
  Comparator is unable to wake the device from sleep.
- **WORKAROUND**
  There are two possible workarounds:
  1. Low Offset Workaround: Add an external comparator device and connect its digital output to a GPIO pin configured for wake on interrupt
  2. Internal Workaround: Configure an SIO and GPIO pin to act as a comparator using the SIO pin in differential mode and the GPIO pin to route in the differential signal reference for the SIO. See Cypress Application Note AN60580 for information on how to implement a comparator with SIO
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

16. Comparator Enable

- **PROBLEM DEFINITION**
  The LSB of the Active Power Mode Configuration Register (PM_ACT_CFG7, 0x43A7), which is used to enable the comparators on a PSoC device have bits 1 and 2 reversed. Bit 1 controls comparator 2 and bit 2 controls comparator 1.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Enabling comparator 1 and comparator 2 using the PM_ACT_CFG7 (0x43A7).
- **SCOPE OF IMPACT**
  None.
- **WORKAROUND**
  PSoC Creator implements the required software workaround. When writing to these registers directly, write to bit 1 to control comparator 2 and write to bit 2 to control comparator 1.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

17. LVD and Comparator Interrupt Level

- **PROBLEM DEFINITION**
  The LVD and comparator interrupts only support level trigger mode. Setting the LVD and comparator interrupt modes to edge mode has no effect. See the *PSoC 3: CY8C34 Family Technical Reference Manual* for details.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  NA
- **SCOPE OF IMPACT**
  An LVD or comparator interrupt keeps interrupts pending, because they are level triggered, until the LVD or comparator output changes to the inactive state.
- **WORKAROUND**
  The LVD and comparator signals are routed out to GPIOs through the Digital System Interconnect (DSI) and brought back in as GPIO interrupts, which are edge triggered.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

18. UDB Low Power Retention

- **PROBLEM DEFINITION**
  When the device enters a low power mode (sleep or hibernate), the following register values are not retained.
  - UDB[00..15]_D0
  - UDB[00..15]_D1
  - UDB[00..15]_CTL
  - UDB[00..15]_MSK
  - UDB[00..15]_ACTL
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Entering one of the device low power modes while using a UDB based component.
- **SCOPE OF IMPACT**
  The register values are not retained upon wakeup. The UDB based component will not function in the same manner as prior to entering the low power mode.
- **WORKAROUND**
  Preserve each of the registers value by storing in SRAM prior to entering a low power mode. Upon wakeup, restore register values to proper location. Because component placement can change between each build, Cypress recommends using the component `#defines` located in the *component.h* file, rather than absolute register names. In the following example, preserve and restore PWM_1_COMPARE1_LSB.
  ```
  #define PWM_1_COMPARE1_LSB     (*(reg8 *) PWM_1_PWMUDB_sP8_pwmdp_u0__D0_REG)
  ```
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon. Workaround for ES2 fix available in PSoC Creator Beta 5.

19. Low Power Mode and JTAG/SWD

- **PROBLEM DEFINITION**
  If the JTAG/SWD interfaces are enabled, the device does not enter any of the low power modes.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  JTAG/SWD interface enabled.
- **SCOPE OF IMPACT**
  If either the JTAG/SWD interface is enabled and a low power mode is entered, the low power mode is skipped and the device continues to operate in the active mode.
- **WORKAROUND**
  None.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

20. Power System Initialization

- **PROBLEM DEFINITION**
  The Central Timewheel (CTW) is not automatically enabled in low power modes. See the *PSoC 3: CY8C34 Family Technical Reference Manual* for details. If sleep low power mode is entered and if the central timewheel is not already enabled, increased wake times or low voltage reset may occur.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Entering sleep low power mode.
- **SCOPE OF IMPACT**
  If sleep low power mode is entered and if the central timewheel is not already enabled, the low power regulators will not be powered, which results in either increased wake times or low voltage reset.
- **WORKAROUND**
  Enable and use the central timewheel (register bit value PM.TW_CFG2[2] = ‘1’ in *PSoC 3: CY8C34 Family Technical Reference Manual*) prior to entering sleep low power mode. Central timewheel time settings are not critical.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

21. Sleep Request and IRQ

- **PROBLEM DEFINITION**
  When a simultaneous sleep or hibernate request and IRQ is generated, the CPU halts and prevents further code execution without entering a lower power mode.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  When a sleep request and IRQ is triggered simultaneously.
- **SCOPE OF IMPACT**
  CPU is halted and further code execution is prevented.
- **WORKAROUND**
  Use the WDT to recover the CPU. This workaround does not conflict with workaround from errata item "WDT Does Not Work in Low Power Modes" as the device does not enter a low power mode.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

22. Analog Low Power Routing

- **PROBLEM DEFINITION**

  Placing the device into sleep or hibernate mode, calling Stop() APIs for the DeltaSigma ADC, or not calling Start() APIs for the DeltaSigma ADC component causes the analog components connections to the analog global to lose their high impedance state and can cause undesirable shorts of the analog routing to either GND, Vdd, or to each other. This issue affects the Comparator, VIDAC, SC/CT, and DeltaSigma Modulator ADC (DSM). This issue affects both direct connections to analog resources and analog routing which use the DSM for track jumping.

- **PARAMETERS AFFECTED**

  NA

- **TRIGGER CONDITION(S)**

  Placing the device into sleep or hibernate modes, calling Stop() API's for the DeltaSigma ADC, or not calling Start() API for DeltaSigma ADC.

- **SCOPE OF IMPACT**

  Depending on the analog component, the result can consist of the analog global shorting together, shorting to GND, or shorting to Vdda. This may impact external circuitry attached to the affected blocks and have an effect on analog accuracy. The impact of the issue is application dependent.

- **WORKAROUND**

  There are two possible workarounds:

  1. Do not use sleep or hibernate mode on the device and place then enable the DeltaSigma ADC of the device to avoid shorting of the analog globals. This prevents the analog router from using the DeltaSigma ADC inputs for track jumping of other analog resources..
  2. If sleep or hibernate mode is required, place analog mux components in PSoC Creator in-between the analog pins and the connections to the analog components. The analog mux connections must be made directly to the analog component inputs. Before entering a low power mode, disconnect the inputs from the components using the analog mux to prevent the affected components from affecting the design.

- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

23. SWD Clock

- **PROBLEM DEFINITION**

  When using SWD via the USBIO to acquire, program, or debug the device, the P1[1] SWDCK pin must be pulled to ground when using the USB SWDCK pin (P15[7]).

- **PARAMETERS AFFECTED**

  NA

- **TRIGGER CONDITION(S)**

  The SWDCK pin on P1[1] in a high logic state.

- **SCOPE OF IMPACT**

  SWD clock will not be seen by SWD interface on device.

- **WORKAROUND**

  Ensure that the P1[1] SWDCK pin is pulled to ground when using the USBIO for SWD. The easiest method is to tie the P1[1] SWDCK pin to ground with a 100 K resistor.

- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

24. SWD ACK

- **PROBLEM DEFINITION**
  When reading the acknowledge response of a SWD transaction, an ACK will return a '011b' value rather then the expected '001b'. A value of '011b' traditional means a parity error, however in ES2 silicon revision '011b' signifies an acknowledgment.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Reading the acknowledge response packet of a SWD transfer.
- **SCOPE OF IMPACT**
  NA
- **WORKAROUND**
  If a value of '011b' is returned from a SWD transaction, treat it as an acknowledge and not a data error.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

25. SWO Pin

- **PROBLEM DEFINITION**
  When the device is configured with Single Wire Debug (SWD) as the debug port, P1[3] is automatically configured for SWO and cannot be used as a GPIO.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Configuring the device to use SWD as the debug port.
- **SCOPE OF IMPACT**
  Unable to use P1[3] as a GPIO.
- **WORKAROUND**
  NA
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

26. JTAG/SWD XRES Requirement

- **PROBLEM DEFINITION**
  Device reset cannot be done through the JTAG/SWD interface.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Attempts to execute a software reset through the JTAG/SWD interface.
- **SCOPE OF IMPACT**
  NA
- **WORKAROUND**
  Two workarounds are available:
  1. For 100-pin and 68-pin devices, do not use the Configurable XRES pin, only use the dedicated XRES pin. The dedicated XRES pin is not affected by reads of the CNVL_XRESMEN bit.
  2. For 48 pin devices, always configure the GPIO XRES pin P1[2] to pull-up drive mode before reading the XRES NVL bit using the spc_nvl_read command. This is done by writing 0x05 to PRT1_PC2 register (0x500 A). This will apply a 5 kO pull-up to the pin, which may have an effect on circuitry attached to the pin. PSoC Creator Beta 3 implements the required workaround when programming the device.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

27. Configurable XRES Pin

- **PROBLEM DEFINITION**
  When reading the NV Latches, the CNVL_XRESMEN bit glitches to '0', thus resetting the device if the configurable XRES pin is enabled.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Reading the status of the XRES NVL.
- **SCOPE OF IMPACT**
  None.
- **WORKAROUND**
  Two workarounds are available:
  1. For 100-pin and 68-pin devices, do not use the Configurable XRES pin, only use the dedicated XRES pin. The dedicated XRES pin is not affected by reads of the CNVL_XRESMEN bit
  2. For 48-pin devices, always configure the GPIO XRES pin P1[2] to pull-up drive mode before reading the XRES NVL bit using the spc_nvl_read command. This is done by writing 0x05 to PRT1_PC2 register (0x500A). This will apply a 5 kΩ pull-up to the pin, which may have an effect on circuitry attached to the pin. PSoC Creator Beta 3 implements the required workaround when programming the device
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

28. 68-Pin QFN Boost Circuit

- **PROBLEM DEFINITION**
  The 68-pin QFN package of ES2 devices have Vbat and Vboost shorted together.
- **TRIGGER CONDITION(S)**
  None.
- **SCOPE OF IMPACT**
  Vboost circuit does not function and supply will be shorted if Vbat is connected to GND and Vboost is connected to supply voltage.
- **WORKAROUND**
  Do not use the Vboost feature of the chip and ground both Vbat and Vboost as detailed in Section 2 of the *CY8C34 family datasheet*.
- **FIX STATUS**
  Silicon revision fix confirmed in ES2 with date code 1026 or later.

29. Segment LCD Vddio Restriction

- **PROBLEM DEFINITION**
  If segment LCD drive is enabled, then all Vddio supplies must be greater than or equal to the LCD bias voltage (Vbias = V0).
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Vddio0, Vddio1, Vddio2, or Vddio3 less than LCD bias (Vbias) when segment LCD drive is enabled.
- **SCOPE OF IMPACT**
  If a Vddio supply is less than the LCD bias voltage (Vbias), the LCD bias voltage will be clamped to the lowest Vddio supply voltage.
- **WORKAROUND**
  Ensure all Vddio supplies are ≥ LCD bias (Vbias). If the application requires digital pins to be driven to a voltage less than Vbias, the SIO pins can be used in regulated output mode and GPIO pins can be configured for open drain, drives low mode, and driven high with a pull-up to the required voltage.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

30. Analog Connectivity

- **PROBLEM DEFINITION**
  Vbat, Vddd, and Vdda are not directly routable to analog globals.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  NA
- **SCOPE OF IMPACT**
  NA
- **WORKAROUND**
  Connect the supply rail to be measured to a GPIO and then route that I/O to an analog global. The supply rail to be measured must be less than or equal to the GPIO pins VDDIO supply.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

31. Analog Routing

- **PROBLEM DEFINITION**
  The SC/CT hardware blocks have reversed input connections. This issue only applies when performing manual analog routing with direct register writes.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  NA
- **WORKAROUND**
  Use PSoC Creator to route these hardware modules. PSoC Creator currently implements the required workaround. No user intervention is required.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

32. VIDAC0 Operation

- **PROBLEM DEFINITION**

  VIDAC0 does not operate correctly when its output is greater than 2.4 V in either voltage or current mode.

- **PARAMETERS AFFECTED**

  NA

- **TRIGGER CONDITION(S)**

  Use of VIDAC0 with an output voltage greater than 2.4 V.

- **SCOPE OF IMPACT**

  Output of VIDAC0 does not meet specifications and cannot output a voltage greater than 2.4 V. VDAC1, VDAC2, and VDAC3 are not affected.

- **WORKAROUND**

  Two workarounds are possible:

  1. Do not use any VDACs or IDACs whose output voltage can exceed 2.4 V.
  2. If one or more VDACs or IDACs must be used with outputs exceeding 2.4 V, several user steps are required to determine if they are placed into VIDAC0 and must be moved to other VIDAC hardware if required.
     a) After each build of the project, open the report file (*.rpt) located in the Results tab of the Workspace Explorer of PSoC Creator
     b) Expand the 'Analog component placement' branch in the *.rpt file and look for a line that begins with VIDAC[0]. If no line begins with VIDAC[0], the errata workaround is complete because VIDAC0 was not used in the design
     c) If a line beginning with VIDAC[0] such as "VIDAC[0]@[Chip=0][FFB(VIDAC,0)]: \VDAC8_1:viDAC8\ (fixed)" is present, examine the component instance name (VDAC8_1 in this example). If the component with this instance name does not experience an output voltage greater than 2.4 V the errata workaround is complete
     d) If the component with this instance name does require an output greater than 2.4 V, copy the full instance name with slashes (example: \VDAC8_1:viDAC8\)
     e) Open the projects design wide resource (*.cydwr) file and open the directives tab. Click the add directive icon
     f) Paste the full instance name copied from the report file into the "Component (Signal) Name” column
     g) In the "Directive Type" column select "ForceComponentFixed"
     h) In the "Directive Value" column type in the following text "f(vidac,1)" where the numeric parameter is the VIDAC resource to use (VIDAC1 in this example). This directive forces the component to be placed into a specific VIDAC hardware resource
     i) Several iterations may be required to ensure no VDACs or IDACs are placed in VIDAC0 with outputs greater than 2.4 V

- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

33. VDAC Output

- **PROBLEM DEFINITION**
  VDAC output produces a glitch of up to 100 ns on every DAC output update.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITIONS(S)**
  DAC output update.
- **SCOPE OF IMPACT**
  VDAC output produces a glitch on every DAC update. Update occurs on a CPU write or DSI strobe signal. The glitch is noticed more prominently when it is buffered (due to the low output impedance of the buffer).
- **WORKAROUND**
  Glitches cannot be completely eliminated with a workaround. Glitches can be reduced by not buffering the VDAC output or by adding capacitance to the output to filter the glitches. The glitch filter should be comprised of a low pass filter with a cut off frequency below 1 MHz.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

34. VDAC/IDAC Strobe

- **PROBLEM DEFINITION**
  On each write to the VDAC/IDAC the DAC outputs the previously written data causing a one write delay to the DAC output.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Writing new output data to the VDAC/IDAC.
- **SCOPE OF IMPACT**
  The VDAC/IDAC always outputs the previously written data for firmware updates. For hardware updates, the hardware strobe always outputs the previously strobed data. The interface appears as if it has a two stage pipeline between data writes/strobes and the DAC output.
- **WORKAROUND**
  Write (firmware) or strobe (hardware) the VDAC/IDAC twice with each update insuring the current data is output form the DAC. DMA also requires two writes to update the DAC which can be achieved by chaining two identical DMA Transaction Descriptors (TDs). The firmware workaround is already implemented in both VDAC and IDAC Component Write APIs in PSoC Creator.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

35. IDAC Current Consumption

- **PROBLEM DEFINITIO**

  Using a VIDAC in IDAC mode causes an increase in current consumption of approximately 1 mA in the chip due to setting of the IDAC bit. The CapSense component, which includes an embedded IDAC exhibits the same symptoms. Calling the Start API sets the bit. Calling the Stop API does not clear the bit.
- **PARAMETERS AFFECTED**

  NA
- **TRIGGER CONDITION(S)**

  Starting a IDAC by setting the DAC_MODE_ENUM bit located in the DAC[0..3]_CR0 register (0x5820).
- **WORKAROUND**

  NA
- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

36. IDAC and Analog Global Performance

- **PROBLEM DEFINITION**

  Enabling an IDAC by calling the start API in either a IDAC component or CapSense component as it intergrates an IDAC results in leakage from Vdda to ground on analog globals AGR[3], AGR[7], AGL[3], and AGL[7].
- **PARAMETERS AFFECTED**

  NA
- **TRIGGER CONDITION(S)**

  Starting an IDAC by setting the DAC_MODE_ENUM bit located in the DAC[0..3]_CR0 register (0x5820).
- **SCOPE OF IMPACT**

  Causes voltage offsets of signals routed onto the affected analog globals due to interaction of the leakage and internal switch resistances.
- **WORKAROUND**

  Disable the analog supply pump by clearing bit 0 and bit 1 in register PUMP_CR0 (0x5876).
- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

37. SIO Increased Current Consumption

- **PROBLEM DEFINITION**

  Each SIO pin may cause up to an additional 1 mA of Vddio current in some use cases.

- **PARAMETERS AFFECTED**

  NA

- **TRIGGER CONDITION(S)**

  If an SIO pin's voltage exceeds its Vddio supply by 0.5 V, the trigger condition is set (region 1). After the trigger condition is set, the SIO pin causes increased current when its voltage is between Vss + 0.5 V and Vddio – 0.5 V (region 2). The trigger condition is reset when the SIO pin is brought within the range of Vss to Vss + 0.5 V (region 3). The trigger condition may unknowningly be met during device powerup due to differences in supply ramps.

- **SCOPE OF IMPACT**

  Up to 1 mA of additional current per SIO is possible on the SIO pin's Vddio supply when in the high current region after the trigger condition is met. No additional Vddio current will occur when not in the high current region even if the trigger condition is met. No other features of the SIO pin are impacted.

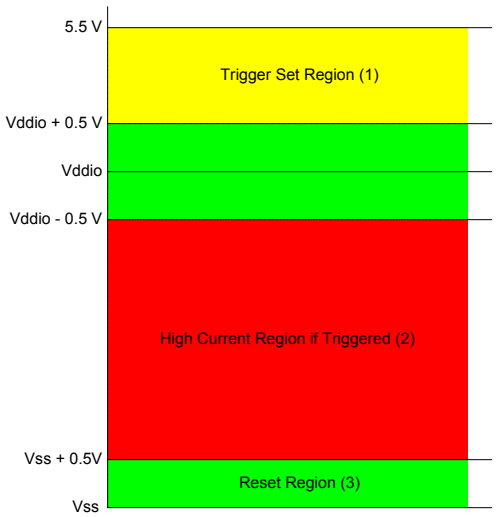
- **WORKAROUND**

  There are three workarounds available:

  1. If trigger condition cannot occur based on system design then no action is required
  2. If trigger condition can occur in the system:
     a) If increased Vddio current is acceptable no action is required
     b) If the SIO pin is used as a digital input or output that will only quickly transition through the high current region, then no action is required. Higher current is seen during the brief transition period through the high current region from high to low logic levels if the trigger condition is met
     c) If the SIO pin must operate in the high current region after the trigger condition is met, no direct workaround is available and increased current is seen. If the SIO can be brought back between Vss and Vss+0.5 V, the trigger condition can be reset until the pin retriggers the condition. The SIO can be brought back to Vss by setting the pin to a low logic level by using API, DMA, or hardware. This will minimize the duration of the extra Vddio current

- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.



38. SIO Port Registers

- **PROBLEM DEFINITION**
  Reading and writing to the SIO port registers with the DMA causes incorrect data to be written to or read from the port register.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Reading and writing the SIO port registers with the DMA.
  PRT12.SIO_HYST_EN
  PRT12.SIO_REG_HIFREQ
  PRT12.SIO_DIFF
  PRT12.SIO_CFG
- **SCOPE OF IMPACT**
  Incorrect data will be latched in the SIO port register on a write. Incorrect data will be read from a SIO port register on a read.
- **WORKAROUND**
  Do not use the DMA to read or write to the SIO port registers.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

39. I/O Pin Configuration

- **PROBLEM DEFINITION**
  Using Pin Configuration Registers to read or write odd number port pins (PRTx_PC1, PRTx_PC3, PRTx_PC5, PRTx_PC7 where x = Port Number) does not work when using DMA.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Using Pin Configuration registers to read or write odd number port pins with DMA.
- **WORKAROUND**
  Use CPU to read or write to the Pin Configuration registers or use DMA to read and write to the Port Configuration register.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

40. Interrupts

- **PROBLEM DEFINITION**

  When two or more interrupts of different priorities are enabled at the same time and the higher priority interrupt triggers at approximately the same time that the lower priority interrupt being serviced returns, the lower priority interrupt may stop responding.
- **PARAMETERS AFFECTED**

  NA
- **TRIGGER CONDITION(S)**

  When two interrupts of different priorities are enabled at the same time and the higher priority interrupt triggers at approximately the same time that the lower priority interrupt being serviced returns.
- **SCOPE OF IMPACT**

  The lower priority interrupt will stop servicing it's interrupt when triggered until the device is Reset.
- **WORKAROUND**

  There are two workarounds available:
  1. Set all interrupts to the same priority
  2. Check the 'ES2' box in the Interrupts section under Design Wide Resources in PSoC Creator. This implements a hex file patch, which allows interrupts of different priorities to be used
- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

41. Fixed Function Timer Capture

- **PROBLEM DEFINITION**

  When using a Fixed Function timer and configuring it to interrupt on capture, the first value returned when reading the capture count value is 0xFF.
- **PARAMETERS AFFECTED**

  NA
- **TRIGGER CONDITION(S)**

  Reading the count value of a capture on a Fixed Function timer.
- **WORKAROUND**

  On initial capture, after calling the start API, read the capture count value twice and ignore the first read value.
- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

42. Fixed Function Timer ISR

- **PROBLEM DEFINITION**

  Using an external clock supplied to an I/O pin may result in an ISR becoming executed multiple times for a single interrupt condition. This issue does not apply when using a clock generated internal to the chip.
- **PARAMETERS AFFECTED**

  NA
- **TRIGGER CONDITION(S)**

  Triggering an ISR when using an external clock with a Fixed Function Timer component.
- **WORKAROUND**

  Use a UDB based Timer instead of a Fixed Function based Timer when interrupts are needed.
- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

43. USB EP0 Transaction Failures

- **PROBLEM DEFINITION**
  Transfers through USB EP0 may fail. These failures manifest as STALL and Data Toggle errors.
- **PARAMETERS AFFECTED**
  None.
- **TRIGGER CONDITION(S)**
  Any USB transfer through EP0.
- **SCOPE OF IMPACT**
  Causes incorrect data packets to transfer between the device and host.
- **WORKAROUND**
  Software workaround available in PSoC Creator Beta 5. Software workaround requires multiple changes to automatically generated APIs in PSoC Creator. Manual alteration is not feasible.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

44. USB Bus Clock

- **PROBLEM DEFINITION**
  USB peripheral requires that the bus clock is greater than or equal to 33 MHz rather then the specified minimum value of 24 MHz to meet bus timing requirements.
- **PARAMETERS AFFECTED**
  None.
- **TRIGGER CONDITION(S)**
  Bus clock less than 33 MHz when USB is enabled.
- **SCOPE OF IMPACT**
  USB generated interrupts may not be detected by the interrupt controller.
- **WORKAROUND**
  Configure the bus clock to be greater than or equal to 33 MHz. PSoC Creator provides a design rule check for this condition.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

45. USB Suspend

- **PROBLEM DEFINITION**

  If USB is enabled and the chip enters hibernate or sleep mode the D+ and D- pins are both pulled high with 5 kΩ resistors in violation of the USB specification for suspend mode.

- **PARAMETERS AFFECTED**

  NA

- **TRIGGER CONDITION(S)**

  USB interface enabled when the chip enters hibernate or sleep mode.

- **SCOPE OF IMPACT**

  For a high speed USB device in the USB suspend mode D+ must be pulled high with a 1.5 kΩ resistor and D- configured for high impedance. This errata causes both D+ and D- to be pulled high with 5 kΩ resistors when the device enters hibernate or sleep mode. Hibernate and sleep mode may not be entered if USB is enabled to meet the USB bus specification. If USB is disabled on the device no errata exists.

- **WORKAROUND**

  The USB component in PSoC Creator implements the required workaround in the API to enter USB suspend mode. The component workaround places the PSoC device into Alternate Active mode with all resources disabled except USB to reduce current to the lowest possible level, and it properly configures the D+ and D- pins for suspend mode. The use of Alternate Active mode verse Sleep or Hibernate for the workaround results in an increase of 1.4 mA of current.

- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

46. USBIO Used as GPIO

- **PROBLEM DEFINITION**

  The USBIO cannot be controlled using the GPIO port and pin registers.

- **TRIGGER CONDITION(S)**

  Use of USBIO as GPIO pins. Does not impact use of the pins for USB.

- **SCOPE OF IMPACT**

  Read and write of USBIO using port and pin registers has no effect.

- **WORKAROUND**

  Use the USB registers to control the I/O by setting the USB_USBIO_CR1 (0x6012) register bit 7 to bit banged mode and using bit 4 and bit 5 to toggle data. Bit 0 and bit 1 should be used to read the status of the USBIO pins.

- **FIX STATUS**

  Silicon revision fix confirmed in production silicon.

47. Power Mode: I²C Available

- **PROBLEM DEFINITION**
  Setting the I²C to be unavailable via the PM.AVAIL.CR4 register (0x43C4) causes the Delta Sigma ADC to return inaccurate data. Setting this bit to unavailable results in reduced power consumption.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Setting Bit 4 (avail_i2C) of PM.AVAIL.CR4 to a value of '0'.
- **SCOPE OF IMPACT**
  Delta Sigma ADC returns inaccurate information due to portions of the Delta Sigma's logic becoming powered down with the I²C hardware.
- **WORKAROUND**
  Ensure that bit 4 (avail_i2C) of PM.AVAIL.CR4 is constantly set to a value of '1'. This bit is set to the proper value by default.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

48. I²C Clocking

- **PROBLEM DEFINITION**
  The I2C_CLK_DIV1 and I2C_CLK_DIV2 registers as described in the TRM are not implemented. The I2C_CLK_DIV register with reduced clock divider options is implemented and described below in the workaround section.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  NA
- **SCOPE OF IMPACT**
  The resolution of generated I²C bus SCL frequencies is reduced.
- **WORKAROUND**
  The I2C_CLK_DIV1 and I2C_CLK_DIV2 registers that provide a fully programmable 10-bit clock divider are not available. Instead use the I2C_CLK_DIV register which provides dividers of 1, 2, 4, 8, 16, 32, and 64 to generate an appropriate SCL clock rate. I²C components implement the required workaround.

  I²C Clock Divide Factor Register

  Reset: System reset for retention flops [reset_all_retention]

  Register: Address

  I2C_CLK_DIV: 0x49DB

Bits	7	6	5	4	3	2	1	0
SW Access: Reset	NA:00000					R/W:000		
HW Access	NA					R		
Name						divide_factor		

  Based on this register value, internal glitch clock enable is derived using system clock.

Bits	Name	Description
2:0	divide_factor[2:0]	000b /1 001b /2 010b /4 011b /8 100b /16 101b /32 110b /64.

- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

49. Reading ECC

- **PROBLEM DEFINITION**
  When reading ECC data (0x80000-0x81FFF) with the CPU on a device in debug mode, a value of 0x00 is returned.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Reading ECC information while in debug mode.
- **SCOPE OF IMPACT**
  A value of 0x00 is returned rather than the correct data.
- **WORKAROUND**
  Temporarily disable the ECC_EN bit (located in SPC Array ID 0x80) before performing a read function. See section 45.3 of the Nonvolatile Memory Programming section in the *PSoC 3 Technical Reference Manual* for details on SPC access.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

50. Enabling ECC in Firmware

- **PROBLEM DEFINITION**
  The ECC logic samples the ECC_EN bit in CNVL anytime the bit changes value.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Altering the value of the ECC_EN bit in CNVL.
- **SCOPE OF IMPACT**
  Causes the ECC error interrupt to trigger.
- **WORKAROUND**
  Do not change the ECC enable bit value in firmware. Only use PSoC Programmer or PSoC Creator to alter the value during device programming.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

51. SPC Checksum Failure

- **PROBLEM DEFINITION**
  When performing an SPC checksum of all Flash contents (SPC Command 0x0C, Flash Array ID 0x3F), the checksum calculation will timeout and a checksum failure is returned.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  Performing a checksum on all Flash contents.
- **SCOPE OF IMPACT**
  Checksum failure will consistently be returned due to timeout.
- **WORKAROUND**
  Individually perform checksum on each block of Flash (SPC Command 0x0C, Flash Array ID 0x00-0x3E). To perform a complete flash checksum, sum together each block checksum to a uint32 variable. See section 45.3 of the Nonvolatile Memory Programming section in the *PSoC 3 Technical Reference Manual* for details on SPC access.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

52. DMA Intraspoke Bursts

- **PROBLEM DEFINITION**
  Intraspoke DMA transfers are limited to a one byte burst length.
- **TRIGGER CONDITION(S)**
  Intraspoke DMA transfer configured for greater than one byte burst length.
- **SCOPE OF IMPACT**
  Data becoming corrupted during DMA transfer.
- **WORKAROUND**
  Limit DMA transactions to one byte burst length transfers. Refer to Table 7-2 in the PHUB section (Section 7.1) of the *PSoC 3 Technical Reference Manual* to determine if both peripherals are on the same spoke.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

53. CAN Conformance

- **PROBLEM DEFINITION**
  The CAN controller does not respond properly to a RX short to ground condition (Bus Off behavior). Glitch filtering does not meet certification requirements.
- **PARAMETERS AFFECTED**
  NA
- **TRIGGER CONDITION(S)**
  RX short to ground. Electrically noisy environment.
- **SCOPE OF IMPACT**
  No impact for user software development. Affects testing and certification for production.
- **WORKAROUND**
  None.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

54. Opamp Buffering of V_{REF}

- **PROBLEM DEFINITION**
  When routing the 1.024 V reference into a opamp results in an incorrect voltage output if the power mode is configured for anything other then mode 0x00.
- **TRIGGER CONDITION(S)**
  Rotuing the 1.024 V reference voltage to an opamp on the device.
- **SCOPE OF IMPACT**
  Output of opamp will deviate from expected value of 1.024 V.
- **WORKAROUND**
  Configure opamp power mode using the Opamp_SetPower() API into the required power mode of 0x00.
- **FIX STATUS**
  Silicon revision fix confirmed in production silicon.

Document History Page

Document Title: PSoC® 3: CY8C34 Family Errata Silicon Revision ES2 Document Number: 001-61136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2921477	RLRM	04/23/10	New errata for the CY8C34 silicon.
*A	2964144	RLRM	06/29/10	Added: Analog Low Power Routing Erratum USB EP0 Transaction Failures Erratum DMA Intraspoke Bursts Erratum Configurable XRES Pin Erratum Updated: Datasheet revision Errata summary table Electrical specifications table Workaround part of Delta Sigma ADC Output Count Errata Removed: Digital Filter Block (DFB) under problem definition of Device Function Errata SIO information from Electrical Specifications Internal Main Oscillator Errata Changed: JTAG or SWD to JTAG/SWD throughout the document
*B	3043361	RLRM	09/30/10	Added: Comparator Enable Erratum Removed: Del Sig ADC DC Specifications from Electrical specifications table. Vdda Monotonicity Erratum SIO Power Up State Erratum CPU Register Read of Register TMRx_SR Erratum Updated: Device Features Erratum Analog Power Routing Erratum Opamp Buffering of V_{REF} Erratum Electrical Specifications table Partnumber column under PSoC 3: CY8C34 Family Errata Summary table on page 1. Electrical specifications table.
*C	3121790	RLRM	01/07/2011	Changed Silicon Revision ES2 Replaced part numbers ES2 Electrical specification content changed. Electrical specification “Parameters Affected table” some values are changed. Fix status has been changed from Available to Confirmed in Errata Summary table. “Analog Low Power Routing” content updated with new content. “SWD Clock” content updated with new content.

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