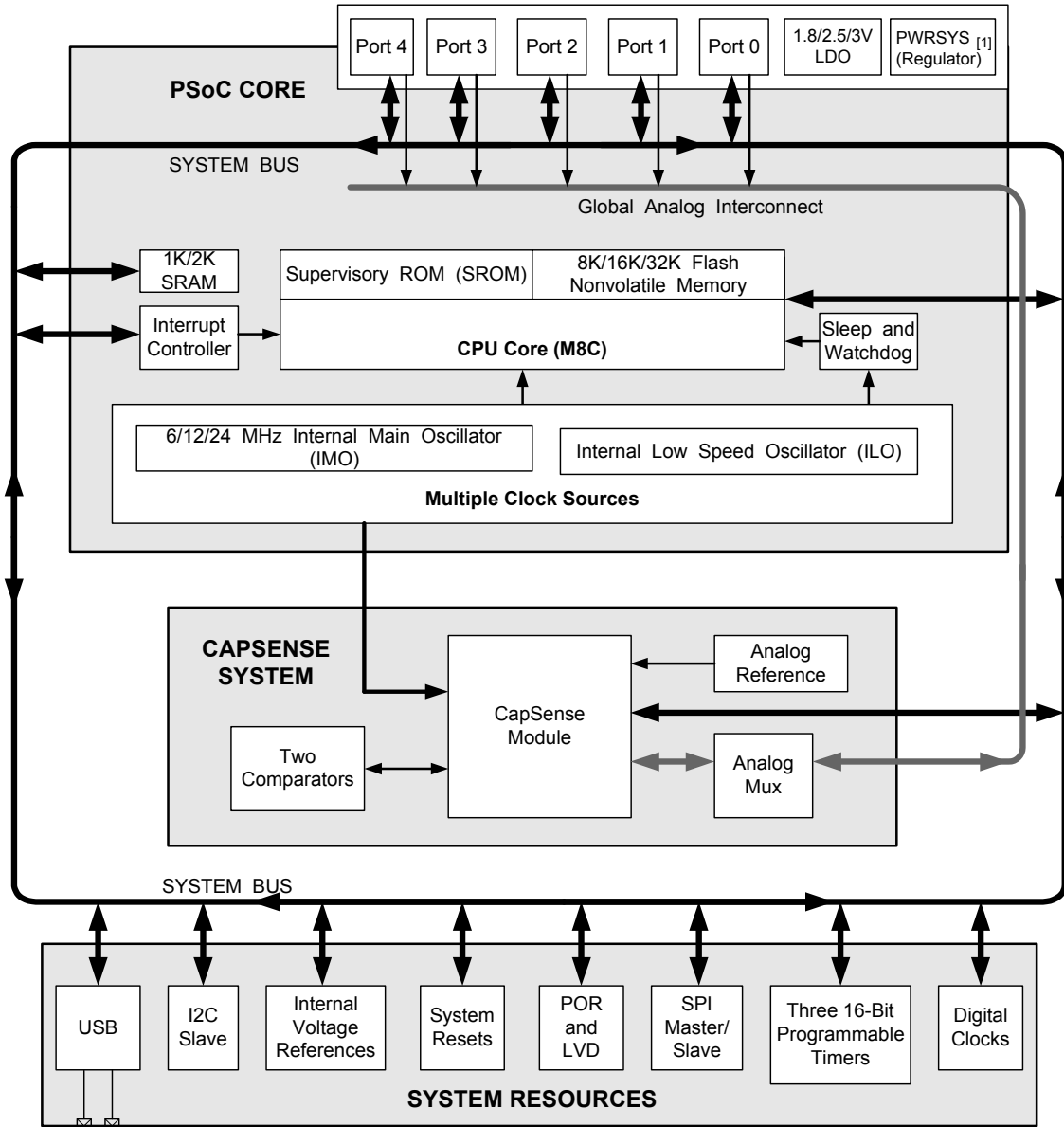


Features

- 1.71 V to 5.5 V operating range
- Low power CapSense® block
 - Configurable capacitive sensing elements
 - Supports combination of CapSense buttons, sliders, touchpads, touchscreens, and proximity sensors
- Powerful Harvard architecture processor
 - M8C CPU speed can be up to 24 MHz or sourced by an external crystal, resonator, or clock signal
 - Low power at high speed
 - Interrupt controller
 - Temperature range: -40 °C to +85 °C
- Flexible on-chip memory
 - Three program/data storage size options:
 - CY8C20x36A: 8K Flash / 1K SRAM
 - CY8C20x46A, CY8C20x96A: 16K Flash/2K SRAM
 - CY8C20x66A: 32K Flash/2K SRAM
 - 50,000 Flash Erase/Write cycles
 - Partial Flash updates
 - Flexible protection modes
 - In-System Serial Programming (ISSP)
- Full Speed USB
 - Available on CY8C20646A, CY8C20666A, CY8C20x96A only
 - 12 Mbps USB 2.0 compliant
 - Eight unidirectional endpoints
 - One bidirectional control endpoint
 - Dedicated 512 byte buffer
 - Internally regulated at 3.3V
- Precision, programmable clocking
 - Internal Main Oscillator (IMO): 6/12/24 MHz ± 5%
 - Internal Low Speed Oscillator (ILO) at 32 kHz for Watchdog and Sleep Timers
 - Precision 32 kHz oscillator for optional external crystal
 - 0.25% accuracy for USB with no external components (CY8C20646A, CY8C20666A, CY8C20x96A only)
- Programmable pin configurations
 - Up to 36 general purpose I/Os (GPIOs) (depending on package)
 - Dual mode GPIO: All GPIOs support digital I/O and analog inputs
 - 25 mA sink current on each GPIO
 - 120 mA total sink current on all GPIOs
 - Pull up, High Z, Open Drain modes on all GPIO
 - CMOS drive mode – 5 mA source current on ports 0 and 1 and 1 mA on ports 2, 3, and 4
 - 20 mA total source current on all GPIOs
 - Selectable, regulated digital I/O on port 1
 - Configurable input threshold on port 1
 - Hot swap capability on all Port 1 GPIO
- Versatile analog mux
 - Common internal analog bus
 - Simultaneous connection of I/O
 - High PSRR comparator
 - Low dropout voltage regulator for all analog resources
- Additional system resources
 - I²C Slave:
 - Selectable to 50 kHz, 100 kHz, or 400 kHz
 - No clock stretching (under most conditions)
 - Implementation during sleep modes with less than 100 µA
 - Hardware address validation
 - SPI master and slave: Configurable 46.9 kHz to 12 MHz
 - Three 16-Bit timers
 - Watchdog and sleep timers
 - Internal voltage reference
 - Integrated supervisory circuit
 - 8 to 10-Bit incremental analog-to-digital converter (ADC)
 - Not available on CY8x20xx6AN versions
 - Two general purpose high speed, low power analog comparators
- Complete development tools
 - Free development tool (PSoC Designer™)
 - Full featured, In-Circuit Emulator (ICE) and Programmer
 - Full speed emulation
 - Complex breakpoint structure
 - 128K trace memory
- Package options
 - CY8C20x36A:
 - 16-Pin 3 x 3 x 0.6 mm QFN
 - 24-Pin 4 x 4 x 0.6 mm QFN
 - 32-Pin 5 x 5 x 0.6 mm QFN
 - 48-Pin SSOP
 - 48-Pin 7 x 7 x 1.0 mm QFN
 - CY8C20x46A:
 - 16-Pin 3 x 3 x 0.6 mm QFN
 - 24-Pin 4 x 4 x 0.6 mm QFN
 - 30-Ball WLCSP
 - 32-Pin 5 x 5 x 0.6 mm QFN
 - 48-Pin SSOP
 - 48-Pin 7 x 7 x 1.0 mm QFN (with USB)
 - CY8C20x96A:
 - 24-Pin 4 x 4 x 0.6 mm QFN (with USB)
 - 32-Pin 5 x 5 x 0.6 mm QFN (with USB)
 - CY8C20x66A:
 - 32-Pin 5 x 5 x 0.6 mm QFN
 - 48-Pin 7 x 7 x 1.0 mm QFN (with USB)
 - 48-Pin SSOP
 - 30-Ball WLCSP

Logic Block Diagram



Note

1. Internal voltage regulator for internal circuitry

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PSoC® Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the [Logic Block Diagram on page 2](#), consists of three main areas:

- The Core
- CapSense Analog System
- System Resources (including a full speed USB port).

A common, versatile bus allows connection between I/O and the analog system.

Each CY8C20x36A/46A/66A/96A PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 36 GPIO are also included. The GPIO provides access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard architecture microprocessor.

CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1V or 1.2V analog reference, which together support capacitive sensing of up to 33 inputs^[2]. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

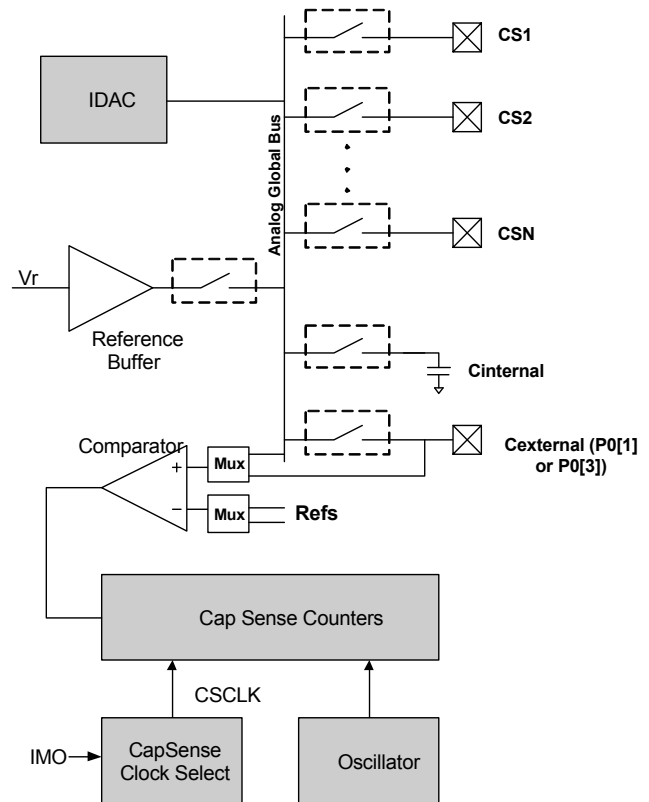
SmartSense™

SmartSense is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easy to use and provides a robust noise immunity. It is the only auto-tuning solution that establishes, monitors, and maintains all required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.

Note

2. 36 GPIOs= 33 pins for capacitive sensing+2 pins for I²C + 1 pin for modulator capacitor.

Figure 1. CapSense System Block Diagram



Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

Additional System Resources

System resources provide additional capability, such as configurable USB and I²C slave, SPI master/slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

These system resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I²C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I²C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I²C enhanced slave interface appears as a 32-byte RAM buffer to the external I²C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For usage details, refer to the application note [I2C Enhanced Slave Operation - AN56007](#).
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced Power-On-Reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the [Technical Reference Manual](#) for the CY8C20x36A/46A/66A/96A PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located at www.cypress.com/psoc. Select Application Notes under the Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. Refer to [Development Kits on page 38](#).

Training

Free PSoC and CapSense technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, create a technical support case or call technical support at 1-800-541-4736.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs.

These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in the following four steps:

1. Select components
2. Configure components
3. Organize and connect
4. Generate, verify, and debug

Select Components

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components. These components are called user modules. User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and programmable system-on-chip varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Timer User Module configures one digital PSoC block. The user module parameters permit you to establish the period, mode, and timer clock. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

User modules are documented in datasheets that are viewed directly in PSoC Designer. These datasheets explain the internal operation of the component and provide performance specifications. Each datasheet describes the use of each user module parameter and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move to developing code for the project, you perform the 'Generate Configuration Files' step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. Based on your design, software is generated. Application programming interfaces (APIs) are provided with high level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both. The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pinouts

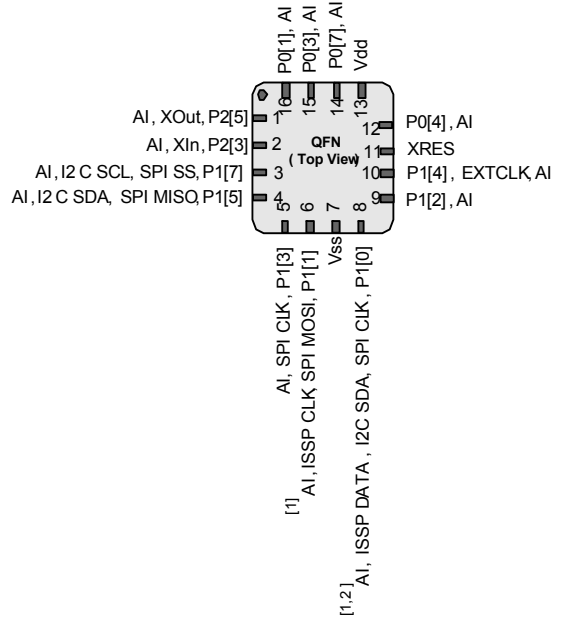
The CY8C20x36A/46A/66A/96A PSoC device is available in a variety of packages, which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

16-Pin QFN (No E-Pad)

Table 1. Pin Definitions - CY8C20236A, CY8C20246A PSoC Device

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	IOHR	I	P1[7]	I ² C SCL, SPI SS
4	IOHR	I	P1[5]	I ² C SDA, SPI MISO
5	IOHR	I	P1[3]	SPI CLK
6	IOHR	I	P1[1]	ISSP CLK ^[1] , I ² C SCL, SPI MOSI
7	Power		V _{SS}	Ground connection
8	IOHR	I	P1[0]	ISSP DATA ^[1] , I ² C SDA, SPI CLK ^[2]
9	IOHR	I	P1[2]	
10	IOHR	I	P1[4]	Optional external clock (EXTCLK)
11	Input		XRES	Active high external reset with internal pull down
12	IOH	I	P0[4]	
13	Power		V _{DD}	Supply voltage
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	Integrating input
16	IOH	I	P0[1]	Integrating input

Figure 2. CY8C20236A, CY8C20246A PSoC Device



LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

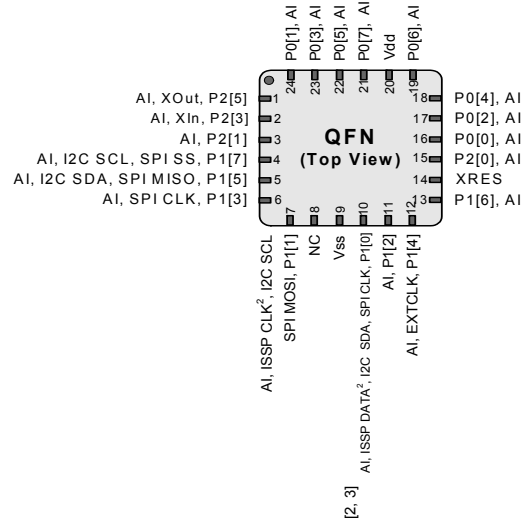
- On power up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1])line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- Alternate SPI clock.

24-Pin QFN

Table 2. Pin Definitions - CY8C20336A, CY8C20346A [1]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I ² C SCL, SPI SS
5	IOHR	I	P1[5]	I ² C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK ^[2] , I ² C SCL, SPI MOSI
8			NC	No connection
9	Power		V _{SS}	Ground connection
10	IOHR	I	P1[0]	ISSP DATA ^[2] , I ² C SDA, SPI CLK ^[3]
11	IOHR	I	P1[2]	
12	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
13	IOHR	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull down
15	I/O	I	P2[0]	
16	IOH	I	P0[0]	
17	IOH	I	P0[2]	
18	IOH	I	P0[4]	
19	IOH	I	P0[6]	
20	Power		V _{DD}	Supply voltage
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		V _{SS}	Center pad must be connected to ground

Figure 3. CY8C20336A, CY8C20346A PSoC Device



LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

- The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- On power up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1])line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues
- Alternate SPI clock.

24-Pin QFN with USB

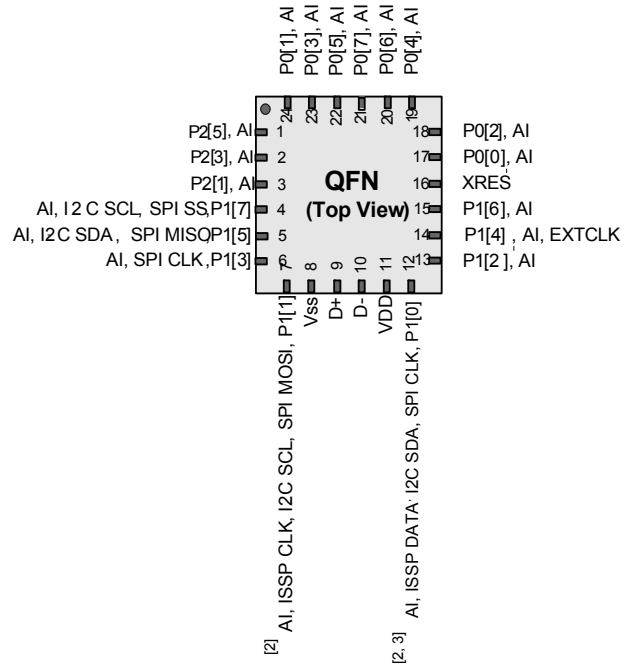
Table 3. Pin Definitions - CY8C20396A PSoC Device [1]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I ² C SCL, SPI SS
5	IOHR	I	P1[5]	I ² C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK ^[2] , I ² C SCL, SPI MOSI
8	Power		V _{SS}	Ground
9	I/O	I	D+	USB D+
10	I/O	I	D-	USB D-
11	Power		V _{DD}	Supply
12	IOHR	I	P1[0]	ISSP DATA ^[2] , I ² C SDA, SPI CLK ³
13	IOHR	I	P1[2]	
14	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
15	IOHR	I	P1[6]	
16	RESET INPUT		XRES	Active high external reset with internal pull down
17	IOH	I	P0[0]	
18	IOH	I	P0[2]	
19	IOH	I	P0[4]	
20	IOH	I	P0[6]	
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		V _{SS}	Thermal pad must be connected to Ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

1. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
2. On power up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1])line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
3. Alternate SPI clock

Figure 4. CY8C20396A PSoC Device

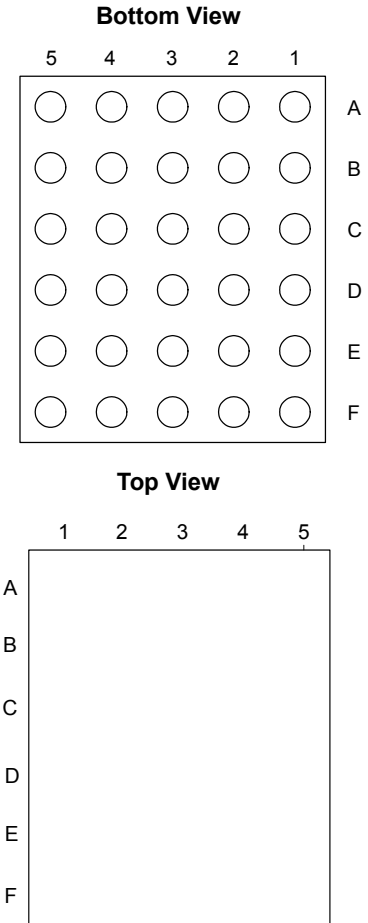


30-Ball Part Pinout

Table 4. CY8C20766A, CY8C20746A 30-Ball Part Pinout (WLCSP)

Pin No.	Type		Name	Description
	Digital	Analog		
A1	IOH	I	P0[2]	
A2	IOH	I	P0[6]	
A3	Power		V _{DD}	Supply voltage
A4	IOH	I	P0[1]	Integrating Input
A5	I/O	I	P2[7]	
B1	I/O	I	P2[6]	
B2	IOH	I	P0[0]	
B3	IOH	I	P0[4]	
B4	IOH	I	P0[3]	Integrating Input
B5	I/O	I	P2[5]	Crystal Output (Xout)
C1	I/O	I	P2[2]	
C2	I/O	I	P2[4]	
C3	IOH	I	P0[7]	
C4	IOH	I	P0[5]	
C5	I/O	I	P2[3]	Crystal Input (Xin)
D1	I/O	I	P2[0]	
D2	I/O	I	P3[0]	
D3	I/O	I	P3[1]	
D4	I/O	I	P3[3]	
D5	I/O	I	P2[1]	
E1	Input		XRES	Active high external reset with internal pull down
E2	IOHR	I	P1[6]	
E3	IOHR	I	P1[4]	Optional external clock input (EXT CLK)
E4	IOHR	I	P1[7]	I ² C SCL, SPI SS
E5	IOHR	I	P1[5]	I ² C SDA, SPI MISO
F1	IOHR	I	P1[2]	
F2	IOHR	I	P1[0]	ISSP DATA ^[1] , I ² C SDA, SPI CLK ^[2]
F3	Power		V _{SS}	Supply ground
F4	IOHR	I	P1[1]	ISSP CLK ^[1] , I ² C SCL, SPI MOSI
F5	IOHR	I	P1[3]	SPI CLK

Figure 5. CY8C20766A 30-Ball WLCSP



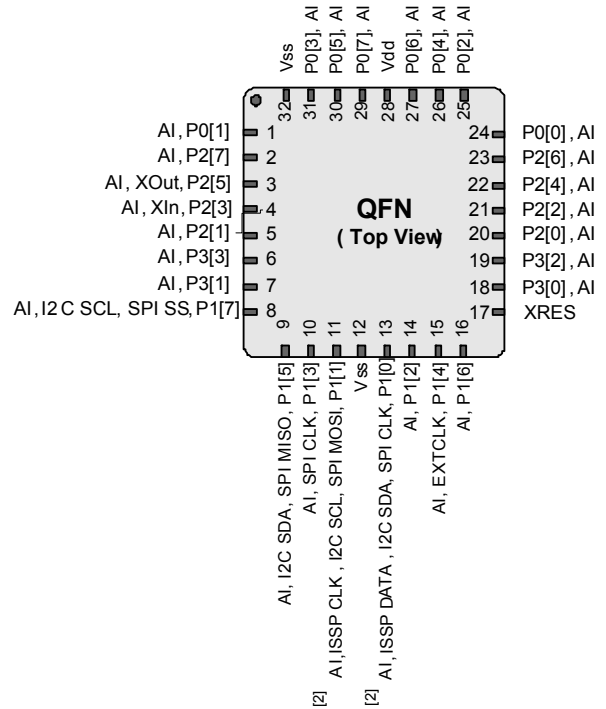
1. On power up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1])line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
2. Alternate SPI clock.

32-Pin QFN

Table 5. Pin Definitions - CY8C20436A, CY8C20446A, CY8C20466A PSoC Device [1]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating input
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I ² C SCL, SPI SS
9	IOHR	I	P1[5]	I ² C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK ^[2] , I ² C SCL, SPI MOSI.
12	Power		V _{SS}	Ground connection.
13	IOHR	I	P1[0]	ISSP DATA ^[2] , I ² C SDA., SPI CLK ^[3]
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		V _{DD}	Supply voltage
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	Integrating input
32	Power		V _{SS}	Ground connection
CP	Power		V _{SS}	Center pad must be connected to ground

Figure 6. CY8C20436A, CY8C20446A, CY8C20466A PSoC Device



LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

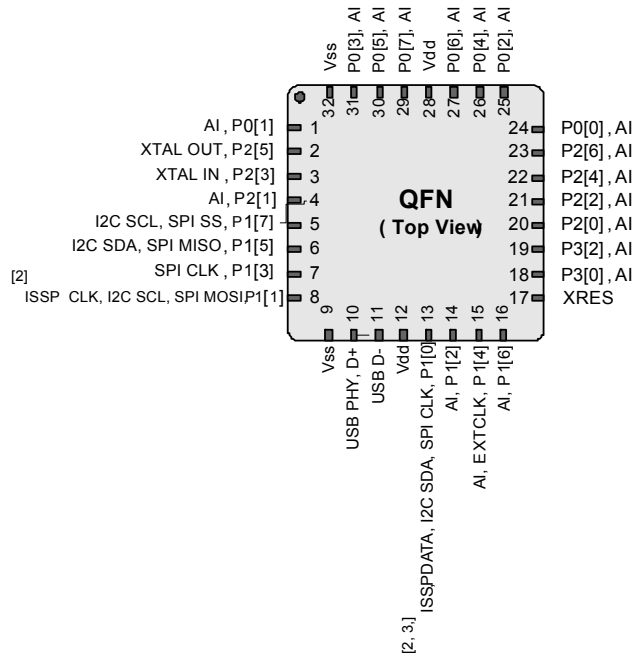
- The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- On power up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- Alternate SPI clock.

32-Pin QFN (with USB)

Table 6. Pin Definitions - CY8C20496A PSoc Device ^[1]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating Input
2	I/O	I	P2[5]	XTAL Out
3	I/O	I	P2[3]	XTAL In
4	I/O	I	P2[1]	
5	IOHR	I	P1[7]	I ² C SCL, SPI SS
6	IOHR	I	P1[5]	I ² C SDA, SPI MISO
7	IOHR	I	P1[3]	SPI CLK
8	IOHR	I	P1[1]	ISSP CLK ^[2] , I ² C SCL, SPI MOSI
9	Power		V _{SS}	Ground Pin
10		I	D+	USB D+
11		I	D-	USB D-
12	Power		V _{DD}	Power pin
13	IOHR	I	P1[0]	ISSP DATA ^[2] , I ² C SDA, SPI CLK ^[3]
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		V _{DD}	Power Pin
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	Integrating Input
32	Power		V _{SS}	Ground Pin

Figure 7. CY8C20496A PSoc Device



LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

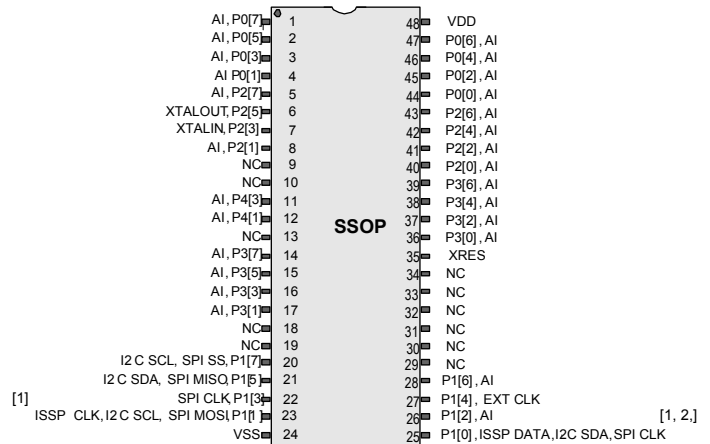
1. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
2. On power up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate SPI clock.
3. Alternate SPI clock.

48-Pin SSOP

Table 7. Pin Definitions - CY8C20536A, CY8C20546A, and CY8C20566A PSoC Device^[1]

Pin No.	Digital	Analog	Name	Description
1	IOH	I	P0[7]	
2	IOH	I	P0[5]	
3	IOH	I	P0[3]	Integrating Input
4	IOH	I	P0[1]	Integrating Input
5	I/O	I	P2[7]	
6	I/O	I	P2[5]	XTAL Out
7	I/O	I	P2[3]	XTAL In
8	I/O	I	P2[1]	
9			NC	No connection
10			NC	No connection
11	I/O	I	P4[3]	
12	I/O	I	P4[1]	
13			NC	No connection
14	I/O	I	P3[7]	
15	I/O	I	P3[5]	
16	I/O	I	P3[3]	
17	I/O	I	P3[1]	
18			NC	No connection
19			NC	No connection
20	IOHR	I	P1[7]	I ² C SCL, SPI SS
21	IOHR	I	P1[5]	I ² C SDA, SPI MISO
22	IOHR	I	P1[3]	SPI CLK
23	IOHR	I	P1[1]	ISSP CLK ^[1] , I ² C SCL, SPI MOSI
24			V _{SS}	Ground Pin
25	IOHR	I	P1[0]	ISSP DATA ^[1] , I ² C SDA, SPI CLK ^[2]
26	IOHR	I	P1[2]	
27	IOHR	I	P1[4]	Optional external clock input (EXT CLK)
28	IOHR	I	P1[6]	
29			NC	No connection
30			NC	No connection
31			NC	No connection
32			NC	No connection
33			NC	No connection
34			NC	No connection
35			XRES	Active high external reset with internal pull down
36	I/O	I	P3[0]	
37	I/O	I	P3[2]	
38	I/O	I	P3[4]	
39	I/O	I	P3[6]	
40	I/O	I	P2[0]	
41	I/O	I	P2[2]	
42	I/O	I	P2[4]	
43	I/O	I	P2[6]	
44	IOH	I	P0[0]	
45	IOH	I	P0[2]	
46	IOH	I	P0[4]	
47	IOH	I	P0[6]	
48	Power		V _{DD}	Power Pin

Figure 8. CY8C20536A, CY8C20546A, and CY8C20566A PSoC Device



LEGEND A = Analog, I = Input, O = Output, NC = No Connection, H = 5 mA High Output Drive, R = Regulated Output Option.

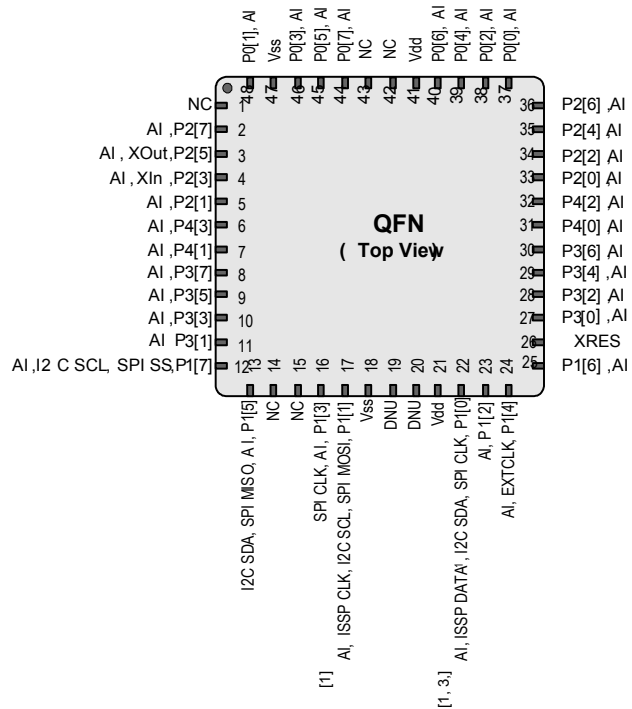
- On power up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1])line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues..
- Alternate SPI clock.

48-Pin QFN

Table 8. Pin Definitions - CY8C20636A PSoC Device [1, 2]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I ² C SCL, SPI SS
13	IOHR	I	P1[5]	I ² C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	ISSP CLK ^[1] , I ² C SCL, SPI MOSI
18	Power		V _{SS}	Ground connection
19			DNU	
20			DNU	
21	Power		V _{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA ^[1] , I ² C SDA, SPI CLK ^[3]
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V _{DD}	Supply voltage
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V _{SS}	Ground connection
48	IOH	I	P0[1]	
CP	Power		V _{SS}	Center pad must be connected to ground

Figure 9. CY8C20636A PSoC Device



LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

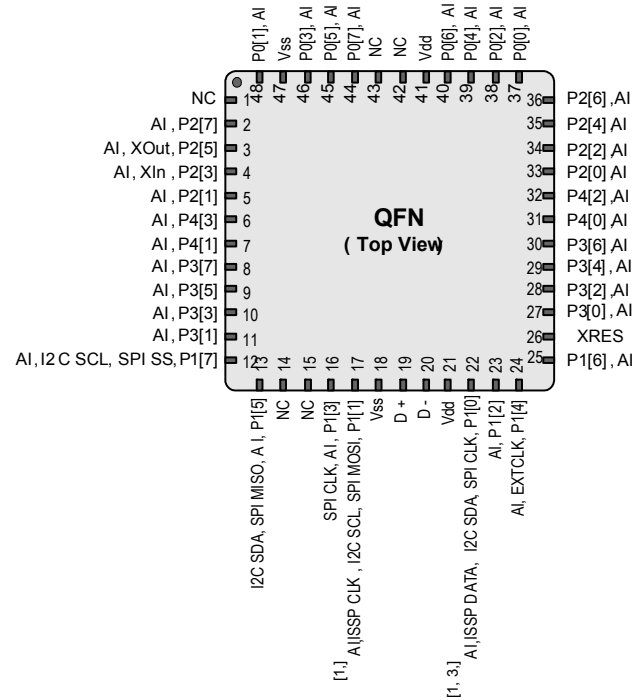
- On power up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1])line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- Alternate SPI clock.

48-Pin QFN with USB

Table 9. Pin Definitions - CY8C20646A, CY8C20666A PSoC Device [1, 2]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I ² C SCL, SPI SS
13	IOHR	I	P1[5]	I ² C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	ISSP CLK ^[1] , I ² C SCL, SPI MOSI
18	Power		V _{SS}	Ground connection
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		V _{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA ^[1] , I ² C SDA, SPI CLK ^[3]
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V _{DD}	Supply voltage
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V _{SS}	Ground connection
48	IOH	I	P0[1]	
CP	Power		V _{SS}	Center pad must be connected to ground

Figure 10. CY8C20646A, CY8C20666A PSoC Device



LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

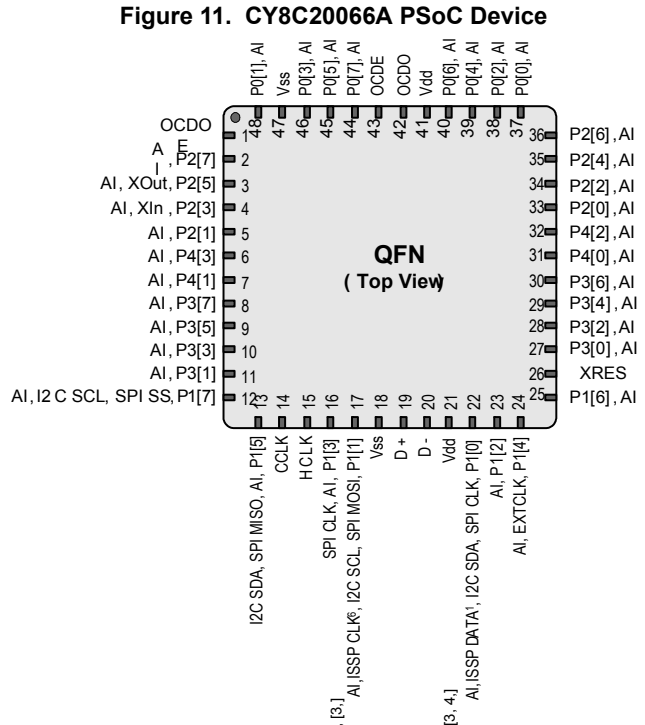
- On Power Up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1])line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull up resistance on these lines combines with the pull down resistance (5.6K ohm) and form a potential divider. Hence, during power up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- Alternate SPI clock.

48-Pin QFN OCD

The 48-pin QFN part is for the CY8C20066A On-Chip Debug (OCD) PSoC device. Note that this part is only used for in-circuit debugging.

Table 10. Pin Definitions - CY8C20066A PSoC Device [1, 2]

Pin No.	Digital	Analog	Name	Description
1			OCDOE	OCD mode direction pin
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I ² C SCL, SPI SS
13	IOHR	I	P1[5]	I ² C SDA, SPI MISO
14			CCLK	OCD CPU clock output
15			HCLK	OCD high speed clock output
16	IOHR	I	P1[3]	SPI CLK.
17	IOHR	I	P1[1]	ISSP CLK ^[3] , I ² C SCL, SPI MOSI
18	Power		V _{SS}	Ground connection
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		V _{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA ^[3] , I ² C SDA, SPI CLK ^[4]
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	



Pin No.	Digital	Analog	Name	Description
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V _{DD}	Supply voltage
42			OCDO	OCD even data I/O
43			OCDE	OCD odd data output
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V _{SS}	Ground connection
48	IOH	I	P0[1]	
CP	Power		V _{SS}	Center pad must be connected to ground

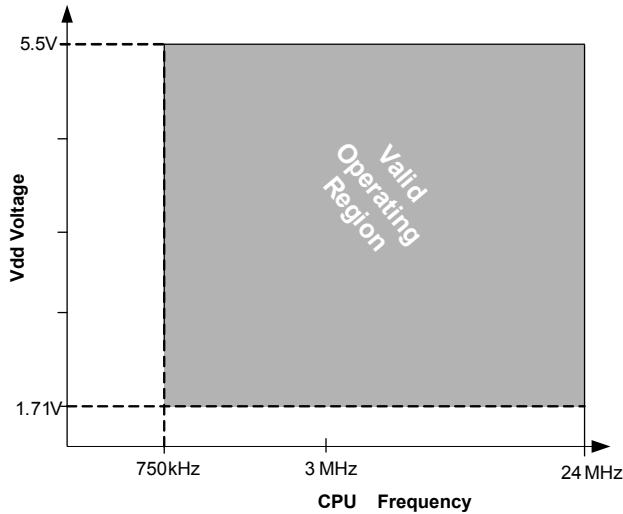
LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

1. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.
2. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
3. On Power Up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull up resistance on these lines combines with the pull down resistance (5.6K ohm) and form a potential divider. Hence, during power up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
4. Alternate SPI clock.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x36A/46A/66A/96A PSoC devices. For the latest electrical specifications, confirm that you have the most recent data sheet by visiting the web at <http://www.cypress.com/psoc>.

Figure 12. Voltage versus CPU Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 11. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{STG}	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25°C ± 25°C. Extended duration storage temperatures above 85°C degrades reliability.	-55	+25	+125	°C
V _{DD}	Supply voltage relative to V _{SS}		-0.5	-	+6.0	V
V _{IO}	DC input voltage		V _{SS} - 0.5	-	V _{DD} + 0.5	V
V _{IOZ}	DC voltage applied to tristate		V _{SS} - 0.5	-	V _{DD} + 0.5	V
I _{MIO}	Maximum current into any port pin		-25	-	+50	mA
ESD	Electro static discharge voltage	Human Body Model ESD	2000	-	-	V
LU	Latch up current	In accordance with JESD78 standard	-	-	200	mA

Operating Temperature

Table 12. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T _A	Ambient temperature		-40	-	+85	°C
T _C	Commercial temperature range		0		70	°C
T _J	Operational die temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 37 . The user must limit the power consumption to comply with this requirement.	-40	-	+100	°C

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 13. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DD}^{[1, 2, 3, 4]}$	Supply Voltage	Refer the table DC POR and LVD Specifications on page 23	1.71	–	5.50	V
I_{DD24}	Supply Current, IMO = 24 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	3.32	4.00	mA
I_{DD12}	Supply Current, IMO = 12 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	1.86	2.60	mA
I_{DD6}	Supply Current, IMO = 6 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current	–	1.13	1.80	mA
I_{SB0}	Deep Sleep Current	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	0.10	0.50	μA
I_{SB1}	Standby Current with POR, LVD and Sleep Timer	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	1.07	1.50	μA

- When V_{DD} remains in the range from 1.71V to 1.9V for more than 50 μsec, the slew rate when moving from the 1.71V to 1.9V range to greater than 2V must be slower than 1V/500 μsec to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
- If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
 - Bring the device out of sleep before powering down.
 - Assure that V_{DD} falls below 100 mV before powering back up.
 - Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
 - Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register. For the referenced registers, refer to the *CY8C20x36 Technical Reference Manual*. In deep sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected for edge rates slower than 1V/ms.
- For USB mode, the V_{DD} supply for bus-powered application should be limited to 4.35V-5.35V. For self-powered application, V_{DD} should be 3.15V-3.45V.
- For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD} , the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.

DC General Purpose I/O Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 5.5V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 2.4V to 3.0V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 1.71V to 2.4V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 14. 3.0V to 5.5V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull up Resistor		4	5.60	8	kΩ
V _{OH1}	High Output Voltage Port 2 or 3 Pins	IOH ≤ 10 μA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.20	–	–	V
V _{OH2}	High Output Voltage Port 2 or 3 Pins	IOH = 1 mA, maximum of 20 mA source current in all I/Os	V _{DD} - 0.90	–	–	V
V _{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH < 10 μA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.20	–	–	V
V _{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH = 5 mA, maximum of 20 mA source current in all I/Os	V _{DD} - 0.90	–	–	V
V _{OH5}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	IOH < 10 μA, V _{DD} > 3.1 V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.30	V
V _{OH6}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	IOH = 5 mA, V _{DD} > 3.1V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V _{OH7}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	IOH < 10 μA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V _{OH8}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	IOH = 2 mA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V _{OH9}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH < 10 μA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.10	V
V _{OH10}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH = 1 mA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V _{OL}	Low Output Voltage	IOL = 25 mA, V _{DD} > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V _{IL}	Input Low Voltage		–	–	0.80	V
V _{IH}	Input High Voltage		2.00	–	–	V
V _H	Input Hysteresis Voltage		–	80	–	mV
I _{IL}	Input Leakage (Absolute Value)		–	0.001	1	μA
C _{PIN}	Pin Capacitance	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF

Table 15. 2.4V to 3.0V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull up Resistor		4	5.60	8	kΩ
V _{OH1}	High Output Voltage Port 2 or 3 Pins	I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.20	–	–	V
V _{OH2}	High Output Voltage Port 2 or 3 Pins	I _{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.40	–	–	V
V _{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.20	–	–	V
V _{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.50	–	–	V
V _{OH5A}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	I _{OH} < 10 μA, V _{DD} > 2.4V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V _{OH6A}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	I _{OH} = 1 mA, V _{DD} > 2.4V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V _{OL}	Low Output Voltage	I _{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V _{IL}	Input Low Voltage		–	–	0.72	V
V _{IH}	Input High Voltage		1.40	–	–	V
V _H	Input Hysteresis Voltage		–	80	–	mV
I _{IL}	Input Leakage (Absolute Value)		–	1	1000	nA
C _{PIN}	Capacitive Load on Pins	Package and pin dependent Temp = 25°C	0.50	1.70	7	pF

Table 16. 1.71V to 2.4V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull up Resistor		4	5.60	8	kΩ
V _{OH1}	High Output Voltage Port 2 or 3 Pins	I _{OH} = 10 μA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.20	–	–	V
V _{OH2}	High Output Voltage Port 2 or 3 Pins	I _{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.50	–	–	V
V _{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I _{OH} = 100 μA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.20	–	–	V
V _{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I _{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V _{DD} - 0.50	–	–	V
V _{OL}	Low Output Voltage	I _{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V
V _{IL}	Input Low Voltage		–	–	0.30 x V _{DD}	V
V _{IH}	Input High Voltage		0.65 x V _{DD}	–	–	V

Table 16. 1.71V to 2.4V DC GPIO Specifications (continued)

Symbol	Description	Conditions	Min	Typ	Max	Units
V _H	Input Hysteresis Voltage		–	80	–	mV
I _{IL}	Input Leakage (Absolute Value)		–	1	1000	nA
C _{PIN}	Capacitive Load on Pins	Package and pin dependent Temp = 25°C	0.50	1.70	7	pF

Table 17. DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{usb}	USB D+ Pull Up Resistance	With idle bus	900	-	1575	Ω
R _{usbA}	USB D+ Pull Up Resistance	While receiving traffic	1425	-	3090	Ω
V _{ohusb}	Static Output High		2.8	-	3.6	V
V _{olusb}	Static Output Low			-	0.3	V
V _{di}	Differential Input Sensitivity		0.2	-		V
V _{cm}	Differential Input Common Mode Range		0.8	-	2.5	V
V _{se}	Single Ended Receiver Threshold		0.8	-	2.0	V
C _{in}	Transceiver Capacitance			-	50	pF
I _{io}	Hi-Z State Data Line Leakage	On D+ or D- line	-10	-	+10	μA
R _{ps2}	PS/2 Pull Up Resistance		3000	5000	7000	Ω
R _{ext}	External USB Series Resistor	In series with each USB pin	21.78	22.0	22.22	Ω

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{SW}	Switch Resistance to Common Analog Bus		–	–	800	Ω
R _{GND}	Resistance of Initialization Switch to V _{SS}		–	–	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8V

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{LPC}	Low Power Comparator (LPC) common mode	Maximum voltage limited to V _{DD}	0.0	–	1.8	V
I _{LPC}	LPC supply current		–	10	40	μA
V _{OSLPC}	LPC voltage offset		–	2.5	30	mV

Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $1.71\text{V} \leq V_{DD} \leq 5.5\text{V}$.

Table 20. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{COMP}	Comparator Response Time	50 mV overdrive		70	100	ns
Offset		Valid from 0.2 V to $V_{DD}-0.2\text{V}$		2.5	30	mV
Current		Average DC current, 50 mV overdrive		20	80	μA
PSRR	Supply voltage > 2 V	Power Supply Rejection Ratio		80		dB
	Supply voltage < 2 V	Power Supply Rejection Ratio		40		dB
Input Range			0		1.5	V

ADC Electrical Specifications
Table 21. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input Voltage Range		0		V_{REFADC}	V
C_{IIN}	Input Capacitance				5	pF
R_{IN}	Input Resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	$1/(500\text{fF} \cdot \text{Data Clock})$	$1/(400\text{fF} \cdot \text{Data Clock})$	$1/(300\text{fF} \cdot \text{Data Clock})$	Ω
Reference						
V_{REFADC}	ADC Reference Voltage		1.14		1.26	V
Conversion Rate						
F_{CLK}	Data Clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25		6	MHz
S8	8-bit Sample Rate	Data Clock set to 6 MHz. Sample Rate = $0.001 / (2^{\text{Resolution}} / \text{Data Clock})$		23.43		ksp/s
S10	10-bit Sample Rate	Data Clock set to 6 MHz. Sample Rate = $0.001 / (2^{\text{Resolution}} / \text{Data Clock})$		5.85		ksp/s
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8		10	bits
DNL	Differential Nonlinearity		-1		+2	LSB
INL	Integral Nonlinearity		-2		+2	LSB
E_{OFFSET}	Offset Error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E_{GAIN}	Gain Error	For any resolution	-5		+5	%FSR
Power						
I_{ADC}	Operating Current			2.10	2.60	mA
PSRR	Power Supply Rejection Ratio	PSRR ($V_{DD} > 3.0\text{V}$)		24		dB
		PSRR ($V_{DD} < 3.0\text{V}$)		30		dB

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 22. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{POR0}	1.66 V selected in PSoC Designer	V _{DD} must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V _{POR1}	2.36 V selected in PSoC Designer		–	2.36	2.41	
V _{POR2}	2.60 V selected in PSoC Designer		–	2.60	2.66	
V _{POR3}	2.82 V selected in PSoC Designer		–	2.82	2.95	
V _{LVD0}	2.45 V selected in PSoC Designer		2.40	2.45	2.51	V
V _{LVD1}	2.71 V selected in PSoC Designer		2.64 ^[1]	2.71	2.78	
V _{LVD2}	2.92 V selected in PSoC Designer		2.85 ^[2]	2.92	2.99	
V _{LVD3}	3.02 V selected in PSoC Designer		2.95 ^[3]	3.02	3.09	
V _{LVD4}	3.13V selected in PSoC Designer		3.06	3.13	3.20	
V _{LVD5}	1.90 V selected in PSoC Designer		1.84	1.90	2.32	
V _{LVD6}	1.80 V selected in PSoC Designer		1.75 ^[4]	1.80	1.84	
V _{LVD7}	4.73 V selected in PSoC Designer		4.62	4.73	4.83	

1. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
2. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
3. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
4. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 23. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{DD} _{IWRITE}	Supply Voltage for Flash Write Operations		1.71	–	5.25	V
I _{DDP}	Supply Current During Programming or Verify		–	5	25	mA
V _{ILP}	Input Low Voltage During Programming or Verify	See the appropriate DC General Purpose I/O Specifications on page 19	–	–	V _{IL}	V
V _{IHP}	Input High Voltage During Programming or Verify	See appropriate DC General Purpose I/O Specifications on page 19 table on pages 15 or 16	V _{IH}	–	–	V
I _{ILP}	Input Current when Applying V _{ILP} to P1[0] or P1[1] During Programming or Verify	Driving internal pull down resistor	–	–	0.2	mA
I _{IHP}	Input Current when Applying V _{IHP} to P1[0] or P1[1] During Programming or Verify	Driving internal pull down resistor	–	–	1.5	mA
V _{OLP}	Output Low Voltage During Programming or Verify		–	–	V _{SS} + 0.75	V
V _{OHP}	Output High Voltage During Programming or Verify	See appropriate DC General Purpose I/O Specifications on page 19 table on page 16. For V _{DD} > 3V use V _{OHP4} in Table 12 on page 17 .	V _{OH}	–	V _{DD}	V
Flash _{ENPB}	Flash Write Endurance	Erase/write cycles per block	50,000	–	–	-
Flash _{DR}	Flash Data Retention	Following maximum Flash write cycles; ambient temperature of 55°C	10	20	–	Years

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 24. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{IMO24}	Internal Main Oscillator Frequency at 24 MHz Setting		22.8	24	25.2	MHz
F _{IMO12}	Internal Main Oscillator Frequency at 12 MHz Setting		11.4	12	12.6	MHz
F _{IMO6}	Internal Main Oscillator Frequency at 6 MHz Setting		5.7	6.0	6.3	MHz
F _{CPU}	CPU Frequency		0.75	–	25.20	MHz
F _{32K1}	Internal Low Speed Oscillator Frequency		19	32	50	kHz
F _{32K_U}	Internal Low Speed Oscillator (ILO) Untrimmed Frequency)		13	32	82	kHz
DC _{IMO}	Duty Cycle of IMO		40	50	60	%
DC _{ILO}	Internal Low Speed Oscillator Duty Cycle		40	50	60	%
SR _{POWER_UP}	Power Supply Slew Rate	V _{DD} slew rate during power up	–	–	250	V/ms
T _{XRST}	External Reset Pulse Width at Power Up	After supply voltage is valid	1			ms
T _{XRST2}	External Reset Pulse Width after Power Up ^[1]	Applies after part has booted	10			μs

1. The minimum required XRES pulse length is longer when programming the device (see [Table 30 on page 27](#)).

AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 25. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO Operating Frequency	Normal Strong Mode Port 0, 1	0	–	6 MHz for 1.71 V < V_{DD} < 2.40 V 12 MHz for 2.40 V < V_{DD} < 5.50 V	MHz
T_{RISE23}	Rise Time, Strong Mode, Clload = 50 pF Ports 2 or 3	V_{DD} = 3.0 to 3.6 V, 10% – 90%	15	–	80	ns
$T_{RISE23L}$	Rise Time, Strong Mode Low Supply, Clload = 50 pF, Ports 2 or 3	V_{DD} = 1.71 to 3.0 V, 10% – 90%	15	–	80	ns
T_{RISE01}	Rise Time, Strong Mode, Clload = 50 pF Ports 0 or 1	V_{DD} = 3.0 to 3.6 V, 10% – 90% LDO enabled or disabled	10	–	50	ns
$T_{RISE01L}$	Rise Time, Strong Mode Low Supply, Clload = 50 pF, Ports 0 or 1	V_{DD} = 1.71 to 3.0 V, 10% – 90% LDO enabled or disabled	10	–	80	ns
T_{FALL}	Fall Time, Strong Mode, Clload = 50 pF All Ports	V_{DD} = 3.0 to 3.6 V, 10% – 90%	10	–	50	ns
T_{FALLL}	Fall Time, Strong Mode Low Supply, Clload = 50 pF, All Ports	V_{DD} = 1.71 to 3.0 V, 10% – 90%	10	–	70	ns

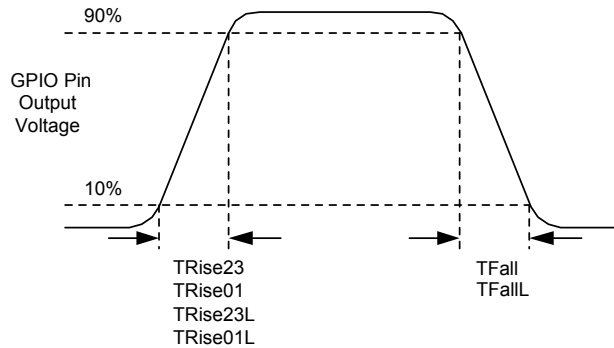
Figure 13. GPIO Timing Diagram


Table 26.AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{DRATE}	Full speed data rate	Average bit rate	12-0.25%	12	12 + 0.25%	MHz
T _{JR1}	Receiver jitter tolerance	To next transition	-18.5	–	18.5	ns
T _{JR2}	Receiver jitter tolerance	To pair transition	-9	–	9	ns
T _{DJ1}	FS Driver jitter	To next transition	-3.5	–	3.5	ns
T _{DJ2}	FS Driver jitter	To pair transition	-4.0	–	4.0	ns
T _{FDEOP}	Source jitter for differential transition	To SE0 transition	-2	–	5	ns
T _{FEOPT}	Source SE0 interval of EOP		160	–	175	ns
T _{FEOPR}	Receiver SE0 interval of EOP		82	–		ns
T _{FST}	Width of SE0 interval during differential transition			–	14	ns

Table 27. AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{FR}	Transition rise time	50 pF	4	–	20	ns
T _{FF}	Transition fall time	50 pF	4	–	20	ns
T _{FRFM} ^[1]	Rise/fall time matching		90	–	111	%
V _{crs}	Output signal crossover voltage		1.30	–	2.00	V

1. T_{FRFM} is not met under all conditions. There is a corner case at lower supply voltages, such as those under 3.3V. This condition does not affect USB communications. Signal integrity tests show an excellent eye diagram at 3.15V.

AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 28. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{LPC}	Comparator Response Time, 50 mV Overdrive	50 mV overdrive does not include offset voltage.			100	ns

AC External Clock Specifications

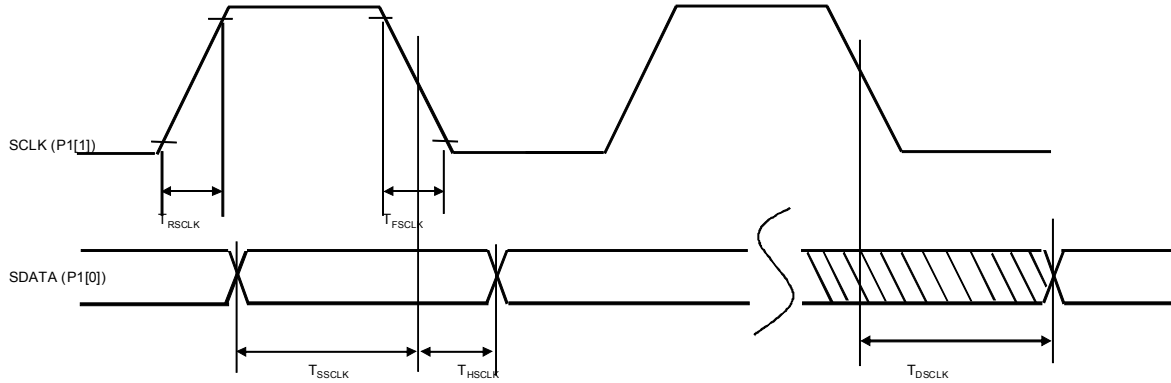
The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 29. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F _{OSCEXT}	Frequency (external oscillator frequency)		0.75	–	25.20	MHz
	High Period		20.60	–	5300	ns
	Low Period		20.60	–	–	ns
	Power Up IMO to Switch		150	–	–	µs

AC Programming Specifications

Figure 14. AC Waveform



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 30. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise Time of SCLK		1	–	20	ns
T_{FSCLK}	Fall Time of SCLK		1	–	20	ns
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK		40	–	–	ns
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash Erase Time (Block)		–	–	18	ms
T_{WRITE}	Flash Block Write Time		–	–	25	ms
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	$3.6 < V_{DD}$	–	–	60	ns
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	$3.0 \leq V_{DD} \leq 3.6$	–	–	85	ns
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	$1.71 \leq V_{DD} \leq 3.0$	–	–	130	ns
T_{XRST3}	External Reset Pulse Width after Power Up	Required to enter programming mode when coming out of sleep	300	–	–	μ s
T_{XRES}	XRES Pulse Length		300	–	–	μ s
$T_{VDDWAIT}$	V_{DD} stable to wait-and-poll hold off		0.1	–	1	ms
$T_{VDDXRES}$	V_{DD} stable to XRES assertion delay		14.27	–	–	ms
T_{POLL}	SDATA high pulse time		0.01	–	200	ms
T_{ACQ}	“Key window” time after a V_{DD} ramp acquire event, based on 256 ILO clocks.		3.20	–	19.60	ms
$T_{XRESINI}$	“Key window” time after an XRES event, based on 8 ILO clocks		98	–	615	μ s

AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 31. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f _{SCL}	SCL Clock Frequency	0	100	0	400	kHz
t _{HD;STA}	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	μs
t _{LOW}	LOW Period of the SCL Clock	4.7	–	1.3	–	μs
t _{HIGH}	HIGH Period of the SCL Clock	4.0	–	0.6	–	μs
t _{SU;STA}	Setup Time for a Repeated START Condition	4.7	–	0.6	–	μs
t _{HD;DAT}	Data Hold Time	0	–	0	–	μs
t _{SU;DAT}	Data Setup Time	250	–	100 ^[1]	–	ns
t _{SU;STO}	Setup Time for STOP Condition	4.0	–	0.6	–	μs
t _{BUF}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	μs
t _{SP}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns

1. A Fast-Mode I²C-bus device can be used in a Standard Mode I²C-bus system, but the requirement t_{SU;DAT} ≥ 250 ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250 ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Figure 15. Definition for Timing for Fast/Standard Mode on the I²C Bus

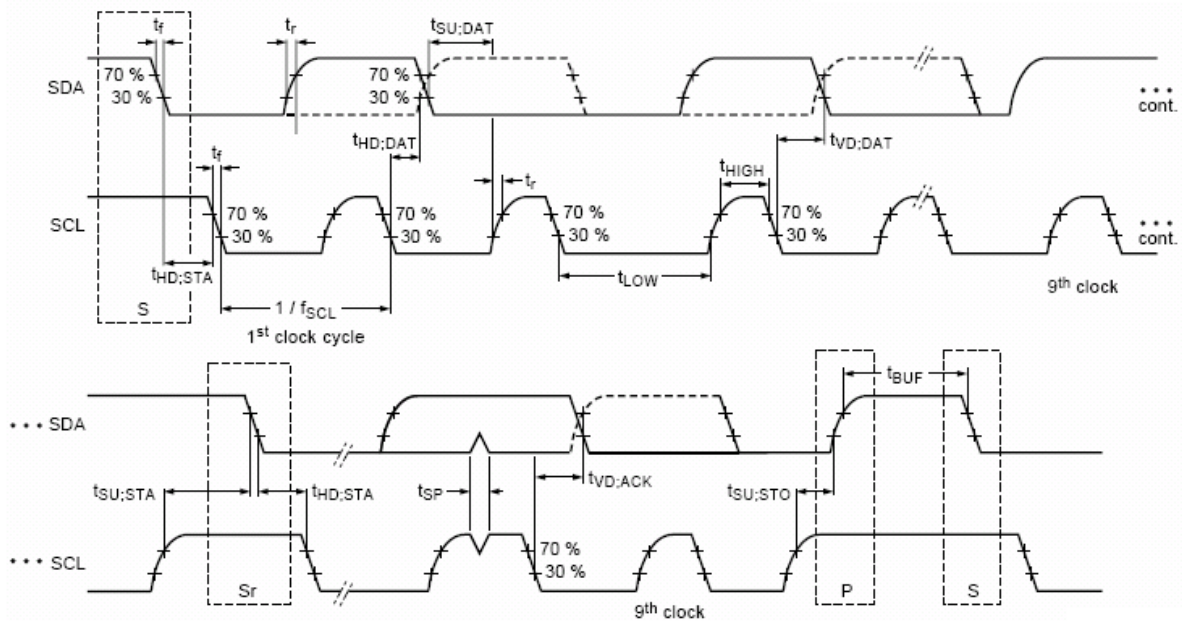


Table 32. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$			6 3	MHz
DC	SCLK duty cycle			50		%
T_{SETUP}	MISO to SCLK setup time	$V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$	60 100			ns
T_{HOLD}	SCLK to MISO hold time		40			ns
T_{OUT_VAL}	SCLK to MOSI valid time				40	ns
T_{OUT_HIGH}	MOSI high time		40			ns

Figure 16. SPI Master Mode 0 and 2

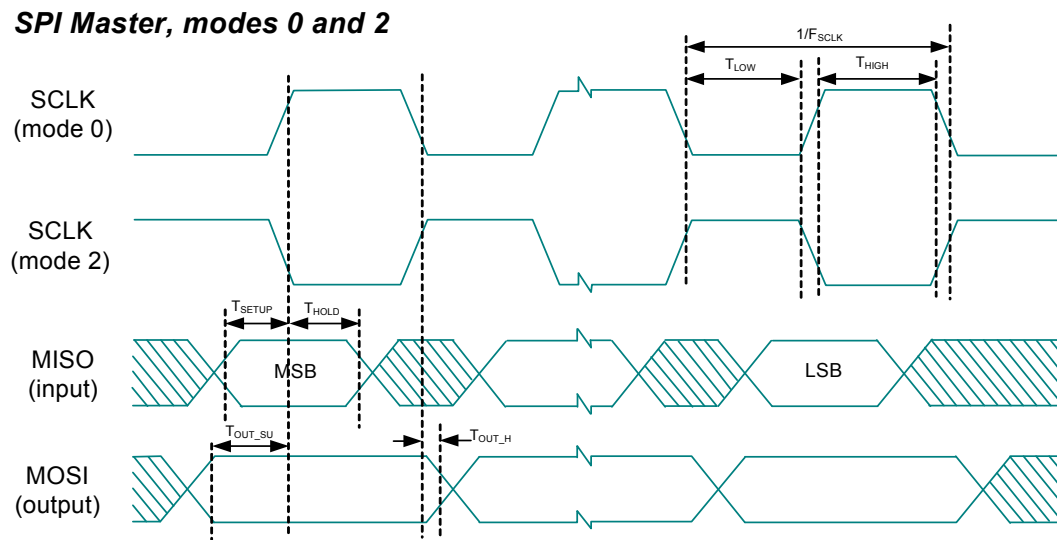
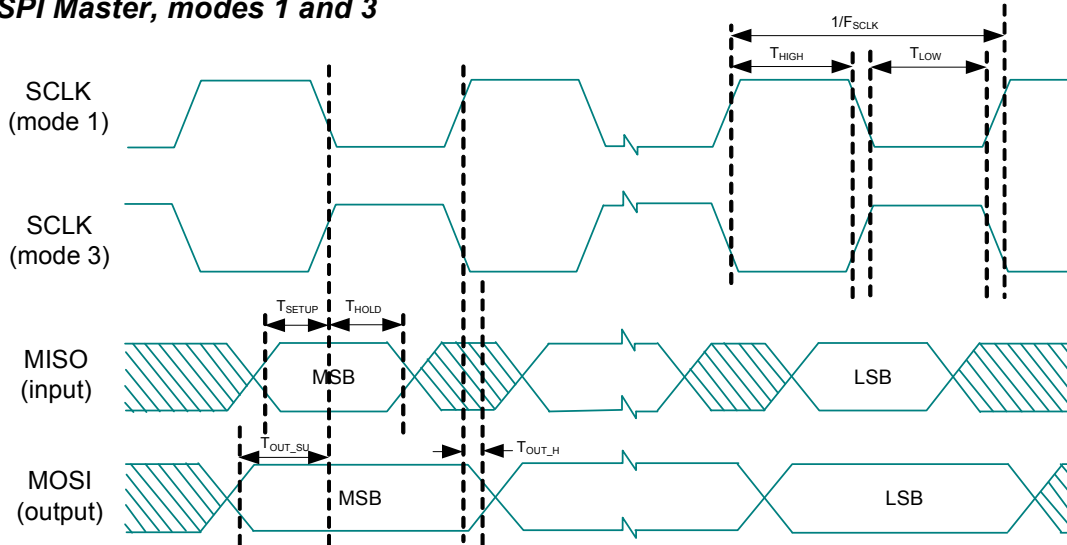


Figure 17. SPI Master Mode 1 and 3
SPI Master, modes 1 and 3

Table 33. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$			12 6	MHz
T_{LOW}	SCLK low time		41.67			ns
T_{HIGH}	SCLK high time		41.67			ns
T_{SETUP}	MOSI to SCLK setup time		30			ns
T_{HOLD}	SCLK to MOSI hold time		50			ns
T_{SS_MISO}	SS high to MISO valid				153	ns
T_{SCLK_MISO}	SCLK to MISO valid				125	ns
T_{SS_HIGH}	SS high time				50	ns
T_{SS_CLK}	Time from SS low to first SCLK		2/SCLK			ns
T_{CLK_SS}	Time from last SCLK to SS high		2/SCLK			ns

Figure 18. SPI Slave Mode 0 and 2

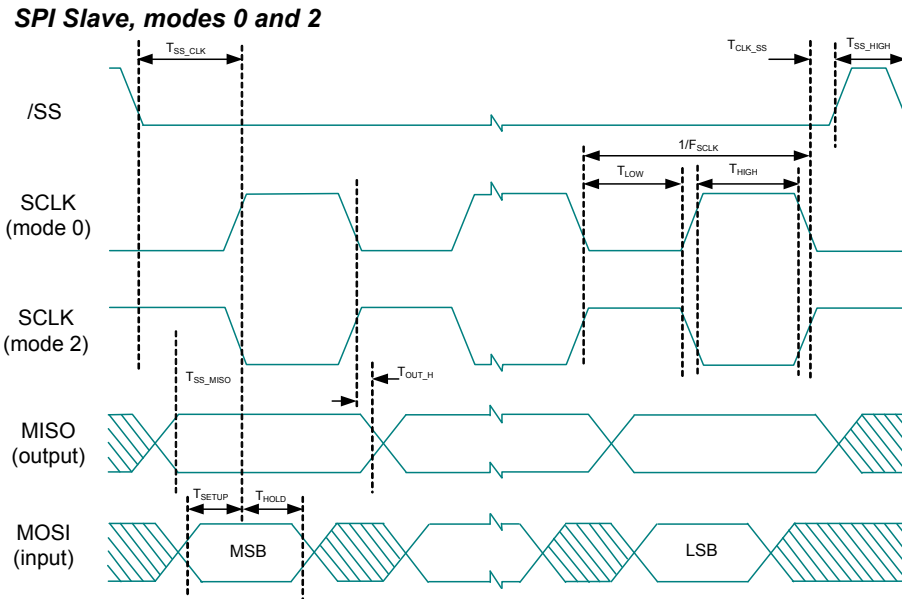
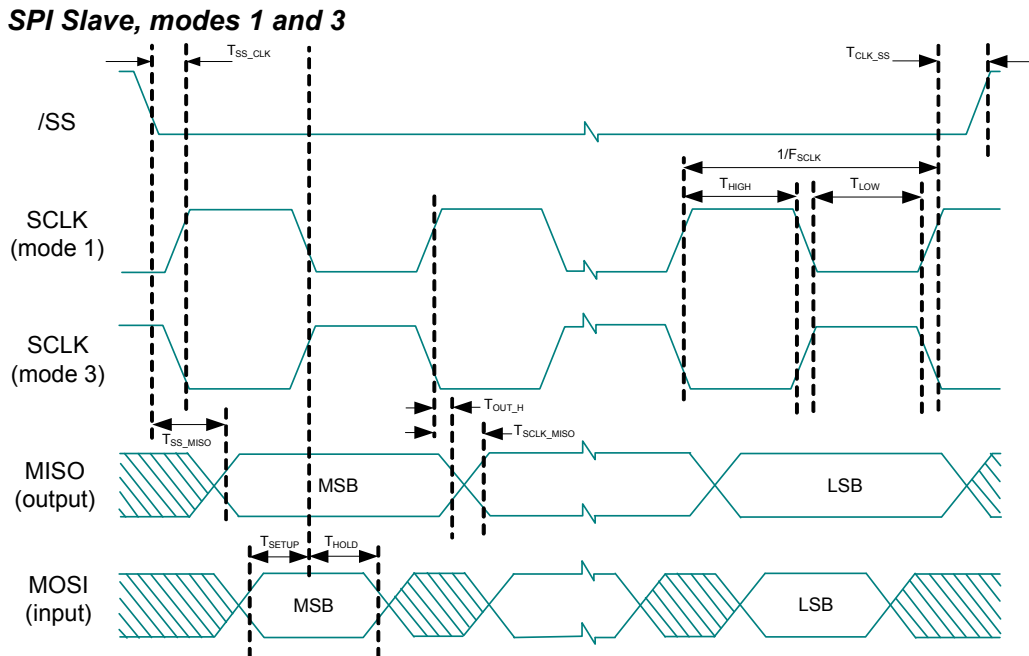


Figure 19. SPI Slave Mode 1 and 3

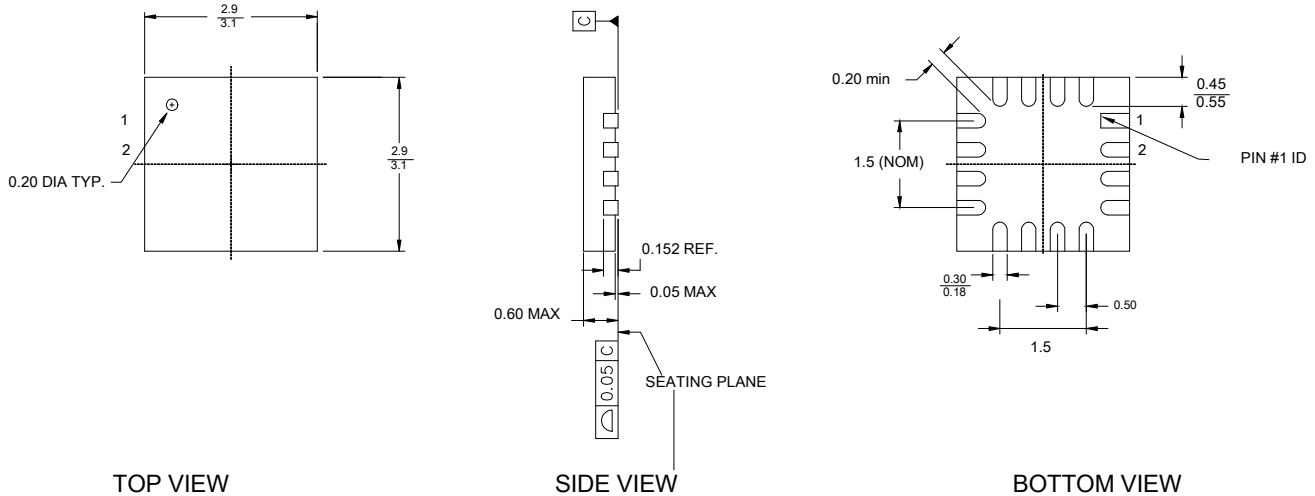


Packaging Information

This section illustrates the packaging specifications for the CY8C20x36A/46A/66A/96A PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at <http://www.cypress.com/design/MR10161>.

Figure 20. 16-pin QFN No E-pad 3x3x0.6 mm Package Outline (Sawn)



TOP VIEW

SIDE VIEW

BOTTOM VIEW

PART NO.	DESCRIPTION
LG16A	LEAD-FREE
LD16A	STANDARD

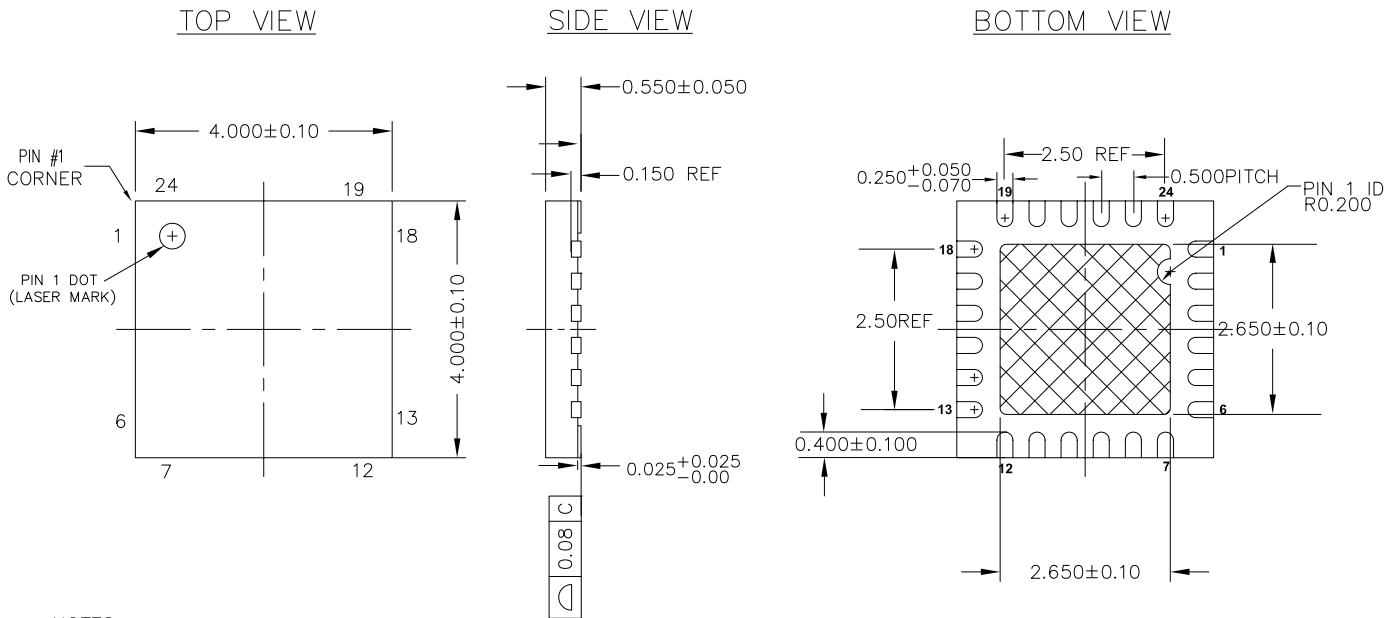
NOTES:

1. JEDEC # MO-220
2. Package Weight: 0.014g
3. DIMENSIONS IN MM, MIN


MAX

001-09116 *E

Figure 21. 24-Pin (4x4x0.6 mm) QFN

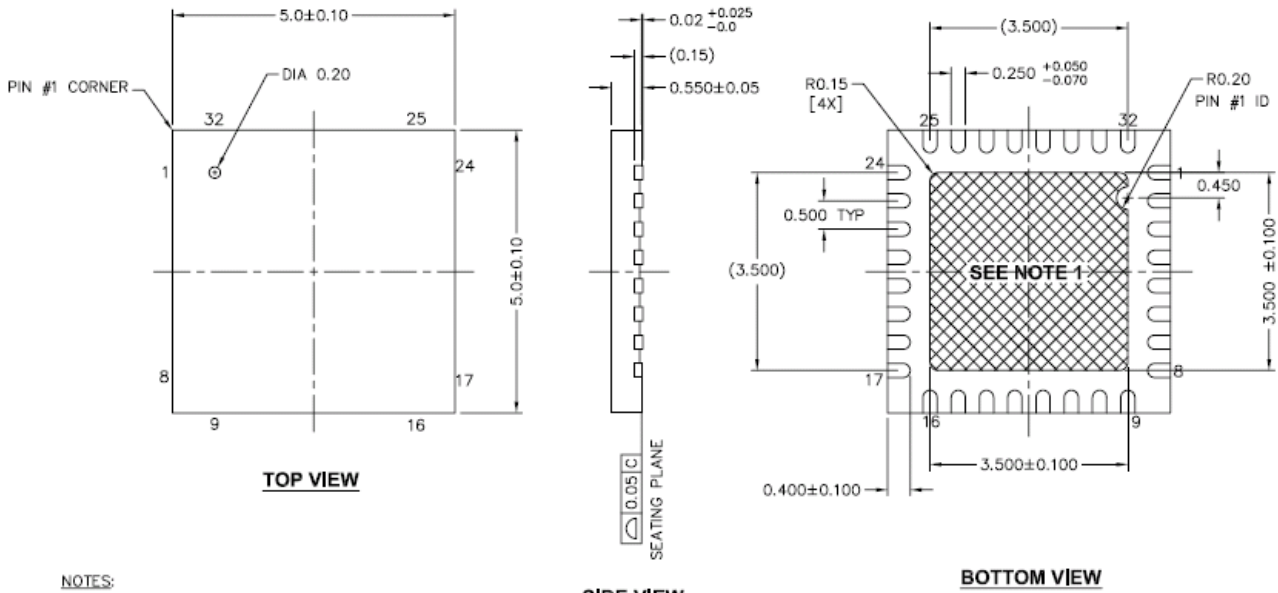


NOTES :


1.  HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. UNIT PACKAGE WEIGHT : 0.024 grams
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *C

Figure 22. 32-Pin (5x5x0.6 mm) QFN

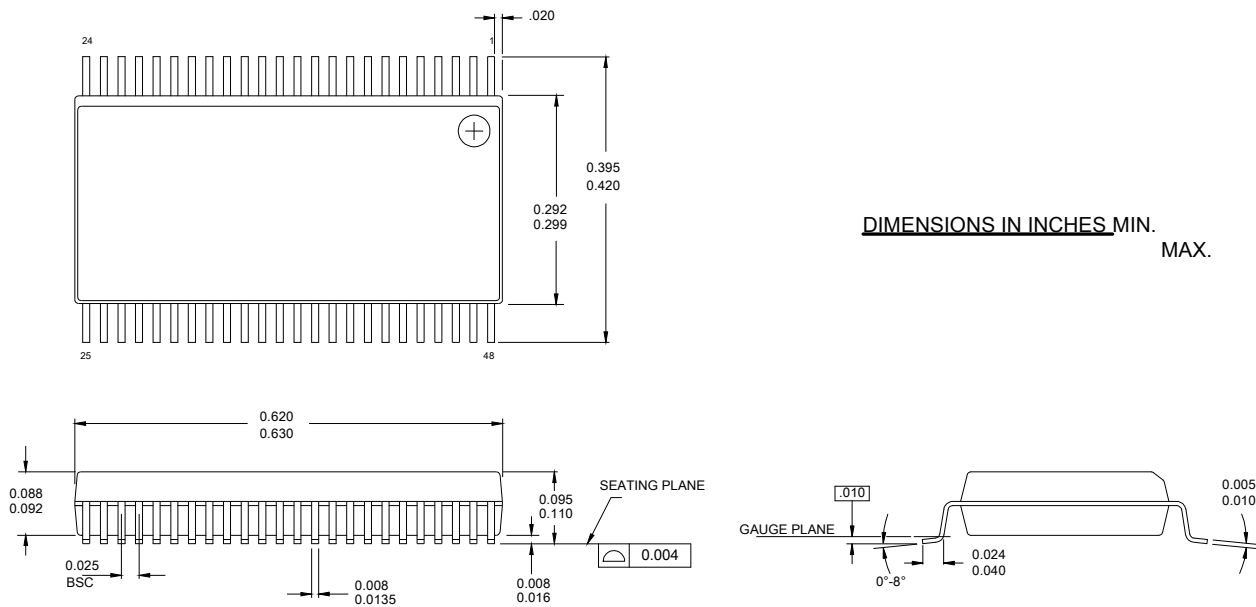


NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

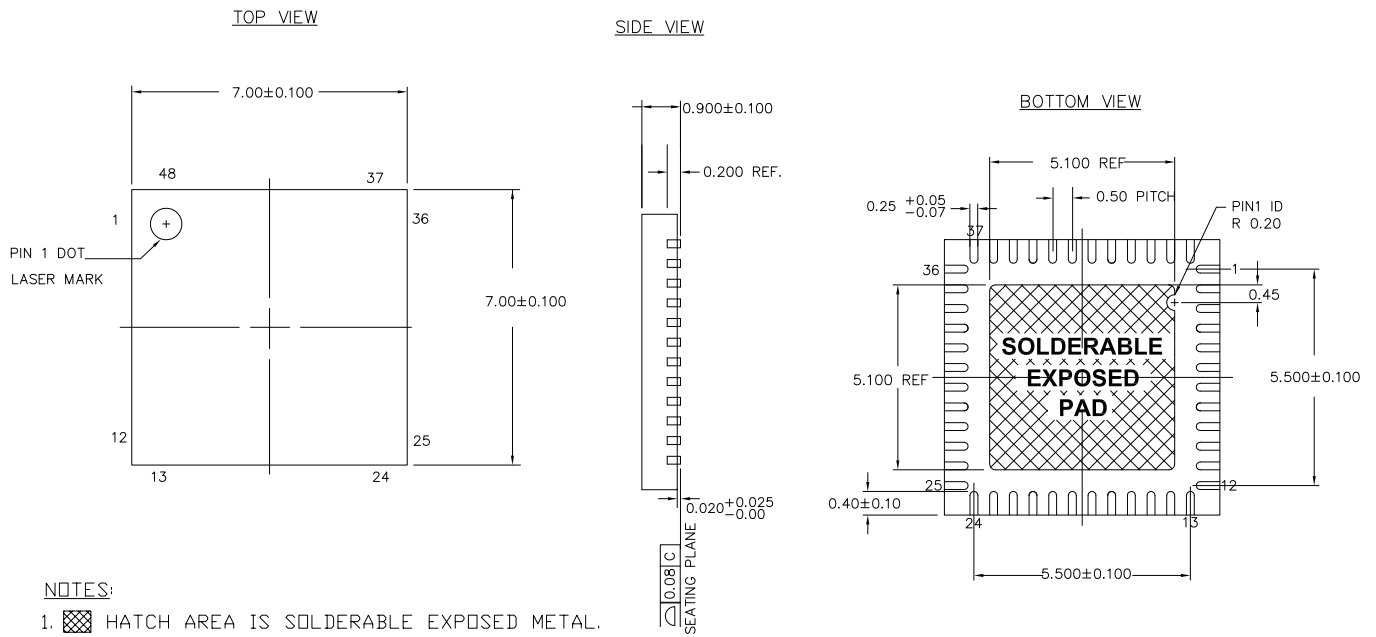
001-42168 *D

Figure 23. 48-Pin (300 MIL) SSOP



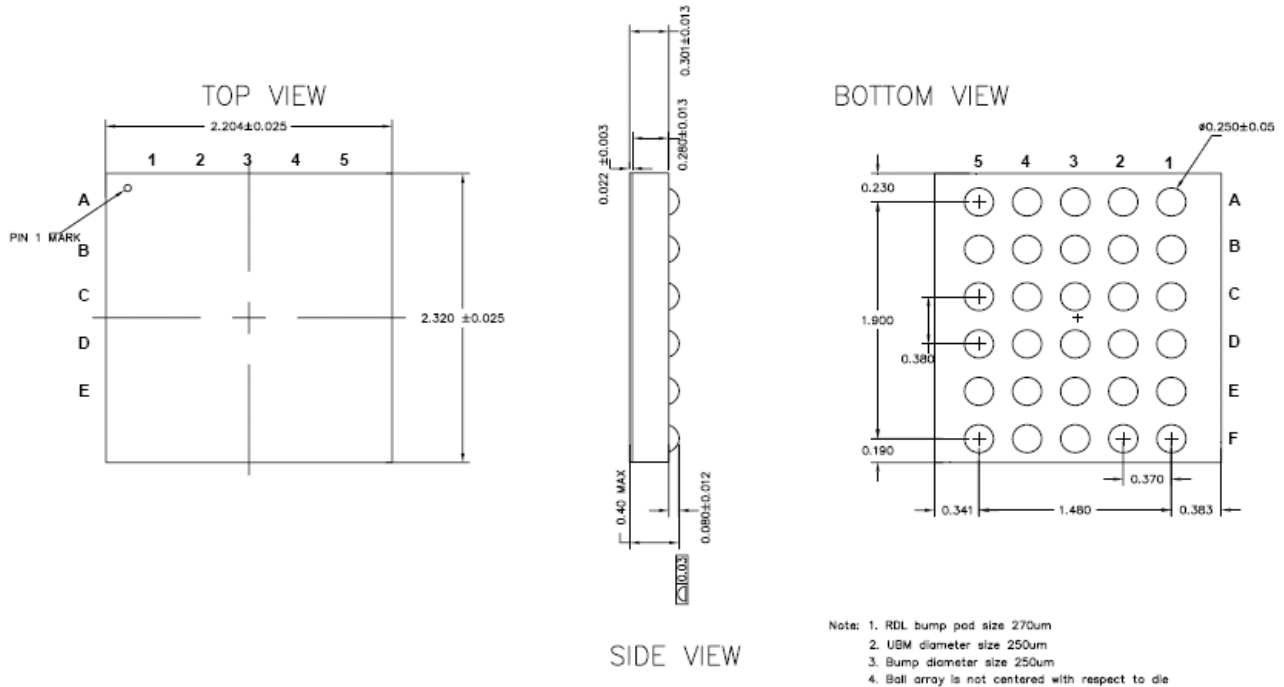
51-85061 *D

Figure 24. 48-Pin (7x7x1.0 mm) QFN



001-13191 *E

Figure 25. 30-Ball (2.2x2.32x0.40 mm) WLCSP



* ALL DIMENSION ARE IN MILLIMETER
 Package weight : TBD
 Jedec Publication 95

001-50669 *B

Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Thermal Impedances

Table 34. Thermal Impedances per Package

Package	Typical θ_{JA} [1]
16 Pin QFN	33 °C/W
24 Pin QFN ^[2]	21 °C/W
32 Pin QFN ^[2]	20 °C/W
48 Pin SSOP	69 °C/W
48 Pin QFN ^[2]	18 °C/W
30 Ball WLCSP	54 °C/W

- $T_J = T_A + \text{Power} \times \theta_{JA}$.
- To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

Capacitance on Crystal Pins

Table 35. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32 Pin QFN	3.2 pF
48 Pin QFN	3.3 pF

Solder Reflow Peak Temperature

This table lists the minimum solder reflow peak temperature to achieve good solderability.

Table 36. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature ^[1]	Maximum Peak Temperature
16 Pin QFN	240 °C	260 °C
24 Pin QFN	240 °C	260 °C
32 Pin QFN	240 °C	260 °C
48 Pin SSOP	220 °C	260 °C
48 Pin QFN	240 °C	260 °C
30 Ball WLCSP	240 °C	260 °C

- Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are $220 \pm 5^\circ\text{C}$ with Sn-Pb or $245 \pm 5^\circ\text{C}$ with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows XP and Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers. PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family. PSoC Designer is available free of charge at <http://www.cypress.com/psocdesigner> and includes a free C compiler.

PSoC Designer Software Subsystems

You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time. Code Generation Tools PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices. The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24MHz) operation.

Standard Cypress PSoC IDE tools are available for debugging the CY8C20x36A/46A/66A/96A family of parts. However, the additional trace length and a minimal ground plane in the Flex-Pod can create noise problems that make it difficult to debug the design. A custom bonded On-Chip Debug (OCD) device is available in a 48-pin QFN package. The OCD device is recommended for debugging designs that have high current and/or high analog accuracy requirements. The QFN package is compact and is connected to the ICE through a high density connector.

PSoC Programmer

PSoC Programmer is flexible enough and is used on the bench in development and is also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of cost at <http://www.cypress.com/psocprogrammer>.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66A Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466A-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466A-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443A-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466A-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3280-20x66 Universal CapSense Controller

The CY3280-20X66 CapSense Controller Kit is designed for easy prototyping and debug of CY8C20xx6A CapSense Family designs with pre-defined control circuitry and plug-in hardware. Programming hardware and an I2C-to-USB bridge are included for tuning and data acquisition.

The kit includes:

- CY3280-20x66 CapSense Controller Board
- CY3240-I2USB Bridge
- CY3210 MiniProg1 Programmer
- USB 2.0 Retractable Cable
- CY3280-20x66 Kit CD

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.

Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)
Table 37. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit ^[1]	Foot Kit ^[2]	Adapter ^[3]
CY8C20236A-24LKXI	16 QFN	CY3250-20246QFN	CY3250-16QFN-FK	See note 2
CY8C20246A-24LKXI	16 QFN	CY3250-20246QFN	CY3250-16QFN-FK	See note 3
CY8C20336A-24LQXI	24 QFN	CY3250-20346QFN	CY3250-24QFN-FK	See note 2
CY8C20346A-24LQXI	24 QFN	CY3250-20346QFN	CY3250-24QFN-FK	See note 3
CY8C20396A-24LQXI	24 QFN	Not Supported		
CY8C20436A-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 2
CY8C20446A-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 3
CY8C20466A-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 3
CY8C20496A-24LQXI	32 QFN	Not Supported		
CY8C20536A-24PVXI	48 SSOP	CY3250-20566	CY3250-48SSOP-FK	See note 3
CY8C20546A-24PVXI	48 SSOP	CY3250-20566	CY3250-48SSOP-FK	See note 3
CY8C20566A-24PVXI	48 SSOP	CY3250-20566	CY3250-48SSOP-FK	See note 3
CY8C20636A-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 3
CY8C20646A-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 3
CY8C20666A-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 3

1. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.

2. Foot kit includes surface mount feet that can be soldered to the target PCB.

3. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at <http://www.emulation.com>.

Third Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at <http://www.cypress.com> under Documentation > Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note "Debugging - Build a PSoC Emulator into Your Board - AN2323" at <http://www.cypress.com/?rID2748>.

Ordering Information

The following table lists the CY8C20x36A/46A/66A/96A PSoC devices' key package features and ordering codes..

Table 38. PSoC Device Key Features and Ordering Information

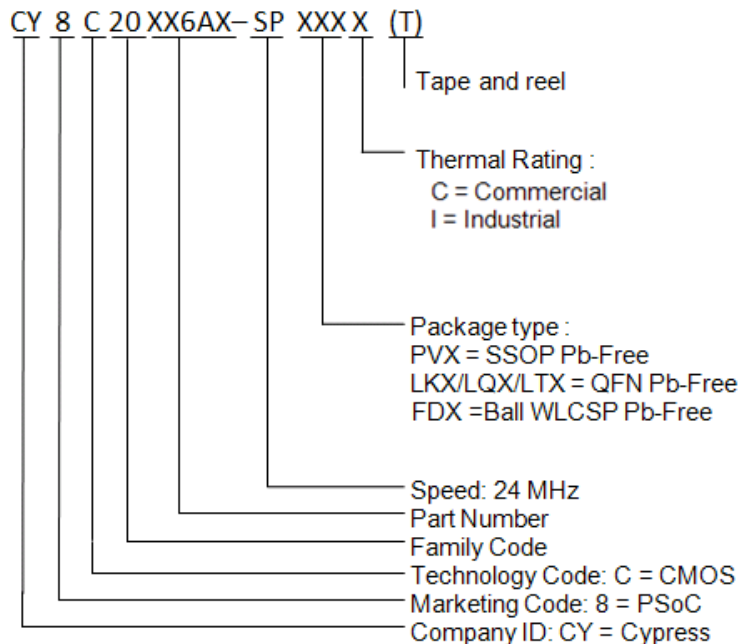
Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs ^[1]	XRES Pin	USB	ADC
16-Pin (3x3x0.6 mm) QFN	CY8C20236A-24LKXI	8K	1K	1	13	13	Yes	No	Yes
16-Pin (3x3x0.6 mm) QFN (Tape and Reel)	CY8C20236A-24LKXIT	8K	1K	1	13	13	Yes	No	Yes
16 Pin (3x3 x 0.6 mm) QFN	CY8C20246A-24LKXI	16K	2K	1	13	13	Yes	No	Yes
16 Pin (3x3 x 0.6 mm) QFN (Tape and Reel)	CY8C20246A-24LKXIT	16K	2K	1	13	13	Yes	No	Yes
24-Pin (4x4x0.6mm) QFN	CY8C20336A-24LQXI	8K	1K	1	20	20	Yes	No	Yes
24-Pin (4x4x0.6 mm) QFN (Tape and Reel)	CY8C20336A-24LQXIT	8K	1K	1	20	20	Yes	No	Yes
24 Pin (4x4 x 0.6 mm) QFN	CY8C20346A-24LQXI	16K	2K	1	20	20	Yes	No	Yes
24 Pin (4x4 x 0.6 mm) QFN (Tape and Reel)	CY8C20346A-24LQXIT	16K	2K	1	20	20	Yes	No	Yes
24-Pin (4x4x0.6 mm) QFN	CY8C20396A-24LQXI	16K	2K	1	19	19	Yes	Yes	Yes
24-Pin (4x4x0.6 mm) QFN (Tape and Reel)	CY8C20396A-24LQXIT	16K	2K	1	19	19	Yes	Yes	Yes
32-Pin (5x5x0.6 mm) QFN	CY8C20436A-24LQXI	8K	1K	1	28	28	Yes	No	Yes
32-Pin (5x5x0.6 mm) QFN (Tape and Reel)	CY8C20436A-24LQXIT	8K	1K	1	28	28	Yes	No	Yes
32 Pin (5x5 x 0.6 mm) QFN	CY8C20446A-24LQXI	16K	2K	1	28	28	Yes	No	Yes
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20446A-24LQXIT	16K	2K	1	28	28	Yes	No	Yes
32 Pin (5x5 x 0.6 mm) QFN	CY8C20466A-24LQXI	32K	2K	1	28	28	Yes	No	Yes
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20466A-24LQXIT	32K	2K	1	28	28	Yes	No	Yes
32 Pin (5x5 x 0.6 mm) QFN	CY8C20496A-24LQXI	16K	2K	1	25	25	Yes	Yes	Yes
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20496A-24LQXIT	16K	2K	1	25	25	Yes	Yes	Yes
48-Pin SSOP	CY8C20536A-24PVXI	8K	1K	1	34	34	Yes	No	Yes
48-Pin SSOP (Tape and Reel)	CY8C20536A-24PVXIT	8K	1K	1	34	34	Yes	No	Yes
48-Pin SSOP	CY8C20546A-24PVXI	16K	2K	1	34	34	Yes	No	Yes
48-Pin SSOP (Tape and Reel)	CY8C20546A-24PVXIT	16K	2K	1	34	34	Yes	No	Yes
48-Pin SSOP	CY8C20566A-24PVXI	32K	2K	1	34	34	Yes	No	Yes
48-Pin SSOP (Tape and Reel)	CY8C20566A-24PVXIT	32K	2K	1	34	34	Yes	No	Yes
48 Pin (7x7 mm) QFN	CY8C20636A-24LTXI	8K	1K	1	36	36	Yes	No	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20636A-24LTXIT	8K	1K	1	36	36	Yes	No	Yes
48 Pin (7x7 mm) QFN	CY8C20646A-24LTXI	16K	2K	1	36	36	Yes	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20646A-24LTXIT	16K	2K	1	36	36	Yes	Yes	Yes
48 Pin (7x7 mm) QFN	CY8C20666A-24LTXI	32K	2K	1	36	36	Yes	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20666A-24LTXIT	32K	2K	1	36	36	Yes	Yes	Yes
48 Pin (7x7 mm) QFN (OCD) ^[1]	CY8C20066A-24LTXI	32K	2K	1	36	36	Yes	Yes	Yes
30-Pin WLCSP	CY8C20746A-24FDXC	16K	1K	1	27	27	Yes	No	Yes
30-Pin WLCSP (Tape and Reel)	CY8C20746A-24FDXCT	16K	1K	1	27	27	Yes	No	Yes

Table 38. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs ^[1]	XRES Pin	USB	ADC
30-Pin WLCSP	CY8C20766A-24FDXC	32K	2K	1	27	27	Yes	No	Yes
30-Pin WLCSP (Tape and Reel)	CY8C20766A-24FDXCT	32K	2K	1	27	27	Yes	No	Yes
24-Pin (4x4x0.6mm) QFN	CY8C20336AN-24LQXI	8K	1K	1	20	20	Yes	No	No
24-Pin (4x4x0.6mm) QFN (Tape and Reel)	CY8C20336AN-24LQXIT	8K	1K	1	20	20	Yes	No	No
32-Pin (5x5x0.6mm) QFN	CY8C20436AN-24LQXI	8K	1K	1	28	28	Yes	No	No
32-Pin (5x5x0.6mm) QFN (Tape and Reel)	CY8C20436AN-24LQXIT	8K	1K	1	28	28	Yes	No	No
48 Pin (7x7 mm) QFN	CY8C20636AN-24LTXI	8K	1K	1	36	36	Yes	No	No
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20636AN-24LTXIT	8K	1K	1	36	36	Yes	No	No

1. Dual-function Digital I/O Pins also connect to the common analog mux.

Ordering Code Definitions



Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
DAC	digital-to-analog converter
DC	direct current
EOP	end of packet
FSR	full scale range
GPIO	general purpose input/output
GUI	graphical user interface
I ² C	inter-integrated circuit
ICE	in-circuit emulator
IDAC	digital analog converter current
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
ISSP	in-system serial programming
LCD	liquid crystal display
LDO	low dropout (regulator)
LSB	least-significant bit
LVD	low voltage detect
MCU	micro-controller unit
MIPS	mega instructions per second
MISO	master in slave out
MOSI	master out slave in
MSB	most-significant bit
OCD	on-chip debugger
POR	power on reset
PPOR	precision power on reset
PSRR	power supply rejection ratio
PWRSYS	power system
PSoC®	Programmable System-on-Chip
SLIMO	slow internal main oscillator
SRAM	static random access memory
SNR	signal to noise ratio
QFN	quad flat no-lead
SCL	serial I ² C clock
SDA	serial I ² C data
SDATA	serial ISSP data
SPI	serial peripheral interface
SS	slave select
SSOP	shrink small outline package
TC	test controller
USB	universal serial bus
USB D+	USB Data +
USB D-	USB Data-
WLCSP	wafer level chip scale package
XTAL	crystal

Units of Measure

Table 39 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

Table 39. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femto farad
g	gram
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
KHz	kilohertz
Ksps	kilo samples per second
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μW	microwatts
mA	milli-ampere
ms	milli-second
mV	milli-volts
nA	nanoampere
ns	nanosecond
nV	nanovolts
Ω	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
s	sigma: one standard deviation
V	volts
W	watt

Glossary

Crosspoint connection	Connection between any GPIO combination via analog multiplexer bus.
Differential non-linearity	Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step.
Hold time	Hold time is the time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.
I²C	It is a serial multi-master bus used to connect low speed peripherals to MCU.
Integral nonlinearity	It is a term describing the maximum deviation between the ideal output of a DAC/ADC and the actual output level.
Latch up current	Current at which the latch up test is conducted according to JESD78 standard (at 125 degree celsius)
Power supply rejection ratio (PSRR)	The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage of the device.
Scan	The conversion of all sensor capacitances to digital values.
Setup time	Period required to prepare a device, machine, process, or system for it to be ready to function.
Signal-to-noise ratio	The ratio between a capacitive finger signal and system noise.
SPI	Serial peripheral interface is a synchronous serial data link standard.

Reference Documents

- Technical reference manual for [CY8C20xx6](#) devices
- In-system Serial Programming (ISSP) protocol for 20xx6 – [AN2026C](#)
- Host Sourced Serial Programming for 20xx6 devices – [AN59389](#)

Document History Page

Document Title: CY8C20X36A/46A/66A/96A CapSense® Applications Document Number: 001-54459				
Revision	ECN	Origin of Change	Submission Date	Description of Change
**	2737924	SNV	07/14/09	New silicon and document
*A	2764528	MATT	09/16/2009	Updated AC Chip Level Specifications Updated ADC User Module Electrical Specifications table Added Note 5. Added SR _{POWER_UP} parameter. Updated Ordering information. Updated Capacitance on Crystal Pins
*B	2803229	VZD	11/10/09	Added Contents on page 3 . Added Note 6 on page 20. Edited Features section to include reference to Incremental ADC.
*C	2846083	DST/KEJO	01/12/2010	Updated AC Programming Specifications on page 27 per CDT 56531 Updated Idd typical values in DC Chip-Level Specifications on page 18 . Added 30-pin WLCSP pin and package details Added Contents on page 2.
*D	2935141	KEJO/ISW/SSHH	03/05/2010	Updated Features on page 1 . Added SmartSense™ on page 4 . Updated PSoC® Functional Overview on page 4 . Removed SNR statement regarding on page 4 (Analog Multiplexer section). Updated on page 5 with the I2C enhanced slave interface point. Removed references to “system level” in Designing with PSoC Designer on page 6 . Changed TC CLK and TC DATA to ISSP CLK and ISSP DATA respectively in all the pinouts. Modified notes in Pinouts. Updated 30-ball pin diagram. Removed IMO frequency trim options diagram in Electrical Specifications on page 17 . Updated and formatted values in DC and AC specifications. Updated Ordering information table. Updated 48-pin SSOP package diagram. Added 30-Ball WLCSP package spec 001-50669. Removed AC Analog Mux Bus Specifications section. Added SPI Master and Slave mode diagrams. Modified Definition for Timing for Fast/Standard Mode on the I2C Bus on page 28 . Updated Thermal Impedances on page 37 . Combined Development Tools with Development Tool Selection on page 38 . Removed references to “system level”. Updated Evaluation Tools on page 39 . Added Ordering Code Definitions on page 42 . Updated Acronyms Used on page 43 . Added Glossary and Reference Documents on page 44 Changed data sheet status from Preliminary to Final

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