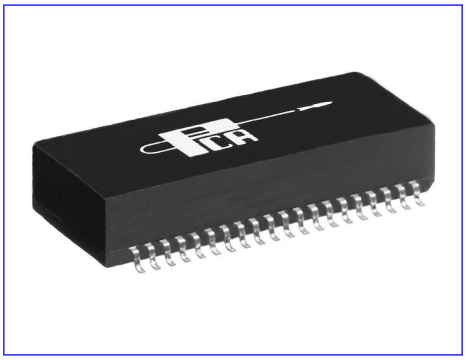
10/100 Base-X Module for ICS 1890 & SSI 78Q2120 Multi-Port Applications

EPF8047S



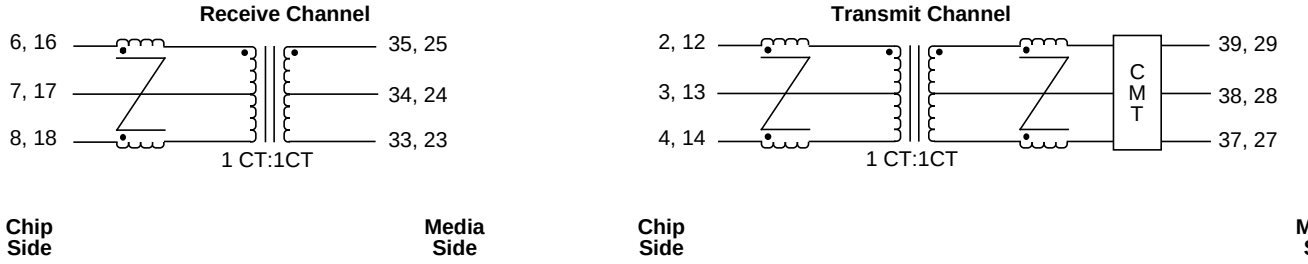
- Significantly improved common mode attenuation •
- Guaranteed to operate with 8 mA DC bias at 70°C •
- Complies with or exceeds IEEE 802.3, 10 BT/100 BX Standards •

Electrical Parameters @ 25° C

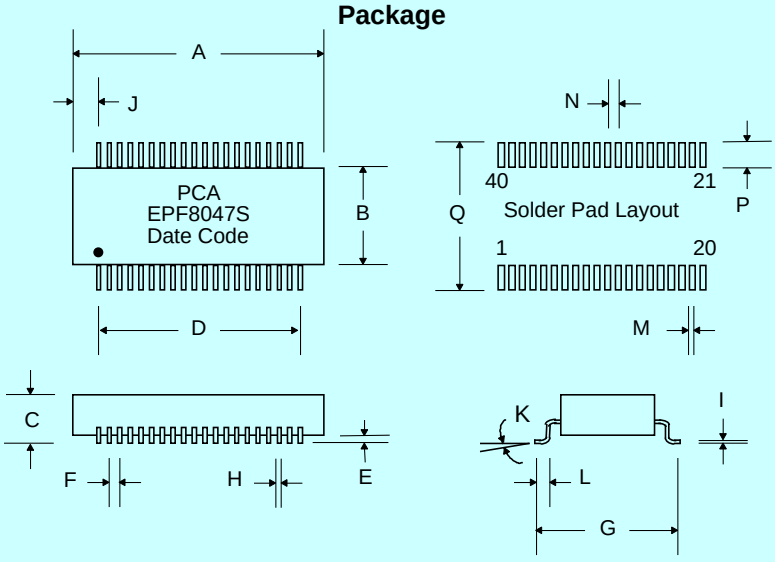
OCL @ 70°C	**Insertion Loss** (dB Max.)						**Return Loss** (dB Min.)						**Common Mode Rejection** (dB Min.)						**Crosstalk** (dB Min.) [Between Channels]	
100 KHz, 0.1 Vrms 8 mA DC Bias	0.1-80 MHz		80-100 MHz		150 MHz		1-30 MHz		30-60 MHz		100 MHz		30-100 MHz		200 MHz		300-500 MHz		0.1-60 MHz	60-100 MHz
Media Side	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv		
350µH	-1	-1	-1	-1	-3	-3	-18	-18	-18	-18	-10	-10	-40	-40	-30	-20	-20	-10	-35	-35

• **Isolation** : 1500 Vrms • **Impedance** : 100 Ω • **Rise Time** : 3.0 nS Max. •

Schematic



Package



Dimensions

Dim.	(Inches) Min.	Max.	Nom.	(Millimeters) Min.	Max.	Nom.
A	1.110	1.130		28.19	28.70	
B	.470	.490		11.94	12.45	
C	.240	.250		6.10	6.35	
D	.950	Typ.		24.13	Typ.	
E	.008	.012		.203	.305	
F	.050	Typ.		1.27	Typ.	
G	.620	.630		15.75..	16.00	
H	.016	.022		406	.559	
I	.008	.012		.203	.305	
J	.085	Typ.		2.16	Typ.	
K	0°	8°		0°	8°	
L	.045	Typ.		1.14	Typ.	
M			.030			.762
N			.050			1.27
P			.090			2.29
Q			.670			17.02

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CSF8047Sa Rev. Orig. 1/8/97

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The circuit below is a guideline for interconnecting PCA's EPF8047S with ICS 1890 chip for 10/100 Mb/s applications. Further details can be obtained from the chip manufacturer application notes. Connection to the alternative chip SSI 78Q2120 is straight forward; please consult the SSI data sheet recommendations for completing this project.

Typical insertion loss of the isolation transformer is 0.5dB. This parameter covers the entire spectrum of the encoded signals in 10/100 protocols. Under terminated conditions, to transmit a 2V pk-pk signal across the cable, you must adjust the chips supporting resistor to get at least 2.12V pk-pk across the transmit pins.

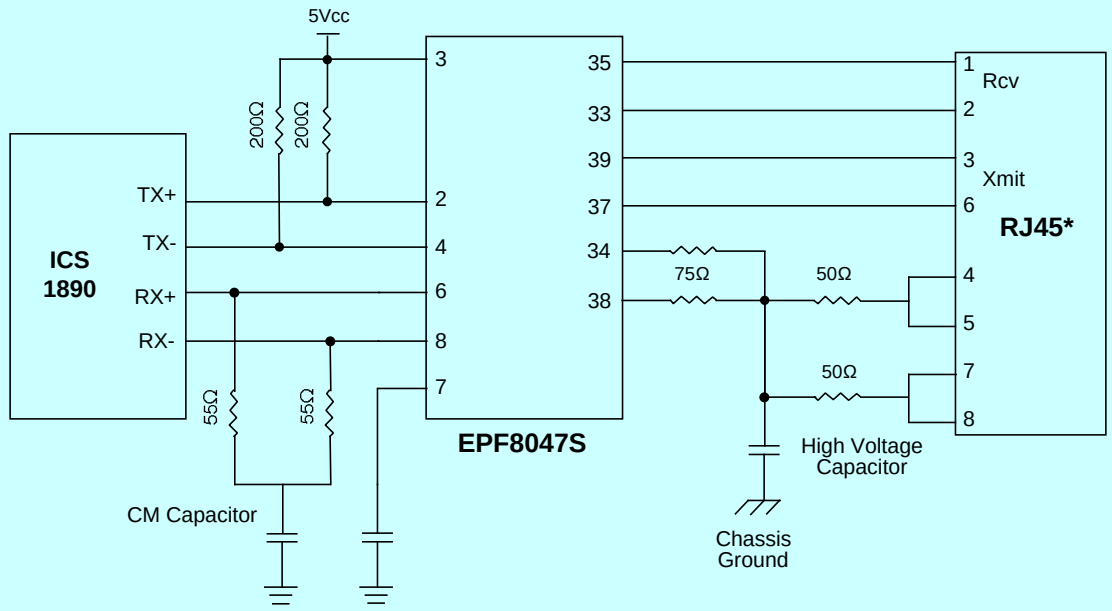
Primary side center taps can be returned to the chip side ground plane; but more often than not, if the ground plane is itself noisy, field experience has shown that it may worsen EMI situation. It is perhaps wiser to carefully lay the system borad so that substantial gain in EMI suppression is obtained from the so called "common mode termination" on the cable side as shown below. In any event, this configuration has been known to be quite successful in the field in EMI containment for similar applications.

The phantom resistors shown around the connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPF8047S. There need not be any ground plane beyond this plane.

For best results, PCB designer should design the outgoing traces preferably to be 50 Ω, balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit for UTP (only one port shown)



Notes : Only one port shown for Hub side connection.

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