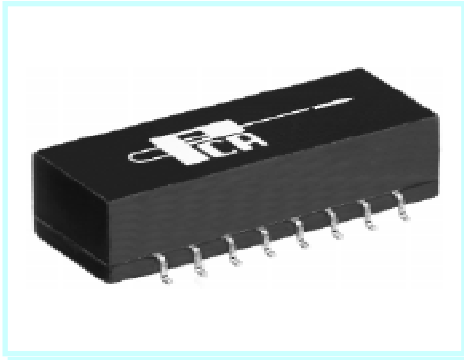


100 Base-X Interface Module

EPF8019GM



- Optimized to work with ML6692/94 PHY chip •
- Guaranteed to operate with 8 mA DC bias at 70°C on cable side •
- Complies with or exceeds IEEE 802.3, 100 BX Standards •
- Robust construction allows for severe soldering processes •

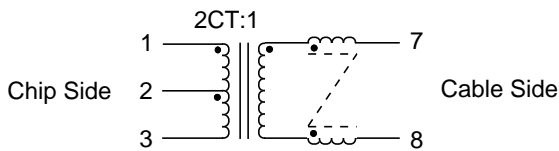
Electrical Parameters @ 25° C

OCL (μ H Min.)	Insertion Loss (dB Max.)				Return Loss (dB Min.)						Common Mode Rejection (dB Min.)						Crosstalk (dB Min.) [Between Channels]
	1-80 MHz		80-100 MHz		1-30 MHz		30-60 MHz		60-100 MHz		1-30 MHz		30-100 MHz		100-200 MHz		
100 KHz, 0.1 Vrms 8 mA DC Bias @ 70°C																	
Cable Side	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	
350	-1	-1	-2	-2	-18	-18	-12	-12	-8	-10	-40	-40	-30	-30	-25	-25	-40

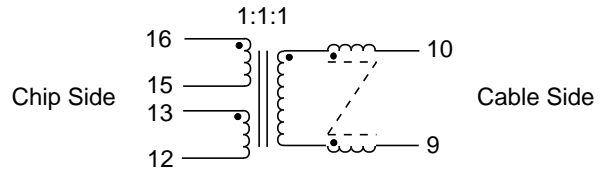
• Isolation : 1500 Vrms • Cable Impedance : 100 Ω •

Schematic

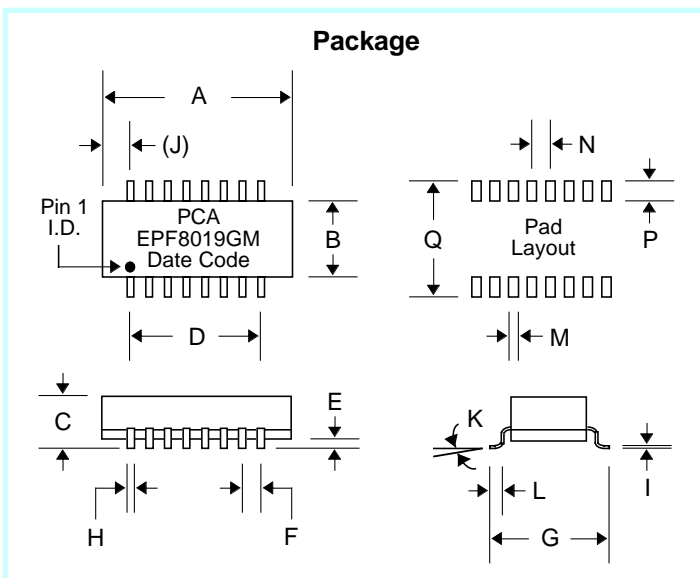
Transmit Channel



Receive Channel



Package



Dimensions

Dim.	(Inches)			(Millimeters)		
	Min.	Max.	Nom.	Min.	Max.	Nom.
A	.970	.990	.980	24.64	25.15	24.89
B	.380	.400	.390	9.65	10.16	9.91
C	.225	.245	.235	5.72	6.22	5.97
D	---	---	.700	---	---	17.78
E	.010	.015	.013	.254	.381	.330
F	---	---	.100	---	---	2.54
G	.500	.520	.510	12.70	13.20	12.95
H	.018	.022	.020	.457	.559	.508
I	.008	.012	.010	.203	.305	.254
J	---	---	.140	---	---	3.56
K	0°	8°	---	0°	8°	---
L	.025	.045	.035	.635	1.14	.889
M	---	---	.030	---	---	.762
N	---	---	.100	---	---	2.54
P	---	---	.090	---	---	2.29
Q	---	---	.560	---	---	14.22

EPF8019GM

The circuit below is a guideline for interconnecting PCA's EPF8019GM with ML6692 or ML6694 chip applications. Further details can be obtained from the chip manufacturer application notes.

Typical insertion loss of the isolation transformer is 0.5dB. This parameter covers the entire spectrum of the encoded signals in 100 BX protocol. Under terminated conditions, to transmit a 2V pk-pk signal across the cable, you must adjust the chips supporting resistor to get at least 2.12V pk-pk across the transmit pins.

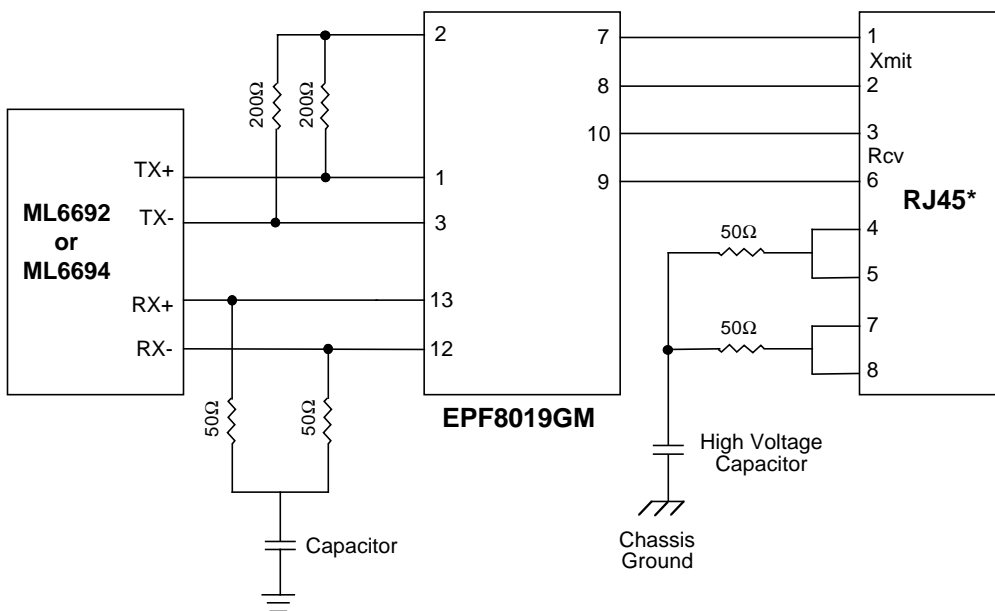
Note that in the 100 BX application, you need to use only one half of the RCV side primary winding and terminate it with 50 Ω balanced load as shown.

The phantom resistors shown around the connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPF8019GM. There need not be any ground plane beyond this plane.

For best results, PCB designer should design the outgoing traces preferably to be 50 Ω , balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit for UTP



Notes : * NIC Side is shown. Hub side connection will swap pins 3-6 with 1-2.