DSP56602

Advance Information
16-BIT DIGITAL SIGNAL PROCESSOR

The DSP56602 is a ROM-based 16-bit fixed-point CMOS Digital Signal Processor (DSP) designed for low-power digital cellular subscriber applications. This 60 MHz chip is optimized for processing-intensive, yet cost-effective, low power consumption digital mobile communications applications. The DSP56602 is a member of the DSP56600 core family of DSPs, and is capable of executing one instruction per clock cycle. The DSP56602 provides for customer-specifiable, factory-programmed ROM. Application development can be performed using the DSP56603EVM Evaluation Module or the DSP56603ADS Application Development System. **Figure 1** provides a block diagram of the DSP56602, showing the core structures and the expansion areas. The DSP56600 core includes the Data Arithmetic Logic Unit (Data ALU), Address Generation Unit (AGU), Program Controller, Program Patch Detector, Bus Interface Unit, On-Chip Emulation (OnCE™) module, JTAG port, and a Phase Lock Loop (PLL)-based clock generator. The expansion areas provide the program and data memories, as well as a versatile set of on-chip peripherals and external ports.

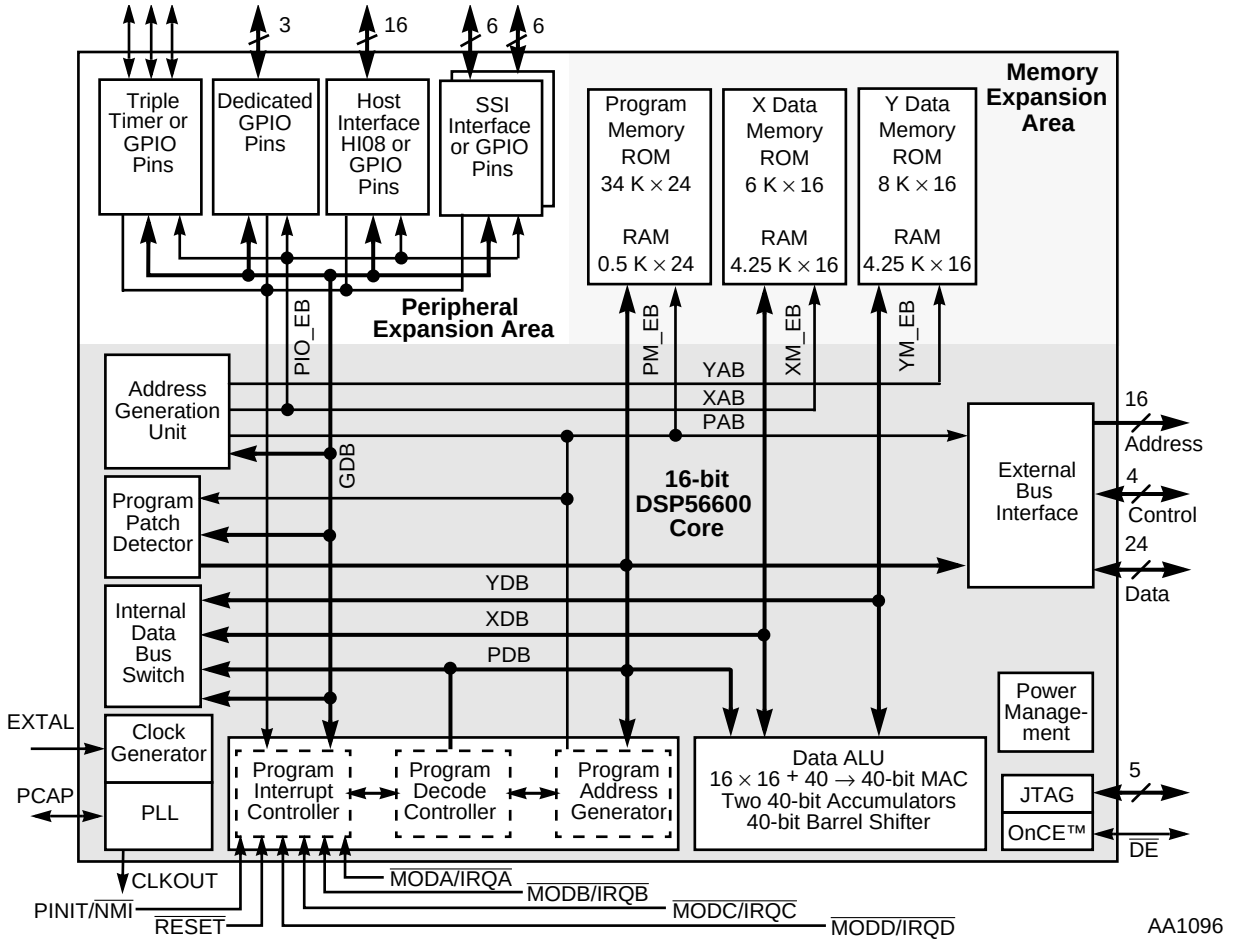

Figure 1 DSP56602 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preliminary Information

Rev. 1

DSP56602 FEATURES

Digital Signal Processing Core

- High-performance DSP56600 core
- Up to 60 Million Instructions Per Second (MIPS) at 2.7–3.3 V
- Fully pipelined 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Two 40-bit accumulators including extension bits
- 40-bit parallel barrel shifter
- Highly parallel instruction set with unique DSP addressing modes
- Code-compatible with the DSP56300 core
- Position-independent code support
- User-selectable stack extension
- Nested hardware DO loops
- Fast auto-return interrupts
- On-chip support for software patching and enhancements
- On-chip Phase Lock Loop (PLL) circuit
- Real-time trace capability via external address bus
- On-Chip Emulation (OnCE) module and JTAG port

Memory

- 34 K × 24 of customer-specifiable factory-programmed Program ROM
- 0.5 K × 24 of Program RAM
- 10.25 K × 16 of X data memory, organized as follows:
  - 6 K × 16 of X data ROM
  - 4.25 K × 16 of X data RAM
- 12.25 K × 16 of Y data memory, organized as follows:
  - 8 K × 16 of Y data ROM
  - 4.25 K × 16 of Y data RAM
- Off-chip expansion for both program fetch and program data transfers
- No additional logic needed for interface to external SRAM memories

Peripheral Circuits

- Three dedicated General Purpose Input / Output (GPIO) pins and as many as thirty-one additional GPIO pins (user-selectable as peripherals or GPIO pins)
- Host Interface (HI08) support: one 8-bit parallel port (or as many as sixteen additional GPIO pins)
  - Direct interface to Motorola HC11, Hitachi H8, 8051 family, and Thomson P6 family
  - Minimal logic interface to standard ISA bus, Motorola 68K family, and Intel x86 microprocessor family.
- Synchronous Serial Interface (SSI) support: two 6-pin ports (or twelve additional GPIO pins)
  - Supports serial devices with one or more industry-standard codecs, other DSPs, microprocessors, and Motorola SPI-compliant peripherals
  - Independent transmitter and receiver sections and a common SSI clock generator
  - Network mode using frame sync and up to 32 time slots
  - 8-bit, 12-bit, and 16-bit data word lengths
- Three programmable timers (or as many as three additional GPIO pins)
- Three external interrupt / mode control lines
- One external reset pin for hardware reset

Energy Efficient Design

- Very low power CMOS design
  - Operating voltage range: 1.8 V to 3.3 V
  - < 0.85 mA / MIPS at 2.7 V
  - < 0.55 mA / MIPS at 1.8 V
- Low power Wait for interrupt standby mode, and ultra low power Stop standby mode
- Fully static, HCMOS design for operating frequencies from 60 MHz down to 0 Hz (DC)
- Special power management circuitry

PRODUCT DOCUMENTATION

The three manuals listed in **Table 1** are required for a complete description of the DSP56602 and are necessary to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

Table 1 DSP56602 Chip Documentation

Topic	Description	Order Number
DSP56600 Family Manual	Detailed description of the DSP56600-family architecture, and 16-bit DSP core processor and the instruction set	DSP56600FM/AD
DSP56602 User's Manual	Detailed description of memory, peripherals, and interfaces of the DSP56602	DSP56602UM/AD
DSP56602 Technical Data sheet	Electrical and timing specifications, pin descriptions, and package descriptions	DSP56602/D

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