DSP56167

Advance Information
16-BIT DIGITAL SIGNAL PROCESSOR

The general-purpose, programmable DSP56167 is an enhanced version of the DSP56166 with added features. Designed primarily for speech coding and digital communications, the DSP56167 has a built-in ΣΔ codec and Phase Lock Loop (PLL). This MPU-style DSP also contains memories and digital peripherals that provide a cost effective, high performance solution to many DSP applications. On-Chip Emulation (OnCE™) circuitry provides convenient and inexpensive debug facilities normally available only through expensive external hardware. This RAM-based DSP contains a 2 K × 16 Program RAM and a 4 K × 16 data RAM. The Central Processing Unit (CPU) consists of three execution units operating in parallel allowing up to six operations to occur in an instruction cycle. This parallelism greatly increases the effective processing speed of the DSP56167. The MPU-style programming model and instruction set allow straightforward generation of efficient, compact code. The DSP56167 is a member of Motorola's DSP56100 family of 16-bit Digital Signal Processors (DSPs).

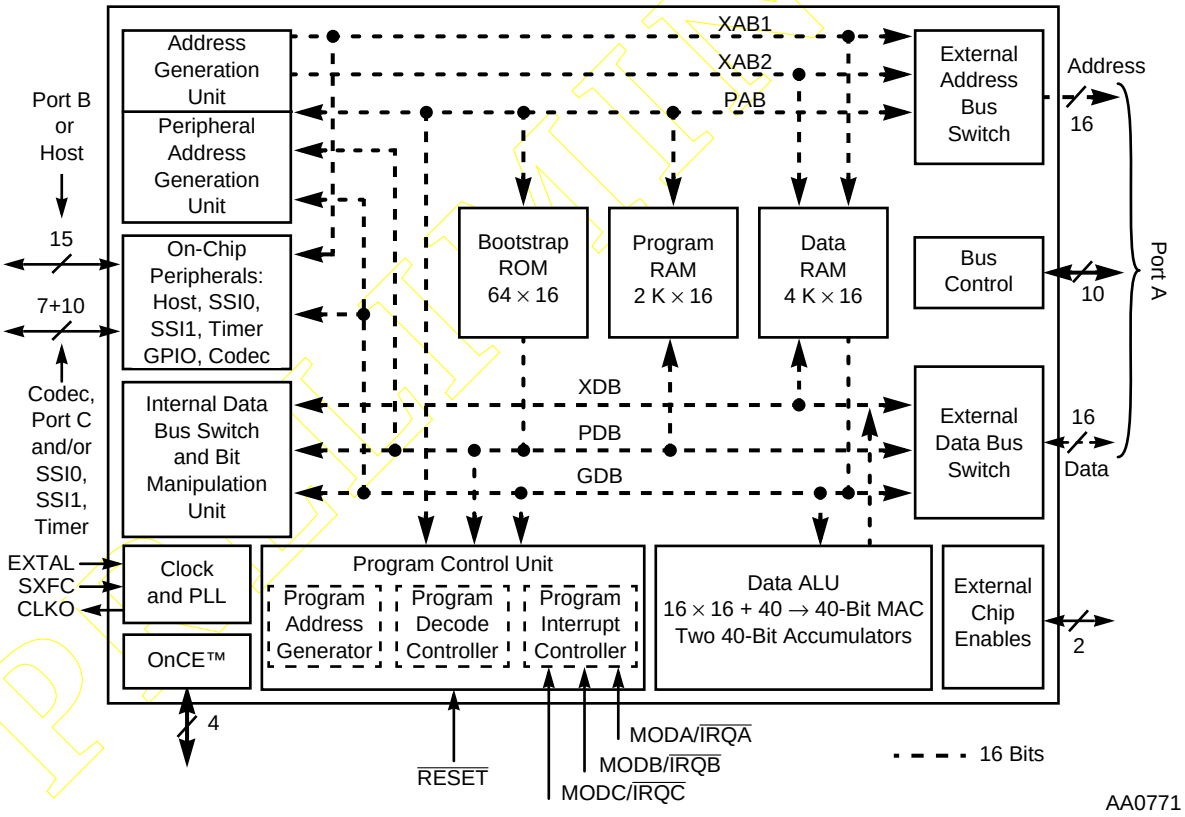


Figure 1 DSP56167 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

©1996, 1997 MOTOROLA, INC.

Downloaded from Elcodis.com electronic components distributor

TABLE OF CONTENTS

FOR TECHNICAL ASSISTANCE:

Telephone: 1 (800) 521-6274

Email: dsphelp@dsp.sps.mot.com

Internet: http://www.motorola-dsp.com

PRELIMINARY

Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low; for example, the $\overline{\text{RESET}}$ pin is active when low
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Downloaded from Elcodis.com electronic components distributor

FEATURES

- Digital Signal Processing Core
  - Up to 30 Million Instructions Per Second (MIPS) at 60 MHz with 33.3 ns instruction cycle
  - Single-cycle 16 × 16-bit parallel Multiply-Accumulate
  - 2 × 40-bit accumulators with extension byte
  - Fractional and integer arithmetic with support for multiprecision arithmetic
  - Highly parallel instruction set with unique DSP addressing modes
  - Nested hardware DO loops including infinite loops and DO zero loop
  - Two instruction LMS adaptive filter loop
  - Fast auto-return interrupts
  - Three external interrupt request pins
  - Three 16-bit internal data and three 16-bit internal address buses
  - Individual programmable wait states on the external bus for program, data, and peripheral memory spaces
  - Programmable absolute short addressing mode
  - Off-chip memory-mapped peripheral space with programmable access time and separate peripheral enable pin
  - Peripheral Address Generation Unit (PAGU)
  - On-chip memory-mapped peripheral registers
  - On-Chip Emulation (OnCE™) port for unobtrusive, processor speed-independent debugging with $\overline{DR}$ line static latch with Reset
- Memory
  - Modified Harvard architecture permits simultaneous accesses to program and data memories
  - 2 K × 16-bit on-chip Program RAM
  - 4 K × 16-bit on-chip data RAM
  - 64 × 16-bit bootstrap ROM
  - External memory expansion with 16-bit address and data buses with static latches with Reset and software-controlled $\overline{BG}$ pull-down
  - Bootstrap loading from external byte-wide Program ROM, Host Interface, or 16-bit Synchronous Serial Interface (SSI0)

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

- Peripherals
  - Up to twenty-five General Purpose Input / Output (GPIO) pins, depending on which peripherals are enabled
  - Byte-wide Host Interface with Direct Memory Access (DMA) support (or up to fifteen Port B GPIO lines)
  - On-chip ΣΔ voice band codec, Analog-to-Digital (A / D) and Digital-to-Analog (D / A)
    - Internal voltage reference (1 / 2 of positive power supply) and split-voltage operation (with respect to the core)
    - No off-chip components required
  - 16-bit SSI support: two 4-pin ports (or up to eight Port C GPIO lines)
  - One 16-bit timer / event counter (or two Port C GPIO lines)
  - Double-buffered peripherals
  - Independent external chip enables $\overline{BR}$ and $\overline{PEREN}$ during Bus Master mode
  - Software-programmable, Phase Lock Loop-based (PLL) frequency synthesizer for the DSP core clock with a wide input frequency range (12.2 KHz to 60 MHz) that initializes to a preset low frequency operation during hardware reset
- Energy Efficient Design
  - Power-saving Wait and Stop modes
  - Fully static, HCMOS design allows operation from 60 MHz down to DC operating frequencies
  - 112-pin plastic Thin Quad Flat Pack (TQFP) surface-mount package

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56167 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW) (the source for the latest information)

Table 1 DSP56167 Documentation

Name	Description	Order Number
DSP56100 Family Manual	Detailed description of the DSP56100 family processor core and instruction set	DSP56100FM / AD
DSP56167 User's Manual	Detailed functional description of the DSP56167 memory configuration, operation, and register programming	See note below
DSP56167 Technical Data	DSP56167 features list and physical, electrical, timing, and package specifications	DSP56167 / D

Note: The DSP56167 User's Manual is currently being developed and will not be available for general release until the end of the second quarter of 1997. The DSP56167 is a feature expanded, enhanced version of the DSP56166 and is entirely software compatible. Until the DSP56167 User's Manual is available, the user can refer to the *DSP56166 User's Manual,* order number DSP56166UM / AD for information common to both chips and **Section 4** of this document for a description of the added features and enhanced capability of the DSP56167.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

SECTION 1

SIGNAL/PIN DESCRIPTIONS

INTRODUCTION

DSP56167 signals are organized into thirteen functional groups as summarized in **Table 1-1**.

Table 1-1 Signal Functional Group Allocations

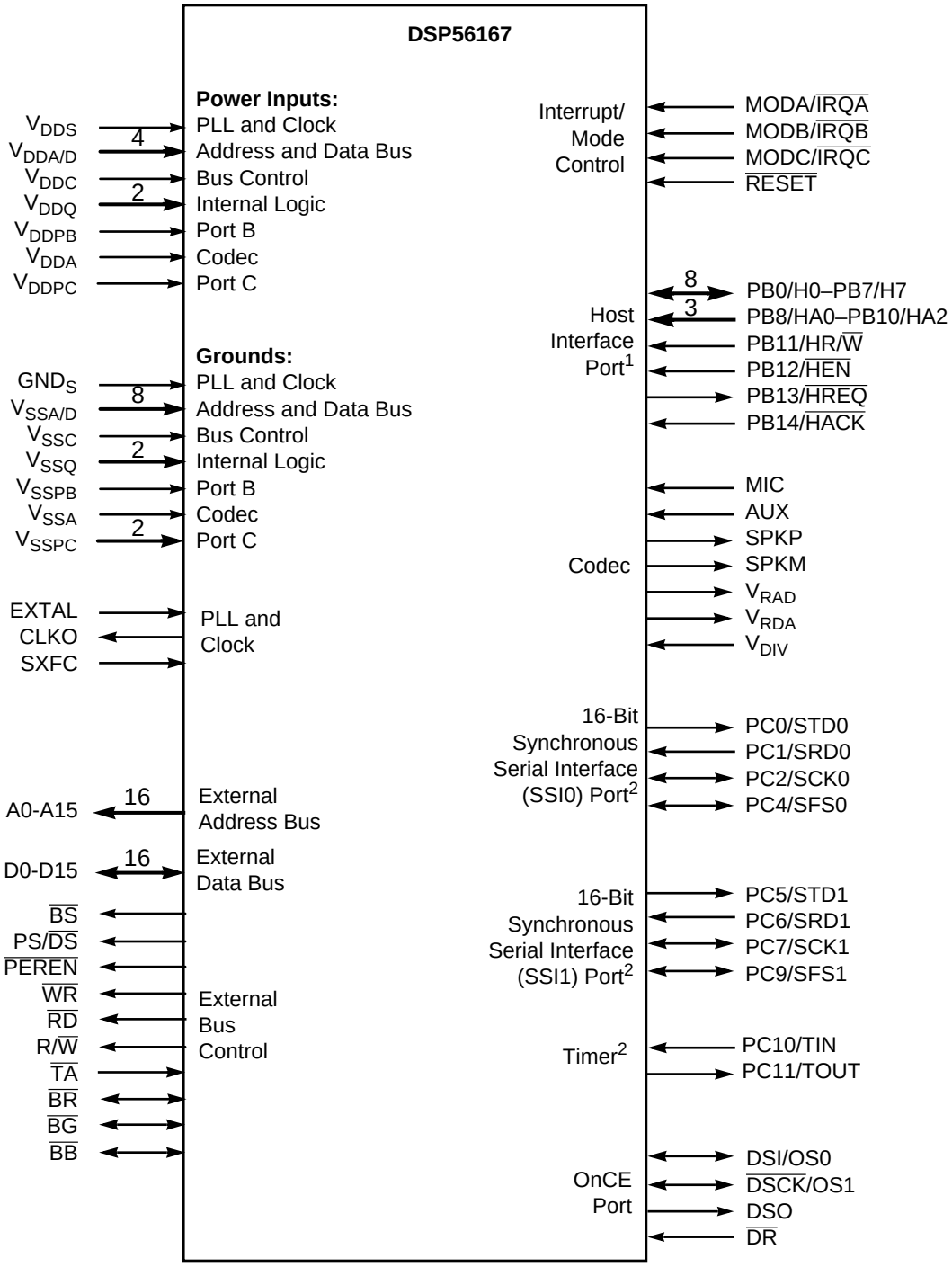
Functional Group		Number of Signals	Detailed Description
Power (V_{DDX})		11	**Table 1-2**
Ground (V_{SSX})		16	**Table 1-3**
PLL and Clock		3	**Table 1-4**
Address Bus	Port A[1]	16	**Table 1-5**
Data Bus		16	**Table 1-6**
Bus Control		10	**Table 1-7**
Interrupt and Mode Control		4	**Table 1-8**
Host Interface (HI) Port	Port B[2]	15	**Table 1-9**
Codec		7	**Table 1-10**
16-Bit Synchronous Serial Interface (SSI0) Port	Port C[3]	4	**Table 1-11**
16-Bit Synchronous Serial Interface (SSI1) Port		4	**Table 1-12**
Timer		2	**Table 1-13**
On-Chip Emulation (OnCE) Port		4	**Table 1-14**

Note:
1. Port A signals define the External Memory Interface port.
2. Port B signals are GPIO signals multiplexed on the external pins also used with the HI signals.
3. Port C signals are GPIO signals multiplexed on the external pins also used by the SSI ports and the Timer.

Figure 1-1 is a diagram of DSP56167 signals by functional group.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor



Note: 1. The HI port signals are multiplexed with the Port B GPIO signals (PB0–PB14).
2. The 16-bit SSI and Timer signals are multiplexed with the Port C GPIO signals (PC0–PC2, PC4–PC7, and PC9–PC11).

AA0772

Figure 1-1 Signals Identified by Functional Group

Downloaded from Elcodis.com electronic components distributor

POWER

Table 1-2 Power

Power Names	Description
V_{DDS}	**Synthesizer Power**—This line is dedicated to the PLL circuits and must remain noise-free to ensure stable PLL frequency and performance. Ensure that the input voltage to this line is well-regulated and uses an extremely low impedance path to tie to the V_{DD} power rail. Use a 0.1 µF capacitor and a 0.01 µF capacitor located as close as possible to the chip package to connect between the V_{DDS} line and the GND_S line.
$V_{DDA/D}$	**Address and Data Bus Power**—These lines supply power to the address and data busses.
V_{DDC}	**Bus Control Power**—This line supplies power to the bus control logic.
V_{DDQ}	**Quiet Power**—These lines supply a quiet power source to the internal logic circuits. Ensure that the input voltage to this line is well-regulated and uses an extremely low impedance path to tie to the V_{DD} power rail. Use a 0.1 µF bypass capacitor located as close as possible to the chip package to connect between the V_{DDQ} lines and the V_{SSQ} lines.
V_{DDPB}	**Port B Power**—These lines supply power to the Port B HI logic.
V_{DDA}	**Codec Power**—This line supplies power to the codec logic.
V_{DDPC}	**Port C Power**—This line supplies power to the SSI and Timer logic.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

GROUND

Table 1-3 Ground

Ground Names	Description
GND_S	**Synthesizer Ground**—This line supplies a dedicated quiet ground connection for the PLL and clock circuits and must remain relatively noise-free to ensure stable PLL frequency and performance. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 µF capacitor and a 0.01 µF capacitor located as close as possible to the chip package to connect between the V_{DDS} line and the GND_S line.
$V_{SSA/D}$	**Address and Data Bus Ground**—These lines connect system ground to the address bus.
V_{SSC}	**Bus Control Ground**—This line connects ground to the bus control logic.
V_{SSQ} (4)	**Quiet Ground**—These lines supply a quiet ground connection for the internal logic circuits. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 µF bypass capacitor located as close as possible to the chip package to connect between the V_{DDQ} line and the V_{SSQ} line.
V_{SSPB}	**Port B Host Interface Ground**—These lines supply ground connections for the Port B HI logic.
V_{SSA}	**Codec Power**—This line supplies a ground connection to the codec logic.
V_{SSPC}	**Port C Power**—This line supplies a ground connection to the SSI and Timer logic.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

PLL AND CLOCK

Table 1-4 PLL and Clock Signals

Signal Name	Signal Type	State during Reset	Signal Description
EXTAL	Input	Input	**External Clock/Crystal Input**—This input should be connected to an external crystal or to an external oscillator. A sine wave with a minimum swing of 1 V_P can be applied to this pin. After being squared, the input clock can provide the DSP core clock directly. Internally, the clock is divided to produce a four-phase instruction clock (T0, T1, T2, and T3) with the instruction clock period being equal to two input clock periods. This input clock can also be selected as the input clock for the on-chip codec and PLL.
CLKO	Output	Chip-driven	**PLL Output Clock**—This buffered clock signal output can be one of three signals, selected by programming the two bits, CS1 and CS2 in the PLL Control Register (PLCR): • A squared version of the EXTAL input • A squared version of the EXTAL input divided by 2 • A delayed version of the DSP core master clock CLKO can be disabled by setting the Clockout Disable (CD) Bit 7 of the Operating Mode Register (OMR). Note: For information about programming the PLCR or OMR, see the *DSP56100 Family Manual*.
SXFC	Input	Input	**External Filter Capacitor**—Connect an external capacitor to the filter circuit of the PLL between this input and V_{DDS}. See **Section 2** of this document for additional information about capacitor size selection.

ADDRESS BUS

Table 1-5 Address Bus Signals

Signal Names	Signal Type	State during Reset	Signal Description
A0–A15	Output	Tri-stated	**Address Bus—**These signals change in T0 and specify the address for external program and data memory accesses. If there is no external bus activity, A0–A15 remain at their previous values to reduce power consumption.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

DATA BUS

Table 1-6 Data Bus Signals

Signal Names	Signal Type	State during Reset	Signal Description
D0–D15	Input/ Output	Tri-stated	**Data Bus**—These signals provide the bidirectional data bus for external program and data memory accesses. Read data is sampled in by the trailing edge of T2, while write data output is enabled by the leading edge of T2 and tri-stated at the leading edge of T0. D0–D15 are tri-stated when there is no bus activity.

BUS CONTROL

Table 1-7 Bus Control Signals

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{BS}$	Output	Pulled high	**Bus Select—**$\overline{BS}$ is asserted when the DSP accesses the external bus, and it acts as an early indication of imminent external bus access by the DSP56167. It may also be used with the bus wait input $\overline{WT}$ to generate wait states. $\overline{BS}$ is pulled high when the $\overline{BG}$ or $\overline{RESET}$ signal is asserted.
PS/$\overline{DS}$	Output	Tri-stated	**Program/Data Memory Select—**This signal is asserted high for external program memory access and low for external data memory access. The timing is the same as for the Address Bus signals A0–A15. If the external bus is not used during an instruction cycle, PS/$\overline{DS}$ goes high at the next T0.
$\overline{PEREN}$	Output	Tri-stated	**Peripheral Enable**—This output is asserted only when the external peripheral data memory space (X:$FF00–X:$FF7F) is referenced. The timing is the same as for the Address Bus signals A0–A15. The signal is asserted and deasserted in T0. $\overline{PEREN}$ is driven high for any program space access and for any data memory access outside of the peripheral data memory address range.
$\overline{WR}$	Output	Tri-stated	**Write Enable—**$\overline{WR}$ is asserted low during external memory write cycles. When $\overline{WR}$ is asserted in T1, the data bus signals (D0–D15) become outputs. The DSP puts data on the bus on the leading edge of T2. When $\overline{WR}$ is deasserted in T3, the data should be latched in the external device. The signal qualifies A0–A15 and PS/$\overline{DS}$. $\overline{WR}$ is tri-stated when the DSP is not the bus master. $\overline{WR}$ can be connected directly to the $\overline{WE}$ pin of a Static RAM chip.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 1-7 Bus Control Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{RD}$	Output	Tri-stated	**Read Enable—**$\overline{RD}$ is asserted low during external memory read cycles. When $\overline{RD}$ is asserted in late T0/early T1, the data bus signals (D0–D15) become inputs and an external device is enabled on the data bus. When $\overline{RD}$ is deasserted in T3, the data is latched in the DSP. The signal qualifies A0–A15 and PS/$\overline{DS}$. $\overline{RD}$ is tri-stated when the DSP is not the bus master. $\overline{RD}$ can be connected directly to the $\overline{OE}$ pin of a ROM or Static RAM.
R/$\overline{W}$	Output	Tri-stated	**Read/Write**—The timing for this signal is the same as the bus address lines, providing an early write signal. R/$\overline{W}$ changes in T0 and is high for a read access and low for a write access. If the external bus is not used during an instruction cycle, R/$\overline{W}$ goes high at the next T0.
$\overline{TA}$	Input	Input	**Transfer Acknowledge—**When there is external bus cycle activity, $\overline{TA}$ can be used to insert Wait States (WS) in the external bus cycle. $\overline{TA}$ is sampled on the leading edge of the clock input. If $\overline{TA}$ is sampled high, the bus cycle will end 2T after TA is sampled low, assuming the Bus Control Register (BCR) is not programmed to insert its own WS. The number of WS is determined by $\overline{TA}$ and the BCR and is equal to the larger of the two determining sources. $\overline{TA}$ continues to be sampled as the BCR WS number decrements. If $\overline{TA}$ is sampled low, but there are remaining WS required by the BCR, the bus cycle continues until the BCR requirement is satisfied. If the BCR requirement is satisfied, but $\overline{TA}$ has not been sampled low, the WS continue until 2T after $\overline{TA}$ is sampled low. To be sampled high at the start of the bus cycle, $\overline{TA}$ must be driven high in T3 on the previous instruction cycle. If TA is sampled low at T0 of a bus cycle and no WS are specified by the BCR, no WS are inserted in the external bus cycle. If there is no external bus activity, the DSP ignores $\overline{TA}$.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 1-7 Bus Control Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{BR}$	Input or Output	Input	**Bus Request—**After reset, this signal is an input (Slave mode). When the $\overline{BR}$ input is asserted, an external device, such as another processor or DMA controller, becomes the master of the external address and data buses. The DSP asserts the $\overline{BG}$ output signal after a few T states (i.e., T0, T1, etc.) to acknowledge the $\overline{BR}$ input. The DSP releases control of the external bus at the earliest possible time consistent with proper synchronization. At release, the DSP tri-states $\overline{PEREN}$, PS/$\overline{DS}$, $\overline{RD}$, $\overline{WR}$, and R/$\overline{W}$, and deasserts the $\overline{BB}$ signal to indicate the bus is released. While the bus is released, the DSP may continue internal operations using internal memory spaces. If external access is required, the DSP bus controller inserts WS until the bus is available. Bus control returns to the DSP when the $\overline{BR}$ and $\overline{BB}$ inputs are both deasserted. Note: Interrupts are not serviced while a DSP instruction is waiting for the bus. Note: $\overline{BR}$ cannot interrupt the execution of a read-modify-write instruction. If the master bit in the Operating Mode Register (OMR) is set, this signal is an output (Master mode). In this mode the DSP is not the default bus master and must assert $\overline{BR}$ to gain control of the external bus. After asserting $\overline{BR}$, the DSP bus controller inserts WS until the $\overline{BG}$ input is asserted. The DSP begins processing external accesses on the rising edge of the clock after $\overline{BB}$ is sampled high. $\overline{BR}$ remains asserted until the DSP no longer needs the bus. In Master mode, the Request Hold (RH) bit in the BCR allows $\overline{BR}$ to be asserted under software control. Note: During external accesses caused by an instruction executed out of external program memory, $\overline{BR}$ remains asserted for consecutive external X data memory accesses and continues toggling for consecutive external program memory accesses until RH in the BCR is set. Note: In Master mode, $\overline{BR}$ can also be used for non-arbitration uses. If $\overline{BG}$ is always asserted, $\overline{BR}$ is asserted in T0 of every external bus access. In this case, $\overline{BR}$ can act as a chip select signal to enable and disable an external memory device between external and internal accesses. In this case, the $\overline{BR}$ timing is similar to A0–A15, R/$\overline{W}$, and PS/$\overline{DS}$ and is asserted and deasserted in T0.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 1-7 Bus Control Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{BG}$	Output or Input	Driven high	**Bus Grant—**After reset, this signal is an output (Slave mode) that is asserted to acknowledge an external device request for bus control (i.e., assertion of a $\overline{BR}$ input). The DSP asserts the $\overline{BG}$ output signal after a few T states to acknowledge receipt of the $\overline{BR}$ input. The DSP releases control of the external bus at the earliest possible time consistent with proper synchronization. At release, the DSP tri-states $\overline{PEREN}$, PS / $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, and R / $\overline{W}$ and deasserts the $\overline{BB}$ output. When the $\overline{BR}$ and $\overline{BB}$ inputs are deasserted, the DSP regains control of the bus and the $\overline{BG}$ output is deasserted. Note: $\overline{BG}$ may be asserted in the middle of an instruction that requires more than one external bus cycle for execution, but never during a read-modify-write instruction. If the master bit in the OMR is set, this signal is an input (Master mode). In this mode the external bus master asserts $\overline{BG}$ to acknowledge the $\overline{BR}$ signal generated by the DSP to request control of the bus. The DSP begins processing external accesses on the rising edge of the clock after the $\overline{BB}$ input generated by the other bus master is sampled high. When the $\overline{BG}$ input is deasserted, the DSP releases the bus as soon as the current transfer is complete.
$\overline{BB}$	Input or Output	Input	**Bus Busy—**After reset, this signal is an input. An external master asserts this input signal to indicate that it has control of the bus and is performing a bus access. When the DSP acquires control of the external bus and performs and external access, it asserts $\overline{BB}$ as an output signal to the other bus master devices. The DSP deasserts $\overline{BB}$ and it again becomes an input when the DSP releases bus control.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

INTERRUPT AND MODE CONTROL

Table 1-8 Interrupt and Mode Control Signals

Signal Name	Signal Type	State during Reset	Signal Description
MODA / $\overline{\text{IRQA}}$	Input	Input	**Mode Select A/External Interrupt Request A** — This input has two functions: 1. to select the initial chip operating mode, and 2. after synchronization, to allow an external device to request a DSP interrupt. MODA is read and internally latched in the DSP when the processor exits the Reset state. MODA, MODB, and MODC select the initial chip operating mode. Several clock cycles (depending on PLL stabilization time) after leaving the Reset state, the MODA signal changes to external interrupt request $\overline{\text{IRQA}}$. The chip operating mode can be changed by software after reset. The $\overline{\text{IRQA}}$ input is a synchronized external interrupt request that indicates that an external device is requesting service. It may be programmed to be level-sensitive or negative-edge-sensitive. If level-sensitive triggering is selected, an external pull up resistor is required for wired-OR operation. If the processor is in the Stop state and $\overline{\text{IRQA}}$ is asserted, the processor will exit the Stop state.
MODB / $\overline{\text{IRQB}}$	Input	Input	**Mode Select B/External Interrupt Request B** — This input has two functions: 1. to select the initial chip operating mode, and 2. after internal synchronization, to allow an external device to request a DSP interrupt. MODB is read and internally latched in the DSP when the processor exits the Reset state. MODA, MODB, and MODC select the initial chip operating mode. Several clock cycles (depending on PLL stabilization time) after leaving the Reset state, the MODB signal changes to external interrupt request $\overline{\text{IRQB}}$. After reset, the chip operating mode can be changed by software. The $\overline{\text{IRQB}}$ input is an external interrupt request that indicates that an external device is requesting service. It may be programmed to be level-sensitive or negative-edge-triggered. If level sensitive triggering is selected, an external pull up resistor is required for wired-OR operation.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 1-8 Interrupt and Mode Control Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
MODC/$\overline{\text{IRQC}}$	Input	Input	**Mode Select C/External Interrupt Request C**— This input has two functions: 1. to select the initial chip operating mode, and 2. after synchronization, to allow an external device to request a DSP interrupt. MODC is read and internally latched in the DSP when the processor exits the Reset state. MODA, MODB, and MODC select the initial chip operating mode. Several clock cycles (depending on PLL stabilization time) after leaving the Reset state, the MODC signal changes to external interrupt request $\overline{\text{IRQC}}$. After reset, the chip operating mode can be changed by software. The $\overline{\text{IRQC}}$ input is an external interrupt request that indicates that an external device is requesting service. It may be programmed to be level-sensitive or negative-edge-triggered. If level sensitive triggering is selected, an external pull up resistor is required for wired-OR operation.
$\overline{\text{RESET}}$	Input	Input	**Reset** — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the DSP is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, and MODC signals. The internal reset signal is deasserted synchronous with the internal clocks.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

HOST INTERFACE (HI) PORT

Table 1-9 HI Signals

Signal Name	Signal Type	State during Reset	Signal Description
H0–H7	Input/ Output	Tri-stated	**Host Data Bus (H0–H7)**—This data bus transfers data between the host processor and the DSP56167. The bus signals are inputs except when HR/$\overline{W}$ is high and $\overline{HEN}$ is asserted (host read).
PB0–PB7			**Port B GPIO 0–7 (PB0–PB7)**—These signals are GPIO signals (PB0–PB7) when the Host Interface is not selected. After reset, the default state for these signals is GPIO input.
HA0–HA2	Input	Tri-stated	**Host Address 0 – Host Address 2 (HA0–HA2)**—These inputs provide the address selection for each Host Interface register and are stable when $\overline{HEN}$ is asserted.
PB8–PB10	Input/ Output		**Port B GPIO 8–10 (PB8–PB10)**—These signals are GPIO signals (PB8–PB10) when the Host Interface is not selected. After reset, the default state for these signals is GPIO input.
HR/$\overline{W}$	Input	Tri-stated	**Host Read/Write**—This input selects the direction of data transfer for each host processor access. If HR/$\overline{W}$ is high and $\overline{HEN}$ is asserted, H0–H7 are outputs and DSP data is transferred to the host processor. If HR/$\overline{W}$ is low and $\overline{HEN}$ is asserted, H0–H7 are inputs and host data is transferred to the DSP. HR/$\overline{W}$ is stable when $\overline{HEN}$ is asserted.
PB11	Input/ Output		**Port B GPIO 11 (PB11)**—This signal is a GPIO signal (PB11) when the Host Interface is not being used. After reset, the default state for this signal is GPIO input.
$\overline{HEN}$	Input	Tri-stated	**Host Enable—**This input enables a data transfer on the host data bus. When $\overline{HEN}$ is asserted and HR/$\overline{W}$ is high, H0–H7 are outputs and DSP data is transferred to the host processor. If HR/$\overline{W}$ is low and $\overline{HEN}$ is asserted, H0–H7 are inputs and host data is transferred to the DSP. This input may be used as a chip select input from the external host.
PB12	Input/ Output		**Port B GPIO 12 (PB12)**—This signal is a GPIO signal (PB12) when the Host Interface is not being used. After reset, the default state for this signal is GPIO input.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 1-9 HI Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{\text{HREQ}}$	Open drain Output	Tri-stated	**Host Request—** This signal is used by the Host Interface to request service from the host processor, DMA controller, or a simple external controller. HREQ is asserted when an enabled request occurs in the HI. The signal is deasserted when the request is cleared or masked, the DMA controller asserts $\overline{\text{HACK}}$, or the DSP is reset.
PB13	Input/ Output		**Port B GPIO 13 (PB13)**—This signal is a General Purpose (not open-drain) I/O signal (PB13) when the Host Interface is not selected. After reset, the default state for this signal is GPIO input.
$\overline{\text{HACK}}$	Input	Tri-stated	**Host Acknowledge—** This input has two functions: 1. **Host Acknowledge handshake signal—**$\overline{\text{HACK}}$ may be used as a data strobe for HI DMA data transfers 2. **MC68000 Host Interrupt Acknowledge—**This function enables the HI Interrupt Vector Register (IVR) onto the HI data bus if the $\overline{\text{HREQ}}$ output is asserted. In this case, all other HI control pins are ignored and the HI state is not affected.
PB14	Input/ Output		**Port B GPIO 14 (PB14)**—This signal is a GPIO signal (PB14) when the Host Interface is not selected. After reset, the default state for this signal is GPIO input.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

CODEC

Table 1-10 Codec Signals

Signal Name	Signal Type	State during Reset	Signal Description
AUX	Input	Input	**Auxiliary Input**—This signal is selected as the analog input to the A/D converter when the INS bit in Codec Control Register 1 (CCR1) is set. Leave this pin floating when the codec is not used.
MIC	Input	Input	**Microphone Input—**This signal is selected as the analog input to the A/D converter when the INS bit in CCR1 is cleared. Leave this pin floating when the codec is not used.
SPKP	Output		**Speaker Output 1—**This signal is the negative analog output from the on-chip D/A converter. Leave this pin floating when the codec is not used. In the codec Power Down mode, this signal connects internally to VDIV through a high impedance path.
SPKM	Output		**Speaker Output 2—**This signal is the positive analog output from the on-chip D/A converter. Leave this pin floating when the codec is not used. In the codec Power Down mode, this signal connects internally to VDIV through a high impedance path.
VRAD	Output		**Voltage Reference Output for A/D—** This is the output from the op-amp buffer in the A/D sections reference voltage generator. It has a value of 1/2 V_{DDA}. This voltage is used as the analog ground internal to the A/D block. Always connect this pin to ground through two capacitors even when the codec is not used. In codec Power Down mode, the VRAD signal is tri-stated.
VRDA	Output		**Voltage Reference Output for D/A—** This is the output from the op-amp buffer in the D/A sections reference voltage generator. It has a value of 1/2 V_{DDA}. This voltage is used as the analog ground internal to the D/A block. Always connect this pin to ground through two capacitors even when the codec is not used. In codec Power Down mode, the VRDA signal is tri-stated.
VDIV	Output		**Voltage Division Output—**This is the input to the op-amp buffer in the reference voltage generator. It is connected to a resistor divider network located within the codec block that provides a voltage equal to 1/2 V_{DDA}. Leave this pin floating when the codec is not used. This output is not affected by codec Power Down mode.
Note: The SPKP and SPKM outputs consist of a fully differential driver stage, with each output having an operating range of ±1.0 V_P from VRDA. The output op-amp can provide up to ±0.35 mA of current which can drive a resistive load of 3 kΩ in series with 15 nF capacitance between the differential outputs.			

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

16-BIT SYNCHRONOUS SERIAL INTERFACE 0 PORT

Table 1-11 16-Bit Synchronous Serial Interface 0 (SSI0) Signals

Signal Name	Signal Type	State during Reset	Signal Description
STD0 PC0	Output	Tri-stated	**Serial Transmit Data 0 (STD0)—**This output transmits serial data from the SSI0 Transmit Shift Register (TSR0). **Port C GPIO 0 (PC0)**— This signal is a GPIO signal (PC0) when the SSI0 STD0 function is not being used. After reset, the default state is GPIO input.
SRD0 PC1	Input	Tri-stated	**Serial Receive Data 0 (SRD0)—**The input receives serial data into the SSI0 Receive Shift Register (RSR0). **Port C GPIO 1 (PC1)**— This signal is a GPIO signal (PC1) when the SSI0 SRD0 function is not being used. After reset, the default state is GPIO input.
SCK0 PC2	Input/ Output	Tri-stated	**Serial Clock 0 (SCK0)—**This bidirectional signal provides the serial bit rate clock for the SSI0 interface. The clock signal can be continuous or gated and is used by both the transmitter and receiver. **Port C GPIO 5 (PC5)**— This signal is a GPIO signal (PC2) when the SSI0 SCK0 function is not being used. After reset, the default state is GPIO input.
SFS0 PC4	Input/ Output	Tri-stated	**Serial Frame Sync 0**— This bidirectional signal is used by the SSI0 serial interface for frame sync I/O or flag I/O. The SFS0 is used by both the transmitter and receiver to synchronize data transfer and can be an input or an output. **Port C GPIO 4 (PC4)**— This signal is a GPIO signal (PC4) when the SSI0 SFS0 function is not being used. After reset, the default state is GPIO input.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

16-BIT SYNCHRONOUS SERIAL INTERFACE 1 PORT

Table 1-12 16-Bit Synchronous Serial Interface 1 (SSI1) Signals

Signal Name	Signal Type	State during Reset	Signal Description
STD1 PC5	Output	Tri-stated	**Serial Transmit Data 1 (STD1)—**This output transmits serial data from the SSI1 Transmit Shift Register (TSR1). **Port C GPIO 5 (PC5)**— This signal is a GPIO signal (PC5) when the SSI1 STD1 function is not being used. After reset, the default state is GPIO input.
SRD1 PC6	Input	Tri-stated	**Serial Receive Data 0 (SRD0)—**The input receives serial data into the SSI1 Receive Shift Register (RSR1). **Port C GPIO 6 (PC6)**— This signal is a GPIO signal (PC6) when the SSI1 SRD1 function is not being used. After reset, the default state is GPIO input.
SCK1 PC7	Input/ Output	Tri-stated	**Serial Clock 1 (SCK1)—**This bidirectional signal provides the serial bit rate clock for the SSI1 interface. The clock signal can be continuous or gated and is used by both the transmitter and receiver. **Port C GPIO 7 (PC7)**— This signal is a GPIO signal (PC7) when the SSI1 SCK1 function is not being used. After reset, the default state is GPIO input.
SFS0 PC9	Input/ Output	Tri-stated	**Serial Frame Sync 1**— This bidirectional signal is used by the SSI1 serial interface for frame sync I/O or flag I/O. The SFS1 is used by both the transmitter and receiver to synchronize data transfer and can be an input or an output. **Port C GPIO 9 (PC9)**— This signal is a GPIO signal (PC9) when the SSI1 SFS1 function is not being used. After reset, the default state is GPIO input.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

TIMER

Table 1-13 Timer Signals

Signal Name	Signal Type	State during Reset	Signal Description
TIN PC10	Input	Tri-stated	**Timer Input —**This input signal receives external pulses to be counted by the on-chip 16-bit timer when external clocking is selected. The pulses are internally synchronized to the DSP core internal clock. **Port C GPIO 10 (PC10)—** This signal is a GPIO signal (PC10) when the Timer function is not being used.
TIO1 PC11	Input/ Output	Tri-stated	**Timer Output—**This output generates pulses, toggles on a timer overflow event, or toggles on a compare event. **Port C GPIO 11 (PC11)—**This signal is a GPIO signal (PC11) when the Timer function is not being used.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

On-CHIP EMULATION PORT

Table 1-14 On-Chip Emulation (OnCE) Port Signals

Signal Name	Signal Type	State during Reset	Signal Description
DSI/OS0	Input/ Output	Low Output	**Debug Serial Input/Chip Status 0—**Serial data or commands are provided to the OnCE controller through the DSI/OS0 signal when it is an input. The data received on the DSI signal will be recognized only when the DSP has entered the Debug mode of operation. Data is latched on the falling edge of the DSCK serial clock. Data is always shifted into the OnCE serial port Most Significant Bit (MSB) first. When the DSI/OS0 signal is an output, it works in conjunction with the OS1 signal to provide chip status information. The DSI/OS0 signal is an output when the processor is not in Debug mode. When switching from output to input, the signal is tri-stated.
DSCK/OS1	Input/ Output	Low Output	**Debug Serial Clock/Chip Status 1—**The DSCK/OS1 signal supplies the serial clock to the OnCE port when it is an input. The serial clock provides pulses required to shift data into and out of the OnCE serial port. (Data is clocked into the OnCE port on the falling edge and is clocked out of the OnCE serial port on the rising edge.) The debug serial clock frequency must be no greater than $^{1}/_{8}$ of the processor clock frequency. When switching from input to output, the signal is tri-stated. When it is an output, this signal works with the OS0 signal to provide information about the chip status. The DSCK/OS1 signal is an output when the chip is not in Debug mode.
DSO	Output	Pulled high	**Debug Serial Output—**Data contained in one of the OnCE port controller registers is provided through the DSO output signal, as specified by the last command received from the external command controller. Data is always shifted out the OnCE serial port MSB first. Data is clocked out of the OnCE serial port on the rising edge of DSCK. The DSO signal also provides acknowledge pulses to the external command controller. When the chip enters the Debug mode, the DSO signal will be pulsed low to indicate (acknowledge) that the OnCE is waiting for commands. After the OnCE receives a read command, the DSO signal will be pulsed low to indicate that the requested data is available and the OnCE serial port is ready to receive clocks in order to deliver the data. After the OnCE receives a write command, the DSO signal will be pulsed low to indicate that the OnCE serial port is ready to receive the data to be written; after the data is written, another acknowledge pulse will be provided.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 1-14 On-Chip Emulation (OnCE) Port Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{DR}$	Input	Input	**Debug Request—**The debug request input ($\overline{DR}$) allows the user to enter the Debug mode of operation from the external command controller. When $\overline{DR}$ is asserted, it causes the DSP to finish the current instruction being executed, save the instruction pipeline information, enter the Debug mode, and wait for commands to be entered from the DSI line. While in Debug mode, the $\overline{DR}$ signal lets the user reset the OnCE controller by asserting it and deasserting it after receiving acknowledge. It may be necessary to reset the OnCE controller in cases where synchronization between the OnCE controller and external circuitry is lost. $\overline{DR}$ must be deasserted after the OnCE port responds with an acknowledge on the DSO signal and before sending the first OnCE command. Asserting $\overline{DR}$ will cause the chip to exit the Stop or Wait state. Having $\overline{DR}$ asserted during the deassertion of $\overline{RESET}$ will cause the DSP to enter Debug mode.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

SECTION 2

SPECIFICATIONS

GENERAL CHARACTERISTICS

The DSP56167 is fabricated in high-density HCMOS with TTL compatible inputs and outputs.

Table 2-1 Absolute Maximum Ratings (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to +7.0	V
All Input Voltages	V_{IN}	(V_{SS} – 0.5) to (V_{DD} + 0.5)	V
Current Drain per Pin excluding V_{DD} and V_{SS}	I	10	mA
Storage Temperature	T_{stg}	–55 to +150	°C

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 2-2 Recommended Operating Conditions

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	4.5 to 5.5	V
Operating Temperature Range	T_J	–40 to 105	°C

Table 2-3 Thermal Characteristics for 112-pin TQFP Package

Thermal Resistance	Symbol	Value	Rating
Junction-to-Ambient	$R_{\theta JA}$	38.4	°C / W
Junction-to-Case (estimated)	$R_{\theta JC}$	5.5	°C / W
Thermal characterization parameter	Ψ_{JT}	2.3	°C / W

Note:
1. See discussion under **Design Considerations, Heat Dissipation, page 4-1**.
2. Junction-to-ambient thermal resistance is based on measurements on a horizontal, single-sided, printed circuit board per SEMI G38-87 in natural convection. SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Road, Mountain View, CA 94043, (415) 964-5111.
3. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88 with the exception that the cold plate temperature is used for the case temperature.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

DC ELECTRICAL CHARACTERISTICS

Table 2-4 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Input High Voltage • EXTAL – DC coupled – AC coupled • $\overline{\text{RESET}}$ • MODA, MODB, MODC • All other inputs	V_{IHC} V_{IHR} V_{IHM} V_{IH}	 $0.7 \times V_{DD}$ 1.0 2.5 3.5 2.0	 — — — — —	 V_{DD} V_{DD} V_{DD} V_{DD} V_{DD}	 V V V V V
Input Low Voltage • EXTAL – DC coupled – AC coupled • MODA, MODB, MODC • All other inputs	 V_{ILC} V_{ILC} V_{ILM} V_{IL}	 –0.5 –0.5 –0.5 –0.5	 — — — —	 $0.2 \times V_{DD}$ $V_{DD} - 1$ 2.0 0.8	 V V V
Input Leakage Current EXTAL, $\overline{\text{RESET}}$, MODA / $\overline{\text{IRQA}}$, MODB / $\overline{\text{IRQB}}$, MODC / $\overline{\text{IRQC}}$, $\overline{\text{BR}}$	I_{IN}	–1	—	1	µA
Tri-state (Off–state) Input Current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output High Voltage (I_{OH} = –10 µA)	V_{OHC}	$V_{DD} - 0.1$	—	—	V
Output High Voltage (I_{OH} = –0.4 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OH} = 10 µA)	V_{OLC}	—	—	0.1	V
Output Low Voltage (I_{OL} = 3.2 mA) R / $\overline{\text{W}}$ I_{OL} = 1.6 mA, open-drain $\overline{\text{HREQ}}$ I_{OL} = 6.7 mA, TXD I_{OL} = 6.7 mA	V_{OL}	—	—	0.4	V
Internal Supply Current[1] • Normal mode with codec and PLL disabled • Wait mode with codec and PLL disabled • Stop mode with PLL and CLKO disabled	 I_{CCI} I_{CCW} I_{CCS}	 — — —	 100 11 400	 	 mA mA µA
PLL current when active	I_{CCPLL}	—	2		mA
Analog Current • Codec enabled • Codec disabled	I_{CCA}	 — —	 10 75	 	 mA µA
Input Capacitance	C_{IN}	—	10	—	pF

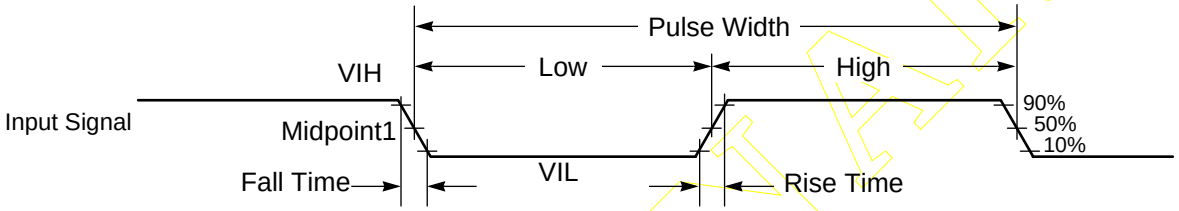
Note: 1. **Section 4 Design Considerations** describes how to calculate the external supply current.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, $\overline{\text{RESET}}$, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56167 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

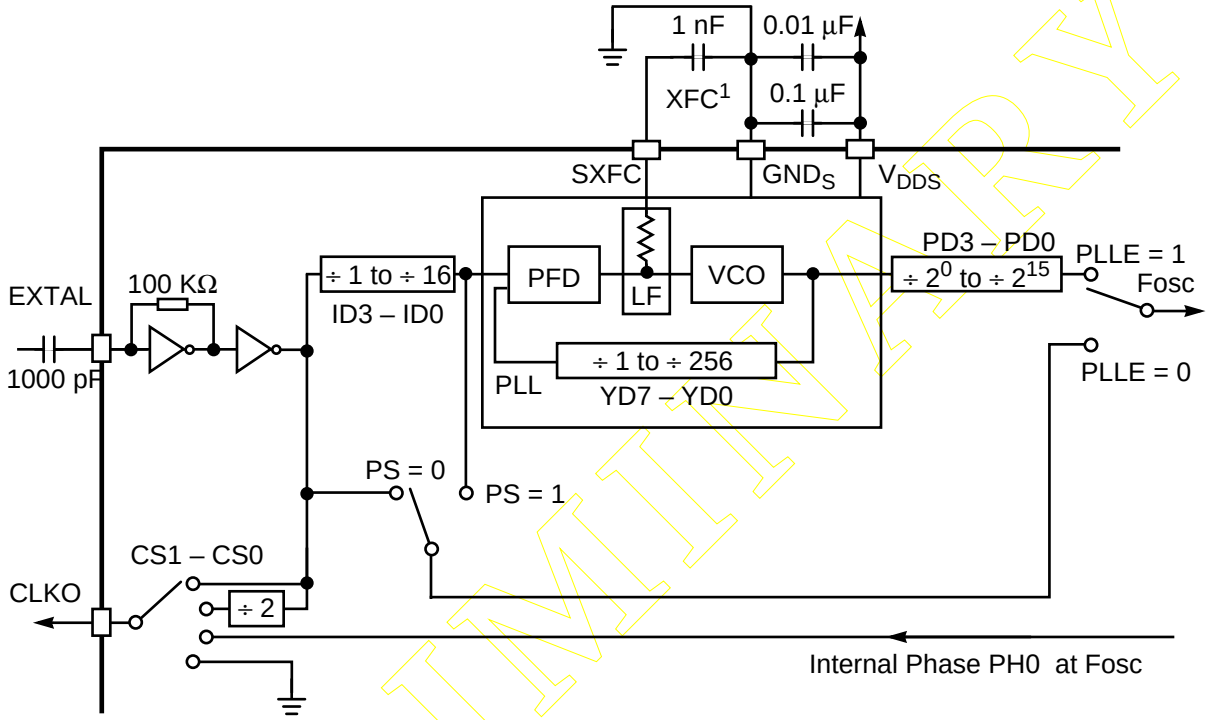
Figure 2-1 Signal Measurement Reference

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

CLOCK OPERATION

The system clock must be externally supplied by connecting a square wave voltage source to EXTAL. **Figure 2-2** shows the recommended connection of the external source to EXTAL and the external filter capacitor to SFXC.



Note: 1. Must be a low leakage capacitor and must be located very close to the SXFC and VDDS pins.

AA0773

Figure 2-2 Connecting EXTAL and the External Filter Capacitor

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 2-5 Clock Operation

Num	Characteristics	Symbol	60 MHz		Unit
			Min	Max	
1	Frequency of Operation (EXTAL input)	E_f	0	60	MHz
2	Instruction Cycle Time = $2 \times T_C$	I_{CYC}	33	∞	ns
3	Wait State = T_C = 2 T	WS	16.6	∞	ns
4	EXTAL cycle period	T_C	16.6	∞	ns
5	EXTAL rise time[1]		—	3	ns
6	EXTAL fall time[1]		—	3	ns
7	EXTAL width high[2,3,4] (48–52% duty cycle)	T_H	8	∞	ns
8	EXTAL width low[2,3,4] (48–52% duty cycle)	T_L	8	∞	ns

Note:
1. Rise and fall time may be relaxed to 12 ns maximum if the EXTAL input frequency is ≤ 20 MHz. If E_f is between 20 MHz and 40 MHz, rise and fall time should be 4 ns maximum. If E_f is between 40 MHz and 60 MHz, rise and fall time should meet the specified value (3 ns maximum).
2. The duty cycle may be relaxed to 43–57% if the EXTAL input frequency is ≤ 20 MHz. If the EXTAL input frequency is between 20MHz and 40MHz, the duty cycle should be such that T_H and T_L are 12 ns minimum. If the EXTAL input frequency is between 40 MHz and 60 MHz, the duty cycle should be such that T_H and T_L meet the specified values in the 60 MHz column (8 ns minimum).
3. $T = I_{CYC}/4$ is used in the electrical characteristics. The exact length of each T is affected by the duty cycle of the external clock input.
4. Duty cycles and EXTAL widths are measured at the EXTAL input signal midpoint when AC coupled and at $V_{DD}/2$ when DC coupled.

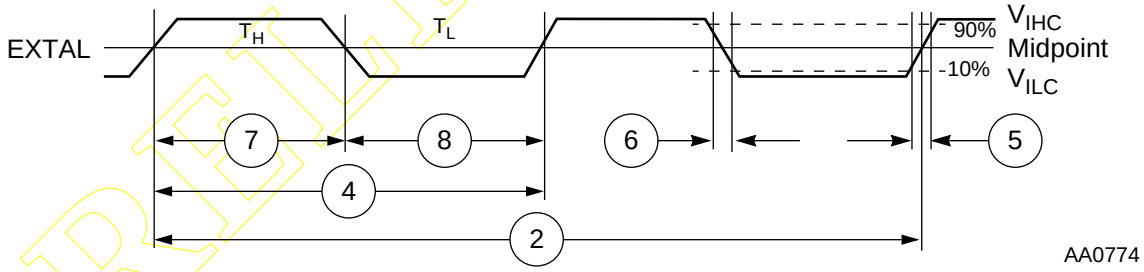


Figure 2-3 External Clock Timing

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

PHASE LOCK LOOP (PLL) AND OTHER CLOCK TIMING

Table 2-6 PLL and Other Clock Characteristics

Characteristics	Min	Max	Unit
PLL output frequency	10	Maximum f [1]	MHz
EXTAL input clock amplitude	1	V_{DD}	V_P

Note: 1. Maximum DSP operating frequency
2. An AC coupling capacitor is required on EXTAL if the levels are out of the normal CMOS level range ($V_{ILC} > 0.2 \times V_{DD}$ or $V_{IHC} < 0.7 \times V_{DD}$).

RESET, STOP, MODE SELECT, AND INTERRUPT TIMING

V_{DD} = 5.0 V ± 10%; T_J = –40 to +115°C; C_L = 50 pF + 2 TTL loads
WS = number of wait states programmed into the external bus access using BCR (WS = 0–15)

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing (60 MHz)

Num	Characteristics	Min	Max	Unit
10	$\overline{\text{RESET}}$ Assertion to Address, Data and control signals High Impedance	—	21.0	ns
11	Minimum Stabilization Duration[1] OMR Bit 6 = 0 OMR Bit 6 = 1	 600KT 60T	 — —	 ns ns
12	Asynchronous $\overline{\text{RESET}}$ Deassertion to First External Address Output[7]	16T	18T + 15	ns
13	Synchronous Reset Setup Time from $\overline{\text{RESET}}$ Deassertion to Rising Edge of CLKO	5	cyc – 2	ns
14	Synchronous Reset Delay Time from CLKO High to the First External Access[7]	16T + 3	16T + 16	ns
15	Mode Select Setup Time	4.8	—	ns
16	Mode Select Hold Time	4.0	—	ns
17	Edge-Triggered Interrupt Request Width	8.0	—	ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$ Assertion to External Data Memory Access Out Valid — Caused by First Interrupt Instruction Fetch — Caused by First Interrupt Instruction Execution	 11T + 3 19T + 3	 — —	 ns ns
19	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$ Assertion to General Purpose Output Valid Caused by the Execution of the First Interrupt Instruction	22T + 3	—	ns

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing (60 MHz) (Continued)

Num	Characteristics	Min	Max	Unit
20	Delay from External Data Memory Address Output Valid Caused by First Interrupt Instruction Execution to Interrupt Request Deassertion for Level Sensitive Fast Interrupts[2]	—	5T – 22 + cyc × WS	ns
21	Delay from General-Purpose Output Valid Caused by the Execution of the First Interrupt Instruction to $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$ Deassertion for Level Sensitive Fast Interrupts—If 2nd Interrupt Instruction is: Single Cycle[2] Two Cycles	 — —	 cyc – 26 3cyc – 26	 ns ns
22	Synchronous setup time from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$ assertion to Synchronous falling edge of CLKO[5,6]	12	—	ns
23	Falling Edge of CLKO to First Interrupt Vector Address Out Valid after Synchronous recovery from Wait State[3,5]	27T + 3	27T + 16	ns
24	$\overline{\text{IRQA}}$ Width Assertion to Recover from STOP State[4]	17	—	ns
25	Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of first instruction (exiting STOP)[1,3] OMR Bit 6 = 0 OMR Bit 6 = 1	 524303T + 3 47T + 3	 — —	 ns ns
28	Duration for Level Sensitive $\overline{\text{IRQA}}$ Assertion to Cause the Fetch of First $\overline{\text{IRQA}}$ Interrupt Instruction (exiting STOP)[1,3] OMR Bit 6 = 0 OMR Bit 6 = 1	 524303T 47T	 — —	 ns ns
29	Delay from Level Sensitive $\overline{\text{IRQA}}$ Assertion to First Interrupt Vector Address Out Valid (exiting STOP)[1,3] OMR bit 6 = 0 OMR bit 6 = 1	 524303T + 3 47T + 3	 — —	 ns ns
30	$\overline{\text{DR}}$ Asserted to CLK low (Setup Time for Synchronous Recovery from Wait State)	8	cyc+8	ns
31	CLK low to DSO ($\overline{\text{ACK}}$) Valid (Enter Debug Mode) After Synchronous Recovery from Wait State	18cyc	—	ns
32	$\overline{\text{DR}}$ to DSO ($\overline{\text{ACK}}$) Valid (Enter Debug Mode) After Asynchronous Recovery from Stop Mode After Asynchronous Recovery from Wait Mode	 29cyc 18cyc	 — —	 ns ns
33	$\overline{\text{DR}}$ Assertion Width Recovery from Wait / Stop without entering Debug Short wakeup from Wait / Stop and enter Debug Long wakeup from Stop enter Debug	 10 29cyc 262157cyc	 10cyc — —	 ns ns ns

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing (60 MHz) (Continued)

Num	Characteristics	Min	Max	Unit

Note:
1. Circuit stabilization delay is required during reset when using an external clock in two cases:
   • after power-on reset, and
   • when recovering from Stop mode.
2. When using fast interrupts and $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ are defined as level-sensitive, then timings 20 and 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the Deasserted Edge-Triggered mode is recommended when using fast interrupt. Long interrupts are recommended when using Level-Sensitive mode.
3. The interrupt instruction fetch is visible on the pins only in Mode 3.
4. The minimum is specified for the duration of an edge triggered $\overline{\text{IRQA}}$ interrupt required to recover from the Stop state. This is not the minimum required so that the $\overline{\text{IRQA}}$ interrupt is accepted.
5. Timing 22 is for all IRQx interrupts while timing #23 is only when exiting the Wait state
6. Timing 22 triggers off T1 in the normal state and off phi1 when exiting the Wait state.
7. The instruction fetch is visible on the pins only in Mode 2 and Mode 3.

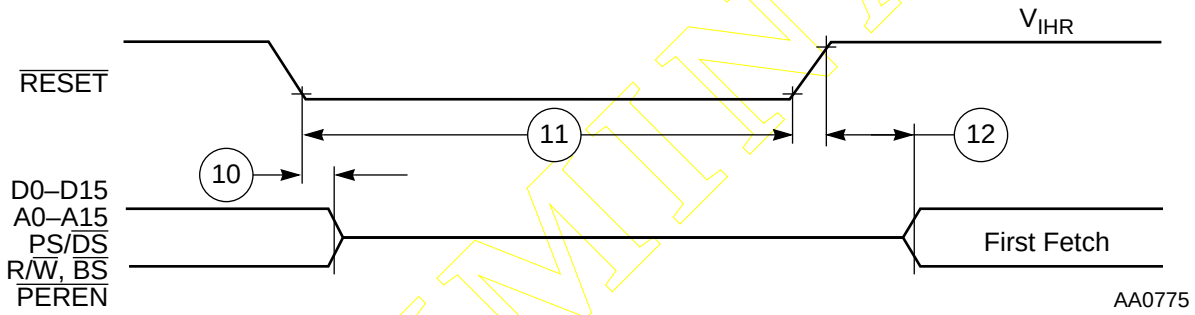


Figure 2-4 Asynchronous Reset Timing

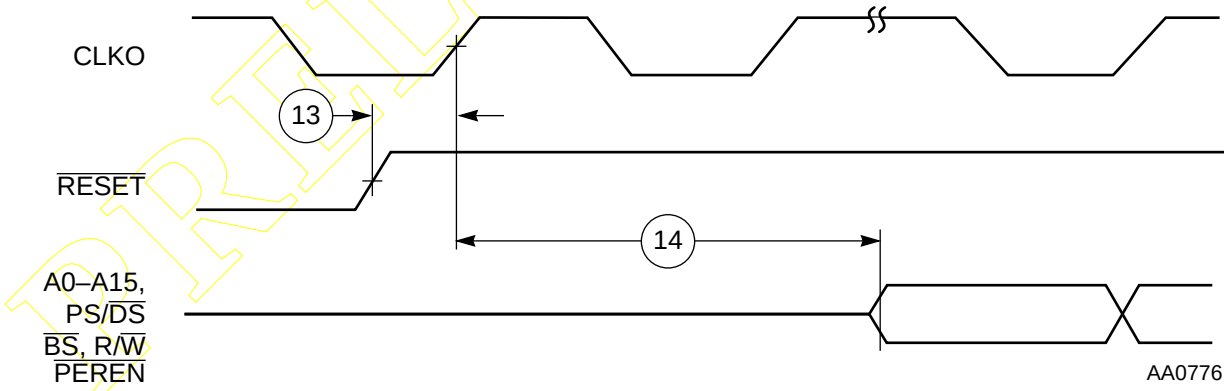


Figure 2-5 Synchronous Reset Timing

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

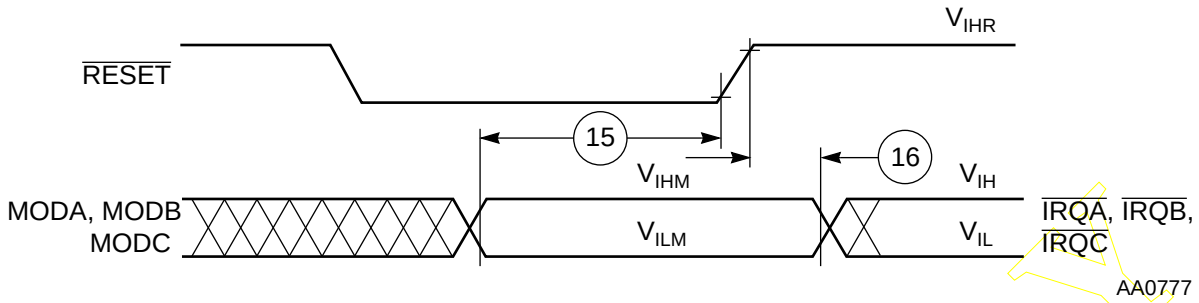


Figure 2-6 Operating Mode Select Timing

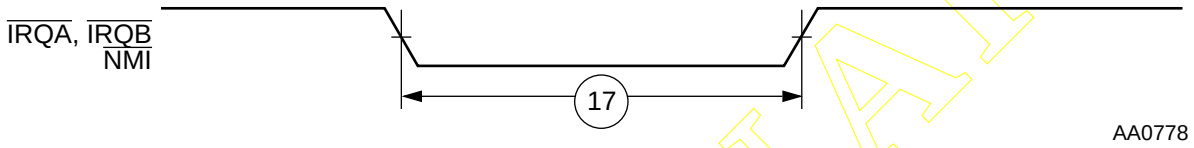


Figure 2-7 External Interrupt Timing (Negative Edge-Triggered)

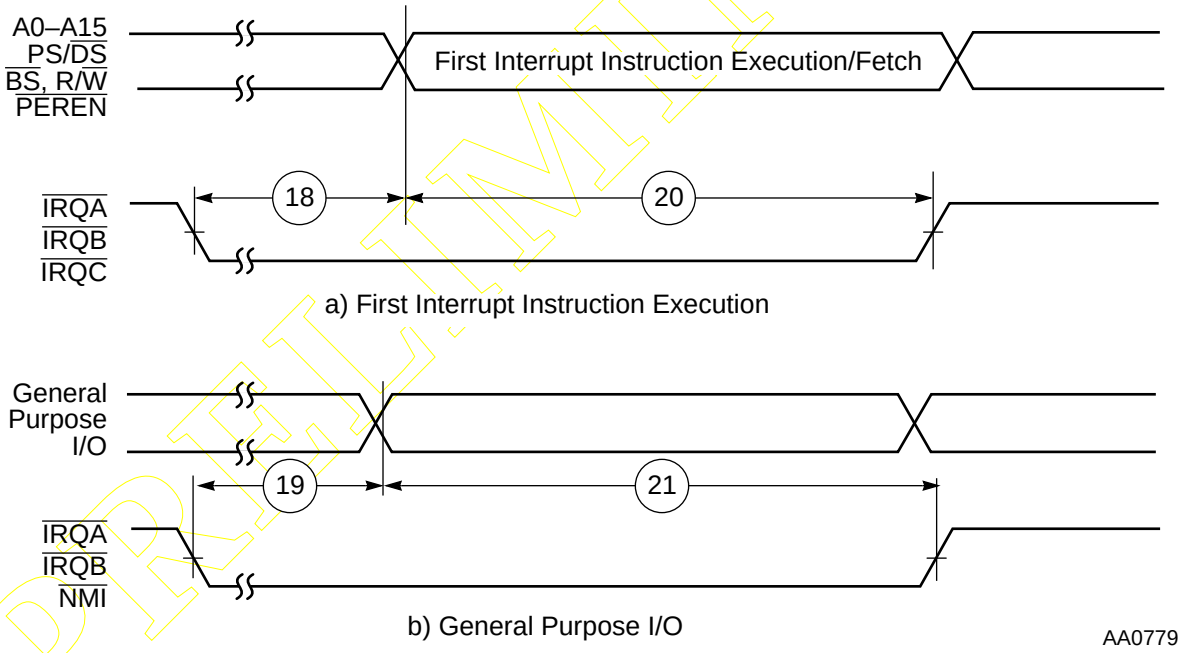


Figure 2-8 External Level-Sensitive Fast Interrupt Timing

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

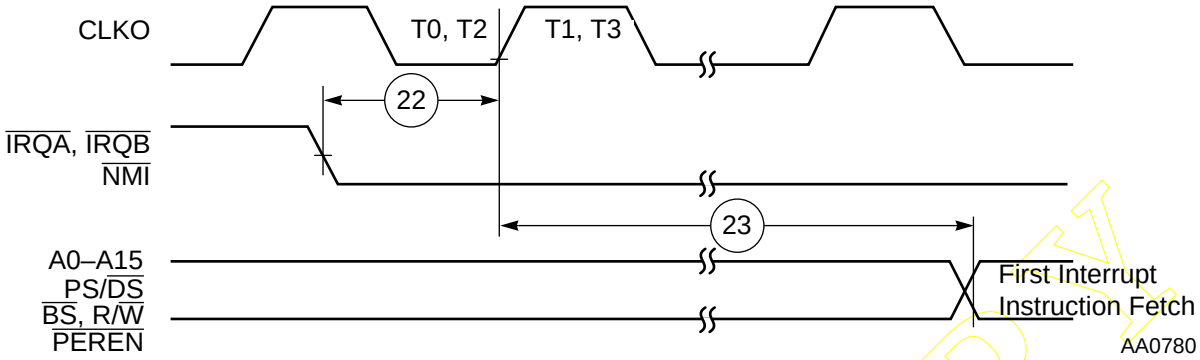


Figure 2-9 Synchronous Interrupt from Wait State Timing

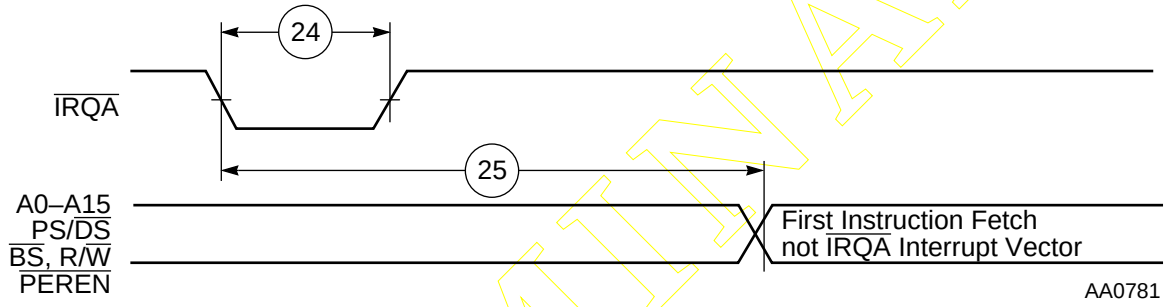


Figure 2-10 Recovery from Stop State Using Asynchronous Interrupt Timing

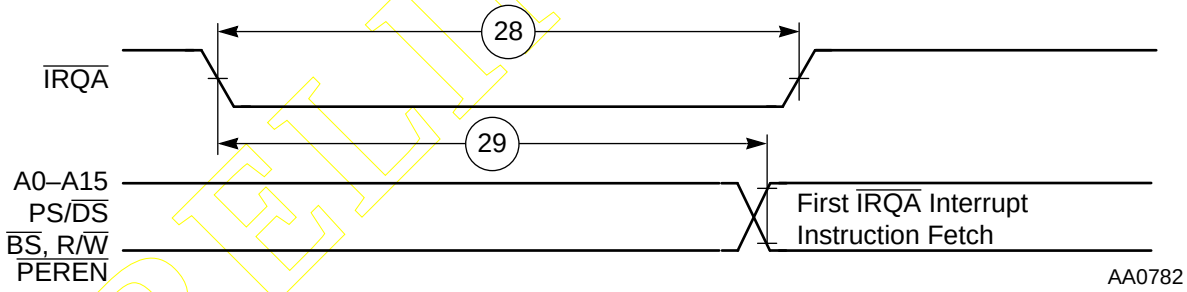


Figure 2-11 Recovery from Stop State Using IRQA Interrupt Service

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

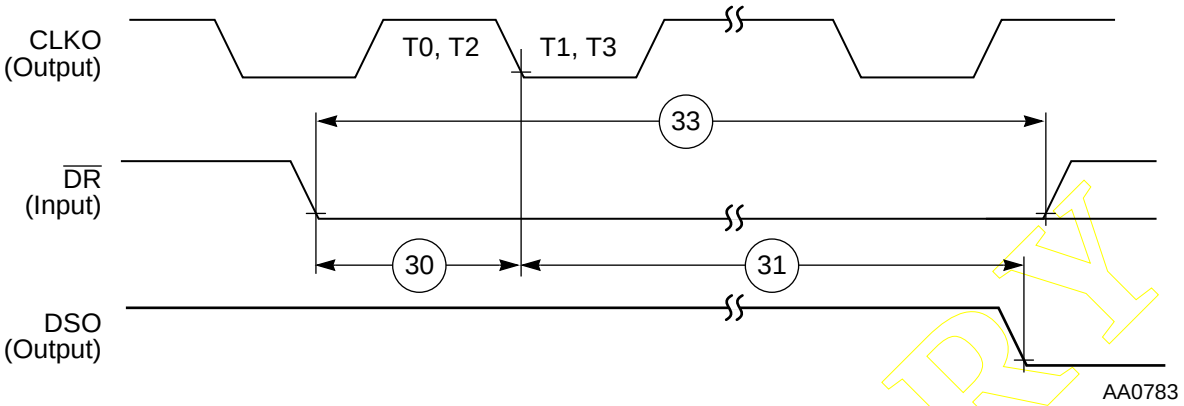


Figure 2-12 Recovery from Wait State Using DR—Synchronous Timing

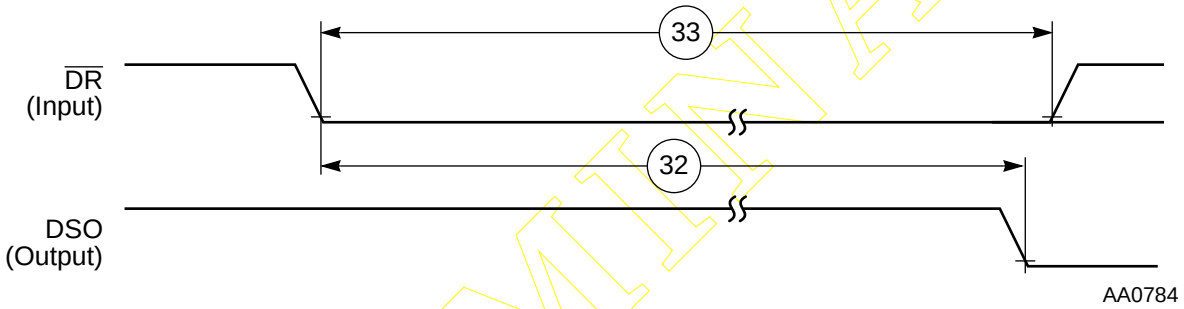


Figure 2-13 Recovery from Wait/Stop State Using DR—Asynchronous Timing

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

EXTERNAL BUS SYNCHRONOUS TIMING

V_{DD} = 5.0 V ± 10%; T_J = –40 to +115°C; C_L = 50 pF + 1 TTL load

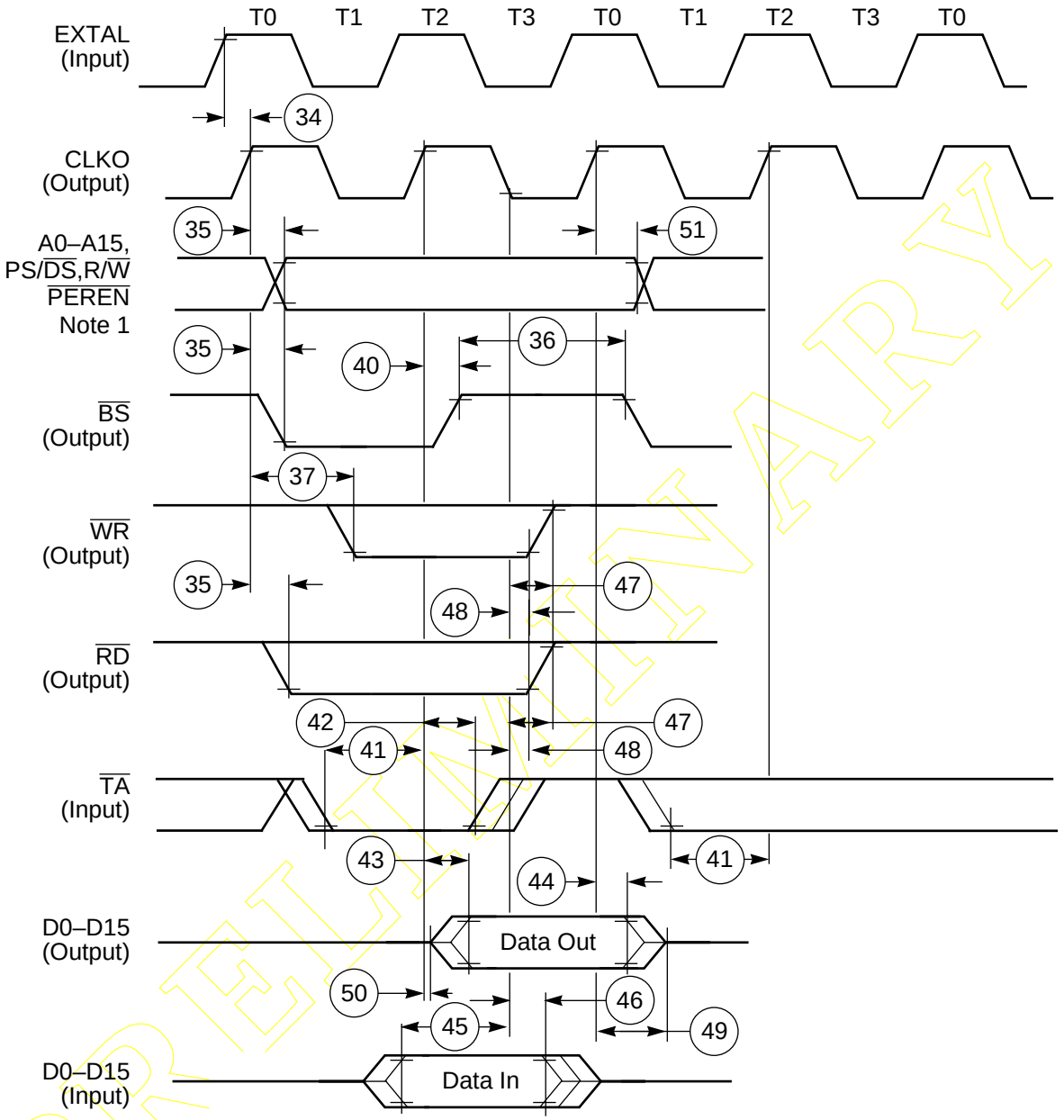
Capacitance Derating: The DSP56167 external bus timing specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the external bus pins (A0–A15, D0–D15, PS/$\overline{DS}$, $\overline{RD}$, $\overline{WR}$, $\overline{BS}$, $\overline{PEREN}$) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins (HI, SSI, and Timer) derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading. When an internal memory access follows an external memory access, the PS/$\overline{DS}$, R/$\overline{W}$, $\overline{RD}$, $\overline{WR}$, $\overline{BS}$, and $\overline{PEREN}$ strobes remain deasserted and A0–A15 do not change from their previous state.

Table 2-8 External Bus Synchronous Timing

Num	Characteristics	60 MHz		Unit
		Min	Max	
34	CLK in (EXTAL) High to CLKO High	2.2	10.0	ns
35	CLKO High to			
	a. A0–A15 Valid	—	4.0	ns
	b. PS/$\overline{DS}$, $\overline{PEREN}$ Assertion, R/$\overline{W}$ Valid	—	4.0	ns
	c. $\overline{BS}$ Assertion	—	4.0	ns
	d. $\overline{RD}$ Assertion	—	4.0	ns
36	$\overline{BS}$ Width Deassertion	14.6	—	ns
37	CLKO High to $\overline{WR}$ Assertion Low	T + 4.0	T + 6.0	ns
40	CLKO High to $\overline{BS}$ Deassertion	—	7.4	ns
41	a.$\overline{TA}$ Assertion to CLKO High (Setup)	6.5	—	ns
	b.$\overline{TA}$ Deassertion to CLKO High (Setup)	6.5	—	ns
42	a. CLKO High to $\overline{TA}$ Assertion (Hold)	2.0	—	ns
	b. CLKO High to $\overline{TA}$ Deassertion (Hold)	2.0	—	ns
43	CLKO High to D0–D15 Out Valid	—	4.0	ns
44	CLKO High to D0–D15 Out Invalid (Hold)	4.0	—	ns
45	D0–D15 In Valid to CLKO Low (Setup)	4.0	—	ns
46	CLKO Low to D0–D15 In Invalid (Hold)	0.0	—	ns
47	CLKO Low to			
	a. $\overline{WR}$ Deassertion	—	3.0	ns
	b. $\overline{RD}$ Deassertion	—	3.0	ns
48	a. $\overline{WR}$ Hold Time from CLKO Low	1.0	—	ns
	b. $\overline{RD}$ Hold Time from CLKO Low	1.0	—	ns
49	CLKO High to D0–D15 tri-stated	—	8.0	ns
50	CLKO High to D0–D15 Out Active	0	—	ns
51	CLKO High to			
	a. A0–A15 Invalid	0	—	ns
	b. PS/$\overline{DS}$, $\overline{PEREN}$, R/$\overline{W}$ Invalid	0	—	ns

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

AA0785

Figure 2-14 External Bus Synchronous Timing—No Wait States

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

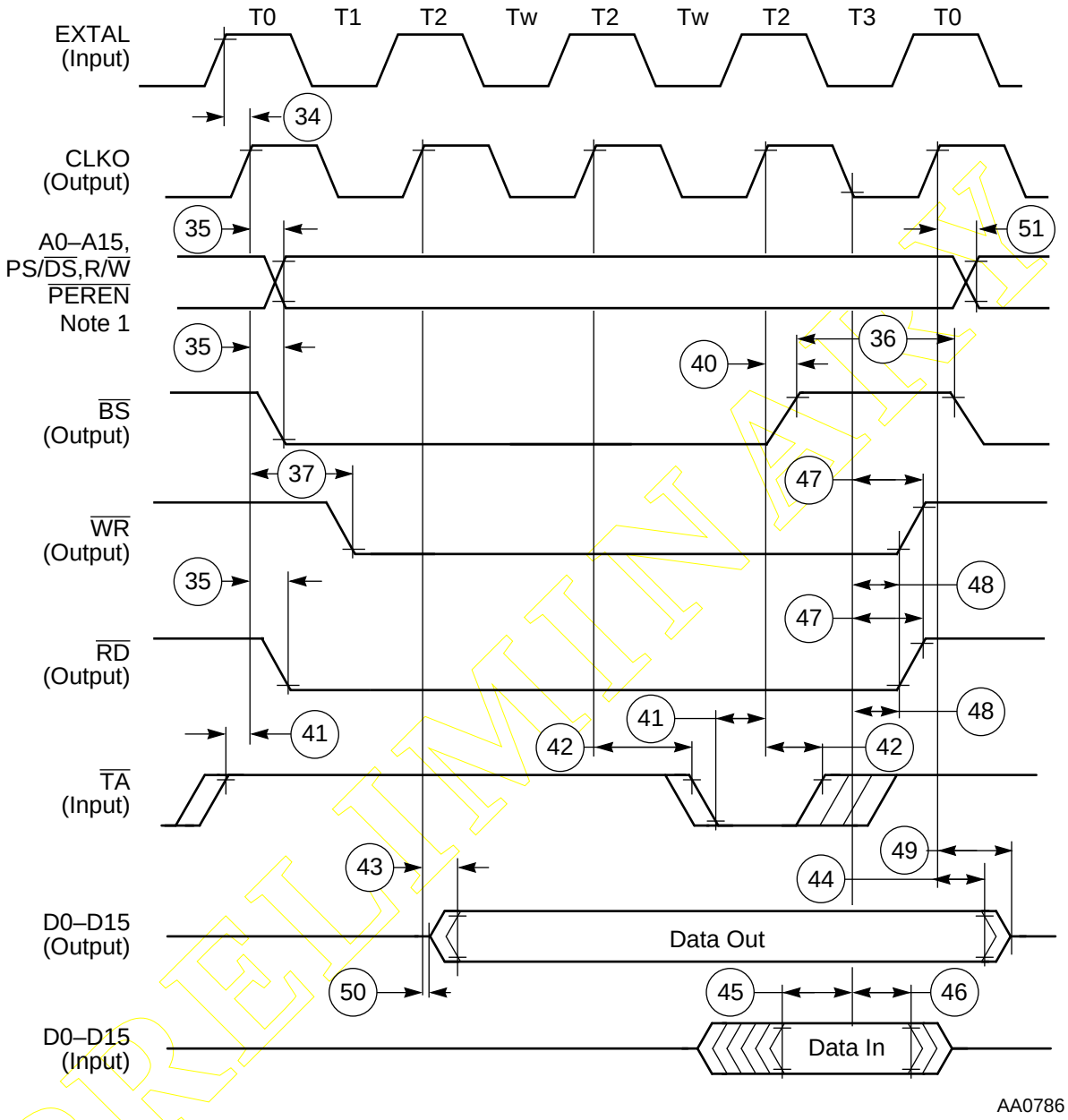


Figure 2-15 External Bus Synchronous Timing—Two Wait States

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

EXTERNAL BUS ASYNCHRONOUS TIMING

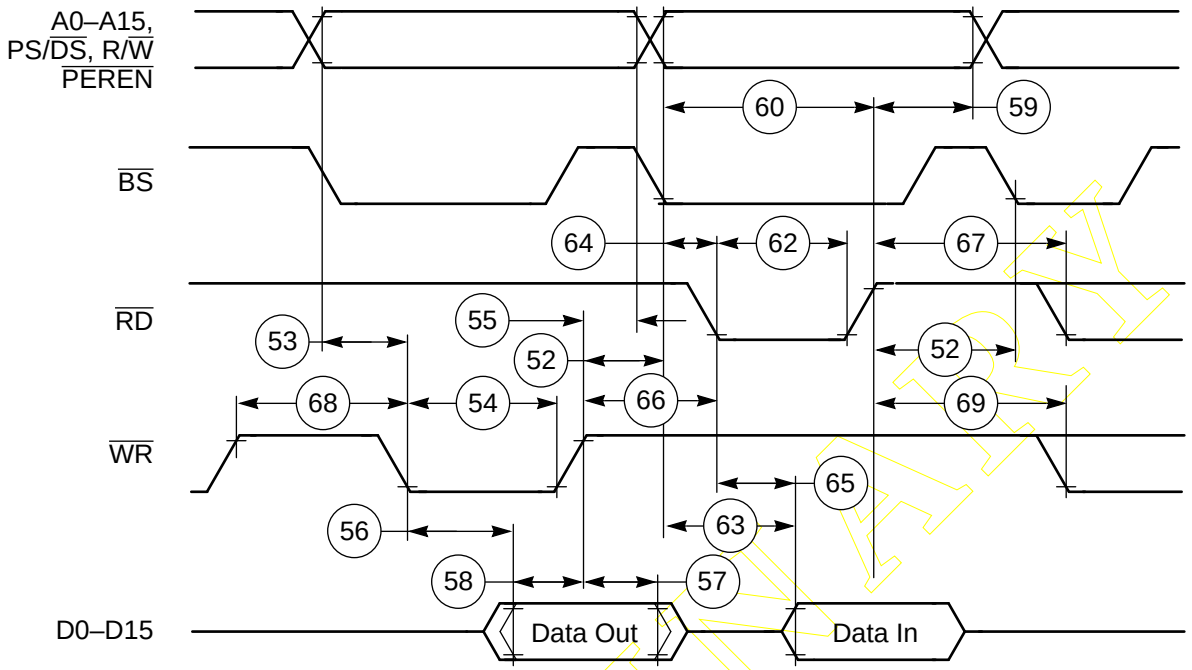
V_{DD} = 5.0 V ± 10%; TJ = –40 to +115°C; CL = 50 pF + 1 TTL load
cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles
WS = Number of Wait States, as determined by BCR (WS = 0 to 31)
WT = WS × cyc = 2T × WS

Table 2-9 External Bus Asynchronous Timing

No.	Characteristics	60 MHz		Unit
		Min	Max	
52	$\overline{WR}$ and $\overline{RD}$ Deassertion High to $\overline{BS}$ Assertion Low (Two Successive Bus Cycles)	14	—	ns
53	Address Valid to $\overline{WR}$ Assertion	6.4	—	ns
54	$\overline{WR}$ Width Assertion	12.5	—	ns
55	$\overline{WR}$ Deassertion to R/$\overline{W}$, Address Invalid	3.3	—	ns
56	$\overline{WR}$ Assertion to D0–D15 Out Valid	10.4	—	ns
57	Data Out Hold Time from $\overline{WR}$ Deassertion	4.0	—	ns
58	Data Out Set up Time to $\overline{WR}$Deassertion a. WS = 0 b. WS > 0	 5.0 WT + T – 3.3	 — —	 ns ns
59	$\overline{RD}$ Deassertion to Address not valid	4.0	—	ns
60	Address valid to $\overline{RD}$ Deassertion	22.1	—	ns
62	$\overline{RD}$ Assertion width a. WS = 0 b. WS > 0	 18 WT + 3T – 7	 — —	 ns ns
63	Address valid to input data valid a. WS = 0 b. WS > 0	 — —	 22 WT + 3T – 5	 ns ns
64	Address valid to $\overline{RD}$ Assertion	—	2.0	ns
65	$\overline{RD}$ Assertion to input data valid	18.6	—	ns
66	$\overline{WR}$ Deassertion to $\overline{RD}$ Assertion	6.8	—	ns
67	$\overline{RD}$ Deassertion to $\overline{RD}$ Assertion	8.5	—	ns
68	$\overline{WR}$ Deassertion to $\overline{WR}$ Assertion	13.1	—	ns
69	$\overline{RD}$ Deassertion to $\overline{WR}$ Assertion	16.0	—	ns

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor



Note: During Read-Modify-Write instructions and internal instructions, the address lines do not change state.

AA0787

Figure 2-16 External Bus Asynchronous Timing

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

BUS ARBITRATION TIMING—SLAVE MODE

V_{DD} = 5.0 V ± 10%; TJ = –40 to +115°C; CL = 50 pF + 1 TTL load
cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles
WS = Number of Wait States for X or P external memory, determined by BCR or BCR2 (WS = 0 to 31)
WT = WS × cyc = 2T × WS
W_X = Number of Wait States for X external memory, determined by BCR or BCR2 (WS = 0 to 31)
W_P = Number of Wait States for P external memory, determined by BCR (WS = 0 to 31)

Table 2-10 Slave Mode Bus Arbitration Timing

No.	Characteristics	60 MHz		Unit
		Min	Max	
70	$\overline{BR}$ Input to CLKO low setup time	2.8	—	ns
71	Delay from $\overline{BR}$ Input Assertion to $\overline{BG}$ Output Assertion	25	—	ns
	No external access by the DSP	5T + 6.6	9T +3.1	
	External read or write access	3T + 6.6	9T+WT+3.1	
	External read-modify-write access	5T + 6.6	26T+ 4T x W_X + 2T x W_P + 2.7	
	Stop mode—external bus released and $\overline{BG}$ asserted	—	—	
	Wait mode	T+6.6	3T + 2.7	
72	CLKO high to $\overline{BG}$ Output Assertion	—	10.2	ns
73	$\overline{BG}$ Output Deassertion duration for two consecutive $\overline{BR}$			
	No external access by the DSP	5T + 3.7	—	ns
	External read or write access	5T + 3.7	—	ns
	External read-modify-write access	5T + 3.4	—	ns
	Stop mode—external bus released and $\overline{BG}$ asserted	—	—	
	Wait mode	2T + 3.3	—	ns
	External DSP accesses pending	3T + 3.4	—	ns
74	CLKO High to Control Bus high impedance	—	8.0	ns
75	CLKO High to $\overline{BB}$ Output Deassertion	7.0	—	ns
76	CLKO High to $\overline{BB}$ Output (tri-stated)	—	18.0	ns
77	$\overline{BR}$ Input Deassertion to $\overline{BG}$ Output Deassertion	—	8.5	ns
78	CLKO High to $\overline{BG}$ Deassertion	—	15.0	ns
79	CLKO High to $\overline{BB}$ Output Active	1.0	—	ns
80	CLKO High to $\overline{BB}$ Output Assertion	—	9.4	ns
81	CLKO High to Address and Control Bus Active	1.0	—	ns
82	CLKO High to Address and Control Bus Valid	—	9.7	ns

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 2-10 Slave Mode Bus Arbitration Timing (Continued)

No.	Characteristics	60 MHz		Unit
		Min	Max	
83	$\overline{BR}$ Assertion to $\overline{BB}$ Deassertion			
	No external access by the DSP		9T + 3.1	ns
	External read or write access		9T + WT + 3.1	ns
	External read-modify-write access		$26T + 4T \times W_X + 2T \times W_P + 2.7$	ns
	Stop mode—external bus released and $\overline{BG}$ asserted		—	
	Wait mode		3T + 2.7	ns
84	$\overline{BR}$ Assertion to Address / Data / Control lines tri-stated			
	No external access by the DSP		9T + 8.0	ns
	External read or write access		9T + WT + 8.0	ns
	External read-modify-write access		$26T + 4T \times W_X + 2T \times W_P + 2.7$	ns
	Stop mode—external bus released and $\overline{BG}$ asserted		—	
	Wait mode		3T + 2.7	ns

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

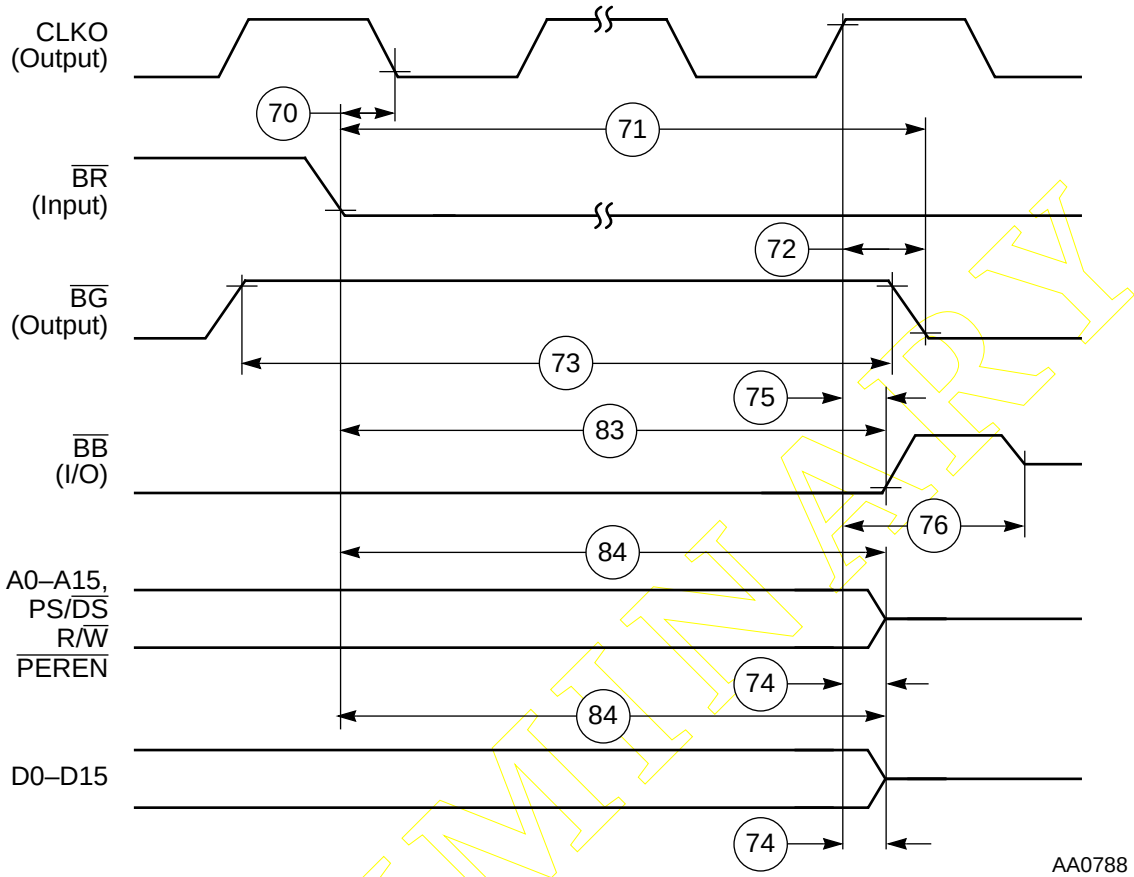


Figure 2-17 External Bus Arbitration Bus Release Timing—Slave Mode

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

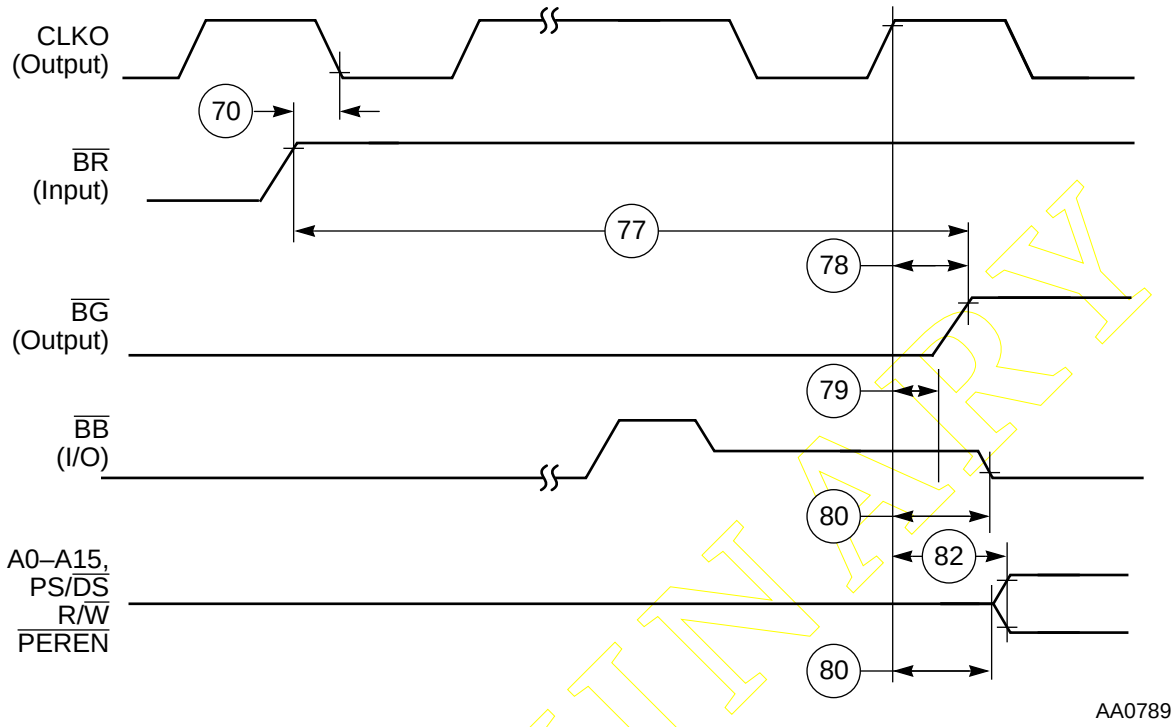


Figure 2-18 External Bus Arbitration Bus Acquisition Timing—Slave Mode

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

BUS ARBITRATION TIMING—MASTER MODE

V_{DD} = 5.0 V ± 10%; TJ = –40 to +115°C; CL = 50 pF + 1 TTL load

Table 2-11 Master Mode Bus Arbitration Timing

No.	Characteristics	60 MHz		Unit
		Min	Max	
85	CLKO high to $\overline{BR}$ Output Valid	—	9.0	ns
86	$\overline{BG}$ Input Valid to CLKO Low (Setup)	1.9	—	ns
87	CLKO Low to $\overline{BG}$ Input Deassertion (Hold)	2.0	—	ns
88	$\overline{BB}$ Input Deassertion to CLKO Low (Setup)	2.0	—	ns
89	CLKO Low to $\overline{BB}$ Input Deassertion (Hold)	2.0	—	ns
90	CLKO High to $\overline{BB}$ Output Assertion	—	11.4	ns
91	CLKO Low to $\overline{BG}$ Input Assertion			
	No external access by the DSP	—	—	ns
	External read or write access	3	—	ns
92	$\overline{BG}$ Deassertion to $\overline{BB}$ Deassertion			
	No external access by the DSP	—	—	ns
	External read or write access	—	48.3	ns
	External read-modify-write-access	—	64.9	ns
	Stop mode - external bus released and $\overline{BG}$ asserted	—	—	ns
	Wait mode	—	—	ns
93	$\overline{BG}$ Deassertion to Address / Data / Control lines tri-stated			
	No external access by the DSP	—	—	ns
	External read or write access	53.3	—	ns
	External read-modify-write-access	69.9	—	ns
	Stop mode - external bus released and $\overline{BG}$ asserted	—	—	ns
	Wait mode	—	—	ns

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

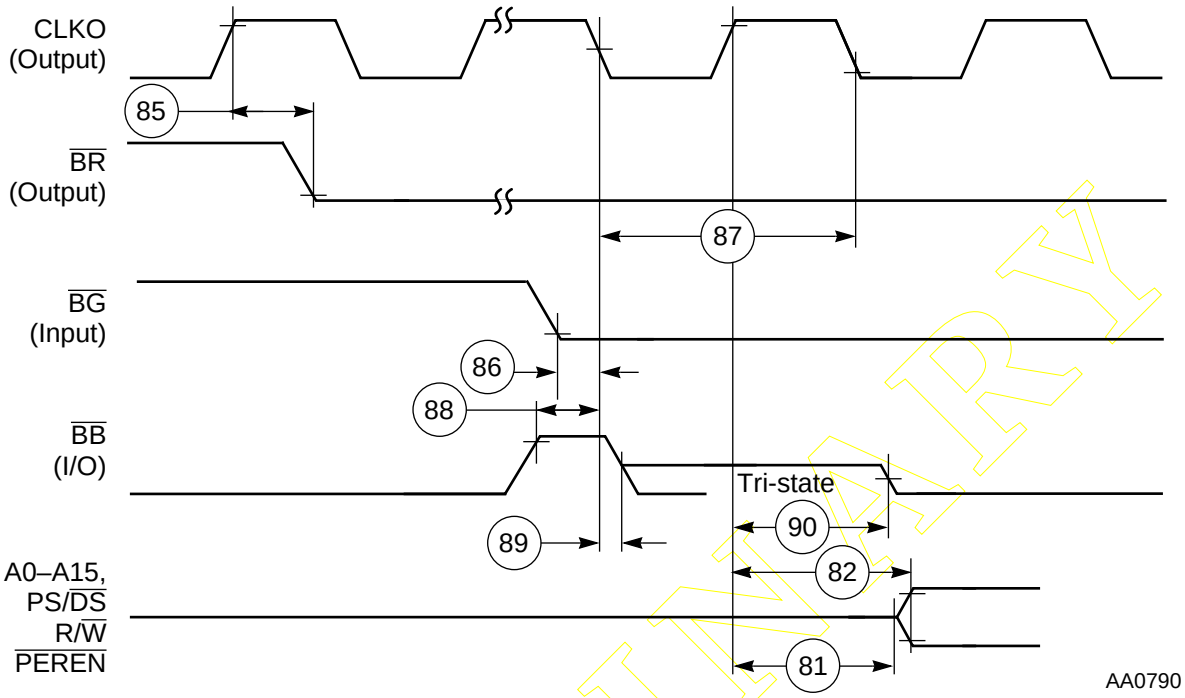


Figure 2-19 External Bus Arbitration Bus Acquisition Timing—Master Mode

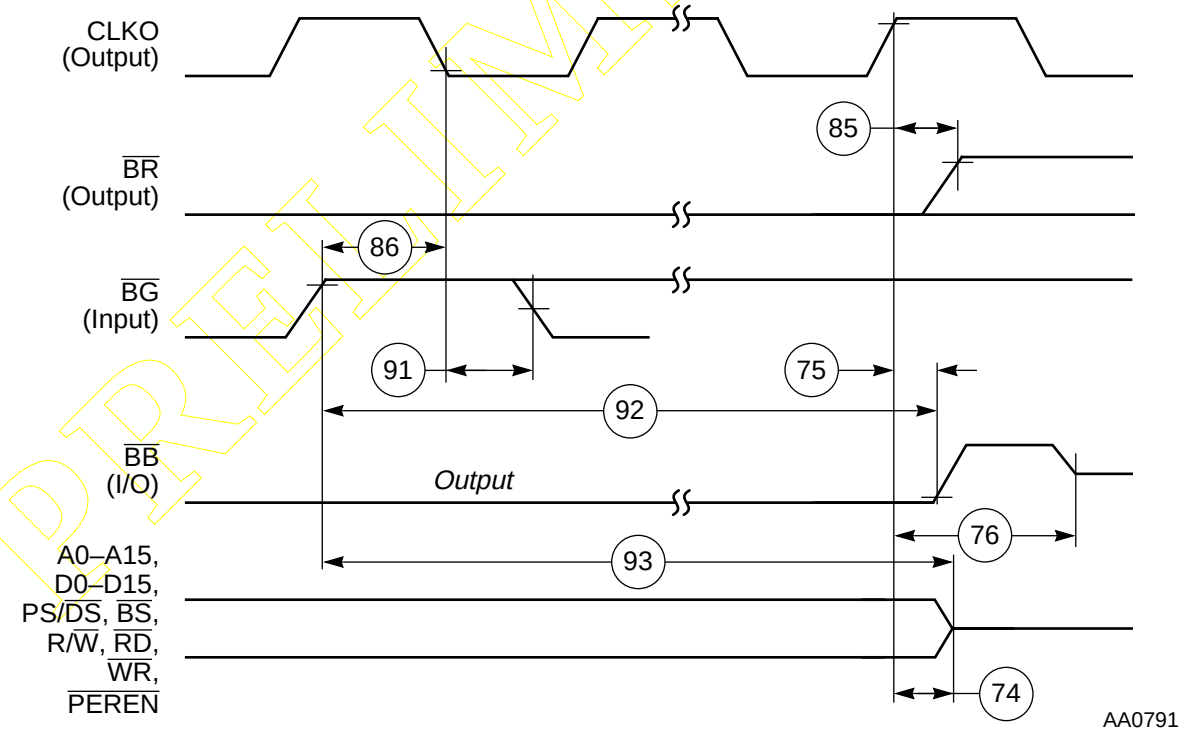


Figure 2-20 External Bus Arbitration Bus Release Timing—Master Mode

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

HOST I/O (HI) TIMING

V_{DD} = 5.0 V ± 10%; T_J = –40 to +115°C; C_L = 50 pF + 1 TTL load
T = I_{CYC} / 4
cyc = Clock cycle = 1/2 Instruction cycle = 2 T cycle
t_{HSDL} = Host Synchronization Time Delay
t_{SUH} = Host processor data setup time

Note: Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications.

Table 2-12 Host I/O Timing

Num	Characteristics	Min	Max	Unit
100	Host Synchronous Delay[1]	T	3T	ns
101	$\overline{HEN}$ / $\overline{HACK}$ assertion width a. CVR,ICR, ISR Read[2,4] b. Read c. Write	 2T + 30 25 27	 — — —	 ns ns ns
102	$\overline{HEN}$ / $\overline{HACK}$ deassertion width[2]	27	—	ns
103	Minimum cycle time between two $\overline{HEN}$ assertions for Consecutive CVR, ICR, ISR reads	4T + 30	—	ns
104	Host data input setup time before $\overline{HEN}$ / $\overline{HACK}$ deassertion	3	—	ns
105	Host data input hold time after $\overline{HEN}$ / $\overline{HACK}$ deassertion	9	—	ns
106	$\overline{HEN}$ / $\overline{HACK}$ assertion to output data active from tri-state	—	24	ns
107	$\overline{HEN}$ / $\overline{HACK}$ assertion to output data valid	—	24	ns
108	$\overline{HEN}$ / $\overline{HACK}$ deassertion to output data tri-stated	—	17	ns
109	Output data hold time after $\overline{HEN}$ / $\overline{HACK}$ deassertion	5	—	ns
110	HR / $\overline{W}$ low setup time before $\overline{HEN}$ assertion	4	—	ns
111	HR / $\overline{W}$ low hold time after $\overline{HEN}$ deassertion	4	—	ns
112	HR / $\overline{W}$ high setup time to $\overline{HEN}$ assertion	4	—	ns
113	HR / $\overline{W}$ high hold time after $\overline{HEN}$ / $\overline{HACK}$ deassertion	3	—	ns
114	HA0–HA2 setup time before $\overline{HEN}$ assertion	0	—	ns
115	HA0–HA2 hold time after $\overline{HEN}$ deassertion	6	—	ns
116	DMA $\overline{HACK}$ assertion to $\overline{HREQ}$ deassertion[3]	6	2T + 35	ns
117	DMA $\overline{HACK}$ deassertion to $\overline{HREQ}$ assertion[3] for DMA RXL Read for DMA TXL Write for All Other Cases	 t_{HSDL} + 3T + 4 t_{HSDL} + 2T + 4 4	 — — —	 ns ns ns

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 2-12 Host I/O Timing (Continued)

Num	Characteristics	Min	Max	Unit
118	Delay from $\overline{\text{HEN}}$ deassertion to $\overline{\text{HREQ}}$ assertion for RXL read[3]	t_{HSDL} + 3T + 4	—	ns
119	Delay from $\overline{\text{HEN}}$ deassertion to $\overline{\text{HREQ}}$ assertion for TXL write[3]	t_{HSDL} + 2T + 4	—	ns
120	Delay from $\overline{\text{HEN}}$ assertion to $\overline{\text{HREQ}}$ deassertion for RXL read, TXL write[3]	13.7	2T + 16.4	ns

Note:
1. "Host synchronization delay (t_{HSDL})" is the time period required for the DSP56167 to sample any external asynchronous input signal, determine whether it is high or low, and synchronize it to the internal clock.
2. See **Host Port Considerations** in the section on **Design Considerations**.
3. $\overline{\text{HREQ}}$ is pulled up by 1 kΩ.
4. Only if two consecutive reads from one of these registers are executed

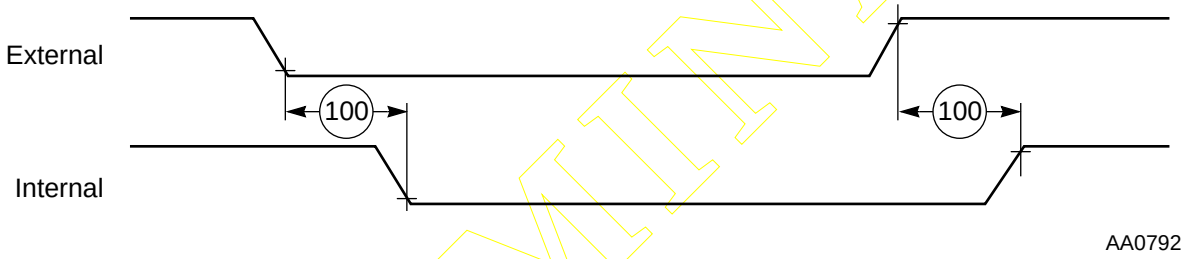


Figure 2-21 Host Synchronization Delay

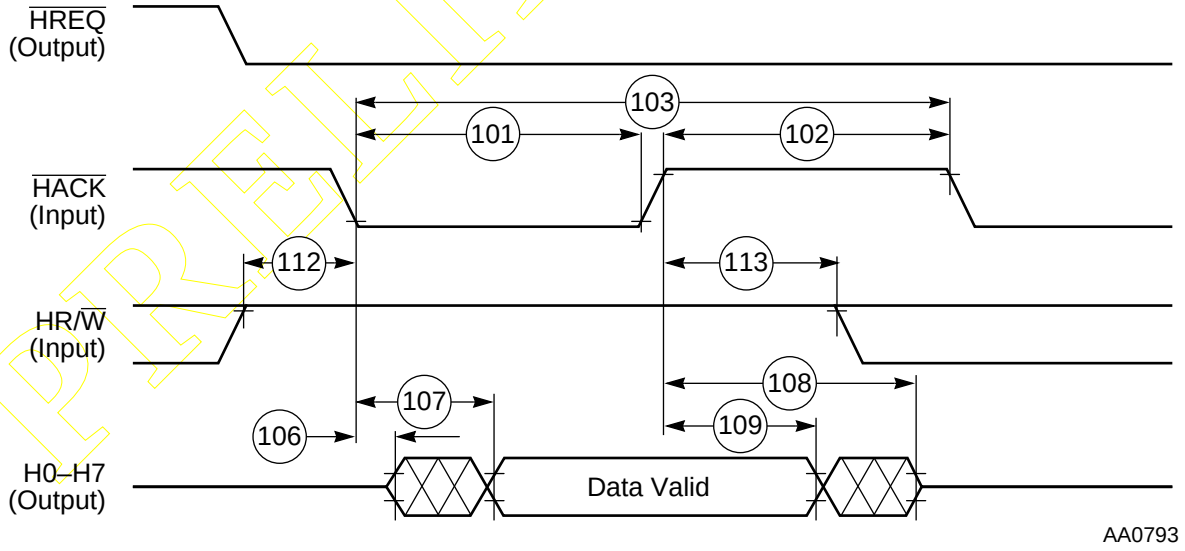


Figure 2-22 Host Interrupt Vector Register (IVR) Read

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

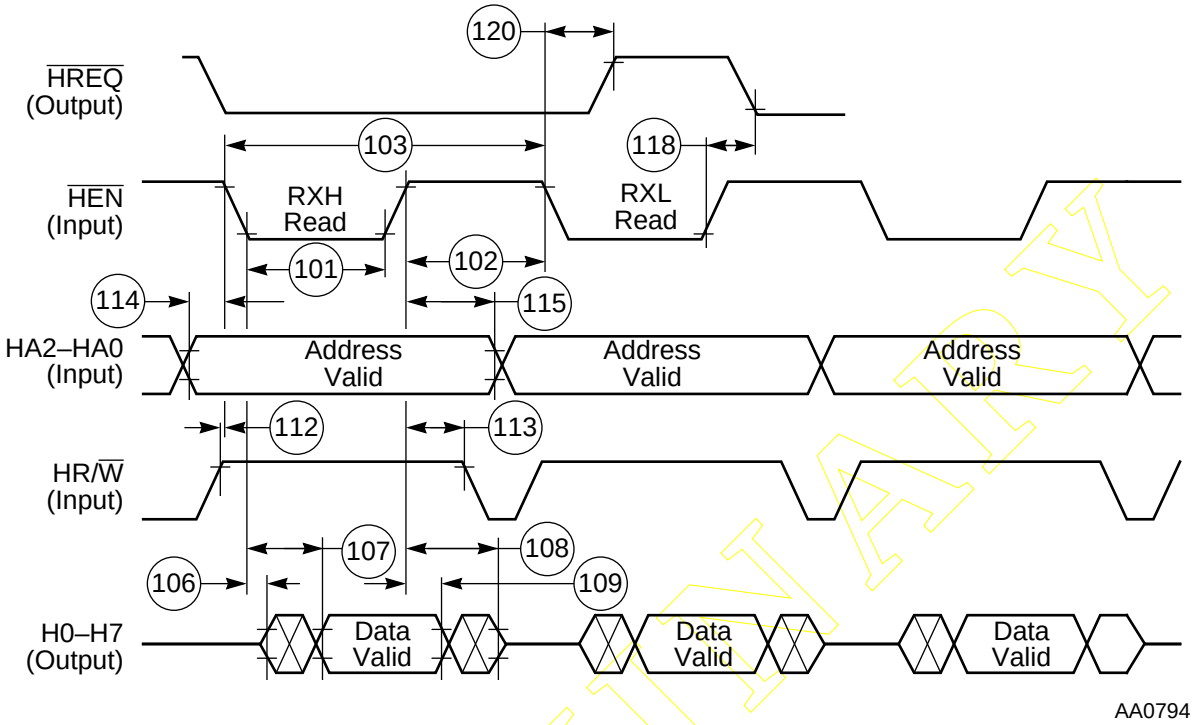


Figure 2-23 Host Read Cycle (Non-DMA Mode)

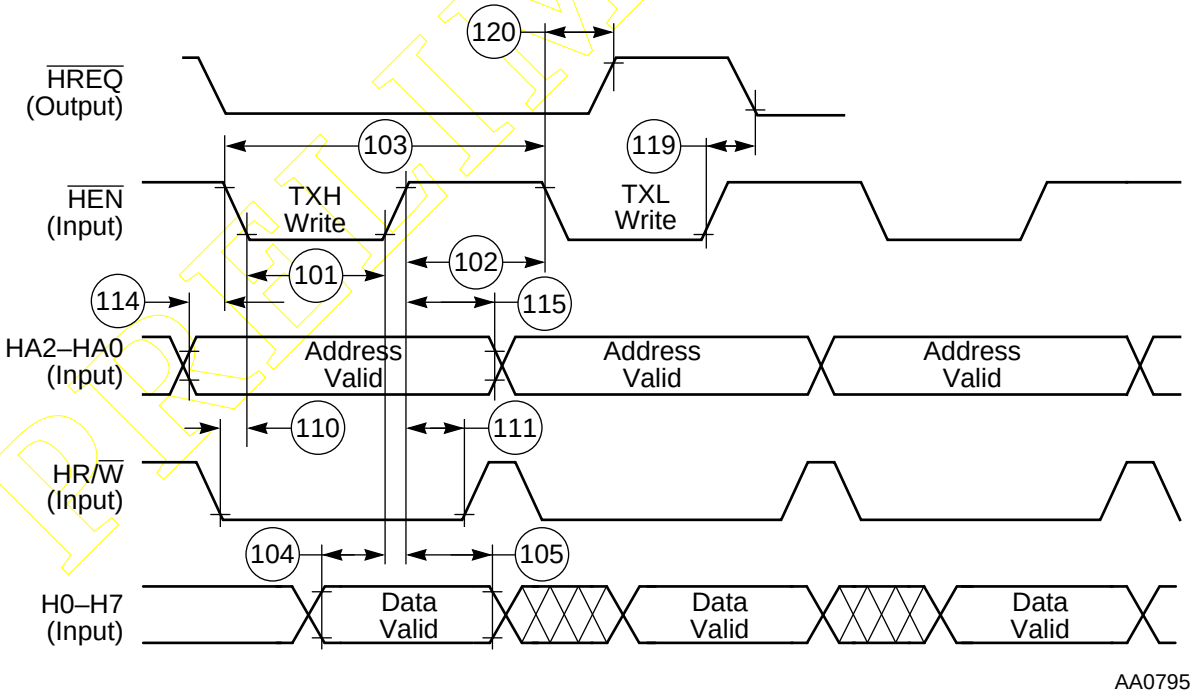


Figure 2-24 Host Write Cycle (Non-DMA Mode)

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

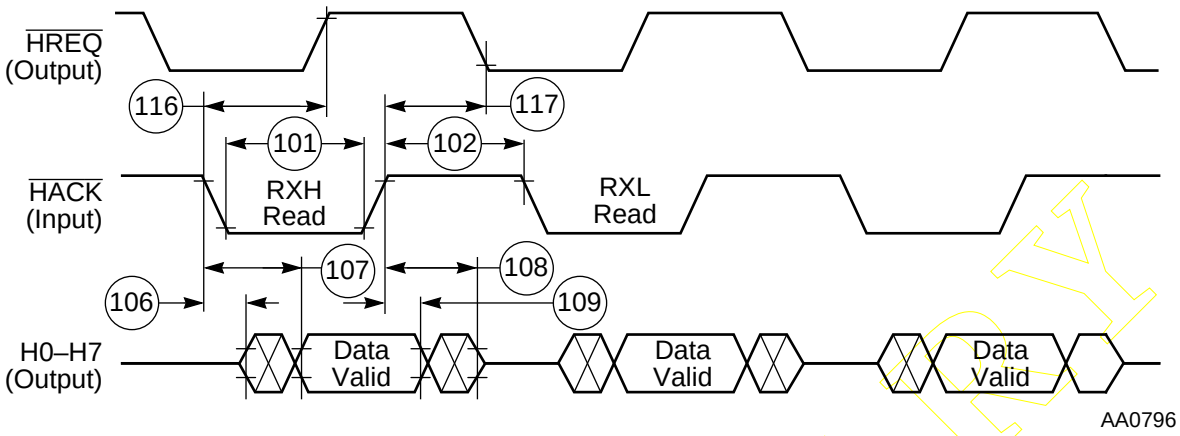


Figure 2-25 Host DMA Read Cycle

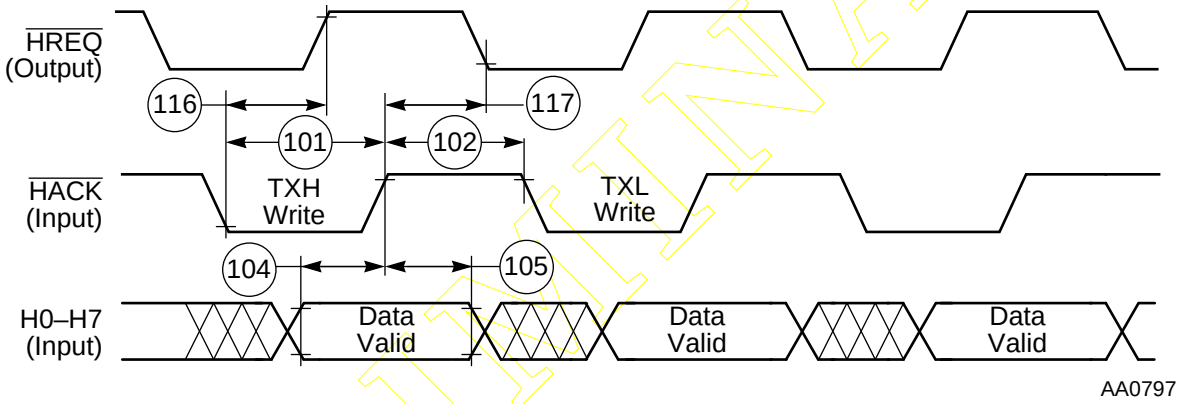


Figure 2-26 Host DMA Write Cycle

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

CODEC ANALOG I/O CHARACTERISTICS

V_{DDA} = 5.0 V ± 10%; T_J = –40 to +115˚C

Table 2-13 Codec Analog I/O Characteristics

Characteristic	Min	Typ	Max	Unit
Input impedance of MIC and AUX when selected as the A/D input:				
–6 dB, MGS[1:0] = 00	60	100	140	kΩ
0 dB, MGS[1:0] = 01	45	75	105	kΩ
6 dB, MGS[1:0] = 10	30	50	70	kΩ
17 dB, MGS[1:0] = 11	30	50	70	kΩ
Input impedance of MIC and AUX when not selected as the A/D input	100	140	—	kΩ
Maximum source or sink current of MIC or AUX when not selected as the A/D input	—	24	—	µA
Input capacitance on MIC and AUX	—	—	10	pF
Peak input voltage on the MIC/AUX input for full scale linearity at V_{DDA} = 5.000 V:				
–6 dB, MGS[1:0] = 00	—	—	1.414	V_P
0 dB [1], MGS[1:0] = 01	—	—	0.707	V_P
6 dB, MGS[1:0] = 10	—	—	0.354	V_P
17 dB, MGS[1:0] = 11	—	—	0.100	V_P
Absolute gain variation due to V_{DDA} variation for all A/D and D/A gain settings (0.83 dB due to 10% variation on V_{DDA})	G – 0.92	G	G + 0.83	dB
A/D absolute gain variation due to internal circuitry for all A/D gain settings (variation from ideal VRAD of 0.5 V_{DDA})	G – 1.49	G	G + 1.27	dB
D/A absolute gain variation due to internal circuitry for all D/A gain settings (variation from ideal VRDA of 0.5 V_{DDA})	G – 1.39	G	G + 1.20	dB
VRDA and VRAD output voltage plus offset (assumes no leakage current on the VDIV pin and VDDA = 5.000 V)	—	2.500 ± 0.010	2.500 ± 0.050	V
SPKP, SPKM, VRDA, and VRAD output current	—	—	350	µA
VDIV AC input impedance	—	42.5	—	kΩ
VDIV I/O voltage plus offset (assumes there is not leakage current on the I/O and V_{DDA} = 5.000 V)	—	2.500 ± 0.005	2.500 ± 0.025	V
Differential DC offset between SPKP and SPKM	—	—	50	mV
Single-ended DC offset of SPKP and SPKM with respect to VRDA	—	—	100	mV

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 2-13 Codec Analog I/O Characteristics (Continued)

Characteristic	Min	Typ	Max	Unit
A/D output DC offset (assuming input is at VRAD): –6 dB, MGS[1:0] = 00 0 dB, MGS[1:0] = 01 6 dB, MGS[1:0] = 10 17 dB, MGS[1:0] = 11	 $FF00 $FE00 $FC00 $F800	 $0000 $0000 $0000 $0000	 $0100 $0200 $0400 $0800	
Allowable differential load capacitance between SPKP and SPKM (with 3 kΩ in series, 4 kHz maximum frequency)	—	—	15	nF
Allowable single-ended load capacitance on SPKP and SPKM (with 1.5 kΩ in series, 4 kHz maximum frequency)[2]	—	—	30	nF
Allowable single-ended shunt capacitance to ground	—	—	50	pF
Allowable differential shunt capacitance	—	—	25	pF
Maximum linear range of single-ended signal output level at VDDA = 5.000 V: –15 dB, VC[3:0] = 0000 –10 dB, VC[3:0] = 0001 –5 dB, VC[3:0] = 0010 0 dB[3], VC[3:0] = 0011 5–40 dB, VC[3:0] > 0011	 — — — — —	 — — — — —	 0.125 0.223 0.397 0.707 1.000	 V_P V_P V_P V_P V_P
Maximum linear range of single-ended signal output level at VDDA = 5.000 V: –15 dB, VC[3:0] = 0000 –10 dB, VC[3:0] = 0001 –5 dB, VC[3:0] = 0010 0 dB[3], VC[3:0] = 0011 5–40 dB, VC[3:0] > 0011	 — — — — —	 — — — — —	 0.250 0.446 0.794 1.414 2.000	 V_P V_P V_P V_P V_P
Single-ended load resistance (referenced from 0.5 V_{DDA})	2.8	—	—	kΩ
Differential load resistance	5.6	—	—	kΩ
Output impedance of SPKP and SPKM at 0 Hz to 4 kHz	—	50	—	Ω
Output impedance of SPKP and SPKM during power down	140	200	280	kΩ
Output transition time of SPKP and SPKM from codec power up condition[4]	—	—	15	µs

Note:
1. 0 dBm0 corresponds to 3.00 dB below the input saturation level of 1.0 V_P with V_{DDA} = 5.0 V.
2. AC coupling is necessary in Single-Ended mode when the load resistor is not tied to VRDA.
3. 0 dBm0 corresponds to 3.00 dB below the output saturation level of 1.0 V_P single-ended with V_{DDA} = 5.0 V.
4. During power down and during the first 15 µs after a power up event, the maximum current loading for SPKP and SPKM pins is 1.0 µA.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

CODEC A/D AND D/A PERFORMANCE

V_{DDA} = 5.0 V ± 10%; T_J = –40 to +115˚C

Table 2-14 Codec Performance Levels

Characteristic	Input Signal Level	Min.	Typical[1]	Max.	Unit
A / D Signal-to-Noise plus distortion ratio S /(N + THD)	0 dBm0	55	65	—	dB
	–50 dBm0	15	20	—	dB
D / A Signal-to-Noise plus distortion ratio S / (N + THD)	0 dB	55	60	—	dB
	–50 dB	15	15	—	dB

Note: 1. 0 dB gain on the A / D and D / A; codec clock at 2.048 MHz with 128 decimation / interpolation ratio
2. 0 dBm0 corresponds to 3.00 dB below the input saturation level of 1.0 V_P single-ended with V_{DDA} = 5.0 V.

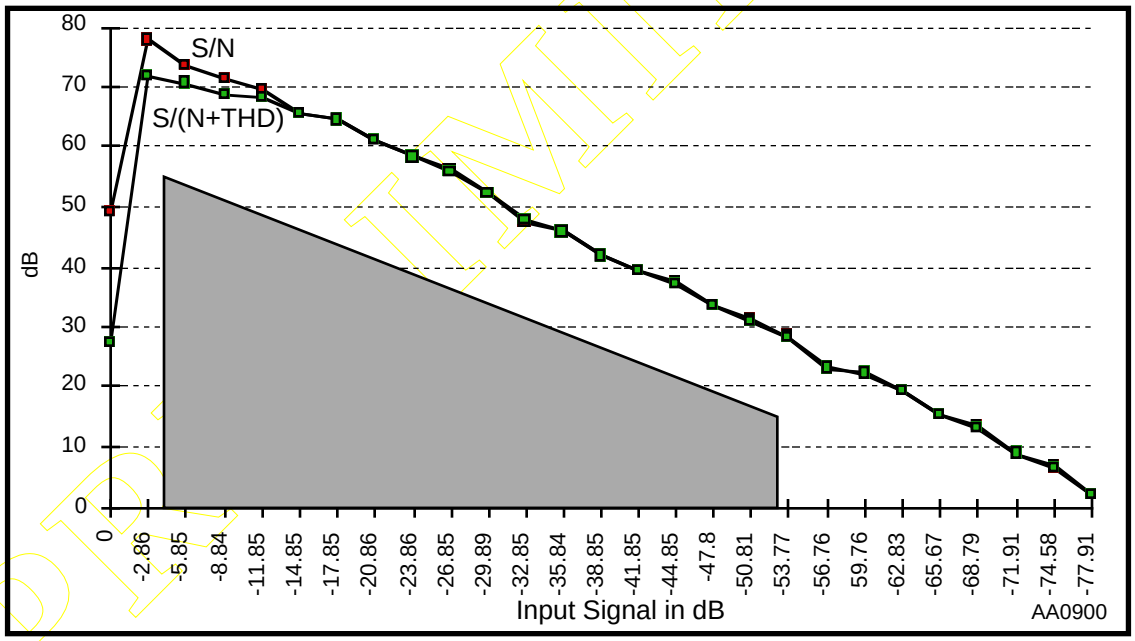


Figure 2-27 An Example of S/N and S/(N + THD) Performance for the Codec A/D Section

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

OTHER ON-CHIP CODEC CHARACTERISTICS

V_{DD} = 5.0 V ± 10%; T_J = –40 to +115˚C; C_L = 50 pF + 1 TTL load

Table 2-15 Codec I/O Device Characteristics

Characteristic	Min.	Typical	Max.	Unit
Codec master clock	1	2.048	3	MHz
Codec sampling rate	7812	16000	46150	Hz
A/D section group delay	0.06	0.17	0.40	ms
D/A section group delay	0.07	0.17	0.37	ms

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

16-BIT SYNCHRONOUS SERIAL INTERFACE (SSI) TIMING

V_{DD} = 5.0 V ± 10%; T_J = –40 to +115°C; C_L = 50 pF + 1 TTL load
T = I_{CYC} / 4
SCK = Serial Clock
SFS = Transmit / Receive Frame Sync
i ck = Internal Clock and Frame Sync
x ck = External Clock and Frame Sync
bl = bit length
wl = word length
T_S = SCK / 2

Note: All the timings for the 16-bit SSI are given for a non-inverted serial clock polarity (SCKP = 0 in CRB) and a non-inverted frame sync (FSI = 0 in CRB). If the polarity of the clock and / or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK and / or the frame sync SFS in the tables and in the figures.

Table 2-16 SSI Timing

Num	Characteristics	60 MHz		Case	Unit
		Min	Max		
134	SCK Rising Edge to SFS In (bl) High	—	20.4	i ck	ns
135	SCK Rising Edge to SFS In (bl) Low	16.7	—	i ck	ns
136	SCK Rising Edge to SFS In (wl) High	—	20.4	i ck	ns
137	SCK Rising Edge to SFS In (wl) Low	—	$T_S \times 2$	i ck	ns
138	Data In Setup Time Before SCK Falling Edge	3.0	—	i ck	ns
139	Data In Hold Time After SCK Falling Edge	8.5	—	i ck	ns
140	SCK Rising Edge to SFS Out (bl) High	—	21	i ck	ns
141	SCK Rising Edge to SFS Out (wl) High	—	16.0	i ck	ns
142	SCK Rising Edge to SFS Out Low	—	20.4	i ck	ns
143	SCK Rising Edge to Data Out Enable from High Impedance	—	1.2	i ck	ns
144	SCK Rising Edge to Data Out Valid	—	10	i ck	ns
145	SCK Rising Edge to Data Out Invalid	—	16.7	i ck	ns
146	SCK Rising Edge to Data Out High Impedance	—	16.7	i ck	ns
150	SCK Clock Cycle[1]	27	—	x ck	ns
153	SCK Clock Rise / Fall Time	—	10	x ck	ns
154	SCK Rising Edge to SFS Out (bl) High	—	3.3	x ck	ns
155	SCK Rising Edge to SFS Out (bl) Low	6	—	x ck	ns

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 2-16 SSI Timing (Continued)

Num	Characteristics	60 MHz		Case	Unit
		Min	Max		
156	SCK Rising Edge to SFS Out (wl) High	—	20.5	x ck	ns
157	SCK Rising Edge to SFS Out (wl) Low	—	35.0	x ck	ns
158	Data In Setup Time Before SCK Falling Edge	7	—	x ck	ns
159	Data In Hold Time After SCK Falling Edge	13.2	—	x ck	ns
160	SCK Rising Edge to SFS In (bl) High	—	26.1	x ck	ns
161	SCK Rising Edge to SFS In (bl) Low	—	13.0	x ck	ns
162	SCK Rising Edge to SFS In (wl) High	—	30	x ck	ns
163	SCK Rising Edge to Data Out Enable from High Impedance	—	7.5	x ck	ns
164	SCK Rising Edge to Data Out Valid	—	20.5	x ck	ns
165	SCK Rising Edge to Data Out Invalid	—	10.4	x ck	ns
166	SCK Rising Edge to Data Out High Impedance	—	19.7	x ck	ns
Note: 1. For internal clock, External Clock Cycle is defined by I_{cyc} and SSI Control Register.					

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

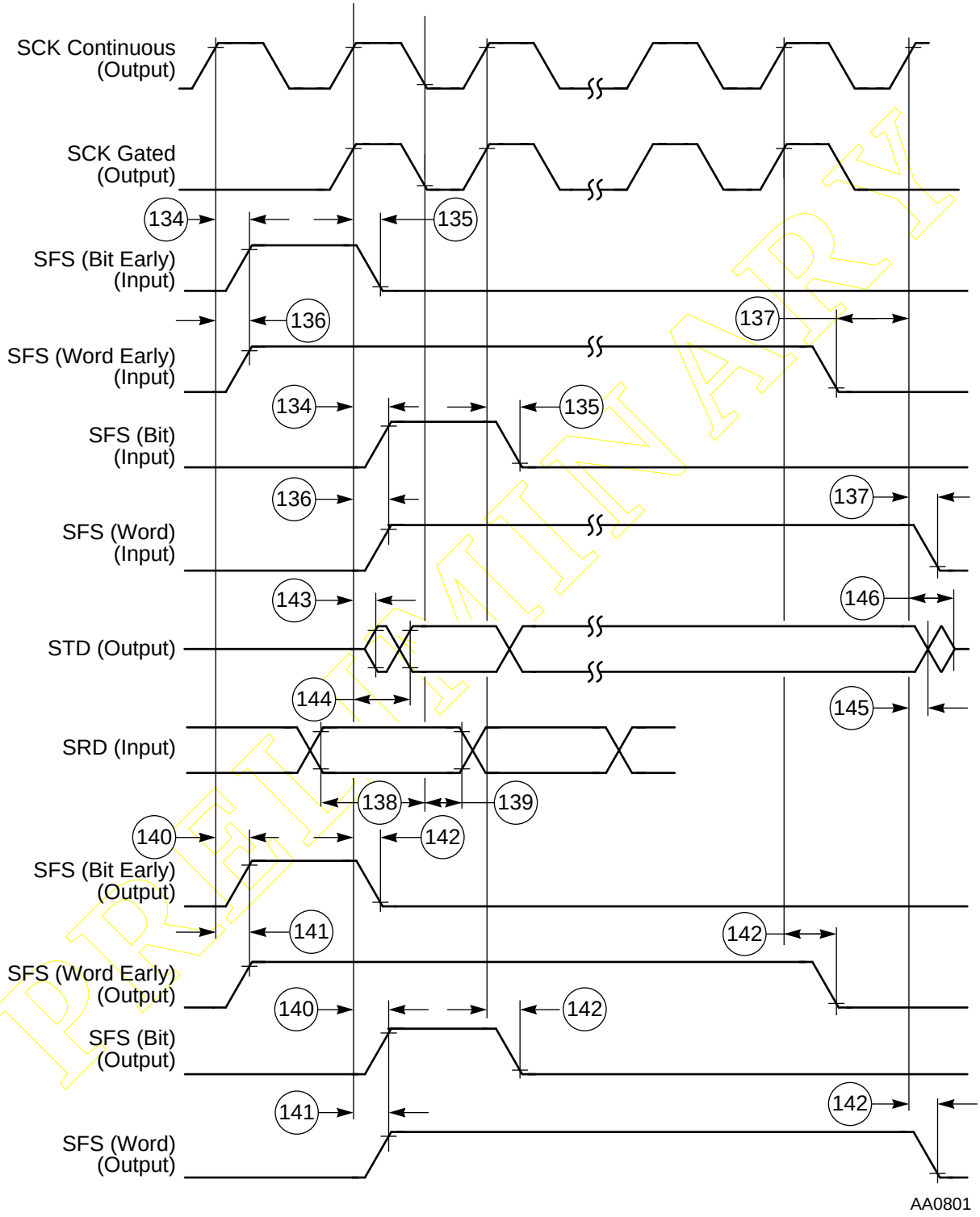


Figure 2-28 SSI Internal Clock Timing

Downloaded from Elcodis.com electronic components distributor

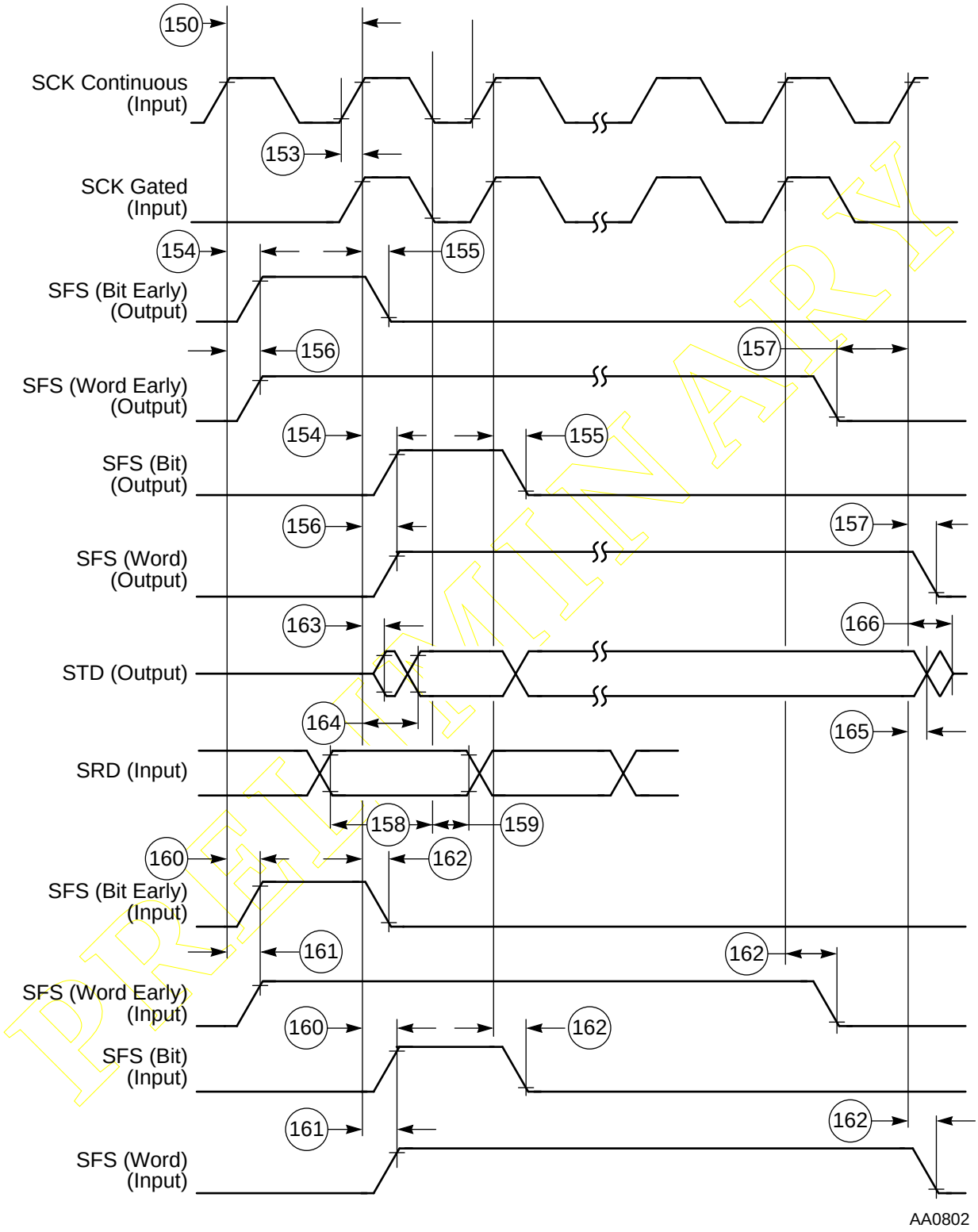


Figure 2-29 SSI External Clock Timing

Downloaded from Elcodis.com electronic components distributor

TIMER TIMING

V_{DD} = 5.0 V ± 10%; T_J = –40 to +115°C; C_L = 50 pF + 1 TTL load

Table 2-17 Timer Timing (60 MHz)

Num	Characteristics	Min	Max	Unit
170	TIN Valid to CLKO low (Setup time)	8	—	ns
171	CLKO Low to TIN Invalid (Hold time)	0	8.0	ns
172	CLKO High to TOUT Asserted	3.5	14.0	ns
173	CLKO High to TOUT Deasserted	0	—	ns
174	Tin Period	8T	—	ns
175	Tin High/Low Period	4T	—	ns

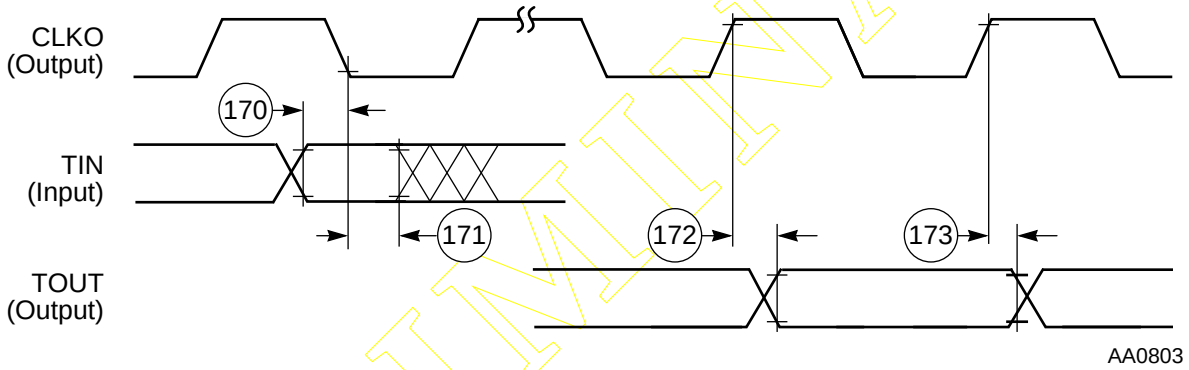


Figure 2-30 Timer Timing

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

GPIO TIMING

V_{DD} = 5.0 V ± 10%; T_J = –40 to +115˚C; C_L = 50 pF + 1 TTL load

Table 2-18 GPIO Timing

Num	Characteristics	Min	Max	Unit
201	CLKO edge to GPIO output valid (GPIO output delay time)	—	19.7	ns
202	CLKO edge to GPIO output not valid (GPIO output hold time)	0	—	ns
203	GPIO input valid to CLKO edge (GPIO input setup time)	10.0	—	ns
204	CLKO edge to GPIO input not valid (GPIO input hold time)	4.0	—	ns

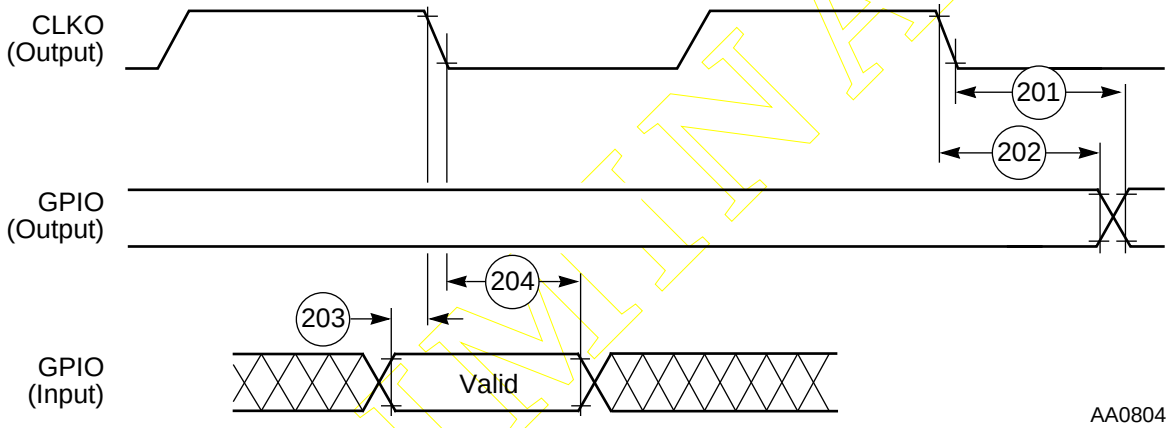


Figure 2-31 GPIO Timing

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

OnCE PORT TIMING

V_{DD} = 5.0 V ± 10%; T_J = –40 to +115°C; C_L = 50 pF + 1 TTL load

Table 2-19 OnCE Port Timing

Num	Characteristics	Min	Max	Unit
180	DSCK High to DSO Valid	—	27.6	ns
181	DSI valid to DSCK low (setup)	15	—	ns
182	DSCK low to DSI invalid (hold)	5	—	ns
183	DSCK high[1]	33	—	ns
184	DSCK low[1]	$2T_C$	—	ns
185	DSCK cycle time[1]	$4T_C$	—	ns
186	CLKO high to OS0–OS1 valid	—	14.5	ns
187	CLKO high to OS0–OS1 invalid	—	21.7	ns
188	Last DSCK high to OS0–OS1[2] Last DSCK high to $\overline{ACK}$ active (data)[2] Last DSCK high to $\overline{ACK}$ active (command)[2]	$10T + T_D + 14.5$ $10T + T_D + 13.5$ $21T + T_D + 13.5$	— — —	ns ns ns
190	DSO ($\overline{ACK}$) asserted to first DSCK high	$3T_C$	—	ns
191	DSO ($\overline{ACK}$) width asserted: a. when entering Debug mode b. when acknowledging command / data transfer	 34 51	 — —	 ns ns
192	Last DSCK low of read register to first DSCK high of next command	$6T_C$	—	ns
193	DSCK high to DSO invalid[2]	7	—	ns
194	$\overline{DR}$ asserted to DSO ($\overline{ACK}$) asserted	19.4	—	ns

Note: 1. 45–55% duty cycle
2. T_D = DSCK high (timing number 183)

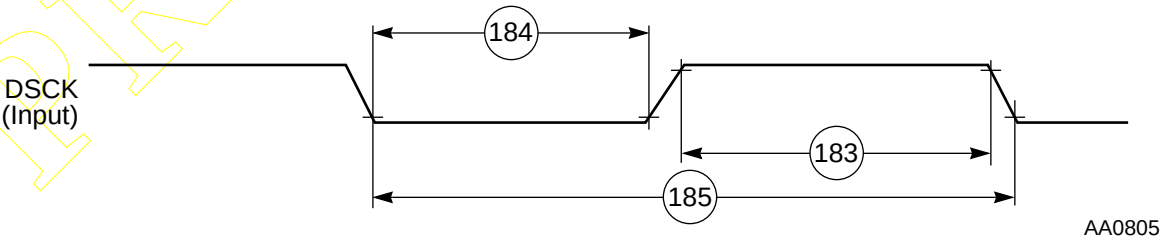


Figure 2-32 OnCE Serial Clock Timing

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

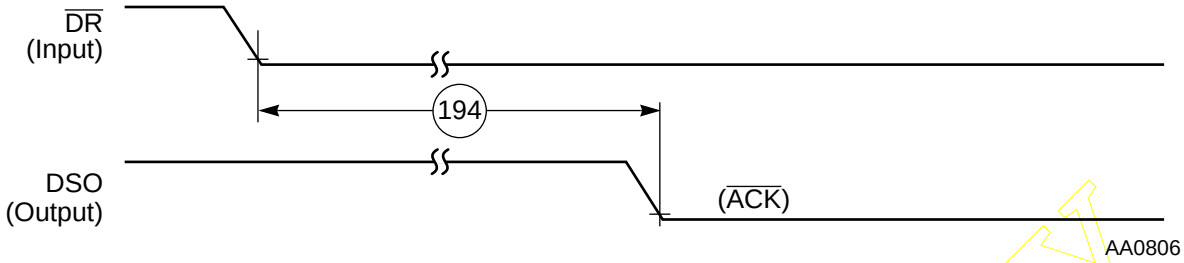
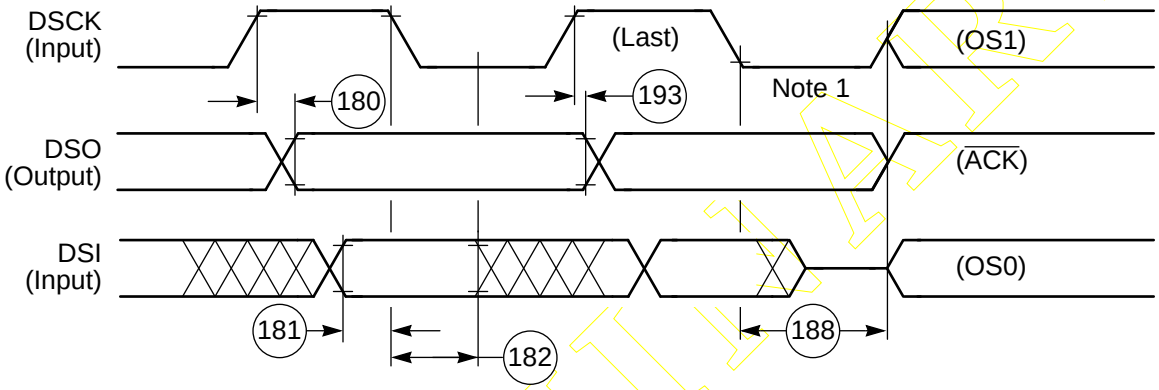
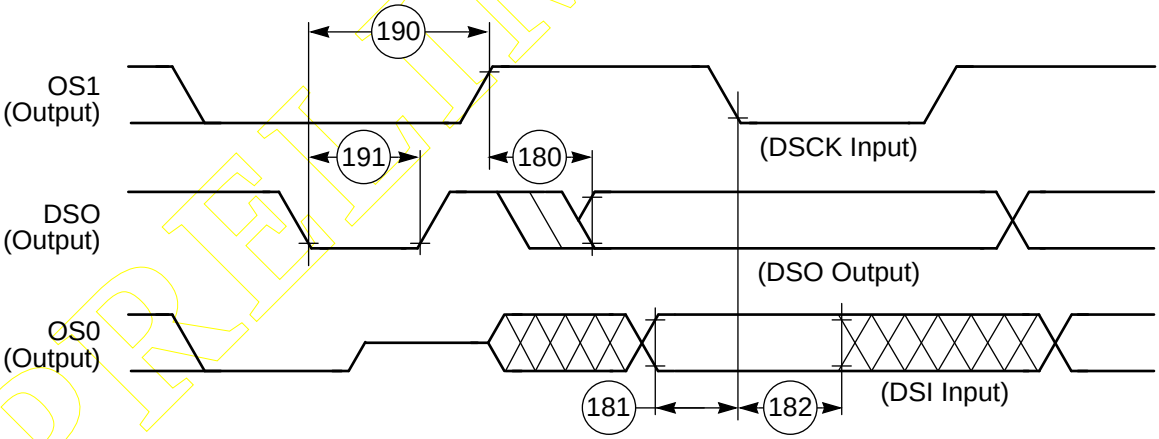


Figure 2-33 OnCE Acknowledge Timing



Note: 1. Tri-state, external pull-down resistor

Figure 2-34 OnCE Data I/O To Status Timing

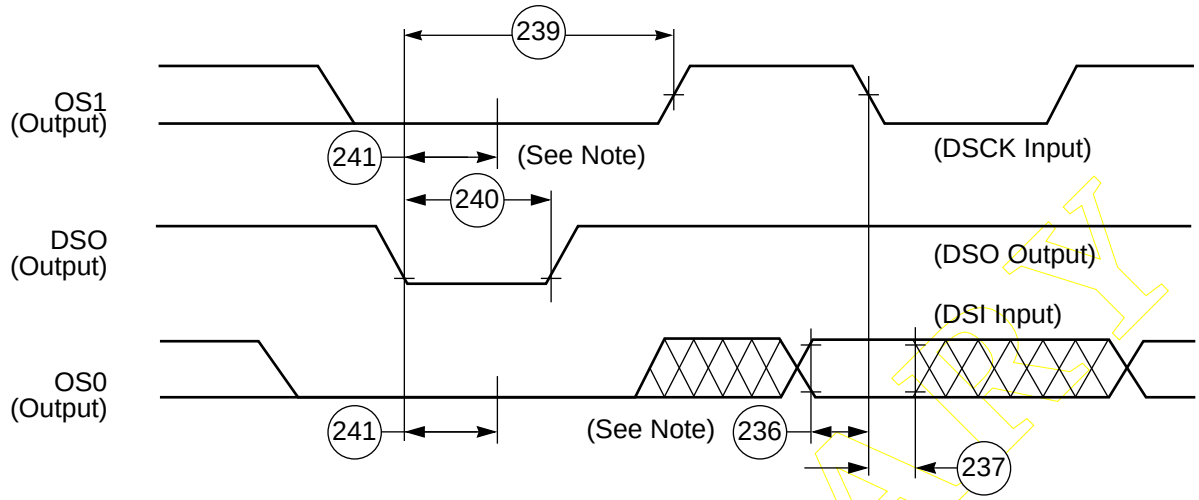


Note 1: Tri-stated, external pull-down resistor

Figure 2-35 OnCE Data I/O To Status Timing

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor



Note: High Impedance, external pull-down resistor

Figure 2-36 OnCE Data I/O To Status Timing

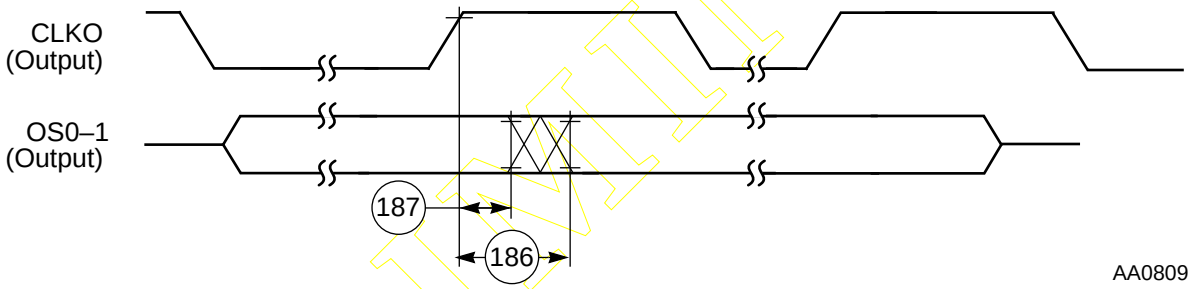


Figure 2-37 OnCE Clock to Status Timing

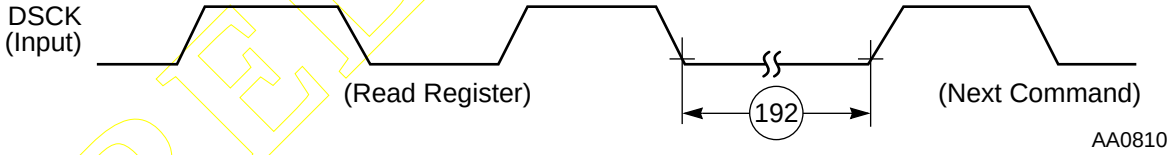


Figure 2-38 OnCE DSCK Next Command After Read Register Timing

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

SECTION 3

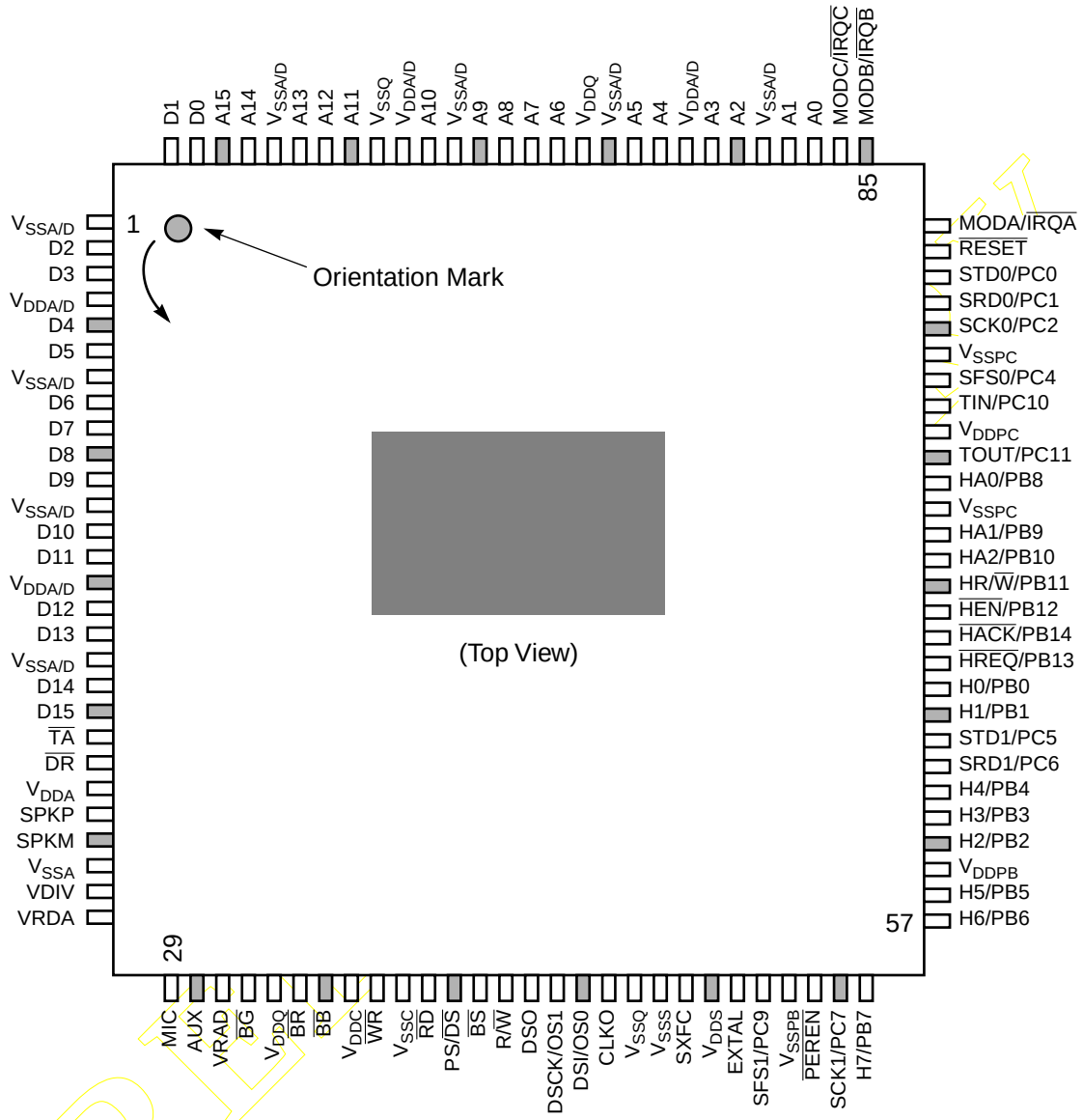
PACKAGING

PIN-OUT AND PACKAGE INFORMATION

Top and bottom views of the TQFP package are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

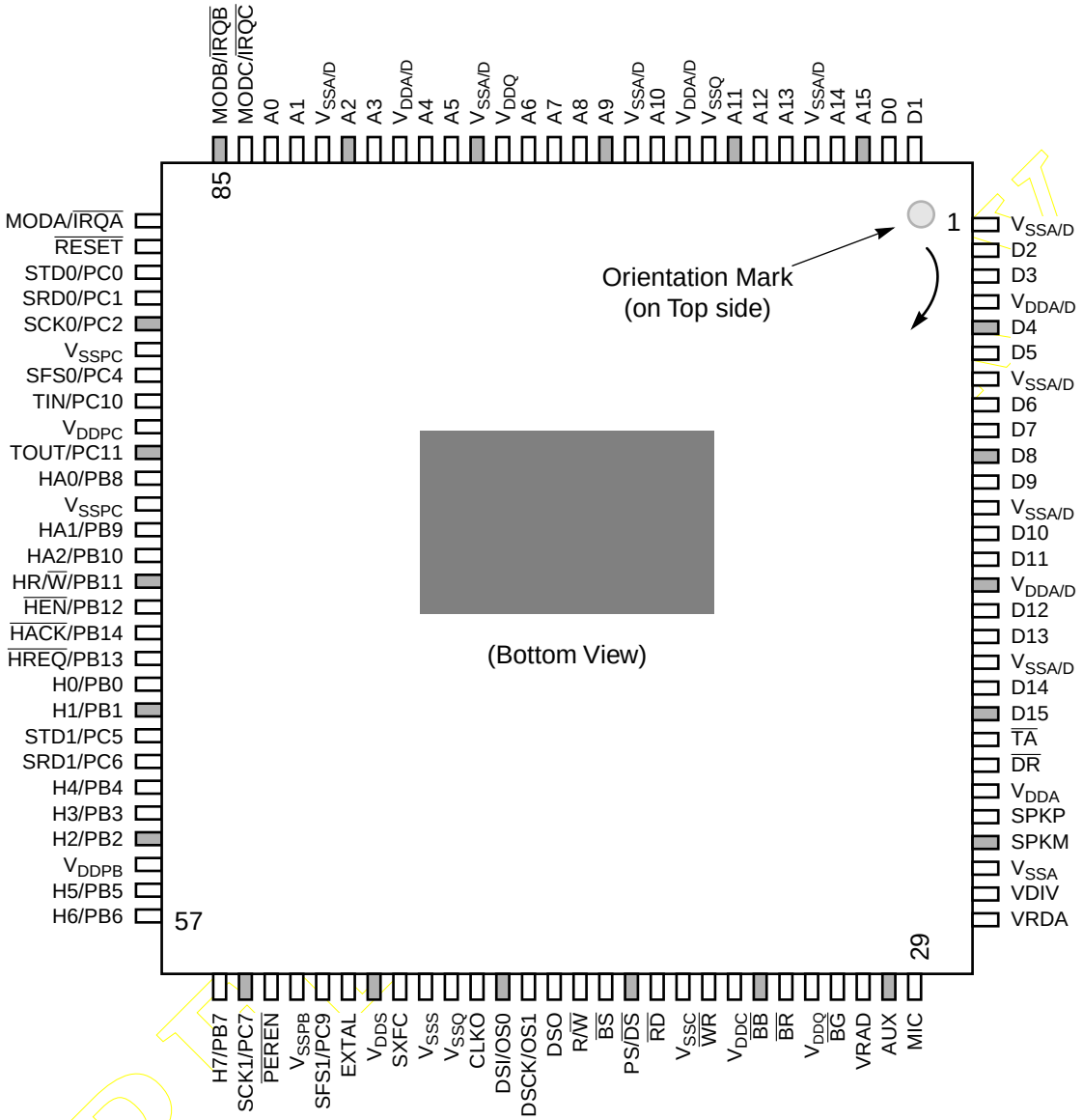


Note: An OVERBAR indicates the signal is asserted when the voltage = ground (active low).

AA0811

Figure 3-1 Top View of the 112-pin Plastic (FV) Thin Quad Flat Package

Downloaded from Elcodis.com electronic components distributor



Note: An OVERBAR indicates the signal is asserted when the voltage = ground (active low).

AA0812

Figure 3-2 Bottom View of the112-pin Plastic (FV) Thin Quad Flat Package

Downloaded from Elcodis.com electronic components distributor

The DSP56167 signals that may be programmed as General Purpose I/O are listed with their primary function in **Table 3-1**.

Table 3-1 DSP56167 General Purpose I/O Pin Identification

Pin Number	Primary Function	Port	GPIO ID
66	H0	B	PB0
65	H1		PB1
60	H2		PB2
61	H3		PB3
62	H4		PB4
58	H5		PB5
57	H6		PB6
56	H7		PB7
74	HA0		PB8
72	HA1		PB9
71	HA2		PB10
70	$\overline{\text{HR/W}}$		PB11
69	$\overline{\text{HEN}}$		PB12
67	$\overline{\text{HREQ}}$		PB13
68	$\overline{\text{HACK}}$		PB14
82	STD0	C	PC0
81	SRD0		PC1
80	SCK0		PC2
78	SFS0		PC4
64	STD1		PC5
63	SRD1		PC6
55	SCK1		PC7
52	SFS1		PC9
77	TIN		PC10
75	TOUT		PC11

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 3-2 DSP56167 Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	$V_{SSA/D}$	26	V_{SSA}	51	EXTAL
2	D2	27	VDIV	52	SFS1/PC9
3	D3	28	VRDA	53	V_{SSPB}
4	$V_{DDA/D}$	29	MIC	54	$\overline{\text{PEREN}}$
5	D4	30	AUX	55	SCK1/PC7
6	D5	31	VRAD	56	H7/PB7
7	$V_{SSA/D}$	32	$\overline{\text{BG}}$	57	H6/PB6
8	D6	33	V_{DDQ}	58	H5/PB5
9	D7	34	$\overline{\text{BR}}$	59	V_{DDPB}
10	D8	35	$\overline{\text{BB}}$	60	H2/PB2
11	D9	36	V_{DDC}	61	H3/PB3
12	$V_{SSA/D}$	37	$\overline{\text{WR}}$	62	H4/PB4
13	D10	38	V_{SSC}	63	SRD1/PC6
14	D11	39	$\overline{\text{RD}}$	64	STD1/PC5
15	$V_{DDA/D}$	40	PS/$\overline{\text{DS}}$	65	H1/PB1
16	D12	41	$\overline{\text{BS}}$	66	H0/PB0
17	D13	42	R/$\overline{\text{W}}$	67	$\overline{\text{HREQ}}$/PB13
18	$V_{SSA/D}$	43	DSO	68	$\overline{\text{HACK}}$/PB14
19	D14	44	DSCK/OS1	69	$\overline{\text{HEN}}$/PB12
20	D15	45	DSI/OS0	70	HR/$\overline{\text{W}}$/PB11
21	$\overline{\text{TA}}$	46	CLKO	71	HA2/PB10
22	$\overline{\text{DR}}$	47	V_{SSQ}	72	HA1/PB9
23	V_{DDA}	48	V_{SSS}	73	V_{SSPC}
24	SPKP	49	SXFC	74	HA0/PB8
25	SPKM	50	V_{DDS}	75	TOUT/PC11

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 3-2 DSP56167 Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
76	V_{DDPC}	89	$V_{SSA/D}$	102	A10
77	TIN / PC10	90	A2	103	$V_{DDA/D}$
78	SFS0 / PC4	91	A3	104	V_{SSQ}
79	V_{SSPC}	92	$V_{DDA/D}$	105	A11
80	SCK0 / PC2	93	A4	106	A12
81	SRD0 / PC1	94	A5	107	A13
82	STD0 / PC0	95	$V_{SSA/D}$	108	$V_{SSA/D}$
83	$\overline{\text{RESET}}$	96	V_{DDQ}	109	A14
84	MODA / $\overline{\text{IRQA}}$	97	A6	110	A15
85	MODB / $\overline{\text{IRQB}}$	98	A7	111	D0
86	MODC / $\overline{\text{IRQC}}$	99	A8	112	D1
87	A0	100	A9		
88	A1	101	$V_{SSA/D}$		

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

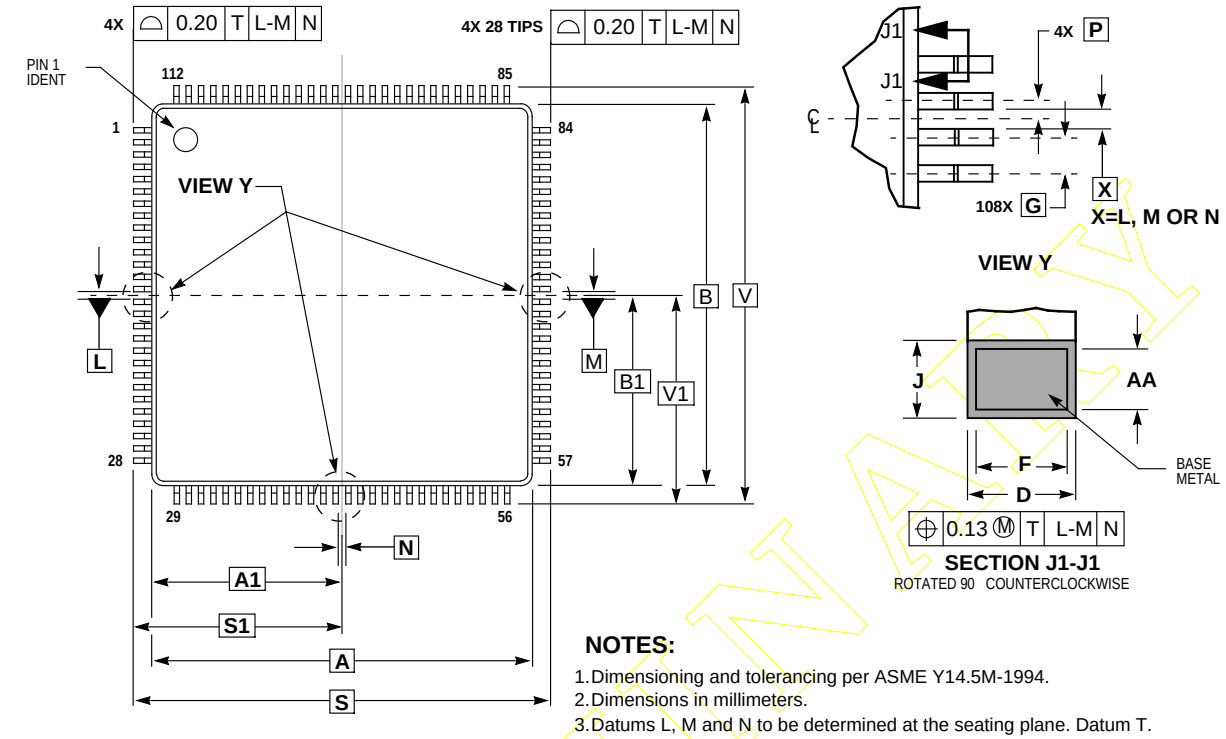
Power and ground pins have special considerations for noise immunity. See the section **Design Considerations**.

Table 3-3 DSP56167 Power Supply Pins

Pin Number	Power Supply	Circuit Supplied
23	V_{DDA}	Codec
26	V_{SSA}	
92	$V_{DDA/D}$	Address Bus Buffers
103		
89	$V_{SSA/D}$	
95		
101		
108		
4	$V_{DDA/D}$	Data Bus Buffers
15		
1	$V_{SSA/D}$	
7		
12		
18		
36	V_{DDC}	Bus Control Buffers
38	V_{SSC}	
59	V_{DDPB}	Port B/Host Interface Buffers
53	V_{SSPB}	
76	V_{DDPC}	Port C/SSI and Timer Buffers
73	V_{SSPC}	
79		
33	V_{DDQ}	Internal Logic
96		
47	V_{SSQ}	
104		
50	V_{DDS}	PLL and Clock
48	V_{SSS}	

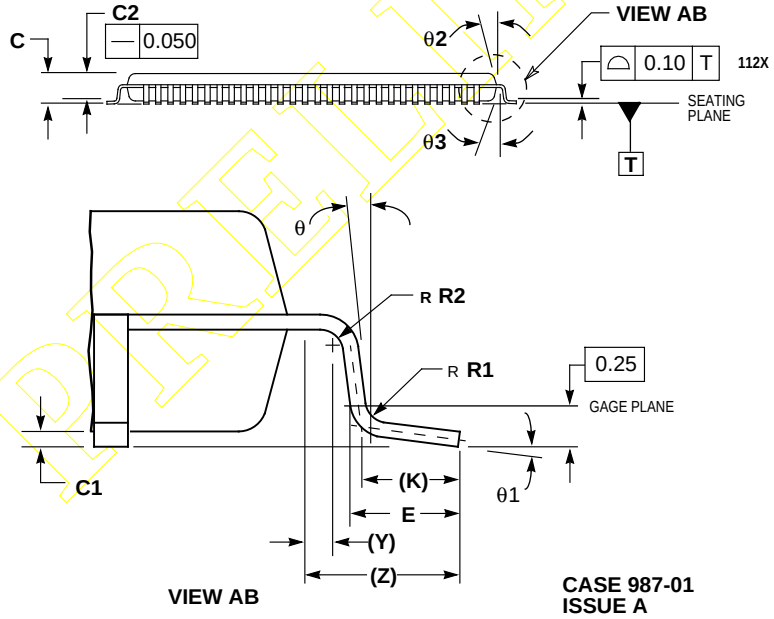
PRELIMINARY

Downloaded from Elcodis.com electronic components distributor



NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Datums L, M and N to be determined at the seating plane. Datum T.
4. Dimensions S and V to be determined at seating plane. Datum T.
5. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.25 per side. Dimensions A and B include mold mismatch.
6. Dimension D does not include dambar protrusion. Allowable dambar protrusion shall not cause the "D" dimension to exceed 0.46 .



CASE 987-01
ISSUE A

DIM	MILLIMETERS MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure 3-3 112-pin Thin Plastic Quad Flat Pack (TQFP) Mechanical Information

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

ORDERING DRAWINGS

Complete mechanical information regarding DSP56167 packaging is available by facsimile through Motorola's Mfax™ system. Call the following number to obtain information by facsimile:

(602) 244-6591

The Mfax automated system requests the following information:

- The receiving facsimile telephone number including area code or country code
- The caller's Personal Identification Number (PIN)

Note: For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.

- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific part technical information or data sheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

The DSP56167 112-pin TQFP package mechanical drawing is referenced as 987-01.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

SECTION 4

DESIGN CONSIDERATIONS

HEAT DISSIPATION

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature ˚C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance ˚C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance ˚C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or otherwise change the thermal dissipation capability of the area surrounding the device on a printed circuit board. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the printed circuit board, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

The thermal performance of plastic packages is more dependent on the temperature of the Printed Circuit Board (PCB) to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T) / P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, Thermal Characterization Parameter or Ψ_{JT}, has been defined to be $(T_J - T_T) / P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface, and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

Note: **Table 2-2 Recommended Operating Conditions** on page 2-2 contains the package thermal values for this chip.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

ELECTRICAL DESIGN CONSIDERATIONS

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the DSP.
- Provide a low-impedance path from the board ground to each V_{SS} pin.
- Use at least six 0.01–0.1 µF bypass capacitors, positioned as close as possible to the four sides of the package, to connect between the V_{DD} power source and V_{SS}. Refer to the following section **Analog I/O Considerations** for special requirements for the codec circuitry.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V_{DD} and V_{SS}. Refer to the following section **Analog I/O Considerations** for special requirements for the codec circuitry.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be less than 6 inches maximum. This recommendation particularly applies to the address and data buses, as well as the PS/$\overline{DS}$, $\overline{BS}$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, $\overline{PEREN}$, $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{HEN}$, HR/$\overline{W}$, and $\overline{HACK}$ pins.
- When calculating capacitance, consider all device loads including parasitic capacitance due to PCB traces,. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

- If possible, do not have digital signals running over the analog V_{DD} and ground planes. Decouple analog V_{DD} and ground planes as close as possible to the DSP.
- Do not route clock signal lines across multiple signal lines. Keep the clock signals away from the analog power and ground lines and all analog signal lines.
- Take special care to minimize noise levels on the PLL supply pins (both V_{DD} and V_{SS}).

ANALOG I/O CONSIDERATIONS

This section discusses the requirements of the on-chip codec. The two analog inputs (MIC and AUX) are electrically identical. When one is not used, it can be left floating. When an input is used, an AC coupling capacitor is required. The value of the capacitor combines with the input impedance of MIC or AUX to determine the cutoff frequency of a high pass filter. The input impedance of MIC and AUX varies with respect to the Microphone Gain Select value (MGS[1:0]). An AC coupling capacitor of 10 µF defines a high pass filter pole of 3 Hz. A smaller capacitor value moves this pole higher in frequency.

Figure 4-1 shows the recommended analog I/O and power supply configurations.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

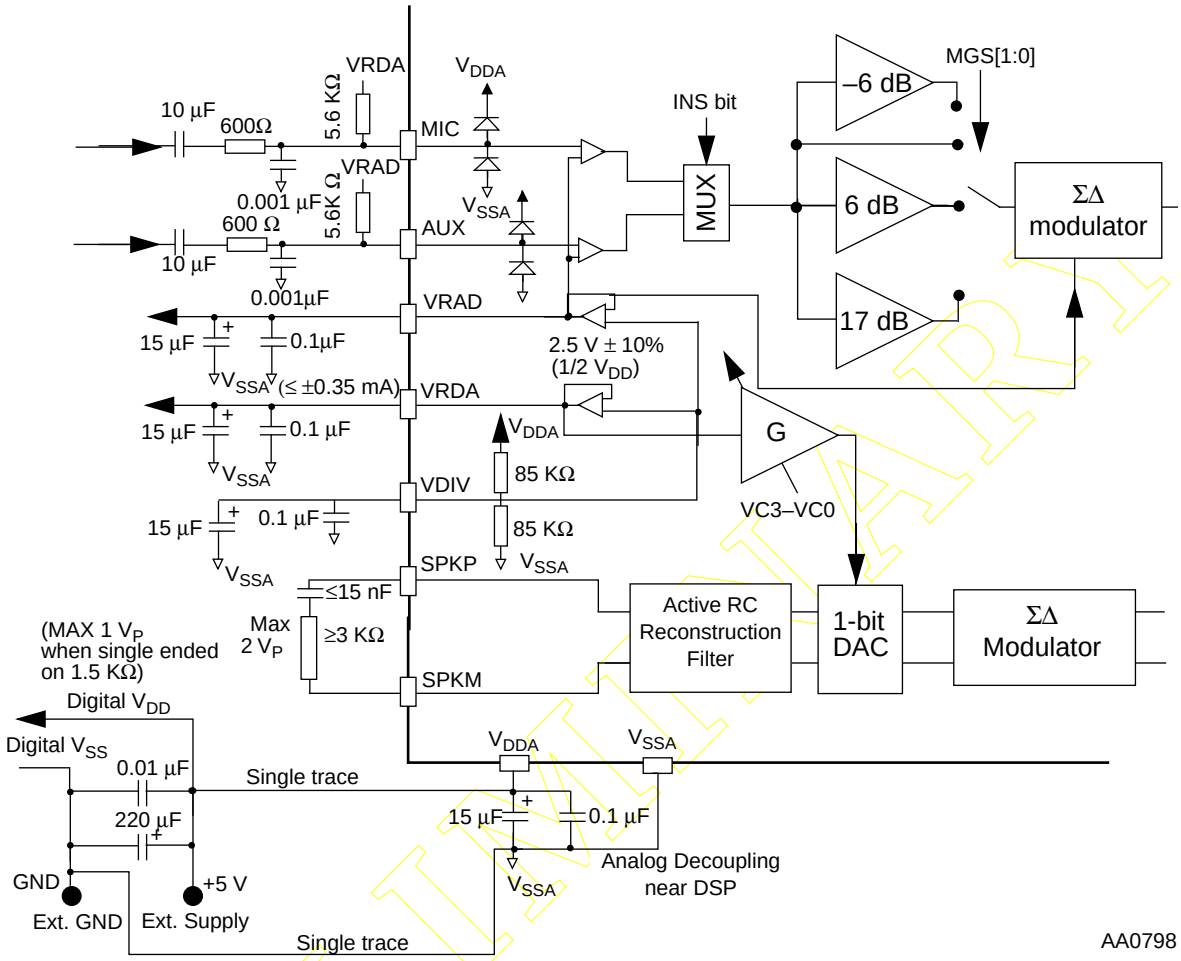


Figure 4-1 Recommended Analog I/O Configuration

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Figure 4-2 shows three possible output configurations. Configuration A is highly recommended, because the termination impedance between SPKP and SPKM is matched. Configurations B and C require an AC coupling capacitor because the load resistor is tied to V_{SSA}.

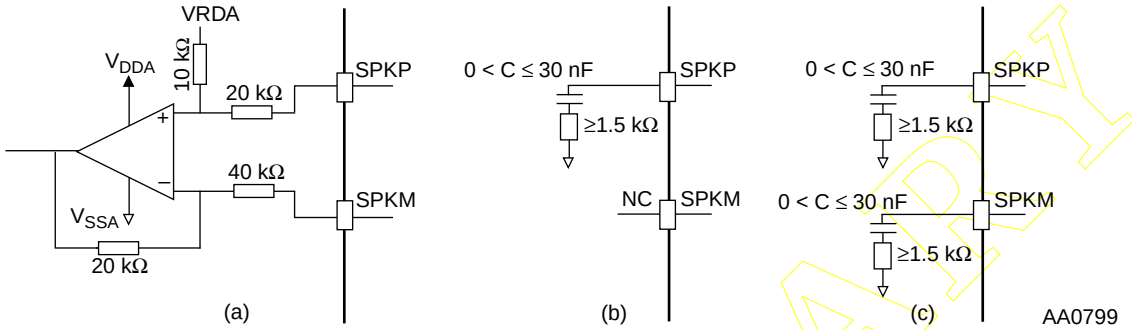


Figure 4-2 Codec Output Configurations

Figure 4-3 shows a recommended layout for power and ground planes. A four-layer board is recommended. The top layer (directly under the parts) and the bottom layers should be interconnected layers. The two center layers should be power and ground. Ground and power planes should be completely separated, and the digital and analog power / ground planes should not overlap. All codec pins and all codec signal traces should be over the analog planes. The analog planes should not encompass any digital pins.

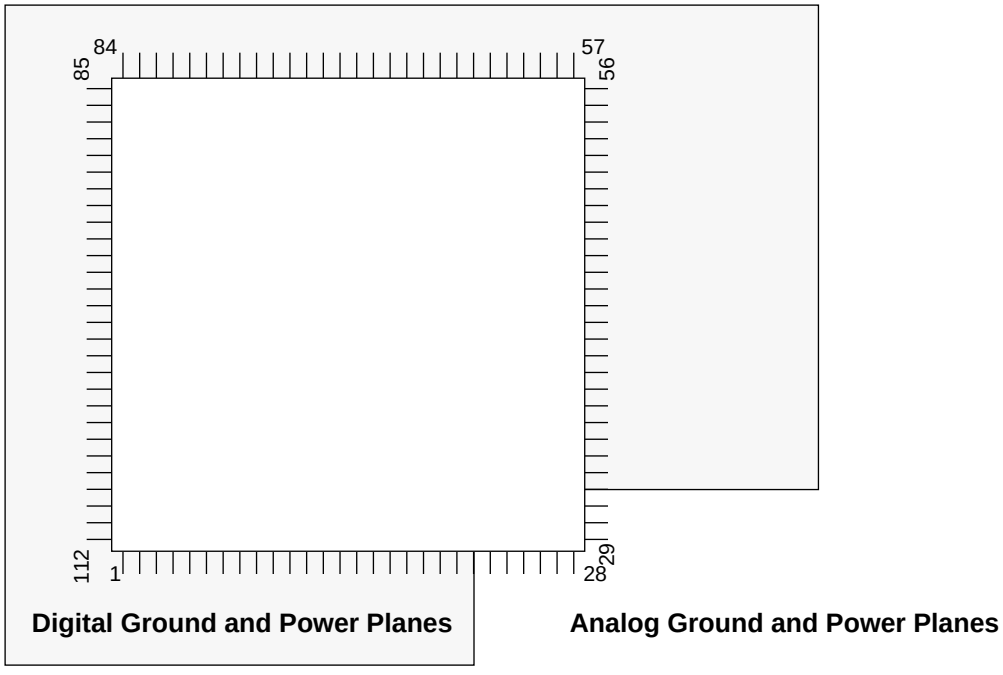


Figure 4-3 Recommended Ground and Power Plane Layout

Downloaded from Elcodis.com electronic components distributor

Figure 4-4 shows that 0.1 µF bypass capacitors should be located as close to the pins being bypassed as possible. Connect the ground side of the bypass capacitors to V_{SSA} by short traces.

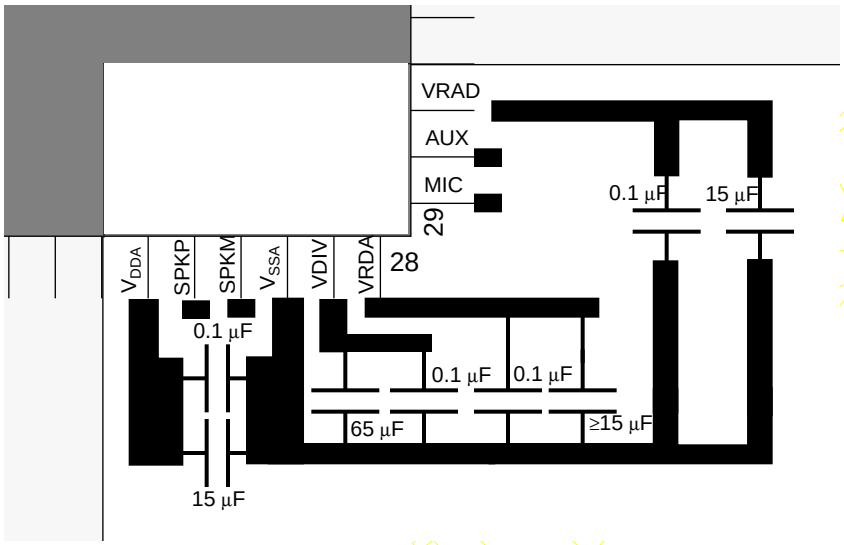


Figure 4-4 Suggested Top Layer Bypassing

The pins requiring 0.1 µF bypass capacitors are VRDA, VRAD, and V_{DDA}. These pins and the VDIV pin should have bypass capacitors of the largest size practical; 10 µF should be considered a minimum size for the larger capacitors (65 µF may be used on VDIV). The capacitors should be placed near the package, but do not have to be immediately next to the pins. As shown in **Figure 4-5** on page 4-8, run the DAC outputs (SPKP and SPKM) next to each other.

If possible, use the output differentially. Shield analog signal traces by running traces connected to the analog ground next to them. All unused board area (on both interconnect levels) should be copper-filled and connected to analog ground. For clarity and simplicity, copper fill is indicated by text, but not shown in. The ADC input anti-aliasing filtering should be done with respect to VRAD.

Figure 4-6 on page 4-9 shows four examples of good power supply connections.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

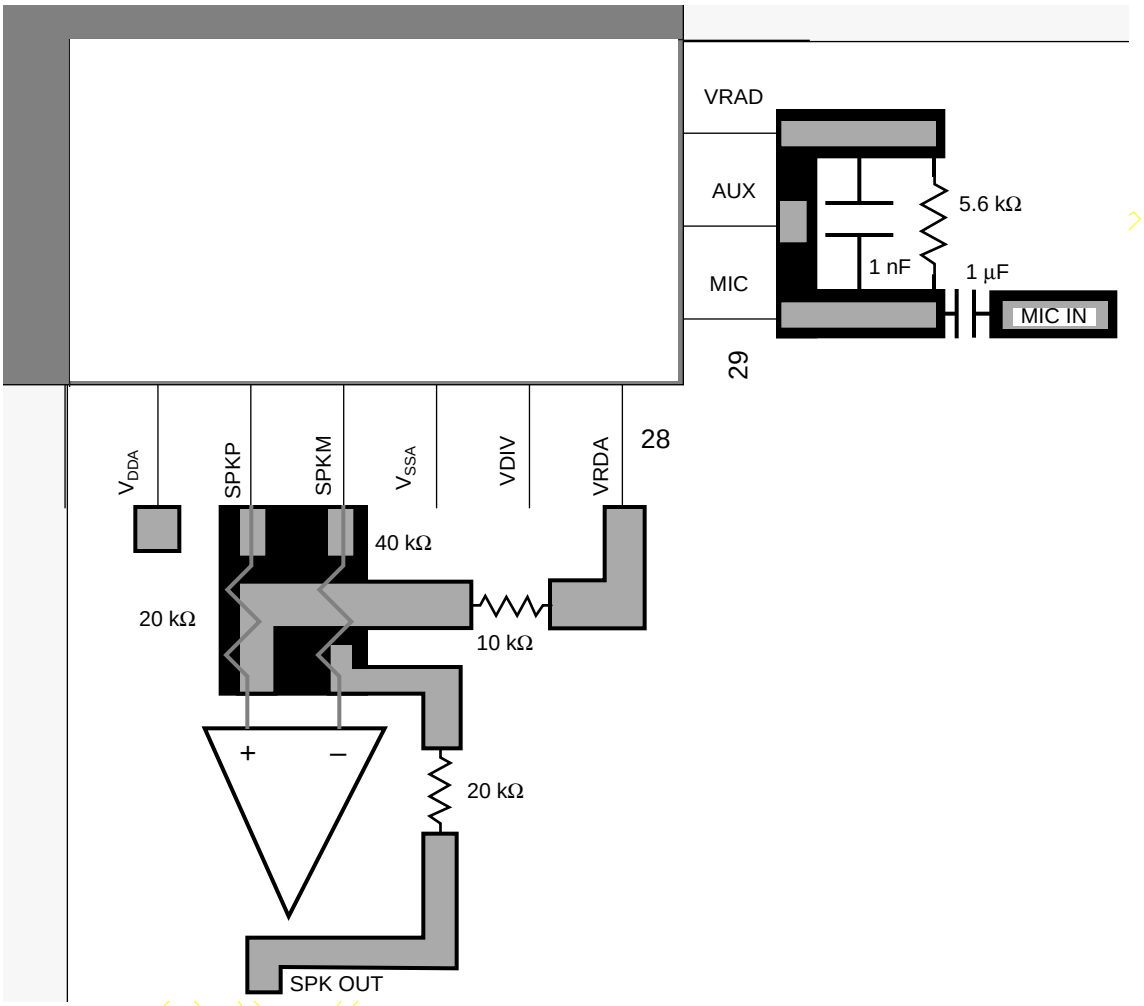


Figure 4-5 Suggested Bottom Layer Routing

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

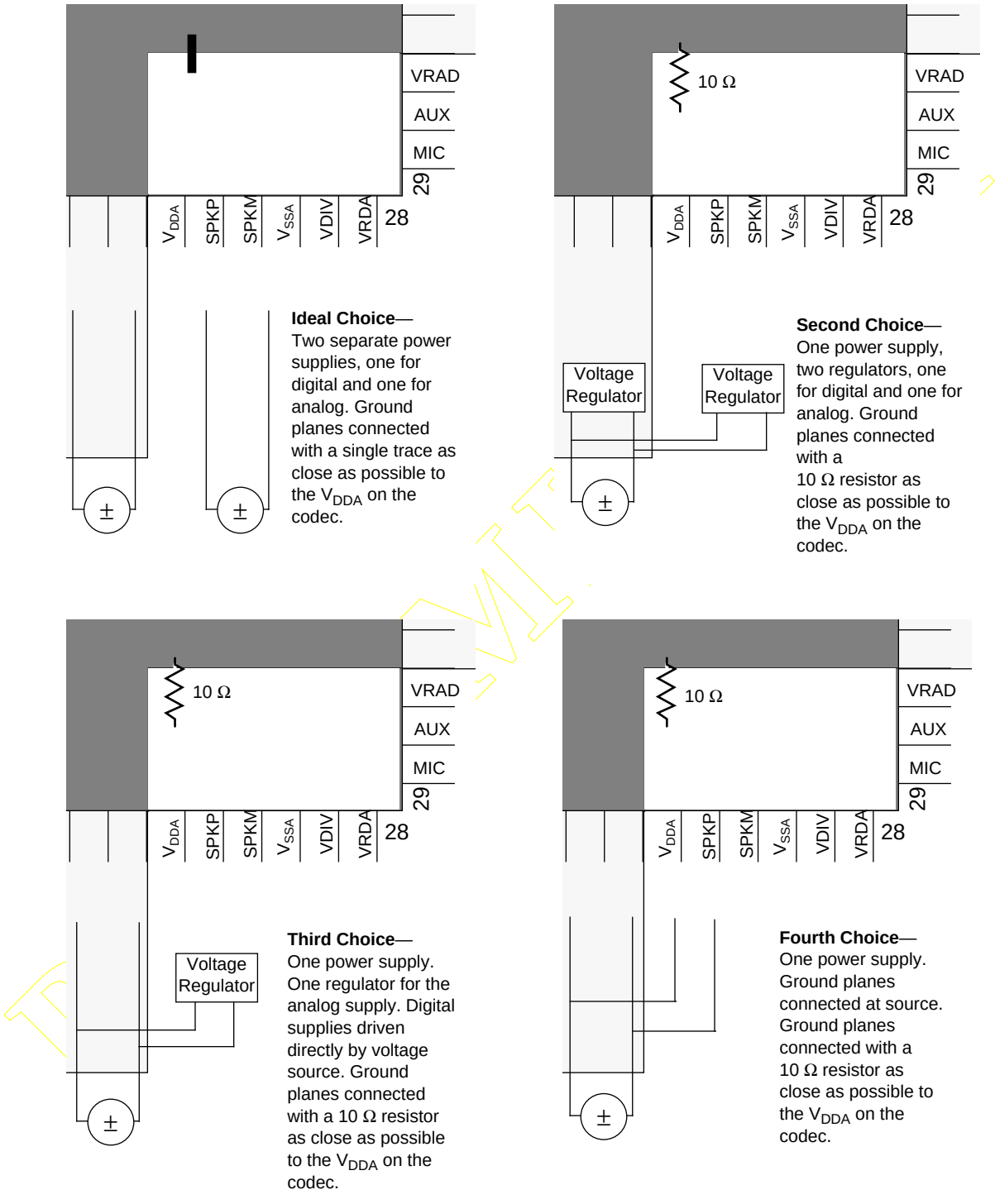


Figure 4-6 Four Possible Power Supply Connections

Downloaded from Elcodis.com electronic components distributor

POWER CONSUMPTION

Power dissipation is a key issue in portable DSP applications. The following describes some factors which affect current consumption. Current consumption is described by the formula:

Equation 3: $I = C \times V \times f$

where: I = current in A
C = node / pin capacitance in F
V = voltage swing in V
f = frequency of node / pin toggle (in Hz)

For example, for an address pin loaded with a 50 pF capacitance and operating at 5.5 V with a 60 MHz clock, toggling at its maximum possible rate (which is 15 MHz), the current consumption is:

Equation 4: $I = 50 \times 10^{-12} \times 5.5 \times 15 \times 10^{6} = 4.125\text{mA}$

The maximum internal current value (I_{CCI}-max), reflects the maximum I_{CC} expected when running a test code. This represents "typical" internal activity, and is included as a point of reference. Some applications may consume more or less current depending on the code used. The typical internal current value (I_{CCI}-typ) reflects what is typically seen when running the given code.

The following steps are recommended for applications requiring very low current consumption:

1. Minimize external memory accesses; use internal memory accesses instead.
2. Minimize the number of pins that are switching.
3. Minimize the capacitive load on the pins.
4. Connect unused digital inputs to V_{DD} or V_{SS}. Connect unused I / O pins through 10 kΩ resistors to V_{DD} or V_{SS}.
5. All Port A input pins and bidirectional pins must have a valid state at all times when Port A is released to minimize power consumption; therefore the pins must be pulled up or down or driven by another device.
6. When the codec is not used, connect V_{DDA} to V_{DD} and V_{SSA} to V_{SS} and decouple VRAD and VARD. Leave all other codec pins floating.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

PLL USAGE CONSIDERATIONS

The PLL can be used to generate the DSP core system clock. The specific operating frequency is determined by choosing the appropriate input frequency (EXTAL) and the ID, YD, and PD counter divider ratios. These ratios are defined in the PLL Control Register 0 (PCR0), using the following formula:

$$Fosc = \frac{YD + 1}{(ID + 1) \times 2^{PD}} \times EXTAL$$

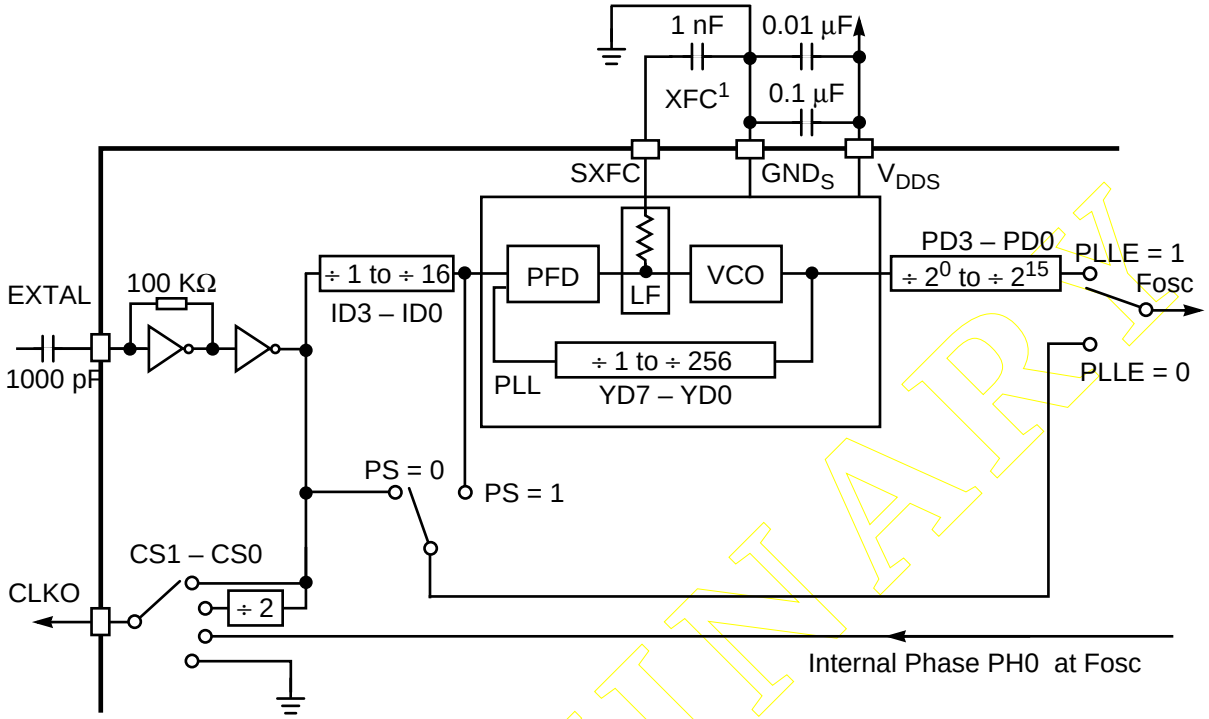
The best PLL performance is attained when the ID and YD counter values are kept in a small range to minimize lock time and jitter. A higher input frequency to the PLL will result in a higher correction rate, therefore producing a more stable output clock. For example, with an input EXTAL frequency of 10 MHz, a PLCR0 value of $0317 will result in a more stable 60 MHz system clock than will a PLCR0 value of $0F5F. A programming ratio of EXTAL / (ID + 1) ≥ 1 MHz is recommended.

The External Filter Capacitor (XFC) is another parameter affecting lock time and stability of the PLL system. This low-leakage capacitor should be connected between SXFC and GND_S, as close as possible to the pins. The PLL pins (VDDS, GNDS, and SXFC) should be isolated, as much as possible, from any external noise, preferably in a separate ground plane. The PLL modifies the voltage on the VCO by varying the charge on the capacitor connected to XFC. In effect, the PLL can be viewed as a second-order control system in which the SFC influences the natural frequency and damping factor for the system. If the capacitor is too small, the system will be severely underdamped and unstable, which yields a large jitter. If the capacitor is too large, the PLL becomes overdamped and may not be able to adjust to voltage changes within a reasonable lock time. The PLL lock detection circuitry does not require the system to be underdamped.

A recommended connection diagram is shown in **Figure 4-7** on page 4-12.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor



Note: 1. Must be a low leakage capacitor and must be located very close to the SXFC and VDDS pins.

AA0773

Figure 4-7 Connecting EXTAL and the External Filter Capacitor

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

HOST PORT USAGE CONSIDERATIONS

Careful synchronization is required when reading multibit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected. The situation exists in the Host port. The considerations for proper operation are discussed below.

Host Programmer Considerations

- **Unsynchronized Reading of Receive Byte Registers—**When reading receive byte registers, RXH or RXL, the host programmer should use interrupts or poll the RXDF flag which indicates that data is available. This assures that the data in the receive byte registers will be stable.
- **Overwriting Transmit Byte Registers—**The host programmer should not write to the transmit byte registers, TXH or TXL, unless the TXDE bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers will transfer valid data to the HRX register.
- **Synchronization of Status Bits from DSP to Host—**HC, HREQ, DMA, HF3, HF2, TRDY, TXDE, and RXDF (refer to *DSP56167 User's Manual*, I/O Interface section, Host/DMA Interface Programming Model for descriptions) status bits are set or cleared from inside the DSP and read by the host processor. The Host can read these status bits very quickly without regard to the clock rate used by the DSP, but the possibility exists that the state of the bit could be changing during the read operation. This is generally not a system problem, since the bit will be read correctly in the next pass of any Host polling routine.

  However, if the Host asserts the HEN for more than timing number 101 (T101), with a minimum cycle time of timing number 103 (T103), then the status is guaranteed to be stable.

Note: A potential problem exists when reading status bits HF3 and HF2 as an encoded pair. If the DSP changes HF3 and HF2 from 00 to 11, there is a small probability that the Host could read the bits during the transition and receive 01 or 10 instead of 11. If the combination of HF3 and HF2 has significance, the Host could read the wrong combination.

Solution:
a. Read the bits twice and check for consensus.
b. Assert $\overline{\text{HEN}}$ access for T101a so that status bit transitions are stabilized.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

- **Overwriting the Host Vector—**The host programmer should change the Host Vector register only when the Host Command bit (HC) is clear. This change will guarantee that the DSP interrupt control logic will receive a stable vector.
- **Cancelling a Pending Host Command Exception**—The host processor may elect to clear the HC bit to cancel the Host Command Exception request at any time before it is recognized by the DSP. Because the Host does not know exactly when the exception will be recognized (due to exception processing synchronization and pipeline delays), the DSP may execute the Host exception after the HC bit is cleared. For these reasons, the HV bits must not be changed at the same time the HC bit is cleared.

DSP Programmer Considerations

When reading HF0 and HF1 as an Encoded Pair, the DMA, HF1, HF0, and HCP, HTDE, and HRDF (refer to *DSP56167 User's Manual*, I/O Interface section, Host/DMA Interface Programming Model for descriptions) status bits are set or cleared by the host processor side of the interface. These bits are individually synchronized to the DSP clock.

Note: A potential problem exists when reading status bits HF1 and HF2 as an encoded pair, (i.e., the four combinations 00, 01, 10, and 11 each have significance). A very small probability exists that the DSP will read the status bits synchronized during transition. The solution to this potential problem is to read the bits twice for consensus.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

SPECIAL DESIGN CONSIDERATIONS FOR CONVERSIONS FROM DSP56166 TO DSP56167

There are several areas to consider when converting a design using a DSP56166 to a design using the DSP56167. Although the DSP56167 is software and pin compatible with the DSP56166, some external component changes are required. Not only have additional features been added in the DSP56167, but there are also changes to existing circuitry that affect DSP operation and circuit design. In addition, several errata in the DSP56166 have been fixed in the DSP56167. The following sections provide detailed information about these design changes.

Note: All references to RSSI are now listed as SSI.

New Feature Descriptions

New features added to the DSP56167 include:

- Programmable absolute short addressing mode (PASAM)
- Peripheral Address Generation Unit (PAGU)
- Independent external chip enable signals $\overline{BR}$ and $\overline{PEREN}$
- Port A BG pull-down under software control
- Port A and OnCE port $\overline{DR}$ signal line keepers with reset
- External program memory access disable

The following sections provide a detailed description of these new features and provide guidelines for use in applications.

PROGRAMMABLE ABSOLUTE SHORT ADDRESSING MODE (PASAM)

Previously on the DSP56166, the absolute short addressing mode allowed the user to access the first 32 locations, from X:$0000 throughX:$001F, of the data memory space using a one word move or bitfield instruction. This feature has been enhanced to allow the user to access any 32 locations within the data memory space, from X:$0000 to X:$FFFF. The block of 32 locations or page of the data memory space is selected by programming the upper 11 bits of the Address ALU Programmable Absolute Short Addressing Mode register (PASAM —X:$FFCA), wait one instruction cycle due to the pipeline delay, and then access the new page using the same absolute short addressing mode instruction. **Figure 4-8** on page 4-16 shows the PASAM architecture.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

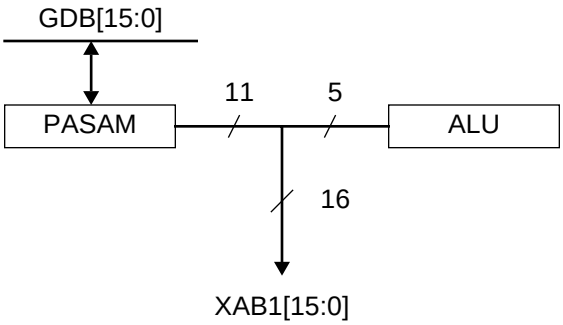


Figure 4-8 Programmable Absolute Short Addressing Mode Architecture

Note: The lower 5 bits of the PASAM register are reserved bits and should be written with zeros for future compatibility. They are read as zeros whenever PASAM is read.

The changes affect the following instructions:

```
move(s)    X:<aa>,D
move(s)    S,X:<aa>
bftst/bfset/bfchg/bfclr#iiii,X:<aa>
```

PASAM Register

The register defined in **Figure 4-9** has been added to the DSP56100 core to allow implementation of this function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
p	p	p	p	p	p	p	p	p	p	p	*	*	*	*	*

Where:

p programmable bits; preset to 0 during processor reset
* reserved bits; write 0 for future compatibility

X:$FFCA

Figure 4-9 Programmable Absolute Short Addressing Mode Register (PASAM)

Using PASAM

To use this function, write the starting address of the selected block into the Programmable Absolute Short Addressing Mode (PASAM) register to point to the desired block or page. You can access the selected block at any time.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

PERIPHERAL ADDRESS GENERATION UNIT (PAGU)

A Peripheral Address Generation Unit (PAGU) has been added to the DSP56167. The PAGU allows the DSP to generate external peripheral addresses. To support this function, some control bits have been added to DSP56100 core registers and a number of new core registers and functional units have been added.

Core changes to support the PAGU include:

- **Defined Interrupt Priority Register (IPR2) bits 1 and 0**—this is the DSP second X memory mapped interrupt priority register at address X:$FFDD.
- **New Registers**—These registers and pointers are used as matched pairs (i.e., PAGUR0 is used with PAGUC0):
  - Peripheral Address Generation Unit Registers (pointers) 0–2 (PAGUR0–PAGUR2]
  - Peripheral Address Generation Unit Compare registers 0–2 (PAGUC0–PAGUC2]
- **New Units—**There are two new processing units:
  - Post Update Address Generation Unit (PUAGU) supports three post-update modes:
    - No Update [(Rn)],
    - Post-increment [(Rn)+], and
    - Post-decrement [(Rn)–]
  - Comparator—Address Comparator and Interrupt Control Unit.
- **New Interrupt Vectors**—There are 3 separate interrupt vectors, one for each Peripheral Address Compare Register, located at addresses P:$0030, P:$0032 and P:$0034, respectively.

The interrupt feature of the PAGU can be enabled by programming the two interrupt enable / priority encoding bits in the IPR2 register. The PAGU interrupt can also be de-asserted if the Peripheral Enable (PE) bit 9 of the Operating Mode Register (OMR), (i.e., the PAGU is disabled). Since the hardware reset clears PE, it also deasserts the PAGU interrupt request.

Once the PAGU is enabled, every time a post update operation occurs, the post updated address will be compared against the value in the corresponding PAC register. When the two values matched, an interrupt request signal will be asserted. When the DSP core recognizes the PAGU interrupt, the interrupt vector corresponding to the updated Peripheral Address Pointer is taken. Its corresponding interrupt request signal is cleared as the interrupt is being serviced. If the Peripheral Address Pointer and / or the PAC register pair values are changed before the corresponding interrupt is serviced, the interrupt will remain pending.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Note: The PAGUC0 compare interrupt has precedence over the PAGUC1 compare interrupt, and the PAGUC1 compare interrupt has precedence over the PAGUC2 compare interrupt.

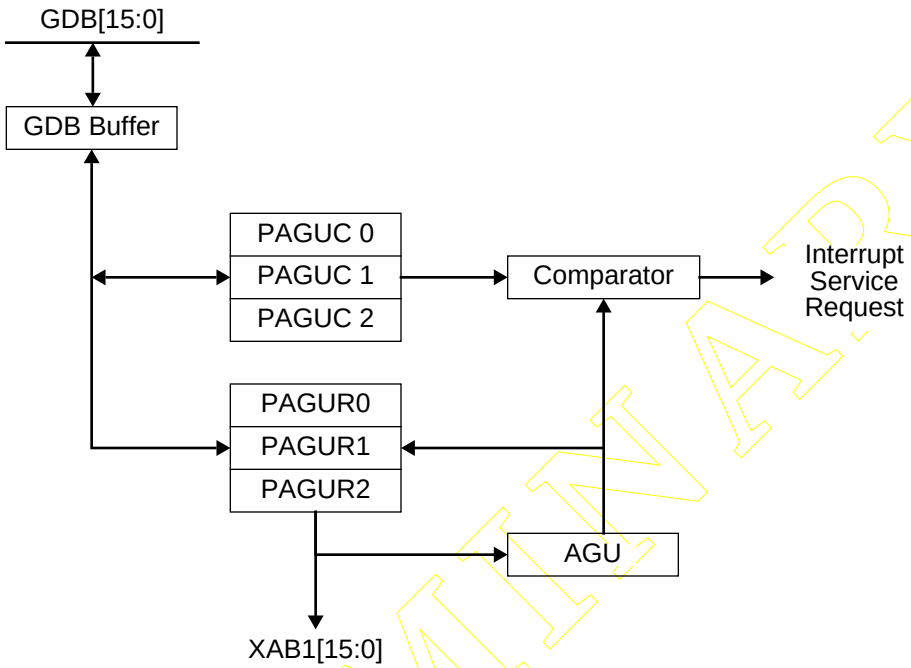


Figure 4-10 PAGU With Address Compare Interrupt Architecture

PAGU Programming Environment

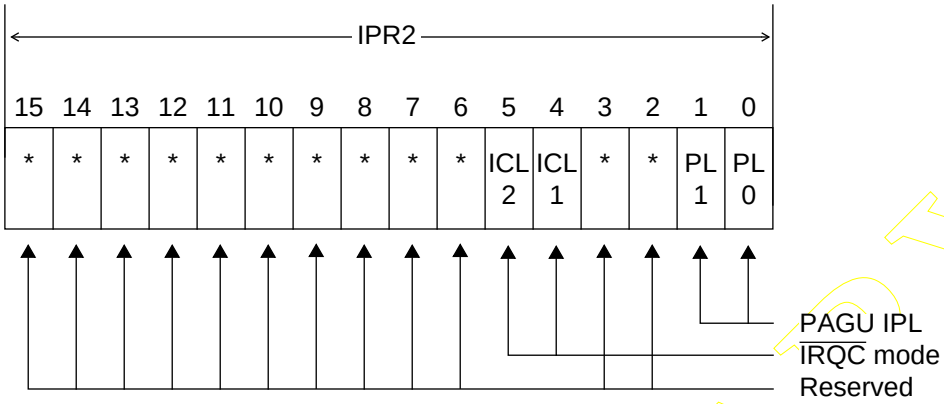
The following tables and figures describe the PAGU programming environment.

Table 4-1 PAGU X Memory-Mapped Registers

PAGU Register	X Memory Mapped Address
PAGUR0	X:$FFD7
PAGUR1	X:$FFD6
PAGUR2	X:$FFD5
PAGUC0	X:$FFCF
PAGUC1	X:$FFCE
PAGUC2	X:$FFCD

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor



Note: IPR2 is reset to zero

Figure 4-11 Interrupt Priority Register IPR2 (X:$FFDD)

Table 4-2 Interrupt Priority Level

PL1	PL0	Enabled	IPL
0	0	No	-
0	1	Yes	0
1	0	Yes	1
1	1	Yes	2

Table 4-3 PAGU Interrupt Vectors

PAGU Interrupt	Interrupt Vector Address
PAGUC0 Compare Interrupt	P:$0030
PAGUC1 Compare Interrupt	P:$0032
PAGUC2 Compare Interrupt	P:$0034

Table 4-4 Level 3 Non-maskable Interrupts

Priority	Exception	Enabled By	IP Reg. Bit No.	Control Register Address
Highest	Hardware RESET	—	—	—
	Illegal Instruction	—	—	—
	Stack Error	—	—	—
Lowest	SWI	—	—	—

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 4-5 Level 0, 1, 2 Maskable Interrupts

Priority	Exception	Enabled By	IP Reg. Bit No.	Control Register Address
Highest	IRQA (External Interrupt)	IRQA mode bit	0,1	X:$FFDF
	$\overline{\text{IRQB}}$ (External Interrupt)	$\overline{\text{IRQB}}$ mode bit	3,4	X:$FFDF
	$\overline{\text{IRQC}}$ (External Interrupt)	$\overline{\text{IRQC}}$ mode bit	IPR2 4,5	X:$FFDD
	PAGU Address Compare 0	-	IPR2 0,1	-
	PAGU Address Compare 1	-	IPR2 0,1	-
	PAGU Address Compare 2	-	IPR2 0,1	-
	Codec RX/TX	COIE	6,7	X:$FFC8
	Host Command	HCIE	8,9	X:$FFC4
	Host/DMA RX Data	HRIE	8,9	X:$FFC4
	Host/DMA TX Data	HTIE	8,9	X:$FFC4
	SSI0 RX Data with Exception Status	RIE	10,11	X:$FFD1
	SSI0 RX Data	RIE	10,11	X:$FFD1
	SSI0 TX Data with Exception Status	TIE	10,11	X:$FFD1
	SSI0 TX Data	TIE	10,11	X:$FFD1
	SSI1 RX Data with Exception Status	RIE	12,13	X:$FFD9
	SSI1 RX Data	RIE	12,13	X:$FFD9
	SSI1 TX Data with Exception Status	TIE	12,13	X:$FFD9
	SSI1 TX Data	TIE	12,13	X:$FFD9
	Timer Overflow	OIE	14,15	X:$FFEC
Lowest	Timer Compare	OIE	14,15	X:$FFEC

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 4-6 Interrupt Vectors Space Mapping

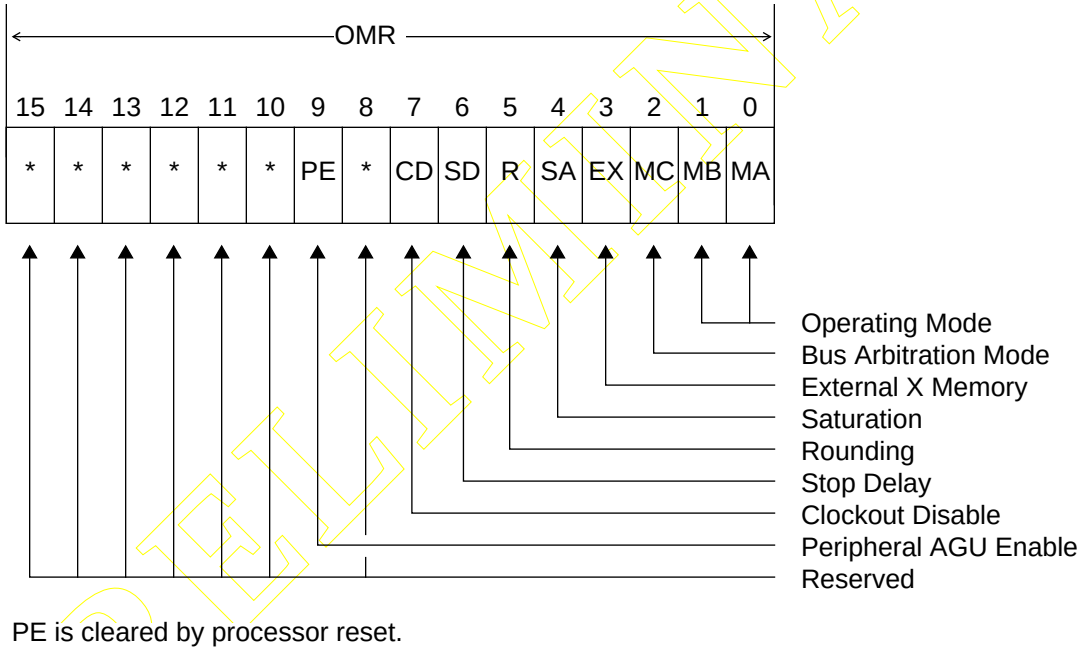
Interrupt Starting Address	IPL	Interrupt Source
$0000	3	Hardware RESET
$0002	3	Illegal Instruction
$0004	3	Stack Error
$0006	3	Reserved
$0008	3	SWI
$000A	0-2	IRQA
$000C	0-2	IRQB
$000E	0-2	IRQC
$0010	0-2	SSI0 Receive Data with Exception Status
$0012	0-2	SSI0 Receive Data
$0014	0-2	SSI0Transmit Data with Exception Status
$0016	0-2	SSI0 Transmit Data
$0018	0-2	SSI1 Receive Data with Exception Status
$001A	0-2	SSI1 Receive Data
$001C	0-2	SSI1 Transmit Data with Exception Status
$001E	0-2	SSI1 Transmit Data
$0020	0-2	Timer Overflow
$0022	0-2	Timer Compare
$0024	0-2	Host DMA Receive Data
$0026	0-2	Host DMA Transmit Data
$0028	0-2	Host Receive Data
$002A	0-2	Host Transmit Data
$002C	0-2	Host Command (default)
$002E	0-2	Codec Receive/Transmit
$0030	0-2	PAGU Address 0 Compare
$0032	0-2	PAGU Address 1 Compare
$0034	0-2	PAGU Address 2 Compare

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Table 4-6 Interrupt Vectors Space Mapping (Continued)

Interrupt Starting Address	IPL	Interrupt Source
$0036	0-2	Available for Host Command
$0038	0-2	Available for Host Command
$003A	0-2	Available for Host Command
.	.	.
.	.	.
.	.	.
$007E	0-2	Available for Host Command

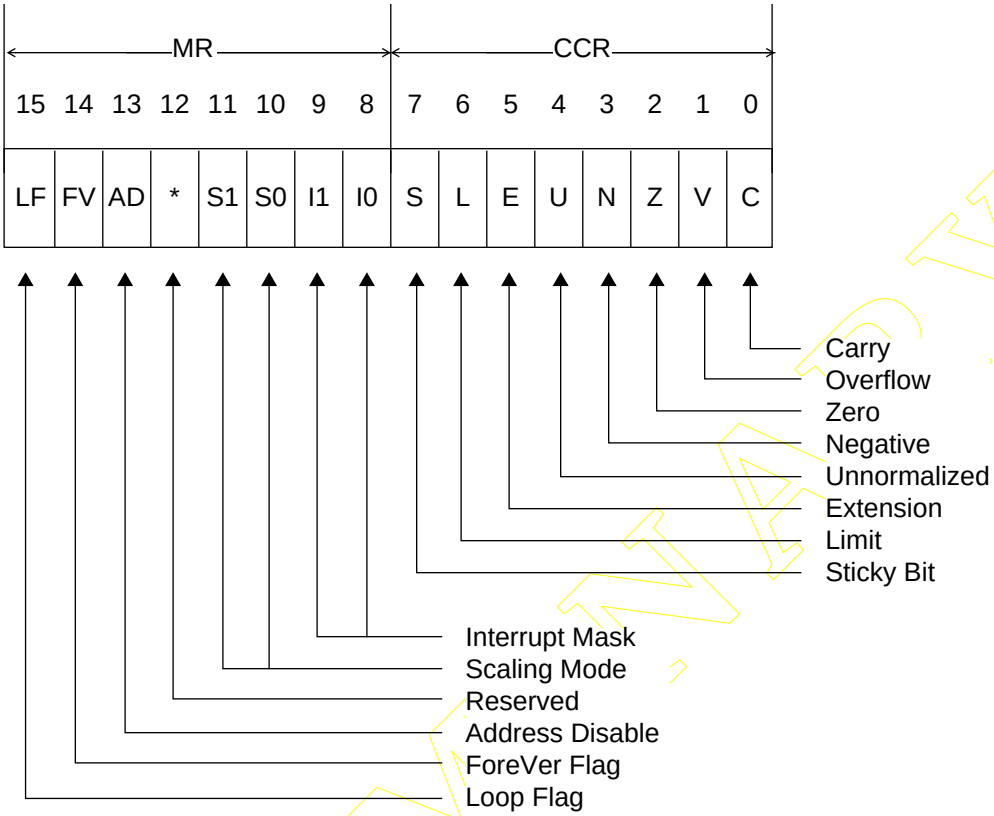


PE is cleared by processor reset.

Figure 4-12 DSP56100 Operating Mode Register (OMR)

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor



AD is cleared by processor reset

Figure 4-13 DSP56167 Status Register (SR)

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

PAGU Operation

The following figures and tables summarize PAGU operation.

Table 4-7 PAGU Operation Summary

PE	AD	Fast Interrupt	Core AALU	PAGU
0	-	-	Drives XAB1 Addr. Reg. Updated	Disabled
1	0	No	Drives XAB1 Addr. Reg. Updated	Disabled
1	-	Yes	Disabled	Drives XAB1Addr. Reg. Updated
1	1	-	Disabled	Drives XAB1 Addr. Reg. Updated

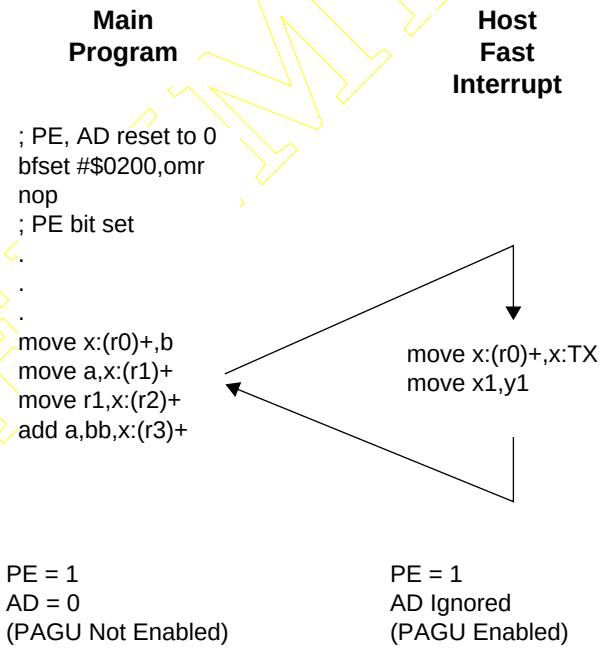


Figure 4-14 PAGU Operation During Fast Interrupt

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

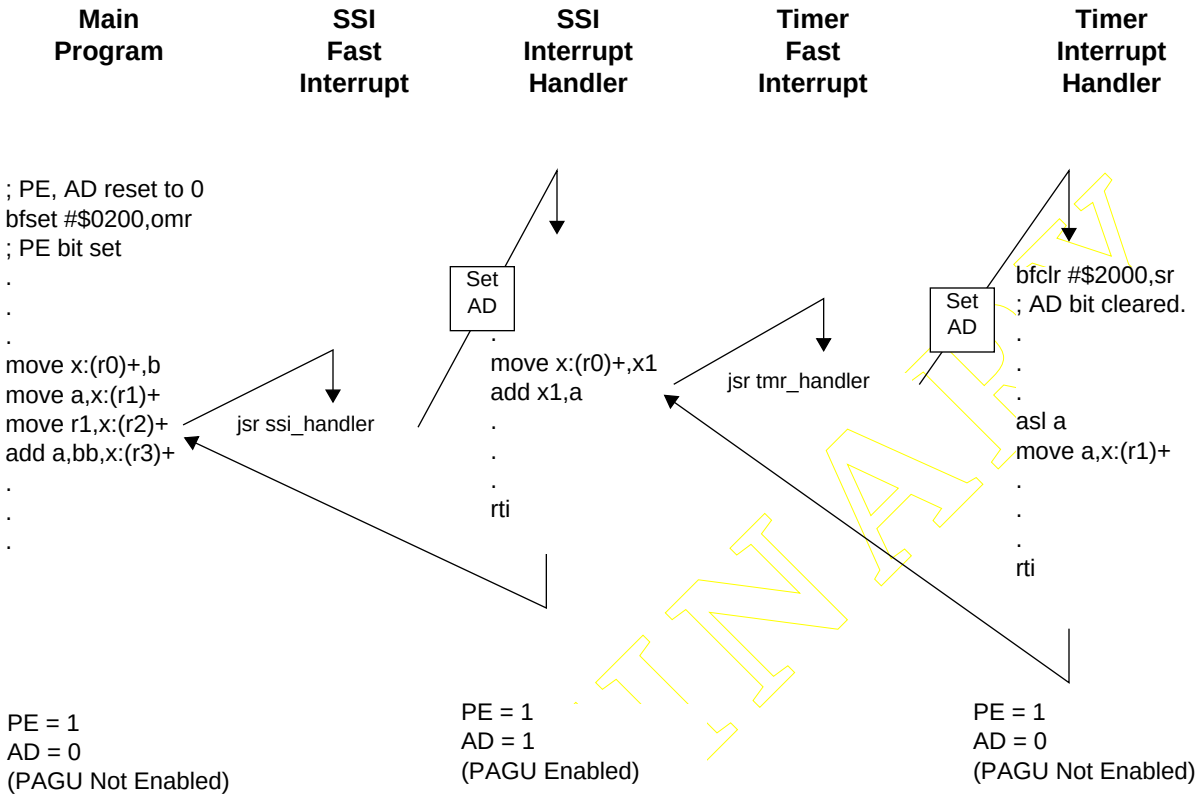


Figure 4-15 PAGU Operation During Normal and Nested Long Interrupt Service Routine

Allowed Move Operations

The PAGU is used for all post update single or multi-cycle moves.

The following conditions apply when using the PAGU:

- BRA(Rn), Lea(Rn) and Norm(Rn) instructions and move instructions with -(Rn), (Rn+Nn), and (R2+xx) addressing modes all use the Core AALU registers.
- Immediate and move peripheral addressing modes work as normal.
- During reduced DALU instructions with dual reads, the first parallel move is executed out of the PAGU and the second parallel move is executed out of the Core AALU.
- During DALU instructions with only one parallel move, the parallel move is executed from the PAGU.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

- During move from peripheral to X memory instruction, the X memory address comes from the PAGU and the peripheral address comes from the Core AALU.
- During moves to and from program memory, the program memory address is output from the Core AALU and the X memory source or destination address, if needed, is output from the PAGU.

Restrictions

The following restrictions apply when using this feature:

- It is illegal to use (r3), (r3)+, (r3)-, and (Rn)+Nn addressing modes when the PAGU is active and the R3 part of the move is not associated with a parallel move.
- Modulo or reverse carry addressing modes is not allowed.
- Must wait one instruction cycle before using the values written to the PAGURn & PAGUCn registers.
- Must wait one instruction cycle before using the PAGU / Core addressing modes after the OMR[PE] and / or SR[AD} bits are changed.

INDEPENDENT EXTERNAL CHIP ENABLE SIGNALS $\overline{BR}$ AND $\overline{PEREN}$

On the DSP56166, while the DSP is in the Master Mode of bus operation, $\overline{BR}$ is asserted for each external memory and external peripheral accesses. When the external peripheral space is accessed, $\overline{PEREN}$ is also asserted. As a result, it is possible to use $\overline{BR}$ as an external chip enable. However, since both $\overline{BR}$ and $\overline{PEREN}$ are asserted for external peripheral space accesses, it is not possible to disable or power-down an external memory versus an external peripheral separately.

The DSP56167 independent chip enable feature allows the DSP to disable or power down the external memory when it is not being accessed even when the external peripheral device is being accessed. As before, the external peripheral device can be disabled using the $\overline{PEREN}$ pin since this signal is deasserted high whenever the external peripheral space is not being accessed.

This feature is enabled when the CHIPEN bit 15 of the Bus Control Register2, (BCR2[15]) is set to 1. It is disabled when CHIPEN is cleared. While in the Bus Master mode of operation (i.e., bit 2 of the OMR is set), the user has the option of enabling $\overline{BR}$ and $\overline{PEREN}$ to act as two independent external chip enable signals.

Note: This feature is not available while the chip is in the Bus Slave Mode of operation, (i.e., OMR[2] is cleared).

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

Programming Environment:

A new control bit called External Chip Enable (ECHIPEN) has been added to the Bus Control Register 2 (BCR2[15] at X:$FFDA), to switch $\overline{BR}$ and $\overline{PEREN}$ from their current mode of operation to the new one.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EC	*	*	*	*	*	*	*	*	*	*	P4	P3	P2	P1	P0

Where:

EC	External Chip Enable; preset to 0 during processor reset
P	External Peripheral Wait States; preset to 0 during processor reset
*	reserved bits; write 0 for future compatibility

Figure 4-16 Port A Bus Control Register 2 (BCR2), X:$FFDA

External Chip Enable Operation

Note: Since, this feature does not alter the $\overline{BR}$ and $\overline{PEREN}$ functions while the DSP is in the Bus Slave Mode of operation, all subsequent discussion assume that the external bus is in the Bus Master Mode of operation.

ECHIPEN is preset to 0 during processor reset. Therefore, upon coming out of reset, $\overline{BR}$ and $\overline{PEREN}$ function as in the DSP56166. This means that $\overline{BR}$ asserts during external memory access (both program and data) and during external peripheral access. $\overline{PEREN}$ is asserted during external peripheral accesses only.

When ECHIPEN is set to 1 via software programming, $\overline{BR}$ only asserts during external memory (program and data) access and $\overline{PEREN}$ asserts only during external peripheral accesses.

If ECHIPEN is now cleared to 0 via software programming, then $\overline{BR}$ and $\overline{PEREN}$ functionality reverts back to be the same as when the chip has just come out of reset.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

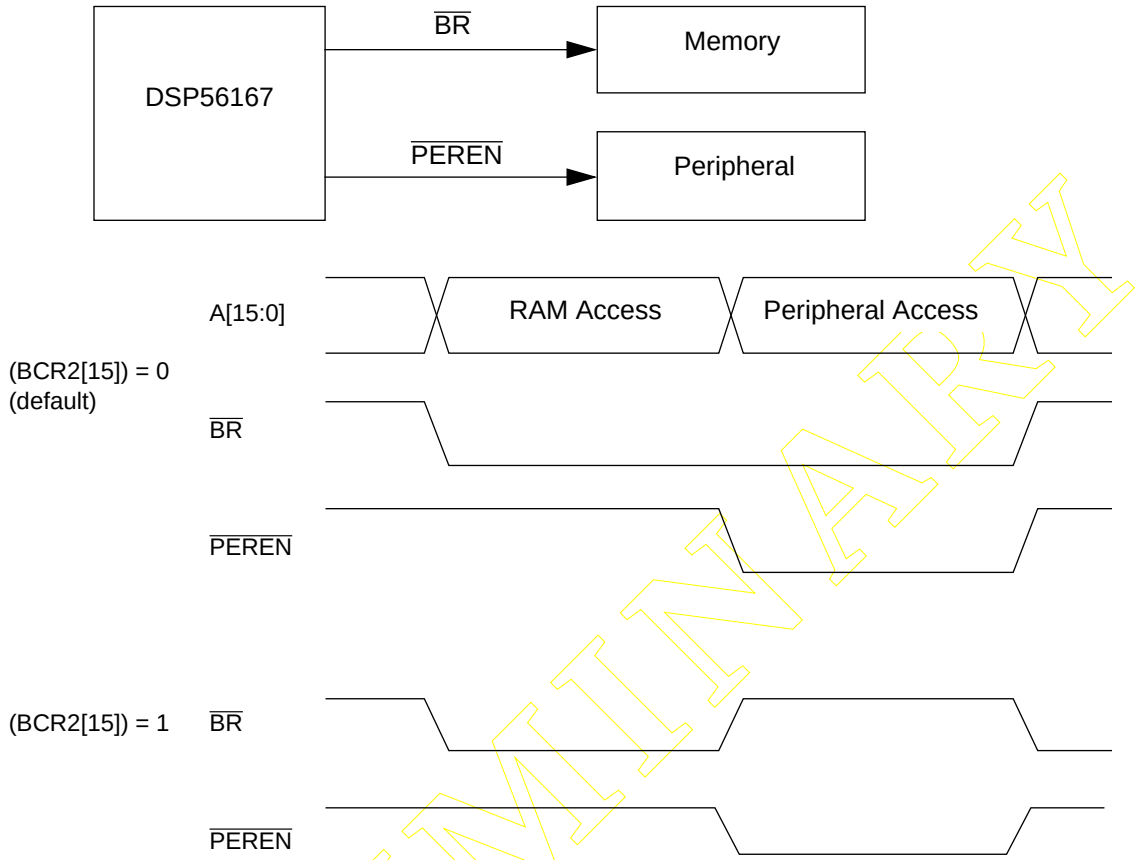


Figure 4-17 External Chip Select Operation

PORT A $\overline{BG}$ PULL-DOWN UNDER SOFTWARE CONTROL

After the $\overline{BG}$ pin is initialized high during hardware reset in bus Master Mode, the $\overline{BG}$ pin can be optionally pulled low by setting Bus Grant Pull Down bit (BGPD) in the Bus Control Register (BCR[13]). This allows the DSP to become the permanent bus master while in bus Master Mode without having to add an external pull-up resistor. When BGPD is cleared, $\overline{BG}$ retains the last logic state that was driven by either the DSP or by an external bus master.

Note: BGPD is cleared by the hardware reset allowing BG to be pulled up as the default state so as not to interfere with any existing bus design.

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

PORT A AND OnCE PORT $\overline{DR}$ SIGNAL LINE KEEPERS WITH RESET

Active pull-up and/or pull-down resistors have always been required for the external bus interface pins to keep them at a valid logic state when the DSP gives up the bus to another bus master. This is also true during hardware reset.

Adding on-chip static latches or keepers eliminates the need of including external resistors on board when no external memory or peripherals are attached to the DSP. When external memory and/or peripherals are desired, most if not all of the external resistors can be eliminated. The on-chip static latch for the OnCE DR pin eliminates the need for the eternal resistor when the OnCE is not needed.

The external bus interface control signals and the OnCE DR pins have built in reset circuitry to guarantee that they will be initialized to the desired functional state when the DSP comes out of hardware reset.

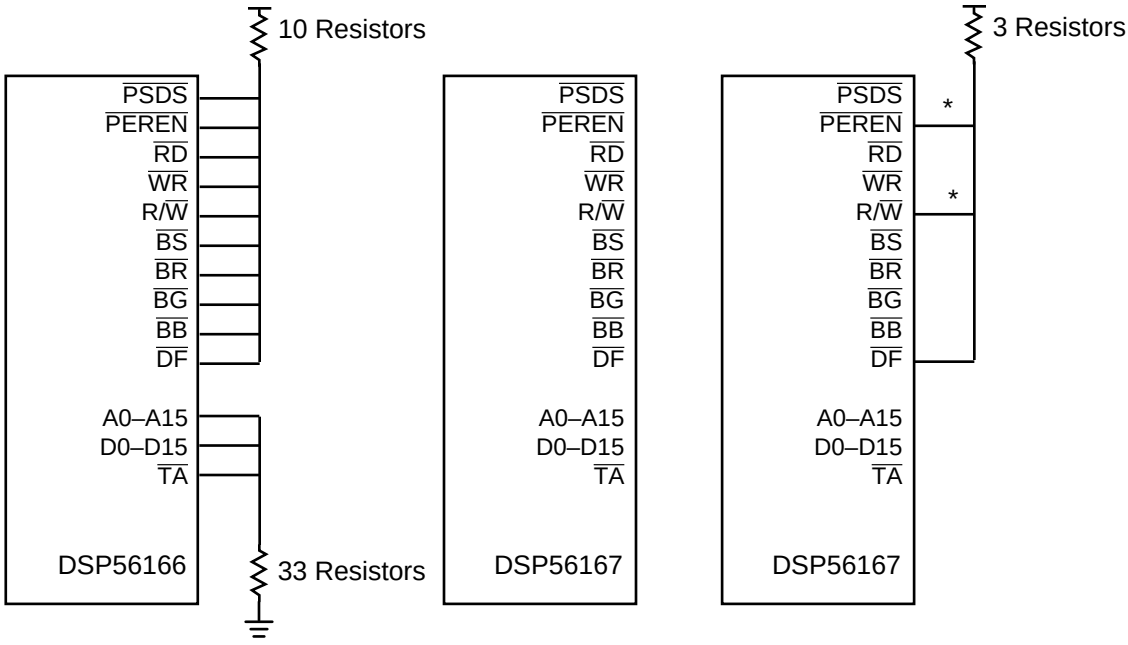


Figure 4-18 DSP56167 Pull-Up/Pull-Down Resistors

Downloaded from Elcodis.com electronic components distributor

EXTERNAL PROGRAM MEMORY ACCESS DISABLE

For those users that run strictly from internal program memory, it is now possible to disable the external program memory access as a power-saving measure.

Note: This has no effect on external data memory or external peripheral accesses.

When this feature is enabled, the internal path from the PAB bus to the Port A address pins is disabled, eliminating unnecessary switching inside the DSP.

External Program Memory Access Disable Programming Environment:

A new control bit called External PAB Disable (EPABDIS) has been added to the Bus Control Register, BCR[12] at X:$FFDE, to disable the external program memory access.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BH	BS	BGPD	EPABDIS	*	*	X4	X3	X2	X1	X0	P4	P3	P2	P1	P0

Where:

BH	Bus Request Hold; preset to 0 during processor reset
BS	Bus State Status; Read Only
BGPD	Bus Grant Pull-Down; preset to 0 during processor reset
EPABDIS	External PAB Disable; preset to 0 during processor reset
X	External Data Memory Wait States; preset to 1 during processor reset
P	External Program Memory Wait States; preset to 1 during processor reset
*	reserved bits; write 0 for future compatibility

Figure 4-19 Port A Bus Control Register (BCR), X:$FFDE

External Program Memory Access Disable Operation

EPABDIS is preset to 0 during processor reset. So, coming out of reset the Port A bus functions exactly as the DSP56166. When EPABDIS is set to 1 via software programming, Port A access is restricted to external data memory or external peripheral accesses.

Note: Attempts to access external program memory while this bit is set result in an incorrect address appearing at the Port A address pins. The results of the operation will be incorrect.

If EPABDIS is cleared to 0 via software programming, then Port A functionality will revert back to be the same as when the chip just came out of reset. However, due to pipeline delays inside the DSP, there should be at least 1 instruction cycle between when EPABDIS is cleared and external program memory is accessed.

Downloaded from Elcodis.com electronic components distributor

Feature Changes Description

Changes to DSP56166 functionality in the DSP56167 include:

- Codec input circuitry can be single-ended or differential
- Codec input impedance is software selectable
- Codec output reference voltages (VRDA and VRAD) are now $1/2\ V_{DDA}$
- Codec output drive capability (for VRDA, VRAD, SPKP, and SPKM) is now 0.35 mA
- Codec single-ended small signal output (SPKP and SPKM) impedance has changed to a range of 4.0–16.0 Ω for 300 Hz and a range of 12.6–50.4 Ω for 3000 Hz
- Codec DAC outputs (absolute single-ended) now can swing between 0.35 V and $V_{DD} - 0.4$ V.

Refer to the section titled **Analog I/O Considerations** on page 4-4 for a detailed description of design requirements for the on-chip codec.

DSP56166 Chip Errata Fixed in the DSP56167

The following DSP56166 chip errata (some of which required hardware workarounds) have been fixed in the DSP56167:

- CHKAAU instruction does not operate correctly if there is a killed instruction between the last valid AALU update and CHKAAU
- The second read from internal data memory of a dual read instruction will transfer the wrong data if it is preceded by a conditional transfer instruction with the condition being false (i.e., the transfer is aborted).
- The OnCE NOS0 status flag does not get updated correctly when the DSP enters the Wait or Stop mode of operation.
- The SSI RS/TX interrupt occurs when the interrupt is enabled even though the RE and TE bits are cleared (i.e., function disabled).
- The SSI receiver does not operate independently from the transmitter in Gated Clock mode.
- In External Gated Clock mode, the SSI STD signal can remain tri-stated during the first two bits of the transmitted word.
- In External Gated Clock mode, the STD signal should not be tri-stated until the end of the transmitted word regardless when the TE bit is cleared (i.e., the function is disabled).

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

- The SSI TDE and TUE bits can be incorrectly set after being cleared if the clear operation is performed is performed during the last half bit period of the current word, or during the first half bit period of the next word.
- The PLL may lock at the maximum VCO frequency during power up at low voltage and high temperature. (The recommended workaround was to connect the SXFC to GND and not V_{CC}).
- The PLL Lock bit failed to be asserted properly in an over-damped system. (The recommended workaround was to use a software time loop of at least 5 ms instead of the “lock bit” polling loop.)
- The PLL may lock at the maximum VCO frequency when coming out of Stop mode of operation. (The workaround was to connect a 10 MΩ resistor between SXFC and GND.)
- Due to SXFC external filter capacitor leakage and noise, the PLL frequency may jitter by as much as 25 MHz at the PLL input frequency rate (output from the ID divider). (The workaround was to use a faster reference clock, a smaller Multiplication Factor, a low-leakage capacitor for the SXFC loop filter capacitor, and to reduce the coupled noise level into the PLL by careful board design.)

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

SECTION 5

ORDERING INFORMATION

DSP56167 ordering information in the table below lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 5-1 DSP56167 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56167	5 V	Thin Quad Flat Pack (TQFP)	112	60	XC56167FV60

PRELIMINARY

Downloaded from Elcodis.com electronic components distributor

OnCE and Mfax are trademarks of Motorola, Inc.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and Ⓜ are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:

USA/Europe/Locations Not Listed:
Motorola Literature Distribution
P.O. Box 5405
Denver, Colorado 80217
303-675-2140
1 (800) 441-2447

Mfax™:
RMFAX0@email.sps.mot.com
TOUCHTONE (602) 244-6609
US & Canada ONLY (800) 774-1848

Asia/Pacific:
Motorola Semiconductors H.K. Ltd.
8B Tai Ping Industrial Park
51 Ting Kok Road
Tai Po, N.T., Hong Kong
852-26629298

Technical Resource Center:
1 (800) 521-6274

DSP Helpline
dsphelp@dsp.sps.mot.com

Japan:
Nippon Motorola Ltd.
Tatsumi-SPD-JLDC
6F Seibu-Butsuryu-Center
3-14-2 Tatsumi Koto-Ku
Tokyo 135, Japan
81-3-3521-8315

Internet:
http://www.motorola-dsp.com

MOTOROLA

Downloaded from Elcodis.com electronic components distributor