SHARC Processor

Preliminary Technical Data

ADSP-21478/ADSP-21479

SUMMARY

Note: This datasheet is preliminary. This document contains material that is subject to change without notice.

High performance 32-bit/40-bit floating point processor optimized for high performance audio processing

Single-instruction, multiple-data (SIMD) computational architecture

On-chip memory—5 Mbits of on-chip RAM, 4 Mbits of on-chip ROM

Up to 266 MHz operating frequency

Qualified for Automotive Applications . See Automotive Products on Page 69

Code compatible with all other members of the SHARC family

The ADSP-2147x processors are available with unique audio-centric peripherals such as the digital applications interface, serial ports, precision clock generators, S/PDIF transceiver, asynchronous sample rate converters, input data port, and more.

For complete ordering information, see Ordering Guide on Page 69.

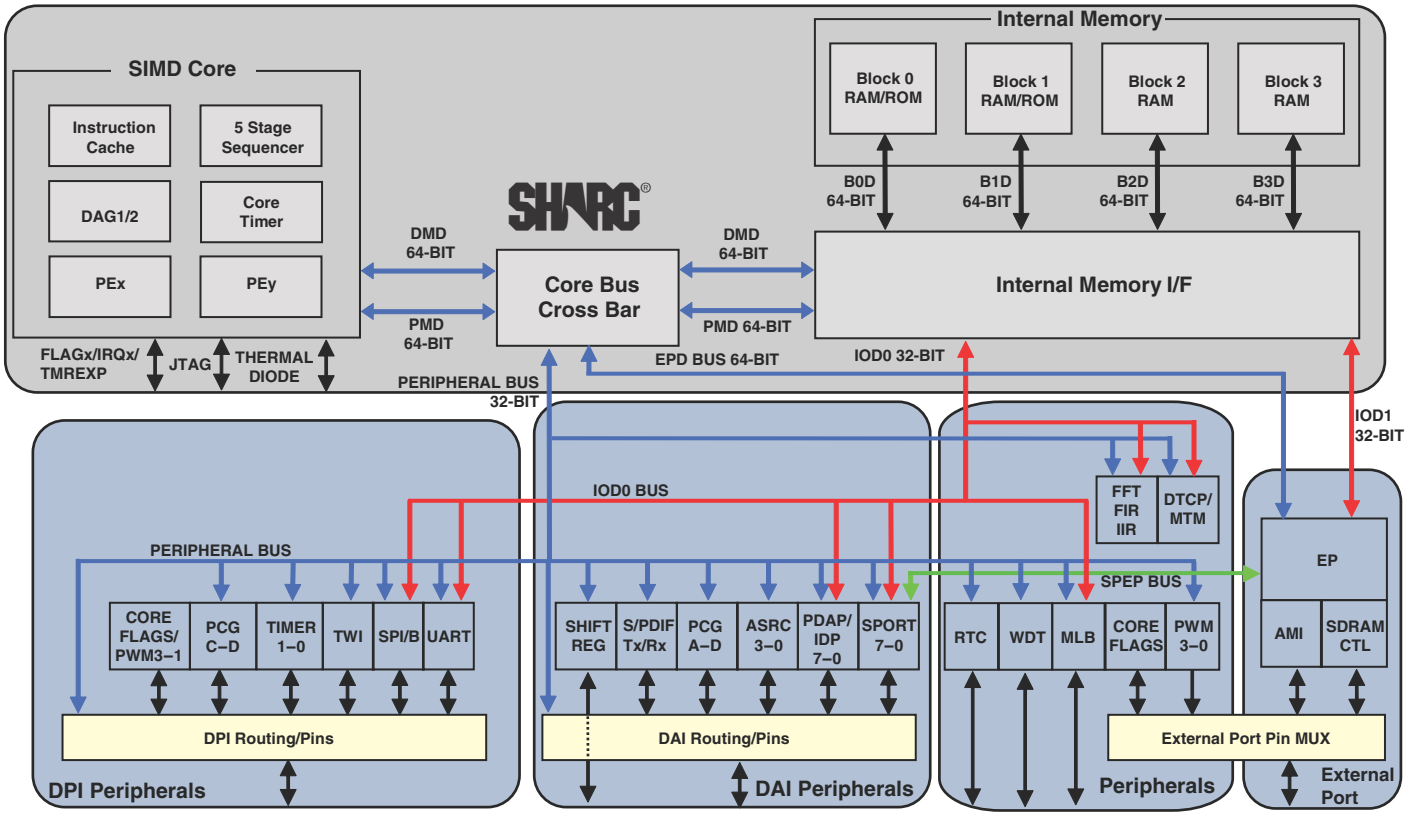

Figure 1. Functional Block Diagram

Rev. PrB

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REVISION HISTORY

3/10—Rev. PrB: Initial version

GENERAL DESCRIPTION

The ADSP-21478/ADSP-21479/ SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The processors are source code compatible with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-2146x, and ADSP-2116x DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. These new processors are 32-bit/40-bit floating point processors optimized for high performance audio applications with its large on-chip SRAM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

Table 1 shows performance benchmarks for the ADSP-2147x processors. Table 2 shows the features of the individual product offerings.

Table 1. Processor Benchmarks

Benchmark Algorithm	Speed (at 266 MHz)
1024 Point Complex FFT (Radix 4, With Reversal)	34.5 µs
FIR Filter (per Tap)[1]	1.88 ns
IIR Filter (per Biquad)[1]	7.5 ns
Matrix Multiply (Pipelined)	
[3 × 3] × [3 × 1]	16.91 ns
[4 × 4] × [4 × 1]	30.07 ns
Divide (y/x)	13.1 ns
Inverse Square Root	20.4 ns

[1] Assumes two files in multichannel SIMD mode

Table 2. ADSP-2147x Family Features

Feature	ADSP-21478	ADSP-21479
Frequency	266 MHz	
RAM	3M bits	5M bits
ROM	N/A	
Pulse-Width Modulation	4 Units	
AMI Interface with 16-bit Support	Yes	
SDRAM Memory Bus Width	16-bit	
Serial Ports	8	
Direct DMA from SPORTs to External Memory	Yes	
FIR, IIR, FFT Accelerator	Yes	
MLB Interface	Automotive Models Only	
Watch Dog Timer	Yes	
Real-time Clock	Yes	
Shift Register	Yes	
IDP/PDAP	Yes	

Table 2. ADSP-2147x Family Features (Continued)

Feature	ADSP-21478	ADSP-21479
UART	1	
DAI (SRU)/DPI (SRU2)	20/14 pins	
S/PDIF Transceiver	1	
SPI	2	
TWI	1	
SRC Performance	–128 dB	
Thermal Diode[1]	Yes	
VISA Support	Yes	
Package[2]	196-Ball CSP_BGA 100-Lead LQFP	

[1] Available on the 100-lead package only.
[2] The 100-lead packages of the ADSP-21478 and 21479 processors do not contain an external port.

The diagram on Page 1 shows the two clock domains that make up the ADSP-2147x processors. The core clock domain contains the following features.

- Two processing elements (PEx, PEy), each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting 2x64-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (up to 5M bit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allows flexible exception handling.

The block diagram of the ADSP-2147x on Page 1 also shows the peripheral clock domain (also known as the I/O processor) which contains the following features:

- IOD0 (peripheral DMA) and IOD1 (external port DMA) buses for 32-bit data transfers
- Peripheral and external port buses for core connection
- External port with an AMI and SDRAM controller
- 4 units for PWM control
- 1 MTM unit for internal-to-internal memory transfers
- Digital applications interface that includes four precision clock generators (PCG), an input data port (IDP/PDAP) for serial and parallel interconnect, an S/PDIF receiver/transmitter, four asynchronous sample rate converters, eight serial ports, a flexible signal routing unit (DAI SRU).

- Digital peripheral interface that includes two timers, a 2-wire interface, one UART, two serial peripheral interfaces (SPI), 2 precision clock generators (PCG), three pulse width modulation (PWM) units, and a flexible signal routing unit (DPI SRU).

As shown in the block diagram on Page 5, the processor uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the processor achieves an instruction cycle time of 3.75 ns at 266 MHz. With its SIMD computational hardware, the processors can perform 1.596 GFLOPS running at 266 MHz.

FAMILY CORE ARCHITECTURE

The ADSP-2147x is code compatible at the assembly level with the ADSP-2146x, ADSP-2137x, ADSP-2136x, ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-2147x shares architectural features with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-2146x and ADSP-2116x SIMD SHARC processors, as shown in Figure 2 and detailed in the following sections.

SIMD Computational Engine

The ADSP-2147x contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

SIMD mode is supported from external SDRAM but is not supported in the AMI.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Timer

The processor contains a core timer that can generate periodic software interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the processor's enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0-R15 and in PEY as S0-S15.

Context Switch

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result registers all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

Universal Registers

These registers can be used for general-purpose tasks. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all system registers (control/status) of the core.

The data bus exchange register (PX) permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM data bus. These registers contain hardware to handle the data width difference.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-2147x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 2). With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-2147x includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators With Zero-Overhead Hardware Circular Buffer Support

The ADSP-2147x's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital

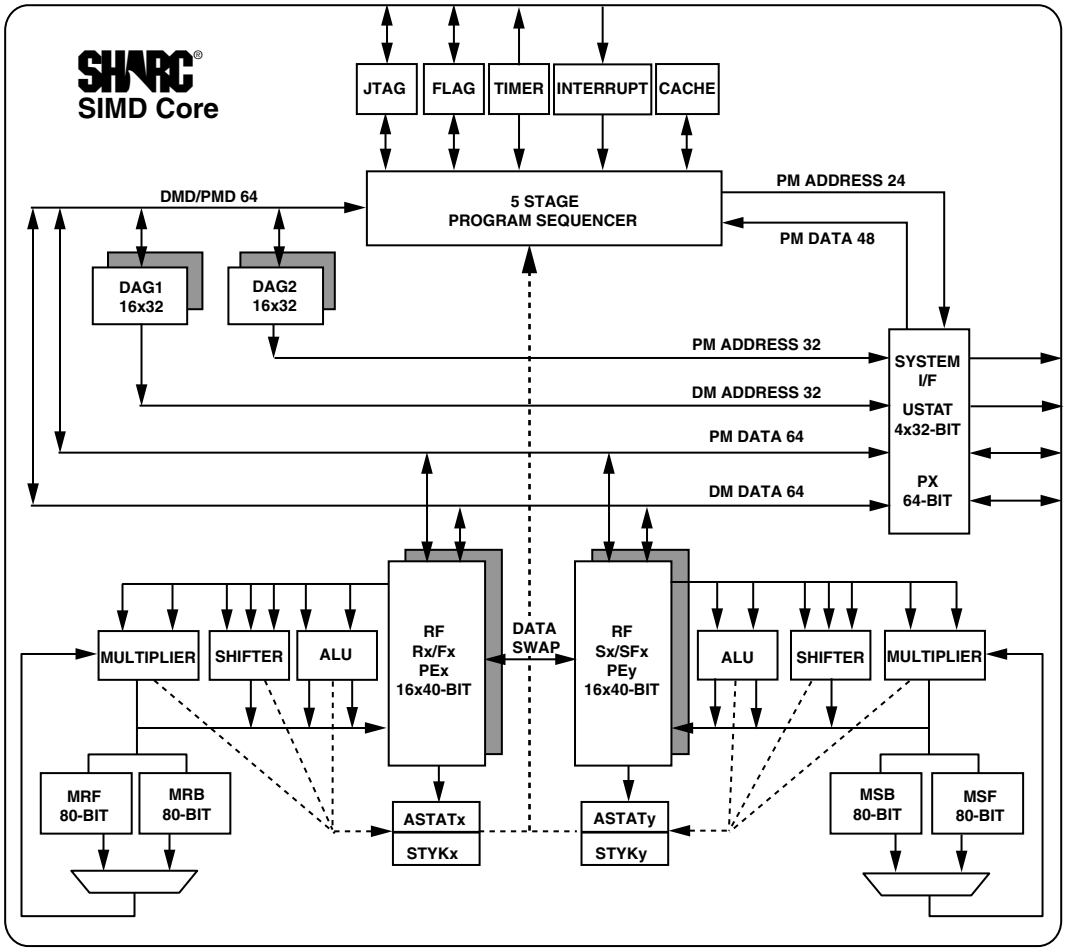


Figure 2. SHARC Core Block Diagram

signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the processors contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-2147x can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the ADSP-2147x supports new instructions of 16 and 32 bits. This feature, called Variable Instruction Set Architecture (VISA), drops redundant/unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external SDRAM memory. This support is not extended to the asynchronous memory interface (AMI). Source modules need to be built using the VISA option, in order to allow code generation tools to create these more efficient opcodes.

On-Chip Memory

The ADSP-21478 processor contains 3 Mbits of internal RAM (Table 3) and the ADSP-21479 processor contains 5 Mbits of internal RAM (Table 4). Each block can be configured for different combinations of code and data storage. Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The ADSP-2147x memory architecture, in combination with its separate on-chip buses, allow two data transfers from the core and one from the I/O processor, in a single cycle.

The processor's SRAM can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 megabits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit

floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory maps in Table 4 and Table 5 display the internal memory address space of the processors. The 48-bit space section describes what this address range looks like to an instruction that retrieves 48-bit memory. The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks (assuming there are no block conflicts). The total bandwidth is realized using the DMD and PMD buses (2 x 64-bits, CCLK speed) and the IOD0/1 buses (2 x 32-bit, PCLK speed).

Table 3. Internal Memory Space (ADSP-21478)[1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 FFFF
Block 0 SRAM 0x0004 9000–0x0004 CFFF	Block 0 SRAM 0x0008 C000–0x0009 1554	Block 0 SRAM 0x0009 2000–0x0009 9FFF	Block 0 SRAM 0x0012 4000–0x0013 3FFF
Reserved 0x0004 D000–0x0004 FFFF	Reserved 0x0009 1555–0x0009 5554	Reserved 0x0009 A000–0x0009 FFFF	Reserved 0x0013 4000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 CFFF	Block 1 SRAM 0x000A C000–0x000B 1554	Block 1 SRAM 0x000B 2000–0x000B 9FFF	Block 1 SRAM 0x0016 4000–0x0017 3FFF
Reserved 0x0005 D000–0x0005 FFFF	Reserved 0x000B 1555–0x000B 5554	Reserved 0x000B A000–0x000B FFFF	Reserved 0x0017 4000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 1FFF	Block 2 SRAM 0x000C 0000–0x000C 2AA9	Block 2 SRAM 0x000C 0000–0x000C 3FFF	Block 2 SRAM 0x0018 0000–0x0018 7FFF
Reserved 0x0006 2000– 0x0006 FFFF	Reserved 0x000C 2AAA–0x0000 D5554	Reserved 0x000C 4000–0x000D FFFF	Reserved 0x0018 8000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 1FFF	Block 3 SRAM 0x000E 0000–0x000E 2AA9	Block 3 SRAM 0x000E 0000–0x000E 3FFF	Block 3 SRAM 0x001C 0000–0x001C 7FFF
Reserved 0x0007 2000–0x0007 FFFF	Reserved 0x000E 2AAA–0x000F 0000	Reserved 0x000E 4000–0x000F FFFF	Reserved 0x001C 8000–0x001F FFFF

[1] Some ADSP-2147x processors include a customer-definable ROM block. ROM addresses on these models are not reserved as shown in this table. Please contact your Analog Devices sales representative for additional details.

Table 4. Internal Memory Space (ADSP-21479)[1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 FFFF
Block 0 SRAM 0x0004 9000–0x0004 EFFF	Block 0 SRAM 0x0008 C000–0x0009 3FFF	Block 0 SRAM 0x0009 2000–0x0009 DFFF	Block 0 SRAM 0x0012 4000–0x0013 BFFF
Reserved 0x0004 F000–0x0004 FFFF	Reserved 0x0009 4000–0x0009 5554	Reserved 0x0009 E000–0x0009 FFFF	Reserved 0x0013 C000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000AFFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 EFFF	Block 1 SRAM 0x000A C000–0x000B 3FFF	Block 1 SRAM 0x000B 2000–0x000B DFFF	Block 1 SRAM 0x0016 4000–0x0017 BFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B 4000–0x000B 5554	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 3FFF	Block 2 SRAM 0x000C 0000–0x000C 5554	Block 2 SRAM 0x000C 0000–0x000C 7FFF	Block 2 SRAM 0x0018 0000–0x0018 FFFF
Reserved 0x0006 4000– 0x0006 FFFF	Reserved 0x000C 5555–0x0000D 5554	Reserved 0x000C 8000–0x000D FFFF	Reserved 0x0019 0000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 3FFF	Block 3 SRAM 0x000E 0000–0x000E 5554	Block 3 SRAM 0x000E 0000–0x000E 7FFF	Block 3 SRAM 0x001C 0000–0x001C FFFF
Reserved 0x0007 4000–0x0007 FFFF	Reserved 0x000E 5555–0x0000F 5554	Reserved 0x000E 8000–0x000F FFFF	Reserved 0x001D 0000–0x001F FFFF

[1] Some ADSP-2147x processors include a customer-definable ROM block. ROM addresses on these models are not reserved as shown in this table. Please contact your Analog Devices sales representative for additional details.

ROM Based Security

The ADSP-2147x has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the processor does not boot-load any external code, executing exclusively from internal ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or Test Access Port will be assigned to each customer. The device will ignore a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

Digital Transmission Content Protection

The DTCP specification defines a cryptographic protocol for protecting audio entertainment content from illegal copying, intercepting, and tampering as it traverses high performance digital buses, such as the IEEE 1394 standard. Only legitimate entertainment content delivered to a source device via another approved copy protection system (such as the DVD content scrambling system) is protected by this copy protection system. For more information on this feature, contact your local ADI sales office.

FAMILY PERIPHERAL ARCHITECTURE

The ADSP-2147x family contains a rich set of peripherals that support a wide variety of applications including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, motor control, imaging, and other applications.

External Port

The external port is available in the 196-ball CSP_BGA package. The interface supports access to the external memory through core and DMA accesses. The external memory address space is divided into four banks. Any bank can be programmed as either asynchronous or synchronous memory. The external ports are comprised of the following modules.

- An Asynchronous Memory Interface which communicates with SRAM, FLASH, and other devices that meet the standard asynchronous SRAM access protocol. The AMI

supports 14M words of external memory in bank 0 and 16M words of external memory in bank 1, bank 2, and bank 3.

- An SDRAM controller that supports a glueless interface with any of the standard SDRAMs. The SDC supports 62M words of external memory in bank 0, and 64M words of external memory in bank 1, bank 2, and bank 3.
- Arbitration logic to coordinate core and DMA transfers between internal and external memory over the external port.

External Memory

The external port provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port, available in the 196-ball CSP_BGA package, may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers. The first is an SDRAM controller for connection of industry-standard synchronous DRAM devices and DIMMs (dual inline memory module), while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types. Non-SDRAM external memory address space is shown in Table 5.

SIMD Access to External Memory

The SDRAM controller on the processor supports SIMD access on the 64-bit EPD (external port data bus) which allows to access the complementary registers on the PEy unit in the normal word space (NW). This improves performance since there is no need to explicitly load the complimentary registers as in SISD mode.

Table 5. External Memory for Non-SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	14M	0x0020 0000–0x00FF FFFF
Bank 1	16M	0x0400 0000–0x04FF FFFF
Bank 2	16M	0x0800 0000–0x08FF FFFF
Bank 3	16M	0x0C00 0000–0x0CFF FFFF

External Memory Execution

In the ADSP-21479, the program sequencer can execute code directly from external memory bank 0 (SRAM, SDRAM). This allows a reduction in internal memory size. With external execution, programs run at slower speeds since 48-bit instructions are fetched in parts from a 16-bit external bus coupled with the inherent latency of fetching instructions from SDRAM. Fetching instructions from SDRAM generally takes 1.5 peripheral clock cycles per instruction.

VISA and Non VISA Access to External Memory

The SDRAM controller on the processor supports VISA code operation which reduces the memory load since the VISA instructions are compressed. Moreover, bus fetching is reduced because in the best case one 48-bit fetch contains 3 valid instructions. Code execution from the traditional non-VISA operation is also supported. Note that code execution is only supported from bank 0 regardless of VISA/non-VISA.

SDRAM Controller

The SDRAM controller, available on the ADSP-21479 in the 196-ball CSP_BGA package, provides an interface of up to four separate banks of industry-standard SDRAM devices or DIMMs, at speeds up to f_{SDCLK}. Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 16M bytes and 128M bytes of memory. SDRAM external memory address space is shown in Table 6.

Table 6. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000–0x03FF FFFF
Bank 1	64M	0x0400 0000–0x07FF FFFF
Bank 2	64M	0x0800 0000–0x0BFF FFFF
Bank 3	64M	0x0C00 0000–0x0FFF FFFF

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. Note that 32-bit wide devices are not supported on SDRAM and the AMI interface.

The SDRAM controller address, data, clock, and control pins can drive loads up to distributed 30 pF loads. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions as well as 32-bit data are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap. In case of 16-bit wide external memory, two 48-bit instructions are stored in six 32-bit wide memory locations. For example, if 2k instructions are placed in 16-bit wide external memory starting at the bank 0 normal-word base address 0x0030 0000 (corresponding to instruction address 0x0020 0000) and ending at address 0x0030 0BFF (corresponding to instruction address 0x0020 07FF), then data buffers can be placed starting at an address that is offset by 3k 32-bit words (for example, starting at 0x0030 0C00).

Asynchronous Memory Controller

The asynchronous memory controller, available on the ADSP-21479 in the 196-ball CSP_BGA package, provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 14M word window and banks 1, 2, and 3 occupy a 16M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

External Port Throughput

The throughput for the external port, based on 133 MHz clock and 16-bit data bus, is 88 M bytes/s for the AMI and 266 M bytes/s for SDRAM.

MediaLB

The automotive models of the ADSP-2147x processors have an MLB interface which allows the processor to function as a media local bus device. It includes support for both 3-pin as well as 5-pin media local bus protocols. It supports speeds up to 1024 FS (49.25 Mbits/sec, FS = 48.1 kHz) and up to 31 logical channels, with up to 124 bytes of data per media local bus frame. For a list of automotive products, see Automotive Products on Page 69.

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the mid-point of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the mid-point of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

PWM signals can be mapped to the external port address lines or to the DPI pins.

Digital Applications Interface (DAI)

The digital applications interface (DAI) provides the ability to connect various peripherals to any of the DAI pins (DAI_P20–1).

Programs make these connections using the signal routing unit (SRU), shown in Figure 1.

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI also includes eight serial ports, four precision clock generators (PCG), S/PDIF transceiver, four ASRCs, and an input data port (IDP). The IDP provides an additional input path to the SHARC core, configurable as either eight channels of serial data, or a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

Serial Ports

The ADSP-2147x features eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports can support up to 16 transmit or 16 receive channels of audio data when all eight SPORTs are enabled, or four full duplex TDM streams of 128 channels per frame.

The serial ports operate at a maximum data rate of $f_{PCLK}/4$. Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

Left-justified mode is a mode where in each frame sync cycle two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified and I^2S protocols (I^2S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs such as the Analog Devices AD183x family), with two data pins, allowing four left-justified

or I^2S channels (using two stereo devices) per serial port, with a maximum of up to 32 I^2S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified and I^2S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

The serial ports also contain frame sync error detection logic where the serial ports detect frame syncs that arrive early (for example frame syncs that arrive while the transmission/reception of the previous word is occurring). All the serial ports also share one dedicated error interrupt.

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, I^2S or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), and are controlled by the SRU control registers.

Asynchronous Sample Rate Converter

The sample rate converter (ASRC) contains four ASRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 128 dB SNR. The ASRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the ASRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Input Data Port

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I^2S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I^2S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generators

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

The outputs of PCG A and B can be routed through the DAI pins and the outputs of PCG C and D can be driven on to the DAI as well as the DPI pins.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface ports (SPI), one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), three PWM modules (PWM3–1), and two general-purpose timers.

Serial Peripheral (Compatible) Interface

The ADSP-2147x SHARC processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Support for bit rates ranging from (f_{PCLK}/1,048,576) to (f_{PCLK}/16) bits per second.

- Support for data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

Timers

The ADSP-2147x has a total of three timers: a core timer that can generate periodic software interrupts and two general-purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watch dog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and the general-purpose timers have one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables the general-purpose timer.

2-Wire Interface Port (TWI)

The TWI is a bidirectional 2-wire, serial bus used to move 8-bit data while maintaining compliance with the I^2C bus protocol. The TWI master incorporates the following features:

- 7-bit addressing
- Simultaneous master and slave operation on multiple device systems with support for multi master data arbitration
- Digital filtering and timed event processing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

Shift Register

The shift register can be used as a serial to parallel data converter. The shift register module consists of an 18-stage serial shift register, 18-bit latch, and three-state output buffers. The shift register and latch have separate clocks. Data is shifted into the serial shift register on the positive-going transitions of the shift register serial clock (SR_SCLK) input. The data in each flip-flop is transferred to the respective latch on a positive-going transition of the shift register latch clock (SR_LAT) input.

The shift register's signals can be configured as follows.

- The SR_SCLK can come from any of the SPORT0–7 SCLK outputs, PCGA/B clock, any of the DAI pins (1–8), and one dedicated pin (SR_SCLK).
- The SR_LAT can come from any of SPORT0–7 Frame sync outputs, PCGA/B frame sync, any of the DAI pins (1–8), and one dedicated pin (SR_LAT).
- The SR_SDI input can from any of SPORT0–7 serial data outputs, any of the DAI pins (1–8), and one dedicated pin (SR_SDI).

Note that the SR_SCLK, SR_LAT, and SR_SDI inputs must come from same source except in the case of where SR_SCLK comes from PCGA/B or SR_SCLK and SR_LAT come from PCGA/B.

If SR_SCLK comes from PCGA/B, then SPORT0–7 will generate the SR_LAT and SR_SDI signals. If SR_SCLK and SR_LAT come from PCGA/B, then SPORT0–7 will generate the SR_SDI signal.

I/O PROCESSOR FEATURES

The I/O processor provides up to 65 channels of DMA as well as an extensive set of peripherals.

DMA Controller

The processor's on-chip DMA controller allows data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-2147x's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP) or the UART.

Up to 67 channels of DMA are available on the ADSP-2147x processors as shown in Table 7.

Programs can be downloaded to the ADSP-2147x using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

Table 7. DMA Channels

Peripheral	DMA Channels
SPORTs	16
PDAP	8
SPI	2
UART	2
External Port	2
Accelerators	2
Memory-to-Memory	2
MLB[1]	31

[1] Automotive models only.

Delay Line DMA

The ADSP-2147x processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and hence to external memory) with limited core interaction.

Scatter/Gather DMA

The ADSP-2147x processor provides scatter/gather DMA functionality. This allows processor DMA reads/writes to/from noncontingeous memory blocks.

FFT Accelerator

FFT accelerator implements radix-2 complex/real input, complex output FFT with no core intervention.

FIR Accelerator

The FIR (finite impulse response) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

IIR Accelerator

The IIR (infinite impulse response) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

Watch Dog Timer

The watch dog timer is used to supervise stability of the system software. When used in this way, software reloads the watch dog timer in a regular manner so that the downward counting timer never expires. An expiring timer then indicates that system software might be out of control.

The ADSP-2147x processors include a 32-bit watch dog timer that can be used to implement a software watch dog function. A software watch dog can improve system reliability by forcing the processor to a known state through generation of a system reset, if the timer expires before being reloaded by software. Software initializes the count value of the timer, and then enables the timer.

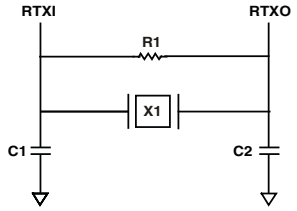
The watch dog timer resets both the core and the internal peripherals. After an external reset, the WDT must be disabled by default. Software must be able to determine if the watch dog was the source of the hardware reset by interrogating a status bit in the watch dog timer control register.

The WDT contains a software programmable Trip Counter register that sets the number of times that the WDT can expire before the $\overline{\text{WDTRSTO}}$ pin is continually asserted until the next time hardware reset is applied. The trip counter is not cleared by the WDT generated reset. This gives software the ability to count the number of WDT generated resets using the CURTRIPVAL field in the trip counter register.

Real-Time Clock

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the SHARC processor. Connect RTC pins RTXI and RTXO with external components as shown in Figure 3.

The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time. An RTCLKOUT signal that operates at 1Hz is also provided for calibration.



NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 3. External Components for RTC

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and an 32,768-day counter. When the alarm interrupt is enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day. The second alarm is for a day and time of that day.

The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch interrupt is enabled and the counter underflows, an interrupt is generated.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the ADSP-2147x boots at system power-up from an 8-bit EPROM via the external port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOT_CFG2–0) pins in Table 8.

Table 8. Boot Mode Selection

BOOT_CFG2–0[1]	Booting Mode
000	SPI Slave Boot
001	SPI Master Boot
010	AMI User Boot (for 8-bit Flash Boot)
011	Reserved
100	Reserved
1xx	Reserved

[1] The BOOT_CFG2 pin is not available on the 100-pin package.

The "Running Reset" feature is used to reset the processor core and peripherals, but without resetting the PLL and SDRAM controller, or performing a boot. The functionality of the $\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ pin has now been extended to also act as the input for initiating a Running Reset. For more information, see the ADSP-214xx SHARC Processor Hardware Reference.

Power Supplies

The processors have separate power supply connections for the internal (V_{DD_INT}) and external (V_{DD_EXT}), power supplies. The internal and analog supplies must meet the V_{DD_INT} specifications. The external supply must meet the V_{DD_EXT} specification. All external supply pins must be connected to the same power supply.

To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DD_INT} and GND.

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-2147x processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide".

DEVELOPMENT TOOLS

The ADSP-2147x processors are supported with a complete set of CROSSCORE® software and hardware development tools, including Analog Devices emulators and VisualDSP++® development environment. The same emulator hardware that supports other SHARC processors also fully emulates the ADSP-2147x processors.

EZ-KIT Lite Evaluation Board

For evaluation of the processors, use the EZ-KIT Lite® board being developed by Analog Devices. The board comes with on-chip emulation capabilities and is equipped to enable software development. Multiple daughter cards are available.

Designing an Emulator-Compatible DSP Board (Target)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on each JTAG DSP. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

Evaluation Kit

Analog Devices offers a range of EZ-KIT Lite® evaluation platforms to use as a cost effective method to learn more about developing or prototyping applications with Analog Devices processors, platforms, and software tools. Each EZ-KIT Lite includes an evaluation board along with an evaluation suite of the VisualDSP++® development and debugging environment with the C/C++ compiler, assembler, and linker. Also included are sample application programs, power supply, and a USB cable. All evaluation versions of the software tools are limited for use only with the EZ-KIT Lite product.

The USB controller on the EZ-KIT Lite board connects the board to the USB port of the user's PC, enabling the VisualDSP++ evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also allows in-circuit programming of the on-board Flash device to store user-specific boot code, enabling the board to run as a stand-alone unit without being connected to the PC.

With a full version of VisualDSP++ installed (sold separately), engineers can develop software for the EZ-KIT Lite or any custom defined system. Connecting one of Analog Devices JTAG emulators to the EZ-KIT Lite board enables high speed, non-intrusive emulation.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2147x architecture and functionality. For detailed information on the ADSP-2147x family core architecture and instruction set, refer to the *SHARC Processor Programming Reference*.

PIN FUNCTION DESCRIPTIONS

Table 9. Pin Descriptions

Name	Type	State During/ After Reset	Description
$ADDR_{23-0}$	I/O/T (ipu)	High-Z/driven low (boot)	**External Address.** The processor outputs addresses for external memory and peripherals on these pins. The ADDR pins can be multiplexed to support the external memory interface data (I/O), and FLAGS15–8 (I/O) and PWM (O). After reset, all DATA pins are in EMIF mode and FLAG(0–3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the $ADDR_{23-4}$ pins for parallel input data.
$DATA_{15-0}$	I/O/T (ipu)	High-Z	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O), and $FLAGS_{7-0}$ (I/O).
AMI_ACK	I (ipu)		**Memory Acknowledge.** External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0-1}$	O/T (ipu)	High-Z	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory on the AMI interface. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. The $\overline{MS1}$ pin can be used in EPORT/FLASH boot mode. For more information on processor booting, see the *ADSP-214xx SHARC Processor Hardware Reference*.
$\overline{AMI\_RD}$	O/T (ipu)	High-Z	**AMI Port Read Enable.** $\overline{AMI\_RD}$ is asserted whenever the processor reads a word from external memory.
$\overline{AMI\_WR}$	O/T (ipu)	High-Z	**AMI Port Write Enable.** $\overline{AMI\_WR}$ is asserted when the processor writes a word to external memory.
FLAG0/$\overline{IRQ0}$	I/O (ipu)	FLAG[0] INPUT	**FLAG0/Interrupt Request0.**
FLAG1/$\overline{IRQ1}$	I/O (ipu)	FLAG[1] INPUT	**FLAG1/Interrupt Request1.**
FLAG2/$\overline{IRQ2}$/$\overline{MS2}$	I/O (ipu)	FLAG[2] INPUT	**FLAG2/Interrupt Request2/Memory Select2.** This pin is multiplexed with $\overline{MS2}$ in the 196 BGA package only.
FLAG3/TMREXP/$\overline{MS3}$	I/O (ipu)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select3.** This pin is multiplexed with $\overline{MS3}$ in the 196 BGA package only.

The following symbols appear in the Type column of Table 9: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26k–63kΩ. The range of an ipd resistor can be between 31k–85kΩ.
In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.
Not all pins are available in the 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 53 on Page 64.

Table 9. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
$\overline{\text{SDRAS}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Row Address Strobe.** Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDCAS}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Column Address Select.** Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Write Enable.** Connect to SDRAM's WE or W buffer pin.
SDCKE	O/T (ipu)	High-Z/ driven high	**SDRAM Clock Enable.** Connect to SDRAM's CKE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T (ipu)	High-Z/ driven high	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with non-SDRAM accesses. This pin replaces the DSP's A10 pin only during SDRAM accesses.
SDDQM	O/T (ipu)	High-Z/ driven high	**DQM Data Mask.** SDRAM Input mask signal for write accesses and ADSP-2147x output enable signal for read accesses. Input data is masked when DQM is sampled high during a write cycle. The output buffers are placed in a High-Z state when DQM is sampled high during a read cycle.
SDCLK	O/T (ipd)	High-Z/ driving	**SDRAM Clock Output.** Clock driver for this pin differs from all other clock drivers. See Figure 49 on page 61.
DAI _$P_{20–1}$	I/O/T (ipu)	High-Z	**Digital Applications Interface**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audiocentric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins. The DAI SRU provides the connection from the serial ports, the S/PDIF module, input data ports (2), and the precision clock generators (4), to the DAI_P20–1 pins.
DPI _$P_{14–1}$	I/O/T (ipu)	High-Z	**Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins. The DPI SRU provides the connection from the timers (2), SPIs (2), UART (1), flags (12), and general-purpose I/O (9) to the DPI_P14–1 pins.
WDT_CLKIN	I		**Watch Dog Timer Clock Input.** This pin should be pulled low when not used.
WDT_CLKO	O		**Watch Dog Resonator Pad Output.**
$\overline{\text{WDTRSTO}}$	O (ipu)		**Watch Dog Timer Reset Out.**
THD_P	I		**Thermal Diode Anode.** When not used, this pin can be left floating.
THD_M	O		**Thermal Diode Cathode.** When not used, this pin can be left floating.

The following symbols appear in the Type column of Table 9: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26k–63kΩ. The range of an ipd resistor can be between 31k–85kΩ.
In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.
Not all pins are available in the 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 53 on Page 64.

Table 9. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
MLBCLK[1]	I		**Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface at 49.152 MHz at Fs=48 kHz. When the MLB controller is not used, this pin should be grounded.
MLBDAT[3]	I/O/T in 3 pin mode. I in 5 pin mode.	High-Z	**Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin is an input only. When the MLB controller is not used, this pin should be grounded.
MLBSIG[3]	I/O/T in 3 pin mode. I in 5 pin mode	High-Z	**Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin is input only. When the MLB controller is not used, this pin should be grounded.
MLBDO[3]	O/T	High-Z	**Media Local Bus Data Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output data pin in 5-pin mode. When the MLB controller is not used, this pin can be left floating.
MLBSO[3]	O/T	High-Z	**Media Local Bus Signal Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output signal pin in 5-pin mode. When the MLB controller is not used, this pin can be left floating.
SR_SCLK	I (ipu)		**Shift Register Serial Clock.** (Active high, rising edge sensitive)
$\overline{\text{SR\_CLR}}$	I (ipu)		**Shift Register Reset.** (Active LOW)
SR_SDI	I (ipu)		**Shift Register Serial Data Input.**
SR_SDO	O (ipu)		**Shift Register Serial Data Output.**
SR_LAT	I (ipu)		**Shift Register Latch Clock Input.** (Active high, rising edge sensitive)
SR_LDO_{17-0}	O/T (ipu)		**Shift Register Parallel Data Output.**
RTXI	I		**RTC Crystal Input.**
RTXO	O		**RTC Crystal Output.**
RTCLKOUT	O (ipd)		**RTC Clock Output.** For calibration purposes. The clock runs at 1 Hz.
TDI	I (ipu)		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic.
TDO	O/T	High-Z	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (ipu)		**Test Mode Select (JTAG).** Used to control the test state machine.
TCK	I		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the device.
$\overline{\text{TRST}}$	I (ipu)		**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor.
$\overline{\text{EMU}}$	O/T (ipu)	High-Z	**Emulation Status.** Must be connected to the ADSP-2147x Analog Devices DSP Tools product line of JTAG emulators target board connector only.

The following symbols appear in the Type column of Table 9: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26k–63kΩ. The range of an ipd resistor can be between 31k–85kΩ.
In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.
Not all pins are available in the 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 53 on Page 64.

Table 9. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
CLK_CFG_{1-0}	I		**Core to CLKIN Ratio Control.** These pins set the start up clock frequency. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset. The allowed values are: 00 = 8:1 01 = 32:1 10 = 16:1 11 = reserved
CLKIN	I		**Local Clock In.** Used in conjunction with XTAL. CLKIN is the clock input. It configures the processors to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processors to use the external clock source such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency.
XTAL	O		**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.
$\overline{\text{RESET}}$	I		**Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
$\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$	I/O (ipu)		**Reset Out/Running Reset In.** The default setting on this pin is reset out. This pin also has a second function as RUNRSTIN which is enabled by setting bit 0 of the RUNRSTCTL register. For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*.
$BOOT\_CFG_{2-0}$	I		**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOT_CFG pins must be valid before $\overline{\text{RESET}}$ (hardware and software) is de-asserted. Note that the BOOT_CFG2 pin is not available on the 100-lead LQFP package.

The following symbols appear in the Type column of Table 9: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26k–63kΩ. The range of an ipd resistor can be between 31k–85kΩ.
In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.
Not all pins are available in the 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 53 on Page 64.

[1] The MLB pins are only available on the ADSP-21479W automotive processor.

Table 10. Pin List, Power and Ground

Name	Type	Description
V_{DD_INT}	P	**Internal Power Supply.**
V_{DD_EXT}	P	**I/O Power Supply.**
V_{DD_RTC}	P	**Real Time Clock Power Supply.**
GND[1]	G	**Ground.**
V_{DD_THD}	P	**Thermal Diode Power Supply**. When not used, this pin can be left floating.

[1] The exposed pad is required to be electrically and thermally connected to GND. Implement this by soldering the exposed pad to a GND PCB land that is the same size as the exposed pad. The GND PCB land should be *robustly* connected to the GND plane in the PCB for best electrical and thermal performance. No separate GND pins are provided in the package.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	100 MHz		266 MHz		Unit
		Min	Max	Min	Max	
V_{DD_INT}[2]	Internal (Core) Supply Voltage	TBD	TBD	TBD	TBD	V
V_{DD_EXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	V
V_{DD_THD}	Thermal Diode Supply Voltage	3.13	3.47	3.13	3.47	V
V_{DD_RTC}[3]	Real-Time Clock Power Supply Voltage	TBD	TBD	TBD	TBD	V
V_{IH}[4]	High Level Input Voltage @ V_{DD_EXT} = Max	2.0	V_{DD_EXT} + 0.5	2.0	V_{DD_EXT} + 0.5	V
V_{IL}[4]	Low Level Input Voltage @ V_{DD_EXT} = Min	–0.3	0.8	–0.3	0.8	V
V_{IH_CLKIN}[5]	High Level Input Voltage @ V_{DD_EXT} = Max	TBD	TBD	TBD	TBD	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DD_EXT} = Max	TBD	TBD	TBD	TBD	V
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	0	TBD	0	TBD	°C
T_J[6]	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	–40	TBD	–40	TBD	°C
T_J	Junction Temperature 196-Ball CSP_BGA @ $T_{AMBIENT}$ 0°C to +70°C	0	TBD	0	TBD	°C

[1] Specifications subject to change without notice.
[2] The expected value is 1.2V +/-50 mV and initial designs should use a programmable regulator that can be adjusted from 0.95 V to 1.26 V.
[3] The expected voltage is = to V_{DD_EXT}.
[4] Applies to input and bidirectional pins: ADDR23–0, DATA15–0, FLAG3–0, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{\text{RUNRSTIN}}$, $\overline{\text{RESET}}$, TCK, TMS, TDI, $\overline{\text{TRST}}$.
[5] Applies to input pin CLKIN.
[6] Applies to automotive models only. See Automotive Products on Page 69

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	100 MHz			266 MHz			Unit
			Min	Typical	Max	Min	Typical	Max	
V_{OH}[2]	High Level Output Voltage	@ V_{DD_EXT} = Min, I_{OH} = –1.0 mA[3]	2.4			2.4			V
V_{OL}[2]	Low Level Output Voltage	@ V_{DD_EXT} = Min, I_{OL} = 1.0 mA[3]			0.4			0.4	V
I_{IH}[4, 5]	High Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max			10			10	µA
I_{IL}[4]	Low Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V			–10			–10	µA
I_{ILPU}[5]	Low Level Input Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V			TBD			TBD	µA
I_{OZH}[6, 7]	Three-State Leakage Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max			10			10	µA
I_{OZL}[6]	Three-State Leakage Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V			–10			–10	µA
I_{OZLPU}[7]	Three-State Leakage Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V			TBD			TBD	µA
$I_{DD\text{-}INTYP}$[8, 9]	Supply Current (Internal)	TBD			TBD			TBD	mA
C_{IN}[10, 11]	Input Capacitance	TBD			TBD			TBD	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: ADDR23-0, DATA15-0, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, FLAG3–0, DAI_Px, DPI_Px, $\overline{\text{EMU}}$, TDO, $\overline{\text{RESETOUT}}$.
[3] See Output Drive Currents on Page 61 for typical drive current capabilities.
[4] Applies to input pins: BOOT_CFGx, CLK_CFGx, TCK, $\overline{\text{RESET}}$, CLKIN.
[5] Applies to input pins with internal pull-ups: $\overline{\text{TRST}}$, TMS, TDI.
[6] Applies to three-statable pins: TDO, MLBDAT, MLBSIG, MLBDO, and MLBSO.
[7] Applies to three-statable pins with pull-ups: DAI_Px, DPI_Px, $\overline{\text{EMU}}$.
[8] Typical internal current data reflects nominal operating conditions.
[9] See Engineer-to-Engineer Note “Estimating Power Dissipation for ADSP-2147x SHARC Processors” for further information.
[10] Applies to all signal pins.
[11] Guaranteed, but not tested.

PACKAGE INFORMATION

The information presented in Figure 4 provides details about the package branding for the ADSP-2147x processors. For a complete listing of product availability, see Ordering Guide on Page 69.

Figure 4. Typical Package Brand

Table 11. Package Brand Information[1]

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Option
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Non Automotive only. For branding information specific to Automotive products, contact Analog Devices Inc.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM POWER DISSIPATION

See Engineer-to-Engineer Note "Estimating Power Dissipation for ADSP-2147x SHARC Processors" for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 62.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 12 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 12. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD_INT})	–0.3 V to +1.32V
Analog (PLL) Supply Voltage (V_{DD_A})	–0.3 V to +1.15V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.3 V to +4.6V
Thermal Diode Supply Voltage (V_{DD_THD})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to +3.8V
Output Voltage Swing	–0.5 V to V_{DD_EXT} +0.5V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 51 on page 61 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 5). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Voltage Controlled Oscillator

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 15.

- The product of CLKIN and PLLM must never exceed 1/2 of f_{VCO} (max) in Table 15 if the input divider is not enabled (INDIV = 0).
- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 15 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$f_{VCO} = 2 \times PLLM \times f_{INPUT}$
$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div PLLD$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = 2, 4, 8, or 16 based on the divider value programmed on the PMCTL register. During reset this value is 2.

f_{INPUT} = is the input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in and Table 13. All of the timing specifications for the ADSP-2147x peripherals are defined in relation to t_{PCLK}. See the peripheral specific section for each peripheral's timing information.

Table 13. Clock Periods

Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}
t_{SDCLK}	SDRAM Clock Period = (t_{CCLK}) × SDCKR

Figure 5 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*.

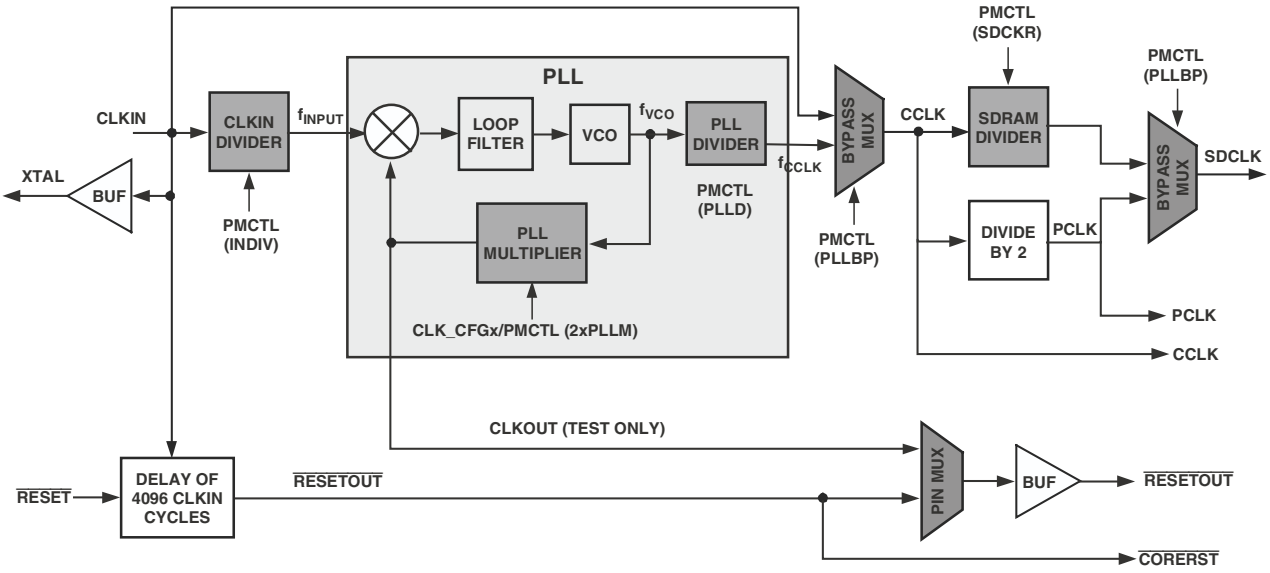


Figure 5. Core Clock and System Clock Relationship to CLKIN

Power-Up Sequencing

The timing requirements for processor startup are given in Table 14. While no specific power-up sequencing is required between V_{DD_EXT} and V_{DD_INT}, there are some considerations that the system designs should take into account.

- No power supply should be powered up for an extended period of time (> 200 ms) before another supply starts to ramp up.
- If the V_{DD_INT} power supply comes up after V_{DD_EXT}, any pin, such as $\overline{\text{RESETOUT}}$ and $\overline{\text{RESET}}$ may actually drive momentarily until the V_{DD_INT} rail has powered up. Systems sharing these signals on the board must determine if there are any issues that need to be addressed based on this behavior.

Note that during power-up, when the V_{DD_INT} power supply comes up after V_{DD_EXT}, a leakage current of the order of three-state leakage current pull-up, pull-down, may be observed on any pin, even if that is an input only (for example the $\overline{\text{RESET}}$ pin) until the V_{DD_INT} rail has powered up.

Table 14. Power Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DD_EXT} or V_{DD_INT} On	0		ms
$t_{IVDDEVDD}$	V_{DD_INT} On Before V_{DD_EXT}	TBD		ms
t_{CLKVDD} [1]	CLKIN Valid After V_{DD_INT} and V_{DD_EXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10 [2]		ms
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20 [3]		ms
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096 \times t_{CK} + 2 \times t_{CCLK}$ [4, 5]		ms

[1] Valid V_{DD_INT} and V_{DD_EXT} assumes that the supplies are fully ramped to their nominal values (it does not matter which supply comes up first). Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on t_{SRST} specification in Table 16. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

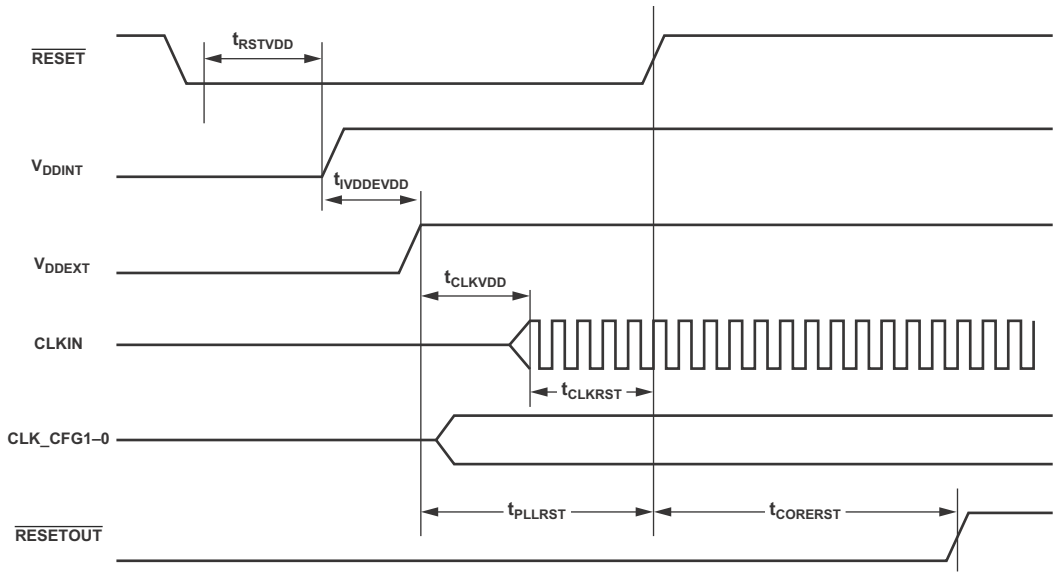


Figure 6. Power-Up Sequencing

Clock Input

Table 15. Clock Input

Parameter		100 MHz Min	100 MHz Max	266 MHz Min	266 MHz Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period	TBD[1]	TBD[2]	22.5[1]	100[2]	ns
t_{CKL}	CLKIN Width Low	TBD	TBD	11.25	45	ns
t_{CKH}	CLKIN Width High	TBD	TBD	11.25	45	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		TBD		6	ns
t_{CCLK}[3]	CCLK Period	10	TBD	3.75	10	ns
f_{VCO}[4]	VCO Frequency	TBD	200	200	533	MHz
t_{CKJ}[5, 6]	CLKIN Jitter Tolerance	–250	+250	–250	+250	ps

[1] Applies only for CLKCFG1–0 = 00 and default values for PLL control bits in PMCTL.
[2] Applies only for CLKCFG1–0 = 01 and default values for PLL control bits in PMCTL.
[3] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[4] See Figure 5 on page 22 for VCO diagram.
[5] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[6] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

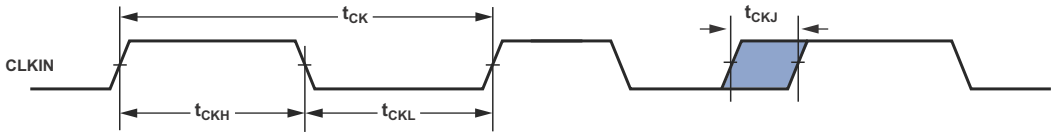


Figure 7. Clock Input

Clock Signals

The ADSP-2147x can use an external clock or a crystal. See the CLKIN pin description in Table 9. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 8 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 16.67 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 266 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

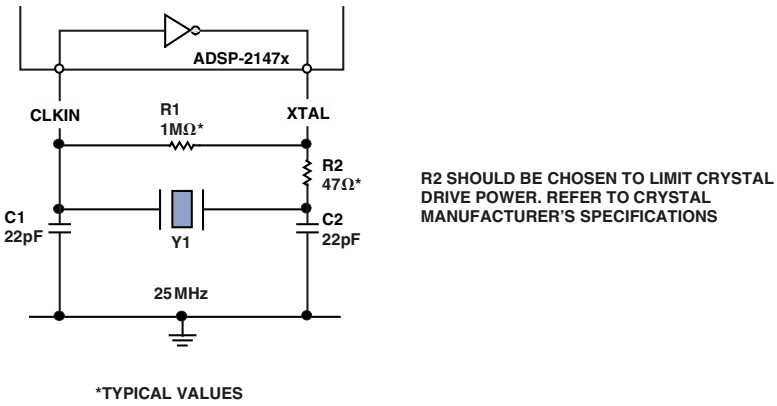


Figure 8. 266 MHz Operation (Fundamental Mode Crystal)

Reset

Table 16. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	4 × t_{CK}		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

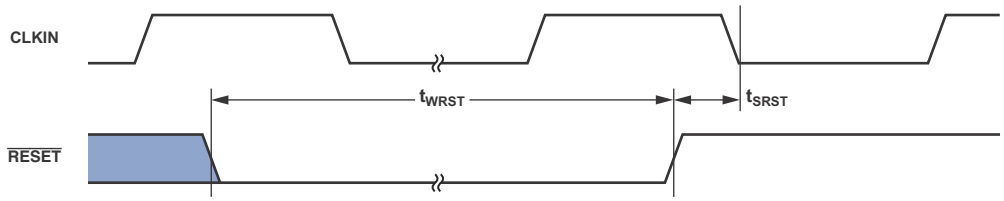


Figure 9. Reset

Running Reset

The following timing specification applies to $\overline{\text{RESET-OUT/RUNRSTIN}}$ pin when it is configured as $\overline{\text{RUNRSTIN}}$.

Table 17. Running Reset

Parameter		Min	Max	Unit
Timing Requirements				
$t_{WRUNRST}$	Running $\overline{\text{RESET}}$ Pulse Width Low	4 × t_{CK}		ns
$t_{SRUNRST}$	Running $\overline{\text{RESET}}$ Setup Before CLKIN High	8		ns

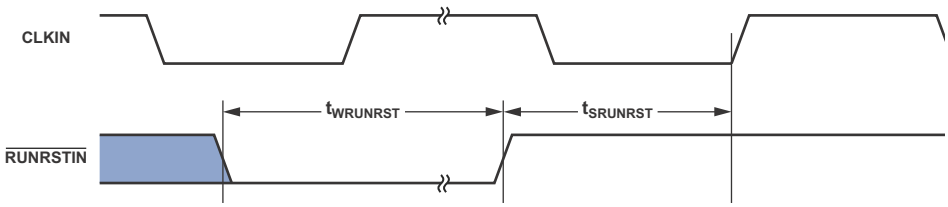


Figure 10. Running Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts as well as the DAI_P20-1 and DPI_P14-1 pins when they are configured as interrupts.

Table 18. Interrupts

Parameter		Min	Max	Unit
Timing Requirement				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{PCLK} + 2$		ns

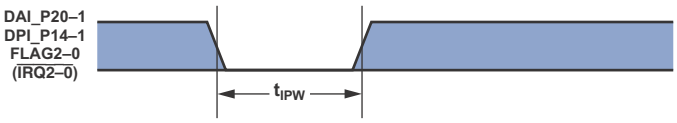


Figure 11. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 19. Core Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{WCTIM}	TMREXP Pulse Width	$4 \times t_{PCLK} - 1$		ns

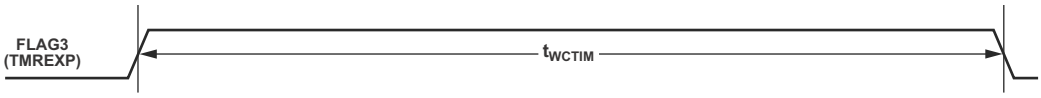


Figure 12. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to timer0 and timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 20. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

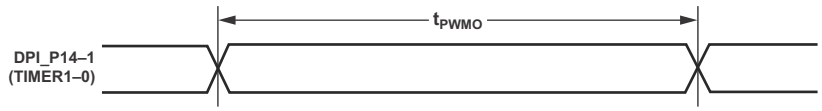


Figure 13. Timer PWM_OUT Timing

Timer WDTH_CAP Timing

The following timing specification applies to timer0 and timer1, and in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specification provided below is valid at the DPI_P14–1 pins.

Table 21. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

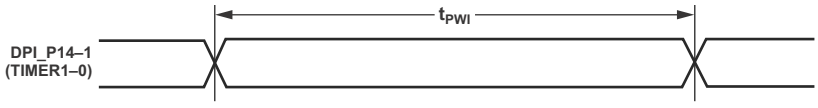


Figure 14. Timer Width Capture Timing

Watch Dog Timer Timing

Table 22. Watch Dog Timer Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{RST}	WDT Clock Rising Edge To Watch Dog Timer $\overline{\text{RESET}}$ Falling Edge	3.7059	6.418	ns
t_{RSTPW}	Reset Pulse Width	$64 \times t_{WDTCLKPER}$		ns

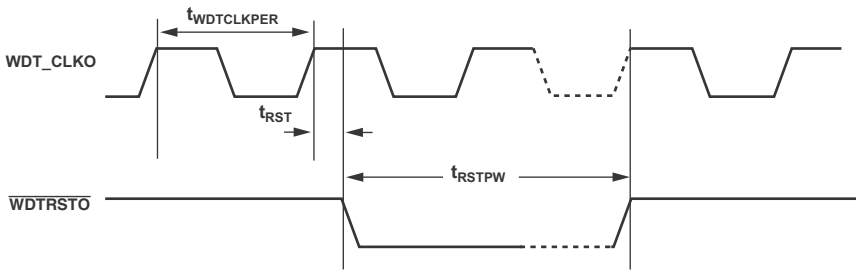


Figure 15. Watch Dog Timer Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example DAI_PB01_I to DAI_PB02_O).

Table 23. DAI/DPI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	10	ns

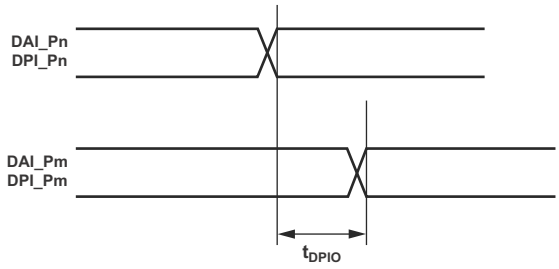


Figure 16. DAI Pin to Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

Table 24. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIW}	Input Clock Period	$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

D = FSxDIV, PH = FSxPHASE. For more information, see the ADSP-214xx SHARC Processor Hardware Reference, "Precision Clock Generators" chapter.

[1] Normal mode of operation.

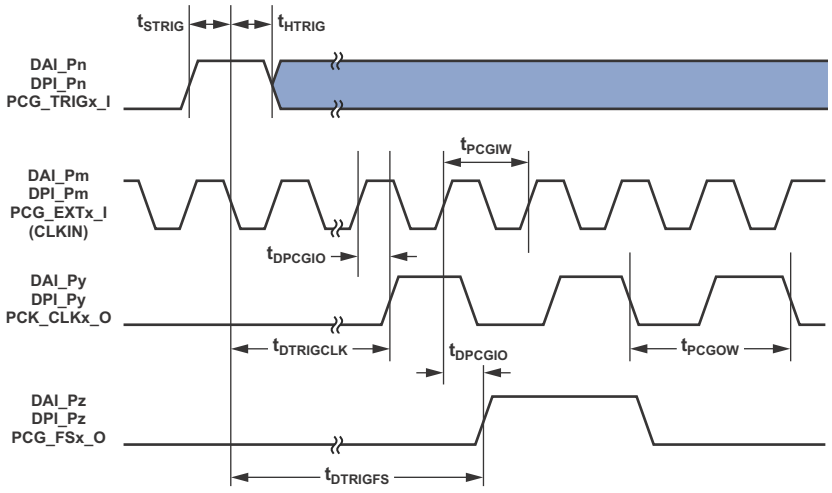


Figure 17. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to ADDR23–0 and DATA7–0 when configured as FLAGS. See Table 9 on Page 14 for more information on flag use.

Table 25. Flags

Parameter		Min	Max	Unit
Timing Requirement				
t_{FIPW}	FLAGs IN Pulse Width[1]	$2 \times t_{PCLK} + 3$		ns
Switching Characteristic				
t_{FOPW}	FLAGs OUT Pulse Width[1]	$2 \times t_{PCLK} - 1.5$		ns

[1] This is applicable when the Flags are connected to DPI_P14–1, ADDR23–0, DATA7–0 and FLAG3–0 pins.

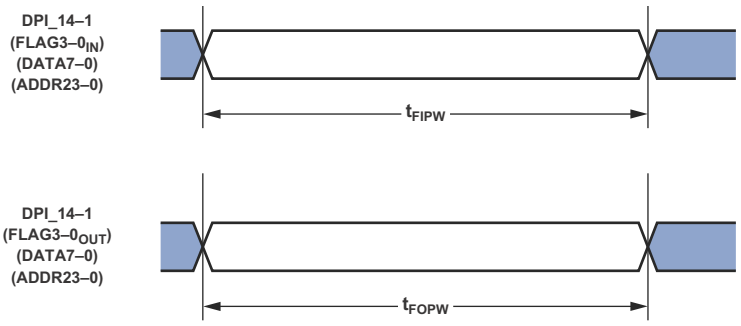


Figure 18. Flags

SDRAM Interface Timing (133 MHz SDCLK)

The 133 MHz access speed is for a single processor. The processor needs to be programmed in $t_{SDCLK} = 2.0 \times t_{CCLK}$ mode when operated at 266 MHz.

Table 26. SDRAM Interface Timing[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDAT}	DATA Setup Before SDCLK	500		ps
t_{HSDAT}	DATA Hold After SDCLK	1.23		ns
Switching Characteristics				
t_{SDCLK}	SDCLK Period	7.5		ns
t_{SDCLKH}	SDCLK Width High	2.6		ns
t_{SDCLKL}	SDCLK Width Low	2.6		ns
t_{DCAD}	Command, ADDR, Data Delay After SDCLK[2]		4.8	ns
t_{HCAD}	Command, ADDR, Data Hold After SDCLK[2]	1.2		ns
t_{DSDAT}	Data Disable After SDCLK		5.3	ns
t_{ENSDAT}	Data Enable After SDCLK	1.3		ns

[1] For f_{CCLK} = 266 MHz (core clock to SDCLK ratio = 1:2).
[2] Command pins include: $\overline{SDCAS}$, $\overline{SDRAS}$, $\overline{SDWE}$, $\overline{MSx}$, SDA10, SDCKE, and DQM.

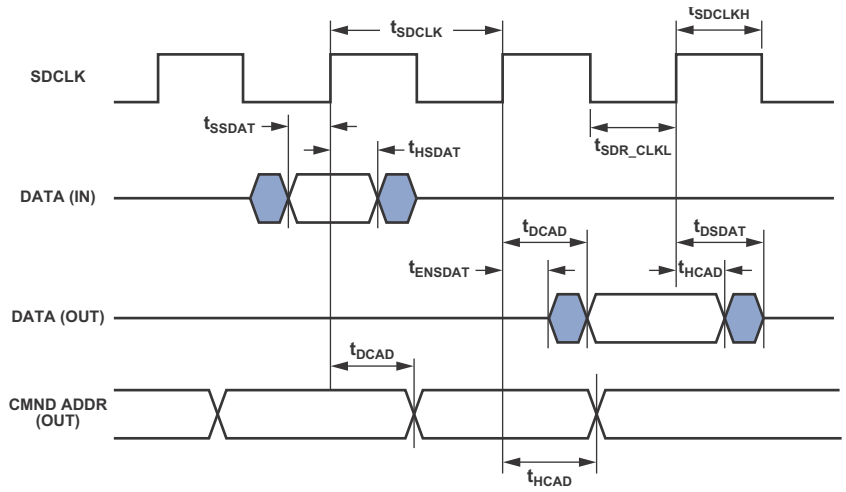


Figure 19. SDRAM Interface Timing

SDRAM Interface Enable/Disable Timing (133 MHz SDCLK)

Table 27. SDRAM Interface Enable/Disable Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DSDC}	Command Disable After CLKIN Rise		$2 \times t_{PCLK} + 3$	ns
t_{ENSDC}	Command Enable After CLKIN Rise	4.0		ns
t_{DSDCC}	SDCLK Disable After CLKIN Rise		8.5	ns
t_{ENSDCC}	SDCLK Enable After CLKIN Rise	3.8		ns
t_{DSDCA}	Address Disable After CLKIN Rise		9.2	ns
t_{ENSDCA}	Address Enable After CLKIN Rise	$2 \times t_{PCLK} - 4$	$4 \times t_{PCLK}$	ns

[1] For f_{CCLK} = 266 MHz (core clock to SDCLK ratio = 1:2).

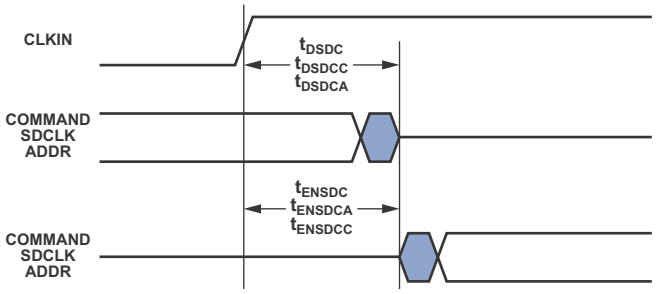


Figure 20. SDRAM Interface Enable/Disable Timing

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 28. Memory Read—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		W + t_{SDCLK} – 5.12	ns
t_{DRLD}	$\overline{\text{AMI\_RD}}$ Low to Data Valid[1]		W – 3	ns
t_{SDS}	Data Setup to $\overline{\text{AMI\_RD}}$ High[3, 4]	2.2		ns
t_{HDRH}	Data Hold from $\overline{\text{AMI\_RD}}$ High	0		ns
t_{DAAK}	AMI_ACK Delay from Address, Selects[2, 5]		t_{SCDCLK} – 10. + W	ns
t_{DSAK}	AMI_ACK Delay from $\overline{\text{AMI\_RD}}$ Low[4]		W – 7.0	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{\text{AMI\_RD}}$ High	RHC+ 0.38		ns
t_{DARL}	Address Selects to $\overline{\text{AMI\_RD}}$ Low[2]	t_{SDCLK} – 3.3		ns
t_{RW}	$\overline{\text{AMI\_RD}}$ Pulse Width	W – 1.4		ns
t_{RWR}	$\overline{\text{AMI\_RD}}$ High to $\overline{\text{AMI\_RD}}$ Low[6]	HI + t_{SDCLK} – 0.8		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
HI = RHC + IC (RHC = (number of Read Hold Cycles specified in AMICTLx register) x t_{SDCLK}
IC = (number of idle cycles specified in AMICTLx register) x t_{SDCLK}).
H = (number of hold cycles specified in AMICTLx register) x t_{SDCLK}.

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{\text{MS}}$x, is referenced.
[3] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[4] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions on Page 61 for the calculation of hold times given capacitive and dc loads.
[5] AMI_ACK delay/setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low). For asynchronous assertion of AMI_ACK (high) user must meet t_{DAAK} or t_{DSAK}.
[6] For Read to Read: Same bank = (1 + RHC) × SDCLK if IC is not programmed. For Read to Read: Different bank = tRWR. For Read to Write: 5 SDCLK cycles + (IC – 4), at least 5 SDCLK cycles for both the same bank and different banks.

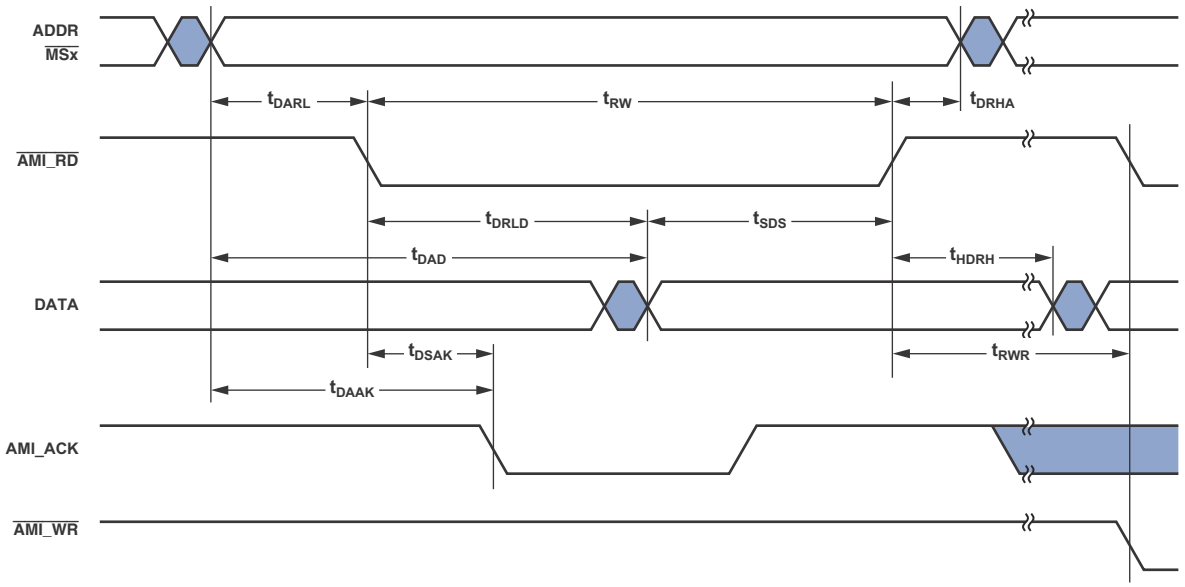


Figure 21. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 29. Memory Write—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	AMI_ACK Delay from Address, Selects[1, 2]		t_{SDCLK} – 10.1 + W	ns
t_{DSAK}	AMI_ACK Delay from $\overline{\text{AMI\_WR}}$ Low[1, 3]		W – 7.1	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{\text{AMI\_WR}}$ Deasserted[2]	t_{SDCLK} – 3.6 + W		ns
t_{DAWL}	Address, Selects to $\overline{\text{AMI\_WR}}$ Low[2]	t_{SDCLK} – 2.7		ns
t_{WW}	$\overline{\text{AMI\_WR}}$ Pulse Width	W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{\text{AMI\_WR}}$ High	t_{SDCLK} – 3.0 + W		ns
t_{DWHA}	Address Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H + 0.15		ns
t_{DWHD}	Data Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H + 0.02		ns
t_{DATRWH}	Data Disable After $\overline{\text{AMI\_WR}}$ Deasserted[4]	t_{SDCLK} – 1.37 + H	t_{SDCLK} + 4.9 + H	ns
t_{WWR}	$\overline{\text{AMI\_WR}}$ High to $\overline{\text{AMI\_WR}}$ Low[5]	t_{SDCLK} – 1.5 + H		ns
t_{DDWR}	Data Disable Before $\overline{\text{AMI\_RD}}$ Low	2 × t_{SDCLK} – 5.1		ns
t_{WDE}	$\overline{\text{AMI\_WR}}$ Low to Data Enabled	t_{SDCLK} – 4.1		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}
H = (number of hold cycles specified in AMICTLx register) x t_{SDCLK}

[1] AMI_ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low). For asynchronous assertion of AMI_ACK (high) user must meet t_{DAAK} or t_{DSAK}.
[2] The falling edge of $\overline{\text{AMI\_MSx}}$ is referenced.
[3] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions on Page 61 for calculation of hold times given capacitive and dc loads.
[5] For Write to Write: 1 + HC, for both same bank and different bank. For Write to Read: 3 SDCLK cycles + HC , for the same bank and different banks.

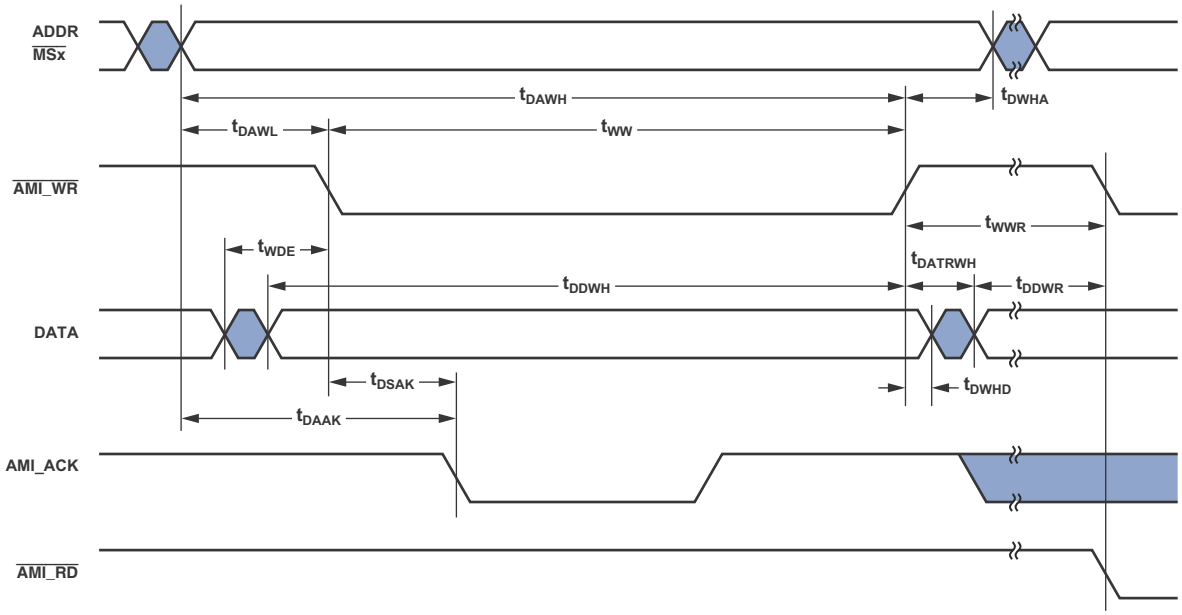


Figure 22. Memory Write—Bus Master

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals (SCLK, FS, Data Channel A, Data Channel B) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 30. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	2.5		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 0.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)		10.5	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)	2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		11	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 31. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
T_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	7		ns
T_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
T_{SDRI}[1]	Receive Data Setup Before SCLK	7		ns
T_{HDRI}[1]	Receive Data Hold After SCLK	2.5		ns
Switching Characteristics				
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		4	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1.0		ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		10.7	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3.6	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		ns
t_{SCKLIW}	Transmit or Receive SCLK Width	$0.5 \times t_{PCLK} - 2$	$0.5 \times t_{PCLK} + 2$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

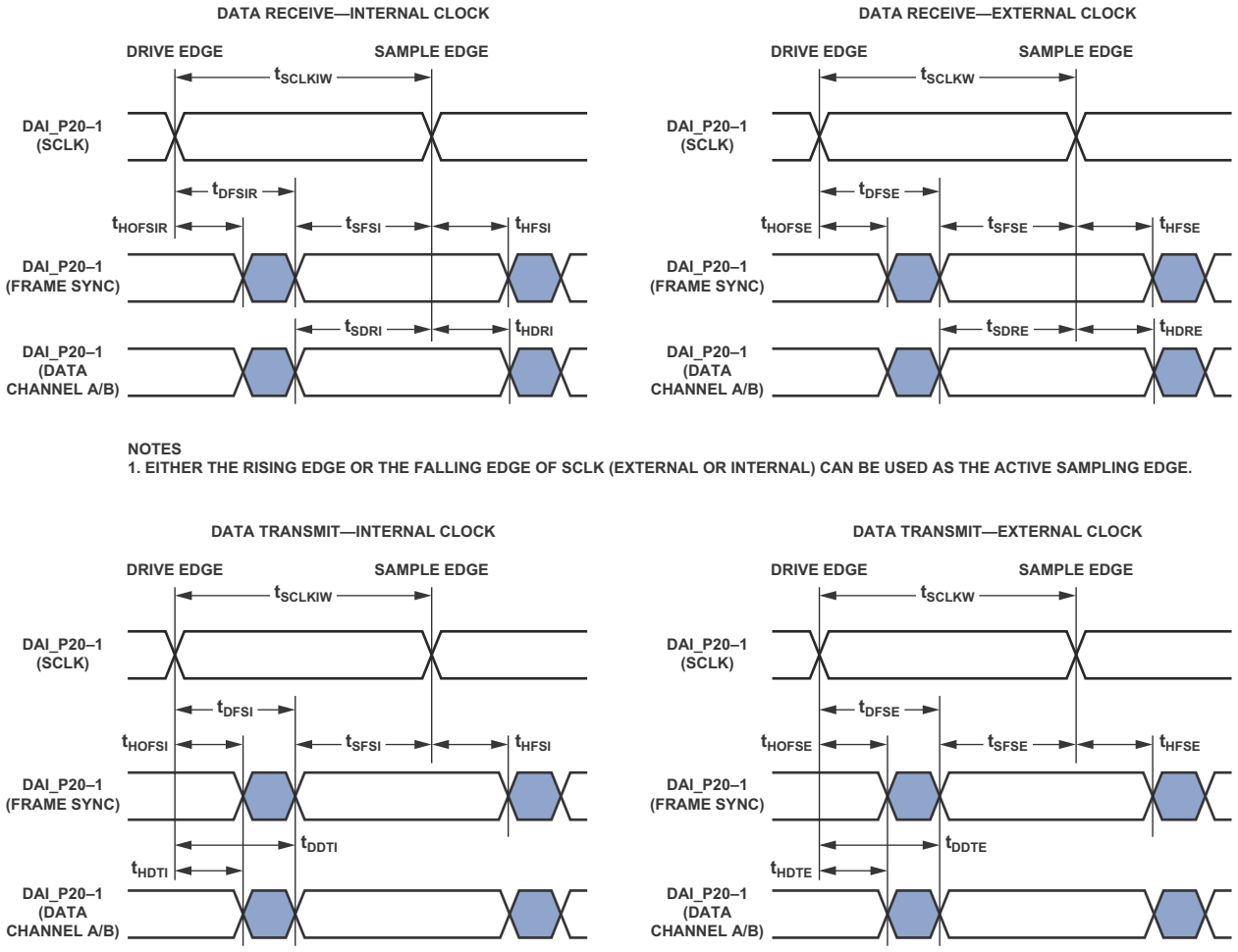


Figure 23. Serial Ports

Table 32. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0		10	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified as well as DSP serial mode, and MCE = 1, MFD = 0.

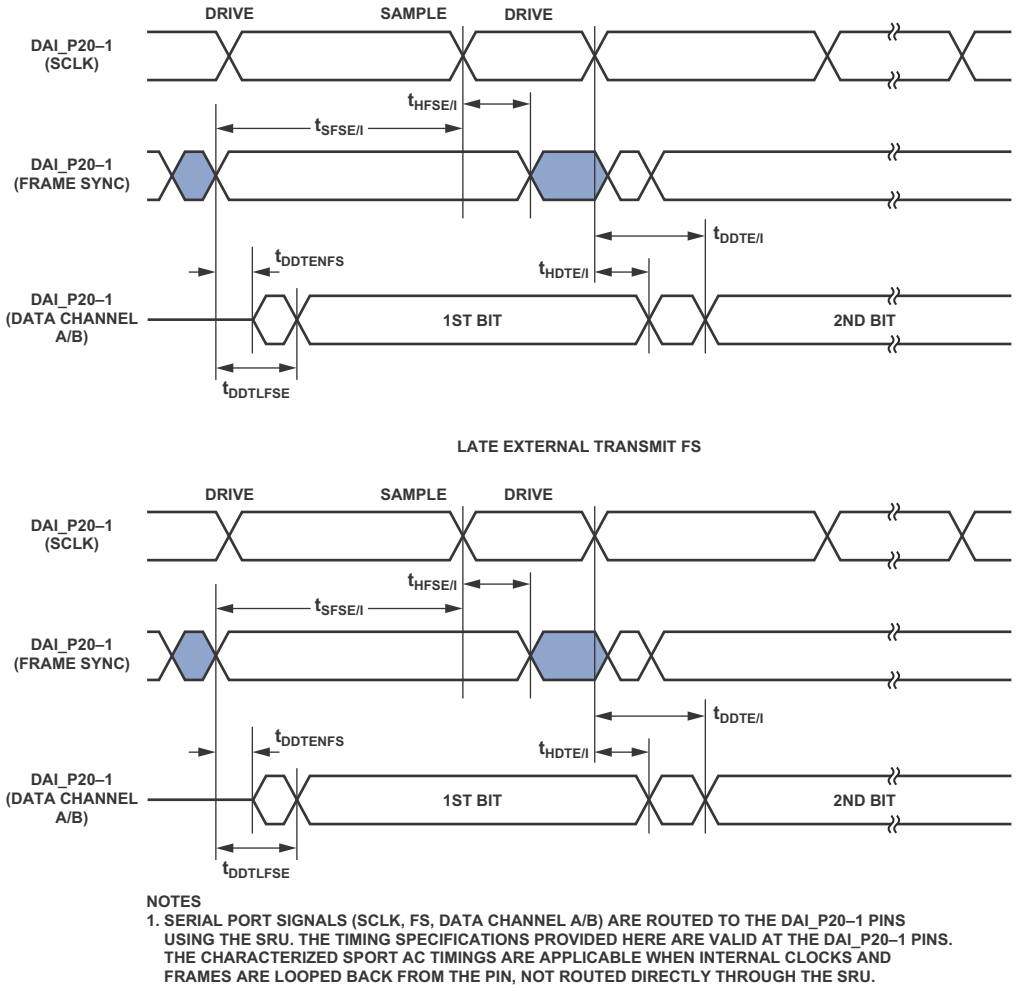


Figure 24. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified mode.

Table 33. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		10	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	–1		ns

[1] Referenced to drive edge.

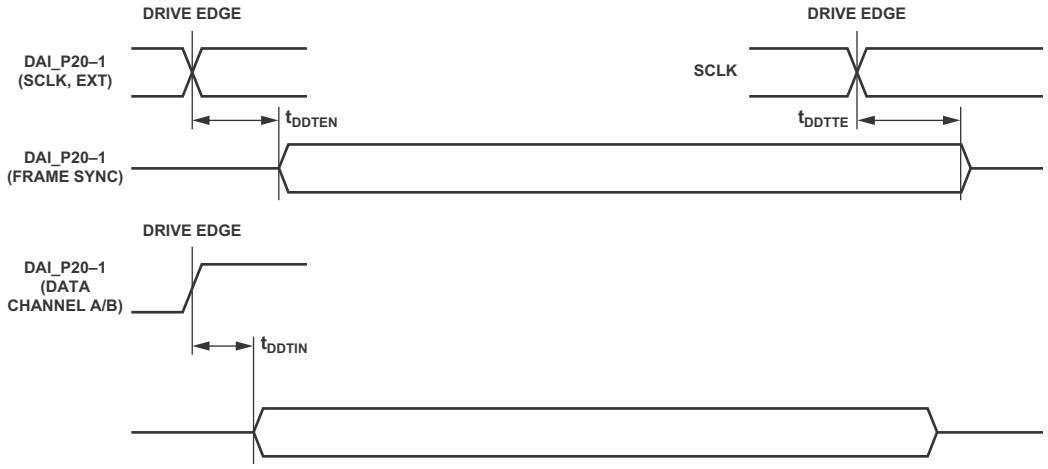


Figure 25. Enable and Three-State

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 34. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 34. Input Data Port (IDP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3.8		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	2.5		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	2.5		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

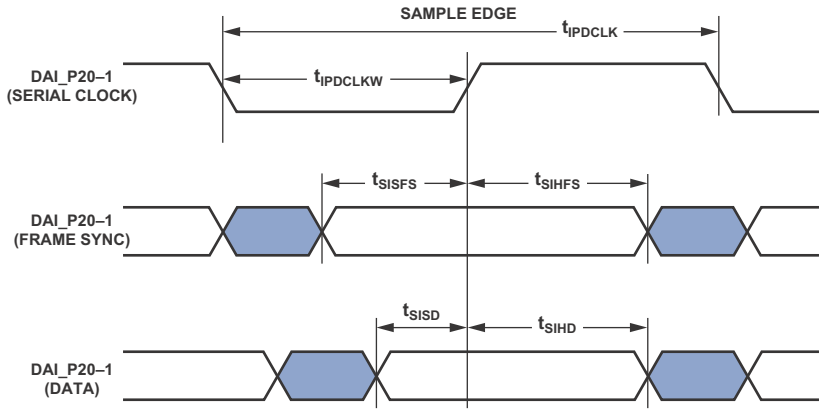


Figure 26. IDP Master Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 35. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the *ADSP-214xx SHARC Processor Hardware Reference*. Note that the 20-bits of external PDAP data can be provided through the ADDR23–0 pins or over the DAI pins.

Table 35. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPHOLD}[1]	PDAP_HOLD Setup Before PDAP_CLK Sample Edge	2.5		ns
t_{HPHOLD}[1]	PDAP_HOLD Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge	3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge	2.5		ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$		ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1$		ns

[1] Source pins of DATA and control are ADDR23–0 or DAI pins. Source pins for SCLK and FS are: 1) DAI pins, 2) CLKIN through PCG, or 3) DAI pins through PCG.

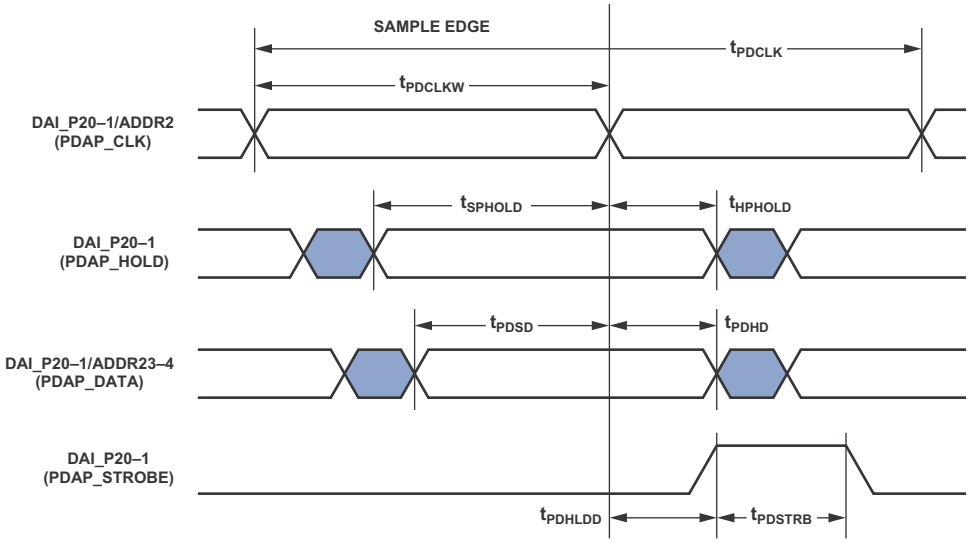


Figure 27. PDAP Timing

Sample Rate Converter—Serial Input Port

The ASRC input signals are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 36 are valid at the DAI_P20–1 pins.

Table 36. ASRC, Serial Input Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	TBD		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	TBD		ns
t_{SRCSD}[1]	Data Setup Before Serial Clock Rising Edge	TBD		ns
t_{SRCHD}[1]	Data Hold After Serial Clock Rising Edge	TBD		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

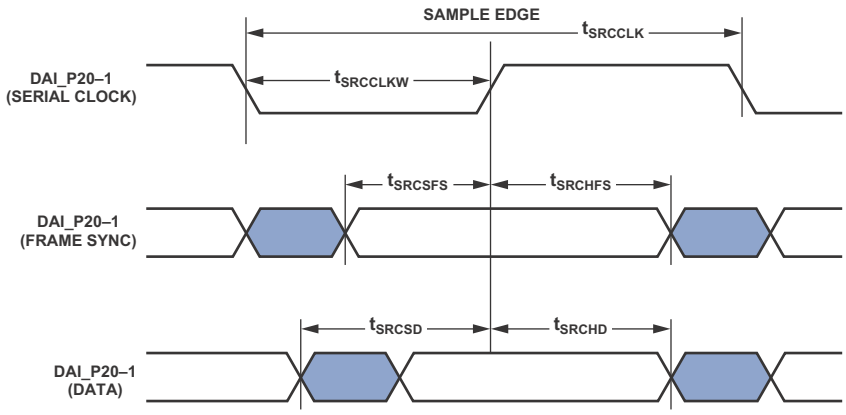


Figure 28. ASRC Serial Input Port Timing

Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and it should meet setup and hold times with regard to the serial clock on the output port. The serial data output has a hold time and delay specification with regard to serial clock. Note that serial clock rising edge is the sampling edge and the falling edge is the drive edge.

Table 37. ASRC, Serial Output Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	TBD		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	TBD		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{SRCTDD}[1]	Transmit Data Delay After Serial Clock Falling Edge		TBD	ns
t_{SRCTDH}[1]	Transmit Data Hold After Serial Clock Falling Edge	TBD		ns

[1] The serial clock, data and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

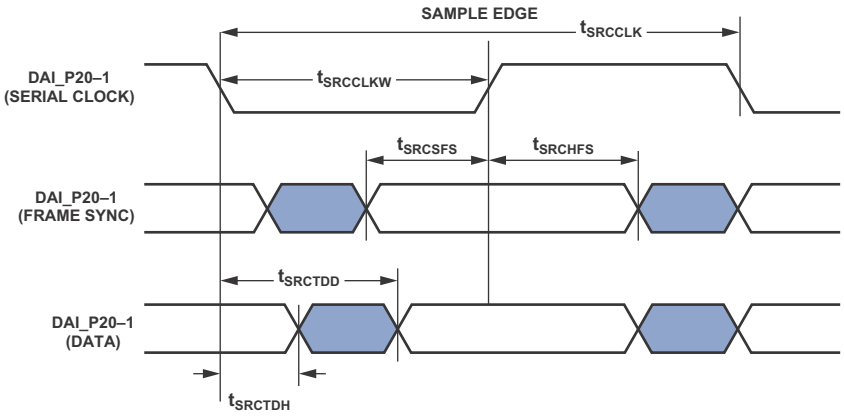


Figure 29. ASRC Serial Output Port Timing

Pulse-Width Modulation Generators (PWM)

The following timing specifications apply when the ADDR23–8/DPI_14–1 pins are configured as PWM.

Table 38. Pulse-Width Modulation (PWM) Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2$	$(2^{16} - 2) \times t_{PCLK} - 2$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 1.5$	$(2^{16} - 1) \times t_{PCLK} - 1.5$	ns

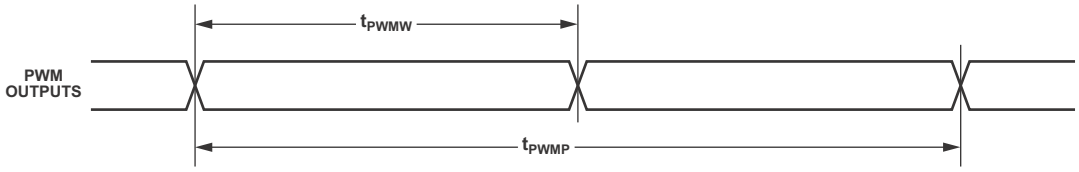


Figure 30. PWM Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I²S, or right justified with word widths of 16-, 18-, 20-, or 24-bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 31 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 Serial clock periods per LRCLK period, the LSB of the data will be right-justified to the next LRCLK transition.

Figure 32 shows the default I²S-justified mode. LRCLK is low for the left channel and HI for the right channel. Data is valid on the rising edge of Serial Clock. The MSB is left-justified to an LRCLK transition but with a single Serial Clock period delay.

Figure 33 shows the left-justified mode. LRCLK is high for the left channel and LO for the right channel. Data is valid on the rising edge of Serial Clock. The MSB is left-justified to an LRCLK transition with no MSB delay.

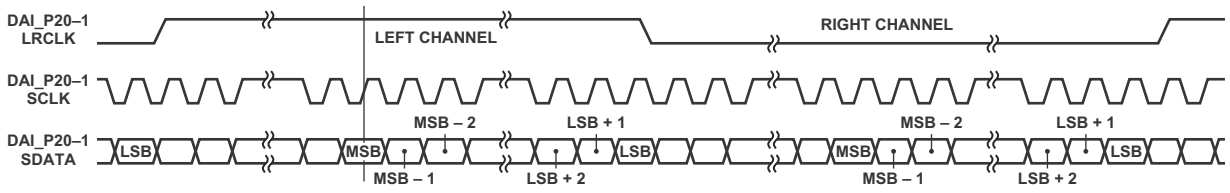


Figure 31. Right-Justified Mode

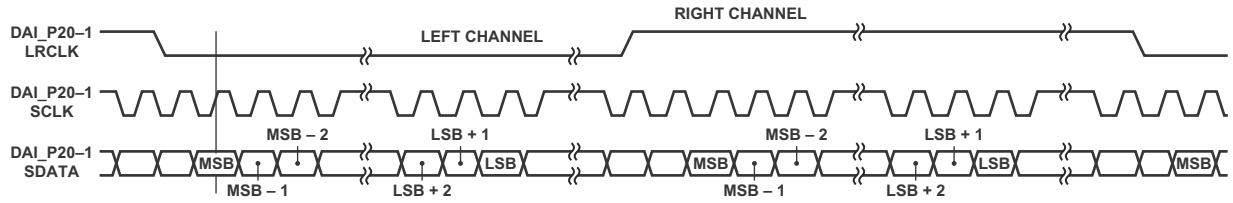


Figure 32. I²S-Justified Mode

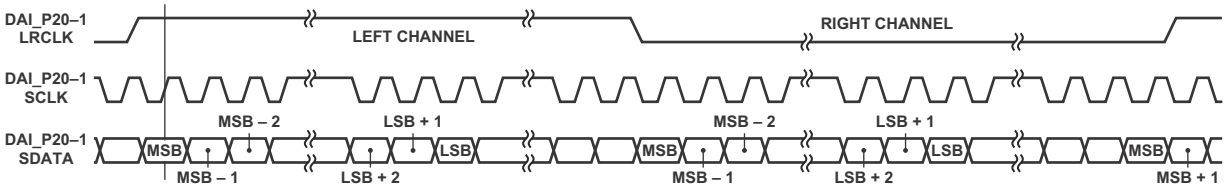


Figure 33. Left-Justified Mode

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 39. Input signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 39. S/PDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		ns
$t_{SIHFCLKW}$	Transmit Clock Width	9		ns
$t_{SIHFCLK}$	Transmit Clock Period	20		ns
$t_{SISCLKW}$	Clock Width	36		ns
t_{SISCLK}	Clock Period	80		ns

[1] The serial clock, data and frame sync signals can come from any of the DAI pins.The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

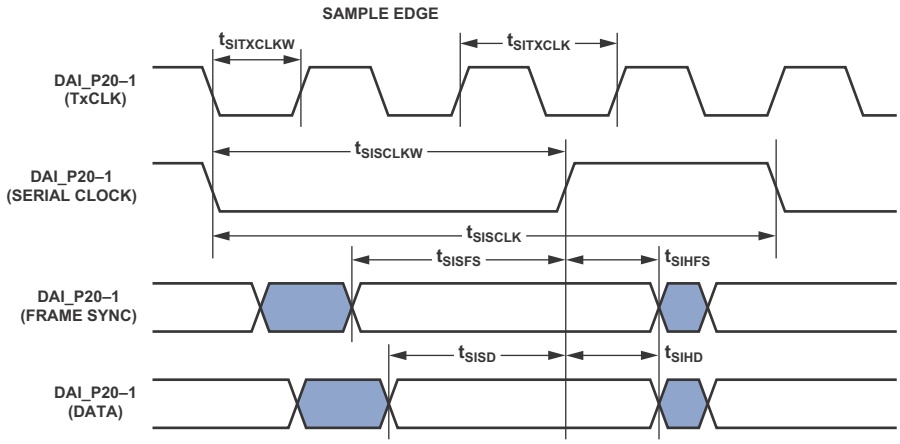


Figure 34. S/PDIF Transmitter Input Timing

Oversampling Clock (HFCLK) Switching Characteristics

The S/PDIF transmitter has an oversampling clock. This HFCLK input is divided down to generate the biphase clock.

Table 40. Over Sampling Clock (HFCLK) Switching Characteristics

Parameter	Max	Unit
HFCLK Frequency for HFCLK = 384 × Frame Sync	Oversampling Ratio × Frame Sync <= $1/t_{SIHFCLK}$	MHz
HFCLK Frequency for HFCLK = 256 × Frame Sync	49.2	MHz
Frame Rate (FS)	192.0	kHz

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the TBD × FS clock.

Table 41. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	LRCLK Delay After Serial Clock		5	ns
t_{HOFSI}	LRCLK Hold After Serial Clock	–2		ns
t_{DDTI}	Transmit Data Delay After Serial Clock		5	ns
t_{HDTI}	Transmit Data Hold After Serial Clock	–2		ns
t_{SCLKIW}[1]	Transmit Serial Clock Width	38.5		ns

[1] Serial clock frequency is TBD x frame sync where FS = the frequency of LRCLK.

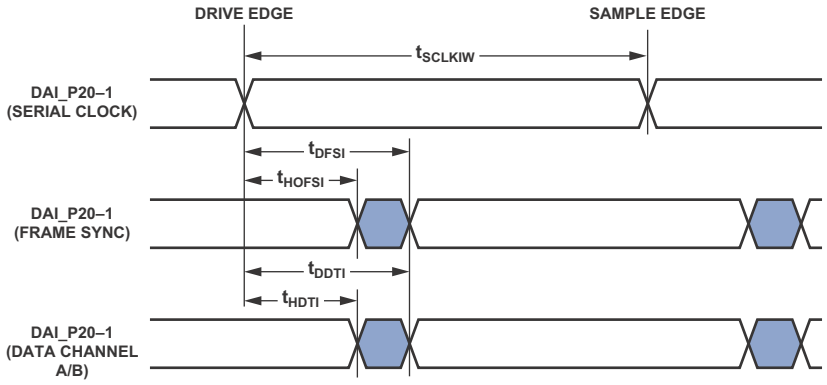


Figure 35. S/PDIF Receiver Internal Digital PLL Mode Timing

SPI Interface—Master

The ADSP-2147x contains two SPI ports. Both primary and secondary are available through DPI only. The timing provided in Table 42 and Table 43 applies to both.

Table 42. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid To SPICLK Edge (Data Input Setup Time)	8.2		ns
t_{HSPIDM}	SPICLK Last Sampling Edge To Data Input Not Valid	2		ns
Switching Characteristics				
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		2.5	
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	DPI Pin (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to DPI Pin (SPI Device Select) High	$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		ns

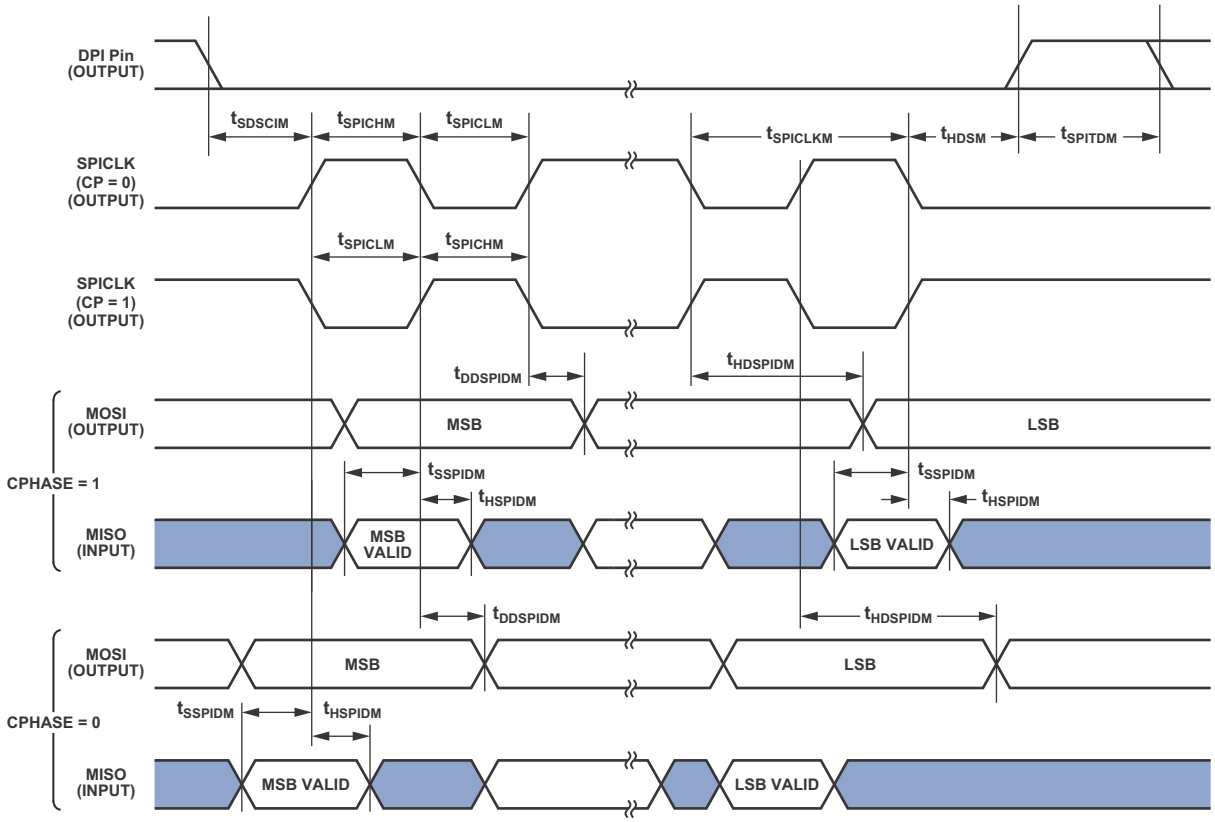


Figure 36. SPI Master Timing

SPI Interface—Slave

Table 43. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$		ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$		ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge, CPHASE = 0 or CPHASE = 1	$2 \times t_{PCLK}$		ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$		ns
t_{SSPIDS}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	2		ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE = 0)	$2 \times t_{PCLK}$		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	6.8	ns
t_{DSOE}[1]	$\overline{SPIDS}$ Assertion to Data Out Active (SPI2)	0	8	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	6.8	ns
t_{DSDHI}[1]	$\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2)	0	8.6	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		9.5	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$		ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{PCLK}$	ns

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, see the processor hardware reference, "Serial Peripheral Interface Port" chapter.

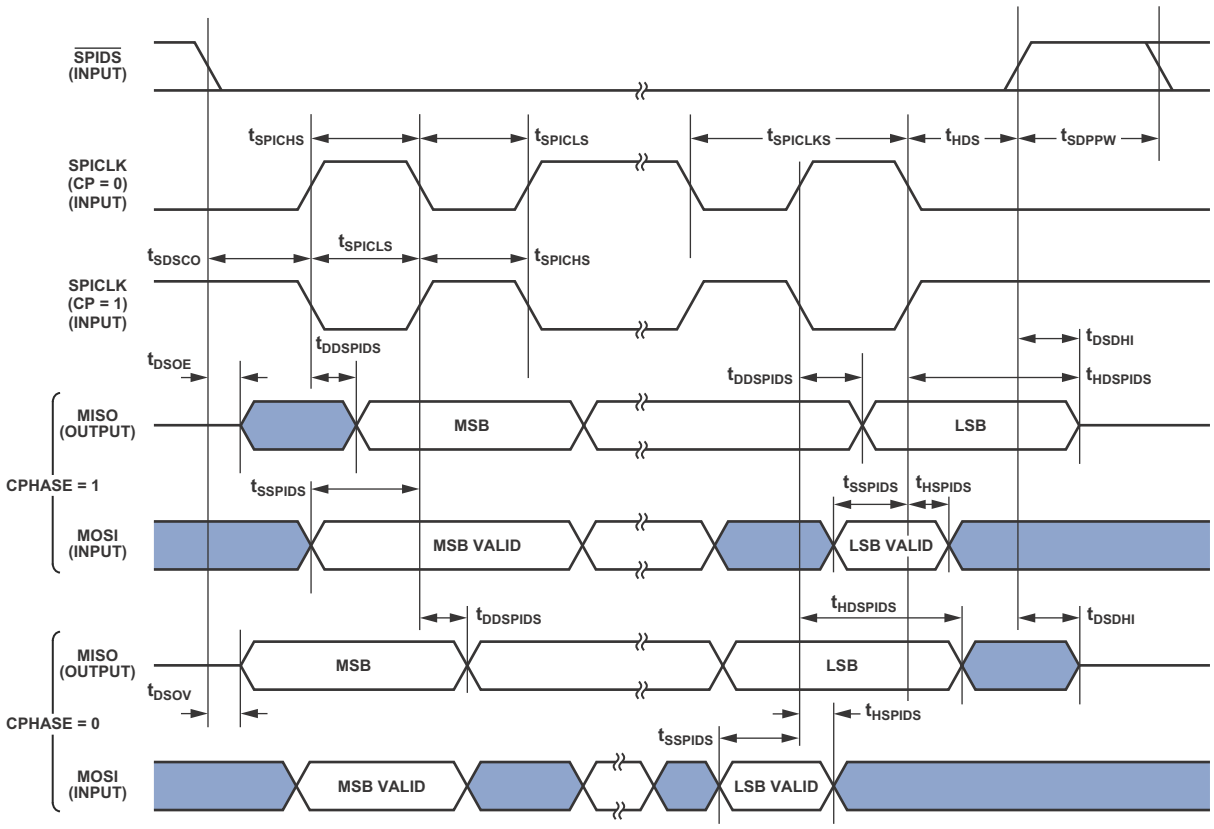


Figure 37. SPI Slave Timing

Media Local Bus

All the numbers given are applicable for all speed modes (1024Fs, 512Fs and 256Fs for 3-pin; 512Fs and 256Fs for 5-pin) unless otherwise specified. Please refer to MediaLB specification document rev 3.0 for more details.

Table 44. MLB Interface, 3-pin Specifications

Parameter		Min	Typ	Max	Unit
Three-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	1024Fs		20.3		ns
	512Fs		40		ns
	256Fs		81		ns
t_{MCKL}	MLBCLK Low Time				
	1024Fs	6.1			ns
	512Fs	14			ns
	256Fs	30			ns
t_{MCKH}	MLBCLK High Time				
	1024Fs	9.3			ns
	512Fs	14			ns
	256Fs	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})				
	1024Fs			1	ns
	512Fs/256Fs			3	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})				
	1024Fs			1	ns
	512Fs/256Fs			3	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation				
	1024Fs			0.7	nspp
	512Fs/256			2.0	nspp
t_{DSMCF}	DAT/SIG Input Setup Time	1			ns
t_{DHMCF}	DAT/SIG Input Hold Time	0			ns
t_{MCFDZ}	DAT/SIG Output Time to Three-state	0		t_{MCKL}	ns
t_{MCDRV}	DAT/SIG Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MDZH}[2]	Bus Hold Time				
	1024Fs	2			ns
	512Fs/256	4			ns
C_{MLB}	DAT/SIG Pin Load				
	1024Fs			40	pf
	512Fs/256			60	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).
[2] The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

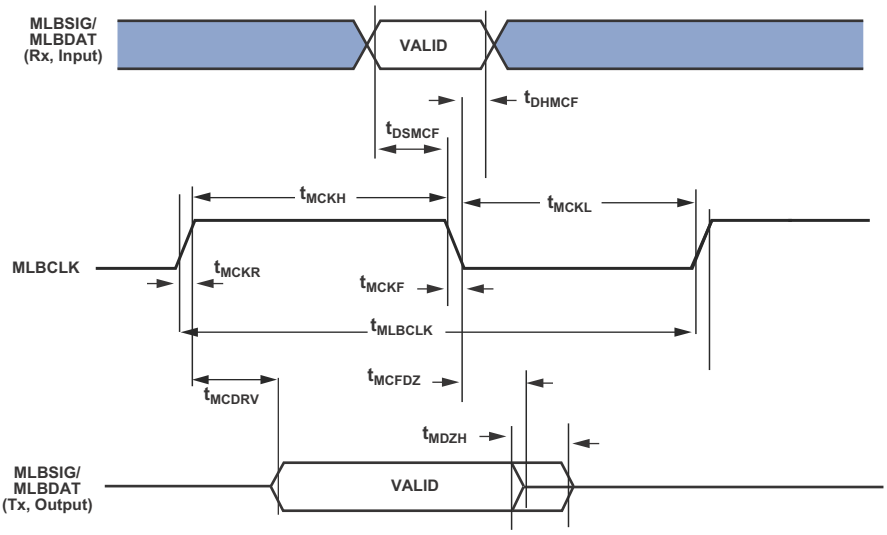


Figure 38. MLB Timing (3-Pin Interface)

Table 45. MLB Interface, 5-pin Specifications

Parameter		Min	Typ	Max	Unit
Five-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	512Fs		40		ns
	256Fs		81		ns
t_{MCKL}	MLBCLK Low Time				
	512Fs	15			ns
	256Fs	30			ns
t_{MCKH}	MLBCLK High Time				
	512Fs	15			ns
	256Fs	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})			6	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})			6	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation			2	nspp
t_{DSMCF}[2]	DAT/SIG Input Setup Time	3			ns
t_{DHMCF}	DAT/SIG Input Hold Time	5			ns
t_{MCDRV}	DS/DO Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MCRDL}[3]	DO/SO Low From MLBCLK High				
	512Fs			10	ns
	256Fs			20	ns
C_{MLB}	DS/DO Pin Load			40	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).
[2] Gate Delays due to OR'ing logic on the pins must be accounted for.
[3] When a node is not driving valid data onto the bus, the MLBSO and MLBDO output lines shall remain low. If the output lines can float at anytime, including while in reset, external pull-down resistors are required to keep the outputs from corrupting the MediaLB signal lines when not being driven.

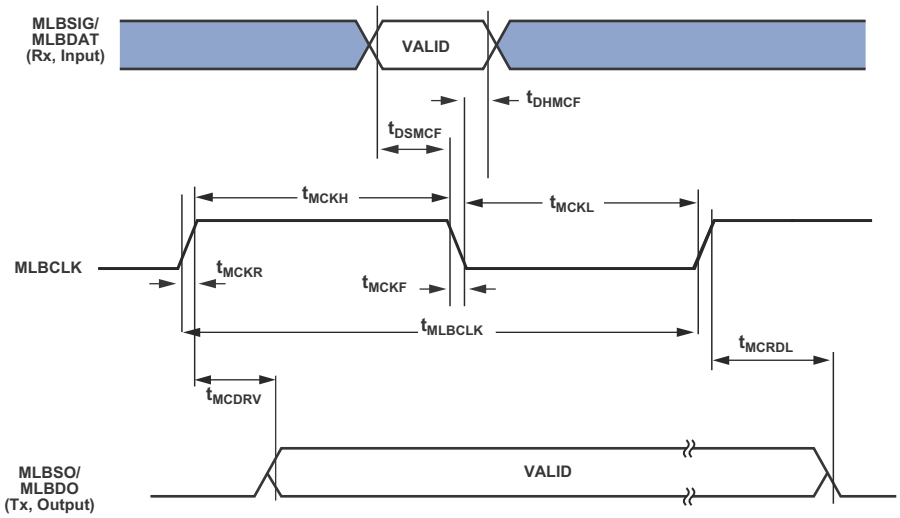


Figure 39. MLB Timing (5-Pin Interface)

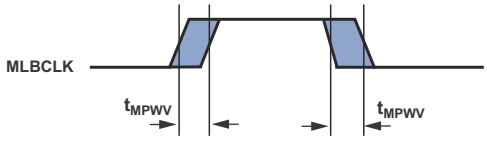


Figure 40. MLB 3-Pin and 5-Pin MLBCLK Pulse Width Variation Timing

Universal Asynchronous Receiver-Transmitter (UART) Port—Receive and Transmit Timing

Figure 41 describes UART port receive and transmit operations. The maximum baud rate is PCLK/16 where PCLK = 1/tPCLK. As shown in Figure 41 there is some latency between the generation of internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

Table 46. Shift Register

Parameter		Min	Max	Unit
Timing Requirement				
t_{RXD}[1]	Incoming Data Pulse Width	$16 \times t_{PCLK}-1$		ns
Switching Characteristic				
t_{TXD}1	Outgoing Data Pulse Width	$16 \times t_{PCLK}-1$		ns

[1] UART signals RXD and TXD are routed through DPI P14-1 pins using the SRU.

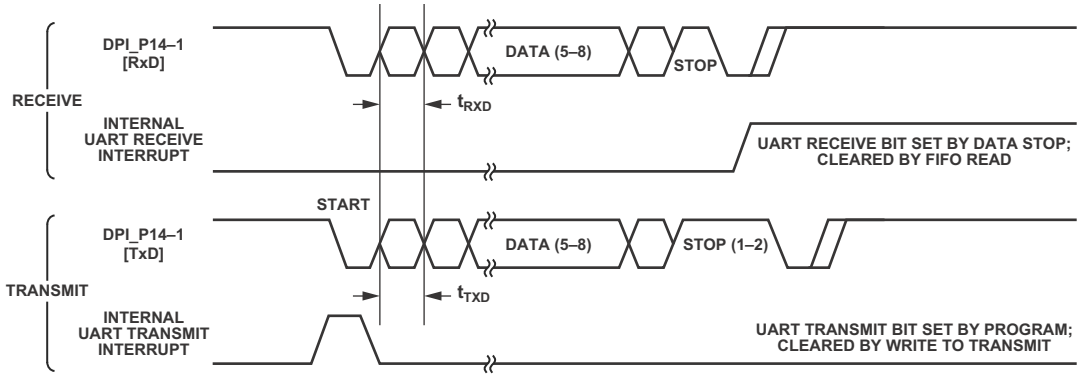


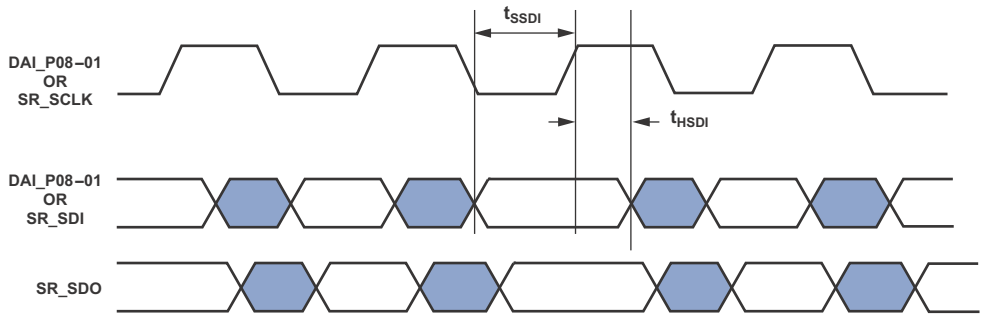
Figure 41. UART Port—Receive and Transmit Timing

Shift Register

Table 47. Shift Register

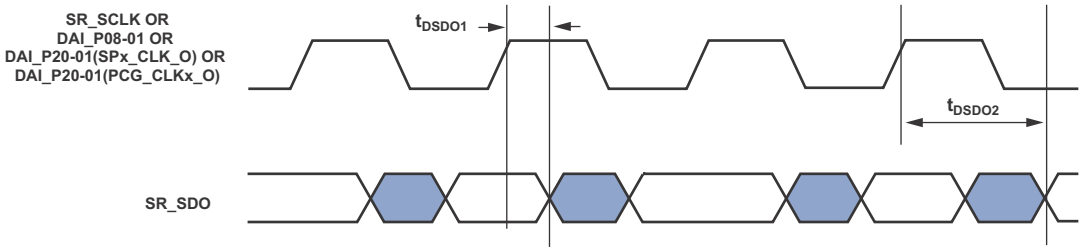
Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDI}	SR_SDI Setup Before SR_SCLK Rising Edge	TBD		ns
t_{HSDI}	SR_SDI Hold After SR_SCLK Rising Edge		TBD	ns
$t_{SSDIDAI}$[1]	DAI_P08–01 (SR_SDI) Setup Before DAI_P08–01 (SR_SCLK) Rising Edge	TBD		ns
$t_{HSDIDAI}$[1]	DAI_P08–01 (SR_SDI) Hold After DAI_P08–01 (SR_SCLK) Rising Edge		TBD	ns
$t_{SSCK2LCK}$[2]	SR_SCLK to SR_LAT Setup	TBD		ns
$t_{SSCK2LCKDAI}$[1, 2]	DAI_P08–01 (SR_SCLK) to DAI_P08–01 (SR_LAT) Setup	TBD		ns
$t_{CLRREM2SCK}$	Removal Time $\overline{SR\_CLR}$ to SR_SDCLK	TBD		ns
$t_{CLRREM2LCK}$	Removal Time $\overline{SR\_CLR}$ to SR_LAT	TBD		ns
t_{CLRW}	$\overline{SR\_CLR}$ Pulse Width	TBD		ns
t_{SCKW}	SR_SDCLK Clock Pulse Width	TBD		ns
t_{LCKW}	SR_LAT Clock Pulse Width	TBD		ns
f_{MAX}	Maximum Clock Frequency SR_SDCLK or SR_LAT		$f_{CCLK} \div 8$	MHz
Switching Characteristics				ns
t_{DSDO1}[3]	SR_SDO Hold After SR_SCLK Rising Edge	TBD		ns
t_{DSDO2}[3]	SR_SDO Max. Delay After SR_SCLK Rising Edge		TBD	ns
$t_{DSDODAI1}$[1, 3]	SR_SDO Hold After DAI_P08–01 (SR_SCLK) Rising Edge	TBD		ns
$t_{DSDODAI2}$[1, 3]	SR_SDO Max. Delay After DAI_P08–01 (SR_SCLK) Rising Edge		TBD	ns
$t_{DSDOSP1}$[3, 4]	SR_SDO Hold After DAI_P20–01 (SR_SCLK) Rising Edge	TBD		ns
$t_{DSDOSP2}$[3, 4]	SR_SDO Max. Delay After DAI_P20–01 (SR_SCLK) Rising Edge		TBD	ns
$t_{DSDOPCG1}$[3, 5, 6]	SR_SDO Hold After DAI_P20–01 (SR_SCLK) Rising Edge	TBD		ns
$t_{DSDOPCG2}$[3, 5, 6]	SR_SDO Max. Delay After DAI_P20–01 (SR_SCLK) Rising Edge		TBD	ns
$t_{DSDOCLR1}$[3]	$\overline{SR\_CLR}$ to SR_SDO Min. Delay	TBD		ns
$t_{DSDOCLR2}$[3]	$\overline{SR\_CLR}$ to SR_SDO Max. Delay		TBD	ns
t_{DLDO1}[3]	SR_LDO Hold After SR_LAT Rising Edge	TBD		ns
t_{DLDO2}[3]	SR_LDO Max. Delay After SR_LAT Rising Edge		TBD	ns
$t_{DLDODAI1}$[3]	SR_LDO Hold After DAI_P08–01 (SR_LAT) Rising Edge	TBD		ns
$t_{DLDODAI2}$[3]	SR_LDO Max. Delay After DAI_P08–01 (SR_LAT) Rising Edge		TBD	ns
$t_{DLDOSP1}$[3, 4]	SR_LDO Hold After DAI_P20–01 (SR_LAT) Rising Edge	TBD		ns
$t_{DLDOSP2}$[3, 4]	SR_LDO Max. Delay After DAI_P20–01 (SR_LAT) Rising Edge		TBD	ns
$t_{DLDOPCG1}$[3, 5, 6]	SR_LDO Hold After DAI_P20–01 (SR_LAT) Rising Edge	TBD		ns
$t_{DLDOPCG2}$[3, 5, 6]	SR_LDO Max. Delay After DAI_P20–01 (SR_LAT) Rising Edge		TBD	ns
$t_{DLDOCLR1}$[3]	$\overline{SR\_CLR}$ to SR_LDO Min. Delay	TBD		ns
$t_{DLDOCLR2}$[3]	$\overline{SR\_CLR}$ to SR_LDO Max. Delay		TBD	ns

[1] DAI_P08–01 are selected as shift register clock, latch clock and serial data input.
[2] Both clocks can be connected to the same clock source. If both clocks are connected to same clock source, then data in the 18-stage shift register is always one cycle ahead of latch register data.
[3] For setup/hold timing requirements of off-chip shift register interfacing devices.
[4] SPORTx Serial clock out, Frame sync out, and Serial data outputs are routed to Shift register block internally and are also routed onto DAI_P20–01.
[5] PCG Serial clock output is routed to SPORT and Shift register block internally and are also routed onto DAI_P20–01. SPORT will generate SR_LAT and SDI internally.
[6] PCG Serial clock and Frame sync outputs are routed to SPORT and Shift register block internally and are also routed onto DAI_P20–01. SPORT will generate SDI internally.



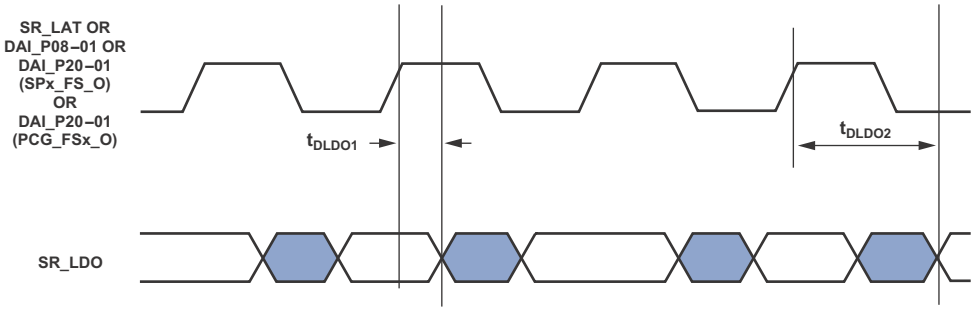
THE TIMING PARAMETERS SHOWN FOR t_{SSDI}, AND t_{HSDI}, ARE ALSO VALID FOR $t_{SSDIDAI}$, AND $t_{HSDIDAI}$.

Figure 42. SR_SDI Setup, Hold



THE TIMING PARAMETERS SHOWN FOR t_{DSDO1} AND t_{DSDO2} ARE ALSO VALID FOR$t_{DSDODAI1}$, $t_{DSDODAI2}$, $t_{DSDOSP1}$, $t_{DSDOSP2}$, $t_{DSDOPCG1}$ AND $t_{DSDOPCG2}$.

Figure 43. SR_ SDO Delay



THE TIMING PARAMETERS SHOWN FOR t_{DLDO1} AND t_{DLDO2} ARE ALSO VALID FOR $t_{DLDODAI1}$, $t_{DLDODAI2}$, $t_{DLDOSP1}$, $t_{DLDOSP2}$, $t_{DLDOPCG1}$, AND $t_{DLDOPCG2}$.

Figure 44. SR_LDO Delay

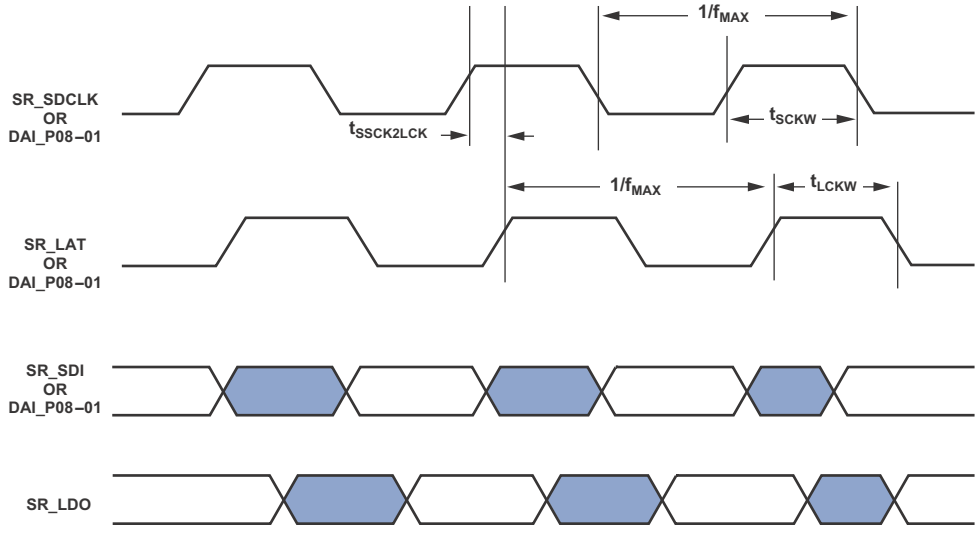


Figure 45. SR_SDCLK to SR_LAT Setup, Clocks Pulse Width and Maximum Frequency

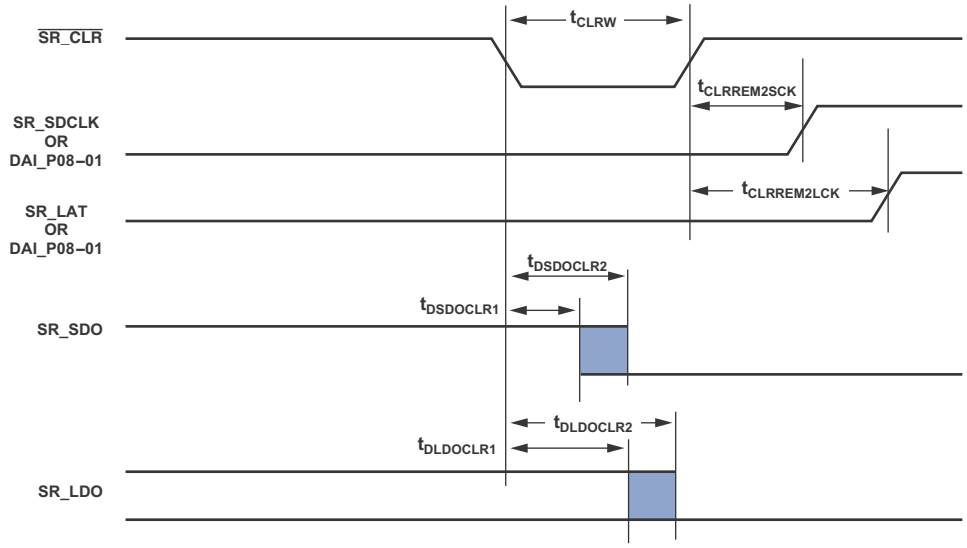


Figure 46. SR_CLR Timing

TWI Controller Timing

Table 48 and Figure 47 provide timing information for the TWI interface. Input Signals (SCL, SDA) are routed to the DPI_P14–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 48. Characteristics of the SDA and SCL Bus Lines for F/S-Mode TWI Bus Devices[1]

Parameter		Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0	100	0	400	kHz
t_{HDSTA}	Hold Time (repeated) Start Condition. After This Period, the First Clock Pulse is Generated.	4.0		0.6		µs
t_{LOW}	Low Period of the SCL Clock	4.7		1.3		µs
t_{HIGH}	High Period of the SCL Clock	4.0		0.6		µs
t_{SUSTA}	Setup Time for a Repeated Start Condition	4.7		0.6		µs
t_{HDDAT}	Data Hold Time for TWI-bus Devices	0		0		µs
t_{SUDAT}	Data Setup Time	250		100		ns
t_{SUSTO}	Setup Time for Stop Condition	4.0		0.6		µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition	4.7		1.3		µs
t_{SP}	Pulse Width of Spikes Suppressed By the Input Filter	n/a	n/a	0	50	ns

[1] All values referred to V_{IHmin} and V_{ILmax} levels. For more information, see Electrical Characteristics on page 20.

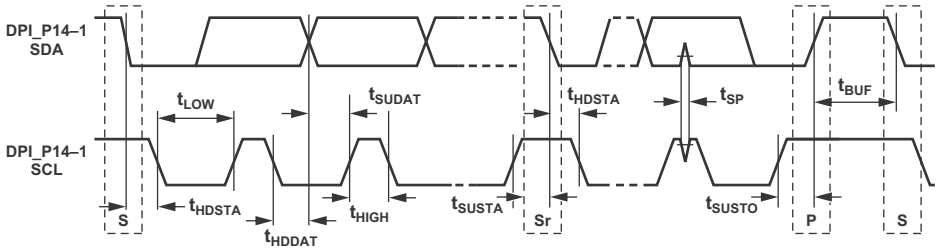


Figure 47. Fast and Standard Mode Timing on the TWI Bus

JTAG Test Access Port and Emulation

Table 49. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = DATA15–0, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, DAI_Px, DPI_Px, FLAG3–0, MLBCLK, MLBDAT, MLBSIG, SR_SCLK, $\overline{\text{SR\_CLR}}$, SR_SDI, and SR_LAT.

[2] System Outputs = DAI_Px, DPI_Px, ADDR23–0, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, FLAG3–0, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, SDCKE, SDA10, SDDQM, SDCLK, MLBDAT, MLBSIG, MLBDO, MLBSO, SR_SDO, SR_LDO and $\overline{\text{EMU}}$.

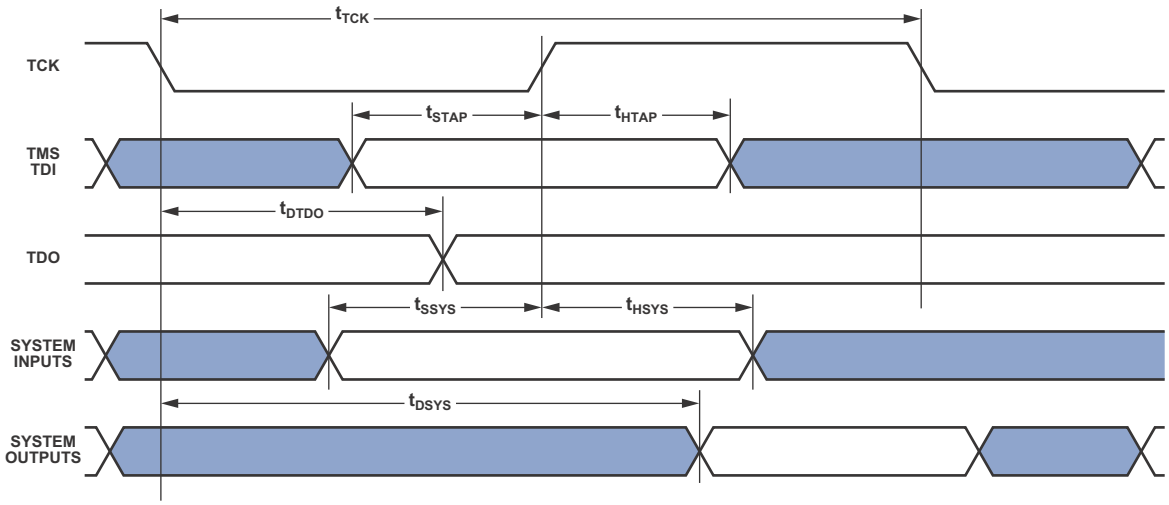


Figure 48. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 49 shows typical I-V characteristics for the output drivers of the ADSP-2147x. The curves represent the current drive capability of the output drivers as a function of output voltage.

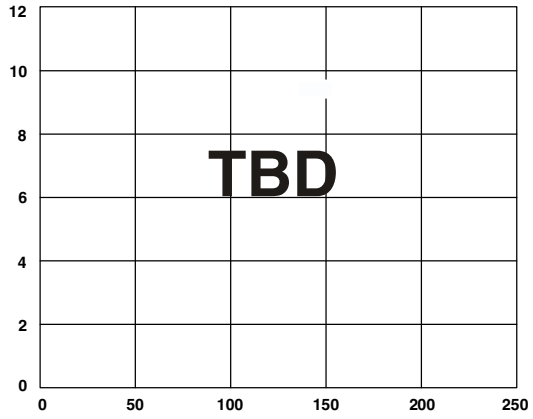


Figure 49. Typical Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 16 on Page 25 through Table 49 on Page 60. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 50.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 51. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

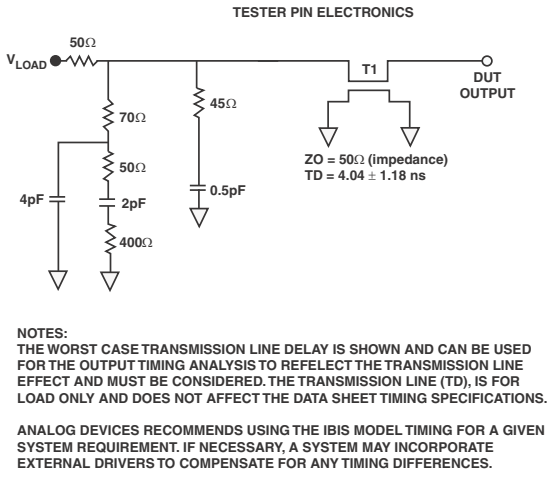


Figure 50. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

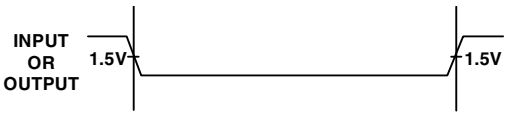


Figure 51. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 50). Figure 54 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 52, Figure 53, and Figure 54 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

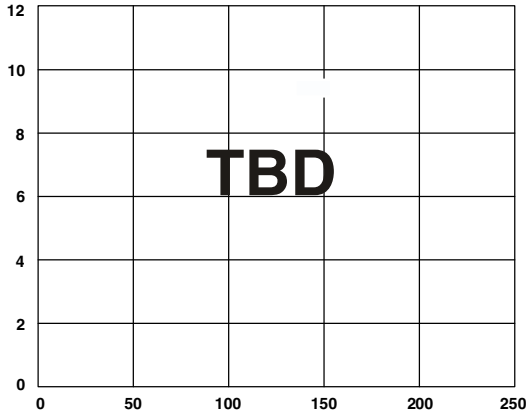


Figure 52. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Max)

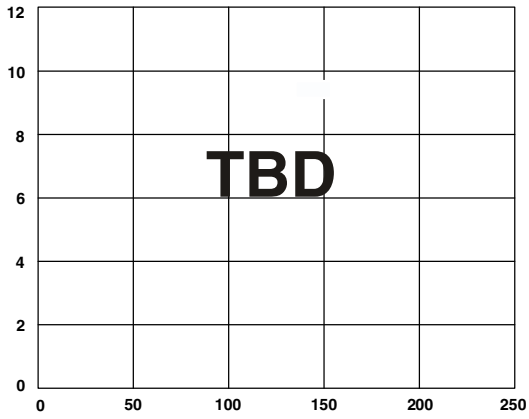


Figure 53. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Min)

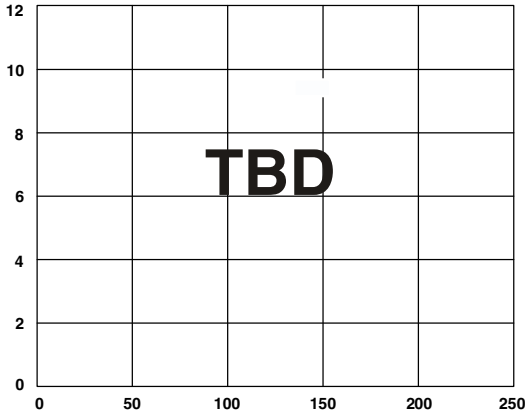


Figure 54. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The ADSP-2147x processor is rated for performance over the temperature range specified in Operating Conditions on Page 19.

Table 50 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (PBGA). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature °C

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the Typical value from Table 50.

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations. Note that the thermal characteristics values provided in Table 50 are modeled values.

Table 50. Thermal Characteristics for 100-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	TBD	°C/W
θ_{JMA}	Airflow = 1 m/s	TBD	°C/W
θ_{JMA}	Airflow = 2 m/s	TBD	°C/W
θ_{JC}		TBD	°C/W
Ψ_{JT}	Airflow = 0 m/s	TBD	°C/W
Ψ_{JMT}	Airflow = 1 m/s	TBD	°C/W
Ψ_{JMT}	Airflow = 2 m/s	TBD	°C/W

Table 51. Thermal Characteristics for 196-Ball CSP_BGA

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	TBD	°C/W
θ_{JMA}	Airflow = 1 m/s	TBD	°C/W
θ_{JMA}	Airflow = 2 m/s	TBD	°C/W
θ_{JC}		TBD	°C/W
Ψ_{JT}	Airflow = 0 m/s	TBD	°C/W
Ψ_{JMT}	Airflow = 1 m/s	TBD	°C/W
Ψ_{JMT}	Airflow = 2 m/s	TBD	°C/W

Thermal Diode

The ADSP-21476x processors incorporate thermal diode/s to monitor the die temperature. The thermal diode of is a grounded collector, PNP Bipolar Junction Transistor (BJT). The THD_P pin is connected to the emitter and the THD_M pin is connected to the base of the transistor. These pins can be used by an external temperature sensor (such as ADM 1021A or LM86 or others) to read the die temperature of the chip.

The technique used by the external temperature sensor is to measure the change in VBE when the thermal diode is operated at two different currents. This is shown in the following equation:

$$\Delta V_{BE} = n \times \frac{kT}{q} \times ln(N)$$

where:

n = multiplication factor close to 1, depending on process variations

k = Boltzmann's constant

T = temperature (°C)

q = charge of the electron

N = ratio of the two currents

The two currents are usually in the range of 10 micro Amperes to 300 micro Amperes for the common temperature sensor chips available.

Table 52 contains the thermal diode specifications using the transistor model.

Table 52. Thermal Diode Parameters – Transistor Model

Symbol	Parameter	Min	Typ	Max	Unit
I_{FW}	Forward Bias Current	TBD		TBD	µA
I_E	Emitter Current	TBD		TBD	
n_Q	Transistor Ideality	TBD	TBD	TBD	
Beta		TBD		TBD	
R_T	Series Resistance	TBD	TBD	TBD	Ω

100-LQFP_EP LEAD ASSIGNMENT

Table 53 lists the lead names and their default function after reset (in parentheses).

Table 53. 100-Lead LQFP_EP Lead Assignments (Numerically by Lead Number)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
V_{DD_INT}	1	V_{DD_EXT}	26	DAI_P10	51	V_{DD_INT}	76
CLK_CFG1	2	DPI_P08	27	V_{DD_INT}	52	FLAG0	77
BOOT_CFG0	3	DPI_P07	28	V_{DD_EXT}	53	V_{DD_INT}	78
V_{DD_EXT}	4	V_{DD_INT}	29	DAI_P20	54	V_{DD_INT}	79
V_{DD_INT}	5	DPI_P09	30	V_{DD_INT}	55	FLAG1	80
BOOT_CFG1	6	DPI_P10	31	DAI_P08	56	FLAG2	81
GND	7	DPI_P11	32	DAI_P04	57	FLAG3	82
NC	8	DPI_P12	33	DAI_P14	58	MLBCLK	83
NC	9	DPI_P13	34	DAI_P18	59	MLBDAT	84
CLK_CFG0	10	DAI_P03	35	DAI_P17	60	MLBDO	85
V_{DD_INT}	11	DPI_P14	36	DAI_P16	61	V_{DD_EXT}	86
CLKIN	12	V_{DD_INT}	37	DAI_P15	62	MLBSIG	87
XTAL	13	V_{DD_INT}	38	DAI_P12	63	V_{DD_INT}	88
V_{DD_EXT}	14	V_{DD_INT}	39	V_{DD_INT}	64	MLBSO	89
V_{DD_INT}	15	DAI_P13	40	DAI_P11	65	$\overline{TRST}$	90
V_{DD_INT}	16	DAI_P07	41	V_{DD_INT}	66	$\overline{EMU}$	91
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	17	DAI_P19	42	V_{DD_INT}	67	TDO	92
V_{DD_INT}	18	DAI_P01	43	GND	68	V_{DD_EXT}	93
DPI_P01	19	DAI_P02	44	THD_M	69	V_{DD_INT}	94
DPI_P02	20	V_{DD_INT}	45	THD_P	70	TDI	95
DPI_P03	21	V_{DD_EXT}	46	V_{DD_THD}	71	TCK	96
V_{DD_INT}	22	V_{DD_INT}	47	V_{DD_INT}	72	V_{DD_INT}	97
DPI_P05	23	DAI_P06	48	V_{DD_INT}	73	$\overline{RESET}$	98
DPI_P04	24	DAI_P05	49	V_{DD_INT}	74	TMS	99
DPI_P06	25	DAI_P09	50	V_{DD_INT}	75	V_{DD_INT}	100
						GND	101*

* Pin no. 101 is the GND supply (see Figure 55 and Figure 56) for the processor; this pad must be **robustly** connect to GND.

Figure 55 shows the top view of the 100-lead LQFP_EP pin configuration. Figure 56 shows the bottom view of the 100-lead LQFP_EP lead configuration.

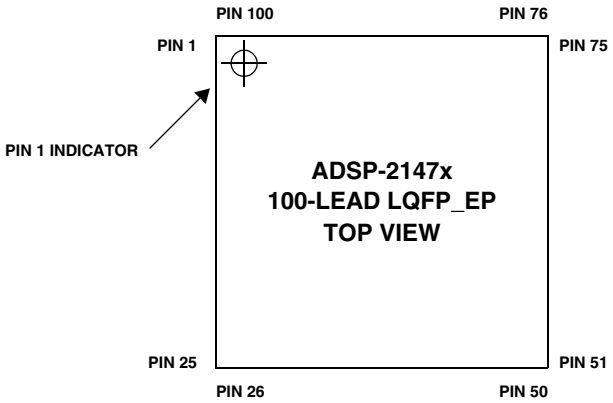


Figure 55. 100-Lead LQFP_EP Lead Configuration (Top View)

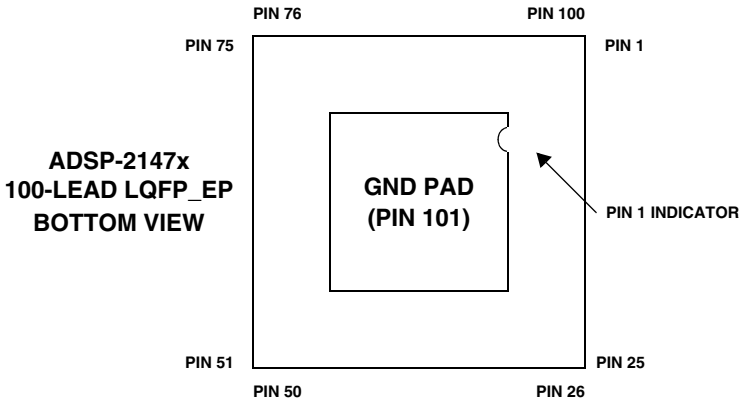


Figure 56. 100-Lead LQFP_EP Lead Configuration (Bottom View)

196-BALL BGA BALL ASSIGNMENT

Table 54. 196-Ball CSP_BGA Ball Assignment (Numerically by Ball No.)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	GND	D1	ADDR6	G1	XTAL	K1	DPI_P02	N1	DPI_P14
A2	SDCKE	D2	ADDR4	G2	SDA10	K2	DPI_P04	N2	SR_LDO1
A3	SDDQM	D3	ADDR1	G3	ADDR11	K3	DPI_P05	N3	SR_LDO4
A4	$\overline{\text{SDRAS}}$	D4	CLK_CFG0	G4	GND	K4	DPI_P09	N4	SR_LDO8
A5	$\overline{\text{SDWE}}$	D5	V_{DD_EXT}	G5	V_{DD_INT}	K5	V_{DD_INT}	N5	SR_LDO10
A6	DATA12	D6	V_{DD_EXT}	G6	GND	K6	GND	N6	DAI_P01
A7	DATA13	D7	V_{DD_EXT}	G7	GND	K7	GND	N7	SR_LDO9
A8	DATA10	D8	V_{DD_EXT}	G8	GND	K8	GND	N8	DAI_P02
A9	DATA9	D9	V_{DD_EXT}	G9	GND	K9	GND	N9	SR_LDO13
A10	DATA7	D10	V_{DD_EXT}	G10	V_{DD_INT}	K10	V_{DD_INT}	N10	SR_SCLK
A11	DATA3	D11	V_{DD_EXT}	G11	V_{DD_EXT}	K11	GND	N11	DAI_P09
A12	DATA1	D12	ADDR14	G12	ADDR21	K12	DAI_P16	N12	SR_SDI
A13	DATA2	D13	ADDR20	G13	ADDR19	K13	DAI_P18	N13	SR_LDO17
A14	GND	D14	WDT_CLKO	G14	RTXO	K14	DAI_P15	N14	DAI_P14
B1	ADDR0	E1	ADDR8	H1	ADDR13	L1	DAI_P03	P1	GND
B2	CLK_CFG1	E2	ADDR7	H2	ADDR12	L2	DPI_P10	P2	SR_LDO3
B3	BOOT_CFG0	E3	ADDR5	H3	ADDR10	L3	DPI_P08	P3	SR_LDO2
B4	TMS	E4	V_{DD_EXT}	H4	ADDR17	L4	DPI_P06	P4	SR_LDO6
B5	$\overline{\text{RESET}}$	E5	V_{DD_INT}	H5	V_{DD_INT}	L5	V_{DD_INT}	P5	$\overline{\text{WDTRSTO}}$
B6	DATA14	E6	V_{DD_INT}	H6	GND	L6	V_{DD_INT}	P6	DAI_P19
B7	DATA11	E7	V_{DD_INT}	H7	GND	L7	V_{DD_INT}	P7	DAI_P13
B8	DATA4	E8	V_{DD_INT}	H8	GND	L8	V_{DD_INT}	P8	SR_LDO11
B9	DATA8	E9	V_{DD_INT}	H9	GND	L9	V_{DD_INT}	P9	SR_LDO15
B10	DATA6	E10	V_{DD_INT}	H10	V_{DD_INT}	L10	V_{DD_INT}	P10	$\overline{\text{SR\_CLR}}$
B11	DATA5	E11	V_{DD_EXT}	H11	V_{DD_EXT}	L11	DAI_P10	P11	SR_LAT
B12	$\overline{\text{TRST}}$	E12	$\overline{\text{AMI\_RD}}$	H12	BOOT_CFG2	L12	DAI_P20	P12	SR_LDO14
B13	FLAG1	E13	ADDR22	H13	ADDR23	L13	DAI_P17	P13	SR_LDO12
B14	DATA0	E14	FLAG2	H14	RTXI	L14	DAI_P04	P14	GND
C1	ADDR2	F1	CLKIN	J1	DPI_P01	M1	DPI_P13		
C2	ADDR3	F2	ADDR9	J2	DPI_P03	M2	DPI_P12		
C3	RTCLKOUT	F3	BOOT_CFG1	J3	ADDR18	M3	SR_LDO0		
C4	$\overline{\text{MS0}}$	F4	NC	J4	$\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$	M4	DPI_P07		
C5	$\overline{\text{SDCAS}}$	F5	NC	J5	V_{DD_INT}	M5	DPI_P11		
C6	DATA15	F6	GND	J6	GND	M6	SR_LDO5		
C7	TCK	F7	GND	J7	GND	M7	SR_LDO7		
C8	TDI	F8	GND	J8	GND	M8	DAI_P07		
C9	SDCLK0	F9	GND	J9	GND	M9	SR_LDO16		
C10	$\overline{\text{EMU}}$	F10	V_{DD_INT}	J10	V_{SS_RTC}	M10	SR_SDO		
C11	TDO	F11	V_{DD_EXT}	J11	V_{DD_RTC}	M11	DAI_P06		
C12	FLAG3	F12	ADDR15	J12	DAI_P11	M12	DAI_P05		
C13	ADDR16	F13	FLAG0	J13	AMI_ACK	M13	DAI_P08		
C14	WDT_CLKIN	F14	$\overline{\text{AMI\_WR}}$	J14	$\overline{\text{MS1}}$	M14	DAI_P12		

OUTLINE DIMENSIONS

The ADSP-2147x processors are available in a 100-lead LQFP_EP and 196-ball CSP_BGA RoHS compliant packages. For package assignment by model, see Ordering Guide on Page 69.

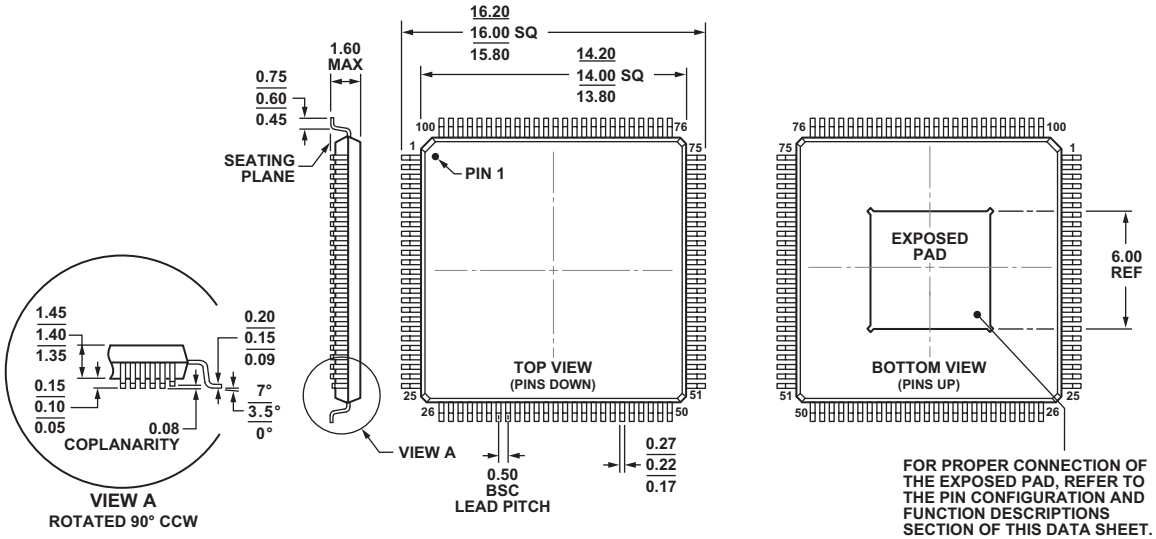


Figure 57. 100-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP]
(SW-100-2)
Dimensions shown in millimeters

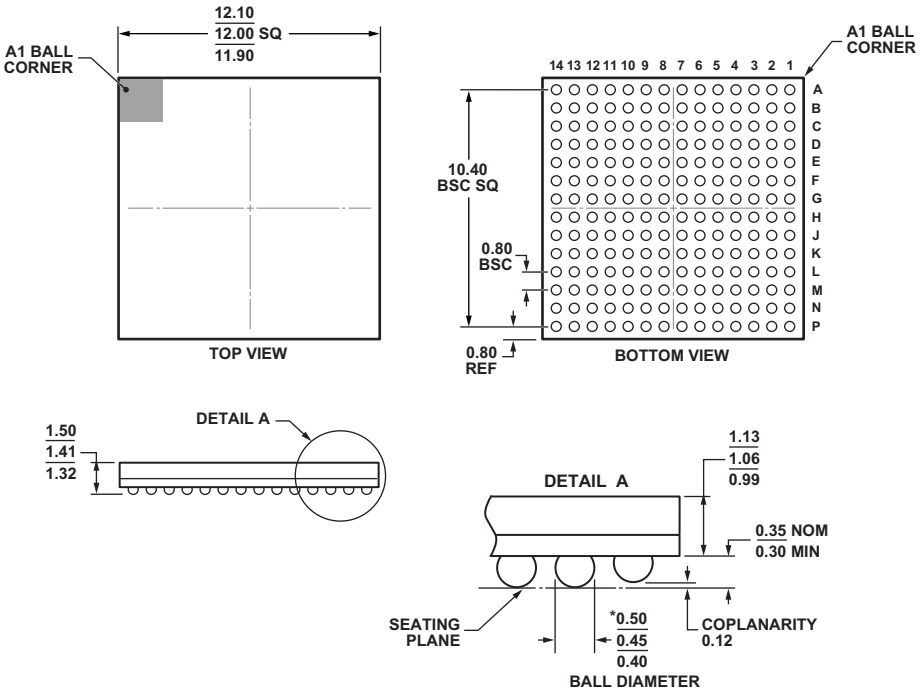


Figure 58. 196-Ball Chip Scale Package, Ball Grid Array [CSP_BGA]
(BG-196-7)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

For industry standard design recommendations, refer to IPC-7351, Generic Requirements for Surface-Mount Design and Land Pattern Standard.

AUTOMOTIVE PRODUCTS

The ADSP-21478 and ADSP-21479 models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these Automotive models may have specifications that differ from the commercial models and designers should review the product Specifications section of this datasheet carefully. Only the Automotive grade products shown in Table 55 are available for use in Automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 55. Automotive Products

Model	Temperature Range[1]	On-Chip SRAM	Package Description	Package Option
AD21478WBBZ3xx[2]	–40°C to +105°C	3 Mbit	100-Lead LQFP_EP	SW-100-2
AD21479WBBZ3xx[3]	–40°C to +105°C	5 Mbit	100-Lead LQFP_EP	SW-100-2

[1] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 19 for junction temperature (T_J) specification which is the only temperature specification.
[2] Z =RoHS Compliant Part
[3] Z =RoHS Compliant Part

ORDERING GUIDE

Model[1]	Temperature Range[2]	On-Chip SRAM	Package Description	Package Option
ADSP-21478KSWZ-ENG	0°C to +70°C	3 Mbit	100-Lead LQFP_EP	SW-100-2
ADSP-21478KBCZ-ENG	0°C to +70°C	3 Mbit	196-Ball CSP_BGA	BC-196-7
ADSP-21479KSWZ-ENG[3]	0°C to +70°C	5 Mbit	100-Lead LQFP_EP	SW-100-2
ADSP-21479KBCZ-ENG	0°C to +70°C	5 Mbit	196-Ball CSP_BGA	BC-196-7

[1] Z =RoHS Compliant Part
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 19 for junction temperature (T_J) specification which is the only temperature specification.
[3] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/SHARC