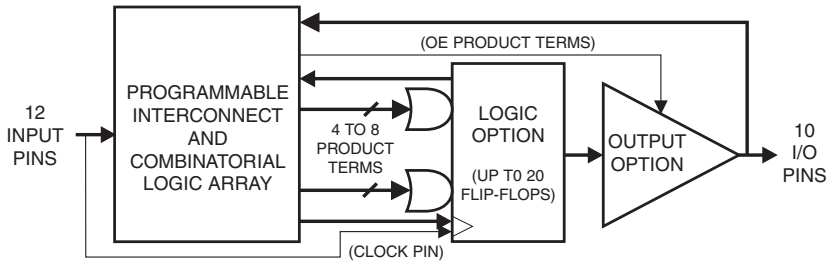
Features

- 3.0V to 3.6V Operating Range
- Advanced, High-speed, Electrically-erasable Programmable Logic Device
  - Superset of 22V10
  - Enhanced Logic Flexibility
  - Architecturally Compatible with ATV750B and ATV750 Software and Hardware
- D- or T-type Flip-flop
- Product Term or Direct Input Pin Clocking
- 15 ns Maximum Pin-to-pin Delay with 3V Operation
- Highest Density Programmable Logic Available in 24-pin Package
  - Advanced Electrically-erasable Technology
  - Reprogrammable
  - 100% Tested
- Increased Logic Flexibility
  - 42 Array Inputs, 20 Sum Terms and 20 Flip-flops
- Enhanced Output Logic Flexibility
  - All 20 Flip-flops Feed Back Internally
  - 10 Flip-flops are also Available as Outputs
- Programmable Pin-keeper Circuits
- Dual-in-line and Surface Mount Package in Standard Pinouts
- Commercial and Industrial Temperature Ranges
- 20-year Data Retention
- 2000V ESD Protection
- 1000 Erase/Write Cycles
- Green Package Options (Pb/Halide-free/RoHS Compliant) Available

Block Diagram



Description

The Atmel “750” architecture is twice as powerful as most other 24-pin programmable logic devices. Increased product terms, sum terms, flip-flops and output logic configurations translate into more usable gates. High-speed logic and uniform, predictable

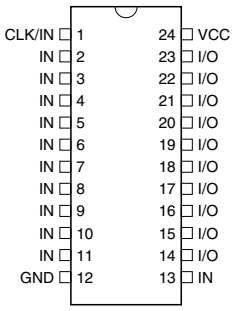
(continued)

Pin Configurations

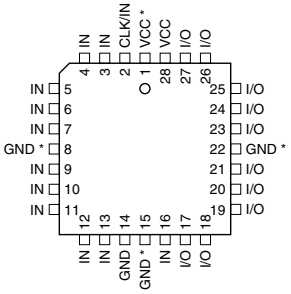
Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bi-directional Buffers
GND	Ground
VCC	3V Supply

Note: For PLCC, pins 1, 8, 15, and 22 can be left unconnected. For superior performance, connect VCC to pin 1 and GND to pins 8, 15, and 22.

DIP/SOIC/TSSOP



PLCC



High-speed Complex Programmable Logic Device

ATF750LVC

Rev. 1447E–02/06

delays guarantee fast in-system performance. The ATF750LVC is a high-performance CMOS (electrically-erasable) complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable technology.

Each of the ATF750LVC's 22 logic pins can be used as an input. Ten of these can be used as inputs, outputs or bi-directional I/O pins. Each flip-flop is individually configurable as either D- or T-type. Each flip-flop output is fed back into the array independently. This allows burying of all the sum terms and flip-flops.

There are 171 total product terms available. There are two sum terms per output, providing added flexibility. A variable format is used to assign between four to eight product terms per sum term. Much more logic can be replaced by this device than by any other 24-pin PLD. With 20 sum terms and flip-flops, complex state machines are easily implemented with logic to spare.

Product terms provide individual clocks and asynchronous resets for each flip-flop. Each flip-flop may also be individually configured to have direct input pin controlled clocking. Each output has its own enable product term. One product term provides a common synchronous preset for all flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power-up.

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +4.6V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)

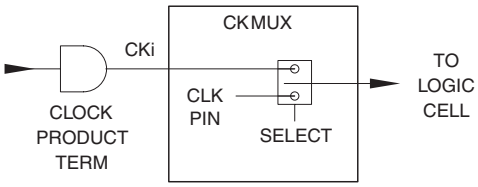
*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 4.6V for pulses of less than 20 ns.

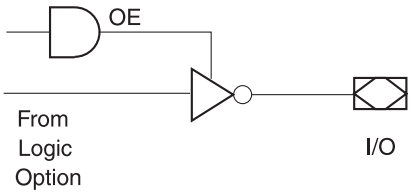
DC and AC Operating Conditions

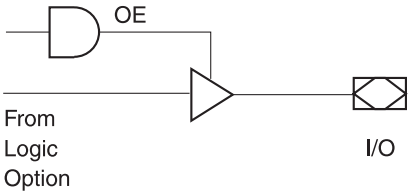
3.3V Operation	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - +85°C
V_{CC} Power Supply	3.0 - 3.6V	3.0 - 3.6V

Clock Mux



Output Options





Bus-friendly Pin-keeper Input and I/Os

All input and I/O pins on the ATF750LVC(L) have programmable “pin-keeper” circuits. If activated, when any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level.

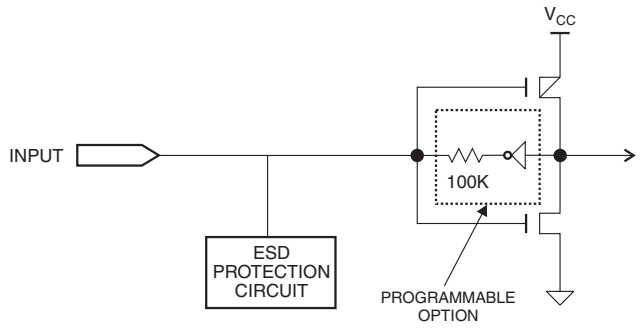
This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which cause unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Enabling or disabling of the pin-keeper circuits is controlled by the device type chosen in the logic compiler device selection menu. Please refer to the software compiler table for more details. Once the pin-keeper circuits are disabled, normal termination procedures are required for unused inputs and I/Os.

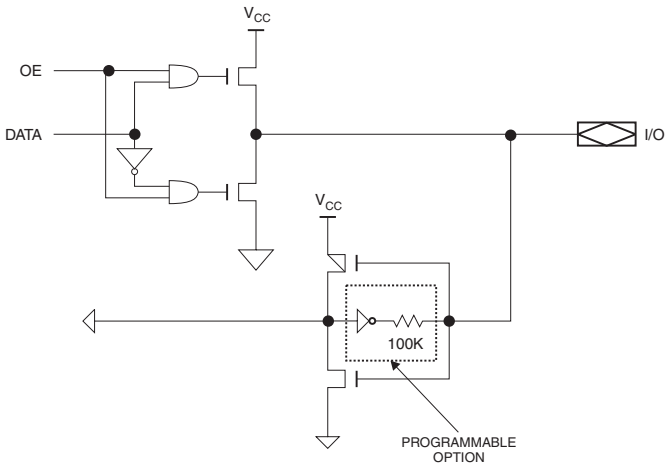
Table 1. Software Compiler Mode Selection

Synario	Wincupl	Pin-keeper Circuit
ATF750LVC	V750C	Disabled
ATF750LVC (PPK)	V750CPPK	Enabled

Input Diagram



I/O Diagram

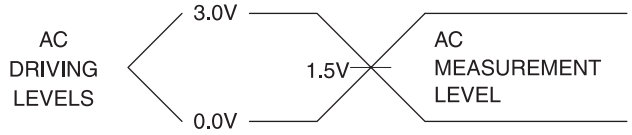


DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = Max, V_{IN} = Max, Outputs Open	C-15	Com.		65	90	mA
				Ind.		70	100	mA
I_{OS}[1][2]	Output Short Circuit Current	V_{OUT} = 0.5V					-120	mA
V_{IL}	Input Low Voltage	3.0 ≤ V_{CC} ≤ 3.6V			-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	I_{OL} = 16 mA	Com., Ind.			0.5	V
			I_{OL} = 12 mA	Mil.			0.5	V
			I_{OL} = 24 mA	Com.			0.8	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	I_{OH} = -2.0 mA		2.4			V

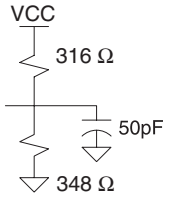
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. This test is performed at initial characterisation only.

Input Test Waveforms and Measurement Levels

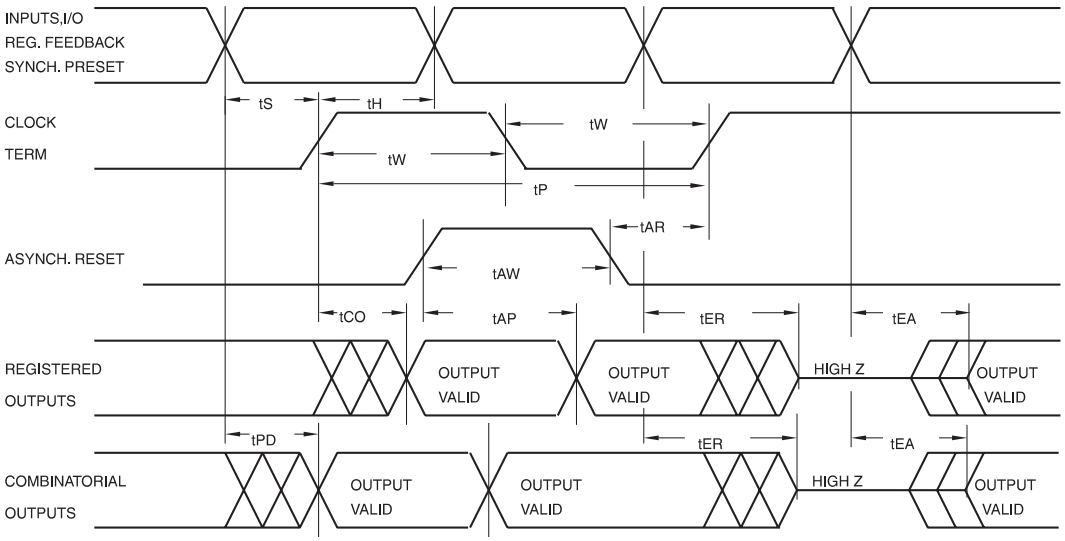


t_R, t_F < 3 ns (10% to 90%)

Output Test Load



AC Waveforms, Product Term Clock(1)



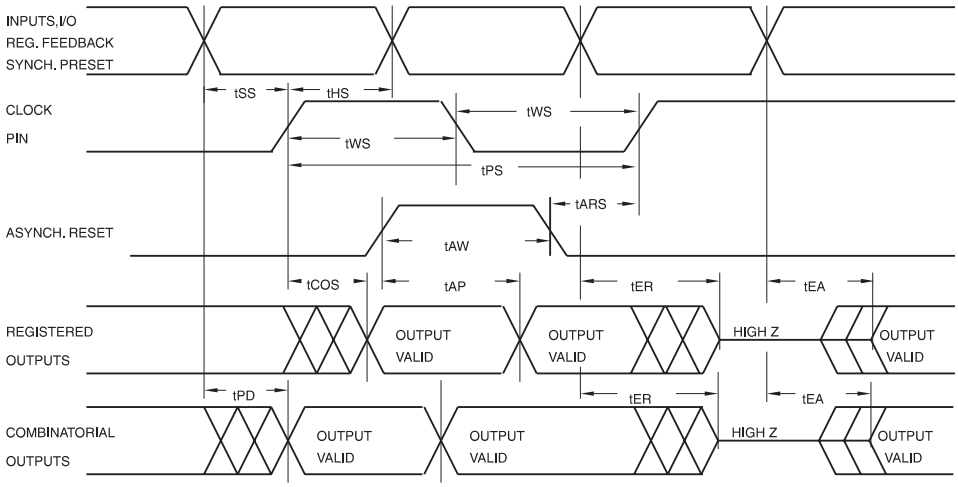
Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

AC Characteristics, Product Term Clock(1)

Symbol	Parameter	-15		Units
		Min	Max	
t_{PD}	Input or Feedback to Non-registered Output		15	ns
t_{EA}	Input to Output Enable		15	ns
t_{ER}	Input to Output Disable		15	ns
t_{CO}	Clock to Output	5	12	ns
t_{CF}	Clock to Feedback	5	9	ns
t_S	Input Setup Time	8		ns
t_{SF}	Feedback Setup Time	7		ns
t_H	Hold Time	5		ns
t_P	Clock Period	14		ns
t_W	Clock Width	7		ns
f_{MAX}	External Feedback $1/(t_S + t_{CO})$		50	MHz
	Internal Feedback $1/(t_{SF} + t_{CF})$		62	MHz
	No Feedback $1/(t_P)$		71	MHz
t_{AW}	Asynchronous Reset Width	15		ns
t_{AR}	Asynchronous Reset Recovery Time	15		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		15	ns
t_{SP}	Setup Time, Synchronous Preset	8		ns

Note: 1. See ordering information for valid part numbers.

AC Waveforms, Input Pin Clock(1)

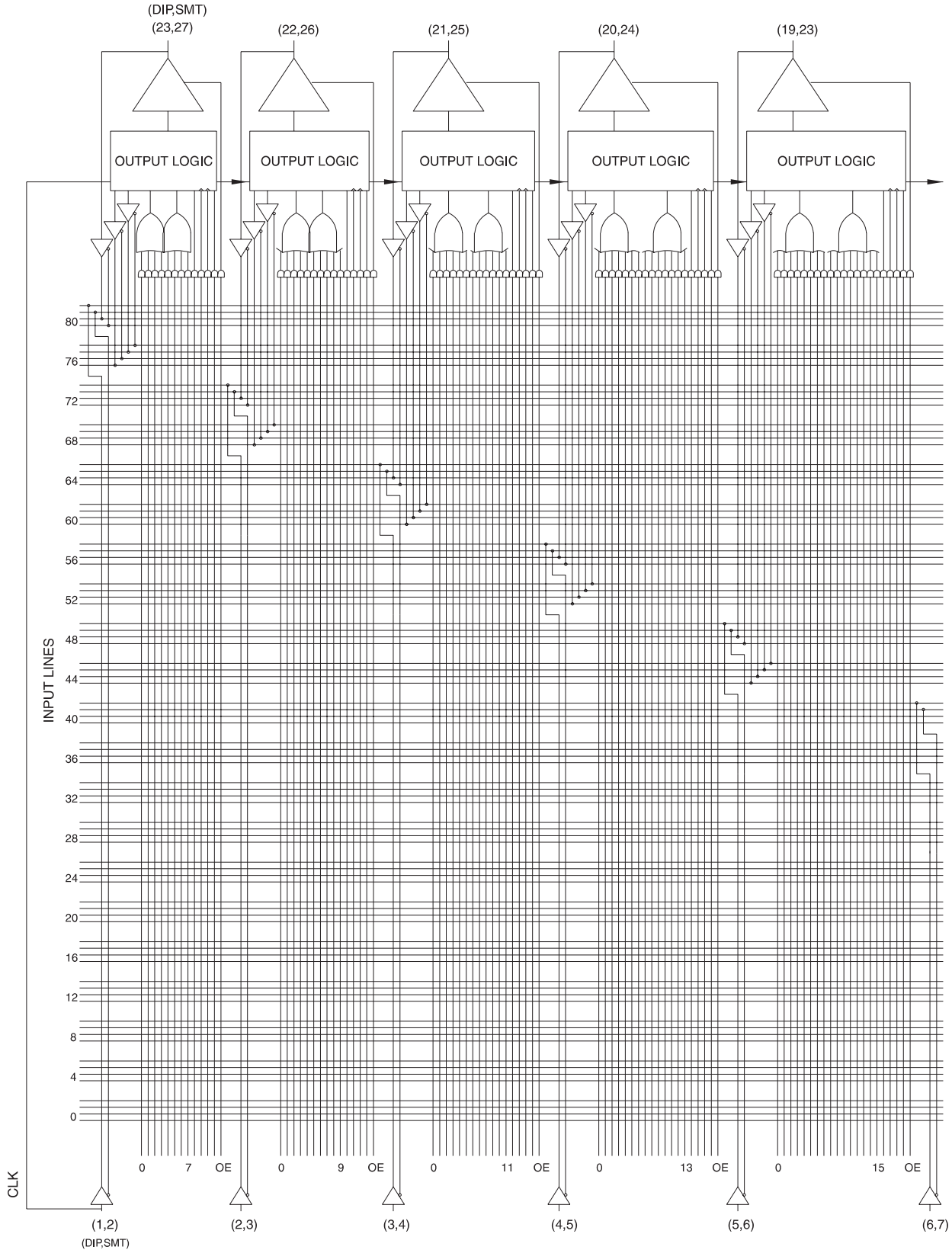


Notes: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

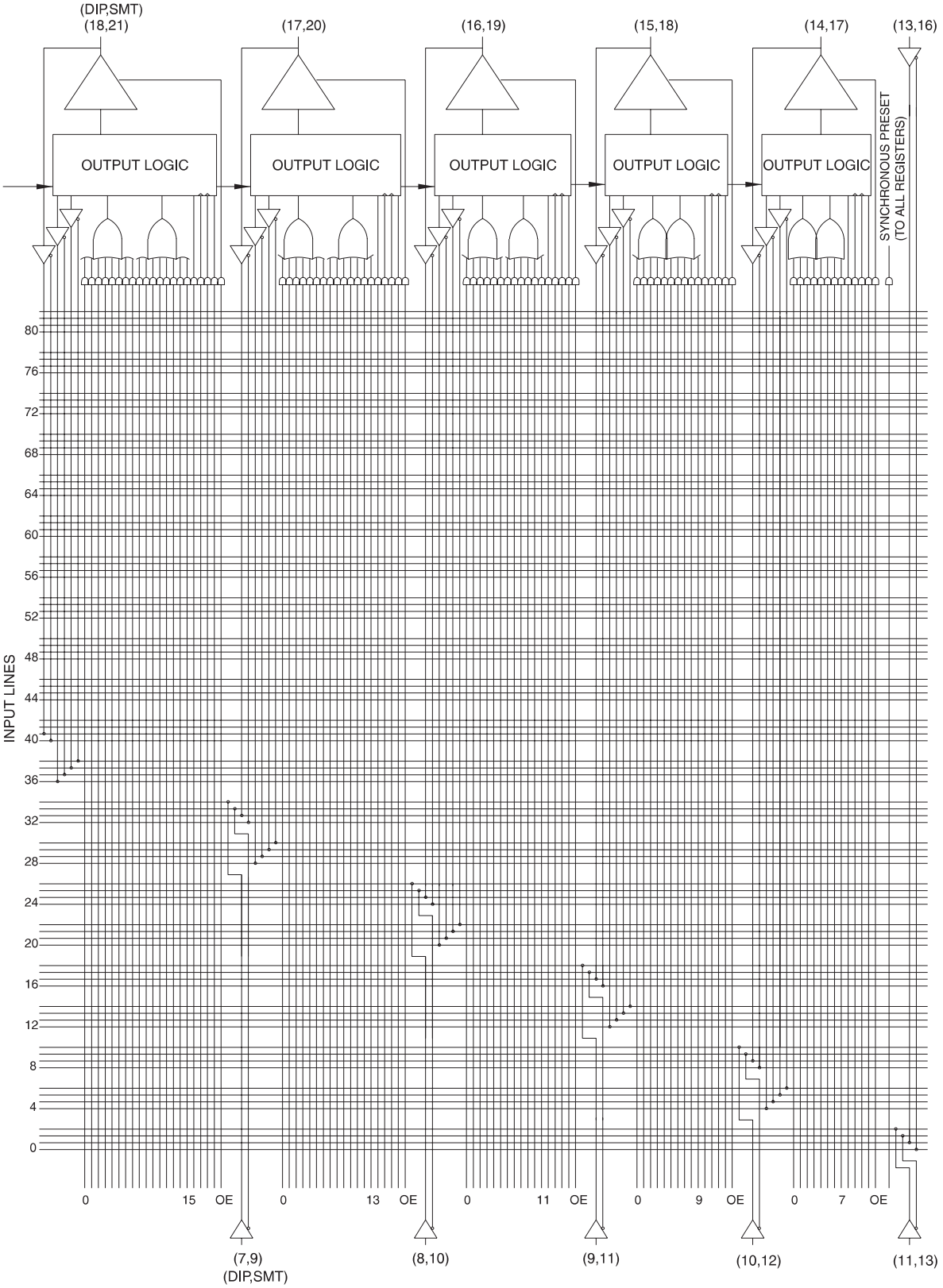
AC Characteristics, Input Pin Clock

Symbol	Parameter	-15		Units
		Min	Max	
t_{PD}	Input or Feedback to Non-registered Output		15	ns
t_{EA}	Input to Output Enable		15	ns
t_{ER}	Input to Output Disable		15	ns
t_{COS}	Clock to Output	0	10	ns
t_{CFS}	Clock to Feedback	0	5.5	ns
t_{SS}	Input Setup Time	8		ns
t_{SFS}	Feedback Setup Time	7		ns
t_{HS}	Hold Time	0		ns
t_{PS}	Clock Period	12		ns
t_{WS}	Clock Width	6		ns
f_{MAXS}	External Feedback $1/(t_{SS} + t_{COS})$		55	MHz
	Internal Feedback $1/(t_{SFS} + t_{CFS})$		80	MHz
	No Feedback $1/(t_{PS})$		83	MHz
t_{AW}	Asynchronous Reset Width	15		ns
t_{ARS}	Asynchronous Reset Recovery Time	15		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		15	ns
t_{SPS}	Setup Time, Synchronous Preset	11		ns

Functional Logic Diagram ATF750LVC, Upper Half



Functional Logic Diagram ATF750LVC, Lower Half



Using the ATF750LVC's Many Advanced Features

The ATF750LVC's advanced flexibility packs more usable gates into 24-pins than any other logic device. The ATF750LVCs start with the popular 22V10 architecture, and add several enhanced features:

- **Selectable D- and T-type Registers**
  Each ATF750LVC flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.
- **Selectable Asynchronous Clocks**
  Each of the ATF750LVC's flip-flops may be clocked by its own clock product term or directly from Pin 1 (SMD Lead 2). This removes the constraint that all registers must use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.
- **A Full Bank of Ten More Registers**
  The ATF750LVC provides two flip-flops per output logic cell for a total of 20. Each register has its own sum term, its own reset term and its own clock term.
- **Independent I/O Pin and Feedback Paths**
  Each I/O pin on the ATF750LVC has a dedicated input path. Each of the 20 registers has its own feedback terms into the array as well. This feature, combined with individual product terms for each I/O's output enable, facilitates true bi-directional I/O design.

Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the ATF750LVC. The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram.

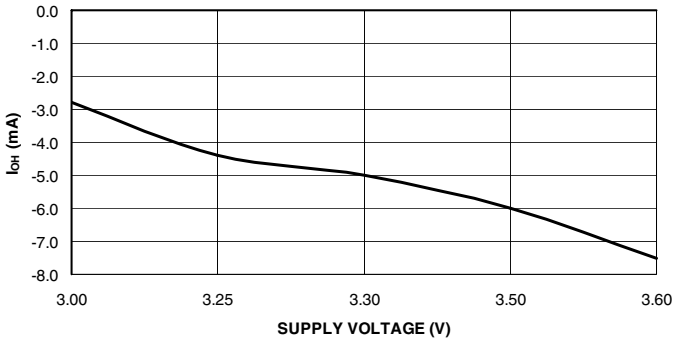
An individual asynchronous reset line is provided for each of the 20 flip-flops. Both master and slave halves of the flip-flops are reset when the input signals received force the internal resets high.

Security Fuse Usage

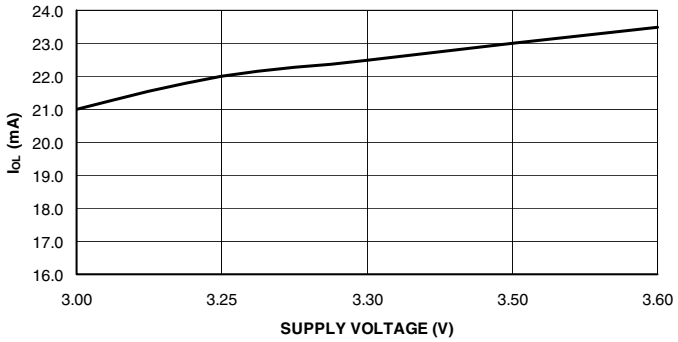
A single fuse is provided to prevent unauthorized copying of the ATF750LVC fuse patterns. Once the security fuse is programmed, all fuses will appear programmed during verify.

The security fuse should be programmed last, as its effect is immediate.

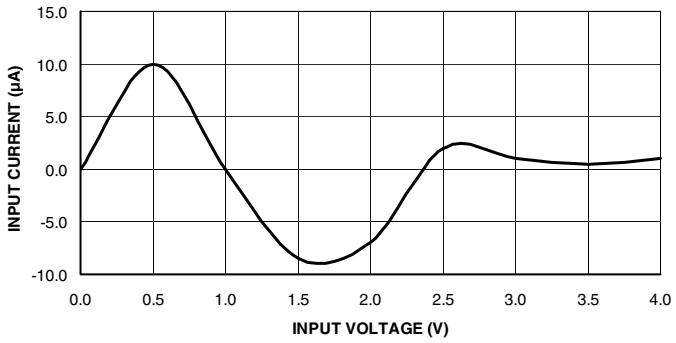
OUTPUT SOURCE CURRENT
VS SUPPLY VOLTAGE (V_{OH} = 2.4V, T_A = 25°C)



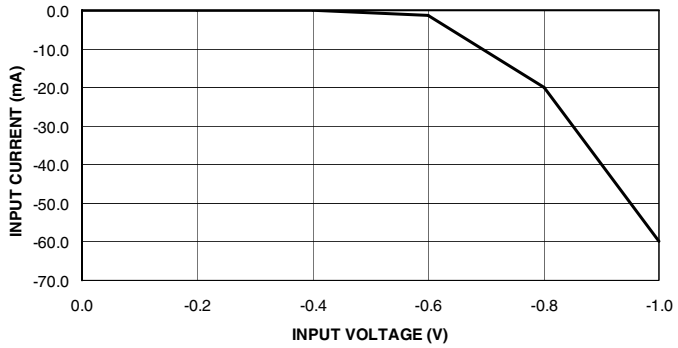
OUTPUT SINK CURRENT
VS SUPPLY VOLTAGE (V_{OL} = 0.5V, T_A = 25°C)



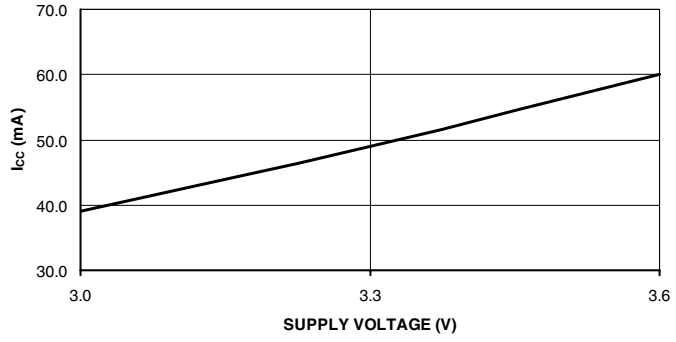
INPUT CURRENT VS
INPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)



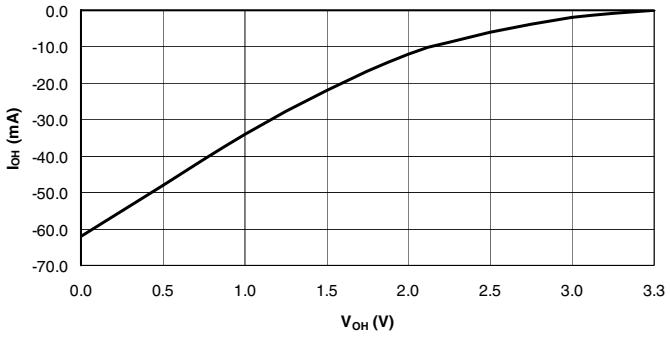
INPUT CLAMP CURRENT VS
INPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)



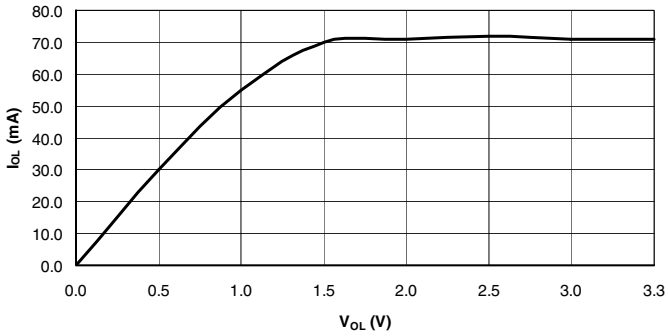
SUPPLY CURRENT
VS SUPPLY VOLTAGE (T_A = 25°C)



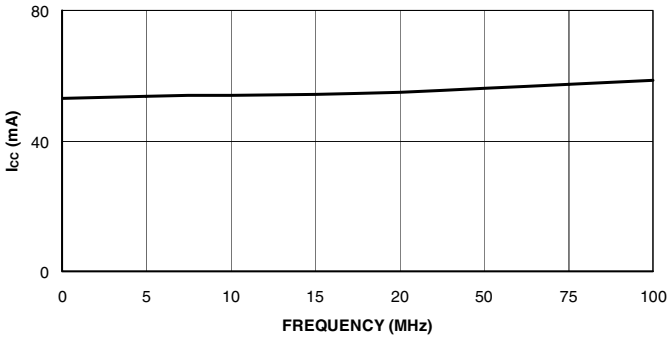
OUTPUT SOURCE CURRENT VS OUTPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)



OUTPUT SOURCE SINK CURRENT VS OUTPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)



SUPPLY CURRENT VS INPUT FREQUENCY (V_{CC} = 5.00V, T_A = 25°C)



ATF750LVC Ordering Information

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MH_z)	Ordering Code	Package	Operation Range
15	10	55	ATF750LVC-15JC ATF750LVC-15PC ATF750LVC-15SC ATF750LVC-15XC(1)	28J 24P3 24S 24X(1)	Commercial (0°C to 70°C)
			ATF750LVC-15JI ATF750LVC-15PI ATF750LVC-15SI ATF750LVC-15X(1)I	28J 24P3 24S 24X(1)	Industrial (-40°C to 85°C)

Note: 1. Special order only; TSSOP package requires special thermal management.

ATF750LVC Green Package Options (Pb/Halide-free/RoHS Compliant)

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MH_z)	Ordering Code	Package	Operation Range
15	10	55	ATF750LVC-15JU ATF750LVC-15PU ATF750LVC-15SU ATF750LVC-15XU	28J 24P3 24S 24X	Industrial (-40°C to 85°C)

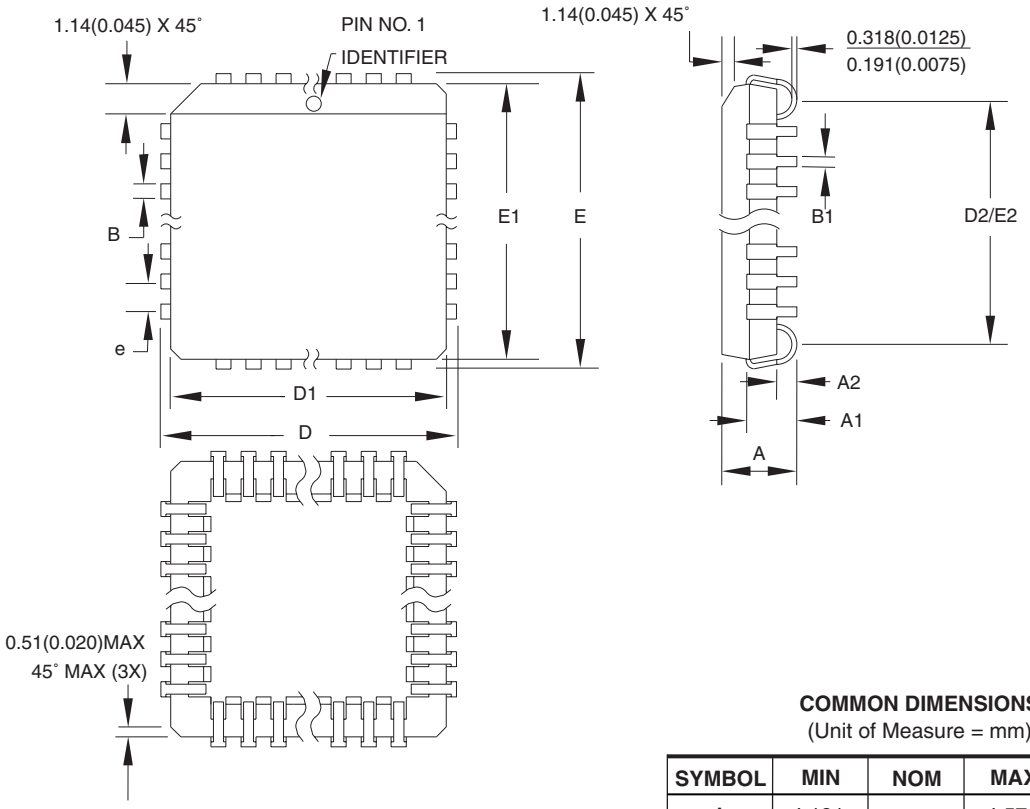
Using “C” Product for Industrial

Because the V_{CC} conditions are the same for commercial and industrial for 3.3V products, and there is only 15°C difference at the high end of the temperature range, there is very little risk in using “C” devices for industrial applications. Just de-rate I_{CC} by 15%.

Package Type	
28J	28-Lead, Plastic J-leaded Chip Carrier (PLCC)
24P3	24-lead, 0.300’ Wide, Plastic Dual Inline Package (PDIP)
24S	24-lead, 0.300” Wide, Plastic Gull Wing Small Outline (SOIC)
24X*	24-lead, 0.173” Wide, Thin Shrink Small Outline (TSSOP)

Package Information

28J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

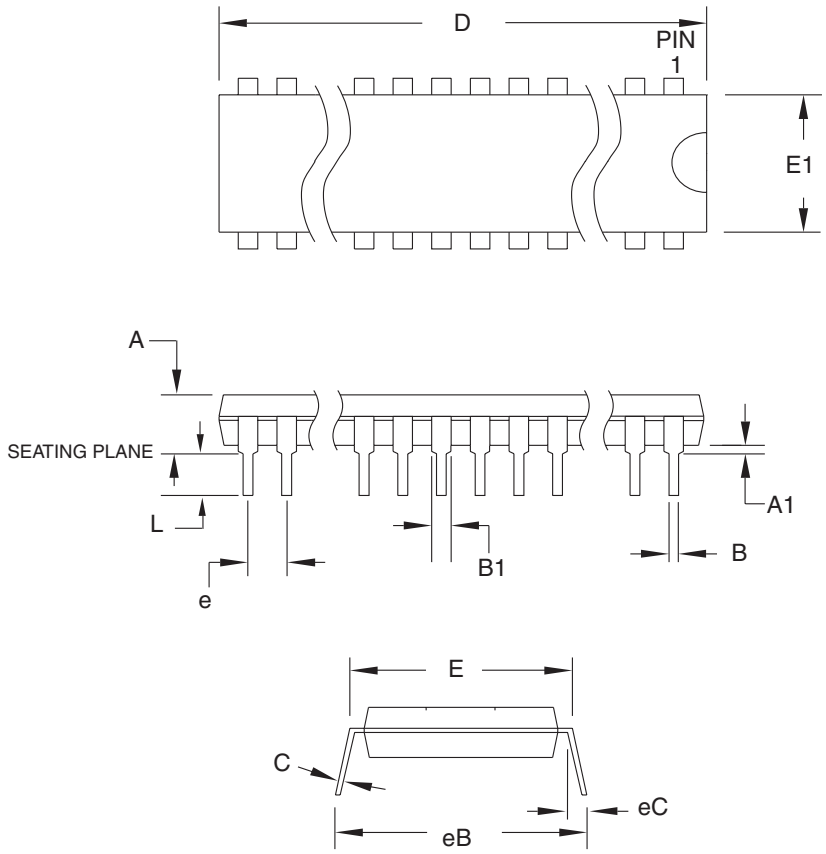
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	12.319	–	12.573	
D1	11.430	–	11.582	Note 2
E	12.319	–	12.573	
E1	11.430	–	11.582	Note 2
D2/E2	9.906	–	10.922	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28J**, 28-lead, Plastic J-leaded Chip Carrier (PLCC)	28J	B

24P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

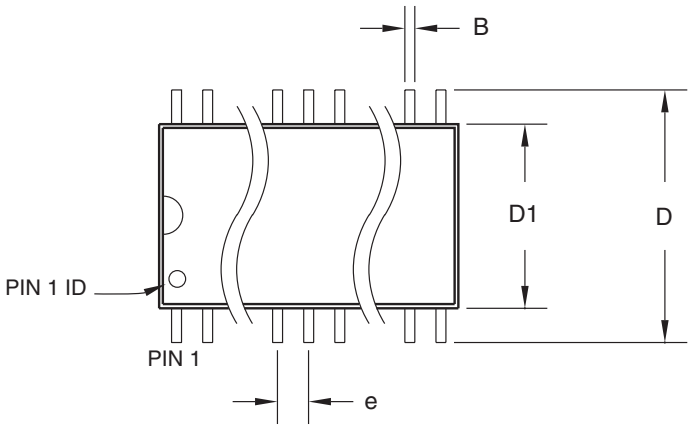
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	31.623	–	32.131	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.651	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

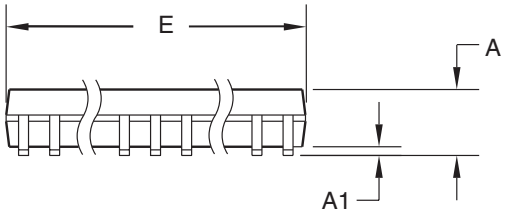
Notes:
1. This package conforms to JEDEC reference MS-001, Variation AF.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

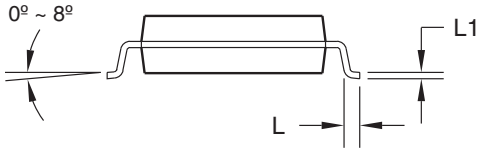
6/1/04

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**24P3**, 24-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	24P3	D

24S – SOIC







COMMON DIMENSIONS
(Unit of Measure = mm)

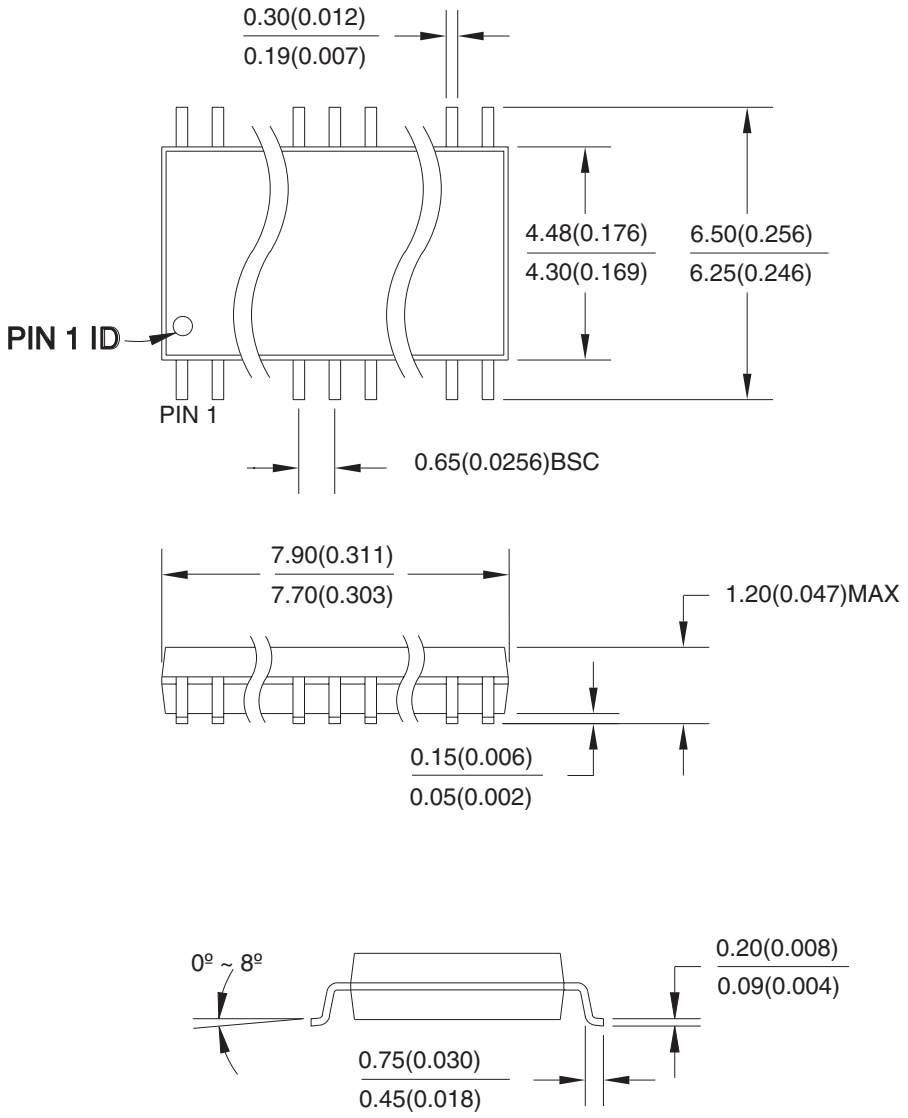
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	2.65	
A1	0.10	–	0.30	
D	10.00	–	10.65	
D1	7.40	–	7.60	
E	15.20	–	15.60	
B	0.33	–	0.51	
L	0.40	–	1.27	
L1	0.23	–	0.32	
e	1.27 BSC			

06/17/2002

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**24S**, 24-lead (0.300" body) Plastic Gull Wing Small Outline (SOIC)	24S	B

24X – TSSOP

Dimensions in Millimeter and (Inches)*
JEDEC STANDARD MO-153 AD
Controlling dimension: millimeters



04/11/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**24X**, 24-lead (4.4 mm body width) Plastic Thin Shrink Small Outline Package (TSSOP)	24X	A

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