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FAST SWITCHING THYRISTOR

ATF1040

Repetitive voltage up to

2000 V

Mean on-state current

1075 A

Surge current

14 kA

Turn-off time

50 μs

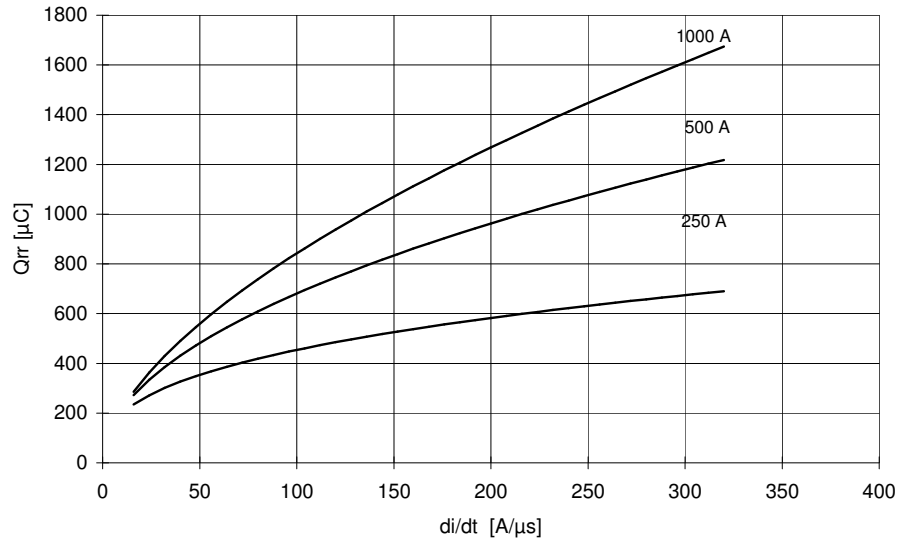
FINAL SPECIFICATION

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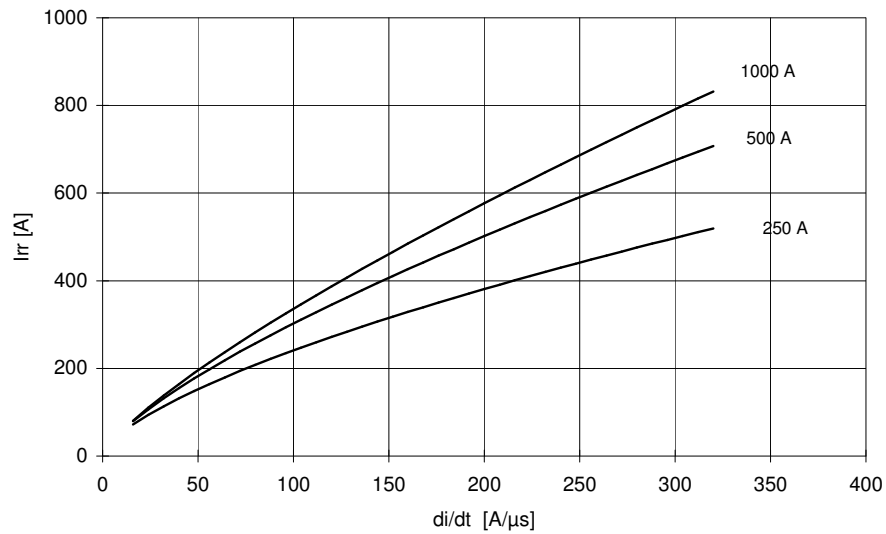
Symbol	Characteristic	Conditions	T _J [°C]	Value	Unit		
BLOCKING							
V _{RRM}	Repetitive peak reverse voltage		125	2000	V		
V _{RSM}	Non-repetitive peak reverse voltage		125	2100	V		
V _{DRM}	Repetitive peak off-state voltage		125	2000	V		
I _{RRM}	Repetitive peak reverse current	V=VRRM	125	150	mA		
I _{DRM}	Repetitive peak off-state current	V=VDRM	125	150	mA		
CONDUCTING							
I _{T(AV)}	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		1075	A		
I _{T(AV)}	Mean on-state current	180° sin, 1 kHz, Th=55°C, double side cooled		1000	A		
I _{TSM}	Surge on-state current, non repetitive	sine wave, 10 ms	125	14	kA		
I ² t	I ² t	without reverse voltage		980 x1E3	A ² s		
V _T	On-state voltage	On-state current = 2000 A	25	2,6	V		
V _{T(TO)}	Threshold voltage		125	1,40	V		
r _T	On-state slope resistance		125	0,414	mohm		
SWITCHING							
di/dt	Critical rate of rise of on-state current, min	From 75% VDRM up to 1200 A, gate 10V 5 ohm	125	500	A/μs		
dv/dt	Critical rate of rise of off-state voltage, min	Linear ramp up to 70% of VDRM	125	500	V/μs		
td	Gate controlled delay time, typical	VD=100V, gate source 20V, 10 ohm, tr=1 μs	25	0,6	μs		
tq	Circuit commutated turn-off time	di/dt = 20 A/μs, I _L = 800 A dV/dt = 200 V/μs, up to 75% VDRM	125	50	μs		
Q _{rr}	Reverse recovery charge	di/dt = 60 A/μs, I _L = 1000 A	125	620	μC		
I _{rr}	Peak reverse recovery current	VR = 50 V		227	A		
I _H	Holding current, typical	VD=5V, gate open circuit	25	500	mA		
I _L	Latching current, typical	VD=5V, tp=30μs	25	850	mA		
GATE							
V _{GT}	Gate trigger voltage	VD=5V	25	3,5	V		
I _{GT}	Gate trigger current	VD=5V	25	350	mA		
V _{GD}	Non-trigger gate voltage, min.	VD=VDRM	125	0,25	V		
V _{FGM}	Peak gate voltage (forward)		25	30	V		
I _{FGM}	Peak gate current		25	10	A		
V _{FGM}	Peak gate voltage (reverse)		25	5	V		
P _{GM}	Peak gate power dissipation	Pulse width 100 μs	25	150	W		
P _{G(AV)}	Average gate power dissipation		25	3	W		
MOUNTING							
R _{th(j-h)}	Thermal impedance, DC	Junction to heatsink, double side cooled		26	°C/kW		
R _{th(c-h)}	Thermal impedance, DC	Case to heatsink, double side cooled		6	°C/kW		
T _j	Operating junction temperature			-30 / 125	°C		
F	Mounting force			14.0 / 17.0	kN		
	Mass			500	g		
ORDERING INFORMATION : ATF1040 S 20 S tq code standard specification VDRM&VRRM/100			D 10 μs	C 12 μs	B 15 μs	A 20 μs	L 25 μs
			M 30 μs	N 35 μs	P 40 μs	R 45 μs	S 50 μs
			T 60 μs	U 70 μs	W 80 μs	X 100 μs	Y 150 μs

SWITCHING CHARACTERISTICS

REVERSE RECOVERY CHARGE
 $T_j = 125\text{ }^\circ\text{C}$



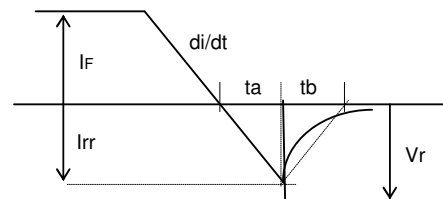
REVERSE RECOVERY CURRENT
 $T_j = 125\text{ }^\circ\text{C}$



$$t_a = I_{rr} / (di/dt) \quad t_b = t_{rr} - t_a$$

$$\text{Softness (s factor)} \quad s = t_b / t_a$$

$$\text{Energy dissipation during recovery } E_r = V_r \cdot (Q_{rr} - I_{rr} \cdot t_a / 2)$$

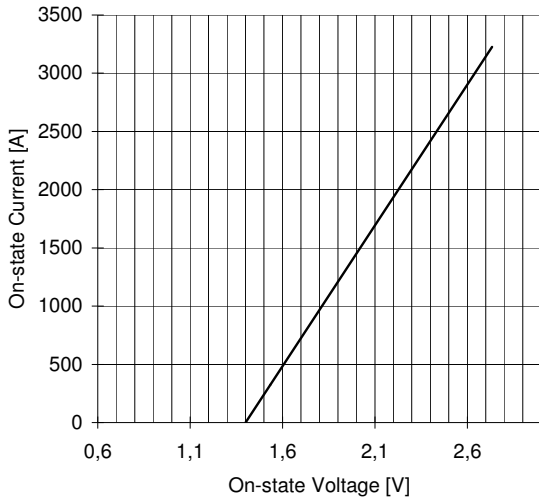


ATF1040 FAST SWITCHING THYRISTOR

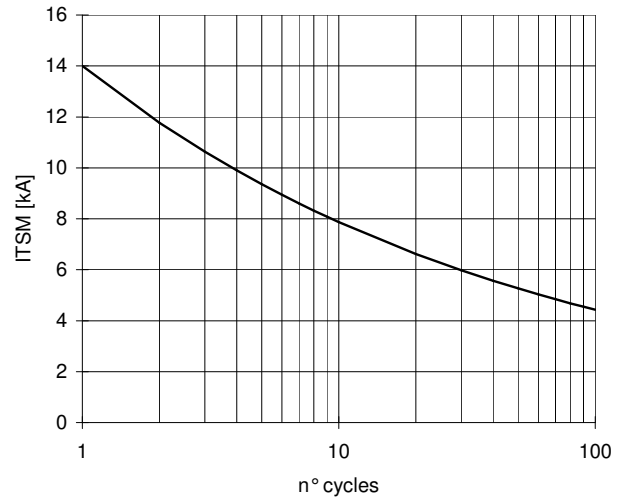


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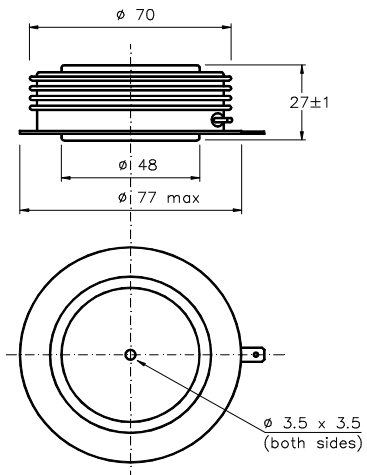
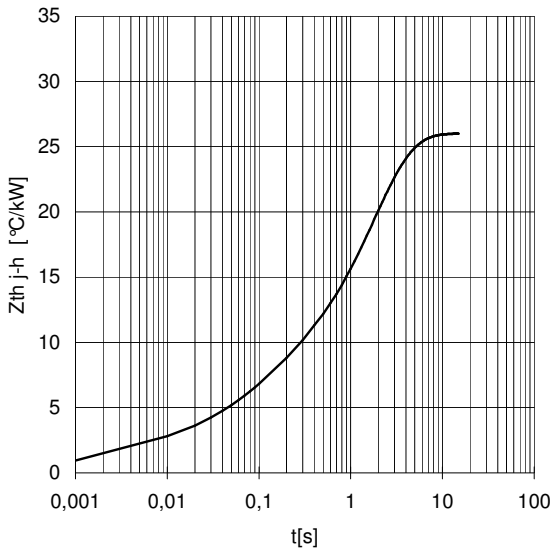
ON-STATE CHARACTERISTIC
T_j = 125 °C



SURGE CHARACTERISTIC
T_j = 125 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED



Dimensions
in mm



Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 μm.

In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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