DAC1408D650

Dual 14-bit DAC, up to 650 Msps, 2× and 4× interpolating with JESD204A interface

Rev. 01 — 26 May 2009 Objective data sheet

1. General description

The DAC1408D650 is a high-speed 14-bit dual channel Digital-to-Analog Converter (DAC) with selectable 2× or 4× interpolating filters optimized for multi-carriers WCDMA transmitters.

Thanks to its digital on-chip modulation, the DAC1408D650 allows the complex I and Q inputs to be converted up from baseband to IF. The mixing frequency is adjusted via a Serial Peripheral Interface (SPI) with a 32-bit Numerically Controlled Oscillator (NCO) and the phase is controlled by a 16-bit register.

The DAC1408D650 also includes a 2× and 4× clock multiplier which provides the appropriate internal clocks and an internal regulation to adjust the output full scale current.

The input data format is serial according to JESD204A specification. This new interface has numerous advantages over the traditional parallel one: easy PCB layout, lower radiated noise, lower pin count, self-synchronous link, skew compensation. DAC1408D650 maximum number of lanes is 4 and its maximum serial data rate is 3.25 Gbps.

2. Features

- Dual 14-bit resolution
- 650 Msps maximum update rate
- Four JESD204A serial input lanes
- Differential CML receiver with termination
- LMF = 421 or LMF = 211 support
- Input data rate up to 325 Msps or 162.5 Msps
- Selectable 2× or 4× interpolation filters
- Two's complement or Binary Offset Data Format (BODF)
- Very low noise cap free integrated PLL
- SFDR: −75 dBc; f_s = 640 Msps; f_o = 4 MHz
- IMD3: 74 dBc; f_s = 640 Msps; f_o = 154 MHz
- Inverse (sin x) / x function
- Embedded complex modulator
- 3 or 4 wire SPI configuration interface
- Differential scalable output current from 1.6 mA to 22 mA
- External analog offset control (10-bit auxiliary DACs)
- Internal digital offset control
- On-chip 1.25 V reference

- 32-bit programmable NCO frequency
- Low power NCO option
- LVDS compatible clock inputs
- Industrial temperature range from −40 °C to +85 °C
- Typical power dissipation: 1.19 W
- Power down and Sleep modes

3. Applications

- Wireless infrastructure: LTE, WiMAX, GSM, CDMA, WCDMA, TD-SCDMA
- Communication: LMDS/MMDS, point to point
- Direct Digital Synthesis (DDS)
- Broadband wireless systems
- Digital radio links
- Instrumentation
- Automated Test Equipment (ATE)

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
DAC1408D650HW/C1	HTQFP100	plastic thermal enhanced thin quad flat package; 100 leads; body 14 × 14 × 1 mm; exposed die pad	SOT638-1

5. Block diagram

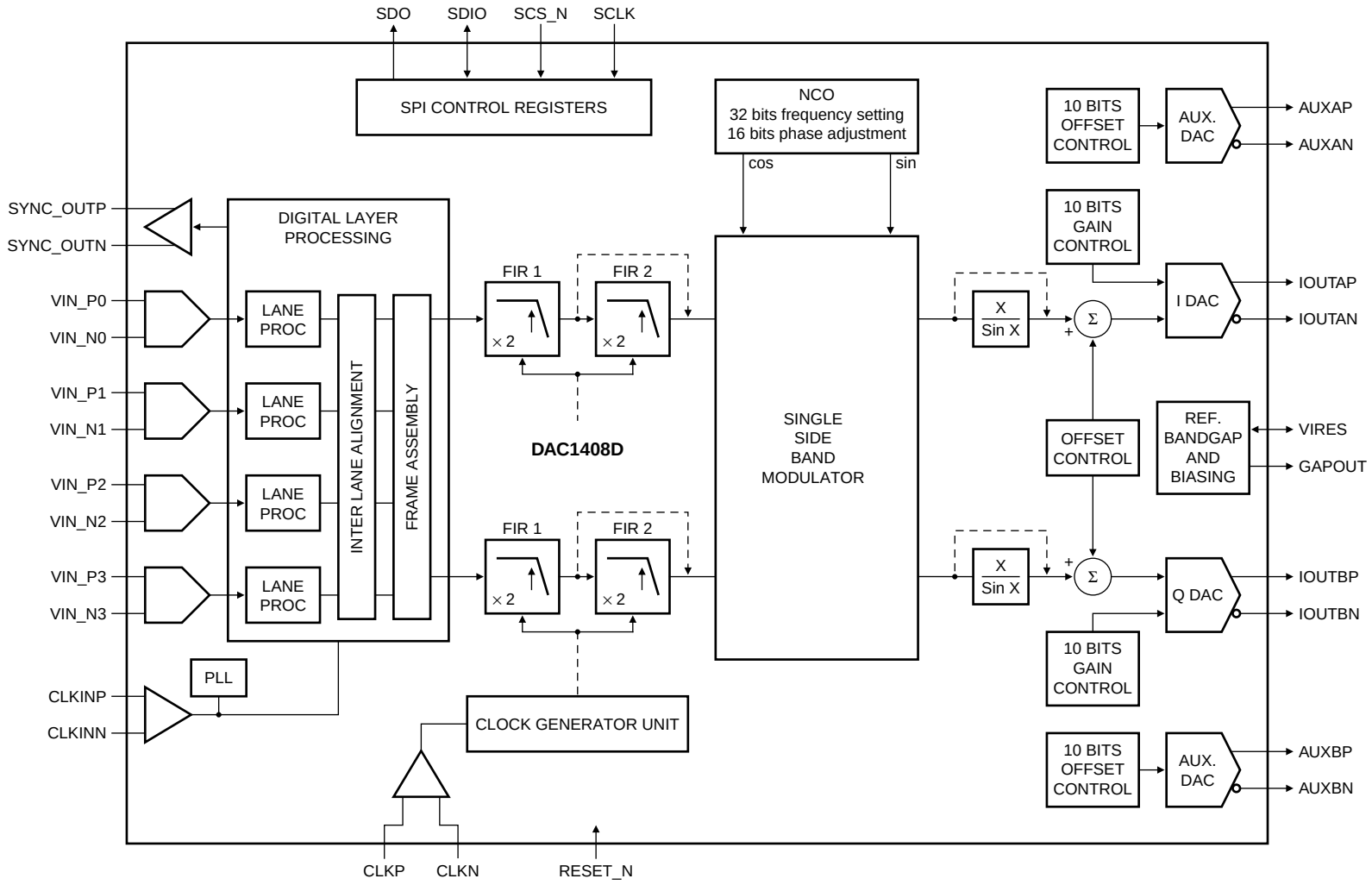


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

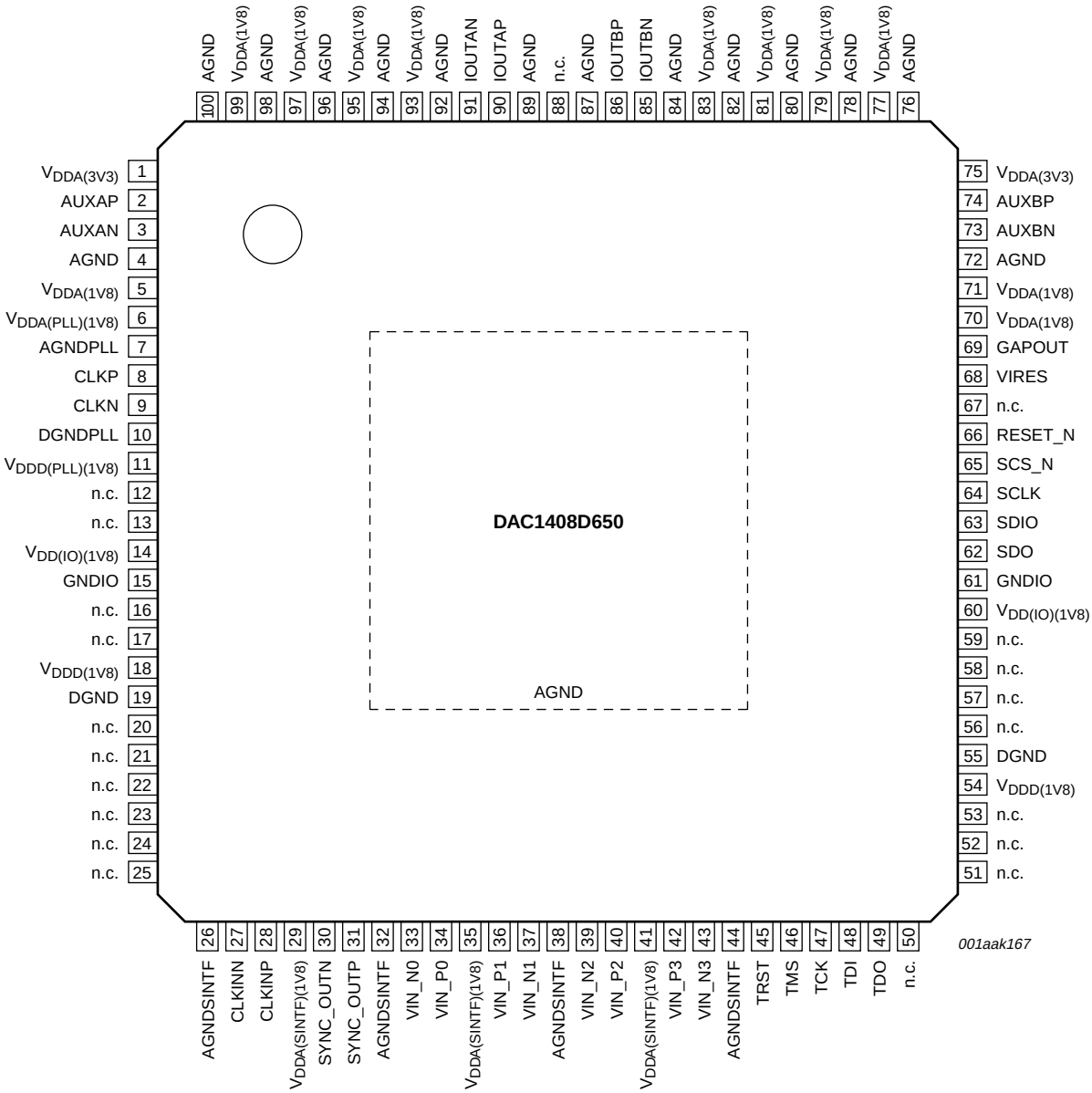


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
$V_{DDA(3V3)}$	1	P	analog supply voltage 3.3 V
AUXAP	2	O	auxiliary DAC B output current
AUXAN	3	O	complementary auxiliary DAC B output current
AGND	4	G	analog ground
$V_{DDA(1V8)}$	5	P	analog supply voltage 1.8 V
$V_{DDA(PLL)(1V8)}$	6	P	PLL analog supply voltage 1.8 V
AGNDPLL	7	G	PLL analog ground
CLKP	8	I	clock input
CLKN	9	I	complementary clock input
DGNDPLL	10	G	PLL digital ground
$V_{DDD(PLL)(1V8)}$	11	P	PLL digital supply voltage 1.8 V
n.c.	12	-	not connected
n.c.	13	-	not connected
$V_{DD(IO)(1V8)}$	14	P	input/output buffers supply voltage 1.8 V
GNDIO	15	G	input/output buffers ground
n.c.	16	-	not connected
n.c.	17	-	not connected
$V_{DDD(1V8)}$	18	P	digital supply voltage 1.8 V
DGND	19	G	digital ground
n.c.	20	-	not connected
n.c.	21	-	not connected
n.c.	22	-	not connected
n.c.	23	-	not connected
n.c.	24	-	not connected
n.c.	25	-	not connected
AGNDSINTF	26	G	serial interface analog ground
CLKINN	27	I	serial interface frame complementary clock input
CLKINP	28	I	serial interface frame clock input
$V_{DDA(SINTF)(1V8)}$	29	P	serial interface analog supply voltage 1.8 V
SYNC_OUTN	30	O	sync request to transmitter, complementary output
SYNC_OUTP	31	O	sync request to transmitter
AGNDSINTF	32	G	serial interface analog ground
VIN_N0	33	I	serial interface lane 0 negative input
VIN_P0	34	I	serial interface lane 0 positive input
$V_{DDA(SINTF)(1V8)}$	35	P	serial interface analog supply voltage 1.8 V
VIN_P1	36	I	serial interface lane 1 positive input
VIN_N1	37	I	serial interface lane 1 negative input
AGNDSINTF	38	G	serial interface analog ground
VIN_N2	39	I	serial interface lane 2 negative input

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
VIN_P2	40	I	serial interface lane 2 positive input
$V_{DDA(SINTF)(1V8)}$	41	P	serial interface analog supply voltage 1.8 V
VIN_P3	42	I	serial interface lane 3 positive input
VIN_N3	43	I	serial interface lane 3 negative input
AGNDSINTF	44	G	serial interface analog ground
TRST	45	I	JTAG Test Reset. Must be tied to GND.
TMS	46	I	JTAG Test Mode Select
TCK	47	I	JTAG Test Clock
TDI	48	I	JTAG Test Data In
TDO	49	O	JTAG Test Data Out
n.c.	50	-	not connected
n.c.	51	-	not connected
n.c.	52	-	not connected
n.c.	53	-	not connected
$V_{DDD(1V8)}$	54	P	digital supply voltage 1.8 V
DGND	55	G	digital ground
n.c.	56	-	not connected
n.c.	57	-	not connected
n.c.	58	-	not connected
n.c.	59	-	not connected
$V_{DD(IO)(1V8)}$	60	P	input/output buffers supply voltage 1.8 V
GNDIO	61	G	input/output buffers ground
SDO	62	O	SPI data output
SDIO	63	I/O	SPI data input/output
SCLK	64	I	SPI clock
SCS_N	65	I	SPI chip select (active LOW)
RESET_N	66	I	general reset (active LOW)
n.c.	67	-	not connected
VIRES	68	I/O	DAC biasing resistor
GAPOUT	69	O	bandgap input/output voltage
$V_{DDA(1V8)}$	70	P	analog supply voltage 1.8 V
$V_{DDA(1V8)}$	71	P	analog supply voltage 1.8 V
AGND	72	G	analog ground
AUXBN	73	O	auxiliary DAC B output
AUXBP	74	O	complementary auxiliary DAC B output
$V_{DDA(3V3)}$	75	P	analog supply voltage 3.3 V
AGND	76	G	analog ground
$V_{DDA(1V8)}$	77	P	analog supply voltage 1.8 V
AGND	78	G	analog ground
$V_{DDA(1V8)}$	79	P	analog supply voltage 1.8 V
AGND	80	G	analog ground

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
$V_{DDA(1V8)}$	81	P	analog supply voltage 1.8 V
AGND	82	G	analog ground
$V_{DDA(1V8)}$	83	P	analog supply voltage 1.8 V
AGND	84	G	analog ground
IOUTBN	85	O	complementary DAC B output current
IOUTBP	86	O	DAC B output current
AGND	87	G	analog ground
n.c.	88	-	not connected
AGND	89	G	analog ground
IOUTAP	90	O	DAC A output current
IOUTAN	91	O	complementary DAC A output current
AGND	92	G	analog ground
$V_{DDA(1V8)}$	93	P	analog supply voltage 1.8 V
AGND	94	G	analog ground
$V_{DDA(1V8)}$	95	P	analog supply voltage 1.8 V
AGND	96	G	analog ground
$V_{DDA(1V8)}$	97	P	analog supply voltage 1.8 V
AGND	98	G	analog ground
$V_{DDA(1V8)}$	99	P	analog supply voltage 1.8 V
AGND	100	G	analog ground
AGND	H[2]	G	analog ground

[1] P: power supply; G: ground; I: input; O: output.

[2] H = heatsink (exposed die pad to be soldered)

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(IO)}$	input/output supply voltage		[1]	–0.5	+2.5	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		[1]	–0.5	+4.6	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)		[2]	–0.5	+2.5	V
V_{DDD}	digital supply voltage		[2]	–0.5	+2.5	V
$V_{DDA(PLL)}$	PLL analog supply voltage		[2]	–0.5	+2.5	V
$V_{DDD(PLL)}$	PLL digital supply voltage		[2]	–0.5	+2.5	V
$V_{DD(sintf)}$	serial interface supply voltage	JESD204A compliant		–0.5	+2.5	
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
T_j	junction temperature			–40	125	°C

[1] The supply voltage $V_{DDA(3V3)}$ may have any value between –0.5 V and +4.6 V provided that the supply voltage differences ΔV_{CC} are respected.

[2] The supply voltages $V_{DDA(1V8)}$, V_{DDD}, $V_{DDA(PLL)}$, $V_{DDD(PLL)}$, $V_{DD(IO)}$ and $V_{DD(sintf)}$ may have any value between –0.5 V and +2.5 V provided that the supply voltage differences ΔV_{CC} are respected.

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	19.8	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	7.7	K/W

[1] In compliance with JEDEC test board, in free air.

9. Characteristics

Table 5. Characteristics

$V_{DDA(1V8)}$ = $V_{DD(PLL)}$ = V_{DDD} = $V_{DD(IO)}$ = $VDD_{(sintf)}$ = 1.65 V to 1.95 V; $V_{DDA(3V3)}$ = 3.0 V to 3.6 V; AGND, GND(PLL), DGND and GNDIO are shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at $V_{DDA(1V8)}$ = $V_{DD(PLL)}$ = V_{DDD} = $V_{DD(IO)}$ = $V_{DD(sintf)}$ = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
$V_{DD(IO)}$	input/output supply voltage		I	1.65	1.8	1.95	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		I	3.0	3.3	3.6	V
V_{DDD}	digital supply voltage		I	1.65	1.8	1.95	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)		I	1.65	1.8	1.95	V
$V_{DDA(PLL)}$	PLL analog supply voltage		I	1.65	1.8	1.95	V
$V_{DDD(PLL)}$	PLL digital supply voltage		I	1.65	1.8	1.95	V
$V_{DD(sintf)}$	serial interface supply voltage	JESD204A compliant	I	1.65	1.8	1.95	V
$I_{DD(IO)}$	input/output supply current	f_o = 19 MHz; f_s = 640 Msps; 2× interpolation; NCO on	I	-	10	-	mA
$I_{DDA(3V3)}$	analog supply current (3.3 V)	f_o = 19 MHz; f_s = 640 Msps; 2× interpolation; NCO on	I	-	43	-	mA
I_{DDD}	digital supply current.	f_o = 19 MHz; f_s = 640 Msps; 2× interpolation; NCO on	I	-	230	-	mA
$I_{DDA(1V8)}$	analog supply current, (1.8 V)	including PLL; f_o = 19 MHz; NCO on; f_s = 640 Msps; 2× interpolation;	I	-	350	-	mA
$I_{DD(sintf)}$	serial interface supply current	JESD204A compliant; f_o = 19 MHz; f_s = 640 Msps; 2× interpolation; NCO on	I	-	83	-	mA
ΔI_{DDD}	digital supply current difference	X/sin X function on	I	-	40	-	mA

Table 5. Characteristics *...continued*

$V_{DDA(1V8)}$ = $V_{DD(PLL)}$ = V_{DDD} = $V_{DD(IO)}$ = $VDD_{(sintf)}$ = 1.65 V to 1.95 V; $V_{DDA(3V3)}$ = 3.0 V to 3.6 V; AGND, GND(PLL), DGND and GNDIO are shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at $V_{DDA(1V8)}$ = $V_{DD(PLL)}$ = V_{DDD} = $V_{DD(IO)}$ = $V_{DD(sintf)}$ = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
P_{tot}	total power dissipation	f_s = 640 Msps; 4× interpolation; NCO off; DAC Q off	C	-	tbd	-	W
		f_s = 640 Msps; 4× interpolation; NCO off	C	-	1.15	-	W
		f_s = 640 Msps; 4× interpolation; NCO on	C	-	1.19	-	W
		f_s = 640 Msps; 2× interpolation; NCO off	C	-	1.29	-	W
		f_s = 640 Msps; 2× interpolation; NCO on	C	-	1.34	-	W
		f_s = 640 Msps; 2× interpolation; NCO Low Power on	C	-	tbd	-	W
		Power-down mode					
		DAC A and DAC B power-down	I	-	0.48	-	W
		DAC A, DAC B and JESD204A power down	I	-	0.17	-	W
		DAC A and DAC B Sleep mode	I	-	0.88	-	W
Clock inputs (CLKP, CLKN, CLKINN, CLKINP)[2]							
V_i	input voltage	range, CLK+ or CLK− $\lvert V_{gpd}\rvert$ < 50 mV[4]	C	825	-	1575	mV
V_{idth}	input differential threshold voltage	$\lvert V_{gpd}\rvert$ < 50 mV[4]	C	−100	-	+100	mV
R_i	input resistance		D	-	10	-	MΩ
C_i	input capacitance		D	-	0.5	-	pF
Digital inputs (SDO, SDIO, SCLK, SCS_N, RESET_N)							
V_{IL}	LOW-level input voltage		C	GNDIO	-	0.35 × $V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage		C	0.65 × $V_{DD(IO)}$	-	$V_{DD(IO)}$	V
I_{IL}	LOW-level input current	V_{IL} = 1 V	I	-	1	-	µA
I_{IH}	HIGH-level input current	V_{IH} = 2.3 V	I	-	1	-	µA
Digital inputs (Vin_p/Vin_n)[7]							
$V_{I(cm)}$	common-mode input voltage		C	0.68	0.78	1.40	V
$V_{I(dif)(p-p)}$	peak-to-peak differential input voltage		C	175	-	1000	mV

Table 5. Characteristics *...continued*

$V_{DDA(1V8)}$ = $V_{DD(PLL)}$ = V_{DDD} = $V_{DD(IO)}$ = $VDD_{(sintf)}$ = 1.65 V to 1.95 V; $V_{DDA(3V3)}$ = 3.0 V to 3.6 V; AGND, GND(PLL), DGND and GNDIO are shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at $V_{DDA(1V8)}$ = $V_{DD(PLL)}$ = V_{DDD} = $V_{DD(IO)}$ = $V_{DD(sintf)}$ = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Z_{tt}	V_{tt} source impedance			-	0.7	-	Ω
ΔZ_i	differential input impedance			-	100	-	Ω
Digital outputs (SYNC_OUTN/SYNC_OUTP)[3]							
$V_{o(cm)}$	common-mode output voltage		C	0.79	0.98	1.46	V
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage		C	0.12	0.48	0.96	V
Analog outputs (IOUTAP, IOUTAN, IOUTBP, IOUTBN)							
$I_{O(fs)}$	full-scale output current	reg value = 00h	D	-	1.6	-	mA
		reg = default value		-	20	-	mA
V_O	output voltage	compliance range	C	1.8	-	$V_{DDA(3V3)}$	V
R_o	output resistance		D	-	250	-	kΩ
C_o	output capacitance		D	-	3	-	pF
$N_{DAC(mono)}$	DAC monotonicity	guaranteed	D	-	tbd	-	bits
ΔE_O	offset error variation		C	-	tbd	-	ppm/°C
ΔE_G	gain error variation		C	-	tbd	-	ppm/°C
Reference voltage output (GAPOUT)							
$V_{O(ref)}$	reference output voltage		I	tbd	1.25	tbd	V
$I_{O(ref)}$	reference output current	external voltage 1.2 V	C	-	39	-	µA
$\Delta V_{O(ref)}$	reference output voltage variation		C	-	131	-	ppm/°C
Analog Auxiliary outputs (AUXAP, AUXAN, AUXBP and AUXBN)							
$I_{O(aux)}$	auxiliary output current	differential outputs	I	-	2.2	-	mA
$V_{O(aux)}$	auxiliary output voltage	compliance range	C	0	-	2	V
$N_{DAC(aux)mono}$	auxiliary DAC monotonicity	guaranteed	D	-	10	-	bits
Input timing (Vin_p / Vin_n)							
f_{data}	data rate	2× interpolation	C	tbd	-	325	Msps
		4× interpolation		tbd	-	162.5	Msps
f_{bit}	bit rate	serial input		tbd	-	3.25	Gbps
Output timing (IOUTAP, IOUTAN, IOUTBP, IOUTBN)							
f_s	sampling frequency			-	-	650	Msps
t_s	settling time	up to 0.5 LSB	D	-	20	-	ns

Table 5. Characteristics *...continued*

$V_{DDA(1V8)}$ = $V_{DD(PLL)}$ = V_{DDD} = $V_{DD(IO)}$ = $VDD_{(sintf)}$ = 1.65 V to 1.95 V; $V_{DDA(3V3)}$ = 3.0 V to 3.6 V; AGND, GND(PLL), DGND and GNDIO are shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at $V_{DDA(1V8)}$ = $V_{DD(PLL)}$ = V_{DDD} = $V_{DD(IO)}$ = $V_{DD(sintf)}$ = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
NCO frequency range; f_s = 640 Msps							
f_{NCO}	NCO frequency	reg value = 00000000h	D	-	0	-	MHz
		reg value = FFFFFFFFh	D	-	640	-	MHz
f_{step}	step frequency		D	-	0.149	-	Hz
Low power NCO frequency range; f_s = 640 Msps							
f_{NCO}	NCO frequency	reg value = 00000000h	D	-	0	-	MHz
		reg value = F8000000h	D	-	620	-	MHz
f_{step}	step frequency		D	-	20	-	MHz
Dynamic performances							
SFDR	spurious-free dynamic range	f_{data} = 320 Msps; f_s = 640 Msps; BW = f_{data} / 2					
		f_o = 4 MHz at 0 dBFS	I	-	−75	-	dBc
		f_o = 19 MHz at 0 dBFS	I	-	−70	-	dBc
		f_o = 70 MHz at 0 dBFS	I	-	−63	-	dBc
		f_{data} =160 Msps; f_s = 640 Msps; BW = f_{data} / 2					
		f_o = 4 MHz at 0 dBFS	I	-	−75	-	dBc
		f_o = 19 MHz at 0 dBFS	I	-	−70	-	dBc
		f_o = 70 MHz at 0 dBFS	I	-	−76	-	dBc
$SFDR_{RBW}$	restricted bandwidth spurious-free dynamic range	f_s = 640 Msps, f_o = 96 MHz at 0 dBFS, BW = 40 Mhz	I [5]	-	tbd	-	dBc
		f_s = 640 Msps, f_o = 150 MHz at 0 dBFS, BW =100 Mhz	I [5]	-	tbd	-	dBc
IMD3	third-order intermodulation distortion	f_{o1} = 47 MHz; f_{o2} = 49 MHz; f_s = 320 Msps; 2× interpolation	C [6]	-	-78		dBc
		f_{o1} = 95 MHz; f_{o2} = 97 MHz; f_s = 640 Msps; 4× interpolation	C [6]	-	-77	-	dBc
		f_{o1} = 159 MHz; f_{o2} = 161 MHz; f_s = 640 Msps; 2× interpolation	C [6]	-	-74	-	dBc
ACPR	adjacent channel power ratio	NCO on; 4× interpolation; f_s = 614.4 Msps; f_o = 115.2 MHz					
		1 carriers; BW = 5 MHz	I	-	70	-	dB
		2 carriers; BW = 10 MHz	C	-	70	-	dB
		4 carriers; BW = 20 MHz	C	-	67	-	dB
		NCO on; 2× interpolation; f_s = 614.4 Msps; f_o = 153.6 MHz					
		1 carriers; BW = 5 MHz	C	-	tbd	-	dB
		2 carriers; BW = 10 MHz	C	-	tbd	-	dB
		4 carriers; BW = 20 MHz	C	-	tbd	-	dB

Table 5. Characteristics *…continued*

$V_{DDA(1V8)}$ = $V_{DD(PLL)}$ = V_{DDD} = $V_{DD(IO)}$ = $VDD_{(sintf)}$ = 1.65 V to 1.95 V; $V_{DDA(3V3)}$ = 3.0 V to 3.6 V; AGND, GND(PLL), DGND and GNDIO are shorted together; T_{amb} = −40 °C to +85 °C; typical values measured at $V_{DDA(1V8)}$ = $V_{DD(PLL)}$ = V_{DDD} = $V_{DD(IO)}$ = $V_{DD(sintf)}$ = 1.8 V; $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate; unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
NSD	noise spectral density	f_s = 640 Msps; 8× interpolation; f_o = 19 MHz at 0 dBFS					
		noise shaper disable	C	-	−154	-	dBm/Hz
		noise shaper enable	C	-	−157	-	dBm/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

[2] CLKP / CLKN and CLKINP / CLKINN inputs are at differential LVDS levels. An external termination resistor with a value of between 80 Ω and 120 Ω (see Figure 11) should be connected across the pins.

[3] SYNC_OUTP / SYNC_OUTN outputs are differential LVDS outputs. They must be terminated by a resistor with a value of between 80 Ω and 120 Ω.

[4] $|V_{gpd}|$ represents the ground potential difference voltage. This is the voltage that results from current flowing through the finite resistance and the inductance between the receiver and the driver circuit ground voltage.

[5] In the band [2.71 MHz ≤ f_{offset} < 3.51 MHz], the restricted bandwidth spurious-free dynamic range in a 30 kHz bandwidth is defined as:

$$SFDR_{RBW} = -56\ \text{dBc} - 15\left[\frac{f\_offset}{MHz} - 2.715\right]$$

[6] IMD3 rejection with −6 dBFs/tone.

[7] Vin_p and Vin_n inputs are differential CML inputs. There are terminated internally to Vtt via 50 Ω (see Figure 4).

10. Application information

10.1 General description

The DAC1408D650 is a dual 14-bit DAC operating up to 650 Msps. Each DAC consists of a segmented architecture, comprising a 6-bit thermometer sub-DAC and an 8-bit binary weighted sub-DAC. With a maximum input data rate of up to 325 Msps and a maximum output sampling rate of 650 Msps, the DAC1408D650 allows more flexibility for wide bandwidth and multi-carrier systems. Combined with its quadrature modulator and its 32-bit NCO, the DAC1408D650 simplifies the frequency selection of the system. This is also possible because of the 2× or 4× interpolation filters that remove undesired images.

DAC1408D650 supports the following JESD204A key features:

- 8b/10b decoding,
- Code group synchronization,
- Inter-lane alignment,
- $1+x^{14}+x^{15}$ scrambling polynomial,
- Character replacement,
- TX/RX synchronization management via SYNC signals.

DAC1408D650 can be interfaced with any logic devices that features high speed SERDES functionality. Such macro is now widely available in FPGA from different vendors. Standalone SERDES ICs can also be used.

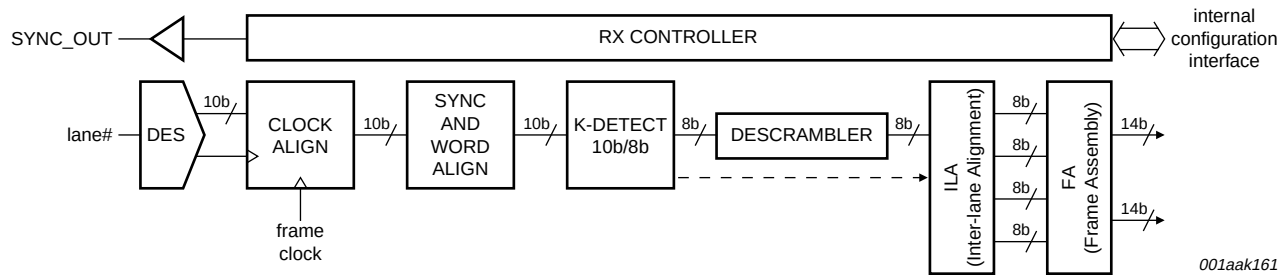
To enhance the intrinsic board layout simplification of the JESD204A standard, NXP includes polarity swapping for each of the lanes and additionally offers lane swapping. Each physical lane can be configured as being logically lane0 or lane1 or lane2 or lane3.

Each DAC generates two complementary current outputs on pins IOUTAP/IOUTAN and IOUTBP/IOUTBN. This provides a full-scale output current of up to 20 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.

The DAC1408D650 must be configured before operating. Therefore, it features an SPI slave interface to access internal registers. Some of these registers also provide information about the JESD204A interface status.

The DAC1408D650 operates at both 3.3 V and 1.8 V each of which has separate digital and analog power supplies. The digital input is 3.3 V compliant and the clock input is LVDS compliant.

10.2 JESD204A receiver



The descrambler can be enabled/disabled

Fig 3. JESD204A receiver

The JEDEC204A defines the following parameters:

L is the number of lanes per link,

M is the number of converters per device,

F is the number of bytes per frame clock period,

The DAC1408D650 supports both LMF = 421 and LMF = 211. The current setting is configurable via the SPI registers interface.

The complete Digital Layer Processing adds a variable delay on each lane path. This is mainly due to the inter-lane alignment.

Table 6. Digital Layer Processing Latency

Symbol	Parameter	Conditions	Test[2]	Min	Typ	Max	Unit
t_d	delay time	Digital Layer Processing delay	D	13	-	28	Cycle[1]

[1] Frame clock cycle

[2] D = guaranteed by design.

10.2.1 Lane input

Each lane is CML compliant. It is terminated to a common voltage with an integrated 50 Ω resistor.

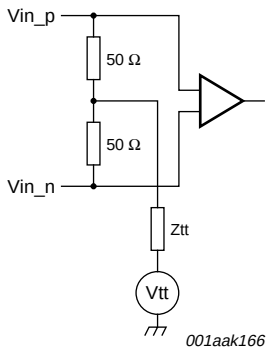


Fig 4. Lane input termination

The common mode voltage is programmable. See Table 39 “Page 2 register allocation map” for register value.

DC coupling is only possible if both DAC and transmitter have the same common mode voltage. Else, AC coupling is required.

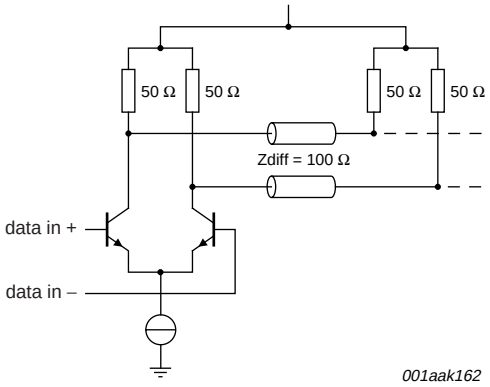


Fig 5. DC coupling

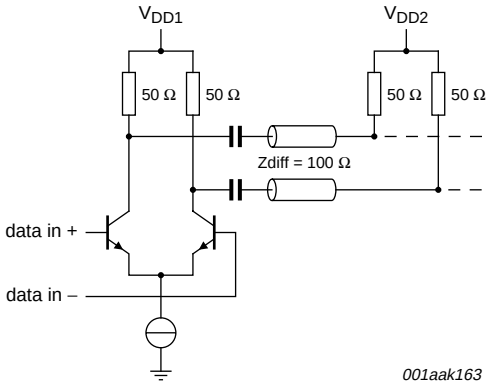


Fig 6. AC coupling

The deserializer performs the incoming data clock recovery and also the serial to parallel conversion. Therefore, each lane includes its own PLL that must first lock.

Then the clock alignment module transfers the data from the re-generated clock to the frame clock domain. The frequency of both clocks are the same but the phase relation between the clocks isn’t known.

10.2.2 Sync & word align

As stated in JESD204A, transmitter and receiver have to first synchronize. This is achieved through SYNC_OUT signals and SYNC pattern (K28.5 symbol).
The receiver (i.e. DAC1408D650) first drives its SYNC outputs. The SYNC signal/pattern is continuously sent until the receiver deasserts the SYNC signal.

The Lane Processing makes use of the SYNC-patterns to synchronize the datastream, determine the initial running disparity and to extract the 10 bits word from the incoming datastream (word-alignment).

The SYNC signal is also used during normal operation by the DAC1408D650 to request a link re-initialization. This occurs when the 8b/10b module loses synchronization.

The SYNC_OUT signal conforms to LVDS signaling. Its common mode voltage (see Table 39 “Page 2 register allocation map”) and its differential peak to peak amplitude (see Table 39 “Page 2 register allocation map”) can be programmed via registers.

SYNC_OUT is synchronous with the frame clock.

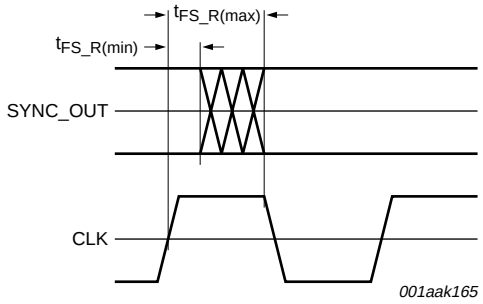


Fig 7. SYNC_OUT timing

Table 7. SYNC_OUT timing

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
t_d	delay time	frame clock to sync	C	tbd	-	tbd	ns

[1] C = guaranteed by characterization.

10.2.3 K detect & word align

This stage monitors the datastream for code-characters (komma-detect), decodes the words to bytes (octets) and performs optional character-replacement as part of frame/lane alignment monitoring and correction. This module will provide the required control signals to the RX-controller and ILA.

This module decodes the 10 bit words into 8 bit words (octets). The decode table is specified in the IEEE Std.802.3-2005 specification (page 41 Table 36 -1a). During decoding, the disparity is calculated according to the disparity rules mentioned in the same specification IEEE Std.802.3-2005 (page 39 chapter 36.2.4.4). When the disparity counter is more than 2 or less than –2, an error will be generated.

The following comma symbols are detected during data transmission irrespective of the running disparity:

/K/=K28.5

/F/=K28.7

/A/=K28.3

/R/=K28.0

/Q/=K28.4

A flag is sent to the control interface to reflect detected commas in registers.

The following flags are also triggered according to the following definitions:

- VALID: a code group that is found in the column of the 8b/10b decoding tables according to the current running disparity.
- DISPARITY ERROR: The received code group exists in the 8b/10b decoding table, but is not found in the proper column according to the current running disparity.
- NOT-IN-TABLE ERROR: The received code group is not found in the 8b/10b decoding table for either disparity.
- INVALID: a code group that either shows a disparity error or that does not exist in the 8b/10b decoding table.

DAC1408D650 supports character replacement whatever the state of the descrambler. When scrambling isn't active, the received K28.3 /A/ or K28.7 /F/ will be replaced by the previous sample. When scrambling is active, the corresponding data octet D28.3 (0xC) or D28.7 (0xFC) will be used.

10.2.4 Descrambler

The used descrambler is the 16-bit parallel self-synchronous descrambler based on the polynomial $1+x^{14}+x^{15}$. This processing can be turned off.

10.2.5 Inter lane alignment

This feature removes strict PCB design skew compensation between the lanes.

This module handles the alignment of the 4 data streams. Due to interlane-skew and each PLL per lane concept, these alignment characters may be received at different times by the receivers. After the sync period, the lock signal will be high. This enables the receiving of K28.3 /A/ characters.

The /A/-characters provided in the initial alignment sequence are then used to align the 4 data streams. With the bit-field sel_ila (2 bits) (refer to Table 65 "Page 4 register allocation map"), one can select the used K28.3 /A/ symbol ("00" => use the 1st /A/ symbol, "01" => use the 2nd /A/ symbol, "10" => use the 3rd /A/ symbol, "11" => use the 4th /A/ symbol) during the initial lane alignment. When all receivers have received their first selected /A/, they start propagating the received data to the frame assembly module at the same point in time.

This module can compensate up to +7/–7 frame clock period mis-alignment between the lanes.

When initial lane alignment isn't supported the manual alignment mode can be used.

After the initial ila sequence, the lane alignment monitoring starts. When a K28.3 /A/ symbol is received among the user data:

- its position is compared to the value of the alignment monitor counter,

- if 2 successive K28.3 /A/ symbols have been received at a wrong position, a realignment takes place,

- if the buffers are empty or overflow, this will be indicated by the registers: buff_err_ln0 .. buff_err_ln3

10.2.6 Frame assembly

DAC1408D650 supports only /F/ = 1, which means that every frame clock period carries one byte per lane.
Frame assembly combines the octet of lane_0 with the 6 msb bits of lane_1 and re-assemble the original 14 bits sample. The same is done for lane_2 and lane_3. Tail bits are dropped.

The frame assembler also handles error previously triggered.
If scrambling is enabled:

If a nit_err (not in table error) or kout_unexp (unexpected control character) occurs in lane_0 and/or lane_1, the previous sample (14 bits) will be repeated 2 times for I (lane_0, lane_1). The same is done for : Q (lane_2, lane_3).

If scrambling is disabled:

if a nit_err (not in table error) or kout_unexp (unexpected control character) occurs in lane_0 and/or lane_1, the previous sample (14 bits) will be repeated once for I (lane_0, lane_1). The same is done for : Q (lane_2, lane_3).

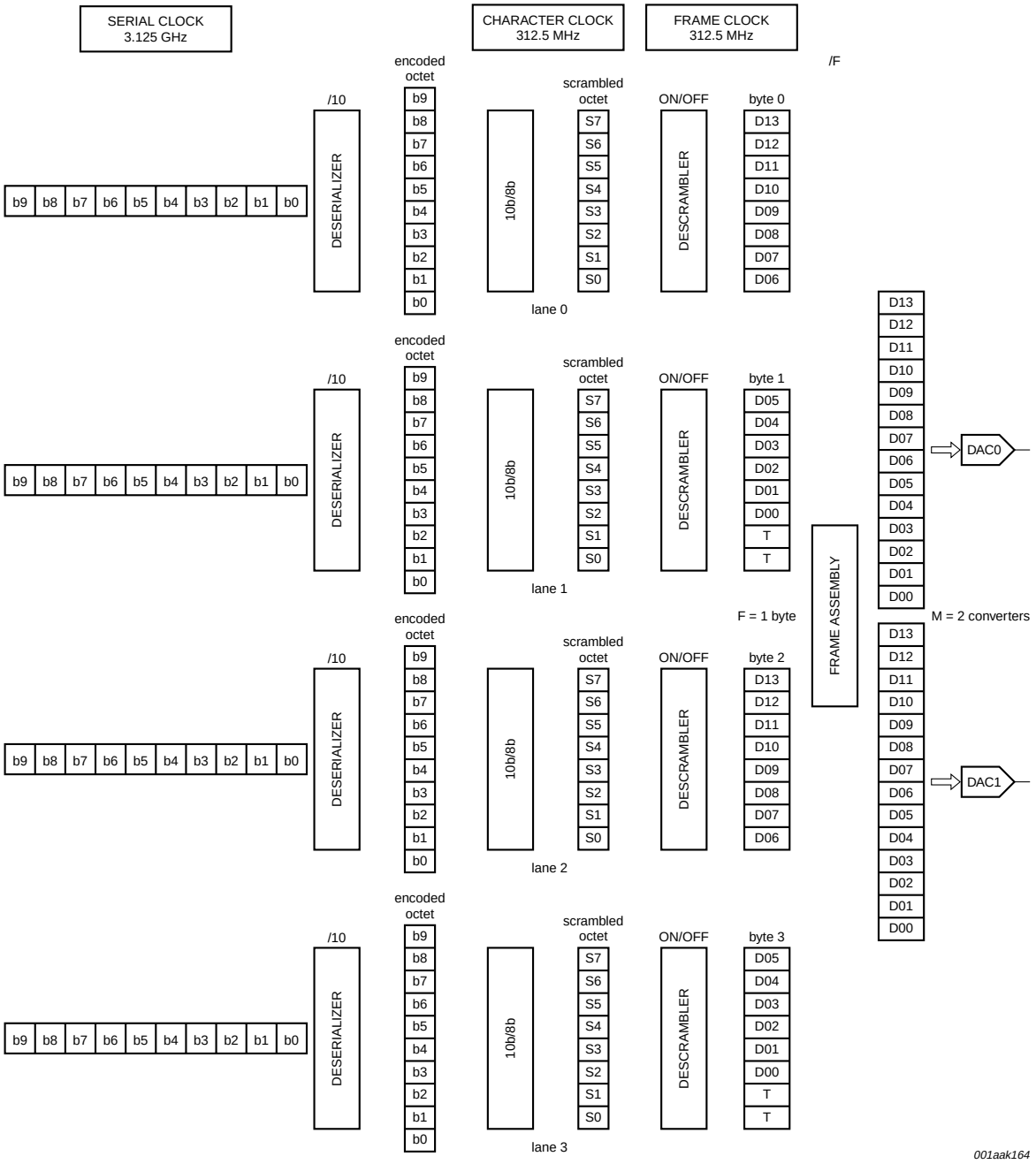


Fig 8. Frame assembly

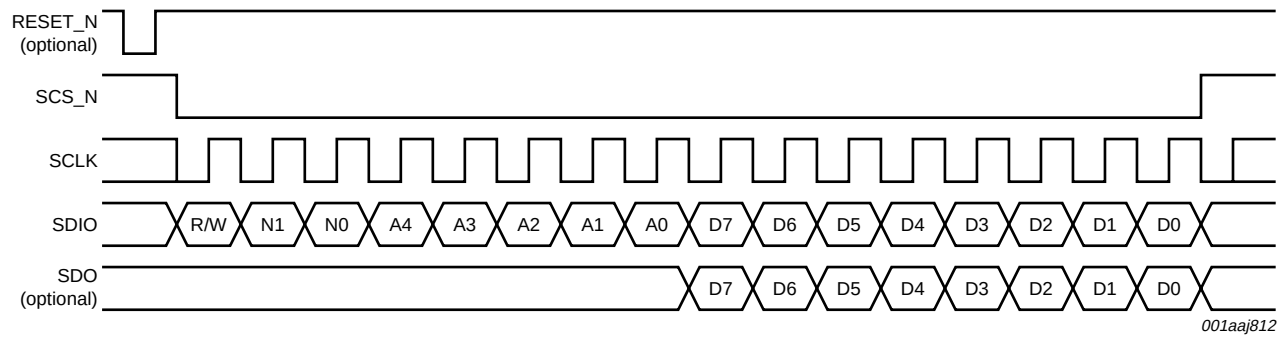
10.3 Serial interface (SPI)

10.3.1 Protocol description

The DAC1408D650 serial interface is a synchronous serial communication port allowing easy interfacing with many industry microprocessors. It provides access to the registers that define the operating modes of the chip in both write and read modes.

This interface can be configured as a 3-wire type (SDIO as bidirectional pin) or a 4-wire type (SDIO and SDO as unidirectional pin, input and output port respectively). In both configurations, SCLK acts as the serial clock, and SCS_N acts as the serial chip select bar.

Each read/write operation is sequenced by the SCS_N signal and enabled by a LOW assertion to drive the chip with 2 bytes to 5 bytes, depending on the content of the instruction byte (see Table 9).



R/W indicates the mode access, (see Table 8):

Fig 9. SPI protocol

Table 8. Read or Write mode access description

R/W	Description
0	Write mode operation
1	Read mode operation

In Table 9 below, N1 and N0 indicate the number of bytes transferred after the instruction byte.

Table 9. Number of bytes to be transferred

N1	N0	Number of bytes transferred
0	0	1
0	1	2
1	0	3
1	1	4

A[4:0]: indicates which register is being addressed. In the case of a multiple transfer, this address concerns the first register after which the next registers follow directly in a decreasing order according to Table 18 “Page 0 register allocation map”.

10.3.2 SPI timing description

The SPI interface can operate at a frequency of up to 15 MHz. The SPI timing is shown in Figure 10.

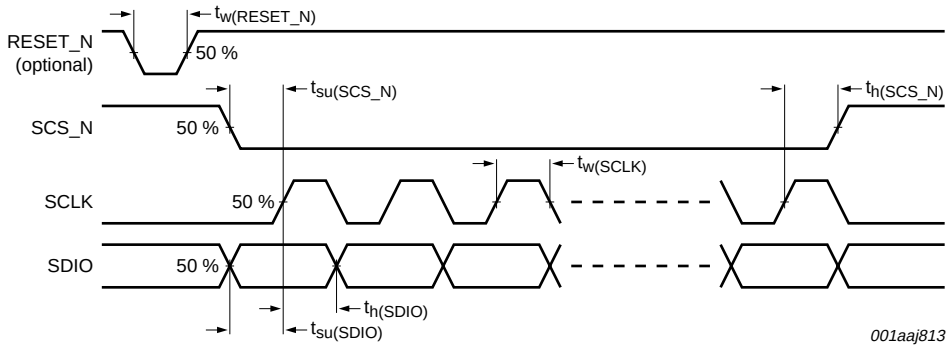


Fig 10. SPI timing diagram

The SPI timing characteristics are given in Table 10.

Table 10. SPI timing characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency	-	-	15	MHz
$t_{w(SCLK)}$	SCLK pulse width	30	-	-	ns
$t_{su(SCS\_N)}$	SCS_N set-up time	20	-	-	ns
$t_{h(SCS\_N)}$	SCS_N hold time	20	-	-	ns
$t_{su(SDIO)}$	SDIO set-up time	10	-	-	ns
$t_{h(SDIO)}$	SDIO hold time	5	-	-	ns
$t_{w(RESET\_N)}$	RESET_N pulse width	30	-	-	ns

10.4 Clock inputs

DAC1408D650 has two differential clock inputs, namely CLKINN/CLKINP and CLKN/CLKP. They must be driven with signals of exactly the same frequency. As the part has internal clock domain transition circuitry, there is no phase requirement between the two clocks.

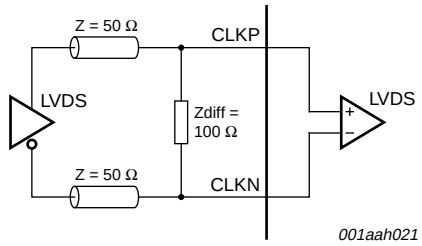


Fig 11. LVDS clock configuration

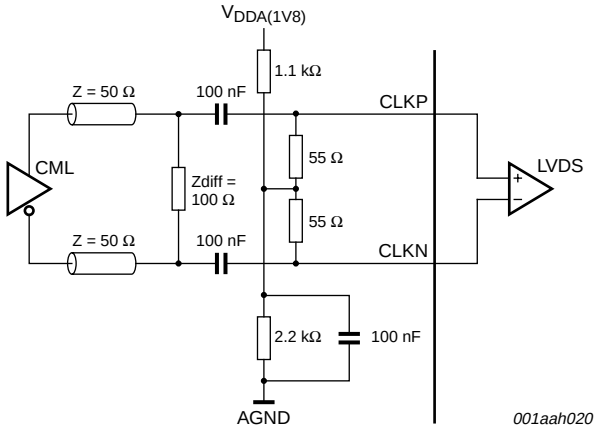


Fig 12. Interfacing CML to LVDS

The DAC1408D650 can operate with a clock frequency up to 325 MHz. Both clock inputs can be LVDS (see Figure 11) but they can also be interfaced with CML (see Figure 12).

During the reset phase (RESET_N asserted), both clocks must be stable and running. This ensures proper reset of the complete device.

10.5 FIR Filters

The two interpolation FIR filters have a stop band attenuation of at least 80 dBc and a pass band ripple of less than 0,0005 dB.

Table 11. Interpolation filter coefficients

First interpolation filter			Second interpolation filter		
Lower	**Upper**	**Value**	**Lower**	**Upper**	**Value**
H(1)	H(55)	–4	H(1)	H(23)	–2
H(2)	H(54)	0	H(2)	H(22)	0
H(3)	H(53)	13	H(3)	H(21)	17
H(4)	H(52)	0	H(4)	H(20)	0
H(5)	H(51)	–34	H(5)	H(19)	–75
H(6)	H(50)	0	H(6)	H(18)	0
H(7)	H(49)	72	H(7)	H(17)	238
H(8)	H(48)	0	H(8)	H(16)	0
H(9)	H(47)	–138	H(9)	H(15)	–660
H(10)	H(46)	0	H(10)	H(14)	0
H(11)	H(45)	245	H(11)	H(13)	2530
H(12)	H(44)	0	H(12)	-	4096
H(13)	H(43)	–408	-	-	-
H(14)	H(42)	0	-	-	-
H(15)	H(41)	650	-	-	-
H(16)	H(40)	0	-	-	-
H(17)	H(39)	–1003	-	-	-
H(18)	H(38)	0	-	-	-
H(19)	H(37)	1521	-	-	-
H(20)	H(36)	0	-	-	-
H(21)	H(35)	–2315	-	-	-
H(22)	H(34)	0	-	-	-
H(23)	H(33)	3671	-	-	-
H(24)	H(32)	0	-	-	-
H(25)	H(31)	–6642	-	-	-
H(26)	H(30)	0	-	-	-
H(27)	H(29)	20756	-	-	-
H(28)		32768	-	-	-

10.6 Quadrature modulator and Numerically Controlled Oscillator (NCO)

The quadrature modulator allows the 14-bit I and Q data to be mixed with the carrier signal generated by the NCO.

The frequency of the NCO is programmed over 32-bit and allows the sign of the sine component to be inverted in order to operate positive or negative, lower or upper single sideband up-conversion.

10.6.1 NCO in 32-bit

When using the NCO, the frequency can be set by the four registers FREQNCO_LSB, FREQNCO_LISB, FREQNCO_UISB and FREQNCO_MSB over 32 bits.

The frequency for the NCO in 32-bit is calculated as follows:

$$f_{NCO} = \frac{M \times f_s}{2^{32}} \quad (1)$$

where M is the decimal representation of FREQ_NCO[31:0].

The phase of the NCO can be set from 0° to 360° by both registers PHINCO_LSB and PHINCO_MSB over 16 bits.

The default setting is f_{NCO} = 96 MHz when f_s = 640 Msps and the default phase is 0°.

10.6.2 Low-power NCO

When using the low-power NCO, the frequency can be set by the 5 MSB of register FREQNCO_MSB.

The frequency for the low-power NCO is calculated as follows:

$$f_{NCO} = \frac{M \times f_s}{2^5} \quad (2)$$

where M is the decimal representation of FREQ_NCO[31:27].

The phase of the low-power NCO can be set by the 5 MSB of the register PHINCO_MSB.

10.6.3 Minus 3dB

During normal use, a full-scale pattern will also be full scale at the output of the DAC. Nevertheless, when the I and Q data are simultaneously close to full scale, some clipping can occur and the Minus_3dB function can be used to reduce the gain by 3 dB in the modulator. This is to keep a full-scale range at the output of the DAC without added interferers.

10.7 x / (sin x)

Due to the roll-off effect of the DAC, a selectable FIR filter is inserted to compensate for the (sin x) / x effect. This filter introduces a DC loss of 3.4 dB. The coefficients are represented in Table 12 “Inversion filter coefficients”.

Table 12. Inversion filter coefficients

First interpolation filter		
Lower	**Upper**	**Value**
H(1)	H(9)	2
H(2)	H(8)	–4
H(3)	H(7)	10
H(4)	H(6)	–35
H(5)	-	401

10.8 DAC transfer function

The full-scale output current for each DAC is the sum of the two complementary current outputs:

$$I_{O(fs)} = I_{IOUTP} + I_{IOUTN} \quad (3)$$

The output current depends on the digital input data:

$$I_{IOUTP} = I_{O(fs)} \times \left(\frac{DATA}{16383}\right) \quad (4)$$

$$I_{IOUTN} = I_{O(fs)} \times \left(\frac{16383 - DATA}{16383}\right) \quad (5)$$

The setting applied to CODING (register 00h[2]; see Table 18 “Page 0 register allocation map”) defines whether the DAC1408D650 operates with a binary input or a two’s complement input.

Table 13 “DAC transfer function” shows the output current as a function of the input data, when $I_{O(fs)}$ = 20 mA.

Table 13. DAC transfer function

Data	I13/Q13 to I0/Q0		IOUTP	IOUTN
	Binary	Two’s complement		
0	00 0000 0000 0000	10 0000 0000 0000	0 mA	20 mA
...	...	...	...	...
8192	10 0000 0000 0000	00 0000 0000 0000	10 mA	10 mA
...	...	...	...	...
16383	11 1111 1111 1111	01 1111 1111 1111	20 mA	0 mA

10.9 Full-scale current

10.9.1 Regulation

Figure 13 shows the internal configuration. The DAC1408D650 reference circuitry integrates an internal bandgap reference voltage which delivers a 1.25 V reference to the GAPOUT pin. It is recommended to decouple pin GAPOUT using a 100 nF capacitor.

The reference current is generated via an external resistor of 910 Ω (1 %) connected to pin VIRES. A control amplifier sets the appropriate full-scale current ($I_{O(fs)}$) for both DACs (see Figure 13 “Internal reference configuration”).

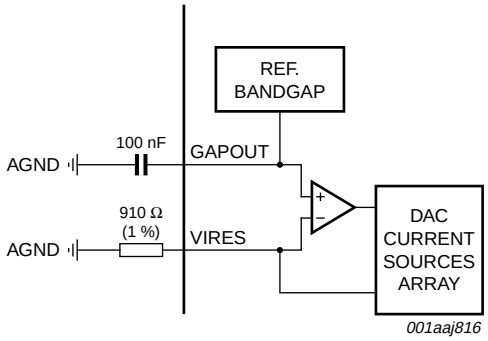


Fig 13. Internal reference configuration

This configuration is optimum for temperature drift compensation because the bandgap reference voltage can be matched to the voltage across the feedback resistor.

10.9.1.1 External regulation

The DAC current can also be set by applying an external reference voltage to the non-inverting input pin GAPOUT and disabling the internal bandgap reference voltage with GAP_PD (register 00h[0]; see Table 19 “COMMON register (address 00h) bit description”).

10.9.2 Full-scale current adjustment

The default full-scale current ($I_{O(fs)}$) is 20 mA but further adjustments can be made by the user to both DACs independently via the serial interface from 1.6 mA to 22 mA, +/- 10 %.

The settings applied to DAC_A_GAIN_COARSE[3:0] (register 0Ah; see Table 29 “DAC_A_CFG_2 register (address 0Ah) bit description” and register 0Bh; see Table 30 “DAC_A_CFG_3 register (address 0Bh) bit description”) and to DAC_B_GAIN COARSE[3:0] (register 0Dh; see Table 32 “DAC_B_CFG_2 register (address 0Dh) bit description” and register 0Eh; see Table 33 “DAC_B_CFG_3 register (address 0Eh) bit description”) define the coarse variation of the full-scale current (see Table 14 “$I_{O(fs)}$ coarse adjustment”).

Table 14. $I_{O(fs)}$ coarse adjustment

Default settings are shown highlighted.

DAC_GAIN_COARSE[3:0]		$I_{O(fs)}$ (mA)
Decimal	**Binary**	
0	0000	1.6
1	0001	3.0
2	0010	4.4
3	0011	5.8
4	0100	7.2
5	0101	8.6
6	0110	10.0
7	0111	11.4
8	1000	12.8
9	1001	14.2
10	1010	15.6
11	1011	17.0
12	1100	18.5
13	**1101**	**20.0**
14	1110	21.0
15	1111	22.0

The settings applied to DAC_A_GAIN_FINE[5:0] (register 0Ah; see Table 29 "DAC_A_CFG_2 register (address 0Ah) bit description") and to DAC_B_GAIN_FINE[5:0] (register 0Dh; see Table 32 "DAC_B_CFG_2 register (address 0Dh) bit description") define the fine variation of the full-scale current (see Table 15 "$I_{O(fs)}$ fine adjustment").

Table 15. $I_{O(fs)}$ fine adjustment

Default settings are shown highlighted.

DAC_GAIN_FINE[5:0]		Delta $I_{O(fs)}$
Decimal	**Two's complement**	
–32	10 0000	–10 %
...	...	...
0	**00 0000**	**0**
...	...	...
31	01 1111	+10 %

The coding of the fine gain adjustment is two's complement.

10.10 Digital offset adjustment

When the DAC1408D650 analog output is DC connected to the next stage, the digital offset correction can be used to adjust the common mode level at the output of the DAC. It adds an offset at the end of the digital part, just before the DAC.

The settings applied to DAC_A_OFFSET[11:0] (register 09h; see Table 28 "DAC_A_CFG_1 register (address 09h) bit description" and register 0Bh; see Table 30 "DAC_A_CFG_3 register (address 0Bh) bit description") and to "DAC_B_OFFSET[11:0]"

(register 0Ch; see Table 31 “DAC_B_CFG_1 register (address 0Ch) bit description” and register 0Eh; see Table 33 “DAC_B_CFG_3 register (address 0Eh) bit description”) define the range of variation of the digital offset (see Table 16 “Digital offset adjustment”).

Table 16. Digital offset adjustment

Default settings are shown highlighted.

DAC_OFFSET[11:0]		Offset applied
Decimal	**Two’s complement**	
–2048	1000 0000 0000	–4096
–2047	1000 0000 0001	–4094
...	...	...
–1	1111 1111 1111	–2
0	**0000 0000 0000**	**0**
+1	0000 0000 0001	+2
...	...	...
2046	0111 1111 1110	+4092
2047	0111 1111 1111	+4094

10.11 Analog output

The DAC1408D650 has two output channels each of which produces two complementary current outputs. These allow the even-order harmonics and noise to be reduced. The pins are IOUTAP/IOUTAN and IOUTBP/IOUTBN respectively and need to be connected via a load resistor R_L to the 3.3 V analog power supply ($V_{DDA(3V3)}$).

For the equivalent analog output circuit of one DAC, refer to Figure 14 “Equivalent analog output circuit (one DAC)”. This circuit consists of a parallel combination of NMOS current sources, and their associated switches, for each segment.

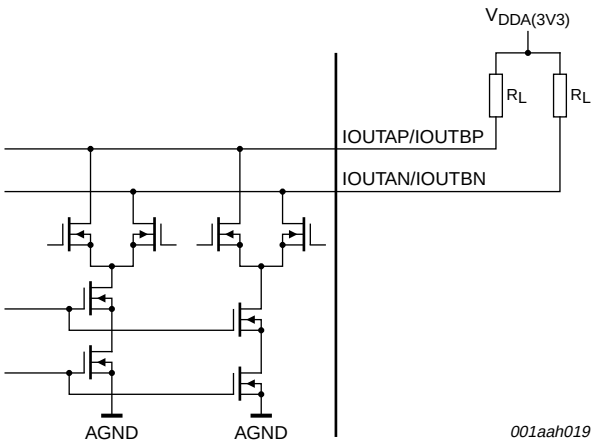


Fig 14. Equivalent analog output circuit (one DAC)

The cascode source configuration increases the output impedance of the source, thus improving the dynamic performance of the DAC by introducing less distortion.

The device can provide an output level of up to 2 $V_{o(p-p)}$ depending on the application, the following stages and the targeted performances.

10.12 Auxiliary DACs

The DAC1408D650 integrates 2 auxiliary DACs that can be used to compensate for any offset between the DAC and the next stage in the transmission path.

Both auxiliary DACs have a resolution of 10-bit and are current sources (referenced to ground).

$$I_{O(AUX)} = I_{AUXP} + I_{AUXN} \tag{6}$$

The output current depends on the auxiliary DAC data:

$$AUXP = I_{O(AUX)} \times \left(\frac{AUX[9:0]}{1023}\right) \tag{7}$$

$$AUXN = I_{O(AUX)} \times \left(\frac{(1023 - AUX[9:0])}{1023}\right) \tag{8}$$

Table 17 “Auxiliary DAC transfer function” shows the output current as a function of the auxiliary DAC data.

Table 17. Auxiliary DAC transfer function

Default settings are shown highlighted.

Data	AUX[9:0] (binary)	I_{AUXP}	I_{AUXN}
0	00 0000 0000	0 mA	2.2 mA
...	...	...	...
512	**10 0000 0000**	**1.1 mA**	**1.1 mA**
...	...	...	...
1023	11 1111 1111	2.2 mA	0 mA

10.13 Output configuration

10.13.1 Basic output configuration

The use of a differentially-coupled transformer output provides optimum distortion performance (see Figure 15 “1 $V_{o(p-p)}$ differential output with transformer”). In addition, it helps to match the impedance and provides electrical isolation.

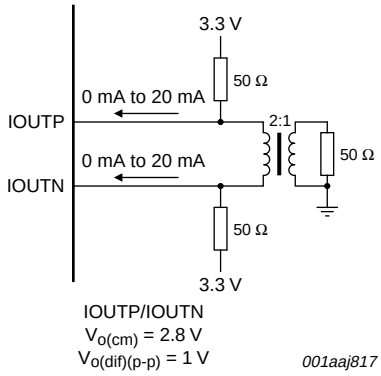


Fig 15. 1 $V_{o(p-p)}$ differential output with transformer

The DAC1408D650 can operate up to 2 $V_{o(p-p)}$ differential outputs. In this configuration, it is recommended to connect the center tap of the transformer to a 62 Ω resistor connected to the 3.3 V analog power supply, in order to adjust the DC common mode to approximately 2.7 V (see Figure 16 “2 $V_{o(p-p)}$ differential output with transformer”).

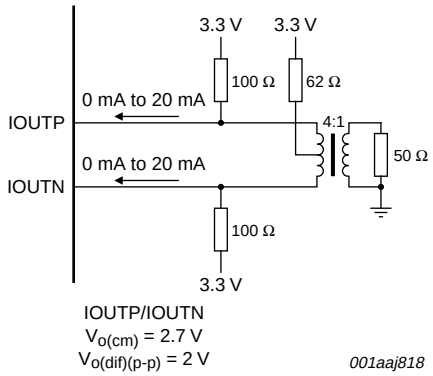


Fig 16. 2 $V_{o(p-p)}$ differential output with transformer

10.13.2 DC interface to an Analog Quadrature Modulator (AQM)

When the system operation requires to keep the DC component of the spectrum, the DAC1408D650 can use a DC interface to connect to an AQM. In this case, the offset compensation for LO cancellation can be made with the use of the digital offset control in the DAC.

Figure 17 provides an example of a connection to an AQM with a 1.7 $V_{i(cm)}$ common mode input level.

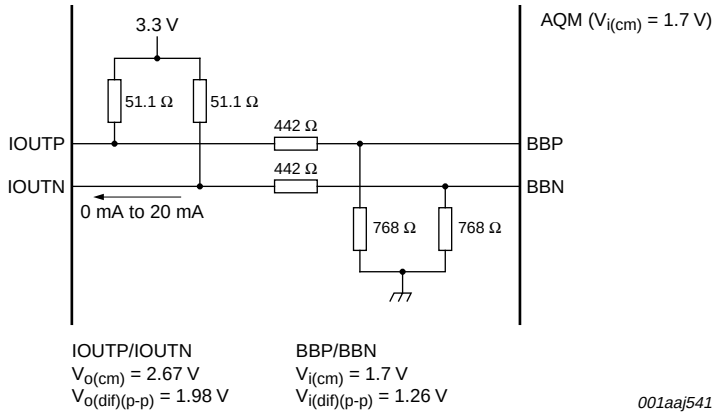


Fig 17. An example of a DC interface to a 1.7 $V_{i(cm)}$ AQM

Figure 18 provides an example of a connection to an AQM with a 3.3 $V_{i(cm)}$ common mode input level.

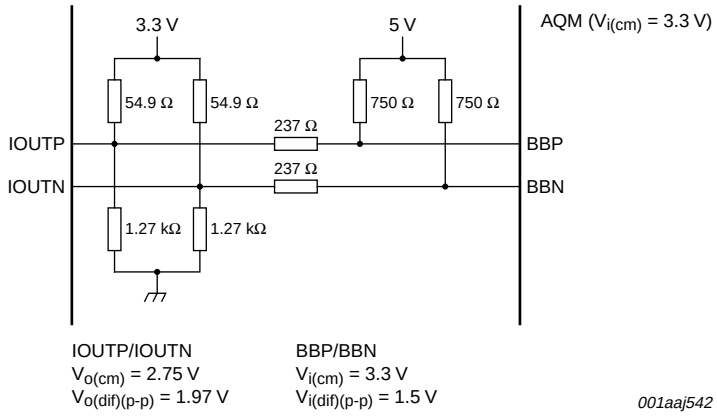


Fig 18. An example of a DC interface to a 3.3 $V_{i(cm)}$ AQM

The auxiliary DACs can be used to control the offset in a precise range or with precise steps.

Figure 19 provides an example of a DC interface with the auxiliary DACs to an AQM with a 1.7 $V_{i(cm)}$ common mode input level.

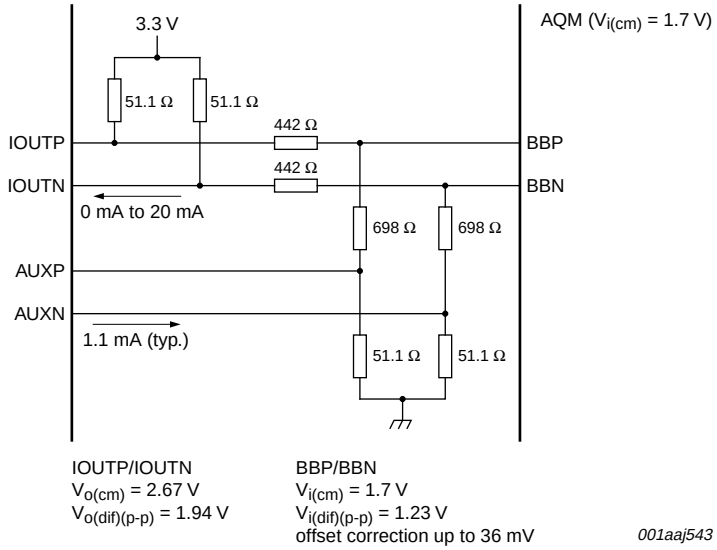


Fig 19. An example of a DC interface to a 1.7 $V_{i(cm)}$ AQM when using auxiliary DACs

Figure 20 provides an example of a DC interface with the auxiliary DACs to an AQM with a 3.3 $V_{i(cm)}$ common mode input level.

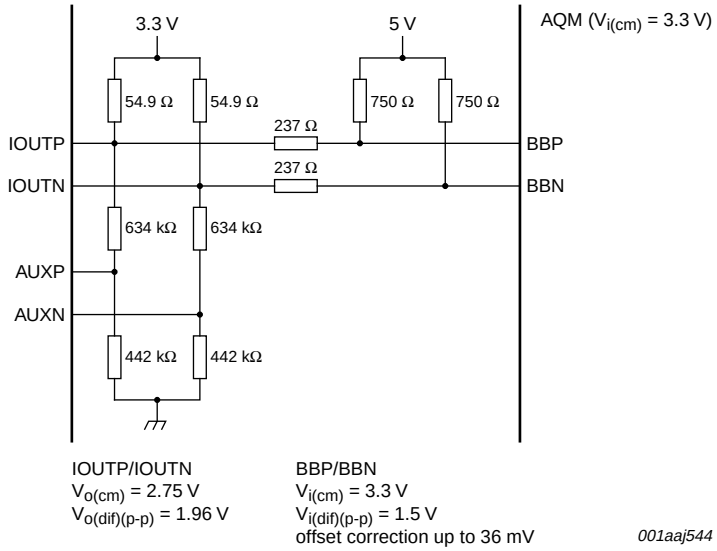


Fig 20. An example of a DC interface to a 3.3 $V_{i(cm)}$ AQM when using auxiliary DACs

The constraints to adjust the interface are the output compliance range of the DAC and the auxiliary DACs, the input common mode level of the AQM, and the range of offset correction.

10.13.3 AC interface to an Analog Quadrature Modulator (AQM)

When the AQM common mode voltage is close to ground, the DAC1408D650 must be AC-coupled and the auxiliary DACs are needed for offset correction.

Figure 20 provides an example of a connection to an AQM with a 0.5 $V_{i(cm)}$ common mode input level when using auxiliary DACs.

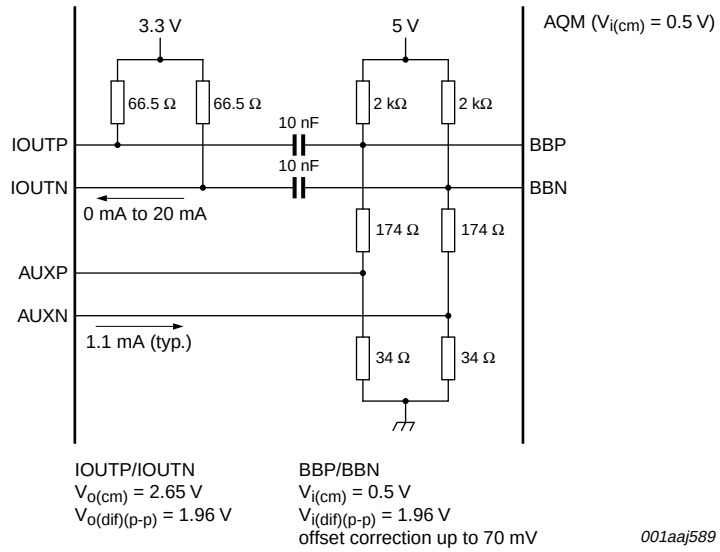


Fig 21. An example of an AC interface to a 0.5 $V_{i(cm)}$ AQM when using auxiliary DACs

10.14 Power and grounding

In order to obtain optimum performance, it is recommended that the 1.8 V analog power supplies on pins 5, 11, 71, 77 and 99 should not be connected with the ones on pins 6, 70, 79, 81, 83, 93, 95 and 97 on the top layer.

To optimize the decoupling, the power supplies should be decoupled with the following ground pins:

- $V_{DDD(1V8)}$: pin 18 with 19 and pin 55 with 54.
- $V_{DD(IO)(3V3)}$: pin 14 with 15 and pin 60 with 61.
- $V_{DDA(1V8)}$: pin 5 with 4; pin 6 with pin 7; pin 11 with 10; pin 71 with 72; pin 77 with 78; pins 79, 81, 83 with 80, 82, 84; pins 93, 95, 97 with 92, 94, 96 and pin 99 with 98.
- $V_{DDA(3V3)}$: pin 1 with 100 and pin 75 with 76.
- $V_{DDA(sintf)(1V8)}$: pin 26 with 29; pin 32 with pin 35 and pin 38; pin 41 with pin 38 and pin 44.

10.15 Configuration interface

10.15.1 Register description

DAC1408D650 implements indirect addressing using a page access method. The page-address is located at address 0x1F and is by default 0x00, which selects page_0 as default-page. For example, to access registers which configure the jesdrx, one must first activate page_4 by writing 0x04 to the page-address 0x1F.

The DAC1408D650 contains 6 different pages.

10.15.2 Detailed descriptions of registers

The register information has been provided in page form accompanied by a detailed description for each bit in the tables following the register allocation map of each page.

10.15.2.1 Page 0 allocation map description

Table 18. Page 0 register allocation map

Address		Register name	R/W	Bit definition								Default	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
0	00h	COMMON	R/W	SPI_3W	SPI_RST	-	-	INTERLEAVED_MODE	DF	PD_ALL	PD_GAP	10001100	8Ch
1	01h	TXCFG	R/W	NCO_EN	NCO_LOWPOWER_SEL	INV_SINE_EN	MODE[2:0]			INT_FIR[1:0]		00000001	01h
2	02h	PLLCFG	R/W	PD_PLL	-	PD_PLL_IO	PLL_DIV[1:0]		PLL_PHASE_SEL[1:0]		PLL_POL	00000000	00h
3	03h	FREQNCO_LSB	R/W	FREQ_NCO[7:0]								01100110	66h
4	04h	FREQNCO_LISB	R/W	FREQ_NCO[15:18]								01100110	66h
5	05h	FREQNCO_UISB	R/W	FREQ_NCO[23:16]								01100110	66h
6	06h	FREQNCO_MSB	R/W	FREQ_NCO[31:24]								00100110	26h
7	07h	PHINCO_LSB	R/W	PHI_NCO[7:0]								00000000	00h
8	08h	PHINCO_MSB	R/W	PHI_NCO[15:8]								00000000	00h
9	09h	DAC_A_CFG_1	R/W	DAC_A_PD	DAC_A_SLEEP	DAC_A_OFFSET[5:0]						00000000	00h
10	0Ah	DAC_A_CFG_2	R/W	DAC_A_GAIN_COARSE[7:6]		DAC_A_GAIN_FINE[5:0]						01000000	40h
11	0Bh	DAC_A_CFG_3	R/W	DAC_A_GAIN_COARSE[9:8]		DA_A_OFFSET[11:6]						11000000	C0h
12	0Ch	DAC_B_CFG_1	R/W	DAC_B_PD	DAC_B_SLEEP	DAC_B_OFFSET[5:0]						00000000	00h
13	0Dh	DAC_B_CFG_2	R/W	DAC_B_GAIN_COARSE[7:6]		DAC_B_GAIN_FINE[5:0]						11000000	40h
14	OEh	DAC_B_CFG_3	R/W	DAC_B_GAIN_COARSE[9:8]		DA_B_OFFSET[11:6]						11000000	C0h
15	OFh	DAC_CFG	R/W	-	-	-	-	-	-	MINUS3DB	NOISESHAPER	11000000	00h
26	1Ah	DAC_A_AUX_MSB	R/W	DAC_A_AUX[9:2]								10000000	80h
27	1Bh	DAC_A_AUX_LSB	R/W	DAC_A_AUX_PD	-	-	-	-	-	DAC_A_AUX[1:0]		00000000	00h
28	1Ch	DAC_B_AUX_MSB	R/W	DAC_B_AUX[9:2]								10000000	80h
29	1Dh	DAC_B_AUX_LSB	R/W	DAC_B_AUX_PD	-	-	-	-	-	DAC_B_AUX[1:0]		00000000	00h
31	1Fh	PAGE_ADDRESS	R/W	PAGE								00000000	00h

10.15.2.2 Page 0 bit definition detailed description

Please refer to Table 18 for a register overview for page 0. In the following tables, all the values emphasized in bold are the default values.

Table 19. COMMON register (address 00h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	SPI_3W	R/W		serial interface bus type
			0	4 wire SPI
			1	**3 wire SPI**
6	SPI_RST	R/W		serial interface reset
			0	**no reset**
			1	performs a reset on all registers except 0x00
3	INTERLEAVED_MODE	R/W		state
			0	disabled
			1	enabled
2	DF	R/W		data format
			0	unsigned format
			1	signed (two's compliment) format
1	PD_ALL	R/W		power-down
			0	no action
			1	all circuits (digital and analog) are switched off
0	GAP_PD	R/W		internal bandgap power-down
			0	no action
			1	internal bandgap references are switched off

Table 20. TXCFG register (address 01h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	NCO_EN	R/W		NCO
			0	disabled (the NCO phase is reset to 0)
			1	enabled
6	NCO_LP_SEL	R/W		low-power NCO
			0	NCO may use all 32 bits
			1	NCO frequency and phase given by the five MSBs of the registers 06h and 08h respectively
5	INV_SINE_EN	R/W		x / (sin x) function
			0	disabled
			1	enabled
4 to 2	MODE[2:0]	R/W		modulation
			000	dual DAC: no modulation
			001	**positive upper single sideband up-conversion**
			010	positive lower single sideband up-conversion
			011	negative upper single sideband up-conversion
			100	negative lower single sideband up-conversion
1 to 0	INT_FIR[1:0]	R/W		interpolation
			00	no interpolation
			01	**2×**
			10	4×
			-	8×

Table 21. PLLCFG register (address 02h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	PLL_PD	R/W		PLL
			0	**switched on**
			1	switched off
6	-	R/W		undefined
5	PLL_DIV_PD	R/W		PLL divider
			0	**switched on**
			1	switched off
4 to 3	PLL_DIV[1:0]	R/W		PLL divider factor
			00	**2**
			01	4
			-	8
2 to 1	PLL_PHASE[1:0]	R/W		PLL phase shift of f_s
			00	**0°**
			01	120°
			10	240°
0	PLL_POL	R/W		clock edge of DAC (f_s)
			0	normal
			1	inverted

Table 22. FREQNCO_LSB register (address 03h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	FREQ_NCO[7:0]	R/W	-	lower 8-bits for the NCO frequency setting

Table 23. FREQNCO_LISB register (address 04h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	FREQ_NCO[15:8]	R/W	-	lower intermediate 8-bits for the NCO frequency setting

Table 24. FREQNCO_UISB register (address 05h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	FREQ_NCO[23:16]	R/W	-	upper intermediate 8-bits for the NCO frequency setting

Table 25. FREQNCO_MSB register (address 06h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	FREQ_NCO[31:24]	R/W	-	most significant 8-bits for the NCO frequency setting

Table 26. PHINCO_LSB register (address 07h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	PH_NCO[7:0]	R/W	-	lower 8-bits for the NCO phase setting

Table 27. PHINCO_MSB register (address 08h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	PH_NCO[15:8]	R/W	-	most significant 8-bits for the NCO phase setting

Table 28. DAC_A_CFG_1 register (address 09h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	DAC_A_PD	R/W		DAC A power
			0	**on**
			1	off
6	DAC_A_SLEEP	R/W		DAC A Sleep mode
			0	**disabled**
			1	enabled
5 to 0	DAC_A_OFFSET[5:0]	R/W	-	lower 6-bits for the DAC A offset

Table 29. DAC_A_CFG_2 register (address 0Ah) bit description

Bit	Symbol	Access	Value	Description
7 to 6	DAC_A_GAIN_COARSE[7:6]	R/W	-	least significant 2-bits for the DAC A gain setting for coarse adjustment
5 to 0	DAC_A_GAIN_FINE[5:0]	R/W	-	lower 6-bits for the DAC A gain setting for fine adjustment

Table 30. DAC_A_CFG_3 register (address 0Bh) bit description

Bit	Symbol	Access	Value	Description
7 to 6	DAC_A_GAIN_COARSE[9:8]	R/W	-	most significant 2-bits for the DAC A gain setting for coarse adjustment
5 to 0	DAC_A_OFFSET[11:6]	R/W	-	most significant 6-bits for the DAC A offset

Table 31. DAC_B_CFG_1 register (address 0Ch) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	DAC_B_PD	R/W		DAC B power
			0	**on**
			1	off
6	DAC_B_SLEEP	R/W		DAC B Sleep mode
			0	**disabled**
			1	enabled
5 to 0	DAC_B_OFFSET[5:0]	R/W		lower 6-bits for the DAC B offset

Table 32. DAC_B_CFG_2 register (address 0Dh) bit description

Bit	Symbol	Access	Value	Description
7 to 6	DAC_B_GAIN_COARSE[7:6]	R/W	-	less significant 2-bits for the DAC B gain setting for coarse adjustment
5 to 0	DAC_B_GAIN_FINE[5:0]	R/W	-	the 6-bits for the DAC B gain setting for fine adjustment

Table 33. DAC_B_CFG_3 register (address 0Eh) bit description

Bit	Symbol	Access	Value	Description
7 to 6	DAC_B_GAIN_COARSE[9:8]	R/W	-	most significant 2-bits for the DAC B gain setting for coarse adjustment
5 to 0	DAC_B_OFFSET[11:6]	R/W	-	most significant 6-bits for the DAC B offset

Table 34. DAC_CFG register (address 0Fh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
1	MINUS_3DB	R/W		NCO gain
			0	**unity**
			1	–3 dB
0	NOISE_SHAPER	R/W		noise shaper
			0	**disabled**
			1	enabled

Table 35. DAC_A_Aux_MSB register (address 1Ah) bit description

Bit	Symbol	Access	Value	Description
7 to 0	AUX_A[9:2]	R/W	-	most significant 8-bits for the auxiliary DAC A

Table 36. DAC_A_Aux_LSB register (address 1Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	AUX_A_PD	R/W		auxiliary DAC A power
			0	**on**
			1	off
1 to 0	AUX_A[1:0]	R/W		lower 2-bits for the auxiliary DAC A

Table 37. DAC_B_Aux_MSB register (address 1Ch) bit description

Bit	Symbol	Access	Value	Description
7 to 0	AUX_B[9:2]	R/W	-	most significant 8-bits for the auxiliary DAC B

Table 38. DAC_B_Aux_LSB register (address 1Dh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	AUX_B_PD	R/W		auxiliary DAC B power
			0	**on**
			1	off
1 to 0	AUX_B[1:0]	R/W		lower 2-bits for the auxiliary DAC B

10.15.2.3 Page 2 allocation map description

Table 39. Page 2 register allocation map

Address		Register name	R/W	Bit definition								Default	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
0	00h	MAINCONTROL	R/W	-	-	FULL RE_INIT	FULL RE_INIT	MAN_PON_ CNTR	MAN_SUPD_ CNTR	FORCE_RES ET_DCLK	FORCE_RE SET_FCLK	00000011	03h
1	01h	MAN_PON	R/W	-	-	MAN_PON_ CLKBUFFE R	MAN_PON_ ALL	MAN_PON_L N3	MAN_PON_L N2	MAN_PON_L N1	MAN_PON_ LN0	00000000	00h
2	02h	MAN_SUPD	R/W	MAN_PLL _SEL_PD _LN3	MAN_PLL _SEL_PD _LN2	MAN_PLL_ SEL_PD_LN 1	MAN_PLL_S EL_PD_LN0	MAN_PLL_S TARTUP_LN 3	MAN_PLL_S TARTUP_LN 2	MAN_PLL_S TARTUP_LN 1	MAN_PLL_S TARTUP_LN 0	00000000	00h
4	04h	RST_EXT_FCLK	R/W	RST_EXT_FCLK_TIME[7:0]								00111111	3Fh
5	05h	RST_EXT_DCLK	R/W	RST_EXT_DCLK_TIME[7:0]								00100000	20h
6	06h	DCSMU_PREDIV CNT	R/W	DCSMU PREDIVIDER[7:0]								00011110	1Eh
7	07h	PLL_CHARGETI ME	R/W	PLL_CHARGE_TIME[7:0]								00110010	32h
8	08h	PLL_RUN_IN_TI ME	R/W	PLL_RUNIN_TIME[7:0]								00110010	32h
9	09h	CA_RUN_IN_TIM E	R/W	CA_RUNIN_TIME[7:0]								00000100	04h
10	0Ah	IQ_LEVEL_CNTR L	R/W	ILEV_CNTRL[1:0]		QLEV_CNTRL[1:0]		IQ_DC_LEVEL[11:9]				01011000	58h
11	0Bh	IQ_DC_LEVEL_L SB	R/W	IQ_DC_LEVEL[7:0]								00000000	00h
16	10h	SET_ICHP_PD1	R/W	-	-	-	-	SET_ICHP_PD1[3:0]				00000001	01h
17	11h	SET_ICHP_PD2	R/W	-	-	-	-	SET_ICHP_PD2[3:0]				00000001	01h
18	12h	SET_ICHP_PFD	R/W	-	-	-	-	SET_ICHP_PFD[3:0]				00000001	01h
19	13h	SET_RATIO_PD1	R/W	-	-	-	-	SET_RATIO_PD1[3:0]				00000010	02h
20	14h	SET_RATIO_PD2	R/W	-	-	-	-	SET_RATIO_PD2[3:0]				00001000	08h
21	15h	SET_RATIO_PFD	R/W	-	-	-	-	SET_RATIO_PFD[3:0]				00000110	06h
22	16h	SET_VCM_VOLT AGE	R/W	-	-	-	-	-	SET_VCM[2:0]			00000010	02h
23	17h	SET_SYNC	R/W	SET_SYNC_VCOM[3:0]				SET_SYNC_LEVEL[3:0]				01000011	43h
26	1Ah	MISC_CNTRLS	R/W	-	-	-	-	-	JD_MODE	CDI_MODE	SR_CDI	00000100	04h

Table 39. Page 2 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
29	1Dh	DIG_VERSION	R	DIG_VERSION_ID[7:0]								11010000	D0h
30	1Eh	JRX_ANA_VERSION	R	JRX_ANA_VERSION_ID[7:0]								00000001	01h
31	1Fh	PAGE_ADDRESS	R/W	PAGE								00000000	00h

10.15.2.4 Page 2 bit definition detailed description

Please refer to Table 39 for a register overview and their default values. In the following tables, all the values emphasized in bold are the default values.

Table 40. MAINCONTROL register (address 00h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
5	FULL_RE_INIT	R/W		initialization
			1	**full re-initialization**
			0	quick re-initialization
4	SYNC_INIT_LEVEL	R/W		sync
			0	sync starts with '0'
			1	sync starts with '1'
3	MAN_PON_CNTRL	R/W		pon
			1	manual control of pon's
			0	pon's jesdrx module controlled by dcsmu
2	MAN_SUPD_CNTRL	R/W		BangBang PLL
			0	run-in timing BangBang PLL controlled by dcsmu
			1	manual control of run-in timing BangBang PLL
1	FORCE_RESET_DCLK	R/W		reset_dcl
			0	release reset_dclk
			1	force reset_dclk
0	FORCE_RESET_FCLK	R/W		reset_fclk
			0	release reset_fclk
			1	force reset_fclk

Table 41. MAN_PON register (address 01h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
5	MAN_PON_CLKBUFFER	R/W		pon_clkbuffer (when man_pon_cntrl = 1)
4	MAN_PON_ALL	R/W		pon_all (when man_pon_cntrl = 1)
3	MAN_PON_LN3	R/W		pon_ln3 (when man_pon_cntrl = 1)
2	MAN_PON_LN2	R/W		pon_ln2 (when man_pon_cntrl = 1
1	MAN_PON_LN1]	R/W		pon_ln1 (when man_pon_cntrl = 1)
0	MAN_PON_LN0	R/W		pon_ln0 (when man_pon_cntrl = 1)

Table 42. MAN_SUPD register (address 02h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	MAN_PLL_SEL_PD_LN3	R/W		sel_pd_ln3 (when man_supd_cntrl = 1)
6	MAN_PLL_SEL_PD_LN2	R/W		sel_pd_ln2 (when man_supd_cntrl = 1)
5	MAN_PLL_SEL_PD_LN1	R/W		sel_pd_ln1 (when man_supd_cntrl = 1)
4	MAN_PLL_SEL_PD_LN0	R/W		sel_pd_ln0 (when man_supd_cntrl = 1)
3	MAN_PLL_STARTUP_LN3	R/W		startup_ln3 (when man_supd_cntrl = 1)
2	MAN_PLL_STARTUP_LN2	R/W		startup_ln2 (when man_supd_cntrl = 1)
1	MAN_PLL_STARTUP_LN1	R/W		startup_ln1 (when man_supd_cntrl = 1)
0	MAN_PLL_STARTUP_LN0	R/W		startup_ln0 (when man_supd_cntrl = 1)

Table 43. RST_EXT_FCLK register (address 04h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	RST_EXT_FCLK[7:0]	R/W	3Fh	specifies extension-time reset_fclk in f_{clk} periods

Table 44. RST_EXT_DCLK register (address 05h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	RST_EXT_DCLK[7:0]	R/W	20h	specifies extension-time reset_dclk (in dclk-periods)

Table 45. DCSMU_PREDIVCNT register (address 06h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	DCSMU_PREDIVCNT[7:0]	R/W	1Eh	value used by dcsmu predivider (at f_{clk})

Table 46. PLL_CHARGETIME register (address 07h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	PLL_CHARGE_TIME[7:0]	R/W	32h	PLL chargetime (at f_{clk}/predivcnt; startup)

Table 47. PLL_RUN_IN_TIME register (address 08h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	PLL_RUNIN_TIME[7:0]	R/W	32h	PLL run in time (at f_{clk}/predivcnt; sel_pd)

Table 48. CA_RUN_IN_TIME register (address 09h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	CA_RUNIN_TIME[7:0]	R/W	04h	clock alignment run in time (at f_{clk}/predivcnt)

Table 49. IQ_LEVEL_CNTRL register (address 0Ah) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	ILEV_CNTRL[1:0]	R/W		
			0	I_IN <= DATA_I_CDI
			1	I_IN <= DATA_I_CDI when EN_DATA_I_CDI='1' else 1X: I_IN <= IQ_DC_LEVEL x 4
5 to 4	QLEV_CNTRL[1:0]	R/W		
			0	Q_IN <= DATA_Q_CDI
			1	Q_IN <= DATA_Q_CDI when EN_DATA_Q_CDI='1' else 1X: Q_IN <= IQ_DC_LEVEL X 4
3 to 0	IQ_DC_LEVEL[11:9]	R/W	-	msb's iq dc level

Table 50. IQ_DC_LEVEL_LSB register (address 0Bh) bit description

Bit	Symbol	Access	Value	Description
7 to 0	IQ_DC_LEVEL[7:0]	R/W	-	lsb's iq dc level

Table 51. SET_ICHP_PD1 register (address 10h) bit description

Bit	Symbol	Access	Value	Description
3 to 0	SET_ICHP_PD1[3:0]	R/W	-	integrating charge pump pd (error < 45 deg.)

Table 52. SET_ICHP_PD2 register (address 11h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
3 to 0	SET_ICHP_PD2[3:0]	R/W	01h	integrating charge pump pd (45 deg. < error < 90 deg.)

Table 53. SET_ICHP_PFD register (address 12h) bit description

Bit	Symbol	Access	Value	Description
3 to 0	SET_ICHP_PFD[3:0]	R/W	-	integrating charge pump pfd (linear PLL)

Table 54. SET_RATIO_PD1 register (address 13h) bit description

Bit	Symbol	Access	Value	Description
3 to 0	SET_RATIO_PD1[3:0]	R/W	-	proportional charge pump pd (error < 45 deg.)

Table 55. SET_RATIO_PD2 (address 14h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
3 to 0	SET_RATIO_PD2[3:0]	R/W	-	proportional charge pump pd (45 deg. < error < 90 deg.)

Table 56. SET_RATIO_PFD register (address 15h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	SET_RATIO_PFD[3:0]	R/W	-	proportional chargepump pfd (linear PLL)

Table 57. SET_VCM_VOLTAGE register (address 16h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	SET_VCM[2:0]	R/W		set Vcm voltage levelr

Table 58. SET_SYNC register (address 17h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	SET_SYNC_VCOM[3:0]	R/W		set sync transmitter common mode level
1 to 0	SET_SYNC_LEVEL[3:0]	R/W		set sync transmitter outputlevel swing

Table 59. MISC_CNTRLS register (address 1Ah) bit description

Bit	Symbol	Access	Value	Description
7	SPI_DAC_MXSEL	R/W		
			0	normal mode (inv_sinc à dac-inputs)
			1	io-bus direct mapped to dac-inputs
6	TEST_CLK_FB	R/W		
			0	~sync = i_sync (normal operation)
			1	~sync = f10_ln0
5	RING_OSC_TEST	R/W		
			0	no action
			1	ring_oscillator test enabled
4	DES_TEST	R/W	-	deserializer test mode
3	DAC_TEST	R/W	-	dac-tes mode
2	JD_MODE	R/W	-	ifdacdsp-mode (see section 3.2.1)
1	CDI_MODE	R/W	-	cdi-mode (see section 3.2.1)
0	SR_CDI	R/W	-	soft reset cdi

Table 60. IO_MUX_CNTRL0 register (address 1Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
6 to 4	DSP-SEL[2:0]	R/W		
			000	MX_DCLK <= EN_DATA_I_CDI and DATA_I_CDI_0
			001	MX_DCLK <= EN_DATA_I_CDI and DATA_I_CDI_1OFF
			010	MX_DCLK <= EN_DATA_Q_CDI and DATA_Q_CDI_0
			011	MX_DCLK <= EN_DATA_Q_CDI and DATA_Q_CDI_1
			100	MX_DCLK <= I_EN and I_OUT(INVSINC_I_OUT) and "00"
			101	MX_DCLK <= Q_EN and Q_OUT(INVSINC_Q_OUT) and "00" others: MX_DCLK <= "101010101010101"
3 to 2	DLP_SEL[1:0]	R/W		
			00	MX_FCLK <= EN_DATA_I_DLP and DATA_I_DLP
			01	MX_FCLK <= EN_DATA_Q_DLP and DATA_Q_DLP
			10	MX_FCLK <= MON_DBG_BUS
			11	MX_FCLK <= "010101010101010"
1 to 0	LN_SEL[1:0]	R/W		
			00	MX_A/MX_F10 <= DATA_LN0 / F10_LN0
			01	MX_A/MX_F10 <= DATA_LN1 / F10_LN1
			10	MX_A/MX_F10 <= DATA_LN2 / F10_LN2
			11	MX_A/MX_F10 <= DATA_LN3 / F10_LN3

Table 61. IO_MUX_CNTRL1 register (address 1Ch) bit description

Bit	Symbol	Access	Value	Description
4	SEL_RI	R/W		
			0	RO_INTR <= INTR
			1	RO_INTR <= RINGOSCILLATOR
3	SEL_FD	R/W		
			0	MX_D <= MX_FCLK
			1	MX_D <= MX_DCLK
2	SEL_AD	R/W		
			0	IO[14:0] <= "00000" & MX_A
			1	IO[14:0] <= MX_D
1 to 0	SEL_CK[1:0]	R/W		
			00	IO[15] <= RO_INTR
			01	IO[15] <= MX_F10
			10	IO[15] <= FCLK
			11	IO[15] <= DCLK

Table 62. DIG_VERSION register (address 1Dh) bit description

Bit	Symbol	Access	Value	Description
7 to 0	DIG_VERSION_ID[7:0]	R/W	-	metalfixable version -id within digital (standard cell)

Table 63. JRX_ANA_VERSION register (address 1Eh) bit description

Bit	Symbol	Access	Value	Description
7 to 0	JRX_ANA_VERSION_ID[7:0]	R/W	-	metalfixable version -id within analog deserializer

Table 64. PAGE_ADDRESS register (address 1Fh) bit description

Bit	Symbol	Access	Value	Description
2 to 0	PAGE	R/W	-	page address

10.15.2.5 Page 4 allocation map description

Table 65. Page 4 register allocation map

Address		Register name	R/W	Bit definition								Default	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
0	00h	SR_DLP_0	R/W	SR_SWA_LN3	SR_SWA_LN2	SR_SWA_LN1	SR_SWA_LN0	SR_CA_LN3	SR_CA_LN2	SR_CA_LN1	SR_CA_LN0	00000000	00h
1	01h	SR_DLP_1	R/W	SR_CNTRL_LN3	SR_CNTRL_LN2	SR_CNTRL_LN1	SR_CNTRL_LN0	SR_DEC_LN3	SR_DEC_LN2	SR_DEC_LN1	SR_DEC_LN0	00000000	00h
2	02h	FORCE_LOCK	R/W	FORCE_LOCK_LN3	FORCE_LOCK_LN2	FORCE_LOCK_LN1	FORCE_LOCK_LN0	-	-	-	SR_ILA	00000000	00h
3	03h	MAN_LOCK_LN_1_0	R/W	MAN_LOCK_LN1[3:0]				MAN_LOCK_LN0[3:0]				00000000	00h
4	04h	MAN_LOCK_2_0	R/W	MAN_LOCK_LN3[3:0]				MAN_LOCK_LN2[3:0]				00000000	00h
5	05h	CA_CNTRL	R/W	WORD_SWAP_LN3	WORD_SWAP_LN2	WORD_SWAP_LN1	WORD_SWAP_LN0	SELECT_RF_F10_LN3	SELECT_RF_F10_LN2	SELECT_RF_F10_LN1	SELECT_RF_F10_LN0	00000000	00h
6	06h	SCR-CNTRL	R/W	MAN_SCR_LN3	MAN_SCR_LN2	MAN_SCR_LN1	MAN_SCR_LN0	FORCE_SRC_LN3	FORCE_SRC_LN2	FORCE_SRC_LN1	FORCE_SRC_LN0	00000000	00h
7	07h	ILA_CNTRL	R/W	SEL_421_211	SEL_ILA[1:0]		SEL_LOCK[2:0]			SUP_LANE_SYN	EN_SCR	10000011	83h
8	08h	FORCE_ALIGN	R/W	-	-	-	-	-	-	DYN_ALIGN_ENA	FORCE_ALIGN	00000000	00h
9	09h	MAN_ALIGN_LN_0_1	R/W	MAN_ALIGN_LN1[3:0]				MAN_ALIGN_LN0[3:0]				00000000	00h
10	0Ah	MAN_ALIGN_LN_1_2	R/W	MAN_ALIGN_LN3[3:0]				MAN_ALIGN_LN2[3:0]				00000000	00h
11	0Bh	FA_ERR_HANDLING	R/W	SEL_KOUT_UNEXP_LN23		SEL_KOUT_UNEXP_LN10		SEL_NIT_ERR_LN23		SEL_NIT_ERR_LN10		00000000	00h
12	0Ch	SYNCOUT_MODE	R/W	SEL_RE_INIT[2:0]			SYNC_POL	SEL_SYNC[3:0]				00000000	00h
13	0Dh	LANE_POLARITY	R/W	-	-	-	-	POL_LN3	POL_LN2	POL_LN1	POL_LN0	00000000	00h
14	OEh	LANE_SELECT	R/W	LANE_SEL_LN3[1:0]		LANE_SEL_LN2[1:0]		LANE_SEL_LN1[1:0]		LANE_SEL_LN0[1:0]		11100100	E4h
16	10h	SOFT_RESET_SCRAMBLER	R/W	-	-	-	-	SR_SCR_LN3	SR_SCR_LN2	SR_SCR_LN1	SR_SCR_LN0	00000000	00h
17	11h	INIT_SCR_S15T8_LN0	R/W	INIT_VALUE_S15_S8_LN0[7:0]								00000000	00h

Table 65. Page 4 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
18	12h	INIT_SCR_S7T1_LN0	R/W	-	INIT_VALUE_S7_S1_LN0[6:0]							00000000	00h
19	13h	INIT_SCR_S15T8_LN1	R/W	INIT_VALUE_S15_S8_LN1[7:0]								00000000	00h
20	14h	INIT_SCR_S7T1_LN1	R/W	-	INIT_VALUE_S7_S1_LN1[6:0]							00000000	00h
21	15h	INIT_SCR_S15T8_LN2	R/W	INIT_VALUE_S15_S8_LN2[7:0]								00000000	00h
22	16h	INIT_SCR_S7T1_LN2	R/W	-	INIT_VALUE_S7_S1_LN2[6:0]							00000000	00h
23	17h	INIT_SCR_S15T8_LN3	R/W	INIT_VALUE_S15_S8_LN3[7:0]								00000000	00h
24	18h	INIT_SCR_S7T1_LN3	R/W	-	INIT_VALUE_S7_S1_LN3[6:0]							00000000	00h
25	19h	INIT_ILA_BUFPTR_LN01	R/W	INIT_ILA_BUFPTR_LN1[3:0]				INIT_ILA_BUFPTR_LN0[3:0]				10001000	88h
26	1Ah	INIT_ILA_BUFPTR_LN23	R/W	INIT_ILA_BUFPTR_LN3[3:0]				INIT_ILA_BUFPTR_LN2[3:0]				10001000	88h
27	1Bh	ERROR_HANDLING	R/W	-	NAD_ERR_CORR	KUX_CORR	NAD_CORR	CORR_MODE[1:0]		IMPL_ALT	IGNORE_ERR	00000000	00h
29	1Fh	PAGE_ADDRESS	R/W	PAGE								00000000	00h

10.15.2.6 Page 4 bit definition detailed description

Please refer to Table 65 for a register overview and their default values. In the following tables, all the values emphasized in bold are the default values.

Table 66. SR_DLP_0 register (address 00h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	SR_SWA_LN3	R/W		softreset sync_word_alignment lane_3
6	SR_SWA_LN2	R/W		softreset sync_word_alignment lane_2
5	SR_SWA_LN1	R/W		softreset sync_word_alignment lane_1
4	SR_SWA_LN0	R/W		softreset sync_word_alignment lane_0
3	SR_CA_LN3	R/W	**0**	softreset clock_alignment lane_3
2	SR_CA_LN2	R/W	1	softreset clock_alignment lane_2
1	SR_CA_LN1	R/W		softreset clock_alignment lane_1
0	SR_CA_LN0	R/W	**1**	softreset clock_alignment lane_0

Table 67. SR_DLP_1 register (address 01h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	SR_CNTRL_LN3	R/W		soft reset controller lane_3
6	SR_CNTRL_LN2	R/W		soft reset controller lane_2
5	SR_CNTRL_LN1	R/W		soft reset controller lane_1
4	SR_CNTRL_LN0	R/W		soft reset controller lane_0
3	SR_DEC_LN3	R/W		soft reset decoder_10b8b lane_3
2	SR_DEC_LN2	R/W		soft reset decoder_10b8b lane_2
1	SR_DEC_LN1	R/W		soft reset decoder_10b8b lane_1
0	SR_DEC_LN0	R/W		soft reset decoder_10b8b lane_0

Table 68. FORCE_LOCK register (address 02h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	FORCE_LOCK_LN3	R/W		
			0	automatic lock sync_word_alignment lane_3
			1	manual lock sync_word_alignment lane_3
6	FORCE_LOCK_LN22	R/W		
			0	automatic lock sync_word_alignment lane_2
			1	manual lock sync_word_alignment lane_2
5	FORCE_LOCK_LN1	R/W		
			0	automatic lock sync_word_alignment lane_1
			1	manual lock sync_word_alignment lane_1
4	FORCE_LOCK_LN0	R/W		
			0	automatic lock sync_word_alignment lane_0
			1	manual lock sync_word_alignment lane_0
0	SR_ILA	R/W		soft reset inter-lane-alignment

Table 69. MAN_LOCK_LN_1_0 register (address 03h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	MAN_LOCK_LN1[3:0]	R/W		manual lock-settting sync-word-alignment lane_1
3 to 0	MAN_LOCK_LN0[3:0]	R/W		manual lock-settting sync-word-alignment lane_0

Table 70. MAN_LOCK_2_0 register (address 04h) bit description

Bit	Symbol	Access	Value	Description
7 to 4	MAN_LOCK_LN3[3:0]	R/W		manual lock-settting sync-word-alignment lane_3
3 to 0	MAN_LOCK_LN2[3:0]	R/W		manual lock-settting sync-word-alignment lane_2

Table 71. CA_CNTRL register (address 05h) bit description

Bit	Symbol	Access	Value	Description
7	WORD_SWAP_LN3	R/W		
			0	dout_ca_ln3[7:0] = din_ca_ln3[7:0]
			1	dout_ca_ln3[7:0] = din_ca_ln3[0:7]
6	WORD_SWAP_LN2	R/W		
			0	dout_ca_ln2[7:0] = din_ca_ln2[7:0]
			1	dout_ca_ln2[7:0] = din_ca_ln2[0:7]
5	WORD_SWAP_LN1	R/W		
			0	dout_ca_ln1[7:0] = din_ca_ln1[7:0]
			1	dout_ca_ln1[7:0] = din_ca_ln1[0:7]
4	WORD_SWAP_LN0	R/W		
			0	dout_ca_ln0[7:0] = din_ca_ln0[7:0]
			1	dout_ca_ln0[7:0] = din_ca_ln0[0:7]
3	SELECT_RF_F10_LN3	R/W		
			0	din_ca_ln3 sampled @ falling edge f10_ln3
			1	din_ca_ln3 sampled @ rising edge f10_ln3
2	SELECT_RF_F10_LN2	R/W		
			0	din_ca_ln2 sampled @ falling edge f10_ln2
			1	din_ca_ln2 sampled @ rising edge f10_ln2
0	SELECT_RF_F10_LN1	R/W		
			0	din_ca_ln1 sampled @ falling edge f10_ln1
			1	din_ca_ln1 sampled @ rising edge f10_ln1
1	SELECT_RF_F10_LN0	R/W		
			0	din_ca_ln0 sampled @ falling edge f10_ln0
			1	din_ca_ln0 sampled @ rising edge f10_ln0

Table 72. SCR-CNTRL register (address 06h) bit description

Bit	Symbol	Access	Value	Description
7	MAN_SCR_LN3	R/W		
			0	scrambling ln3 off (when force_scr_ln3 = 1)
			1	scrambling ln3 on (when force_scr_ln3 = 1)
6	MAN_SCR_LN2	R/W		
			0	scrambling ln2 off (when force_scr_ln2 = 1)
			1	scrambling ln2 on (when force_scr_ln2 = 1)
5	MAN_SCR_LN1	R/W		
			0	scrambling ln1 off (when force_scr_ln1 = 1)
			1	scrambling ln1 on (when force_scr_ln1 = 1)
4	MAN_SCR_LN0	R/W		
			0	scrambling ln0 off (when force_scr_ln0 = 1)
			1	scrambling ln0 on (when force_scr_ln0 = 1)
3	FORCE_SRC_LN3	R/W		
			0	scrambling ln3 depends on lock_ln3 and en_scr
			1	scrambling ln3 depends on man_scr_ln3
2	FORCE_SRC_LN2	R/W		
			0	scrambling ln2 depends on lock_ln2 and en_scr
			1	scrambling ln2 depends on man_scr_ln2
1	FORCE_SRC_LN1	R/W		
			0	scrambling ln1 depends on lock_ln1 and en_scr
			1	scrambling ln1 depends on man_scr_ln1
0	FORCE_SRC_LN0	R/W		
			0	scrambling ln0 depends on lock_ln0 and en_scr
			1	scrambling ln0 depends on man_scr_ln0

Table 73. ILA_CNTRL register (address 07h) bit description

Bit	Symbol	Access	Value	Description
7	SEL_421_211	R/W		
			0	inter-lane alignment based on ln3:ln2 and/or ln1:ln0
			1	inter-lane alignment based on ln3:ln0
6 to 5	SEL_ILA[1:0]	R/W		
			00	ila is done after receiving 1 /A/-symbol
			01	ila is done after receiving 2 /A/-symbols
			10	ila is done after receiving 3 /A/-symbols
			11	ila is done after receiving 4 /A/-symbols
4 to 2	SEL_LOCK[2:0]	R/W		
			000	ila may start only if all (4 or 2) lanes are locked
			001	ila may start if one of the (4 or 2) lanes are locked
			010	ila may start if lane_0 is locked
			011	ila may start if lane_1 is locked
			100	ila may start if lane_2 is locked
			101	ila may start if lane_3 is locked
1	SUP_LANE_SYN	R/W		
			0	inter lane alignment synchronization disabled
			1	inter lane alignment synchronization enabled
0	EN_SCR	R/W		
			0	data descrambling disabled
			1	scrambling ln0 depends on data descrambling enabled

Table 74. FORCE_ALIGN register (address 08h) bit description

Bit	Symbol	Access	Value	Description
1	DYN_ALIGN_ENA	R/W	20h	
			0	no dynamic re-alignment
			1	dynamic re-alignment (and monitoring) enabled
0	FORCE_ALIGN	R/W	20h	
			0	automatic lane alignment based on /A/-symbols
			1	manual lane alignment based on man_align_lnx

Table 75. MAN_ALIGN_LN_0_1 register (address 09h) bit description

Bit	Symbol	Access	Value	Description
7 to 4	MAN_ALIGN_LN1[3:0]	R/W	32h	indicates alignment data-delay for lane_1 [1..15]
3 to 0	MAN_ALIGN_LN0[3:0]	R/W	32h	indicates alignment data-delay for lane_0 [1..15]

Table 76. MAN_ALIGN_LN_0_1 register (address 0Ah) bit description

Bit	Symbol	Access	Value	Description
7 to 4	MAN_ALIGN_LN3[3:0]	R/W	32h	indicates alignment data-delay for lane_3 [1..15]
3 to 0	MAN_ALIGN_LN2[3:0]	R/W	32h	indicates alignment data-delay for lane_2 [1..15]

Table 77. FA_ERR_HANDLING register (address 0Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	SEL_KOUT_UNEXP_LN23[1:0]	R/W		
			00	error_handling i.c.o. unexpected /K/ in lane 2 or 3
			01	error_handling i.c.o. unexpected /K/ in lane 2 and 3
			10	error_handling i.c.o. unexpected /K/ in lane 2
			11	error_handling i.c.o. unexpected /K/ in lane 3
5 to 4	SEL_KOUT_UNEXP_LN10[1:0]	R/W		
			00	error_handling i.c.o. unexpected /K/ in lane 0 or 1
			01	error_handling i.c.o. unexpected /K/ in lane 0 and 1
			10	error_handling i.c.o. unexpected /K/ in lane 0
			11	error_handling i.c.o. unexpected /K/ in lane 1
3 to 2	SEL_NIT_ERR_LN23[1:0]	R/W		
			00	error_handling i.c.o. nit-errors in lane 2 or 3
			01	error_handling i.c.o. nit-errors lane 2 and 3
			10	error_handling i.c.o. nit-errors in lane 2
			11	error_handling i.c.o. nit-errors in lane 3
1 to 0	SEL_NIT_ERR_LN10[1:0]	R/W		
			00	error_handling i.c.o. nit-errors in lane 0 or 1
			01	error_handling i.c.o. nit-errors lane 0 and 1
			10	error_handling i.c.o. nit-errors in lane 0
			11	error_handling i.c.o. nit-errors in lane 1

Table 78. SYNCOUT_MODE register (address 0Ch) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	SEL_RE_INIT[2:0]	R/W		
			000	i_re_init when 1 of the lane_rst's is active
			001	i_re_init when rst_ln0 or rst_ln1 is active
			010	i_re_init when rst_ln2 or rst_ln3 is active
			011	i_re_init when rst_ln0 is active
			100	i_re_init when rst_ln1 is active
			101	i_re_init when rst_ln2 is active
			110	i_re_init when rst_ln3 is active
			111	i_re_init remains '0'
4	SYNC_POL	R/W		
			0	sync_out is active when low
			0	sync_out is active when high
3 to 0	SEL_SYNC[3:0]	R/W		
			0000	sync when 1 of the 4 lane_sync's is active
			0001	sync when all 4 lane_sync;s are active
			0010	sync when sync_ln0 or sync_ln1 is active
			0011	sync when both sync_ln0 and sync_ln1 are active
			0100	sync when sync_ln2 or sync_ln3 is active
			0101	sync when both sync_ln2 and sync_ln3 are active
			0110	sync when sync_ln0 is active
			0111	sync when sync_ln1 is active
			1000	sync when sync_ln2 is active
			1001	sync when sync_ln3 is active
			1010	sync remains fixed '1'
			other	sync remains fixed '0'

Table 79. LANE_POLARITY register (address 1Dh) bit description

Bit	Symbol	Access	Value	Description
3	POL_LN3L	R/W		
			0	no action
			1	invert all databits of dout_ca_ln3[7:0]
2	POL_LN2	R/W		
			0	no action
			1	invert all databits of dout_ca_ln2[7:0]
1	POL_LN1	R/W		
			0	no action
			1	invert all databits of dout_ca_ln1[7:0]
0	POL_LN0	R/W		
				no action
				invert all databits of dout_ca_ln0[7:0]

Table 80. LANE_SELECT register (address 0Eh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	LANE_SEL_LN3[1:0]	R/W		
			00	ila_in_ln3 = lane_ln0 (dout and controls)
			01	ila_in_ln3 = lane_ln1 (dout and controls)
			10	ila_in_ln3 = lane_ln2 (dout and controls)
			11	ila_in_ln3 = lane_ln3 (dout and controls)
5 to 4	LANE_SEL_LN2[1:0]	R/W		
			00	ila_in_ln2 = lane_ln0 (dout and controls)
			01	ila_in_ln2 = lane_ln1 (dout and controls)
			10	ila_in_ln2 = lane_ln2 (dout and controls)
			11	ila_in_ln2 = lane_ln3 (dout and controls)
3 to 2	LANE_SEL_LN1[1:0]	R/W		
			00	ila_in_ln1 = lane_ln0 (dout and controls)
			01	ila_in_ln1 = lane_ln1 (dout and controls)
			10	ila_in_ln1 = lane_ln2 (dout and controls)
			11	ila_in_ln1 = lane_ln3 (dout and controls
1 to 0	LANE_SEL_LN0[1:0]	R/W		
			00	ila_in_ln0 = lane_ln0 (dout and controls)
			01	ila_in_ln0 = lane_ln1 (dout and controls)
			10	ila_in_ln0 = lane_ln2 (dout and controls)
			11	ila_in_ln0 = lane_ln3 (dout and controls)

Table 81. SOFT_RESET_SCRAMBLER register (address 10h) bit description

Bit	Symbol	Access	Value	Description
3	SR_SCR_LN3	R/W		
			0	no action
			1	soft_reset scrambler of lane0
2	SR_SCR_LN2	R/W		
			0	no action
			1	soft_reset scrambler of lane1
1	SR_SCR_LN1	R/W		
			0	no action
			1	soft_reset scrambler of lane2
0	SR_SCR_LN0	R/W		
				no action
				soft_reset scrambler of lane3

Table 82. INIT_SCR_S15T8_LN0 register (address 11h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	INIT_VALUE_S15_S8_LN0[7:0]	R/W	-	init value for ln0 descrambler bits s15:s8

Table 83. INIT_SCR_S7T1_LN0 (address 12h) bit description

Bit	Symbol	Access	Value	Description
6 to 0	INIT_VALUE_S7_S1_LN0[6:0]	R/W	-	init value for ln0 descrambler bits s7:s1

Table 84. INIT_SCR_S15T8_LN1 register (address 13h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	INIT_VALUE_S15_S8_LN1[7:0]	R/W	01h	init value for ln1 descrambler bits s15:s8

Table 85. INIT_SCR_S7T1_LN1 register (address 14h) bit description

Bit	Symbol	Access	Value	Description
6 to 0	INIT_VALUE_S7_S1_LN1[6:0]	R/W	-	init value for ln1 descrambler bits s7:s1

Table 86. INIT_SCR_S15T8_LN2 register (address 15h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	INIT_VALUE_S15_S8_LN2[7:0]	R/W	-	init value for ln2 descrambler bits s15:s8

Table 87. INIT_SCR_S7T1_LN2 register (address 16h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
6 to 0	INIT_VALUE_S7_S1_LN2[6:0]	R/W	-	init value for ln2 descrambler bits s7:s1

Table 88. INIT_SCR_S15T8_LN3 register (address 17h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	INIT_VALUE_S15_S8_LN3[7:0]	R/W	-	init value for ln3 descrambler bits s15:s8

Table 89. INIT_SCR_S7T1_LN3 register (address 18h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	INIT_VALUE_S7_S1_LN3[6:0]	R/W		init value for ln3 descrambler bits s7:s1

Table 90. INIT_ILA_BUFPTR_LN01 register (address 19h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	INIT_ILA_BUFPTR_LN1[3:0]	R/W		init value for ila bufptr ln1
3 to 0	INIT_ILA_BUFPTR_LN0[3:0]	R/W		init value for ila bufptr ln0

Table 91. INIT_ILA_BUFPTR_LN23 register (address 1Ah) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	INIT_ILA_BUFPTR_LN3[3:0]	R/W		init value for ila bufptr ln3
3 to 0	INIT_ILA_BUFPTR_LN2[3:0]	R/W		init value for ila bufptr ln2

Table 92. ERROR_HANDLING register (address 1Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
6	NAD_ERR_CORR	R/W		
			0	nit-errors passed to frame-assembler (fa‘)
			1	nad(nit- and disparity)-errors passed to fa
5	KUX_CORR	R/W		
			0	unexpected k-character errors ignored (@fa)
			01	unexpected k-character errors concealment(2fa)
4	NAD_CORR	R/W		
			0	nad-errors ignored (@fa)
			1	nad-errors concealment (@fa)
3 to 2	CORR_MODE[1:0]	R/W		
			00	conceal 1 period @ fa
			01	conceal 2 periods @ fa
			10	conceal 3 periods @ fa
			11	conceal 4 periods @ fa
1	IMPL_ALT	R/W		
			0	default disparity error detection (table-mode)
			01	alternative disparity error detection (cnt-mode)
0	IGNORE_ERR	R/W		
			0	no action
			1	ignore disparity/nit-errors @ lane-controller

Table 93. PAGE_ADDRESS register (address 1Fh) bit description

Bit	Symbol	Access	Value	Description
2 to 0	PAGE	R/W	-	page_address

10.15.2.7 Page 5 allocation map description

Table 94. Page 5 register allocation map

Address		Register name	R/W	Bit definition								Default	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
0	00h	ILA_MON_1_0	R	ILA_MON_LN1[3:0]				ILA_MON_LN0[3:0				<tbd>	<tbd>
1	01h	ILA_MON_3_2	R	ILA_MON_LN3[3:0]				ILA_MON_LN2[3:0]				<tbd>	<tbd>
2	02h	ILA_BUF_ERR	R	-	-	-	-	ILA_BUF_ERR_LN3	ILA_BUF_ERR_LN2	ILA_BUF_ERR_LN1	ILA_BUF_ERR_LN0	<tbd>	<tbd>
3	03h	CA_MON	R	CA_MON_LN3[1:0]		CA_MON_LN2[1:0]		CA_MON_LN1[1:0]		CA_MON_LN0[1:0]		<tbd>	<tbd>
4	04h	DEC_FLAGS	R	DEC_NIT_ERR_LN3	DEC_NIT_ERR_LN2	DEC_NIT_ERR_LN1	DEC_NIT_ERR_LN0	DEC_DISP_ERR_LN3	DEC_DISP_ERR_LN2	DEC_DISP_ERR_LN1	DEC_DISP_ERR_LN0	<tbd>	<tbd>
5	05h	KOUT_FLAG	R	-	-	-	-	DEC_KOUT_LN3	DEC_KOUT_LN2	DEC_KOUT_LN1	DEC_KOUT_LN0	<tbd>	<tbd>
6	06h	K28_LN0_FLAG	R	-	-	-	K28_7_LN0	K28_5_LN0	K28_4_LN0	K28_3_LN0	K28_0_LN0	<tbd>	<tbd>
6	07h	K28_LN1_FLAG	R	-	-	-	K28_7_LN1	K28_5_LN1	K28_4_LN1	K28_3_LN1	K28_0_LN1	<tbd>	<tbd>
7	08h	K28_LN2_FLAG	R	-	-	-	K28_7_LN2	K28_5_LN2	K28_4_LN2	K28_3_LN2	K28_0_LN2	<tbd>	<tbd>
8	09h	K28_LN3_FLAG	R	-	-	-	K28_7_LN3	K28_5_LN3	K28_4_LN3	K28_3_LN3	K28_0_LN3	<tbd>	<tbd>
9	0Ah	KOUT_UNEXPECTED_FLAG	R	-	-	-	-	DEC_KOUT_UNEXP_LN3	DEC_KOUT_UNEXP_LN2	DEC_KOUT_UNEXP_LN1	DEC_KOUT_UNEXP_LN0	<tbd>	<tbd>
10	0Bh	LOCK_CNT_MON_LN01	R	LOCK_CNT_MON_LN1[3:0]				LOCK_CNT_MON_LN0[3:0]				<tbd>	<tbd>
11	0Ch	LOCK_CNT_MON_LN23	R	LOCK_CNT_MON_LN3[3:0]				LOCK_CNT_MON_LN2[3:0]				<tbd>	<tbd>
16	10h	FLAG_CNT_LSB_LN0	R	FLAG_CNT_LN0[7:0]								<tbd>	<tbd>
17	11h	FLAG_CNT_MSB_LN0	R	FLAG_CNT_LN0[15:8]								<tbd>	<tbd>
18	12h	FLAG_CNT_LSB_LN1	R	FLAG_CNT_LN1[7:0]								<tbd>	<tbd>
19	13h	FLAG_CNT_MSB_LN1	R	FLAG_CNT_LN1[15:8]								<tbd>	<tbd>
20	14h	FLAG_CNT_LSB_LN2	R	FLAG_CNT_LN2[7:0]								<tbd>	<tbd>
21	15h	FLAG_CNT_MSB_LN2	R	FLAG_CNT_LN2[15:8]								<tbd>	<tbd>

Table 94. Page 5 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
22	16h	FLAG_CNT_LSB_LN3	R	FLAG_CNT_LN3[7:0]								<tbd>	<tbd>
23	17h	FLAG_CNT_MSB_LN3	R	FLAG_CNT_LN3[15:8]								<tbd>	<tbd>
25	19h	BER_LEVEL	R/W	BER_LEVEL[7:0]								<tbd>	<tbd>
26	1Ah	INTR_ENA	R/W	INTR_ENA_NIT	INTR_ENA_DISP	INTR_ENA_KOUT	INTR_ENA_KOUT_UNEXP	INTR_ENA_K28_7	INTR_ENA_K28_5	INTR_ENA_K28_3	INTR_ENA_K28_0	<tbd>	<tbd>
27	1Bh	CNTRL_FLAGCNT_LN01	R/W	RST_CFC_LN1	SEL_CFC_LN1[2:0]			RST_CFC_LN0	SEL_CFC_LN0[2:0]			<tbd>	<tbd>
28	1Ch	CNTRL_FLAGCNT_LN23	R/W	RST_CFC_LN3	SEL_CFC_LN3[2:0]			RST_CFC_LN2	SEL_CFC_LN2[2:0]			<tbd>	<tbd>
29	1Dh	MON_FLAGS_RESET	R/W	RST_NIT_ERR-FLAGS	RST_DISP_ERR_FLAGS	RST_KOUT_FLAGS	RST_KOUT_UNEXPECTED_FLAGS	RST_K28_LN3_FLAGS	RST_K28_LN2_FLAGS	RST_K28_LN1_FLAGS	RST_K28_LN0_FLAGS	<tbd>	<tbd>
30	1Eh	DBG_CNTRL	R/W	BER_MODE	INTR_CLEAR	INTR_MODE			DBG_MODE			<tbd>	<tbd>
31	1Fh	PAGE_ADDRESS	R/W	PAGE								<tbd>	<tbd>

10.15.2.8 Page 5 bit definition detailed description

Please refer to Table 94 for a register overview and their default values. In the following tables, all the values emphasized in bold are the default values.

Table 95. ILA_MON_1_0 register (address 00h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	ILA_MON_LN1[3:0]	R/W		ila_buf_ln1 pointer
3 to 0	ILA_MON_LN0[3:0]	R/W		ila_buf_ln0 pointer

Table 96. ILA_MON_3_2 register (address 01h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	ILA_MON_LN3[3:0]	R/W		ila_buf_ln3 pointer
3 to 0	ILA_MON_LN2[3:0]	R/W		ila_buf_ln2 pointer

Table 97. ILA_BUF_ERR register (address 02h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
3	ILA_BUF_ERR_LN3	R/W		
			0	ila_buf_ln3 pointer is in range
			1	ila_buf_ln3 pointer is out of range
2	ILA_BUF_ERR_LN2	R/W		
			0	ila_buf_ln2 pointer is in range
			1	ila_buf_ln2 pointer is out of range
1	ILA_BUF_ERR_LN1	R/W		
			0	ila_buf_ln1 pointer is in range
			1	ila_buf_ln1 pointer is out of range
0	ILA_BUF_ERR_LN0	R/W		
			0	ila_buf_ln0 pointer is in range
			1	ila_buf_ln0 pointer is out of range

Table 98. CA_MON register (address 03h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	CA_MON_LN3[1:0]	R/W		clock alignment phase monitor lane_3
5 to 4	CA_MON_LN2[1:0]	R/W		clock alignment phase monitor lane_2
3 to 2	CA_MON_LN1[1:0]	R/W		clock alignment phase monitor lane_1
1 to 0	CA_MON_LN0[1:0]	R/W		clock alignment phase monitor lane_0

Table 99. DEC_FLAGS register (address 04h) bit description

Bit	Symbol	Access	Value	Description
7	DEC_NIT_ERR_LN3	R/W		not-in-table-errorflag lane_3
6	DEC_NIT_ERR_LN2	R/W		not-in-table-errorflag lane_2
5	DEC_NIT_ERR_LN1	R/W		not-in-table-errorflag lane_1
4	DEC_NIT_ERR_LN0	R/W		not-in-table-errorflag lane_0
3	DEC_DISP_ERR_LN3	R/W		disparity-errorflag lane_3
2	DEC_DISP_ERR_LN2	R/W		disparity-errorflag lane_2
1	DEC_DISP_ERR_LN1	R/W		disparity-errorflag lane_1
0	DEC_DISP_ERR_LN0	R/W		disparity-errorflag lane_0

Table 100. KOUT_FLAG register (address 05h) bit description

Bit	Symbol	Access	Value	Description
3	DEC_KOUT_LN3	R/W		/K/-symbols found in lane_3
2	DEC_KOUT_LN2	R/W		/K/-symbols found in lane_2
1	DEC_KOUT_LN1	R/W		/K/-symbols found in lane_1
0	DEC_KOUT_LN0	R/W		/K/-symbols found in lane_0

Table 101. K28_LN0_FLAG register (address 06h) bit description

Bit	Symbol	Access	Value	Description
4	K28_7_LN0	R/W		k28_7 /F/ -symbols found in lane_0
3	K28_5_LN0	R/W		k28_5 /K/ -symbols found in lane_0
2	K28_4_LN0	R/W		k28_4 /Q/ -symbols found in lane_0
1	K28_3_LN0	R/W		k28_3 /A/ -symbols found in lane_0
0	K28_0_LN0	R/W		k28_0 /R/ -symbols found in lane_0

Table 102. K28_LN1_FLAG register (address 07h) bit description

Bit	Symbol	Access	Value	Description
4	K28_7_LN1	R/W		k28_7 /F/ -symbols found in lane_1
3	K28_5_LN1	R/W		k28_5 /K/ -symbols found in lane_1
2	K28_4_LN1	R/W		k28_4 /Q/ -symbols found in lane_1
1	K28_3_LN1	R/W		k28_3 /A/ -symbols found in lane_1
0	K28_0_LN1	R/W		k28_0 /R/ -symbols found in lane_1

Table 103. K28_LN2_FLAG register (address 08h) bit description

Bit	Symbol	Access	Value	Description
4	K28_7_LN2	R/W		k28_7 /F/ -symbols found in lane_2
3	K28_5_LN2	R/W		k28_5 /K/ -symbols found in lane_2
2	K28_4_LN2	R/W		k28_4 /Q/ -symbols found in lane_2
1	K28_3_LN2	R/W		k28_3 /A/ -symbols found in lane_2
0	K28_0_LN2	R/W		k28_0 /R/ -symbols found in lane_2

Table 104. K28_LN3_FLAG register (address 09h) bit description

Bit	Symbol	Access	Value	Description
4	K28_7_LN3	R/W		k28_7 /F/ -symbols found in lane_3
3	K28_5_LN3	R/W		k28_5 /K/ -symbols found in lane_3
2	K28_4_LN3	R/W		k28_4 /Q/ -symbols found in lane_3
1	K28_3_LN3	R/W		k28_3 /A/ -symbols found in lane_3
0	K28_0_LN3	R/W		k28_0 /R/ -symbols found in lane_3

Table 105. LOCK_CNT_MON_LN01 register (address 0Ah) bit description

Bit	Symbol	Access	Value	Description
3	DEC_KOUT_UNEXP_LN3	R/W		Unexpected /K/-symbols found in lane_3
2	DEC_KOUT_UNEXP_LN2	R/W		Unexpected /K/-symbols found in lane_2
1	DEC_KOUT_UNEXP_LN1	R/W		Unexpected /K/-symbols found in lane_1
0	DEC_KOUT_UNEXP_LN0	R/W		Unexpected /K/-symbols found in lane_0

Table 106. ILA_MON_3_2 register (address 0Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	LOCK_CNT_MON_LN1[3:0]	R/W		lock_state monitor sync-word-alignment ln1
3 to 0	LOCK_CNT_MON_LN0[3:0]	R/W		lock_state monitor sync-word-alignment ln0

Table 107. LOCK_CNT_MON_LN23 register (address 0Ch) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	LOCK_CNT_MON_LN3[3:0]	R/W		lock_state monitor sync-word-alignment ln3
3 to 0	LOCK_CNT_MON_LN2[3:0]	R/W		lock_state monitor sync-word-alignment ln2

Table 108. FLAG_CNT_LSB_LN0 register (address 10h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	IFLAG_CNT_LN0[7:0]	R/W		lsb's of flag_counter ln0

Table 109. FLAG_CNT_MSB_LN0 register (address 11h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	FLAG_CNT_LN0[15:8]	R/W		msb's of flag_counter ln0

Table 110. FLAG_CNT_LSB_LN1 register (address 12h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	FLAG_CNT_LN1[7:0]	R/W		lsb's of flag_counter ln1

Table 111. FLAG_CNT_MSB_LN1 register (address 13h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	FLAG_CNT_LN1[15:8]	R/W		msb's of flag_counter ln11

Table 112. FLAG_CNT_LSB_LN2 register (address 14h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	FLAG_CNT_LN2[7:0]	R/W		lsb's of flag_counter ln2

Table 113. FLAG_CNT_MSB_LN2 register (address 15h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	FLAG_CNT_LN2[15:8]	R/W		msb's of flag_counter ln2

Table 114. FLAG_CNT_LSB_LN3 register (address 16h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	FLAG_CNT_LN3[7:0]	R/W		lsb's of flag_counter ln3

Table 115. FLAG_CNT_MSB_LN3 register (address 17h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	FLAG_CNT_LN3[15:8]	R/W		msb's of flag_counter ln3

Table 116. BER_LEVEL register (address 19h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	BER_LEVEL[7:0]	R/W		level used for simple(dc) ber-measurement

Table 117. INTR_ENA register (address 1Ah) bit description

Bit	Symbol	Access	Value	Description
7	INTR_ENA_NIT	R/W		
			0	no action
			1	nit-error in ln<x> affects i_ln<x>
6	INTR_ENA_DISP	R/W		
			0	no action
			1	disparity-error in ln<x> affects i_ln<x>
5	INTR_ENA_KOUT	R/W		
			0	no action
			1	detection k-controlcharacter in ln<x> affects i_ln<x>
4	INTR_ENA_KOUT_UNEXP	R/W		
			0	no action]
			1	detection unexpected kchar in ln<x> affects i_ln<x>
3	INTR_ENA_K28_7	R/W		
			0	no action
			1	detection k28_7 in ln<x> affects i_ln<x>

Table 117. INTR_ENA register (address 1Ah) bit description *...continued*

Bit	Symbol	Access	Value	Description
2	INTR_ENA_K28_5	R/W		
			0	no action
			1	detection k28_5 in In<x> affects i_In<x>
1	INTR_ENA_K28_3	R/W		
			0	no action
			1	detection k28_3 in In<x> affects i_In<x>
0	INTR_ENA_K28_0	R/W		
			0	no action
			1	detection k28_0 in In<x> affects i_In<x>

Table 118. CNTRL_FLAGCNT_LN01 register (address 1Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	RST_CFC_LN1	R/W		reset flagcnt ln1
6 to 4	SEL_CFC_LN1[2:0]	R/W		select cnt-enable flagcnt ln1 (see section 4.4)
3	RST_CFC_LN0	R/W		reset flagcnt ln0
2 to 0	SEL_CFC_LN0[2:0]	R/W		select cnt-enable flagcnt ln0 (see section 4.4)

Table 119. CNTRL_FLAGCNT_LN23 register (address 1Ch) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	RST_CFC_LN3	R/W		reset flagcnt ln3
6 to 4	SEL_CFC_LN3[2:0]	R/W		select cnt-enable flagcnt ln3 (see section 4.4)
3	RST_CFC_LN2	R/W		reset flagcnt ln2
2 to 0	SEL_CFC_LN2[2:0]	R/W		select cnt-enable flagcnt ln2 (see section 4.4)

Table 120. MON_FLAGS_RESET register (address 1Dh) bit description

Bit	Symbol	Access	Value	Description
7	RST_NIT_ERR-FLAGS	R/W		reset nit-error monitor flags
6	RST_DISP_ERR_FLAGS	R/W		reset disparity monitor flags
5	RST_KOUT_FLAGS	R/W		reset k-symbols monitor flags
4	RST_KOUT_UNEXPECTED_FLAGS	R/W		reset unexpected k-symbols monitor flags
3	RST_K28_LN3_FLAGS	R/W		reset k28_x monitor flags for ln3
2	RST_K28_LN2_FLAGS	R/W		reset k28_x monitor flags for ln2
1	RST_K28_LN1_FLAGS	R/W		reset k28_x monitor flags for ln1
0	RST_K28_LN0_FLAGS0	R/W		reset k28_x monitor flags for ln0

Table 121. DBG_CNTRL register (address 1Eh) bit description

Bit	Symbol	Access	Value	Description
7	BER_MODE	R/W		
			0	no action
			1	simple BER-measurement enabled
6	INTR_CLEAR	R/W		
			00	no action
			01	clear interrupt (to '1')s
5 to 3	INTR_MODE[2:0]	R/W		
			000	intr depends on i_ln0
			001	intr depends on i_ln1
			010	intr depends on i_ln2
			011	intr depends on i_ln3
			100	intr depends on i_ln0 or i_ln1
			101	intr depends on i_ln2 or i_ln3
			110	intr depends on i_ln0 or i_ln1 or i_ln2 or i_ln3
			111	no interrupt
2 to 0	DBG_MODE	R/W		selects signals for mon_dbg_bus (see section A.1)

Table 122. PAGE_ADDRESS register (address 1Fh) bit description

Bit	Symbol	Access	Value	Description
2 to 0	PAGE	R/W	-	page_address

10.15.2.9 Page 6 allocation map description

Table 123. Page 6 register allocation map

Address		Register name	R/W	Bit definition								Default	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
0	00h	LN0_CFG_0	R	LN0_DID[7:0]								<tbd>	<tbd>
1	01h	LN0_CFG_1	R	-	-	-	-	LN0_BID[3:0]				<tbd>	<tbd>
2	02h	LN0_CFG_2	R	-	-	-	LN0_LID[4:0]					<tbd>	<tbd>
3	03h	LN0_CFG_3	R	LN0_SCR	-	-	LN0_L[4:0]					<tbd>	<tbd>
4	04h	LN0_CFG_4	R	LN0_F[7:0]								<tbd>	<tbd>
5	05h	LN0_CFG_5	R	-	-	-	LN0_K[4:0]					<tbd>	<tbd>
6	06h	LN0_CFG_6	R	LN0_M[7:0]								<tbd>	<tbd>
7	07h	LN0_CFG_7	R	LN0_CS[1:0]		-	LN0_N[4:0]					<tbd>	<tbd>
8	08h	LN0_CFG_8	R	-	-	-	LN0_N'[4:0]					<tbd>	<tbd>
9	09h	LN0_CFG_9	R	-	-	-	LN0_S[4:0]					<tbd>	<tbd>
10	0Ah	LN0_CFG_10	R	LN0_HD	-	-	LN0_CF[4:0]					<tbd>	<tbd>
11	0Bh	LN0_CFG_11	R	LN0_RES1[7:0]								<tbd>	<tbd>
12	0Ch	LN0_CFG_12	R	LN0_RES2[7:0]								<tbd>	<tbd>
13	0Dh	LN0_CFG_13	R	LN0_FCHK[7:0]								<tbd>	<tbd>
16	10h	LN1_CFG_0	R	LN1_DID[7:0]								<tbd>	<tbd>
17	11h	LN1_CFG_1	R	-	-	-	-	LN1_BID[3:0]				<tbd>	<tbd>
18	12h	LN1_CFG_2	R	-	-	-	LN1_LID[4:0]					<tbd>	<tbd>
19	13h	LN1_CFG_3	R	LN1_SCR	-	-	LN1_L[4:0]					<tbd>	<tbd>
20	14h	LN1_CFG_4	R	LN1_F[7:0]								<tbd>	<tbd>
21	15h	LN1_CFG_5	R	-	-	-	LN1_K[4:0]					<tbd>	<tbd>
22	16h	LN1_CFG_6	R	LN1_M[7:0]								<tbd>	<tbd>
23	17h	LN1_CFG_7	R	LN1_CS[1:0]		-	LN1_N[4:0]					<tbd>	<tbd>
24	18h	LN1_CFG_8	R	-	-	-	LN1_N'[4:0]					<tbd>	<tbd>
25	19h	LN1_CFG_9	R	-	-	-	LN1_S[4:0]					<tbd>	<tbd>
26	1Ah	LN1_CFG_10	R	LN1_HD	-	-	LN1_CF[4:0]					<tbd>	<tbd>
27	1Bh	LN1_CFG_11	R	LN1_RES1[7:0]								<tbd>	<tbd>

Table 123. Page 6 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
28	1Ch	LN1_CFG_12	R	LN1_RES2[7:0]								<tbd>	<tbd>
29	1Dh	LN1_CFG_13	R	LN1_FCHK[7:0]								<tbd>	<tbd>
31	1Fh	PAGE_ADDRESS	R/W	PAGE								<tbd>	<tbd>

10.15.2.10 Page 6 bit definition detailed description

Please refer to Table 123 for a register overview and their default values. In the following tables, all the values emphasized in bold are the default values.

Table 124. LN0_CFG_0 register (address 00h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	LN0_DID[7:0]	R/W		

Table 125. LN0_CFG_1 register (address 01h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
3 to 0	LN0_BID[3:0]	R/W		

Table 126. LN0_CFG_2 register (address 02h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
4 to 0	LN0_LID[4:0]	R/W		

Table 127. LN0_CFG_3 register (address 03h) bit description
Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	LN0_SCR	R/W		
4 to 0	LN0_L[4:0]	R/W		

Table 128. LN0_CFG_4 register (address 04h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN0_F[7:0]	R/W		

Table 129. LN0_CFG_5 register (address 05h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN0_K[4:0]	R/W		

Table 130. LN0_CFG_6 register (address 06h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN0_M[7:0]	R/W		

Table 131. LN0_CFG_7 register (address 07h) bit description

Bit	Symbol	Access	Value	Description
7 to 6	LN0_CS[1:0]	R/W		
4 to 0	LN0_N[4:0]	R/W		

Table 132. LN0_CFG_8 register (address 08h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN0_N'[4:0]	R/W		

Table 133. LN0_CFG_9 register (address 09h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN0_S[4:0]	R/W		

Table 134. LN0_CFG_10 register (address 0Ah) bit description

Bit	Symbol	Access	Value	Description
7	LN0_HD	R/W		
4 to 0	LN0_CF[4:0]	R/W		

Table 135. LN0_CFG_11 register (address 0Bh) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN0_RES1[7:0]	R/W		

Table 136. LN0_CFG_12 register (address 0Ch) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN0_RES2[7:0]	R/W		

Table 137. LN0_CFG_13 register (address 0Dh) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN0_FCHK[7:0]	R/W		

Table 138. LN1_CFG_0 register (address 10h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN1_DID[7:0]	R/W		

Table 139. LN1_CFG_1 register (address 11h) bit description

Bit	Symbol	Access	Value	Description
3 to 0	LN1_BID[3:0]	R/W		

Table 140. LN1_CFG_2 register (address 12h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN1_LID[4:0]	R/W		

Table 141. LN1_CFG_3 register (address 13h) bit description

Bit	Symbol	Access	Value	Description
7	LN1_SCR	R/W		
4 to 0	LN1_L[4:0]	R/W		

Table 142. LN1_CFG_4 register (address 14h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN1_F[7:0]	R/W		

Table 143. LN1_CFG_5 register (address 15h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN1_K[4:0]	R/W		

Table 144. LN1_CFG_6 register (address 16h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN1_M[7:0]	R/W		

Table 145. LN1_CFG_7 register (address 17h) bit description

Bit	Symbol	Access	Value	Description
7 to 6	LN1_CS[1:0]	R/W		
4 to 0	LN1_N[4:0]	R/W		

Table 146. LN1_CFG_8 register (address 18h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN1_N'[4:0]	R/W		

Table 147. LN1_CFG_9 register (address 19h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN1_S[4:0]	R/W		

Table 148. LN1_CFG_10 register (address 1Ah) bit description

Bit	Symbol	Access	Value	Description
7 to 6	LN1_HD	R/W		
4 to 0	LN1_CF[4:0]	R/W		

Table 149. LN1_CFG_11 register (address 1Bh) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN1_RES1[7:0]	R/W		

Table 150. LN1_CFG_12 register (address 1Ch) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN1_RES2[7:0]	R/W		

Table 151. LN1_CFG_13 register (address 1Dh) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN1_FCHK[7:0]	R/W		

Table 152. PAGE_ADDRESS register (address 1Fh) bit description

Bit	Symbol	Access	Value	Description
2 to 0	PAGE	R/W	-	page_address

10.15.2.11 Page 7 allocation map description

Table 153. Page 7 register allocation map

Address		Register name	R/W	Bit definition								Default	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
0	00h	LN2_CFG_0	R	LN2_DID[7:0]								<tbd>	<tbd>
1	01h	LN2_CFG_1	R	-	-	-	-	LN2_BID[3:0]				<tbd>	<tbd>
2	02h	LN2_CFG_2	R	-	-	-	LN2_LID[4:0]					<tbd>	<tbd>
3	03h	LN2_CFG_3	R	LN2_SCR	-	-	LN2_L[4:0]					<tbd>	<tbd>
4	04h	LN2_CFG_4	R	LN2_F[7:0]								<tbd>	<tbd>
5	05h	LN2_CFG_5	R	-	-	-	LN2_K[4:0]					<tbd>	<tbd>
6	06h	LN2_CFG_6	R	LN2_M[7:0]								<tbd>	<tbd>
7	07h	LN2_CFG_7	R	LN2_CS[1:0]		-	LN2_N[4:0]					<tbd>	<tbd>
8	08h	LN2_CFG_8	R	-	-	-	LN2_N'[4:0]					<tbd>	<tbd>
9	09h	LN2_CFG_9	R	-	-	-	LN2_S[4:0]					<tbd>	<tbd>
10	0Ah	LN2_CFG_10	R	LN2_HD	-	-	LN2_CF[4:0]					<tbd>	<tbd>
11	0Bh	LN2_CFG_11	R	LN2_RES1[7:0]								<tbd>	<tbd>
12	0Ch	LN2_CFG_12	R	LN2_RES2[7:0]								<tbd>	<tbd>
13	0Dh	LN2_CFG_13	R	LN2_FCHK[7:0]								<tbd>	<tbd>
16	10h	LN3_CFG_0	R	LN3_DID[7:0]								<tbd>	<tbd>
17	11h	LN3_CFG_1	R	-	-	-	-	LN3_BID[3:0]				<tbd>	<tbd>
18	12h	LN3_CFG_2	R	-	-	-	LN3_LID[4:0]					<tbd>	<tbd>
19	13h	LN3_CFG_3	R	LN3_SCR	-	-	LN3_L[4:0]					<tbd>	<tbd>
20	14h	LN3_CFG_4	R	LN3_F[7:0]								<tbd>	<tbd>
21	15h	LN3_CFG_5	R	-	-	-	LN3_K[4:0]					<tbd>	<tbd>
22	16h	LN3_CFG_6	R	LN3_M[7:0]								<tbd>	<tbd>
23	17h	LN3_CFG_7	R	LN3_CS[1:0]		-	LN3_N[4:0]					<tbd>	<tbd>
24	18h	LN3_CFG_8	R	-	-	-	LN3_N'[4:0]					<tbd>	<tbd>
25	19h	LN3_CFG_9	R	-	-	-	LN3_S[4:0]					<tbd>	<tbd>
26	1Ah	LN3_CFG_10	R	LN3_HD	-	-	LN3_CF[4:0]					<tbd>	<tbd>
27	1Bh	LN3_CFG_11	R	LN3_RES1[7:0]								<tbd>	<tbd>

Table 153. Page 7 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
28	1Ch	LN3_CFG_12	R	LN3_RES2[7:0]								<tbd>	<tbd>
29	1Dh	LN3_CFG_13	R	LN3_FCHK[7:0]								<tbd>	<tbd>
31	1Fh	PAGE_ADDRESS	R/W	PAGE								<tbd>	<tbd>

10.15.2.12 Page 7 bit definition detailed description

Please refer to Table 153 for a register overview and their default values. In the following tables, all the values emphasized in bold are the default values.

Table 154. LN2_CFG_0 register (address 00h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	LN2_DID[7:0]	R/W		

Table 155. LN2_CFG_1 register (address 01h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
3 to 0	LN2_BID[3:0]	R/W		

Table 156. LN2_CFG_2 register (address 02h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
4 to 0	LN2_LID[4:0]	R/W		

Table 157. LN2_CFG_3 register (address 03h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	LN2_SCR	R/W		
4 to 0	LN2_L[4:0]	R/W		

Table 158. LN2_CFG_4 register (address 04h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN2_F[7:0]	R/W		

Table 159. LN2_CFG_5 register (address 05h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN2_K[4:0]	R/W		

Table 160. LN2_CFG_6 register (address 06h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN2_M[7:0]	R/W		

Table 161. LN2_CFG_7 register (address 07h) bit description

Bit	Symbol	Access	Value	Description
7 to 6	LN2_CS[1:0]	R/W		
4 to 0	LN2_N[4:0]	R/W		

Table 162. LN2_CFG_8 register (address 08h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN2_N'[4:0]	R/W		

Table 163. LN2_CFG_9 register (address 09h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN2_S[4:0]	R/W		

Table 164. LN2_CFG_10 register (address 0Ah) bit description

Bit	Symbol	Access	Value	Description
7	LN2_HD	R/W		
4 to 0	LN2_CF[4:0]	R/W		

Table 165. LN2_CFG_11 register (address 0Bh) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN2_RES1[7:0]	R/W		

Table 166. LN2_CFG_12 register (address 0Ch) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN2_RES2[7:0]	R/W		

Table 167. LN2_CFG_13 register (address 0Dh) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN2_FCHK[7:0]	R/W		

Table 168. LN3_CFG_0 register (address 10h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN3_DID[7:0]	R/W		

Table 169. LN3_CFG_1 register (address 11h) bit description

Bit	Symbol	Access	Value	Description
3 to 0	LN3_BID[3:0]	R/W		

Table 170. LN3_CFG_2 register (address 12h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN3_LID[4:0]	R/W		

Table 171. LN3_CFG_3 register (address 13h) bit description

Bit	Symbol	Access	Value	Description
7	LN3_SCR	R/W		
4 to 0	LN3_L[4:0]	R/W		

Table 172. LN3_CFG_4 register (address 14h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN3_F[7:0]	R/W		

Table 173. LN3_CFG_5 register (address 15h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN3_K[4:0]	R/W		

Table 174. LN3_CFG_6 register (address 16h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN3_M[7:0]	R/W		

Table 175. LN3_CFG_7 register (address 17h) bit description

Bit	Symbol	Access	Value	Description
7 to 6	LN3_CS[1:0]	R/W		
4 to 0	LN3_N[4:0]	R/W		

Table 176. LN3_CFG_8 register (address 18h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN3_N'[4:0]	R/W		

Table 177. LN3_CFG_9 register (address 19h) bit description

Bit	Symbol	Access	Value	Description
4 to 0	LN3_S[4:0]	R/W		

Table 178. LN3_CFG_10 register (address 1Ah) bit description

Bit	Symbol	Access	Value	Description
7	LN3_HD	R/W		
4 to 0	LN3_CF[4:0]	R/W		

Table 179. LN3_CFG_11 register (address 1Bh) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN3_RES1[7:0]	R/W		

Table 180. LN3_CFG_12 register (address 1Ch) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN3_RES2[7:0]	R/W		

Table 181. LN3_CFG_13 register (address 1Dh) bit description

Bit	Symbol	Access	Value	Description
7 to 0	LN3_FCHK[7:0]	R/W		

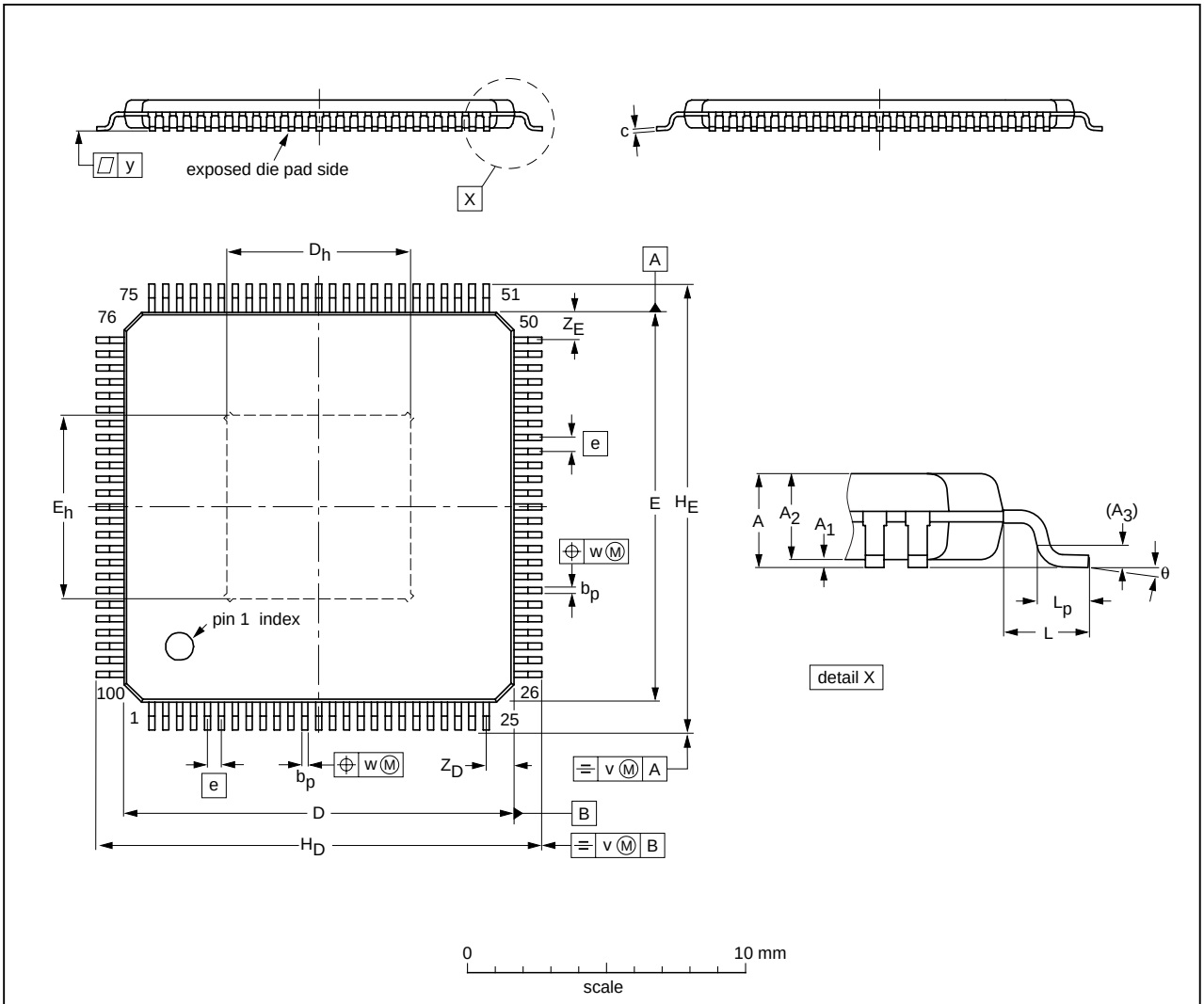
Table 182. PAGE_ADDRESS register (address 1Fh) bit description

Bit	Symbol	Access	Value	Description
2 to 0	PAGE	R/W	-	page_address

11. Package outline

HTQFP100: plastic thermal enhanced thin quad flat package; 100 leads; body 14 x 14 x 1 mm; exposed die pad

SOT638-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	14.1 13.9	7.1 6.1	14.1 13.9	7.1 6.1	0.5	16.15 15.85	16.15 15.85	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT638-1		MS-026				~~03-04-07~~ 05-02-02

Fig 22. Package outline SOT638 (HTQFP100)

12. Abbreviations

Table 183. Abbreviations

Acronym	Description
BW	Bandwidth
BWA	Broadband Wireless Access
CDMA	Code Division Multiple Access
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
EDGE	Enhanced Data rates for GSM Evolution
FIR	Finite Impulse Response
GSM	Global System for Mobile communications
IF	Intermediate Frequency
IMD3	Third Order Intermodulation Product
LMDS	Local Multipoint Distribution Service
LVDS	Low-voltage Differential Signaling
NCO	Numerically Controlled Oscillator
NMOS	Negative Metal-Oxide Semiconductor
PLL	Phase-Locked Loop
SERDES	Serializer/Deserializer
SFDR	Spurious Free Dynamic Range
SPI	Serial Peripheral Interface
WCDMA	Wideband Code Division Multiple Access
WLL	Wireless Local Loop

13. Revision history

Table 184. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
DAC1408D650_1	20090526	Objective data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

14.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

14.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

15. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

16. Tables

Table 1. Ordering information 2
Table 2. Pin description 5
Table 3. Limiting values 8
Table 4. Thermal characteristics 8
Table 5. Characteristics 9
Table 6. Digital Layer Processing Latency 15
Table 7. SYNC_OUT timing 17
Table 8. Read or Write mode access description 21
Table 9. Number of bytes to be transferred 21
Table 10. SPI timing characteristics 22
Table 11. Interpolation filter coefficients 24
Table 12. Inversion filter coefficients 26
Table 13. DAC transfer function 26
Table 14. $I_{O(fs)}$ coarse adjustment 28
Table 15. $I_{O(fs)}$ fine adjustment 28
Table 16. Digital offset adjustment 29
Table 17. Auxiliary DAC transfer function 30
Table 18. Page 0 register allocation map 36
Table 19. COMMON register (address 00h) bit description 37
Table 20. TXCFG register (address 01h) bit description 38
Table 21. PLLCFG register (address 02h) bit description 39
Table 22. FREQNCO_LSB register (address 03h) bit description 39
Table 23. FREQNCO_LISB register (address 04h) bit description 39
Table 24. FREQNCO_UISB register (address 05h) bit description 39
Table 25. FREQNCO_MSB register (address 06h) bit description 39
Table 26. PHINCO_LSB register (address 07h) bit description 39
Table 27. PHINCO_MSB register (address 08h) bit description 40
Table 28. DAC_A_CFG_1 register (address 09h) bit description 40
Table 29. DAC_A_CFG_2 register (address 0Ah) bit description 40
Table 30. DAC_A_CFG_3 register (address 0Bh) bit description 40
Table 31. DAC_B_CFG_1 register (address 0Ch) bit description 40
Table 32. DAC_B_CFG_2 register (address 0Dh) bit description 40
Table 33. DAC_B_CFG_3 register (address 0Eh) bit description 41
Table 34. DAC_CFG register (address 0Fh) bit description 41
Table 35. DAC_A_Aux_MSB register (address 1Ah) bit description 41
Table 36. DAC_A_Aux_LSB register (address 1Bh) bit description 41
Table 37. DAC_B_Aux_MSB register (address 1Ch) bit description 41
Table 38. DAC_B_Aux_LSB register (address 1Dh) bit description 41
Table 39. Page 2 register allocation map 42
Table 40. MAINCONTROL register (address 00h) bit description 44
Table 41. MAN_PON register (address 01h) bit description 44
Table 42. MAN_SUPD register (address 02h) bit description 45
Table 43. RST_EXT_FCLK register (address 04h) bit description 45
Table 44. RST_EXT_DCLK register (address 05h) bit description 45
Table 45. DCSMU_PREDIVCNT register (address 06h) bit description 45
Table 46. PLL_CHARGETIME register (address 07h) bit description 45
Table 47. PLL_RUN_IN_TIME register (address 08h) bit description 45
Table 48. CA_RUN_IN_TIME register (address 09h) bit description 45
Table 49. IQ_LEVEL_CNTRL register (address 0Ah) bit description 46
Table 50. IQ_DC_LEVEL_LSB register (address 0Bh) bit description 46
Table 51. SET_ICHP_PD1 register (address 10h) bit description 46
Table 52. SET_ICHP_PD2 register (address 11h) bit description 46
Table 53. SET_ICHP_PFD register (address 12h) bit description 46
Table 54. SET_RATIO_PD1 register (address 13h) bit description 46
Table 55. SET_RATIO_PD2 (address 14h) bit description 46
Table 56. SET_RATIO_PFD register (address 15h) bit description 47
Table 57. SET_VCM_VOLTAGE register (address 16h) bit description 47
Table 58. SET_SYNC register (address 17h)

continued >>

bit description 47
Table 59. MISC_CNTRLS register (address 1Ah) bit description 47
Table 60. IO_MUX_CNTRL0 register (address 1Bh) bit description 48
Table 61. IO_MUX_CNTRL1 register (address 1Ch) bit description 48
Table 62. DIG_VERSION register (address 1Dh) bit description 49
Table 63. JRX_ANA_VERSION register (address 1Eh) bit description 49
Table 64. PAGE_ADDRESS register (address 1Fh) bit description 49
Table 65. Page 4 register allocation map 50
Table 66. SR_DLP_0 register (address 00h) bit description 52
Table 67. SR_DLP_1 register (address 01h) bit description 52
Table 68. FORCE_LOCK register (address 02h) bit description 52
Table 69. MAN_LOCK_LN_1_0 register (address 03h) bit description 53
Table 70. MAN_LOCK_2_0 register (address 04h) bit description 53
Table 71. CA_CNTRL register (address 05h) bit description 53
Table 72. SCR-CNTRL register (address 06h) bit description 54
Table 73. ILA_CNTRL register (address 07h) bit description 55
Table 74. FORCE_ALIGN register (address 08h) bit description 55
Table 75. MAN_ALIGN_LN_0_1 register (address 09h) bit description 55
Table 76. MAN_ALIGN_LN_0_1 register (address 0Ah) bit description 55
Table 77. FA_ERR_HANDLING register (address 0Bh) bit description 56
Table 78. SYNCOUT_MODE register (address 0Ch) bit description 57
Table 79. LANE_POLARITY register (address 1Dh) bit description 57
Table 80. LANE_SELECT register (address 0Eh) bit description 58
Table 81. SOFT_RESET_SCRAMBLER register (address 10h) bit description 58
Table 82. INIT_SCR_S15T8_LN0 register (address 11h) bit description 58
Table 83. INIT_SCR_S7T1_LN0 (address 12h) bit description 59
Table 84. INIT_SCR_S15T8_LN1 register (address 13h) bit description 59
Table 85. INIT_SCR_S7T1_LN1 register (address 14h) bit description 59
Table 86. INIT_SCR_S15T8_LN2 register (address 15h) bit description 59
Table 87. INIT_SCR_S7T1_LN2 register (address 16h) bit description 59
Table 88. INIT_SCR_S15T8_LN3 register (address 17h) bit description 59
Table 89. INIT_SCR_S7T1_LN3 register (address 18h) bit description 59
Table 90. INIT_ILA_BUFPTR_LN01 register (address 19h) bit description 59
Table 91. INIT_ILA_BUFPTR_LN23 register (address 1Ah) bit description 59
Table 92. ERROR_HANDLING register (address 1Bh) bit description 60
Table 93. PAGE_ADDRESS register (address 1Fh) bit description 60
Table 94. Page 5 register allocation map 61
Table 95. ILA_MON_1_0 register (address 00h) bit description 63
Table 96. ILA_MON_3_2 register (address 01h) bit description 63
Table 97. ILA_BUF_ERR register (address 02h) bit description 63
Table 98. CA_MON register (address 03h) bit description 63
Table 99. DEC_FLAGS register (address 04h) bit description 64
Table 100. KOUT_FLAG register (address 05h) bit description 64
Table 101. K28_LN0_FLAG register (address 06h) bit description 64
Table 102. K28_LN1_FLAG register (address 07h) bit description 64
Table 103. K28_LN2_FLAG register (address 08h) bit description 64
Table 104. K28_LN3_FLAG register (address 09h) bit description 65
Table 105. LOCK_CNT_MON_LN01 register (address 0Ah) bit description 65
Table 106. ILA_MON_3_2 register (address 0Bh) bit description 65
Table 107. LOCK_CNT_MON_LN23 register (address 0Ch) bit description 65
Table 108. FLAG_CNT_LSB_LN0 register (address 10h) bit description 65
Table 109. FLAG_CNT_MSB_LN0 register (address 11h) bit description 65
Table 110. FLAG_CNT_LSB_LN1 register

continued >>

(address 12h) bit description 65
Table 111. FLAG_CNT_MSB_LN1 register (address 13h) bit description 65
Table 112. FLAG_CNT_LSB_LN2 register (address 14h) bit description 66
Table 113. FLAG_CNT_MSB_LN2 register (address 15h) bit description 66
Table 114. FLAG_CNT_LSB_LN3 register (address 16h) bit description 66
Table 115. FLAG_CNT_MSB_LN3 register (address 17h) bit description 66
Table 116. BER_LEVEL register (address 19h) bit description 66
Table 117. INTR_ENA register (address 1Ah) bit description 66
Table 118. CNTRL_FLAGCNT_LN01 register (address 1Bh) bit description 67
Table 119. CNTRL_FLAGCNT_LN23 register (address 1Ch) bit description 67
Table 120. MON_FLAGS_RESET register (address 1Dh) bit description 67
Table 121. DBG_CNTRL register (address 1Eh) bit description 68
Table 122. PAGE_ADDRESS register (address 1Fh) bit description 68
Table 123. Page 6 register allocation map 69
Table 124. LN0_CFG_0 register (address 00h) bit description 71
Table 125. LN0_CFG_1 register (address 01h) bit description 71
Table 126. LN0_CFG_2 register (address 02h) bit description 71
Table 127. LN0_CFG_3 register (address 03h) bit description 71
Table 128. LN0_CFG_4 register (address 04h) bit description 71
Table 129. LN0_CFG_5 register (address 05h) bit description 71
Table 130. LN0_CFG_6 register (address 06h) bit description 71
Table 131. LN0_CFG_7 register (address 07h) bit description 71
Table 132. LN0_CFG_8 register (address 08h) bit description 71
Table 133. LN0_CFG_9 register (address 09h) bit description 72
Table 134. LN0_CFG_10 register (address 0Ah) bit description 72
Table 135. LN0_CFG_11 register (address 0Bh) bit description 72
Table 136. LN0_CFG_12 register (address 0Ch) bit description 72
Table 137. LN0_CFG_13 register (address 0Dh) bit description 72
Table 138. LN1_CFG_0 register (address 10h) bit description 72
Table 139. LN1_CFG_1 register (address 11h) bit description 72
Table 140. LN1_CFG_2 register (address 12h) bit description 72
Table 141. LN1_CFG_3 register (address 13h) bit description 72
Table 142. LN1_CFG_4 register (address 14h) bit description 72
Table 143. LN1_CFG_5 register (address 15h) bit description 72
Table 144. LN1_CFG_6 register (address 16h) bit description 73
Table 145. LN1_CFG_7 register (address 17h) bit description 73
Table 146. LN1_CFG_8 register (address 18h) bit description 73
Table 147. LN1_CFG_9 register (address 19h) bit description 73
Table 148. LN1_CFG_10 register (address 1Ah) bit description 73
Table 149. LN1_CFG_11 register (address 1Bh) bit description 73
Table 150. LN1_CFG_12 register (address 1Ch) bit description 73
Table 151. LN1_CFG_13 register (address 1Dh) bit description 73
Table 152. PAGE_ADDRESS register (address 1Fh) bit description 73
Table 153. Page 7 register allocation map 74
Table 154. LN2_CFG_0 register (address 00h) bit description 76
Table 155. LN2_CFG_1 register (address 01h) bit description 76
Table 156. LN2_CFG_2 register (address 02h) bit description 76
Table 157. LN2_CFG_3 register (address 03h) bit description 76
Table 158. LN2_CFG_4 register (address 04h) bit description 76
Table 159. LN2_CFG_5 register (address 05h) bit description 76
Table 160. LN2_CFG_6 register (address 06h) bit description 76
Table 161. LN2_CFG_7 register (address 07h) bit description 76
Table 162. LN2_CFG_8 register (address 08h)

continued >>

bit description 76
Table 163. LN2_CFG_9 register (address 09h)
bit description 77
Table 164. LN2_CFG_10 register (address 0Ah)
bit description 77
Table 165. LN2_CFG_11 register (address 0Bh)
bit description 77
Table 166. LN2_CFG_12 register (address 0Ch)
bit description 77
Table 167. LN2_CFG_13 register (address 0Dh)
bit description 77
Table 168. LN3_CFG_0 register (address 10h)
bit description 77
Table 169. LN3_CFG_1 register (address 11h)
bit description 77
Table 170. LN3_CFG_2 register (address 12h)
bit description 77
Table 171. LN3_CFG_3 register (address 13h)
bit description 77
Table 172. LN3_CFG_4 register (address 14h)
bit description 77
Table 173. LN3_CFG_5 register (address 15h)
bit description 77
Table 174. LN3_CFG_6 register (address 16h)
bit description 78
Table 175. LN3_CFG_7 register (address 17h)
bit description 78
Table 176. LN3_CFG_8 register (address 18h)
bit description 78
Table 177. LN3_CFG_9 register (address 19h)
bit description 78
Table 178. LN3_CFG_10 register (address 1Ah)
bit description 78
Table 179. LN3_CFG_11 register (address 1Bh)
bit description 78
Table 180. LN3_CFG_12 register (address 1Ch)
bit description 78
Table 181. LN3_CFG_13 register (address 1Dh)
bit description 78
Table 182. PAGE_ADDRESS register (address 1Fh)
bit description 78
Table 183. Abbreviations 80
Table 184. Revision history 81

17. Figures

Fig 1. Block diagram 3
Fig 2. Pin configuration 4
Fig 3. JESD204A receiver 15
Fig 4. Lane input termination 16
Fig 5. DC coupling 16
Fig 6. AC coupling 16
Fig 7. SYNC_OUT timing 17
Fig 8. Frame assembly 20
Fig 9. SPI protocol 21
Fig 10. SPI timing diagram 22
Fig 11. LVDS clock configuration 23
Fig 12. Interfacing CML to LVDS 23
Fig 13. Internal reference configuration 27
Fig 14. Equivalent analog output circuit (one DAC) 29
Fig 15. 1 $V_{o(p-p)}$ differential output with transformer 31
Fig 16. 2 $V_{o(p-p)}$ differential output with transformer 31
Fig 17. An example of a DC interface to a 1.7 $V_{i(cm)}$ AQM 32
Fig 18. An example of a DC interface to a 3.3 $V_{i(cm)}$ AQM 32
Fig 19. An example of a DC interface to a 1.7 $V_{i(cm)}$ AQM when using auxiliary DACs 33
Fig 20. An example of a DC interface to a 3.3 $V_{i(cm)}$ AQM when using auxiliary DACs 33
Fig 21. An example of an AC interface to a 0.5 $V_{i(cm)}$ AQM when using auxiliary DACs 34
Fig 22. Package outline SOT638 (HTQFP100) 79

18. Contents

1 General description 1
2 Features 1
3 Applications 2
4 Ordering information 2
5 Block diagram 3
6 Pinning information 4
6.1 Pinning 4
6.2 Pin description 5
7 Limiting values 8
8 Thermal characteristics 8
9 Characteristics 9
10 Application information 14
10.1 General description 14
10.2 JESD204A receiver 15
10.2.1 Lane input 15
10.2.2 Sync & word align 16
10.2.3 K detect & word align 17
10.2.4 Descrambler 18
10.2.5 Inter lane alignment 18
10.2.6 Frame assembly 19
10.3 Serial interface (SPI) 20
10.3.1 Protocol description 20
10.3.2 SPI timing description 21
10.4 Clock inputs 23
10.5 FIR Filters 24
10.6 Quadrature modulator and Numerically Controlled Oscillator (NCO) 25
10.6.1 NCO in 32-bit 25
10.6.2 Low-power NCO 25
10.6.3 Minus 3dB 25
10.7 x / (sin x) 25
10.8 DAC transfer function 26
10.9 Full-scale current 27
10.9.1 Regulation 27
10.9.1.1 External regulation 27
10.9.2 Full-scale current adjustment 27
10.10 Digital offset adjustment 28
10.11 Analog output 29
10.12 Auxiliary DACs 30
10.13 Output configuration 31
10.13.1 Basic output configuration 31
10.13.2 DC interface to an Analog Quadrature Modulator (AQM) 32
10.13.3 AC interface to an Analog Quadrature Modulator (AQM) 34
10.14 Power and grounding 34
10.15 Configuration interface 35
10.15.1 Register description 35
10.15.2 Detailed descriptions of registers 35
10.15.2.1 Page 0 allocation map description 36
10.15.2.2 Page 0 bit definition detailed description 37
10.15.2.3 Page 2 allocation map description 42
10.15.2.4 Page 2 bit definition detailed description 44
10.15.2.5 Page 4 allocation map description 50
10.15.2.6 Page 4 bit definition detailed description 52
10.15.2.7 Page 5 allocation map description 61
10.15.2.8 Page 5 bit definition detailed description 63
10.15.2.9 Page 6 allocation map description 69
10.15.2.10 Page 6 bit definition detailed description 71
10.15.2.11 Page 7 allocation map description 74
10.15.2.12 Page 7 bit definition detailed description 76
11 Package outline 79
12 Abbreviations 80
13 Revision history 81
14 Legal information 82
14.1 Data sheet status 82
14.2 Definitions 82
14.3 Disclaimers 82
14.4 Trademarks 82
15 Contact information 82
16 Tables 83
17 Figures 87
18 Contents 88

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 26 May 2009
Document identifier: DAC1408D650_1