National Semiconductor

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DAC1054 Quad 10-Bit Voltage-Output Serial D/A Converter with Readback

General Description

The DAC1054 is a complete quad 10-bit voltage-output digital-to-analog converter that can operate on a single 5V supply. It includes on-chip output amplifiers, internal voltage reference, and serial microprocessor interface. By combining in one package the reference, amplifiers, and conversion circuitry for four D/A converters, the DAC1054 minimizes wiring and parts count and is hence ideally suited for applications where cost and board space are of prime concern.

The DAC1054 also has a data readback function, which can be used by the microprocessor to verify that the desired input word has been properly latched into the DAC1054's data registers. The data readback function simplifies the design and reduces the cost of systems which need to verify data integrity.

The logic comprises a MICROWIRE™-compatible serial interface and control circuitry. The interface allows the user to write to any one of the input registers or to all four at once. The latching registers are double-buffered, consisting of 4 separate input registers and 4 DAC registers. Each DAC register may be written to individually. Double buffering allows all 4 DAC outputs to be updated simultaneously or individually.

The four reference inputs allow the user to configure the system to have a separate output voltage range for each DAC. The output voltage of each DAC can range between 0.3V and 2.8V and is a function of V_{BIAS}, V_{REF}, and the input word.

Features

- Single +5V supply operation
- MICROWIRE serial interface allows easy interface to many popular microcontrollers including the COPS™ and HPC™ families of microcontrollers
- Data readback capability
- Output data can be formatted to read back MSB or LSB first
- Versatile logic allows selective or global update of the DACs
- Power fail flag
- Output amplifiers can drive 2 kΩ load
- Synchronous/asynchronous update of the DAC outputs

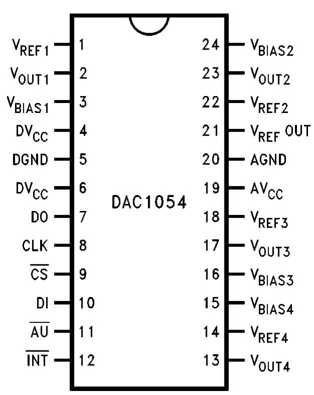
Key Specifications

Guaranteed monotonic over temperature	
Integral linearity error	±3/4 LSB max
Output settling time	3.7 µs max
Analog output voltage range	0.3V to 2.8V
Supply voltage range	4.5V to 5.5V
Clock frequency for write	10 MHz max
Clock frequency for read back	5 MHz max
Power dissipation (f_{CLK} = 10 MHz)	100 mW max
On-board reference	2.65V ±2% max

Applications

- Automatic test equipment
- Industrial process controls
- Automotive controls and diagnostics
- Instrumentation

Connection Diagram



TL/H/11437–1

Top View

Ordering Information

Industrial (−40°C < T_A < +85°C)	Package
DAC1054CIN	N24A Molded DIP
DAC1054CIWM	M24B Small Outline
Military (−55°C < T_A < +125°C)	
DAC1054CMJ/883 or 5962-9466201MJA	J24A Ceramic DIP

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RRD-B30M75/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (AV_{CC}, DV_{CC})	7V
Supply Voltage Difference (AV_{CC}−DV_{CC})	±5.5V
Voltage at Any Pin (Note 3)	GND −0.3V to AV_{CC}/DV_{CC} +0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 4)	30 mA
Power Dissipation (Note 5)	950 mW
ESD Susceptibility (Note 6)	
Human Body Model	2000V
Machine Model	200V
Soldering Information	
N Package (10 sec.)	260°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.) (Note 7)	220°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 1 & 2)

Supply Voltage	4.5V to 5.5V
Supply Voltage Difference (AV_{CC} − DV_{CC})	±1V
Temperature Range	$T_{MIN} < T_A < T_{MAX}$
DAC1054CIN, DAC1054CIWM	$-40°C < T_A < 85°C$
DAC1054CMJ/883	$-55°C < T_A < 125°C$

Converter Electrical Characteristics

The following specifications apply for $AV_{CC} = DV_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.4V$, $R_L = 2\ k\Omega$ (R_L is the load resistor on the analog outputs – pins 2, 13, 17, and 23) and $f_{CLK} = 10$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX}.** All other limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 8)	Limit (Note 9)	Units (Limits)
STATIC CHARACTERISTICS					
n	Resolution		10	**10**	bits
	Monotonicity	(Note 10)	10	**10**	bits
	Integral Linearity Error DAC1054CIN, DAC1054CIWM	(Note 11)		**±0.75**	LSB (max)
	Differential Linearity Error			**±1.0**	LSB (max)
	Fullscale Error	(Note 12)		**±30**	mV
	Fullscale Error Tempco	(Note 13)	−38		ppm/°C
	Zero Error	(Note 14)		**±25**	mV
	Zero Error Tempco	(Note 13)	−38		ppm/°C
	Power Supply Sensitivity	(Note 15)		**−34**	dB (max)
DYNAMIC CHARACTERISTICS					
t_{s+}	Positive Voltage Output Settling Time	(Note 16) $C_L = 200$ pF	1.8	**3.2**	µs
t_{s-}	Negative Voltage Output Settling Time	(Note 16) $C_L = 200$ pF	2.3	**3.7**	µs
	Digital Crosstalk	(Note 17)	15		mV_{p-p}
	Digital Feedthrough	(Note 18)	15		mV_{p-p}
	Clock Feedthrough	(Note 19)	20		mV_{p-p}
	Channel-to-Channel Isolation	(Note 20)	−71		dB
	Glitch Energy	(Note 21)	7		nV−s
	Peak Value of Largest Glitch		38		mV
PSRR	Power Supply Rejection Ratio	(Note 22)	−49		dB

Converter Electrical Characteristics (Continued)

The following specifications apply for $AV_{CC} = DV_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.4V$, $R_L = 2\ k\Omega$ (R_L is the load resistor on the analog outputs – pins 2, 13, 17, and 23) and $f_{CLK} = 10$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX}.** All other limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units (Limits)
DIGITAL AND DC ELECTRICAL CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	$AV_{CC} = DV_{CC} = 5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$AV_{CC} = DV_{CC} = 4.5V$		**0.8**	V (max)
I_{IL}	Digital Input Leakage Current			**1**	µA (max)
C_{IN}	Input Capacitance		4		pF
C_{OUT}	Output Capacitance		5		pF
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_{SOURCE} = 0.8$ mA		**2.4**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_{SINK} = 3.2$ mA		**0.4**	V (max)
V_{INT}	Interrupt Pin Output Voltage	10 kΩ Pullup		**0.4**	V (max)
I_S	Supply Current	Outputs Unloaded	14	**20**	mA
REFERENCE INPUT CHARACTERISTICS					
V_{REF}	Input Voltage Range		0–2.75		V
R_{REF}	Input Resistance		7	**4** **9**	kΩ (min) kΩ (max)
C_{REF}	Input Capacitance	Full-Scale Data Input	25		pF
V_{BIAS} INPUT CHARACTERISTICS					
V_{BIAS}	V_{BIAS} Input Voltage Range		0.3–1.4		V
	Input Leakage		1		µA
C_{BIAS}	Input Capacitance		9		pF
BANDGAP REFERENCE CHARACTERISTICS ($C_L = 220\mu F$)					
$V_{REF}OUT$	Output Voltage			**2.65 ± 2%**	V
$\Delta V_{REF}/\Delta T$	Tempco	(Note 23)	29		ppm/°C
	Line Regulation	$4.5V < V_{CC} < 5.5V$, $I_L = 4$ mA		**5**	mV
$\Delta V_{REF}/\Delta I_L$	Load Regulation	$0 < I_L < 4$ mA $-1 < I_L < 0$ mA	 2.5	**10**	mV mV
I_{SC}	Short Circuit Current	$V_{REF}OUT = 0V$	12		mA
AC ELECTRICAL CHARACTERISTICS					
t_{DS}	Data Setup Time			**15**	ns (min)
t_{DH}	Data Hold Time			**0**	ns (min)
t_{CS}	Control Setup Time			**15**	ns (min)
t_{CH}	Control Hold Time			**0**	ns (min)
f_{WMAX}	Clock Frequency Write			**10**	MHz (max)
f_{RMAX}	Clock Frequency Readback			**5**	MHz (max)
t_H	Minimum Clock High Time			**20**	ns (min)
t_L	Minimum Clock Low Time			**20**	ns (min)

Converter Electrical Characteristics (Continued)

The following specifications apply for $AV_{CC} = DV_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.4V$, $R_L = 2\ k\Omega$ (R_L is the load resistor on the analog outputs − pins 2, 13, 17, and 23) and $f_{CLK} = 10$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX}.** All other limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units (Limits)
AC ELECTRICAL CHARACTERISTICS (Continued)					
t_{CZ1}	Output Hi-Z to Valid 1	$f_{CLK} = 5$ MHz		**70**	ns (max)
t_{CZ0}	Output Hi-Z to Valid 0	$f_{CLK} = 5$ MHz		**70**	ns (max)
t_{1H}	$\overline{CS}$ to Output Hi-Z	10 kΩ with 60 pF, $f_{CLK} = 5$ MHz		**150**	ns (max)
t_{0H}	$\overline{CS}$ to Output Hi-Z	10 kΩ with 60 pF, $f_{CLK} = 5$ MHz		**130**	ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Converter Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to ground, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < GND or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less.

Note 4: The sum of the currents at all pins that are driven beyond the power supply voltages should not exceed 30 mA.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), Θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. The table below details T_{Jmax} and Θ_{JA} for the various packages and versions of the DAC1054.

Part Number	T_{Jmax} (°C)	Θ_{JA} (°C/W)
DAC1054CIN	125	42
DAC1054CIWM	125	57

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: See AN450 "Surface Mounting Methods and Their Effect on Production Reliability" of the section titled "Surface Mount" found in any current Linear Databook for other methods of soldering surface mount devices.

Note 8: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 9: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: A monotonicity of 10 bits for the DAC1054 means that the output voltage changes in the same direction (or remains constant) for each increase in the input code.

Note 11: Integral linearity error is the maximum deviation of the output from the line drawn between zero and full-scale (excluding the effects of zero error and full-scale error).

Note 12: Full-scale error is measured as the deviation from the ideal 2.800V full-scale output when $V_{REF} = 2.650V$ and $V_{BIAS} = 1.400V$.

Note 13: Full-scale error tempco and zero error tempco are defined by the following equation:

$$\text{Error tempco} = \left[\frac{\text{Error}(T_{MAX}) - \text{Error}(T_{MIN})}{V_{SPAN}}\right]\left[\frac{10^6}{T_{MAX} - T_{MIN}}\right]$$

where Error (T_{MAX}) is the zero error or full-scale error at T_{MAX} (in volts), and Error (T_{MIN}) is the zero error or full-scale error at T_{MIN} (in volts); V_{SPAN} is the output voltage span of the DAC1054, which depends on V_{BIAS} and V_{REF}.

Note 14: Zero error is measured as the deviation from the ideal 0.302V output when $V_{REF} = 2.650V$, $V_{BIAS} = 1.400V$, and the digital input word is all zeros.

Note 15: Power Supply Sensitivity is the maximum change in the offset error or the full-scale error when the power supply differs from its optimum 5V by up to 0.50V (10%). The load resistor $R_L = 2\ k\Omega$.

Note 16: Positive or negative settling time is defined as the time taken for the output of the DAC to settle to its final full-scale or zero output to within ±0.5 LSB. This time shall be referenced to the 50% point of the positive edge of $\overline{CS}$, which initiates the update of the analog outputs.

Note 17: Digital crosstalk is the glitch measured on the output of one DAC while applying an all 0s to all 1s transition at the input of the other DACs.

Note 18: All DACs have full-scale outputs latched and DI is clocked with no update of the DAC outputs. The glitch is then measured on the DAC outputs.

Note 19: Clock feedthrough is measured for each DAC with its output at full-scale. The serial clock is then applied to the DAC at a frequency of 10 MHz and the glitch on each DAC full-scale output is measured.

Note 20: Channel-to-channel isolation is a measure of the effect of a change in one DAC's output on the output of another DAC. The V_{REF} of the first DAC is varied between 1.4V and 2.65V at a frequency of 15 kHz while the change in full-scale output of the second DAC is measured. The first DAC is loaded with all 0s.

Note 21: Glitch energy is the difference between the positive and negative glitch areas at the output of the DAC when a 1 LSB digital input code change is applied to the input. The glitch energy will have its largest value at one of the three major transitions. The peak value of the maximum glitch is separately specified.

Note 22: Power Supply Rejection Ratio is measured by varying $AV_{CC} = DV_{CC}$ between 4.50V and 5.50V with a frequency of 10 kHz and measuring the proportion of this signal imposed on a full-scale output of the DAC under consideration.

Note 23: The bandgap reference tempco is defined by the largest value from the following equations:

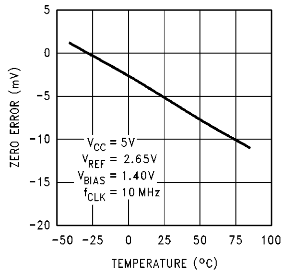
$$\text{Tempco}(T_{MAX}) = \left[\frac{V_{REF}(T_{MAX}) - V_{REF}(T_{ROOM})}{V_{REF}(T_{ROOM})}\right]\left[\frac{10^6}{T_{MAX} - T_{ROOM}}\right] \text{ or } \text{Tempco}(T_{MIN}) = \left[\frac{V_{REF}(T_{MIN}) - V_{REF}(T_{ROOM})}{V_{REF}(T_{ROOM})}\right]\left[\frac{10^6}{T_{ROOM} - T_{MIN}}\right]$$

where $T_{ROOM} = 25°C$, $V_{REF}(T_{MAX})$ is the reference output at T_{MAX}, and similarly for $V_{REF}(T_{MIN})$ and $V_{REF}(T_{ROOM})$.

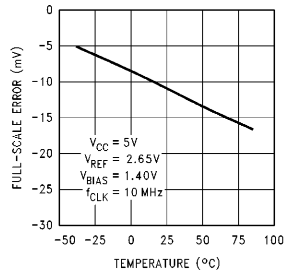
Note 24: A Military RETS specification is available upon request.

Typical Converter Performance Characteristics

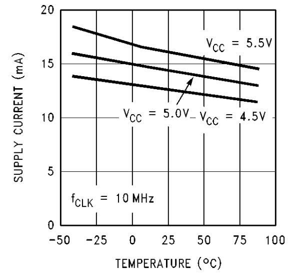
Zero Error vs Temperature



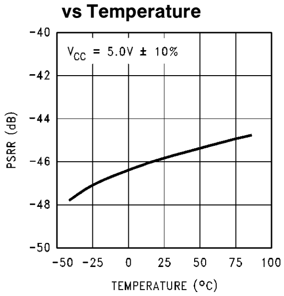
Full-Scale Error vs Temperature



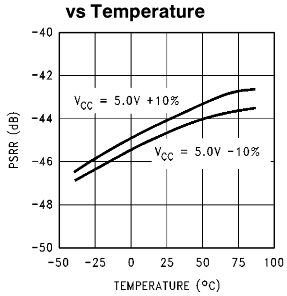
Supply Current vs Temperature



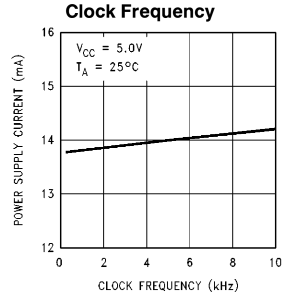
Zero Error PSRR vs Temperature



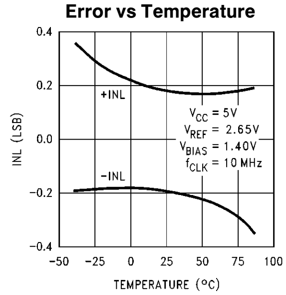
Full-Scale Error PSRR vs Temperature



Supply Current vs Clock Frequency



Integral Non-Linearity Error vs Temperature



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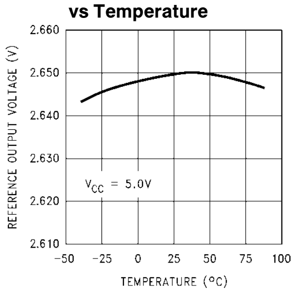
Typical Reference Performance Characteristics

Bandgap Voltage vs Temperature



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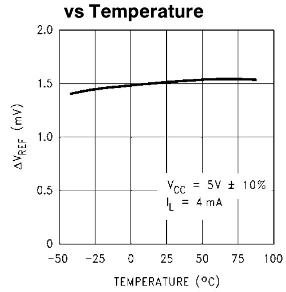
Line Regulation vs Temperature



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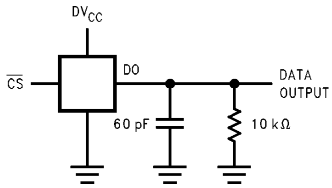
TRI-STATE Test Circuits and Waveforms



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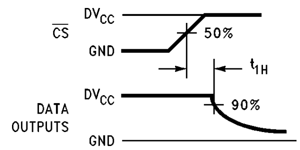

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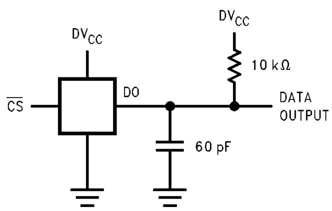

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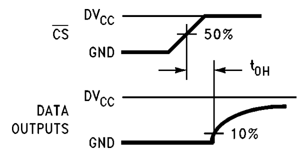

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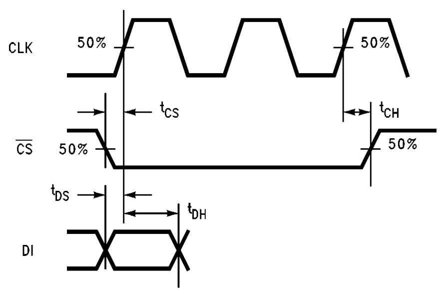
Timing Waveforms

Data Input Timing



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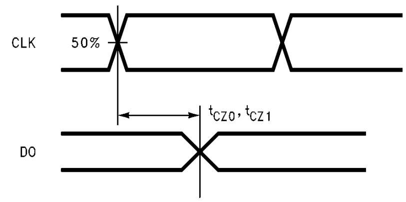
Data Output Timing



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Timing Diagrams

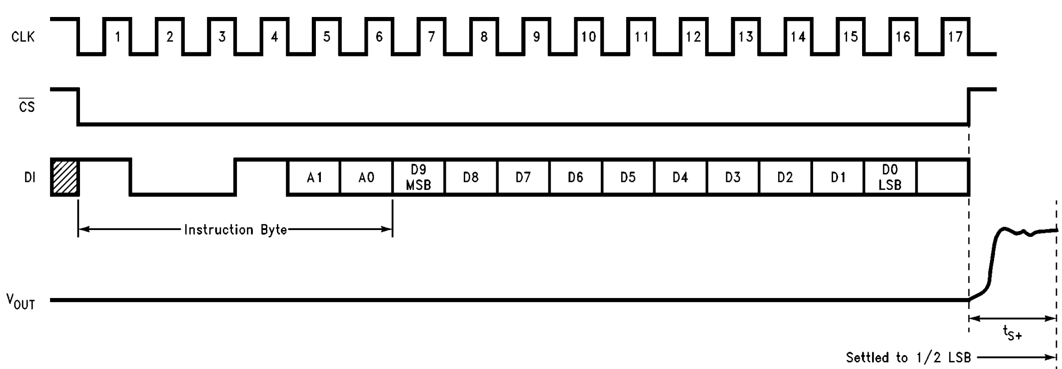

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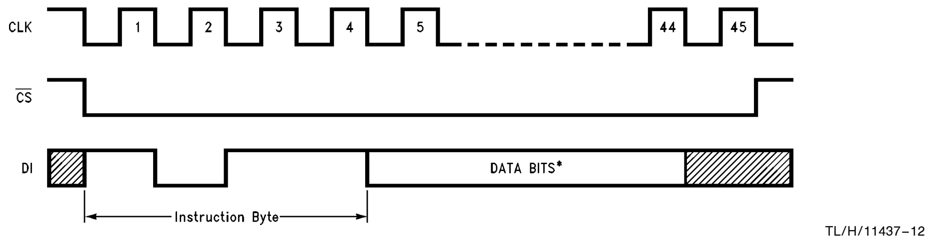
FIGURE 1. Write to One DAC with Update of Output ($\overline{AU}$ = 1), 10 MHz Maximum CLK Rate

Timing Diagrams (Continued)



* DACs are written to MSB first.
DAC1 is written to first, then DACs 2, 3, and 4.

FIGURE 2. Write to All DACs with Update of Outputs ($\overline{AU}$ = 1), 10 MHz Maximum CLK Rate

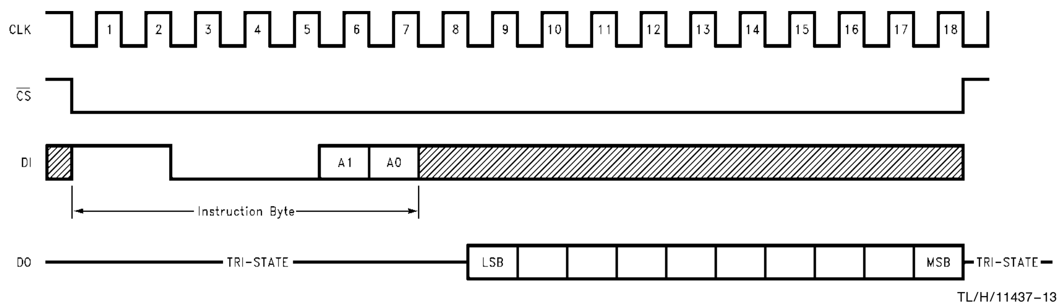
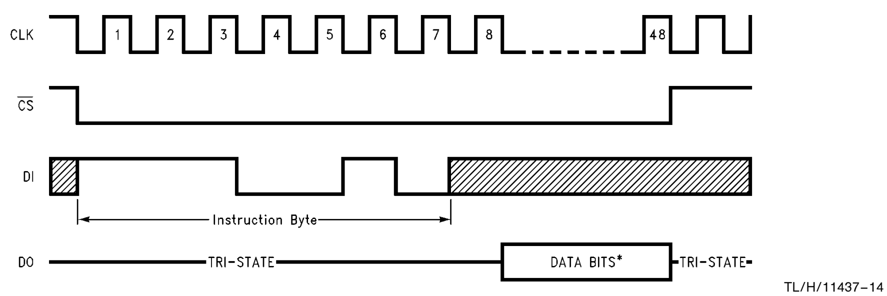


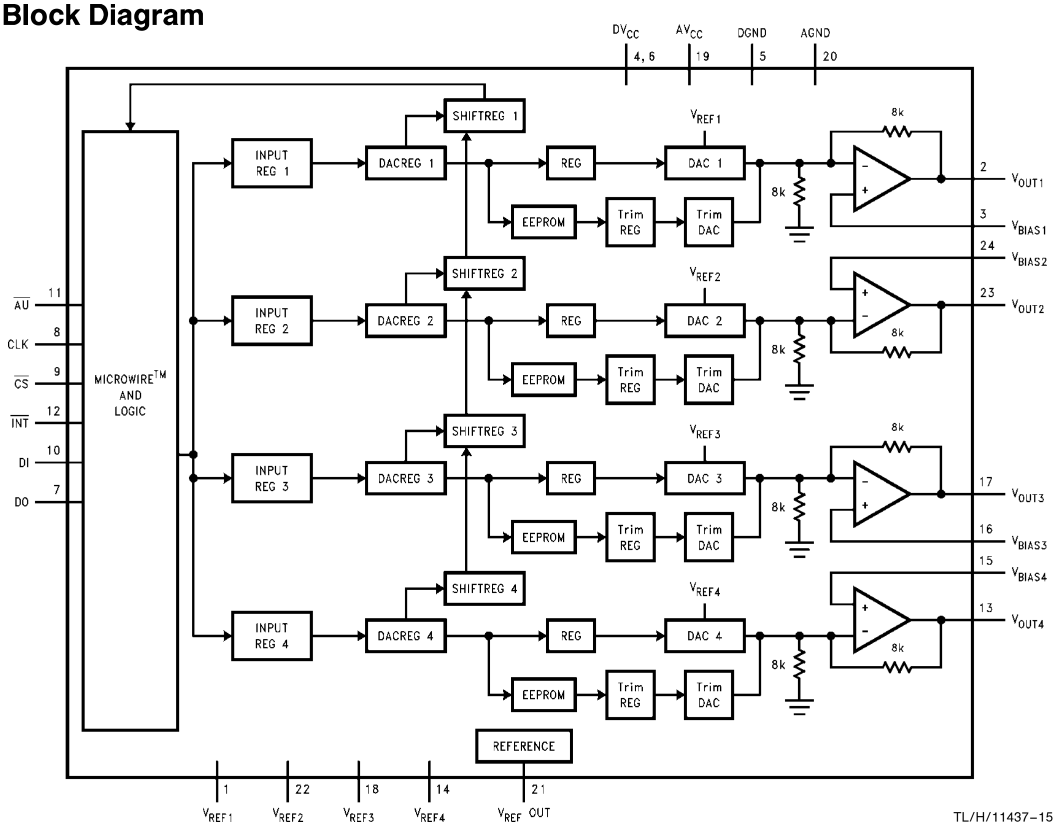
FIGURE 3. Read One DAC, DO LSB First, DO Changes on Falling Edge of CLK ($\overline{AU}$ = 1), 5 MHz Maximum CLK Rate



*DAC1 is read first, then DACs 2, 3, and 4.

FIGURE 4. Read All DACs, DO LSB First, DO Changes on Falling Edge of CLK ($\overline{AU}$ = 1), 5 MHz Maximum CLK Rate

Block Diagram



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Pin Description

V_{OUT1}(2), V_{OUT2}(23), V_{OUT3}(17), V_{OUT4}(13)	The voltage output connections of the four DACS. These provide output voltages in the range 0.3V–2.8V.
V_{REF}OUT(21)	The internal voltage reference output. The output of the reference is 2.65V ±2%.
V_{BIAS1}(3), V_{BIAS2}(24), V_{BIAS3}(16), V_{BIAS4}(15)	The non-inverting inputs of the 4 output amplifiers. These pins set the virtual ground voltage for the respective DACs. The allowed range is 0.3V–1.4V.
AGND(20), DGND(5)	The analog and digital ground pins.
DV_{CC}(4, 6), AV_{CC}(19)	The digital and analog power supply pins. The power supply range of the DAC1054 is 4.5V–5.5V. To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} pins be bypassed separately with bypass capacitors of 10 μF tantalum in parallel with 0.1 μF ceramic.
$\overline{AU}$(11)	When this pin is taken low, all DAC outputs will be asynchronously updated. $\overline{CS}$ must be held high during the update. $\overline{AU}$ must be held high during Read back.
V_{REF1}(1), V_{REF2}(22), V_{REF3}(18), V_{REF4}(14)	The voltage reference inputs for the four DACs. The allowed range is 0V–2.75V.
$\overline{CS}$(9)	The Chip Select control input. This input is active low.
CLK(8)	The external clock input pin.
DI(10)	The serial data input. The data is clocked in MSB first. Preceding the data byte are 4 or 6 bits of instructions. The read back command requires 7 bits of instructions.
DO(7)	The serial data output. The data can be clocked out either MSB or LSB first, and on either the positive or negative edge of the clock.
$\overline{INT}$(12)	The power interrupt output. On an interruption of the digital power supply, this pin goes low. Since this pin has an open drain output, a 10 kΩ pull-up resistor must be connected to the supply.

Applications Information

FUNCTIONAL DESCRIPTION

The DAC1054 is a monolithic quad 10-bit digital-to-analog converter that is designed to operate on a single 5V supply. Each of the four units is comprised of an input register, a DAC register, a shift register, a current output DAC, and an output amplifier. In addition, the DAC1054 has an onboard bandgap reference and a logic unit which controls the internal operation of the DAC1054 and interfaces it to microprocessors.

Each of the four internal 10-bit DACs uses a modified R-2R ladder to effect the digital-to-analog conversion *(Figure 5).* The resistances corresponding to the 2 most significant bits are segmented to reduce glitch energy and to improve matching. The bottom of the ladder has been modified so that the voltage across the LSB resistor is much larger than the input offset voltage of the buffer amplifier. The input digital code determines the state of the switches in the ladder network. An internal EEPROM, which is programmed at the factory, is used to correct for linearity errors in the resistor ladder of each of the four internal DACs. The codes stored in the EEPROM's memory locations are converted to a current, I_{EEPROM}, with a small trim DAC. The sum of currents I_{OUT1} and I_{OUT2} is fixed and is given by

$$I_{OUT1} + I_{OUT2} = \left(\frac{V_{REF} - V_{BIAS}}{R}\right)\frac{1023}{1024}$$

The current output I_{OUT2}, summed with the correction current I_{EEPROM}, is applied to the internal output amplifier and converted to a voltage. The output voltage of each DAC is a function of V_{BIAS}, V_{REF}, and the digital input word, and is given by

$$V_{OUT} = 2\,(V_{REF} - V_{BIAS})\,\frac{DATA}{1024} + \frac{2047}{512}\,V_{BIAS} - \frac{1023}{512}\,V_{REF}$$

The output voltage range for each DAC is 0.3V−2.8V. This range can be achieved by using the internal 2.65V reference and a voltage divider network which provides a V_{BIAS} of 1.40V *(Figure 6).* In this case the DAC transfer function is

$$V_{OUT} = 2.5\,\frac{(DATA)}{1024} + 0.30244$$

The output impedance of any external reference that is used will affect the accuracy of the conversion. In order that this error be less than ½ LSB, the output impedance of the external reference must be less than 2Ω.

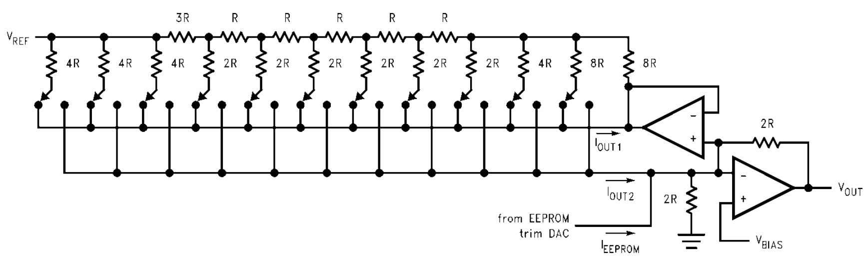

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FIGURE 5. Equivalent Circuit of R-2R Ladder and Output Amplifier

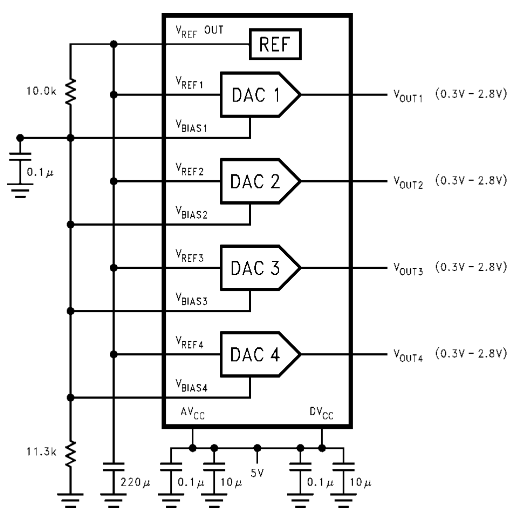

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FIGURE 6. Generating a V_{BIAS} = 1.40V from the Internal Reference, Typical Application

Digital Interface

The DAC1054 has two interface modes: a WRITE mode and a READ mode. The WRITE mode is used to convert a 10-bit digital input word into a voltage. The READ mode is used to read back the digital data that was sent to one or all of the DACs. The WRITE mode maximum clock rate is 10 MHz. READ mode is limited to a 5 MHz maximum clock rate. These modes are selected by the appropriate setting of the RD/$\overline{WR}$ bit, which is part of the instruction byte. The instruction byte precedes the data byte at the DI pin. In both modes, a high level on the Start Bit (SB) alerts the DAC to respond to the remainder of the input stream.

Table I lists the instruction set for the WRITE mode when writing to only a single DAC, and Table II lists the instruction set for a global write. Bits A0 and A1 select the DAC to be written to. The DACs are always written to MSB first. All DACs will be written to sequentially if the global bit (G) is high; DAC 1 is written to first, then DACs 2, 3 and 4 (in that order). For a global write bits A0 and A1 of the instruction byte are not required (see *Figure 2* timing diagram). If the update bit (U) is high, then the DAC output(s) will be updated on the rising edge of $\overline{CS}$; otherwise, the new data byte will be placed only in the input register. Chip Select ($\overline{CS}$) must remain low for at least one clock cycle after the last data bit has been entered. (See *Figures 1* and *2*)

When the U bit is set low an asynchronous update of all the DAC outputs can be achieved by taking $\overline{AU}$ low. The contents of the input registers are loaded into the DAC registers, with the update occurring on the falling edge of $\overline{AU}$. $\overline{CS}$ must be held high during an asynchronous update.

All DAC registers will have their contents reset to all zeros on power up.

TABLE I. WRITE Mode Instruction Set (Writing to a Single DAC)

SB	RD/$\overline{WR}$	G	U	A1	A0	Description
Bit #1	Bit #2	Bit #3	Bit #4	Bit #5	Bit #6	
1	0	0	0	0	0	Write DAC 1, no update of DAC outputs
1	0	0	0	0	1	Write DAC 2, no update of DAC outputs
1	0	0	0	1	0	Write DAC 3, no update of DAC outputs
1	0	0	0	1	1	Write DAC 4, no update of DAC outputs
1	0	0	1	0	0	Write DAC 1, update DAC 1 on $\overline{CS}$ rising edge
1	0	0	1	0	1	Write DAC 2, update DAC 2 on $\overline{CS}$ rising edge
1	0	0	1	1	0	Write DAC 3, update DAC 3 on $\overline{CS}$ rising edge
1	0	0	1	1	1	Write DAC 4, update DAC 4 on $\overline{CS}$ rising edge

TABLE II. WRITE Mode Instruction Set (Writing to all DACs)

SB	RD/$\overline{WR}$	G	U	Description
Bit # 1	Bit #2	Bit #3	Bit #4	
1	0	1	0	Write all DACs, no update of outputs
1	0	1	1	Write all DACs, update all outputs on $\overline{CS}$ rising edge

Digital Interface (Continued)

Table III lists the instruction set for the READ mode. By the appropriate setting of the global (G) and address (A1 and A0) bits, one can select a specific DAC to be read, or one can read all the DACs in succession, starting with DAC 1. The R/$\overline{F}$ bit determines whether the data changes on the rising or the falling edge of the system clock. With the R/$\overline{F}$ bit high, DO goes out of TRI-STATE on the rising edge that occurs 1½ clock cycles after the end of the instruction byte; the data will continue to be sequentially clocked out by the following rising clock edges. With the R/$\overline{F}$ bit low, DO goes out of TRI-STATE on the falling edge that occurs 1 clock cycle after the end of the instruction byte; the data will continue to be sequentially clocked by the next falling clock edges. The rising edge of $\overline{CS}$ returns DO to TRI-STATE. Read back with the R/$\overline{F}$ bit set high is not MICROWIRE compatible. One can choose to read the data back MSB first or LSB first by setting the M/$\overline{L}$ bit. (See *Figures 3* and *4*)

TABLE III. READ MODE Instruction Set

SB	RD/$\overline{WR}$	G	R/$\overline{F}$	M/$\overline{L}$	A1	A0	Description
Bit #1	Bit #2	Bit #3	Bit #4	Bit #5	Bit #6	Bit #7	
1	1	0	0	0	0	0	Read DAC 1, LSB first, data changes on the falling edge
1	1	0	0	0	0	1	Read DAC 2, LSB first, data changes on the falling edge
1	1	0	0	0	1	0	Read DAC 3, LSB first, data changes on the falling edge
1	1	0	0	0	1	1	Read DAC 4, LSB first, data changes on the falling edge
1	1	0	0	1	0	0	Read DAC 1, MSB first, data changes on the falling edge
1	1	0	0	1	0	1	Read DAC 2, MSB first, data changes on the falling edge
1	1	0	0	1	1	0	Read DAC 3, MSB first, data changes on the falling edge
1	1	0	0	1	1	1	Read DAC 4, MSB first, data changes on the falling edge
1	1	0	1	0	0	0	Read DAC 1, LSB first, data changes on the rising edge
1	1	0	1	0	0	1	Read DAC 2, LSB first, data changes on the rising edge
1	1	0	1	0	1	0	Read DAC 3, LSB first, data changes on the rising edge
1	1	0	1	0	1	1	Read DAC 4, LSB first, data changes on the rising edge
1	1	0	1	1	0	0	Read DAC 1, MSB first, data changes on the rising edge
1	1	0	1	1	0	1	Read DAC 2, MSB first, data changes on the rising edge
1	1	0	1	1	1	0	Read DAC 3, MSB first, data changes on the rising edge
1	1	0	1	1	1	1	Read DAC 4, MSB first, data changes on the rising edge
1	1	1	0	0	1	0	Read all DACs, LSB first, data changes on the falling edge
1	1	1	0	1	1	0	Read all DACs, MSB first, data changes on the falling edge
1	1	1	1	0	1	0	Read all DACs, LSB first, data changes on the rising edge
1	1	1	1	1	1	0	Read all DACs, MSB first, data changes on the rising edge

Power Fail Function

The DAC1054 powers up with the $\overline{INT}$ pin in a Low state. To force this output high and reset this flag, the $\overline{CS}$ pin will have to be brought low. When this is done the $\overline{INT}$ output will be pulled high again via an external 10 kΩ pull-up resistor. Any-time a power failure occurs on the DV_{CC} line, the $\overline{INT}$ will be set low when power is reapplied. This feature may be used by the microprocessor to discard data whose integrity is in question.

Power Supplies

The DAC1054 is designed to operate from a +5V (nominal) supply. There are two supply lines, AV_{CC} and DV_{CC}. These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To guarantee accurate conversions, the two supply lines should each be bypassed with a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor.

Typical Applications

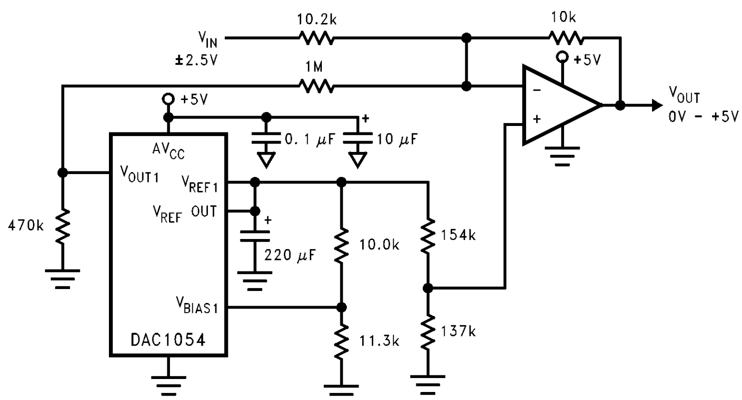

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FIGURE 7. Trimming the Offset of a 5V Op Amp Whose Output is Biased at 2.5V

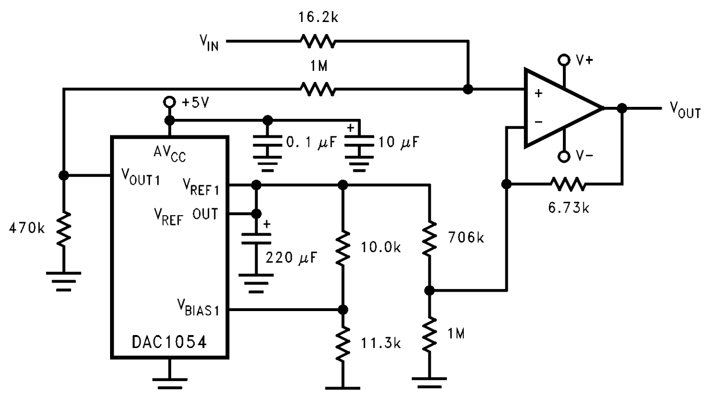

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FIGURE 8. Trimming the Offset of a Dual Supply Op Amp (V_{IN} is Ground Referenced)

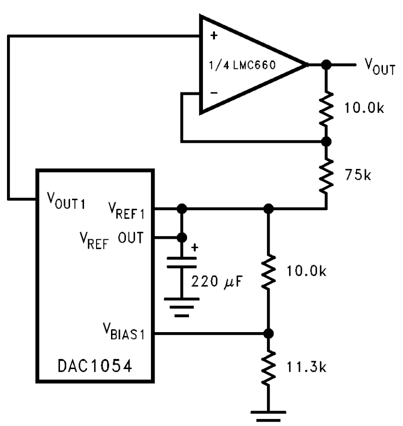

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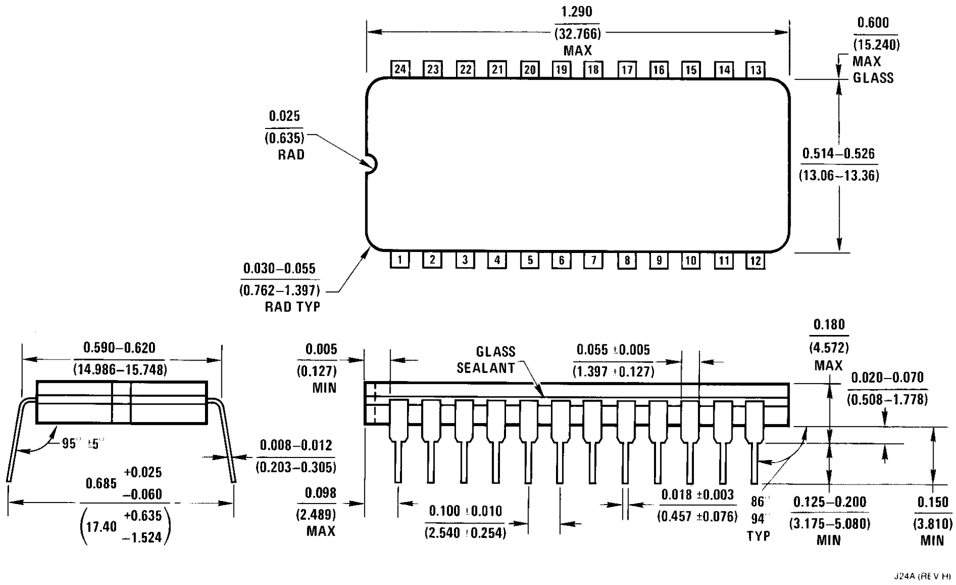
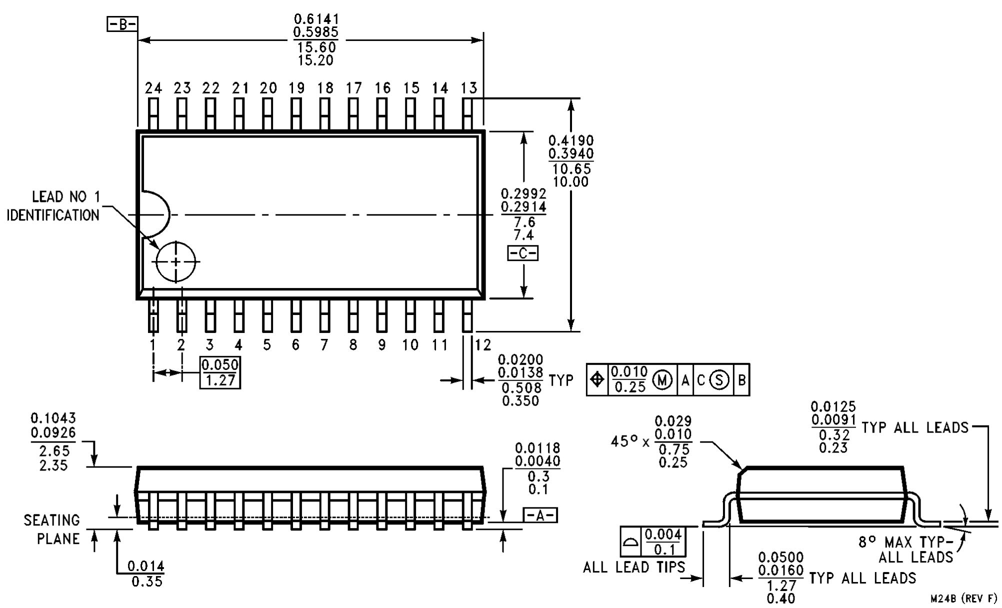
FIGURE 9. Bringing the Output Range Down to Ground

Physical Dimensions inches (millimeters)



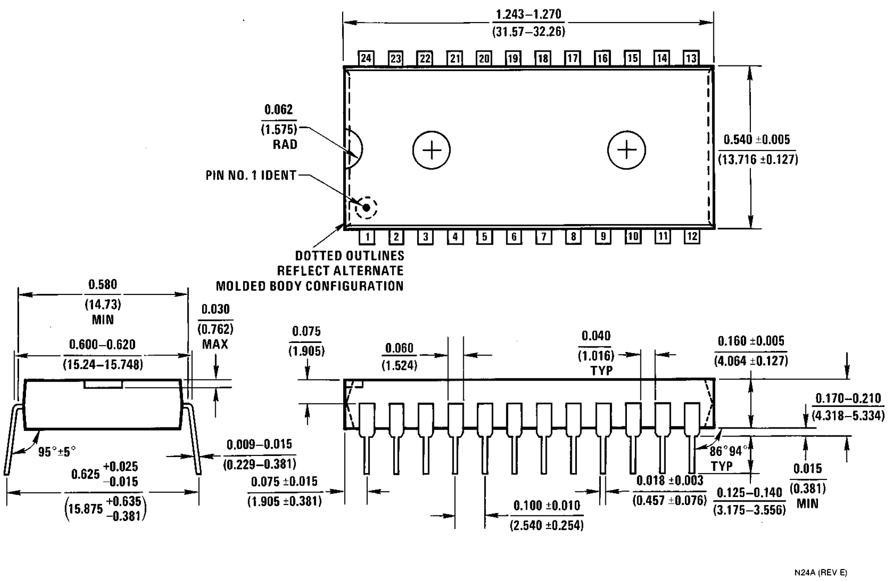
Order Number DAC1054CMJ/883 or 5962-9466201MJA
NS Package Number J24A



Order Number DAC1054CIWM
NS Package Number M24B

Physical Dimensions inches (millimeters) (Continued)

Lit. # 02236



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