National Semiconductor

DAC1265A/DAC1265 Hi-Speed 12-Bit D/A Converter with Reference

General Description

The DAC1265A and DAC1265 are fast 12-bit digital to analog converters with internal voltage reference. These DACs use 12 precision high speed bipolar current steering switches, control amplifier, thin film resistor network, and buried zener voltage reference to obtain a high accuracy, very fast analog output current. The DAC1265A and DAC1265 have 10%–90% full-scale transition time under 35 ns and settle to less than ½ LSB in 200 ns. The buried zener reference has long-term stability and temperature drift characteristics comparable to the best discrete or separate IC references.

These digital to analog converters are recommended for applications in CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 5 MHz for full range transitions.

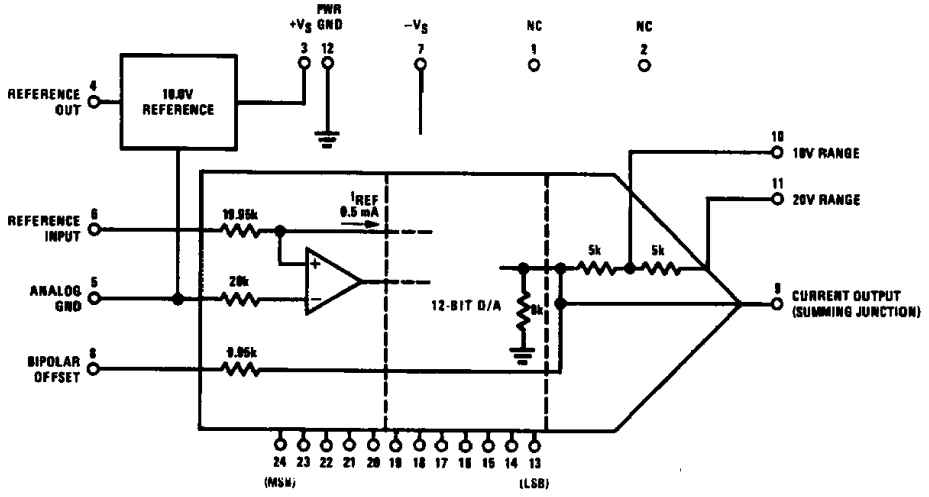
Features

- Bipolar current output DAC and voltage reference
- Fully differential, non-saturating precision current switch — R_{OUT} and C_{OUT} do not change with digital input code.
- Internal buried zener reference — 10V ± 1% max
- Precision thin film resistors for use with external op amp for voltage out or as input resistors for a successive approximation A/D converter
- Superior replacement for 12-bit D/A converters of this type

Key Specifications

- Resolution and Monotonicity — 12 Bits
- Linearity — 12 Bits
  (Guaranteed over temperature)
- Output Current Settling Time — 400 ns max to 0.01%
- Gain Tempco — ± 15 ppm/°C max
- Power Supply Sensitivity — ± 10 ppm of FS/% V_{SUPPLY}

Block and Connection Diagrams



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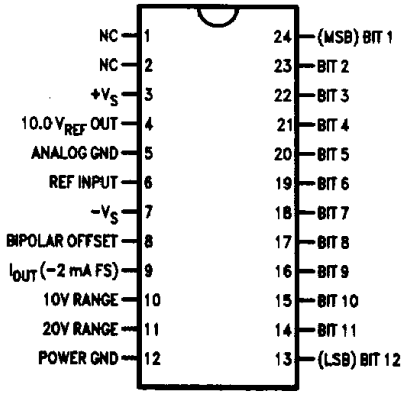
Dual-In-Line Package



Top View

Order Number DAC1265AJ, DAC1265ACJ, DAC1265LJ or DAC1265LCJ
See NS Package Number J24A

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V^+ and V^-)	±18V
Current Output (Pin 9) Voltage	−3V, 12V
Logic Input Voltage	−1V, 7V
Reference Input Voltage (Pin 6)	±12V
Analog GND to Power GND	±1V
Bipolar Offset	±12V
10V Range	±12V
20V Range	V^- to +24V
Power Dissipation (Note 1)	1000 mW
Short-Circuit Duration (Pins 4 to 12)	Continuous
Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC1265AJ, DAC1265LJ	−55°C to +125°C
DAC1265ACJ, DAC1265LCJ	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Susceptibility (Note 13)	TBD

Electrical Characteristics

$V_{SUPPLY} = \pm 15V \pm 5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter	Conditions	See Note	DAC1265A			DAC1265			Units
			Typ (Note 11)	Tested Limit (Note 2)	Design Limit (Note 3)	Typ (Note 11)	Tested Limit (Note 2)	Design Limit (Note 3)	
CONVERTER CHARACTERISTICS									
Resolution				12			12		Bits
Linearity Error Max	Zero and Full-Scale Adjusted AJ and LJ Suffix Parts ACJ and LCJ Suffix Parts	4	±⅛	±¼ ±½	±½	±¼	±½ ±¾	±¾	LSB
Differential Non-Linearity Max	Zero and Full-Scale Adjusted		±¼	±½		±½	±¾		
Monotonicity	AJ and LJ Suffix Parts ACJ and LCJ Suffix Parts			**12** 12	**12**		**12** 12	**12**	Bits
Full-Scale (Gain) Error Max	R2 = 50Ω in *Figure 1*	5	±0.1	±0.20		±0.1	±0.20		% Full-Scale
Offset Error Max All Bits OFF, Logic "0"	Unipolar (*Figure 1* Pin 8 Open)	6	±0.01	±0.05		±0.01	±0.05		
	Bipolar (R1 and R2 = 50Ω in *Figure 2*)	7	±0.05	±0.1		±0.05	±0.15		
Zero Error Max MSB ON	Bipolar (R1 and R2 = 50Ω in *Figure 2*)	8	±0.05	±0.1		±0.05	±0.15		
Gain Adjustment Range Min	R2 = 50Ω ± 50Ω in *Figure 1*			±0.2			±0.2		
Bipolar Offset Adjustment Range Min	R1 = 50Ω ± 50Ω and R2 = 50Ω in *Figure 2*			±0.15			±0.15		
Full-Scale (Gain) Temperature Coefficients Max	Using the Internal Reference: AJ and LJ Suffix	9	10	**15**		15	**30**		ppm/°C
	Using the Internal Reference: ACJ and LCJ Suffix		10		**20**	15		**50**	
Unipolar Offset Temperature Coefficients Max	AJ and LJ Suffix		**1**	**2**		1	**2**		
	ACJ and LCJ Suffix		1		**2**	1		**2**	
Bipolar Zero Temperature Coefficients Max	AJ and LJ Suffix		5	**10**		5	**10**		
	ACJ and LCJ Suffix		5		**10**	5		**10**	
Output Resistance	Exclusive of Offset and Range R_S		7.5	6 to 10		7.5	6 to 10		kΩ

Electrical Characteristics (Continued) $V_{SUPPLY} = \pm 15V \pm 5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter		Conditions	See Note	DAC1265A Typ (Note 11)	DAC1265A Tested Limit (Note 2)	DAC1265A Design Limit (Note 3)	DAC1265 Typ (Note 11)	DAC1265 Tested Limit (Note 2)	DAC1265 Design Limit (Note 3)	Units
Current Output		Unipolar		−2	−1.6 to −2.4		−2	−1.6 to −2.4		mA
		Bipolar		±1.0	±0.8 to ±1.2		±1.0	±0.8 to ±1.2		
Output Capacitance				25			25			pF
Output Noise (FS, 10V Range)		10 Hz to 100 kHz with Internal Reference		40			40			μVrms
Typ Output Voltage Ranges		Using Internal Offset and Range R_S		±2.5, ±5, ±10, 0 to 5, 0 to 10						V
Reference Input Resistance				20.8	15 to 25		20.8	15 to 25		kΩ
Output Compliance Voltage						**−1.5 to 10**			**−1.5 to 10**	V
REFERENCE OUTPUT CHARACTERISTICS										
Reference Voltage	Min	$I_{REF} = 1.5$ mA		10.00	9.90		10.00	9.90		V
	Max				10.10			10.10		
Temperature Coefficient				±8			±12			ppm/°C
Reference Output Current Min					3.0			3.0		mA
Output Resistance Max		$f_O = 1$ kHz, 0.5 mA ≤ I_{REF} ≤ 3 mA		0.05	1.0		0.05	1.0		Ω
DIGITAL AND DC CHARACTERISTICS										
Logic Input Voltage		Logic High Bit ON — AJ and LJ Suffix			**2 to 5.5**			**2 to 5.5**		V
		Logic High Bit ON — ACJ and LCJ Suffix			1.9 to 5.5	**2 to 5.5**		1.9 to 5.5	**2 to 5.5**	
	Max	Logic Low Bit OFF — AJ and LJ Suffix			**0.8**			**0.8**		
		Logic Low Bit OFF — ACJ and LCJ Suffix			1.0	**0.8**		1.0	**0.8**	
Logic Input Current Max		Logic High — AJ and LJ Suffix		150	**300**		150	**300**		μA
		Logic High — ACJ and LCJ Suffix		150	280	**300**	150	280	**300**	
		Logic Low — AJ and LJ Suffix		45	**100**		45	**100**		
		Logic Low — ACJ and LCJ Suffix		45	90	**100**	45	90	**100**	
Power Supply Current Max	I^+	V^+ Supply = 15V ± 10%		3	5		3	5		mA
	I^-	V^- Supply = −15V ± 10%		−12	−18		−12	−18		
Power Dissipation Max		$V_{SUPPLY} = \pm 15V$		225	345		225	345		mW
Power Supply Sensitivity Max		V^+ Supply = 15V ± 10%	10	±3	±10		±3	±10		ppm of FS/% V_{SUPPLY}
		V^- Supply = −15V ± 10%	10	±15	±25		±15	±25		

Electrical Characteristics (Continued) $V_{SUPPLY} = \pm 15V \pm 5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter	Conditions	See Note	DAC1265A			DAC1265			Units
			Typ (Note 11)	Tested Limit (Note 2)	Design Limit (Note 3)	Typ (Note 11)	Tested Limit (Note 2)	Design Limit (Note 3)	
AC CHARACTERISTICS									
Settling Time Max	FSR Change		200		400	200		400	ns
Full-Scale Transition Max	10% to 90% Rise Time Plus Delay Time		15		30	15		30	ns
	90% to 10% Fall Time Plus Delay Time		30		50	30		50	

Note 1: The typical θ_{JA} of the 24-pin package is 80° C/W.

Note 2: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 3: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 4: Linearity error $= \frac{V_{OUT} - V_{OFFSET} - (D \times V_{LSB})}{V_{LSB}}$ where $V_{LSB} = \frac{V_{FS} - V_{OFFSET}}{4095}$ and D is the digital input (0 to 4095) which produced V_{OUT}.

Note 5: Percent gain error for 10V range $= \frac{(V_{FS} - V_{OFFSET}) - (4095/4096)10V}{10V} \times 100$.

Note 6: Unipolar offset error for 10V range $= (V_{OUT}/10V) \times 100$ in percent of full-scale.

Note 7: Bipolar offset error for 10V range $= \frac{V_{OUT} - (-5V)}{10V} \times 100$ in percent of full-scale.

Note 8: Bipolar zero error for 10V range $= (V_{OUT}/10V) \times 100$ in percent of full-scale.

Note 9: Gain error tempco $= \frac{(V_{FS} - V_{OFFSET}) \text{at } (T_{MAX} \text{ or } T_{MIN}) - (V_{FS} - V_{OFFSET}) \text{ at } 25°C}{10V \text{ range} \times (T_{MAX} \text{ or } T_{MIN} - 25°C)} \times 10^6$ in ppm/°C.

Note 10: Power supply sensitivity for 10V range $= 10^6 \times \frac{(V_{FS} - V_{OFFSET}) \text{ at } (16.5V \text{ or } -13.5V) - (V_{FS} - V_{OFFSET}) \text{ at } (13.5V \text{ or } -16.5V)}{10V \times 20\%}$ in ppm of FS/%V_S.

The opposite supply is held at −15V or +15V respectively.

Note 11: Typicals are at 25°C and represent most likely parametric norm.

Note 12: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 13: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description and Applications

1.0 BUFFERED VOLTAGE OUTPUT CONNECTION

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (LF401A) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5 mV maximum offset voltage should be used to keep offset errors below ½ LSB). Unipolar zero will typically be within ± ½ LSB (plus op amp offset), and if a 50Ω fixed resistor is substituted for the 100Ω trimmer (R2, *Figure 1*), full-scale accuracy will be within 0.1% (0.20% maximum). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer (R1, *Figure 2*) will give a bipolar zero error typically within ±2 LSB (0.05%).

1.1 Unipolar Configuration *(Figure 1)*

This configuration will provide a unipolar 0V to 9.9976V output range.

Step 1—Offset Adjust (Zero)

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000V (1 LSB = 2.44 mV). In most cases this trim is not needed.

Step 2—Gain Adjust

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976V (full-scale adjusted to 1 LSB less than nominal full-scale of 10.000V). If a 10.2375V full-scale is desired (exactly 2.5 mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

1.2 Bipolar Configuration *(Figure 2)*

This configuration will provide a bipolar output voltage from — 5.000V to 4.9976V, with positive full-scale occurring with all bits ON (all 1s).

Step 1—Offset Adjust

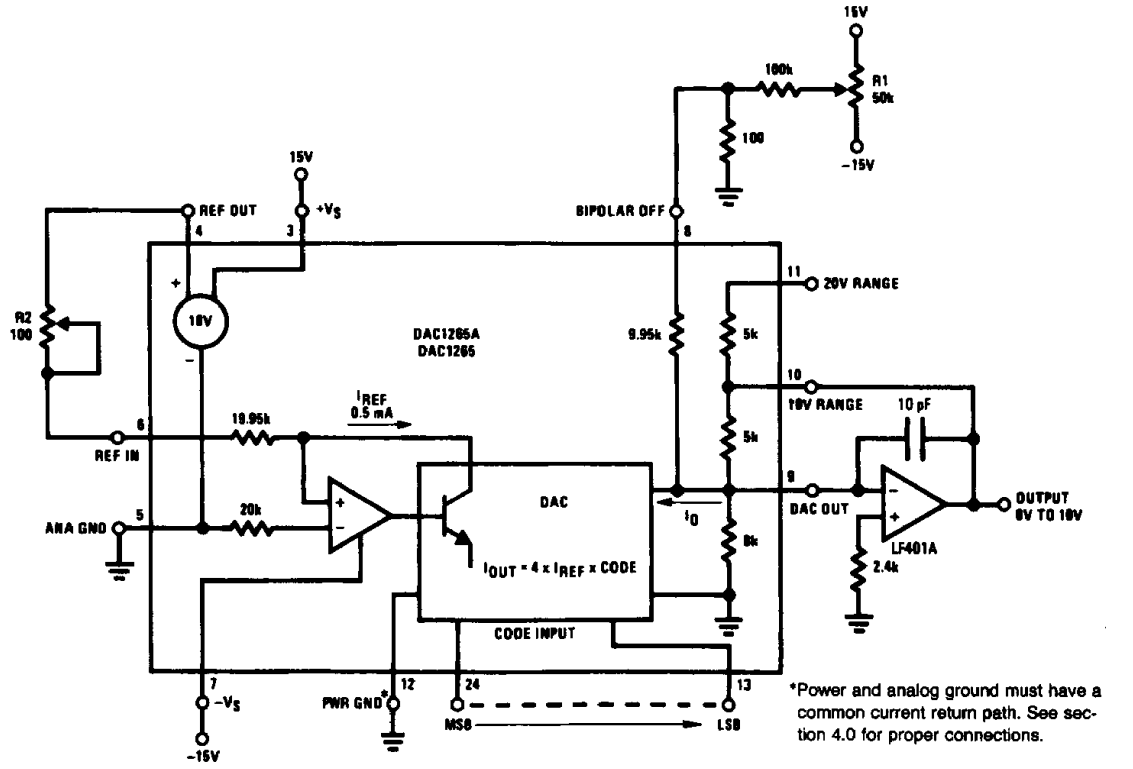
Turn OFF all bits. Adjust 100Ω offset trimmer, R1, to give −5.000V output.

Step 2—Gain Adjust

Turn ON all bits. Adjust 100Ω gain trimmer, R2, to give a reading of 4.9976V.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive. Bipolar zero error (MSB bit ON) is not adjusted separately and is typically < ±0.05% of FS after offset and gain adjust.

Functional Description and Applications (Continued)



*Power and analog ground must have a common current return path. See section 4.0 for proper connections.

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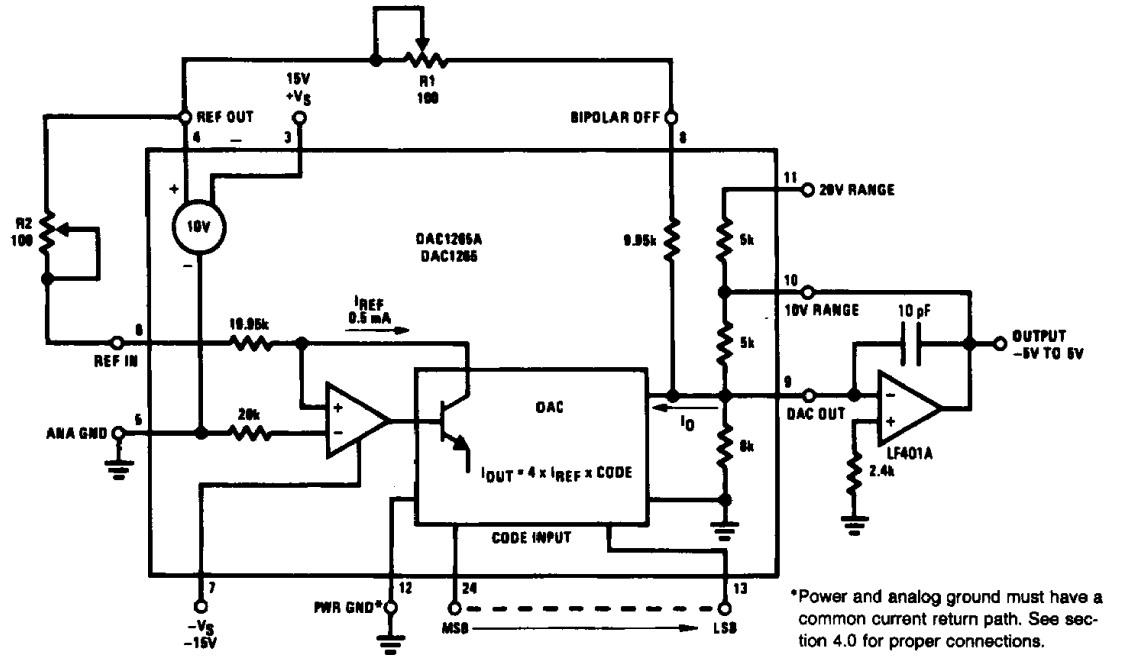
FIGURE 1. 0V to 10V Unipolar Voltage Output



*Power and analog ground must have a common current return path. See section 4.0 for proper connections.

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FIGURE 2. ±5V Bipolar Voltage Output

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Functional Description and Applications (Continued)

1.3 Other Voltage Ranges *(Figure 3)*

The DAC1265A and DAC1265 can also be easily configured for a unipolar 0V to 5V range or ±2.5V and ±10V bipolar ranges by using the additional 5k application resistor provided at the 20V range R terminal, pin 11. For a 5V range (0V to 5V or ±2.5V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either left open for unipolar or connected through a 100Ω pot to the REF OUT for the bipolar range. For the ± 10V range use the 5k resistors in series by connecting only pin 11 to the op amp output and connecting the bipolar offset as shown. The ±10V option is shown in *Figure 3*.

2.0 INTERNAL/EXTERNAL REFERENCE USE

The performance of the DAC1265A and DAC1265 is specified with the internal reference driving the DAC since all trimming and testing (especially for full-scale error and bipolar operation) is done in this configuration.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5 mA to REF IN and 1.0 mA to BIPOLAR OFFSET, if used). A minimum of 1.5 mA is available for driving external circuits. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% maximum error. The temperature coefficient is comparable to that of the full-scale TC for a particular grade.

3.0 DIGITAL INPUT

The DAC1265A and DAC1265 use a standard positive true straight binary code for unipolar outputs (all 1s give full-scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all 0s on the inputs, the output will go to negative full-scale; with 100...00 (only the MSB on), the output will be 0.00V; with all 1s, the output will go to positive full-scale.

The threshold of the digital input circuitry is set at 1.4V and does not vary with supply voltage. The input lines can interface with any type of 5V logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in *Figure 4*. The input line can be modeled as a 30 kΩ resistance connected to a −0.7V rail.

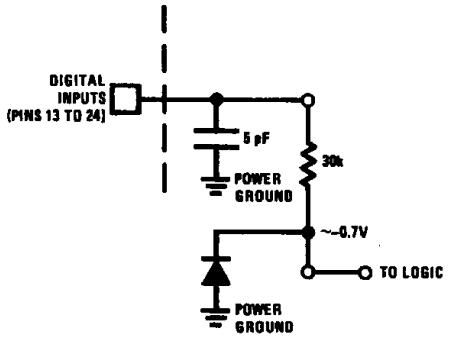

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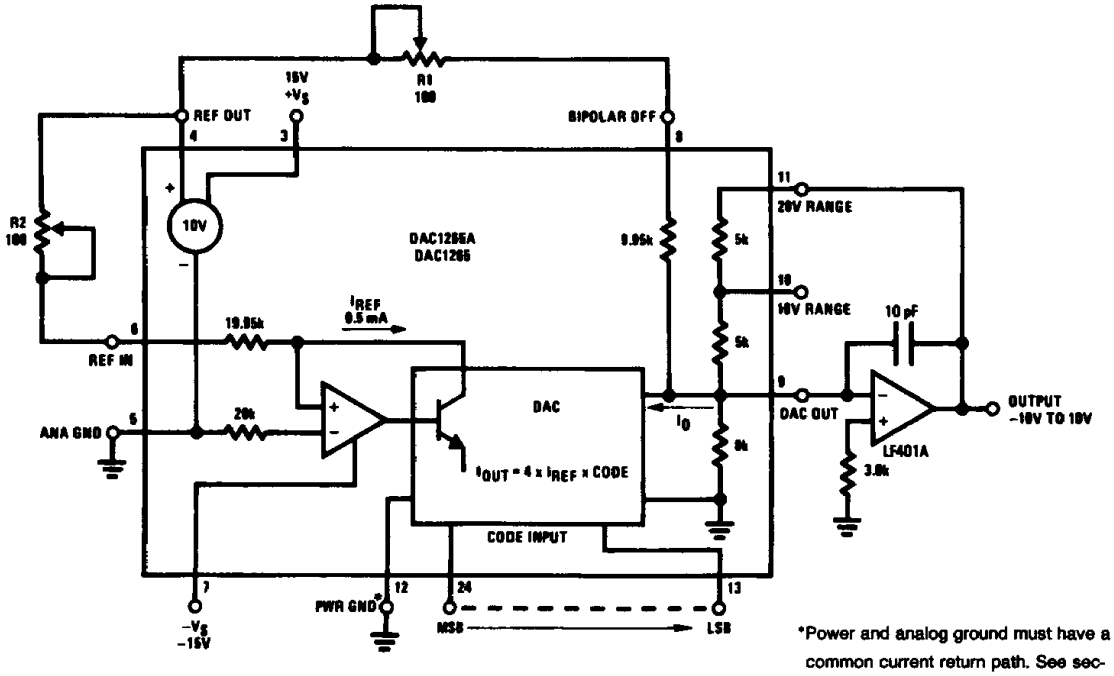
FIGURE 4. Equivalent Digital Input Circuit



*Power and analog ground must have a common current return path. See section 4.0 for proper connections.

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FIGURE 3. ±10V Voltage Output

Functional Description and Applications (Continued)

4.0 APPLICATION OF ANALOG AND POWER GROUNDS

The DAC1265A and DAC1265 have separate analog and power ground pins to allow optimum connections for low noise and high speed performance. The two ground lines can be separated by up to 200 mV without any loss in performance. There may be some loss in linearity beyond that level. If these DACs are to be used in a system in which the two grounds will be ultimately connected at some distance from the device, it is recommended that parallel back-to-back diodes be connected between the ground lines near the device to prevent a fault condition.

The analog ground at pin 5 is the ground reference point for the internal reference and is thus the "high quality" ground; it should be connected directly to the analog reference point of the system. The power ground at pin 12 can be connected to the most convenient ground reference point; analog power return is preferred, but digital ground is acceptable. If power ground contains high frequency noise beyond 200 mV, this noise may feed through the converter, so that some caution will be required in applying these grounds.

5.0 OUTPUT VOLTAGE COMPLIANCE

The DAC1265A and DAC1265 have a typical output compliance range from −2V to 10V. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8k in parallel with 25 pF at the output terminal which produces an equivalent error current if the voltage deviates from power ground. This is a linear effect that does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in non-linear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply.

6.0 DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. *Figure 5* shows a connection using the gain and bipolar output resistors to give a ±1.60V bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 mA to −2 mA unipolar output current and using the 10.0V reference voltage for bipolar offset. For example, setting $R_X = 2.67\ k\Omega$ gives a ±1V range with a 1 kΩ equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. Using a 50Ω resistor for R_X would allow interface to a 50Ω cable with a ±50 mV full-scale swing.

7.0 HIGH SPEED 12-BIT A/D CONVERTERS

The fast settling characteristics of the DAC1265A and DAC1265 make them ideal for high speed successive approximation A/D converters. The internal reference and trimmed internal resistors allow a 12-bit converter system to be constructed with a minimum parts count. Shown in *Figure 6* is a configuration using standard components; this system completes a full 12-bit conversion in 10 μs unipolar or bipolar. This converter will be accurate to ±½ LSB of 12 bits and have a typical gain TC of 10 ppm/°C.

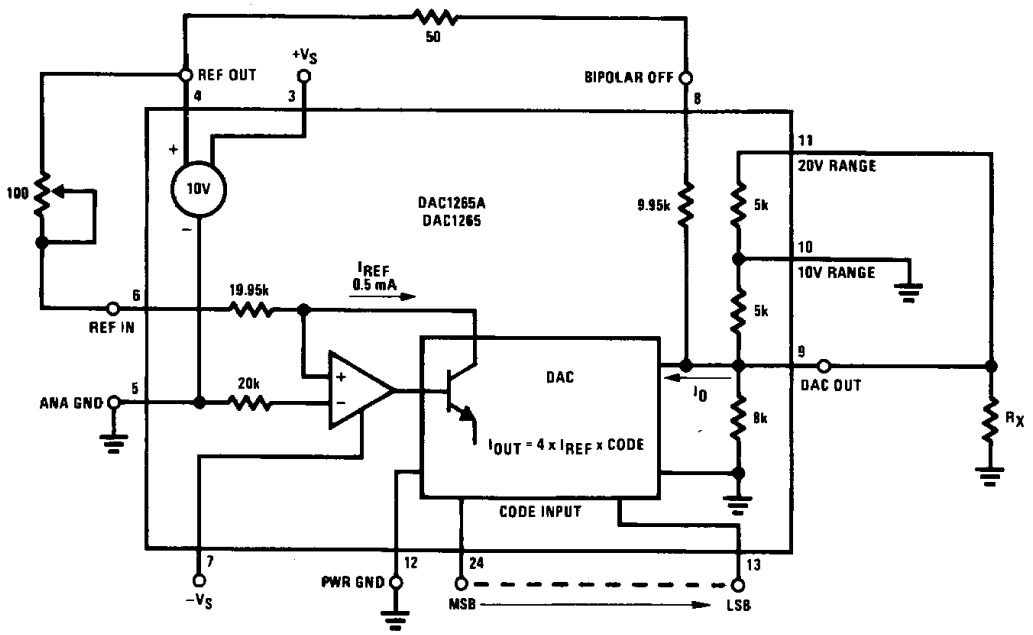

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FIGURE 5. Unbuffered Bipolar Voltage Output

Functional Description and Applications (Continued)

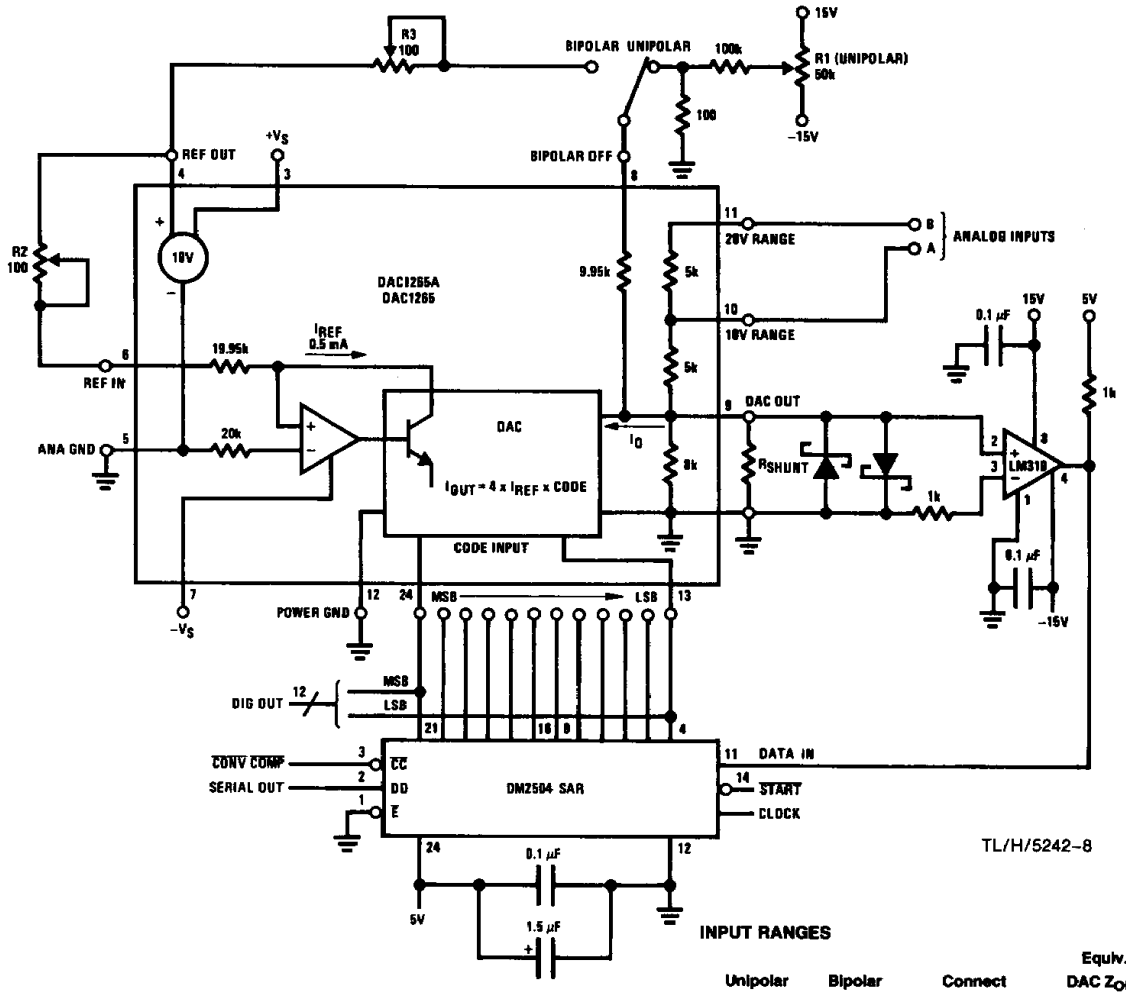
In the unipolar mode, the system range is 0V to 9.9976V, with each bit having a value of 2.44 mV. For true conversion accuracy, an A/D converter should be trimmed so that a given output code results from input levels from ½ LSB below to ½ LSB above the exact voltage represented by that code. Therefore, the converter zero point should be trimmed with an input voltage of 1.22 mV; trim R1 until the LSB just begins to appear in the output code (all other bits "0"). For full-scale, use an input voltage of 9.9963V (10V-1 LSB-½ LSB); then trim R2 until the LSB just begins to appear (all other bits "1").

The bipolar signal range is −5.0V to 4.9976V. Bipolar offset trimming is done by applying a −4.9988V input signal and trimming R3 for the LSB transition (all other bits "0").

Full-scale is set by applying 4.9963V and trimming R2 for the LSB transition (all other bits "1"). In many applications, the pretrimmed internal resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 12-bit ±½ LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance at the summing node of 1 kΩ, 1 LSB = 0.5 mV), to the point that comparator performance will be sacrificed. The contribution to this impedance from the DAC will vary with the input configuration (*Figure 6,* Input Ranges Table).

To prevent dynamic errors, the input signal should have a low dynamic source impedance, such as that of the LF411A op amp.



INPUT RANGES

Unipolar	Bipolar	Connect	Equiv. DAC Z_{OUT}
0 to 5	±2.5	Input to A B to DAC OUT	1.60 kΩ
0 to 10	±5	Input to A	2.35 kΩ
0 to 20	±10	Input to B	3.08 kΩ

FIGURE 6. Fast Precision Analog to Digital Converter

Definition of Terms

Digital Inputs: The DAC1265A and DAC1265 accept digital input codes in binary format and may be user connected for any one of three binary codes: straight binary, two's complement, or offset binary.

Digital Input MSB LSB	Analog Output		
	Straight Binary	Offset Binary	Two's Complement*
000..000	zero	−FS (Full-Scale)	zero
011...111	½ FS−1 LSB	zero−1 LSB	+FS−1 LSB
100..000	½ FS	zero	−FS
111...111	+FS−1 LSB	+FS−1 LSB	zero−1 LSB

*Invert MSB with external inverter to obtain Two's Complement coding

Linearity Error: Linearity error of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full-scale (all bits ON).

Differential Non-Linearity: For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one-bit change in code. A differential non-linearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input. It is guaranteed by testing the major carry transitions, i.e., 100...000 to 011...111, etc.

Settling Time: Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full-scale or major carry transition.

Gain Tempco: The change in full-scale analog output over the specified temperature range expressed in parts per million of full-scale per °C (ppm of FS/°C). Gain error is measured with respect to 25°C at high (T_{MAX}) and low (T_{MIN}) temperatures. Gain tempco is calculated for both high ($T_{MAX}-25°C$) and low ($25°C-T_{MIN}$) ranges by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst-case drift.

Offset Tempco: The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full-scale per °C (ppm of FS/°C). Offset error is measured with respect to 25°C at high (T_{MAX}) and low (T_{MIN}) temperatures. Offset tempco is calculated for both high ($T_{MAX}-25°C$) and low ($25°C-T_{MIN}$) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

Power Supply Sensitivity: Power supply sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in −15V or + 15V supplies. It is specified under DC conditions and expressed as parts per million of full-scale per percent of change in power supply (ppm of FS/%).

Ordering Information

Temperature Range		0°C to 70°C	−55°C to + 125°C
Linearity Error Over Temperature	±½ Bit	DAC1265ACJ	DAC1265AJ
	±¾ Bit	DAC1265LCJ	DAC1265LJ

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